A 4×Two-Way mm-Wave Doherty CMOS PA

Kumaran, Anil Kumar; Wu, Yizhuo; Pashaeifar, Masoud; Nachouane, Hamza; Gao, Chang; Cornelis Nicolaas de Vreede, Leonardus; Alavi, Morteza S.

DOI
10.1109/TMTT.2025.3569155

Publication date
2025

Document Version
Final published version

Published in
IEEE Transactions on Microwave Theory and Techniques

A 4×Two-Way mm-Wave Doherty CMOS PA

Anil Kumar Kumaran, *Graduate Student Member, IEEE*, Yizhuo Wu, *Graduate Student Member, IEEE*, Masoud Pashaeifar, *Member, IEEE*, Hamza Nachouane, *Member, IEEE*, Chang Gao, *Member, IEEE*, Leonardus Cornelis Nicolaas de Vreede, *Senior Member, IEEE*, and Morteza S. Alavi, *Senior Member, IEEE*

***Abstract*—This article introduces a 4 × 2-way Doherty power amplifier (PA) tailored for millimeter-wave (mm-wave) 5G applications. It incorporates an advanced output combiner that consists of four differential 2-way Doherty networks, two quadrature hybrid couplers (QHCs), and a balun to enhance the output power P_{out} and improves power back-off (PBO) efficiency. Realized in 40 nm CMOS bulk technology with a core area of 1.54 mm^2, the prototype delivers a saturated power/peak gain surpassing 25.2 dBm/25.5 dB, and it demonstrates a drain efficiency (DE) exceeding 17.5%/10% at 0 dB/6 dB PBO across a 26–32 GHz band. The proposed mm-wave PA achieves error vector magnitude (EVM)/adjacent channel leakage ratio (ACLR) values of −25 dB/−33 dBc for a 2 GHz 64-quadrature amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM) signal with 9.6 dB PAPR, operating at an average output power (P_{avg}) of 11.3 dBm with an average drain efficiency (DE_{avg}) of 4% without using digital predistortion (DPD). For a 50 MHz 1024-QAM OFDM signal with 10 dB PAPR, it achieves a P_{avg}/DE_{avg} of 7.2 dBm/2% with EVM/ACLR of −35 dB/−42 dBc without DPD.**

***Index Terms*—Adaptive biasing, artificial intelligence (AI), compact, digital predistortion (DPD), Doherty, lumped components, millimeter-wave (mm-wave), power amplifier (PA), power combiner, three-stage, voltage standing wave ratio (VSWR).**

I. Introduction

THE millimeter-wave (mm-wave) bands of fifth-generation (5G) networks enable the multi-gigabit per second data rates, high capacity, and low latency necessary for the next generation of digital innovation and connectivity. To achieve these capabilities, 5G networks employ phased array beamforming systems and spectrally efficient modulation schemes like quadrature amplitude modulation (QAM) and orthogonal frequency-division multiplexing (OFDM). These modulation methods, however, result in signals with a high peak-to-average power ratio (PAPR) [1], [2], [3], [4]. For instance, the commonly used 64-QAM OFDM has a PAPR of 11 dB if no crest factor reduction is applied, necessitating power amplifiers (PAs) to be efficient both at peak power and at 11 dB PBO.

Key requirements for mm-wave front-end design include the following:

1) *High saturated output power (P_{sat}):* Typically around 24–25 dBm for handsets and access points.
2) *Efficiency at peak and deep PBO:* To improve the average efficiency [5], [6].
3) *Large modulation bandwidth (up to* 1.4 GHz*):* To fully leverage the mm-wave spectrum.
4) *High and flat gain:* To compensate for signal losses in preceding stages, such as power splitters, phase shifters, and mixers [7], [8]. Gain flatness can also impact over-the-air performance, such as the coverage area at certain frequencies and can introduce frequency-dependent distortion and intermodulation distortion.
5) *Linearity:* With stringent error vector magnitude (EVM) requirements, such as −25/−30 dB for 64-/256-QAM [5], [6].
6) *Voltage standing wave ratio (VSWR) resilience:* Ensuring compatibility with phased array systems [8].

Nanoscale complementary metal-oxide-semiconductor (CMOS) technologies are being investigated for 5G mm-wave transmitters (TXs) because of their high integration, cost-effectiveness, compact size, and efficiency. However, these technologies face challenges such as limited supply voltage and maximum oscillation frequency (F_{max}), which make it difficult to achieve the desired P_{sat}. Furthermore, $R_{opt} = (V_{DD}^2/2P_{sat})$ cannot be significantly reduced because it needs to match the impedance of the 50 Ω antenna. This limitation raises the quality factor (QF) requirements and restricts the operational bandwidth.

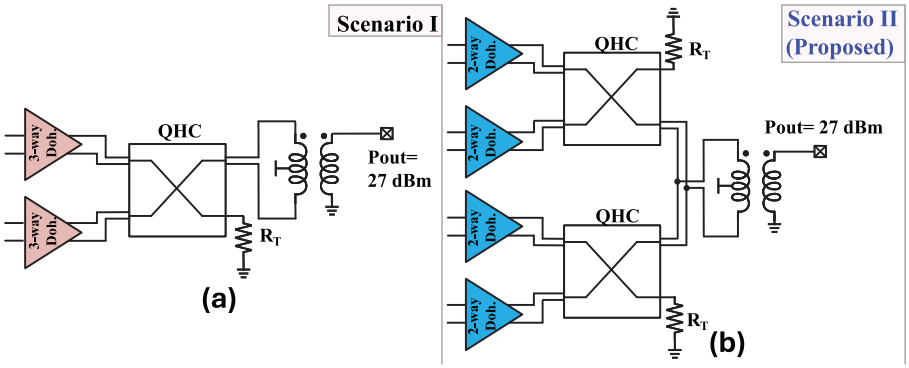
Although recent power combiners satisfy 5G requirements for output power (P_{out}), EVM, and adjacent channel leakage ratio (ACLR), improving average efficiency is still a daunting task [8], [9], [10], [11], [12]. The N-way Doherty amplifier is well regarded for delivering high P_{out} and enhancing average efficiency for signals with high PAPR. Among N-way Doherty configurations, 2-way [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], 3-way [25], [26], [27], and 4-way Doherty amplifiers [28], [29] are commonly used. However, as noted in [30], increasing the number of Doherty stages ideally boosts P_{sat}, but it also adds two inductors and capacitors to the output network for each additional stage in a linear Doherty PA. These additional components raise passive losses more than conventional combiners, potentially reducing P_{sat} in

Received 4 February 2025; revised 9 April 2025 and 3 May 2025; accepted 6 May 2025. Date of publication 25 June 2025; date of current version 28 October 2025. This work was supported in part by Dutch Government through Top Consortium voor Kennis en Innovatie (TKI) and in part by Huawei Sweden through the Open-Research Grant. *(Corresponding author: Anil Kumar Kumaran.)*

Anil Kumar Kumaran, Yizhuo Wu, Masoud Pashaeifar, Chang Gao, Leonardus Cornelis Nicolaas de Vreede, and Morteza S. Alavi are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: a.k.kumaran@tudelft.nl; Yizhuo.Wu@tudelft.nl; M.Pashaeifar@tudelft.nl; l.c.n.devreede@tudelft.nl; Chang.Gao@tudelft.nl; S.M.Alavi@tudelft.nl).

Hamza Nachouane is with Huawei Technologies Sweden AB, 412 50 Gothenburg, Sweden (e-mail: hamza.nachouane1@huawei.com).

Digital Object Identifier 10.1109/TMTT.2025.3569155



Parameters	Scenario I	Scenario II
Number of combining stages	2	3
Stage 1	Two 3-way Doherty	Four 2-way Doherty
Stage 2	One QHC	Two QHCs
Stage 3	-	Non-isolated power combining
Balun	Yes	Yes
Output power per Doherty (dBm)	24	21

(c)

Fig. 1. (a) Scenario I: two 3-way Doherty amplifiers using one QHC. (b) Scenario II (proposed): four 2-way Doherty amplifiers using two QHCs. (c) Comparison between two scenarios.

practice. Furthermore, DE_{avg} shows little improvement beyond the 3-way Doherty configuration for signals with a PAPR of 11 dB. Besides, the impedance of the main PA in symmetrical N-way linear Doherty designs varies from optimum impedance (R_{opt}) to $N \times R_{opt}$, which decreases the operational bandwidth due to the higher QF requirement compared to conventional combiners. Efficiency improvements at deep PBO are also limited by the finite channel resistance of the CMOS PAs [31], [32]. Thus, increasing beyond 2-/3-way Doherty configurations does not significantly enhance average efficiency due to the increased losses in these technologies.

As an alternative approach, this article proposes a novel 4×2-way Doherty PA that meets the key design requirements outlined earlier, specifically achieving high output power by combining a 4-way power combiner with a 2-way Doherty architecture. In this work, we thoroughly analyze the benefits of the proposed front-end in terms of delivered output power, efficiency, bandwidth, linearity, and VSWR performance. The proposed output network enhances efficiency at PBO, linearity, wide operational bandwidth, and large modulation bandwidth, as the 2-way Doherty network exhibits a lower impedance transformation compared to higher-order symmetrical Doherty networks and requires less complicated adaptive biasing circuitry. Furthermore, the proposed combiner comprises two QHCs, which improve the PA's resilience VSWR variations.

This article covers the following topics. Section II analyzes various power combiner topologies, including 2-/3-way Doherty variants and compares their performance with and without losses. Section III details the design methodology for a compact power combiner that integrates four 2-way Doherty amplifiers, two quadrature hybrid couplers (QHCs), and a balanced-to-unbalanced (balun) transformer. Section IV explores the circuit implementation of the proposed 4×2-way Doherty PA prototype, which is fabricated using 40 nm bulk CMOS technology. The experimental results are presented in Section V, and this article concludes in Section VI.

II. Power Combiner Variants

To meet the handset and access point requirements of the 5G standard, a P_{sat} of 24–25 dBm is necessary. Assuming an output network loss of 2–3 dB, the ideal P_{sat} should reach approximately 27 dBm (0.5 W). Achieving this output power requires an N-way power combiner paired with an N-way Doherty network, as 6–8 devices are typically needed to generate 27 dBm using CMOS 40 nm technology. Moreover, as discussed, the PA must support OFDM signals with high PAPR (≈ 9–12 dB), while operating under load mismatch conditions of up to VSWR 3:1. One approach involves increasing the complexity of the Doherty network while reducing the order of the power combiner to achieve a power-added efficiency (PAE) peaking at ≈12 dB PBO. The second approach prioritizes minimizing complexity, thereby improving overall PAE by reducing the output matching network's loss. Based on this tradeoff, integrating the power combiner with 2-/3-way Doherty architectures is the most effective approach, achieving an optimal balance between P_{sat}, average efficiency, and wide bandwidth.

1) *Scenario I:* Two 3-way Doherty amplifiers using a QHC combiner [Fig. 1(a)].
   In this design, the power combiner uses a single QHC to combine the power of two 3-way Doherty PAs. Each 3-way Doherty PA's output network includes either three transmission lines (TLs) or, for a high-pass (HP) model, four inductors and three capacitors. Here, the P_{sat} for each 3-way Doherty and PA is 24 and 19.2 dBm, respectively.
2) *Scenario II (Proposed):* Four 2-way Doherty amplifiers using two QHCs as power combiners [Fig. 1(b)].
   The 4-way power combiner in this design uses a combination of isolated power combining (with two QHCs) and non-isolated power combining in the current domain, which merges the power from the four 2-way Doherty PAs. Each 2-way Doherty achieves a P_{sat} of 21 dBm.

Both scenarios can be classified as balanced PAs due to the inclusion of QHCs at the output. Balanced PAs improve the PA's resilience to VSWR, as highlighted in [8] and [24]. In addition, a symmetrical N-way Doherty design employs equally sized devices, simplifying the design process and allowing the same chain to be reused for each individual PA within the Doherty configuration. Section II-A provides

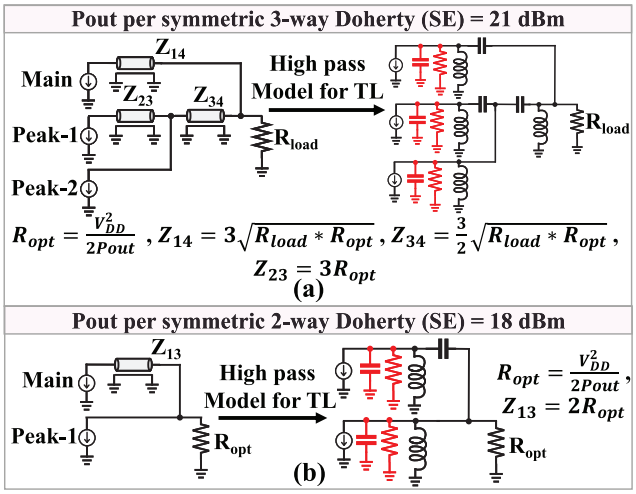


Fig. 2. (a) Schematics of 3-way Doherty PA and (b) 2-way Doherty PA.

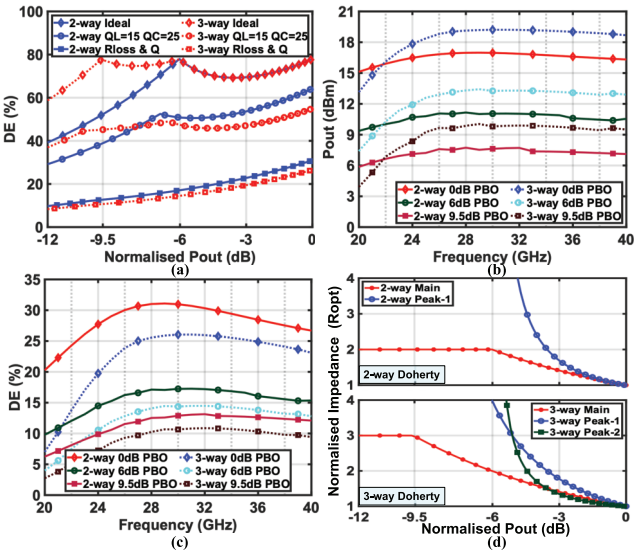


Fig. 3. (a) DE versus normalized P_{out} at 30 GHz for symmetric 2-/3-way Doherty for three cases (ideal, with QF of 15 for inductor and 25 for capacitor, with finite R_{Loss}), (b) DE, (c) P_{out} versus frequency for symmetric SE 2-/3-way Doherty with Q_L = 15, Q_C = 25, and finite R_{Loss}, and (d) normalized impedance versus normalized P_{out} at 30 GHz for symmetric 2-/3-way Doherty.

a comparison of 2-way and 3-way Doherty configurations in terms of P_{out}, DE, bandwidth, and VSWR, considering their losses in the output network.

A. 2-Way Doherty Versus 3-Way Doherty

In Fig. 2(a) and (b), the schematics for 2-way and 3-way Doherty amplifiers with TLs or lumped components are illustrated. The HP model for the TL is selected due to its integration of shunt inductors, which function as a direct current (dc) feed and can be naturally converted into a differential circuit. The figure highlights the device's drain-source capacitance (C_{ds}). In reality, the device includes channel resistance, and C_{ds} has a finite QF, which can be represented as R_{Loss}. These elements, C_{ds} and R_{Loss}, are shown in Fig. 2(a) and (b) in red [31], [32]. Ideally, R_{Loss} should be infinite. To achieve the ideal P_{sat} of 27 dBm, each PA in a symmetric 3-way Doherty configuration needs to generate 19.2 dBm[1] (Scenario I), whereas each PA in a symmetric 2-way Doherty configuration should generate 18 dBm[2] (Scenario II). This implies that the devices used in the 3-way Doherty are bigger, resulting in larger C_{ds} and lower R_{Loss} than in the 2-way Doherty.

1) Output Power and Efficiency Comparison: All simulations in Fig. 3(a)–(c) were conducted with an ideal PA model, and the QF of the capacitors and inductors were set to 25/15, respectively. It is observed that after incorporating QF into the output network and considering finite R_{Loss}, the 2-way Doherty performs better than the 3-way Doherty, even at PBOs of 9.5 and 12 dB [Fig. 3(a)]. Besides, as QF decreases, the output network losses increase, reducing both peak output power and efficiency at peak and PBO. The impact of QF degradation is more pronounced in the 3-way Doherty architecture due to its higher component count. The P_{sat} and DE_{sat} are lower for the 3-way Doherty due to higher passive losses in the output network, which has more lumped components than the 2-way Doherty.

At deep PBO, the main PA in the 3-way Doherty experiences an impedance $R_{Loss}\,||3R_{opt}$, while in the 2-way Doherty, the main PA sees $R_{Loss}\,||2R_{opt}$. Since the main PA in the 3-way Doherty requires a greater impedance transformation (to $3R_{opt}$) at deep PBO compared with 2-way Doherty, its DE peak at 9.5 dB significantly reduced, making it more susceptible to R_{Loss} [refer to Fig. 3(d)]. This suggests that N-way Doherty configurations may not achieve the desired DE peak at deep PBO due to the higher impedance transformation required. Efficiency improvements at deep PBO could be realized through: 1) asymmetric Doherty designs, which employ smaller main PA to improve efficiency at deep PBO; 2) higher supply voltages, allowing the use of smaller devices with larger R_{Loss}; and 3) advances in technology to reduce C_{ds} and have better QFs.

Fig. 3(b) and (c) presents the DE and P_{out} versus frequency for symmetric 2-way and 3-way Doherty configurations with finite R_{Loss} and a QF of 15/25 for inductors and capacitors, respectively. In terms of bandwidth for DE and P_{out}, the 2-way Doherty outperforms the 3-way Doherty. It is also noted that while the 3-way Doherty produces higher P_{out}, despite higher passive losses, this is because it is designed for a single-ended (SE) P_{out} of 21 dBm, whereas the 2-way Doherty is designed for 18 dBm.

Fig. 3(d) illustrates the normalized drain impedance for the main and peak-1 PAs in a symmetric 2-way Doherty configuration, as well as the normalized drain impedance for

[1]Each single-ended (SE) PA must generate 16.2 dBm. Thus, a push-pull configuration generates 19.2 dBm. Subsequently, one bank of 3-way Doherty generates 24 dBm, and 2 × 3-way Doherty eventually delivers 27 dBm.

[2]Each SE PA must generate 15 dBm. Thus, a push-pull configuration generates 18 dBm. Subsequently, one bank of the 2-way Doherty generates 21 dBm, and 4 × 2-way Doherty eventually delivers 27 dBm.

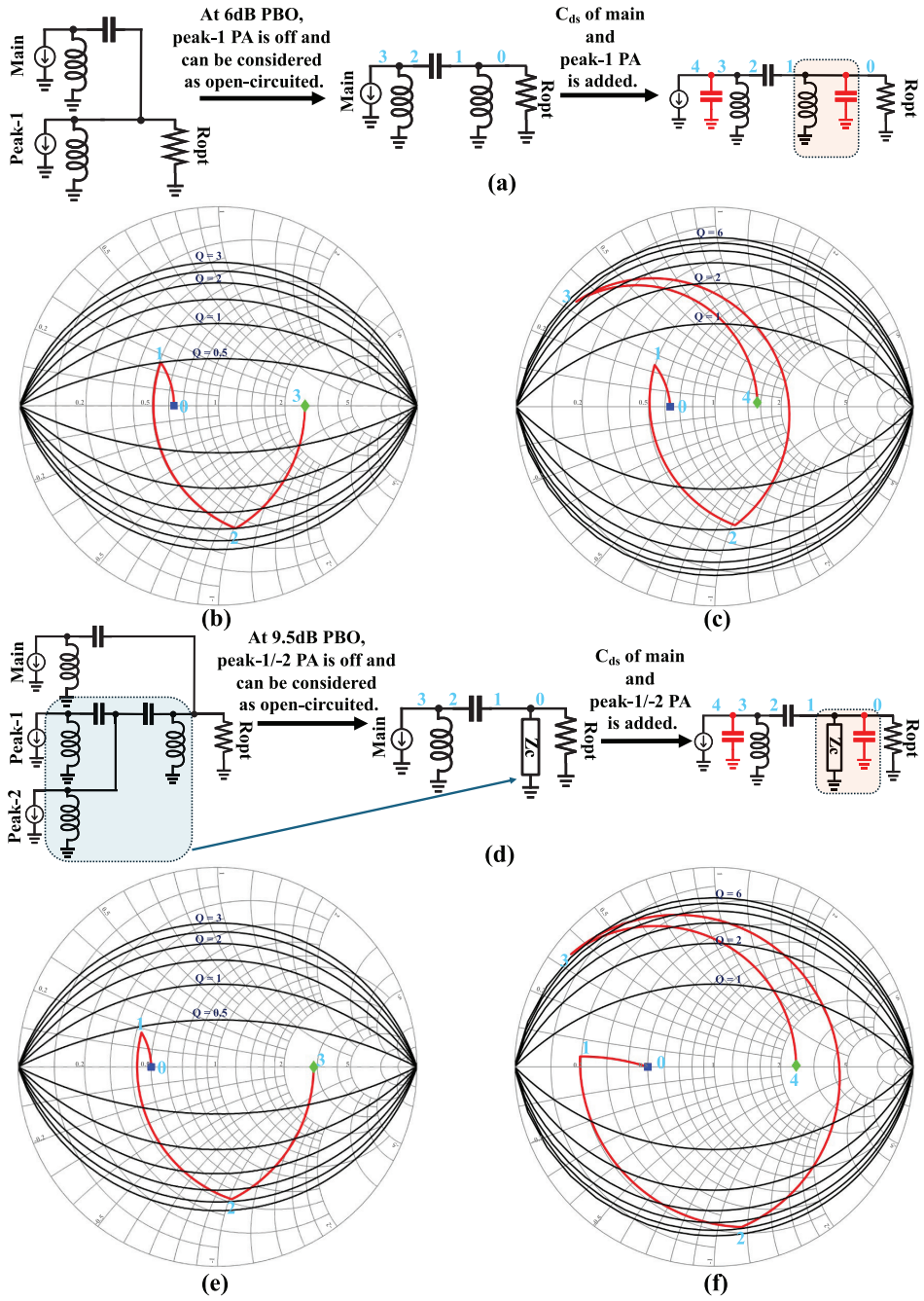


Fig. 4. (a) Schematic of a 2-way Doherty at deep PBO, (b) Smith chart illustrating the impedance trajectory of the main PA in the 2-way Doherty with ideal lumped components, and (c) with a QF of 15/25 for inductors/capacitors and parasitic C_{ds}. (d) Schematic of a 3-way Doherty at deep PBO, (e) Smith chart showing the impedance trajectory of the main PA in the 3-way Doherty with ideal lumped components, and (f) with a QF of 15/25 for inductors/capacitors and parasitic C_{ds}.

the main, peak-1, and peak-2 PAs in a symmetric 3-way Doherty configuration. These simulations employ ideal PAs and output networks, with the impedance normalized to the R_{opt} required to achieve the desired P_{sat}. Notably, R_{opt} differs between the 2-way and 3-way Doherty configurations, as they are designed to generate 18 and 21 dBm, respectively.

2) Bandwidth Comparison: At 6 dB PBO, the peak-1 PA in the 2-way Doherty is inactive and can be approximated as open-circuited, leaving only the main PA active, as shown in the schematic of Fig. 4(a). The impedance at each node is calculated and plotted on the Smith chart [Fig. 4(b)] to visualize the main PA's impedance trajectory, which remains within a Q circle of 2. Similarly, at a deep PBO of 9.5 dB, both peak-1 and peak-2 PAs in the 3-way Doherty are inactive, with only the main PA active, as illustrated in Fig. 4(d). Fig. 4(e) shows the impedance trajectory of the main PA with ideal lumped components, which stays within a Q circle of 2.5. The 3-way Doherty demands a higher QF due to

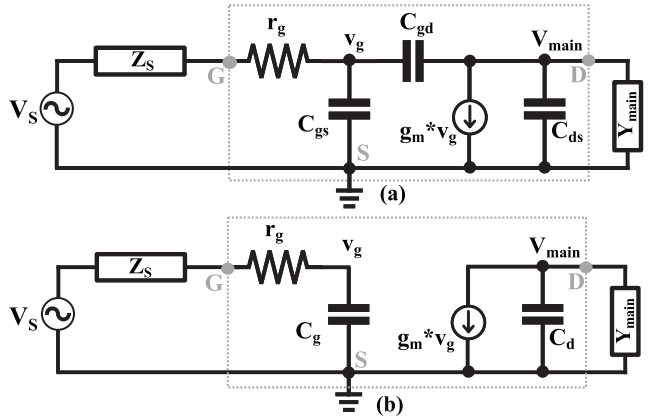


Fig. 5. (a) Schematic model of the MOSFET device and (b) equivalent circuit after applying Miller's theorem to C_{gd}.

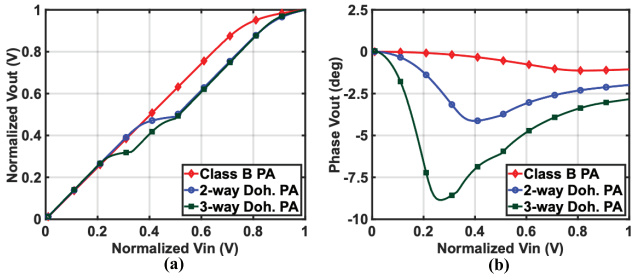


Fig. 6. (a) AM-AM and (b) AM-PM of 2-/3-way Doherty PAs and standalone class-B PA.

the larger impedance transformation ($3R_{opt}$) at deep PBO, thereby limiting the operational bandwidth compared to the 2-way Doherty as explained by $Q = (f_0/\mathrm{BW})$. This bandwidth limitation of the 3-way Doherty is also apparent in the DE and P_{out} versus frequency plots [Fig. 3(b) and (c)].

When a QF of 15/25 is introduced for the inductors/capacitors and parasitic C_{ds} in the 2-/3-way Doherty configurations, the impedance trajectory shifts, as shown in Fig. 4(c) and (f). This reduces the drain impedance of the main PA, extending the trajectory beyond a Q circle of 4 and 6 for the 2-/3-way Doherty configurations, respectively, which further limits the operational bandwidth. The loaded QF (Q_L) at each node can be calculated using $\mathrm{QF} = (\Im(Y)/\Re(Y))$. In addition, for a given unloaded network QF (Q_N) and loaded network QF (Q_L), the insertion loss (IL) can be determined as follows [33]:

$$\mathrm{IL} = 10\log\left(\frac{1}{1+\frac{Q_L}{Q_N}}\right). \tag{1}$$

For steps 0 and 1, Q_N is equal to Q_{ind}; for other steps Q_N can be approximated as $Q_{ind}\|Q_{cap}$ for easier calculation. The total approximate IL for the 2-/3-way Doherty networks are 2.6 and 4.2 dB, respectively.

The Q analysis clearly demonstrates that the 2-way Doherty amplifier has a wider operational bandwidth, requiring a smaller impedance transformation and a lower QF compared to the 3-way Doherty. It also has lower IL due to the reduced number of lumped components.

3) Linearity Comparison: To compare the linearity of 2-way and 3-way Doherty PAs, a theoretical amplitude-to-phase (AM-PM) analysis is performed on the main PA, as it predominantly determines the linearity of the Doherty PA. Fig. 5(a) depicts an metal-oxide-semiconductor field-effect transistor (MOSFET) model consisting a voltage-controlled current source ($g_m V_g$), capacitors [gate-source capacitance (C_{gs}), C_{ds}, and gate-drain capacitance (C_{gd})], and a gate resistance (r_g). The admittance $Y_{main} = G_{main} + jB_{main}$ represents the output load of the main PA, where $G_{main} = (1/R_{main})$ and $B_{main} = (1/X_{main})$. The transistor gate is connected to a voltage source (V_S) with an internal impedance of $Z_S = R_S + jX_S$.

By applying Miller's theorem to the feedback capacitor (C_{gd}), the equivalent schematic shown in Fig. 5(b) is obtained. It is assumed that the drain load of the transistor is purely resistive, and the PA achieves a high voltage gain. Based on these assumptions, the phase of V_{main} ($\angle V_{main}$) is calculated as shown in the following equation:

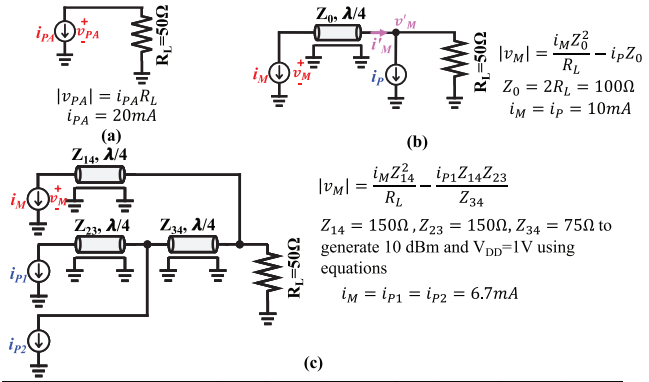
$$\angle V_{main} = \tan^{-1}\left(\frac{R_s + r_g}{X_s - \frac{1}{\omega\left(C_{gd}g_m R_{main} + C_{gs}\right)}}\right). \tag{2}$$

Equation (2) reveals that $\angle V_{main}$ depends on the transistor parameters (C_{gs}, C_{gd}, transconductance (g_m), and r_g) and the output impedance presented to the main PA's drain (R_{main}). In a 2-way symmetrical Doherty PA, the impedance transitions from R_{opt} to $2R_{opt}$, whereas in a 3-way Doherty PA, it changes from R_{opt} to $3R_{opt}$ [as shown in Fig. 3(d)]. This indicates that the 3-way Doherty PA experiences larger fluctuations in $\angle V_{main}$, resulting in greater AM-PM distortion compared to the 2-way Doherty PA.

A non-linear C_{ds} is introduced at the main and peak PAs drains in 2-way and 3-way Doherty. Fig. 6 illustrates the amplitude-to-amplitude (AM-AM) and AM-PM characteristics of class-B, 2-way Doherty, and 3-way Doherty PAs with non-linear C_{ds}, assuming ideal output network and devices. The results show that most of the AM-AM and AM-PM distortion originates from the main PA's non-linear C_{ds}, as it remains active throughout the operation. The impact of the non-linear C_{ds} in the peak-1 PA is noticeable only near saturation power.

As shown in Fig. 6, AM-PM distortion contributes more significantly to the non-linearity of Doherty PAs than AM-AM distortion. Furthermore, AM-PM distortion is larger in 3-way Doherty PA than 2-way Doherty PA, which aligns with the behavior predicted by (2). Moreover, as indicated in (2), $\angle V_{main}$ is also a function of g_m, C_{gd}, and C_{gs}, whose values depend on the gate input voltage and are inherently non-linear. Consequently, load modulation in Doherty PAs exacerbates the AM-PM performance even further compared with the ideal model with non-linear C_{ds}.

In conclusion, AM-PM distortion is the primary contributor to the non-linearity of Doherty PAs, driven largely by load modulation, especially when compared to traditional class B/AB PAs. 3-way Doherty PAs exhibit greater non-linearity due to larger impedance transformations.



VSWR		1	1.5∠0	1.5∠180	2∠0	2∠180	3∠0	3∠180
$R_L(\Omega)$		50	75	33.3	100	25	150	16.7
Class-B	v_M at peak (V)	1	1.5	0.67	2	0.5	3	0.33
2-way Doherty		1	0.33	2	0	3	−0.33	5
3-way Doherty		1	0	2.5	−0.5	4	−1	7
Class-B	v_M at 6dB PBO (V)	0.5	0.75	0.33	1	0.25	1.5	0.17
2-way Doherty		1	0.67	1.5	0.5	2	0.33	3
3-way Doherty		1	0.5	1.75	0.25	2.5	0	4
Class-B	v_M at 9.5dB PBO (V)	0.33	0.5	0.22	0.67	0.17	1	0.11
2-way Doherty		0.67	0.44	1	0.33	1.33	0.22	2
3-way Doherty		1	0.67	1.5	0.5	2	0.33	3

(d)

Fig. 7. (a) Class-B PA, (b) 2-way Doherty, (c) 3-way Doherty, and (d) voltage of the main PA across VSWR for all cases.

4) VSWR Resilience Comparison: Fig. 7 shows the schematics of 2-/3-way Doherty PAs, along with the formula for calculating the voltage across the main PA (v_M). Consider the schematic shown in Fig. 7(b). Since a $\lambda/4$ TL is used, the current and voltage on either side of the TL can be related as follows:

$$\begin{bmatrix} v_M \\ i_M \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} v'_M \\ i'_M \end{bmatrix}. \tag{3}$$

In this regard, let us consider the main and peak PAs as ideal current sources. Here, the combination of the main current source and $\lambda/4$ impedance inverter operates as a voltage source. Since the output impedance of the voltage source is zero and is in parallel with the load, i_P does not contribute to the output current. Thus, the load's voltage and current relationships are as follows:

$$\begin{aligned} v'_M &= i_L R_L \\ i'_M &= i_L - i_P. \end{aligned} \tag{4}$$

Using (3) and (4), we can calculate the magnitude of v_M as shown in the following equation:

$$|v_M| = \frac{i_M Z_0^2}{R_L} - i_P Z_0. \tag{5}$$

Similar to the 2-way Doherty, we can calculate the voltage of the main PA (v_M) for the 3-way Doherty, as shown in the following equation:

$$|v_M| = \frac{i_M Z_{14}^2}{R_L} - \frac{i_{P1} Z_{14} Z_{23}}{Z_{34}} \tag{6}$$

It is evident from (5) and (6) that one term is load-dependent, while the other is load independent, unlike in a class-B PA, where $v_{PA} = i_{PA} R_L$. Note that at 6 dB PBO, (5) and (6) become

$$|v_{M6dB}| = \frac{i_M Z_0^2}{2R_L} \quad \text{and} \quad |v_{M6dB}| = \frac{i_M Z_{14}^2}{2R_L} - \frac{i_{P1} Z_{14} Z_{23}}{4Z_{34}}. \tag{7}$$

Similarly at 9.5 dB PBO, (5) and (6) become

$$|v_{M9p5\ dB}| = \frac{i_M Z_0^2}{3R_L} \quad \text{and} \quad |v_{M9p5dB}| = \frac{i_M Z_{14}^2}{3R_L}. \tag{8}$$

Let us consider the peak currents of the main PA (i_M) and peak PA (i_p) are given as 10 mA, ensuring an output power of 10 dBm with a V_{DD} of 1 V and a load impedance (R_L) of 50 Ω. The table in Fig. 7(d) shows the values of v_M at peak P_{out} for different VSWR cases. At VSWR = 2∠0°, v_m is 0. This implies that an ideal symmetrical 2-way Doherty PA with 6 dB PBO efficiency enhancement cannot operate under a VSWR greater than 2. Fig. 7(c) illustrates a symmetric 3-way Doherty that generates 10 dBm with a 1 V supply and R_L = 50 Ω. The characteristic impedance (Z_0) of the TLs is calculated using the formula shown in Fig. 2(a).

Similarly, for a 3-way Doherty PA, v_M is 0 for VSWR of of 1.5∠0°. Thus, 3-way Doherty cannot work under VSWR greater than 1.5. Also, it is seen that the reliability of a Doherty PA is more sensitive to the load impedance variation, and it increases as the Doherty order increases. In terms of VSWR resilience, the 2-way Doherty amplifier demonstrates superior performance and lesser reliability issues compared with the 3-way Doherty.

Furthermore, from the table in Fig. 7(d), it is evident that the behavior of the 3-way Doherty at 6 dB PBO is similar to that of the 2-way Doherty at 0 dB PBO. Likewise, the 2-way Doherty at 6 dB PBO and the 3-way Doherty at 9.5 dB PBO behave like a class-B PA. This can significantly affect the performance when operating with high PAPR signals.

TABLE I
SUMMARY OF SECTION II-A

Parameters	3-way Doherty	2-way Doherty
Output network (ON)	Consist of 4 inductors and 2 capacitors	Consist of 2 inductors and 1 capacitors
Psat with lossy ON	3-way Doherty has more loss than 2-way Doherty when lossy ON is considered	
Impedance transformation for main PA	3Ropt to Ropt	2Ropt to Ropt
Efficiency at PBO	Higher degradation in PBO efficiency for 3-way Doherty when Rloss is considered (reason - larger impedance transformation)	
Bandwidth	3-way Doherty is narrow band (reason - higher Q requirement due to larger impedance transformation)	
Linearity	3-way Doherty has a larger AM-PM variation (reason - larger impedance transformation)	
VSWR resilience	3-way Doherty can't handle beyond VSWR of 1.5	2-way Doherty can't handle beyond VSWR of 2

B. Selected Power Combiner

The proposed power combiner, illustrated in Fig. 1(b), employs the 2-way Doherty amplifier due to its lower passive losses, wider bandwidth, better linearity, and superior VSWR resilience compared with the 3-way Doherty (refer Table I). The architecture integrates three types of power combining: 1) Doherty; 2) isolated power combining using

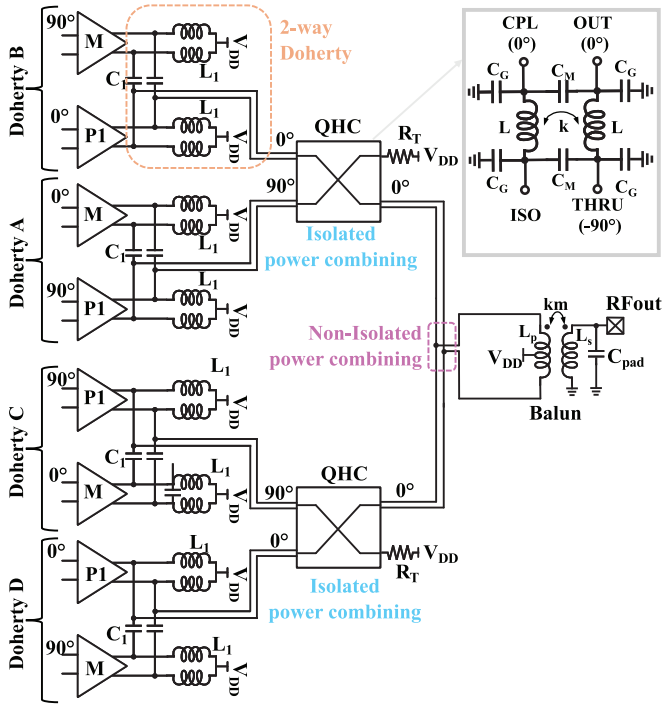


Fig. 8. Schematic of the proposed power combiner using 2-way Doherty network and QHCs.

QHCs; and 3) non-isolated power combining. While non-isolated power combining could be replaced with isolated power combining using QHCs, this substitution would increase losses. At mm-wave frequencies, simulations indicate that each QHC incurs a loss of 0.4–0.5 dB, depending on the metal stack used [8], [22], [34]. Furthermore, adding an extra QHC in the third-stage power combining does not provide significant improvements in VSWR resilience. The proposed design incorporates only two QHCs, minimizing losses and making its performance comparable to the power combiner shown in Fig. 1(a). Additionally, placing the QHCs closer to the drain of the PA is advantageous, as it reduces the effect of fast antenna impedance variations. This proximity helps the QHC maintain impedance stability without adversely affecting Doherty operation. The use of QHCs makes the proposed structure a balanced PA. Thus, the proposed structure diminishes forward power deviation, delivered power loss, and efficiency degradation in both mutual-coupling and impedance mismatch scenarios [35].

III. 4× 2-Way Doherty Combiner Design Procedure

The schematics of the output power combiner are shown in Fig. 8. The phase requirement of each PA is important as it is needed for proper Doherty operation and power combining at the output. The phase of each PA and the phase at the input of QHCs are shown in Fig. 8. It consists of four 2-way Doherty networks (highlighted in orange), two QHCs, and a balun to convert the differential signal to an SE signal. The Doherty network, comprising two inductors and a capacitor, is depicted in Fig. 2(b), and its layout is shown in Fig. 9(a). It has an area of 0.028 mm^2. The inductors supply V_{DD} to the main and peak-1 PAs, respectively. To achieve a P_{sat} of 22 dBm with a V_{DD} of 2 V for a symmetric 2-way Doherty, the SE R_{opt} is 25 Ω calculated using the equations in Fig. 2(b). Z_0 of the TL (Z_{13}), along with the values for the inductor (L_1) and capacitor (C_1) can be determined using the following equation:

$$\begin{aligned} Z_{13} &= 2R_{opt} \\ L_1 &= \frac{Z_{13}}{\omega} \\ C_1 &= \frac{}{Z_{13}\omega}. \end{aligned} \tag{9}$$

The simulation results shown in Fig. 10(a) are based on the EM model of the Doherty output network [as illustrated in Fig. 9(a)] generated using Keysight's Momentum, with capacitors having a QF of 25, and ideal PA models. The designed Doherty network achieves a P_{sat} of 22 dBm, with a 2 dB loss in the output network at 30 GHz. The connection between the Doherty output and the QHC is designed as an L-match network to increase the impedance from 25 to 31 Ω.

In the second stage of power combining, QHCs are employed to enhance VSWR resilience. The differential QHC is designed using a transformer with an SE impedance of 31 Ω and has an area of 0.012 mm^2. The high-k transformer-based QHC design is done using (10) provided in [36], which helps to reduce the transformer size significantly. ω_0 is the center frequency, k is the coupling, L is the inductance in the transformer, and Z_0 is the characteristic impedance. For $Z_0 = 31$ Ω and $k = 0.8$, other parameters can be calculated

$$\begin{aligned} C &= C_M + C_G \\ \frac{C_M}{C} &= k \\ Z_0 &= \sqrt{\frac{L}{C}} \\ \omega_{\lambda/4} &= \frac{1}{\sqrt{LC\left(1-k^2\right)}} \\ \omega_0 &= 0.54\omega_{\lambda/4}. \end{aligned} \tag{10}$$

The isolation ports are properly terminated at 31 Ω. The type of resistor used is a P+ poly resistor without salicide. Fig. 9(b) shows the layout of the QHC. The parasitic ground capacitance of the physical transformer can be absorbed in C_G, and the parasitic interwinding capacitance can be absorbed in C_M.

In the third stage, a non-isolated power combining technique is utilized instead of an additional QHC to minimize losses in the output network. The traces are modeled as a coplanar edge-coupled structure [Fig. 9(c)] with Z_0 equal to the differential Z_0 of transformer-based QHC. Hence, the 4-way combiner, which employs two QHCs and non-isolated combining exhibits a 0.8 dB loss at 30 GHz, including the interconnects, as illustrated in Fig. 10(b).

The balun [Fig. 9(d)] at the output converts the differential-ended signal to an SE signal while also matching it to a 50 Ω SE antenna. The non-isolated combining reduces the differential impedance to 31 Ω since it is a parallel combination. Then,

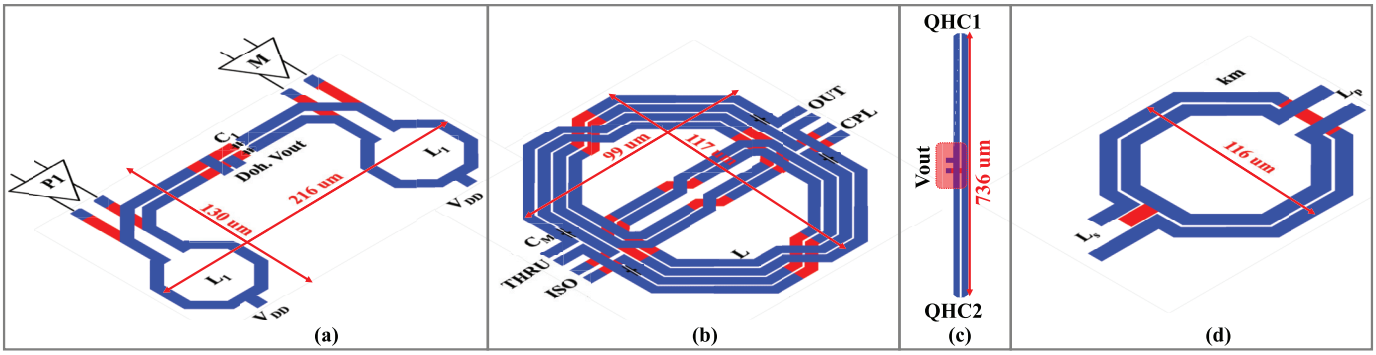


Fig. 9. (a) Layout of 2-way Doherty, (b) QHC, (c) non-isolated power combining, and (d) balun.

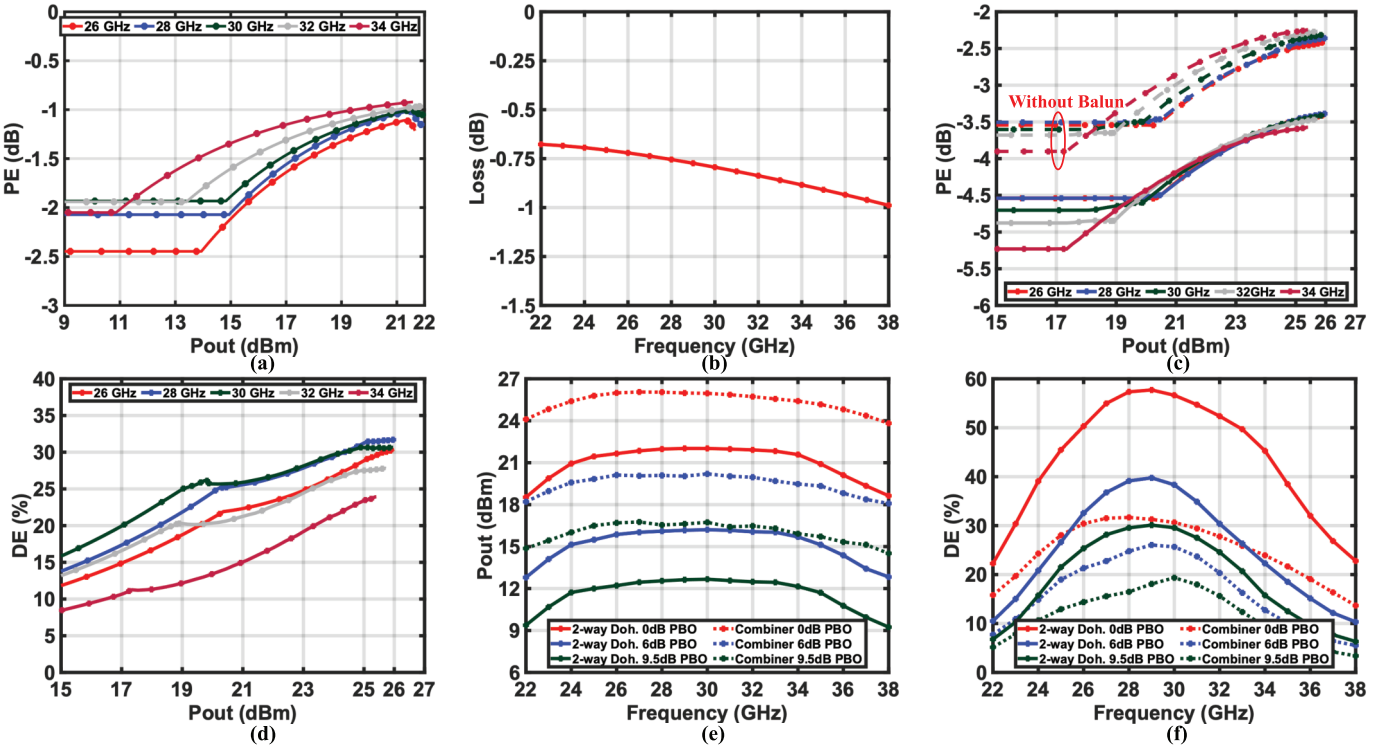


Fig. 10. (a) PE versus P_{out} across the frequency using electromagnetic (EM) model of 2-way Doherty, (b) loss of QHCs and non-isolated power combining interconnects versus frequency using the EM model, (c) PE versus P_{out}, (d) DE versus P_{out} across the frequency of the proposed power combiner, (e) DE, and (f) P_{out} versus frequency of the individual 2-way Doherty and the proposed power combiner.

the balun is used to match R_L of 50 Ω and pad capacitance (C_{pad}) to $R_P = 31$ Ω.

$$N = \frac{R_L}{R_p} = \frac{n}{\text{km}}$$
$$n = \sqrt{\frac{L_s}{L_p}}$$
$$\omega_0 = \frac{1}{\sqrt{L_s C_{\text{pad}}}}. \tag{11}$$

However, this comes at the cost of reduced passive efficiency. The balun can be integrated into the Doherty output network to achieve an SE output, as suggested in [24], [26], and [32]. The decision to use a differential power combiner (including the Doherty network and QHC) stems from the poor grounding of PAs, particularly for Doherty A and C, due to the ground pads being positioned on either side—a limitation of the technology (see Fig. 11). Maintaining the signal differential until the end relatively mitigates this issue.

Fig. 10(c)–(f) presents the simulation results using the EM model of the proposed network shown in Fig. 8, with a QF of 25 for the capacitors and ideal PAs. Fig. 10(c) and (d) illustrates the passive efficiency (PE) and DE versus P_{out} across the frequency range of 26–34 GHz. At 30 GHz, the proposed power combiner achieves a P_{sat} of 26 dBm and a maximum DE of 30%, with a loss of 4.6 dB in the output network. Fig. 10(c) shows that the balun introduces an additional 1 dB of loss. This balun can be omitted if a differential antenna is used or if better technology provides improved grounding for the PAs and allows the balun to be absorbed into the Doherty network, as previously discussed.

Fig. 10(e) and (f) shows DE and P_{out} at 0/6/9.5 dB PBO for both the individual 2-way Doherty and the proposed

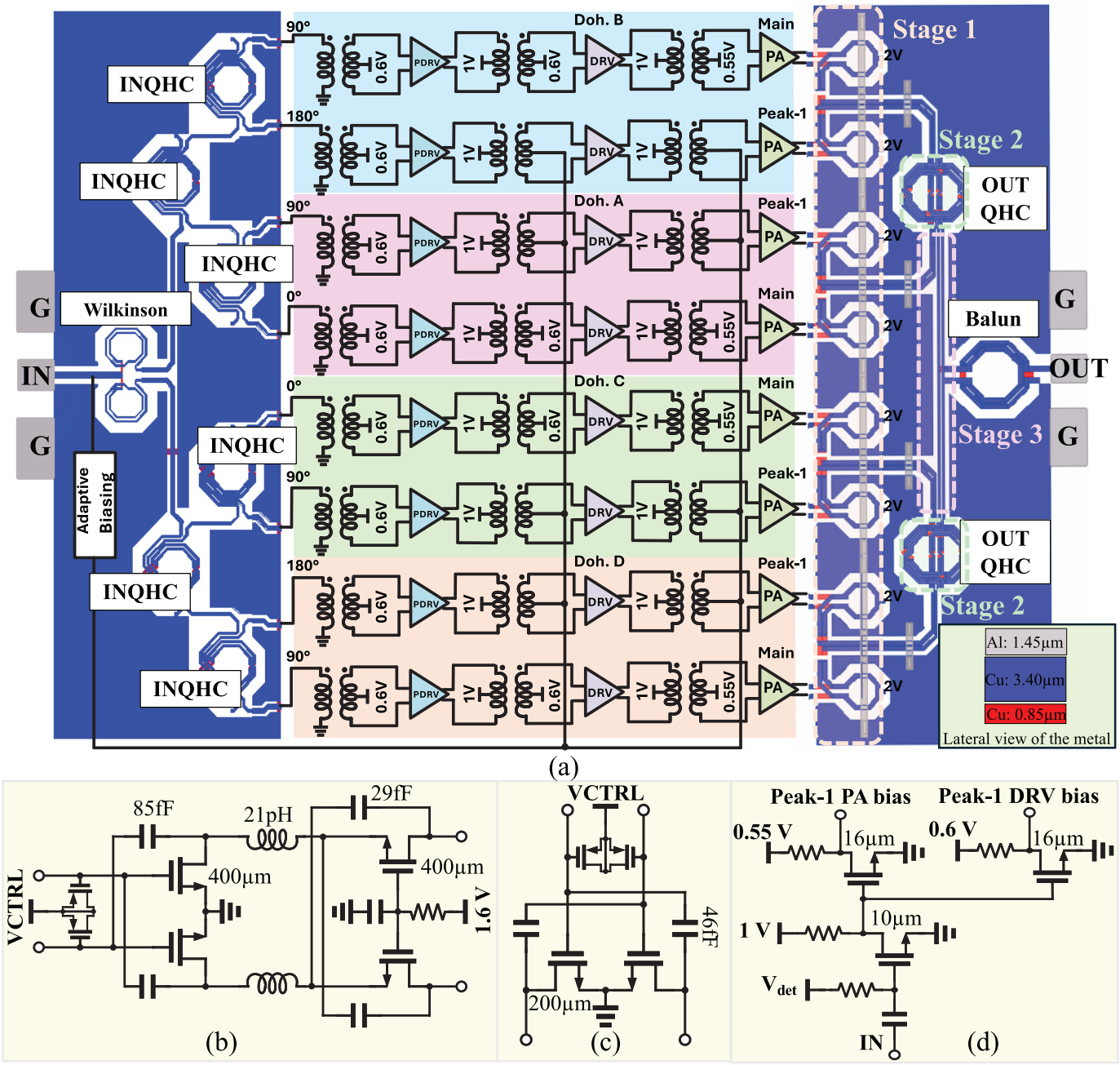


Fig. 11. (a) Schematics of the proposed 4× 2-way Doherty PA, including output combiner's layout, (b) cascode PA, (c) driver (DRV)/predriver (PDRV), and (d) adaptive biasing.

power combiner. The proposed power combiner exhibits a 1 dB bandwidth in P_{out} of 10 GHz (24–34 GHz), which is comparable to that of the individual 2-way Doherty. This indicates that the bandwidth of the proposed network is limited by the Doherty network, not by the QHCs or balun. Across the frequency range of 24–34 GHz, the proposed network achieves a DE of more than 25/15% at 0/6 dB PBO, respectively.

IV. Circuit Implementation

Fig. 11(a) presents a detailed diagram of the proposed PA configuration. The initial component is an SE input splitter that generates the required phase for the main and peak-1 PAs within each Doherty amplifier. The phase of the peak-1 PA must lead by 90° relative to the main PA in each Doherty. In addition, the output phases of Doherty B and D must be 90° ahead of Doherty A and C to ensure that the power is combined in phase by the output QHCs. The input splitter comprises a Wilkinson divider and six QHCs. The Wilkinson power splitter is designed with lumped components to match a 50 Ω impedance and provide wideband matching [37], [38], [39]. After the power is divided by the Wilkinson, each output is fed to three transformer-based SE QHCs [40], which are designed to produce the necessary phase shifts as depicted in Fig. 11(a). The isolation ports are terminated with 50 Ω, using P+ poly resistors without salicide. Fig. 12(a) demonstrates that the phase variation across the frequency for the main and

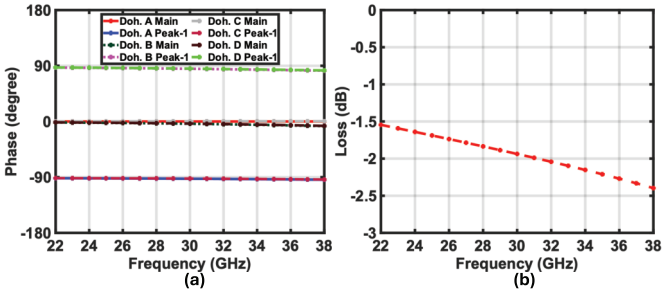


Fig. 12. (a) Phase variation across the frequency for main and peak-1 path in each Doherty [(A, B, C, and D)] and (b) loss across the frequency for the input splitter using the EM model.

peak-1 paths in each Doherty is less than 5°, and the input splitter introduces less than 2 dB of loss in the frequency range 24–32 GHz [refer Fig. 12(b)]. Although the use of three QHCs extends the bandwidth, it also increases the insertion loss [36].

Following the input splitter, each branch in the Doherty amplifier, namely, the main and peak-1 paths, includes an input balun, PDRV, inter-stage matching, DRV, inter-stage matching, and the PA itself. A balun is then used to convert the SE signal into a differential signal while providing interstage matching. This balun employs a double-tuned transformer design [41], [42], [43] to achieve broad matching, resulting in a PE of 70%, as calculated using the equation from [44]. The required power gain is attained by incorporating two additional driver stages, each utilizing a neutralized common-source transistor consisting of four unit cells, each with 50 fingers and a width of 1 μm [Fig. 11(c)]. A bias of 0.6 V is applied to the PDRVs and DRVs. The interstage matching between PDRVs and DRVs employs a double-tuned transformer network to ensure wideband matching, achieving a PE [44] of 74%.

The intermediary stage between the DRV and PA also uses a double-tuned transformer technique for wideband matching, achieving a PE of 69%. Fig. 11(b) shows the detailed schematic of the cascode PA. To maximize output-to-input isolation and ensure unconditional stability [45], two pairs of neutralization capacitors are used for the common-source and common-gate transistors. Additionally, two 21 pH inductors align the voltage and current wave phases, thereby improving DE [46]. Each common-source transistor in the PA comprises eight unit cells, each with 50 fingers and a width of 1 μm, optimized for cut-off frequency (f_T) and $F_{\max}$ while minimizing the effects of device parasitics and interconnections [47]. The cascode transistors include five unit cells with a transistor aspect ratio of 2 μm/40 nm and 40 fingers [24]. The bias is set at 0.55 V for the common-source transistor and 1.6 V for the common-gate transistors. Additionally, two PMOS varactors are employed at the PA and DRV inputs to enhance their AM-PM profiles. The non-linear variation of the input capacitance of an NMOS transistor can be compensated by adding a PMOS varactor at the input. The varactors at the PA and DRV inputs are not driven dynamically, and the control voltage (VCTRL) can be used to compensate for PVT variations or model inaccuracy during the design phase [48].

An adaptive biasing circuit, as shown in Fig. 11(d), is employed to implement Doherty load modulation. Adopted from [49], this circuit includes a SE envelope detector with an

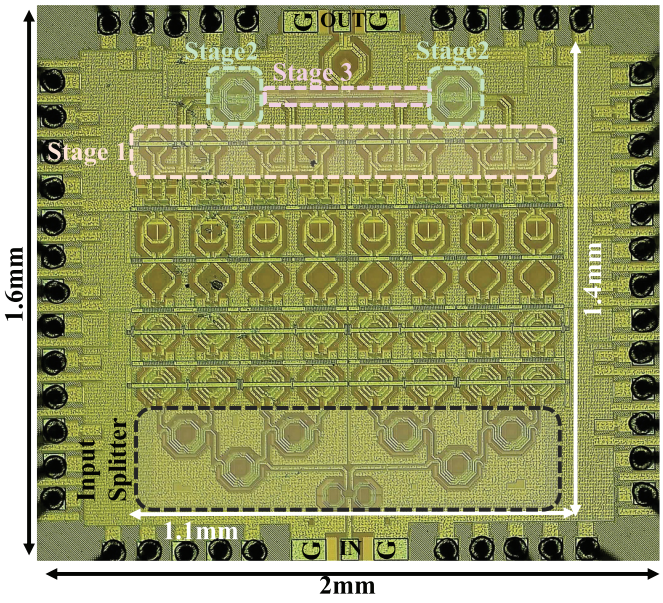


Fig. 13. Die micrograph of the proposed 4 × 2-way Doherty PA.

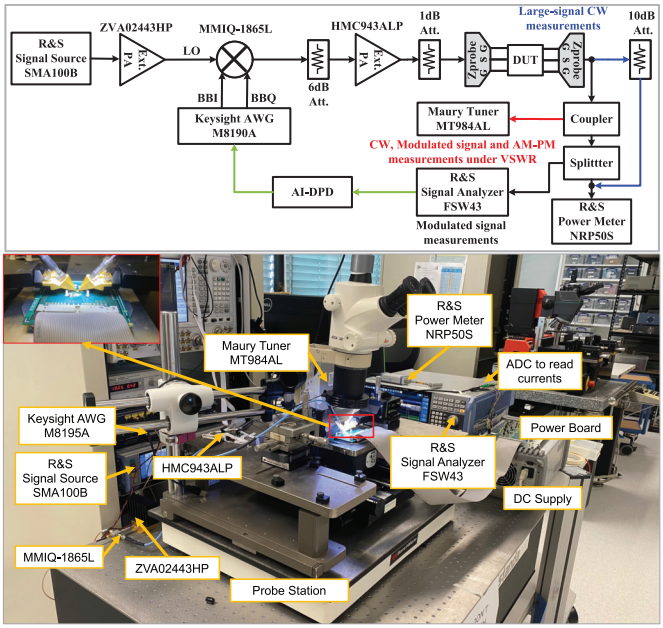


Fig. 14. Measurement setup of the proposed 4 × 2-way Doherty PA.

RF input and a turn-on voltage (V_{det}), along with two drivers for the DRV and PA. The V_{det} of the envelope detector can be adjusted to control the activation of the peak-1 PA, thereby influencing load modulation. If V_{det} is increased, the peak-1 PAs remain on, causing the output network to function as a power combiner without improving efficiency at PBO. The adaptive biasing circuit provides a 3 dB bandwidth of 2.5 GHz.

V. Measurement Results

The proposed PA was fabricated using a 40 nm bulk CMOS technology, as depicted in Fig. 13. The core area of the 4 × 2-way Doherty power combiner is 1.1 × 1.4 mm^2. Measurements were conducted using a high-frequency probe station, with

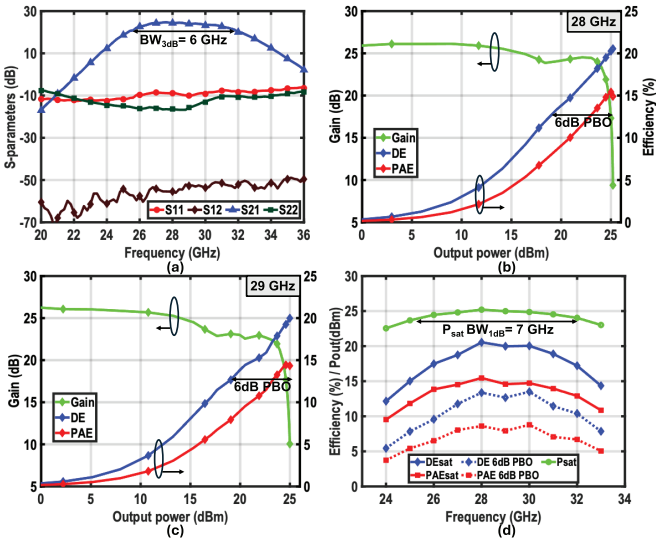


Fig. 15. (a) *S*-parameter measurement, (b) large-signal measurements at 28 GHz, (c) 29 GHz, and (d) P_{sat}, DE, and PAE across the frequency range 24–33 GHz at full power and 6 dB PBO.

dc supplies, bias voltages, and the adaptive biasing turn-on voltage wire-bonded directly to a printed circuit board (PCB). The PAs operates with a 2 V supply voltage, while the DRVs and PDRVs within each Doherty amplifier use a 1 V supply. Fig. 14 illustrates the setup for continuous wave (CW) (blue), modulated (black), and VSWR measurements (red). The insertion loss of the *Z*-probe, cables, and directional coupler was measured and de-embedded from the results.

A. CW Measurement Results

The small-signal *S*-parameter performance is measured using the Keysight E8361A vector network analyzer with the input power set to −20 dBm. As demonstrated in Fig. 15(a), the proposed PA achieves more than 6 GHz small-signal $BW_{3\ dB}$ where its S_{11}/S_{12} are less than −8/−50 dB over a 24–32 GHz band. At 28 GHz, PA's S_{22} is −18 dB, while its input matching is −9 dB. The PA offers 25.5 dB small-signal gain at 28 GHz.

The large signal CW measurement results are reported in Fig. 15(b)–(d). As V_{det} increases, peak-1 PAs are always on and there is no load modulation. Thus leading to no efficiency improvement at 6 dB PBO. But if V_{det} is reduced a lot, then the gain won't be flat and the PA becomes non-linear. Thus, V_{det} = 0.5 V is chosen for measurements in Fig. 15(b)–(d). From Fig. 15(b), the output power at 1 dB compression ($P_{1\ dB}$), P_{sat}, and gain are 23 dBm, 25.2 dBm, and 25.5 dB at 28 GHz, respectively. Its DE at P_{sat} and 6 dB PBO are 20.5%, and 13.3%, respectively. Fig. 15(d) shows P_{sat}, DE, and PAE across the frequency at 6 dB PBO, and full power with V_{det} of 0.5 V. It can be seen that the proposed PA achieves more than 24.5 dBm P_{sat} and a DE of better than 17.5%/10% at 6/0 dB PBO across the 26–32 GHz band. The PA achieves a 1 dB bandwidth of 7 GHz with respect to the P_{sat}.

B. Modulated Signal Measurement Results

The PA dynamic performance is verified using wideband modulated signals such as "64-QAM OFDM," "256-QAM OFDM," and "1024-QAM OFDM" signals. As demonstrated in Fig. 14, the baseband in-phase/quadrature (I/Q) modulated signals are generated with an arbitrary waveform generator (Keysight AWG M8190A) and upconverted using a Marki I/Q mixer (MMIQ-1865L). A directional coupler (Marki C20-0240) is employed at the output to provide the signal for an R&S FSW43 signal analyzer, while an R&S NRP50S measures the output power. Fig. 16(a) exhibits 11.3 dBm/4 % average output power (P_{avg})/average drain efficiency (DE_{avg}) measured for a 12 Gb/s OFDM 64-QAM signal at 28 GHz with 9.6 dB PAPR. Its EVM/ACLR are −25 dB/−33.6 dBc, respectively. Similarly, the proposed PA achieves 11.5 dBm/4 % P_{avg}/DE_{avg} for a 6 Gb/s OFDM 64-QAM signal with EVM/ACLR of −25 dB/−32.3 dBc, respectively [Fig. 16(b)].

For a 6.4 and 3.2 Gb/s OFDM 256-QAM signal with 9.8 dB PAPR, the proposed PA achieves an EVM/ACLR of −30 dB/−39.4 dBc and −30 dB/−39.5 dBc, respectively [Fig. 16(c) and (d)]. Furthermore, the spectral purity and constellation of a 100 MHz and 50 MHz OFDM 64-QAM signal is measured at 28 GHz with EVM/ACLR of −35 dB/−42.1 dBc and −35 dB/−42.3 dBc which are illustrated in Fig. 16(e) and (f).

Fig. 17 illustrates P_{avg} and DE_{avg} for an OFDM signal with different bandwidths (2000/1000/800/400/100 MHz) and modulation schemes (64/256) within the 24–33 GHz frequency band, aiming to meet specific EVM requirements. To elaborate, considering the minimum EVM requirement for a 64-QAM signal as −21.9 dB [5], [6] and providing a 3 dB margin, we present P_{avg}/DE_{avg} for an EVM of −25 dB. The proposed PA achieves a P_{avg}/DE_{avg} performance surpassing 10 dBm/3 % in the 25–30 GHz band, as shown in Fig. 17(a) and (b). Additionally, Fig. 17(c) and (d) exhibits corresponding results for OFDM 256-QAM signals with bandwidths of 800/400/100 MHz.

C. Comparison Between Doherty Mode and Power Combiner Mode

As previously discussed, V_{det} determines when the peak-1 PAs activate, significantly impacting back-off efficiency. Setting V_{det} = 0.9 V keeps the peak-1 PAs continuously on, causing the output network to function as a simple power combiner without providing efficiency enhancement at PBO. From Fig. 18(a), it can be observed that the power combiner mode exhibits a flat gain but fails to improve efficiency at 6 dB PBO at 28 GHz.

Fig. 18(b) presents the EVM and DE_{avg} versus P_{avg} for a 2 GHz 64-QAM OFDM signal under two scenarios: V_{det} = 0.5 V (Doherty mode) and V_{det} = 0.9 V (power combiner mode). It is evident that, for the power combiner mode (V_{det} = 0.9 V), P_{avg} increases by 3 dB to meet the EVM requirement of −25 dB for the 64-QAM OFDM signal. However, the average efficiency remains constant at 4% in both modes, thanks to the Doherty operation improving efficiency at PBO.

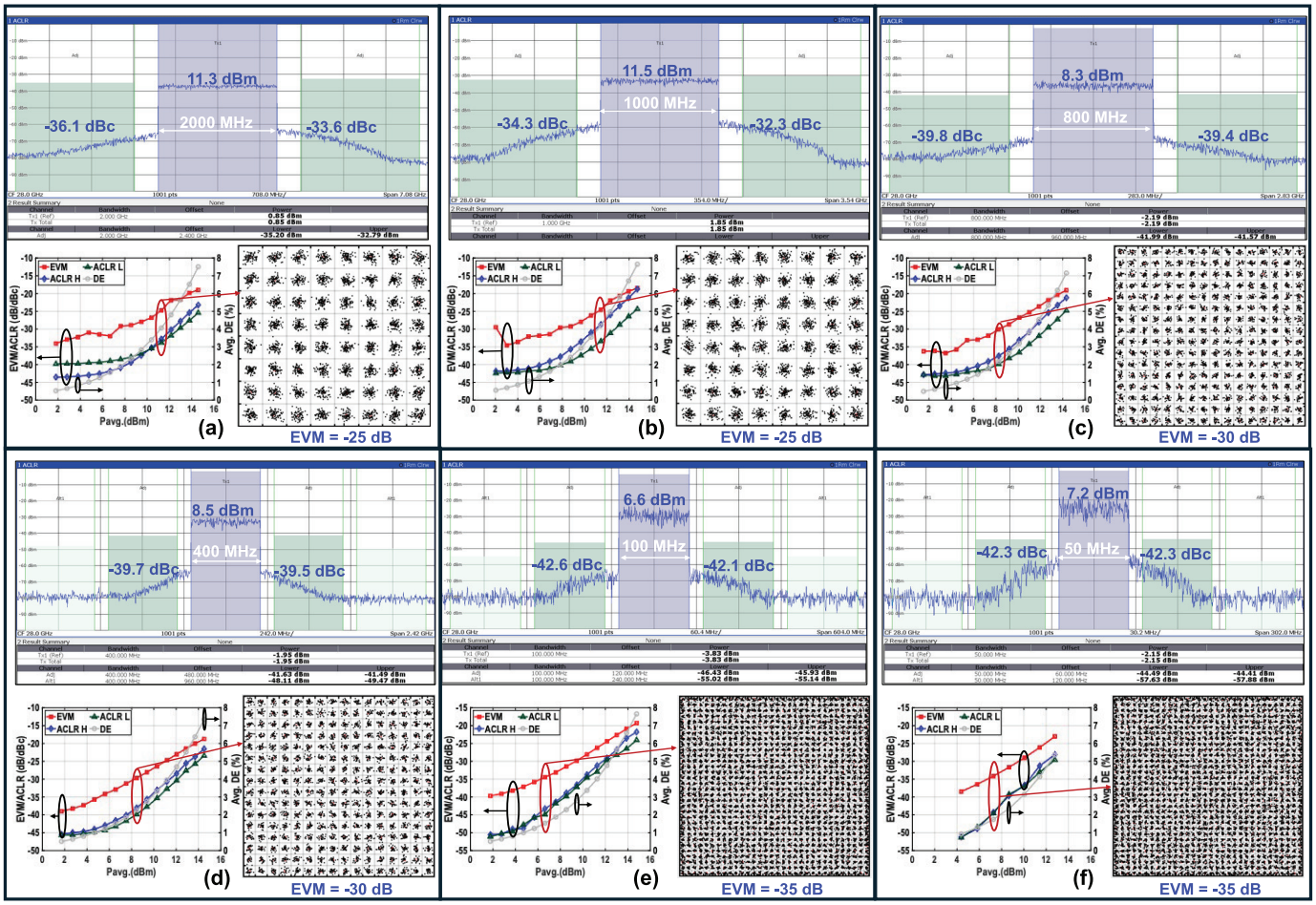


Fig. 16. (a) OFDM 2000 MHz 64-QAM, (b) OFDM 1000 MHz 64-QAM, (c) OFDM 800 MHz 256-QAM, (d) OFDM 400 MHz 256-QAM, (e) OFDM 100 MHz 1024-QAM, and (f) OFDM 50 MHz 1024-QAM at 28 GHz measurement results.

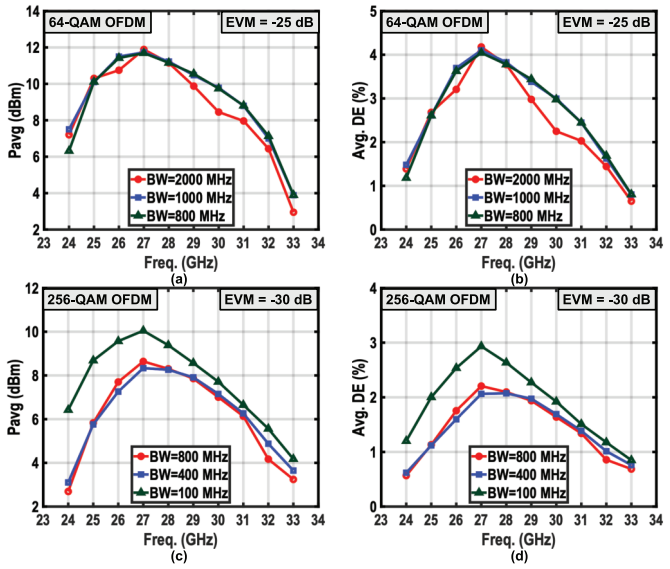


Fig. 17. (a) P_{avg}, (b) DE_{avg} for OFDM 64-QAM, (c) P_{avg}, and (d) DE_{avg} for OFDM 256-QAM across the frequency to achieve a certain EVM.

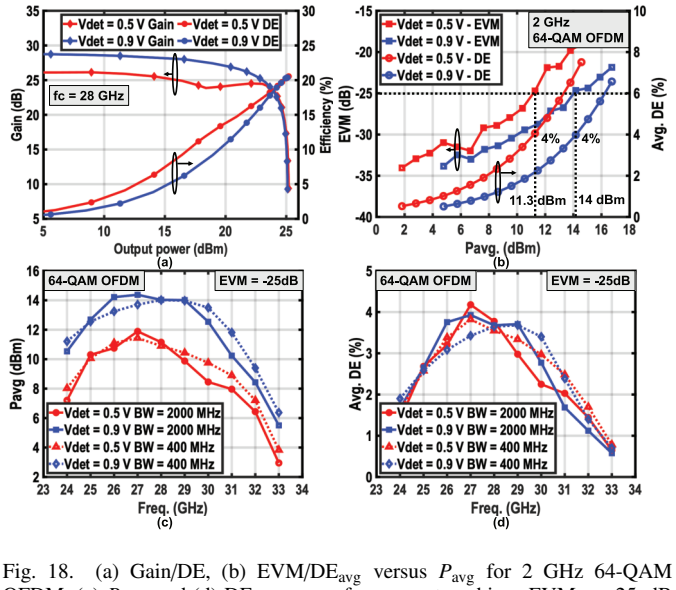


Fig. 18. (a) Gain/DE, (b) EVM/DE_{avg} versus P_{avg} for 2 GHz 64-QAM OFDM, (c) P_{avg}, and (d) DE_{avg} versus frequency to achieve EVM = −25 dB with V_{det} = 0.5 V and 0.9 V at 28 GHz.

Fig. 18(c) and (d) displays P_{avg} and DE_{avg} for a 64-QAM OFDM signal with varying bandwidths (2000/400 MHz) across frequencies to achieve an EVM of −25 dB. These results indicate that enabling the power combiner mode

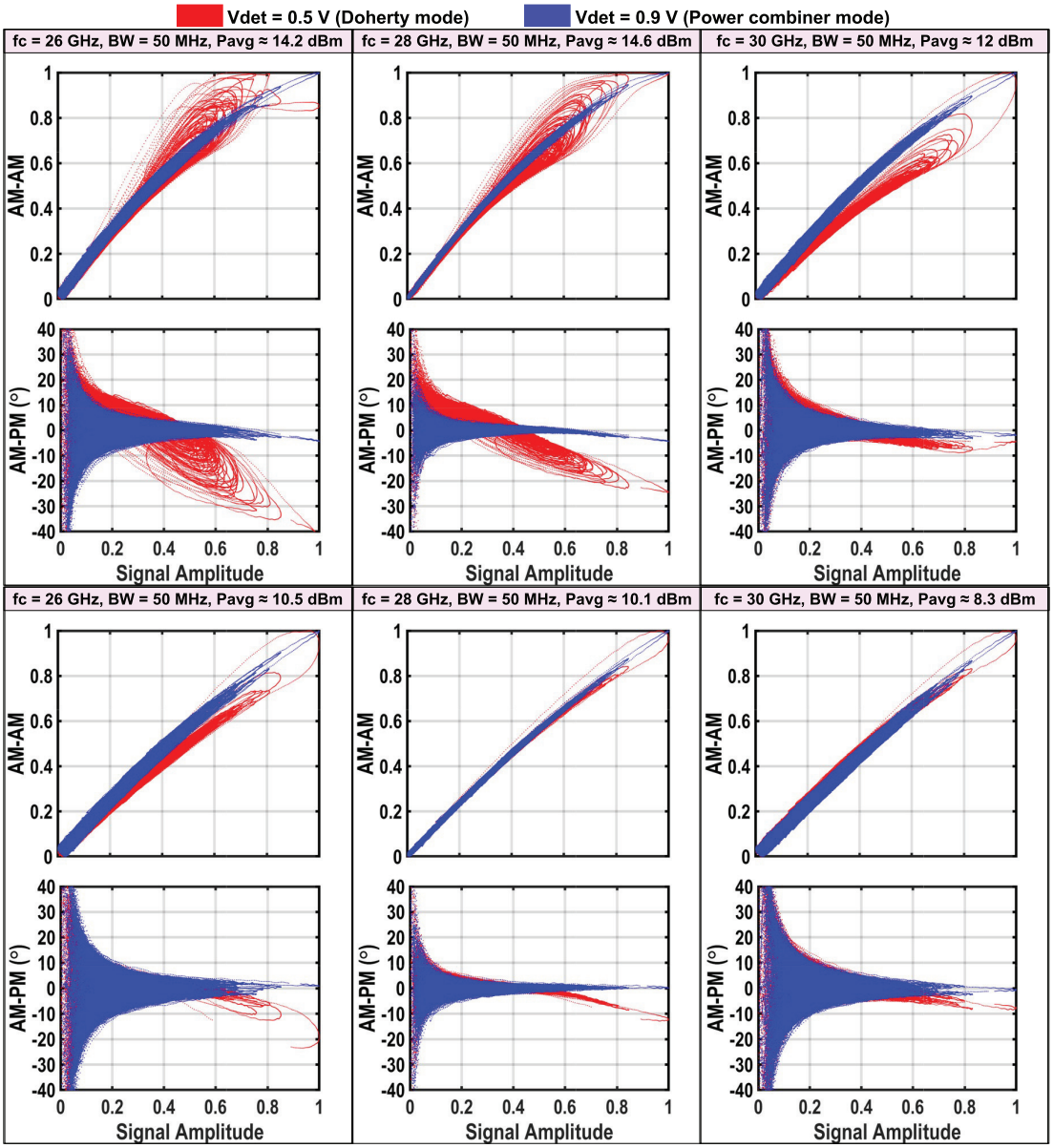


Fig. 19. The measured AM-AM/AM-PM of the proposed PA with Doherty mode (V_{det} = 0.5 V) and power combiner mode (V_{det} = 0.9 V) employing 64-QAM OFDM signals with PAPR ≈ 9.5 dB for different frequencies.

improves P_{avg} by at least 2 dB, while DE_{avg} remains similar to Doherty across the frequency range. This suggests that the Doherty mode exhibits greater non-linearity.

To delve deeper, we analyze AM-AM and AM-PM characteristics for V_{det} = 0.5/0.9 V. Fig. 19 shows the AM-AM and AM-PM distortions for Doherty mode (V_{det} = 0.5 V) and power combiner mode (V_{det} = 0.9 V) using a 64-QAM OFDM signal with bandwidth of 50 MHz across different frequencies. For $P_{\text{avg}} \approx$ 14 dBm at 28 GHz, where the power combiner mode meets the EVM requirement of −25 dB, the Doherty mode exhibits higher AM-AM and AM-PM distortions, particularly for 50 MHz bandwidth. This explains the Doherty mode's inferior EVM performance.

At lower $P_{\text{avg}} \approx$ 10 dBm, both modes show similar AM-AM performance, but the Doherty mode suffers from greater AM-PM distortion. This indicates that AM-PM deterioration occurs earlier in the Doherty mode, contributing significantly to reduced EVM. The primary cause of AM-PM distortion is load modulation, which exacerbates the non-linearity of transistor parasitics such as C_{ds}, making the Doherty PA inherently non-linear. Similarly, adaptive biasing and phase misalignment also affect linearity, but these can be considered secondary effects.

These distortions can be mitigated through DPD, which linearizes the AM-AM and AM-PM characteristics, enabling the Doherty PA to operate at higher P_{avg} and achieve the intended efficiency improvements. An off-chip deep recurrent neural network (RNN)-based digital predistortion (DPD) is employed to linearize the PA. This system utilizes a gated recurrent unit (GRU) regressor for PA modeling and DPD learning, and it is referred to as AI-DPD [53]. The block

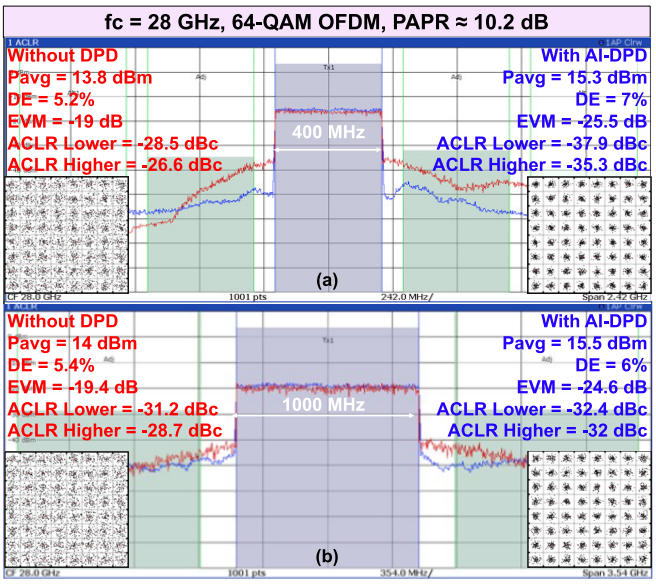


Fig. 20. (a) OFDM 400 MHz 64-QAM and (b) OFDM 1000 MHz 64-QAM at 28 GHz measurement results with and without AI-DPD.

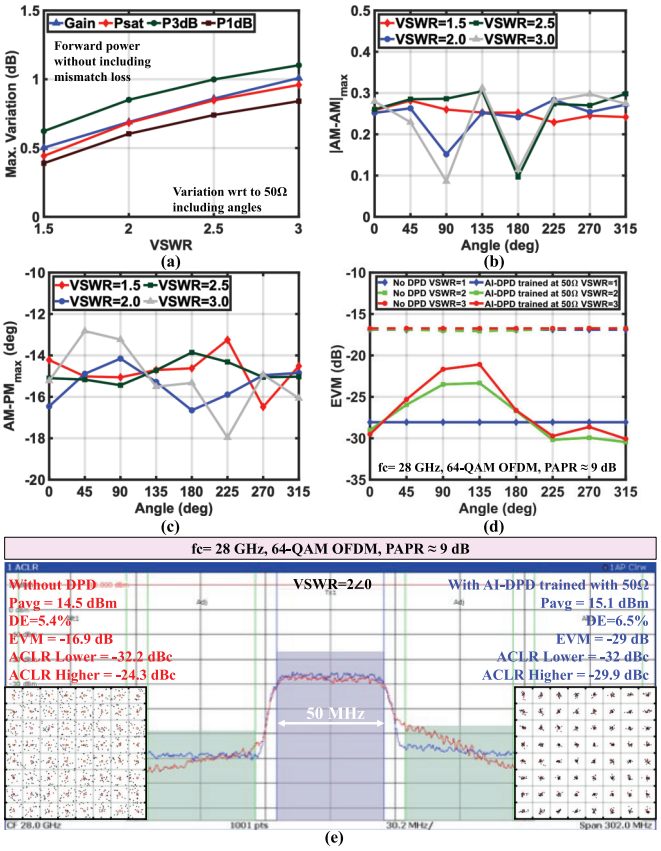


Fig. 21. (a) Gain/$P_{1\,\mathrm{dB}}$/$P_{3\,\mathrm{dB}}$/P_{sat} variation across VSWR, (b) maximum AM-AM error, (c) maximum AM-PM error across angles for different VSWR, (d) EVM versus VSWR angles for 50 MHz 64-QAM OFDM signal with and without AI-DPD trained at 50 Ω, and (e) spectrum and constellation for VSWR = 2° with and without AI-DPD trained at 50 Ω.

diagram illustrating the steps involved in AI-DPD can be found in the Appendix.

Fig. 20 shows the measured spectrum and constellation of 1-CC 64-QAM OFDM signals with 400/1000 MHz modulation bandwidths at 28 GHz with and without the AI-DPD. With the implementation of AI-DPD, the proposed PA meets the −25 dB EVM requirement for a 64-QAM signal at a similar average power. This enhances the $\mathrm{DE}_{\mathrm{avg}}$ and allows the proposed PA to operate closer to its saturated power. The related ACLR is also improved by 7 dB. It is noteworthy that the AI-DPD correction is restricted to up to the 1000 MHz modulation bandwidth as the AI-DPD algorithm requires a sampling rate of at least 3.5–4 times the baseband bandwidth to ensure adequate coverage of adjacent channels and effectively mitigate spurious leakage.

D. VSWR Results

As previously discussed, maintaining linearity, gain, and output power stability under load mismatch is critical for mm-wave phased-array systems. The VSWR resilience of the proposed PA is assessed by measuring its AM-PM characteristics and large-signal performance under various VSWR conditions. The PA's VSWR variation shown in Fig. 21(a) comprises Gain/$P_{1\,\mathrm{dB}}$/$P_{3\,\mathrm{dB}}$ (output power at 3-dB compression point)/P_{sat} variations at 28 GHz, demonstrating less than a 1.1 dB maximum variation over different VSWR angles. Its maximum AM-AM and AM-PM variations are less than 0.3 V and −18°, thus showing the VSWR resiliency of the proposed PA.

Fig. 21(e) exhibits measured constellations and spectrum of 1-CC 64-QAM OFDM signals with a 50 MHz modulation bandwidth at 28 GHz with and without the AI-DPD of the PA under VSWR = 2°. Notably, the AI-DPD model trained for VSWR = 1 or 50 Ω improves the EVM by more than 12 dB, achieving −29 dB with 15.1 dBm average power. The related ACLR is also improved. Fig. 21(d) exhibits EVM of 1-CC 64-QAM OFDM signals with 50 MHz modulation bandwidth at 28 GHz with and without the AI-DPD (trained at 50 Ω) under VSWR = 2/3, including eight different angles for 15 dBm average power. For VSWR = 3, the proposed PA achieves the lowest EVM of −21 dB, thanks to the VSWR resilient output network.

E. Comparison With State of the Art

The performance evaluation of the proposed 4 × 2-way Doherty PA is summarized in Table II and compared to that of previous designs with $P_{\mathrm{sat}} > 23$ dBm. The results highlight that even with a supply voltage of 2 V, our compact mm-wave front-end achieves P_{sat} of 25.2 dBm with a power gain of 25.5 dB. Furthermore, its core area (1.54 mm^2) is the second best among the PAs, achieving 25 dBm. The ITRS FoM is included to compare the overall performance [52], and the proposed PA has an FoM of 91.5 dB, which is the second best among efficiency-enhanced PAs. It also supports a 2 GHz 64-QAM OFDM signal with an average power of 11.3 dBm while meeting the EVM requirement of −25 dB. Notably, at 6/0 dB PBO, the DE maintains superiority over 10/17.5% across the same frequency spectrum of 26–32 GHz. The DE primarily drops at 6 dB PBO due to the lossy C_{ds} of the main

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

Specifications	This Work	Efficiency-Enhanced PAs					Mm-Wave 5G PAs		
		X.Zhang TMTT'24 [50]	X.Zhang ISSCC'24 [29]	W.Zhu ISSCC'24 [51]	Z.Ma ISSCC'22 [26]	C.Chappidi JSSC'18 [14]	M.Pashaeifar ISSCC'24 [8]	S.Daneshgar TMTT'20 [11]	H.Ahn RFIC'20 [10]
Architecture	4x2-way Parallel Doherty PA	Rat-race coupler based 4x2-way Doherty PA	4-way Doherty PA	7-Way LMBA PA	3-way Parallel Series Doherty PA	Dual frequency-PBO reconfigurable PA	Chain-Weaver 8-way Balanced PA	2-stacked 4-way power combined PA	8-way Power Combiner
Technology	40 nm CMOS	45 nm SOI	45 nm SOI	65nm CMOS	55 nm CMOS	130 nm SiGe BiCMOS	40 nm CMOS	28nm CMOS	65 nm CMOS
Supply (V)	2(PA) 1(DRV/PDRV)	2.2	2,1	1	2.4, 1.2^{+}	4,1.6	2,1	2.2	NA
Oper. Freq. (GHz)	26-32	34.5-40	42.5-50	27.8-38.7	26-30	30-55	35-43	36.5-42	27-28
Freq. (GHz)	28	37	47	28	28	40	37	39	28
Core Area (mm^2)	1.54	1.84	0.81	2.2	0.54	0.96	2.08	0.95	0.25
Gain (dB)	25.5	18.5	17.1	17	16.1	23.4^{++}	29.9	38	15.9
P_{sat} (dBm)	25.2	27.5	24	26.2	25.5	23.7	25.2	26	23.2
DE_{sat}/PAE_{sat} (%)	20.5/15.3	NA/18	30*/26.8	30*/25.4	32.5/25.2	35*/26	NA/16.2	NA/26.6	NA/33.5
DE_{6dB}/PAE_{6dB} (%)	13.3/8.6	NA/15	24*/21.7	22*/19.7	25.4/20.4	22.5*/16.5*	NA	NA/10.4*	NA/15*
ITRS FoM (dB)	91.5	89.6	88.8	86.2	84.6	93.3	98.6	110.1	83.3
Modulation Scheme	64-QAM OFDM	64 QAM	64 QAM OFDM	64 QAM	64 QAM	16 QAM	64 QAM OFDM	64 QAM OFDM	256 QAM
Data rate (Gb/s)	12/6/2.4	2.4	12	4.5	1.5#	4	12	0.6	0.8
Modulation BW (MHz)	2000/1000/400	400	2000	750	250	1000	2000	100	100
EVM_{rms} (dB)	-25/-24.6/-25.5	-25.1	-25	-26.8	-25.2	-19.2	-25	-28.5*	-31.2
ACLR (dBc)	-33/-32/-35.3	-26.2	-30.5	-32.7	-27	-30	-30.7	-33*	-30
P_{avg} (dBm)	11.3/15.5/15.3	18.5	14.1	17.3	17.7	16.9	16	19.5	18.2
PAE_{avg} (%)	4/6/7.2 (DE_{avg})	10.9	13.7	13.9	17.5	24.6	4.1	8.3	17.6
DPD	No#/Yes/Yes (AI-DPD)	No	No	No	No	Yes	No	Yes	No
Output Config.	SE	DE	DE	SE	SE	SE	SE	SE	SE

NA - Not Available. SE - Single-ended. DE - Differential-ended. #limited by equipment. *Graphically estimated. +Nominal voltage of the technology. ++Gain at P_{sat}.
ITRS FoM = P_{sat}(dBm) + Gain(dB) + $10log_{10}(PAE_{max}[\%])$ + $20log_{10}(f_c[GHz])$ [52].

PA [31], [32]. The proposed 4 × 2-way Doherty PA is resilient to VSWR, thanks to QHC included in the compact output network.

With assistance from DPD, the proposed PA can meet the linearity requirement for a 1 GHz 64-QAM OFDM signal at an average power of 15.5 dBm. The proposed PA preserves its required linearity and improves its average power while achieving the required EVM of −21.9 dB across VSWR of 2. Meanwhile, the DPD needs to be trained only at 50 Ω, thus reducing training time, thanks to the VSWR resilience of the proposed PA.

VI. CONCLUSION

A mm-wave 4 × 2-way Doherty PA has been implemented that features a high P_{out} and gain. The design procedure for implementing the output network has been thoroughly explained. The proposed PA is fabricated using 40 nm CMOS technology, occupying a core area of 1.54 mm^2. The realized front-end operating at 28 GHz demonstrates a power gain of 25.5 dB, a peak power of 25.2 dBm, and a DE of 20.5 %/15.3 % at PBO levels of 0/6 dB. It attains an EVM and ACLR of −25 dB/−32 dBc for a 1000 MHz 64-OFDM signal with a P_{avg} of 11.5 dBm and a 4 % DE_{avg}. For an 800 MHz 256-QAM OFDM signal, the proposed PA achieves EVM/ACLR of −30 dB/−39 dBc with a P_{avg}/DE_{avg} of 8.3 dBm/2 %. It is also resilient to VSWR variations, keeping gain and $P_{1\,dB}$ deviation less than 1 and 0.8 dB, respectively. With the help of AI-DPD, the proposed PA can achieve a P_{avg} of 15.3 dBm for 400 MHz 64-QAM OFDM signal, thus improving DE_{avg}. These results make it a promising choice for adoption in 5G mm-wave TXs or phased arrays.

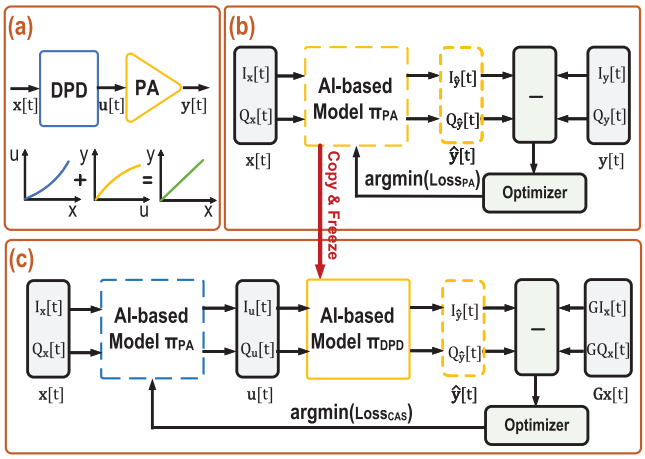


Fig. 22. (a) Basic concept of DPD. (b) Step 1 of OpenDPD training process: PA modeling. (c) Step 2 of OpenDPD training process: DPD learning.

APPENDIX

The linearization of Doherty PAs typically relies on DPD to approximate the inverse function of the PA. This study introduces an off-chip, deep RNN-based AI-DPD framework utilizing a GRU regressor for PA modeling and DPD learning [53] to address the challenges conventional DPD methods face with increasing modulation bandwidth due to growing memory effects [54]. Implementation occurs in three phases: data acquisition, algorithm training, and deployment. The process generates ideal baseband input in MATLAB, passes through the mm-wave 4 × 2-way Doherty PA setup, and then downconverts and digitizes via a spectrum analyzer (R&S FSW43). To

effectively mitigate spurious leakage, the sampling rate must be at least 3–4 times the baseband bandwidth.

Algorithm training uses the open-source OpenDPD platform [53] in two steps, as illustrated in Fig. 22. First, a GRU-based PA model (π_{PA}) is trained using acquired baseband signals, minimizing discrepancies between π_{PA} outputs and the physical PA. Once complete, π_{PA} coefficients are copied and frozen. Then, another GRU-based DPD model (π_{DPD}) with identical architecture is cascaded with the frozen π_{PA}. This cascaded model trains via gradient descent to emulate a linear PA with gain G, enabling π_{DPD} to learn the inverse function while addressing memory effects through the RNN's time-sequential modeling capability.

After achieving satisfactory linearization performance, the algorithm generates the predistorted signal $u[t]$ as shown in Fig. 22, which serves as Doherty PA input for experimental linearization testing.

ACKNOWLEDGMENT

The authors would like to thank Z. Y. Chang, E. Shokrolahzade, C. De Martino, Dr. Bueno, G. D. Singh, and Dr. M. Spirito for their support and helpful discussions. They also thank IMEC Leuven, Leuven, Belgium, for handling the tape-out.

REFERENCES

[1] E. G. Larsson, O. Edfors, F. Tufvesson, and T. L. Marzetta, "Massive MIMO for next generation wireless systems," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 186–195, Feb. 2014.

[2] M. Shafi et al., "5G: A tutorial overview of standards, trials, challenges, deployment, and practice," *IEEE J. Sel. Areas Commun.*, vol. 35, no. 6, pp. 1201–1221, Jun. 2017.

[3] I. Ahmed et al.., "A survey on hybrid beamforming techniques in 5G: Architecture and system model perspectives," *IEEE Commun. Surveys Tuts.*, vol. 20, no. 4, pp. 3060–3097, 4th Quart., 2018.

[4] T. Tuovinen, N. Tervo, and A. Pärssinen, "Analyzing 5G RF system performance and relation to link budget for directive MIMO," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6636–6645, Dec. 2017.

[5] P. M. Asbeck, N. Rostomyan, M. Özen, B. Rabet, and J. A. Jayamon, "Power amplifiers for mm-wave 5G applications: Technology comparisons and CMOS-SOI demonstration circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3099–3109, Jul. 2019.

[6] H. Wang, P. M. Asbeck, and C. Fager, "Millimeter-wave power amplifier integrated circuits for high dynamic range signals," *IEEE J. Microw.*, vol. 1, no. 1, pp. 299–316, Jan. 2021.

[7] B. Sadhu et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[8] M. Pashaeifar, A. K. Kumaran, L. C. N. De Vreede, and M. S. Alavi, "32.7 a 25.2dBm PSAT, 35-to-43 GHz VSWR-resilient chain-weaver eight-way balanced PA with an embedded impedance/power sensor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 532–534.

[9] K. Dasgupta, S. Daneshgar, C. Thakkar, J. Jaussi, and B. Casper, "A 26 dBm 39 GHz power amplifier with 26.6% PAE for 5G applications in 28nm bulk CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 235–238.

[10] H. Ahn, I. Nam, and O. Lee, "A 28-GHz highly efficient CMOS power amplifier using a compact symmetrical 8-way parallel-parallel power combiner with IMD3 cancellation method," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 187–190.

[11] S. Daneshgar et al., "High-power generation for mm-wave 5G power amplifiers in deep submicrometer planar and FinFET bulk CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 6, pp. 2041–2056, Jun. 2020.

[12] D. Manente, F. Padovan, D. Seebacher, M. Bassi, and A. Bevilacqua, "A 28-GHz stacked power amplifier with 20.7-dBm output P1dB in 28-nm bulk CMOS," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 170–173, 2020.

[13] N. Rostomyan, M. Özen, and P. Asbeck, "28 GHz Doherty power amplifier in CMOS SOI with 28% back-off PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 446–448, May 2018.

[14] C. R. Chappidi, X. Wu, and K. Sengupta, "Simultaneously broadband and back-off efficient mm-Wave PAs: A multi-port network synthesis approach," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2543–2559, Sep. 2018.

[15] Y.-C. Chen, Y.-H. Lin, J.-L. Lin, and H. Wang, "A Ka-band transformer-based Doherty power amplifier for multi-Gb/s application in 90-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 12, pp. 1134–1136, Dec. 2018.

[16] F. Wang, T.-W. Li, S. Hu, and H. Wang, "A super-resolution mixed-signal Doherty power amplifier for simultaneous linearity and efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3421–3436, Dec. 2019.

[17] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz linear Doherty power amplifier in silicon for 5G applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, Jun. 2019.

[18] Z. Zong et al., "A 28-GHz SOI-CMOS Doherty power amplifier with a compact transformer-based output combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 6, pp. 2795–2808, Jun. 2021.

[19] N. S. Mannem, T.-Y. Huang, and H. Wang, "Broadband active load-modulation power amplification using coupled-line baluns: A multifrequency role-exchange coupler Doherty amplifier architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3109–3122, Oct. 2021.

[20] S. Kim, H.-C. Park, D. Kang, D. Minn, and S.-G. Yang, "A 24.5–29.5GHz broadband parallel-to-series combined compact Doherty power amplifier in 28-nm bulk CMOS for 5G applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 171–174.

[21] T.-Y. Huang, N. S. Mannem, S. Li, D. Jung, M.-Y. Huang, and H. Wang, "26.1 a 26-to-60GHz continuous coupler-Doherty linear power amplifier for over-an-octave back-off efficiency enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 354–356.

[22] M. Pashaeifar, L. C. N. de Vreede, and M. S. Alavi, "A millimeter-wave mutual-coupling-resilient double-quadrature transmitter for 5G applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3784–3798, Dec. 2021.

[23] F. Wang and H. Wang, "A high-power broadband multi-primary DAT-based Doherty power amplifier for mm-wave 5G applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1668–1681, Jun. 2021.

[24] M. Pashaeifar, L. C. N. de Vreede, and M. S. Alavi, "A millimeter-wave CMOS series-Doherty power amplifier with post-silicon inter-stage passive validation," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 2999–3013, Oct. 2022.

[25] X. Zhang, S. Li, D. Huang, and T. Chi, "A 38GHz deep back-off efficiency enhancement PA with three-way Doherty network synthesis achieving 11.3dBm average output power and 14.7% average efficiency for 5G NR OFDM," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2022, pp. 239–242.

[26] Z. Ma, K. Ma, K. Wang, and F. Meng, "A 28GHz compact 3-way transformer-based parallel-series Doherty power amplifier with 20.4%/14.2% PAE at 6-/12-dB power back-off and 25.5dBm PSAT in 55nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 320–322.

[27] A. K. Kumaran, M. Pashaeifar, H. M. Nemati, L. C. N. de Vreede, and M. S. Alavi, "A 26GHz balun-first three-way Doherty PA in 40nm CMOS with 20.7 dBm psat and 20dB power gain," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2023, pp. 189–192.

[28] M. Mortazavi, Y. Shen, D. Mul, L. C. N. de Vreede, M. Spirito, and M. Babaie, "A four-way series Doherty digital polar transmitter at mm-Wave frequencies," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 803–817, Mar. 2022.

[29] X. Zhang, H. Guo, and T. Chi, "32.1 a 47GHz 4-way Doherty PA with 23.7dBm P1dB and 21.7% / 13.1% PAE at 6 / 12dB back-off supporting 2000 MHz 5G NR 64-QAM OFDM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 520–522.

[30] A. K. Kumaran, H. M. Nemati, L. C. N. De Vreede, and M. S. Alavi, "Compact N-way Doherty power combiners for mm-wave 5G transmitters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2022, pp. 438–442.

[31] G. D. Singh, H. M. Nemati, M. S. Alavi, and L. C. N. de Vreede, "An inverted Doherty power amplifier insensitive to load variation with an embedded impedance sensor in its output power-combining network," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 12, pp. 5194–5208, May 2023.

[32] A. K. Kumaran, M. Pashaeifar, M. Alexanderson, L. C. N. D. Vreede, and M. S. Alavi, "A single-supply balun-first three-way mm-wave Doherty PA," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 5, pp. 2757–2772, May 2024.
[33] G. D. Singh, H. M. Nemati, and L. C. N. de Vreede, "A low-loss load correction technique for self-healing power amplifiers using a modified two-tap six-port network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 9, pp. 4069–4081, Sep. 2021.
[34] N. S. Mannem, M. Huang, T. Huang, and H. Wang, "A reconfigurable hybrid series/parallel Doherty power amplifier with antenna VSWR resilient performance for MIMO arrays," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3335–3348, Dec. 2020.
[35] M. Pashaeifar, L. C. N. de Vreede, and M. S. Alavi, "14.4 a 24-to-30GHz double-quadrature direct-upconversion transmitter with mutual-coupling-resilient series-Doherty balanced PA for 5G MIMO arrays," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 223–225.
[36] J. S. Park and H. Wang, "A transformer-based poly-phase network for ultra-broadband quadrature signal generation," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4444–4457, Dec. 2015.
[37] D. M. Pozar, *Microwave Engineering*, 4th ed., Hoboken, NJ, USA: Wiley, 2012.
[38] S. Y. Kim et al., "A low-power BiCMOS 4-element phased array receiver for 76–84 GHz radars and communication systems," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 359–367, Feb. 2012.
[39] J. Chen, P. Miao, and D. Zhao, "Analysis, design and modeling of millimeter-wave Wilkinson power combiner for 5G phased array," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2019, pp. 1–3.
[40] R. C. Frye, S. Kapur, and R. C. Melville, "A 2-GHz quadrature hybrid implemented in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 550–555, Mar. 2003.
[41] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, "An ultra-wideband IF millimeter-wave receiver with a 20 GHz channel bandwidth using gain-equalized transformers," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 323–331, Feb. 2016.
[42] M. Vigilante and P. Reynaert, "On the design of wideband transformer-based fourth order matching networks for {*E*} -band receivers in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, Aug. 2017.
[43] A. K. Kumaran, "Linear and efficient power amplifier for WiFi," M.S. thesis, Dept. Microelectronics, Delft Univ. Technol., Delft, The Netherlands, 2020. [Online]. Available: http://resolver.tudelft.nl/uuid:9370704d-a455-4a64-924e-ab428450327c
[44] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer—A new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.
[45] S. V. Thyagarajan, A. M. Niknejad, and C. D. Hull, "A 60 GHz drain-source neutralized wideband linear power amplifier in 28 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2253–2262, Aug. 2014.
[46] H.-T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-FET millimeter-wave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1543–1556, Apr. 2013.
[47] D. Zhao and P. Reynaert, "A 60-GHz dual-mode class AB power amplifier in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2323–2337, Oct. 2013.
[48] M. Vigilante et al., "A wideband class-AB power amplifier with 29–57-GHz AM–PM compensation in 0.9-V 28-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1288–1301, May 2018.
[49] H. T. Nguyen, T. Chi, S. Li, and H. Wang, "A linear high-efficiency millimeter-wave CMOS Doherty radiator leveraging multi-feed on-antenna active load modulation," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3587–3598, Dec. 2018.
[50] X. Zhang, S. Li, and T. Chi, "A millimeter-wave watt-level Doherty power amplifier in silicon," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 3, pp. 1674–1686, Mar. 2024.
[51] W. Zhu et al., "32.8 A 27.8-to-38.7GHz load-modulated balanced power amplifier with scalable 7-to-1 load-modulated power-combine network achieving 27.2dBm output power and 28.8%/23.2%/16.3%/11.9% Peak/6/9/12dB back-off efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 534–536.
[52] *International Technology Roadmap for Semiconductors 2001, System Drivers Edition, Semiconductor Ind. Assoc.*, San Jose, CA, USA, 2001, p. 10.
[53] Y. Wu, G. D. Singh, M. Beikmirza, L. C. N. De Vreede, M. Alavi, and C. Gao, "OpenDPD: An open-source end-to-end learning & benchmarking framework for wideband power amplifier modeling and digital pre-distortion," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2024, pp. 1–5.
[54] T. Kobal, Y. Li, X. Wang, and A. Zhu, "Digital predistortion of RF power amplifiers with phase-gated recurrent neural networks," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 6, pp. 3291–3299, Jun. 2022.

Anil Kumar Kumaran (Graduate Student Member, IEEE) received the B.Tech. degree in Electronics and Communication Engineering from Amrita Viswa Vidhyapeetham, Coimbatore, India, in May 2015, and the M.Sc. degree in Microelectronics from Delft University of Technology, Delft, The Netherlands, in August 2020, where he is currently pursuing the Ph.D. degree at the ELCA Research Group.

Before joining his master's degree, he worked as an Onsite Validation Engineer at Texas Instruments India, Bangalore, India. His research activity primarily focuses on designing linear and efficient mm-wave transmitters for 5G cellular applications.

Mr. Kumaran also serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (TCAS-II).

Yizhuo Wu (Graduate Student Member, IEEE) received the M.Sc. degree in Microelectronics from TU Delft, Delft, The Netherlands, in 2023.

She is currently a Ph.D. Student supervised by Dr. Chang Gao at the Laboratory of Efficient Circuits and Systems for Machine Intelligence (EMI), TU Delft. Her research focuses on software-hardware co-designed AI for I/Q signal processing, which aims to find energy-efficient solutions for high-frequency signal processing tasks.

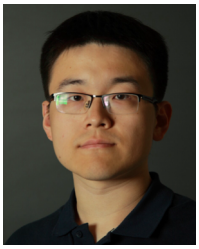
Masoud Pashaeifar (Member, IEEE) received the M.Sc. degree in circuits and systems from the University of Tehran, Tehran, Iran, in 2013, and the Ph.D. degree in Electrical Engineering from Delft University of Technology, Delft, The Netherlands, in 2024.

He led the Hardware Research Group, Bakhtar Communication Company, Tehran, from 2014 to 2018, focusing on wireless communication system design. From September 2022 to December 2024, he was with Apple Inc., Munich, Germany, as a Senior mm-Wave IC Design Engineer. He is currently with NXP Semiconductors, Eindhoven, The Netherlands, working as a Principal Wireless Connectivity Architect and Designer, where he develops next-generation communication systems. His research interests include mm-wave and sub-terahertz (THz) integrated circuit and system design for wireless communication and radar applications.

Dr. Pashaeifar received the IEEE Solid-State Circuits Society Predoctoral Achievement Award from 2021 - 2022. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SOLID-STATE CIRCUITS LETTERS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, IEEE MICROWAVE AND WIRELESS TECHNOLOGY LETTERS, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.

Hamza Nachouane (Member, IEEE) received the Ph.D. degree in Electronic and Telecommunications Engineering from the National Institute of Posts and Telecommunications, Rabat, Morocco, in 2017.

From 2018 to 2020, he was a Post-Doctoral Fellow with the Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden. He is currently a Senior RF Expert with Gothenburg Research Center, Huawei Technologies Sweden AB, Gothenburg. His research background and interests span a wide range of applications within telecommunications and sensing industries, including future energy-efficient base stations, transceiver circuits and architectures, MIMO antenna systems, and microwave electronics.



Chang Gao (Member, IEEE) received the joint bachelor's degree from the University of Liverpool, Liverpool, U.K., and Xi'an Jiaotong-Liverpool University, Suzhou, China, in July 2015, the master's degree from the Imperial College London, London, U.K., in September 2016, and the joint Ph.D. degree (Hons.) in neuroscience from the Institute of Neuroinformatics, University of Zürich, Zürich, Switzerland, and ETH Zürich, Zürich, in March 2022,

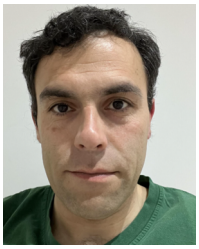
In August 2022, he joined Delft University of Technology, Delft, The Netherlands, as an Assistant Professor with the Department of Microelectronics, where he is leading the Laboratory of Efficient Machine Intelligence (EMI), working on research in neuromorphic algorithm-hardware co-design for edge AI and its applications in future wireless communications, computer vision, audio processing, and more.

Dr. Gao received the 2022 Misha Mahowald Early Career Award in Neuromorphic Engineering and the 2022 Marie-Curie Postdoctoral Fellowship. He is a 2023 Dutch Research Council (NWO) Veni laureate and a 2023 MIT Technology Review Innovator Under 35 in Europe for his contribution to algorithm-hardware co-design for efficient sparse recurrent neural network edge computing.

Leonardus Cornelis Nicolaas de Vreede (Senior Member, IEEE) received the Ph.D. degree (cum laude) from Delft University of Technology, Delft, The Netherlands, in 1996.

In 1996, he joined Delft University of Technology, an Assistant Professor, working on the non-linear distortion behavior of active devices. In 1999 and 2015, he was appointed as an Associate Professor and a Full Professor with Delft University of Technology, where he became responsible for the Electronics Research Laboratory (ERL/ELCA). He worked on solutions for improved linearity and RF performance at the device, circuit, and system levels. He is currently a Co-Founder/Advisor of Anteverta-MW, Eindhoven, The Netherlands, a company specializing in RF device characterization. He has co-authored more than 180 IEEE-refereed conference papers, journal articles, and over 20 patents. His current interests include RF measurement systems, RF technology optimization, and (digital-intensive) energy-efficient/wideband circuit/system concepts for wireless applications.

Prof. de Vreede was a co-recipient of the IEEE Microwave Prize in 2008 and a Mentor of the Else Kooi Prize Awarded for Ph.D. Work in 2010 and the Dow Energy Dissertation Prize Awarded for Ph.D. Work in 2011. He received the Delft University of Technology (TUD) Entrepreneurial Scientist Award in 2015. He co-guided several students who won (best) paper awards at various conferences.



Morteza S. Alavi (Senior Member, IEEE) was born in Tehran, Iran. He received the B.S.E.E. degree from Iran University of Science and Technology, Tehran, in 2003, the M.S.E.E. degree from the University of Tehran, Tehran, in 2006, and the Ph.D. degree in Electrical Engineering from Delft University of Technology (TU-Delft), Delft, The Netherlands, in 2014.

He was the Co-Founder and the CEO of DitIQ B.V., Delft, a local company developing energy-efficient, wideband wireless transmitters for the next generation of the cellular network. Since September 2016, he has been with the Electronic Circuits and Architectures (ELCA) Research Group, TU-Delft, where he is currently an Associate Professor. He has co-authored the book *Radio-Frequency Digital-to-Analog Converter* (Elsevier, 2016). His primary research interest is designing high-frequency and high-speed wireless/cellular communication and sensor systems, as well as in the field of wireline transceivers.

Dr. Alavi was a recipient of the Best Paper Award of the 2011 IEEE International Symposium on Radio-Frequency Integrated Technology (RFIT). He received the Best Student Paper Award (Second Place) at the 2013 Radio-Frequency Integrated Circuits (RFIC) Symposium. His Ph.D. student also won the Best Student Paper Award (First Place) of the 2017 RFIC Symposium held in Honolulu, HI, USA. His master's student received the 2021 Institute of Semiconductor Engineers (ISE) President Best Paper Award of the International SoC Design Conference (ISOCC). He was a co-recipient of the 2022 Best Paper Award of the honorable mentioned IEEE Brain and SSCS Joint Communities paper.