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# Low-Offset Band-Pass Signal Shaper with High Time Resolution in 40 nm CMOS Technology

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***Abstract*— State-of-the-art readout integrated circuits (ROICs) operating in particle-counting mode are gravitating toward high time resolution, low-noise, and low-power analog readout frontends to detect and register the arrival time of charge signals with a high accuracy. To achieve a time resolution of a few nanoseconds, an intermediate stage, known as a signal shaper block, is the preferred solution in the readout frontend, as it compensates for the inter-symbol interference-induced errors by realizing a band-pass transfer function. This paper presents the design methodology and experimental characterization of a state-of-the-art, high time resolution, low-offset, and power-efficient band-pass signal shaper block intended for fitting the voltage signals generated by a charge-sensitive amplifier (CSA) as a function of charge signals as small as 160 aC, into timeframes of 2.5 ns with 17 times offset attenuation while consuming 0.17 mW of power. Detailed information about the operation principle of this CSA, designed in TSMC 40 nm MS/RF CMOS technology, is reported in a previous publication.**

***Keywords— readout integrated circuit ROIC, analog frontend, charge-sensitive amplifier, signal shaper block, low-offset, low-noise, power-efficient, high time resolution***

## I. Introduction

The advanced world of industrial technology leverages breakthrough instrumentation and imaging devices as inspection and metrology tools. Modern imaging systems, such as scanning electron microscopes (SEMs), have been elaborately investigated, probed, and developed to be used in a plethora of fields including: particle- and astrophysics, material science, biology, and many other applications [1] - [4]. To achieve a better performance, the SEM has to operate with a smaller primary current, leading to a weaker signal reaching the detector. This, combined with the need for fast scanning, demands a high time resolution, resulting in single electron counting [5].

Manifold applications and system constraints have motivated the evolution, expansion, and development of various readout architectures for the sensor readout frontend. The tendency with state-of-the-art imaging systems is to design low-power and low-silicon area occupation readout frontends with high time resolution and high accuracy in hit registration [6].

To accurately register the weak and high event-rate charge signals produced by the detector as a result of a detected electron, a high bandwidth, low-noise analog frontend is often required. This can be attained by cascading a few stages (Fig. 1) comprised of a preamplifier, which provides the interface for the detector, a signal shaper for generating an output signal with a well-defined shape, and a threshold discriminator for distinguishing the signal concerning the noise level as well as digitizing the hit data [7], [8].

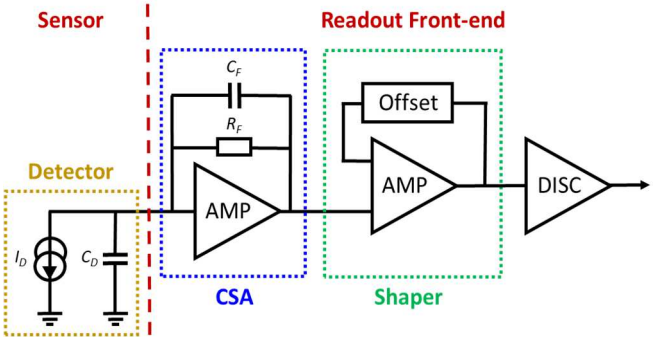


Fig. 1. Simplified block diagram of the readout frontend electronics.

The target is to realize a particle-counting mode of operation in the analog frontend by detecting charge signals equivalent to 160 aC (equivalent to 1000 electrons) with a time resolution of 2.5 ns, allowing an event rate up to 400 MEvents/s, and a power consumption of less than 500 µW [6], [8], [9].

In [8] and [9], as a tradeoff between noise and bandwidth, a preamplifier operating in a charge-sensitive mode (i.e. CSA) is proposed and evaluated through experimental tests converting charge into voltage signals with a sufficient SNR and minimum power consumption. However, due to the limited bandwidth, the voltage signals after the CSA show up with a long tail in the time domain. Moreover, the drift of the DC level (offset) at the CSA output is not controlled sufficiently, which can deteriorate the detection accuracy [6]. Therefore, in order to fit within timeframes of 2.5 ns by eliminating the tail of the CSA voltage signal and compensating the associated offset, implementing an intermediate stage known as signal shaper block is necessary. Moreover, thanks to signal amplification in the signal shaper block, the offset associated with the discriminator will play a less significant role in detection accuracy; hence, it can be eliminated as a minor contribution.

Signal shaper blocks are widely used in many imaging frontends [10] to measure the energy of the input charge signal with a high resolution. Thus, the transfer function of the signal shaper blocks contains a set of complex conjugate poles which makes them operate with much fewer constraints on signal processing speed and power consumption. As an example, in the X-ray detector frontends in [11] and [12], the signal shaper

block accommodates the voltage signal generated by the CSA as a function of a different set of input charges into timeframes of 200 ns . However, for the particle-counting mode of operation, such a complex transfer function is not required. Here, the key is to realize a band-pass transfer function for the signal shaper block to eliminate the tail of the CSA voltage signal and compensate for the inter-symbol interference (ISI) [6], [9].

This paper presents the design of a high time resolution, low-offset, power-efficient band-pass signal shaper block in 40 nm CMOS technology as well as the experimental qualification tests implemented to monitor and characterize its functionality and performance. Section II presents the operation principle, transfer function, and the challenges associated with the design of the signal shaper block. In Section III, the sub-building blocks of the signal shaper (i.e., amplifiers, filtering, and offset cancelation loop) are presented. Section IV introduces the measurement setup and provides the experimentally obtained performance results. The paper ends with conclusions.

## II. Signal Shaper Block

The main objective behind the design of the readout frontend is to realize the particle counting mode for registering the arrival moment of high event-rate charge signals. Regarding the operation of the CSA presented in [8] and [9], such data are encrypted in the rising edge of the CSA output voltage signal which can be further processed in the digital domain after discrimination with respect to a reference level. However, due to the limited bandwidth of the low-noise CSA, its output voltage signal shows up with a long tail in time domain which, for a consecutive set of events, gives rise to signal pileup. Thus, in the case of direct discrimination after the CSA block, the detection accuracy will deteriorate due to the ISI-induced errors [6]. This phenomenon is shown in Fig. 2.

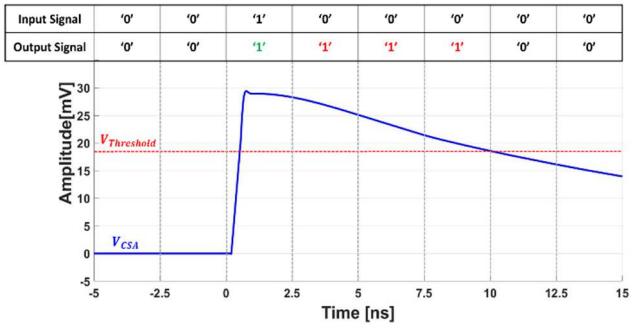


Fig. 2. Example of direct discrimination after the low-bandwidth CSA. The blue solid line represents the voltage signal after the CSA while the red dashed line illustrates the threshold voltage level.

Known as a deterministic source of error, ISI-induced errors can be mitigated by adding a small amount of architectural complexity. When modeling the signal pileup as a shift of the signal baseline, the signal shaper block must include a baseline restorer (BLR) loop to eliminate the low frequency contributions of the input signal. In other words, the low frequency contributions of the voltage signal after the CSA (including the falling phase of the voltage signal and the offset of the CSA) are wiped out while the high frequency contributions (including the rising phase of the CSA voltage signal) are passed. With respect to the aforementioned expected performance, the signal shaper block should realize a transfer function for the band-pass filter in the frequency domain (Fig. 3). The attenuation factor $A_1$ and the frequency of the transfer function zero $f_1$ should be carefully set to maximize the SNR while limiting the signal time-width after the signal shaper block.

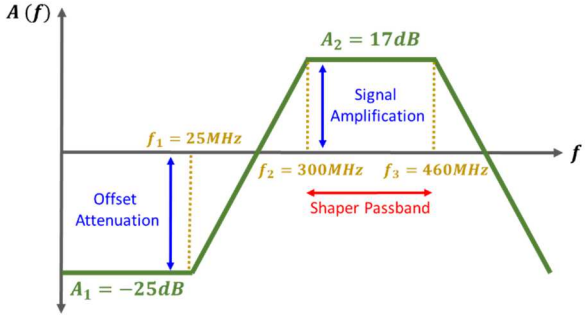


Fig. 3. Expected transfer function of the signal shaper block.

Once the transfer function is known, in the next step, the optimum architecture at the system level must be chosen for implementation. As shown in Fig. 4, a possible approach is to design the signal shaper block operating in closed-loop mode with amplifiers in a forward path, and a low-pass network in the feedback branch. The feedback branch, which realizes the BLR function, diminishes the gain of the transfer function by a factor of $G_{Loop}(0)$ at low frequencies, while at frequencies higher than its first pole, the transfer function of the shaper follows the behavior of the forward path. The idea behind the BLR is to track the low frequency contributions of the signal after amplification in the forward path and then subtract them from the signal at the input of the signal shaper block. In this way, the desired transfer function is realized. Thanks to the implemented negative loop, the system continuously tracks the voltage at the shaper output node and tries to fix it to a reference DC level $V_{ref}$ to eliminate the low frequency noise contributions and diminish any offset associated with the CSA and shaper sub-blocks by a factor of $A_1$ while the signal of interest is amplified by a factor of $A_2$. The voltage $V_{ref}$ is set equivalent to the desired DC voltage level at the output node of the signal shaper block.

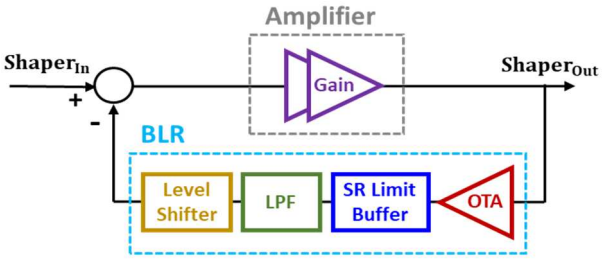


Fig. 4. Block diagram of the signal shaper block.

The BRL includes the following sub-blocks: an OTA followed by a slew-rate limited stage and a low-pass filter. The OTA compares the shaper output node with $V_{ref}$ in order to drive the slew-rate limited stage with a voltage signal once $V_{ref}$ is exceeded. The slew-rate limited stage generates a blunt voltage signal, as a function of the OTA output, to drive the low-pass filter. The motivation for adding the slew-rate limited stage in the BLR chain is to minimize the charge stored in the capacitor of the low-pass filter to shrink the amplitude of the undershoot at the shaper output [13].

By setting the bandwidth of the BLR chain, the low-pass filter integrates the signal provided by the slew-rate limited buffer to both record the low frequency contributions of the

signal and track the tail of the CSA voltage signal in the time domain. The signal generated by the low-pass filter is applied to the differential amplifier in the forward path to close the loop and subtract it from the CSA voltage signal. The simulated signals generated after each sub-block of the signal shaper block are shown in Fig. 5.

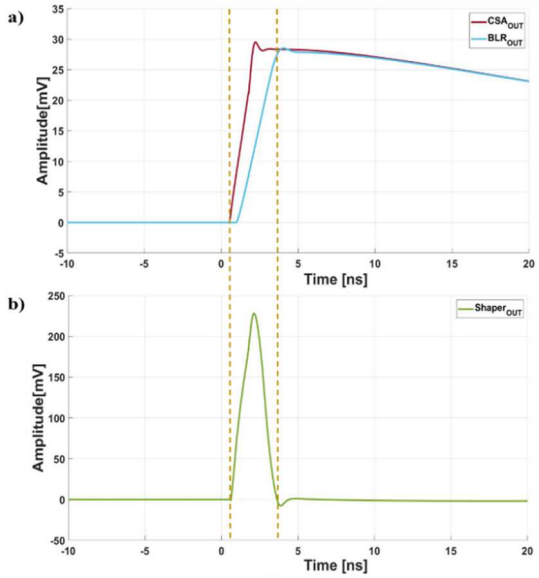


Fig. 5. Simulated signals generated after each sub-block of the signal shaper block: (a) CSA and BLR output signals, (b) shaper output signal.

Regarding the application requirements, the transfer function parameters should be set to provide and indicate the design specs. The attenuation factor $A_1$ should be larger than 20 dB to sufficiently attenuate both the offset and the tail of the CSA voltage signal. The gain of the passband $A_2$ should be larger than 15 dB to provide amplification; however, this gain cannot be too large for stability reasons. Moreover, regarding the rise time of the CSA voltage signal $t_r = 2.56$ ns [8], the central frequency of the band-pass should be set at 380 MHz with a margin of 80 MHz on the side bands. Hence, the first pole $f_1$ of the BLR should be set at 25 MHz. With respect to the power consumption of the already designed CSA and the overall power budget, the signal shaper block must have a power consumption of less than 200 µW.

## III. Signal Shaper Building Blocks

As shown in Fig. 4, the signal shaper has two cascaded amplifiers in the forward path and the BRL chain in the feedback branch. The BLR chain including an OTA followed by a slew-rate limited buffer stage and a low-pass filter. To achieve the best tradeoff between speed, noise, offset dispersion, and power compensation, it is beneficial all building blocks to be designed with a simple circuit topology.

### A. Amplifiers

The amplifiers of the forward path boost the signal voltage level to make it less prone to the digitization errors associated with the discriminator. As a tradeoff between the gain, noise, and power consumption, two differential amplifiers (Fig. 6) are connected in series. Both stages are designed with short channel devices to provide wide bandwidth with a sufficient gain. The first stage provides differential output while the second stage has a single-ended output to load the discriminator. When cascading the amplifiers, the overall DC gain is 17 dB with the first pole at 460 MHz.

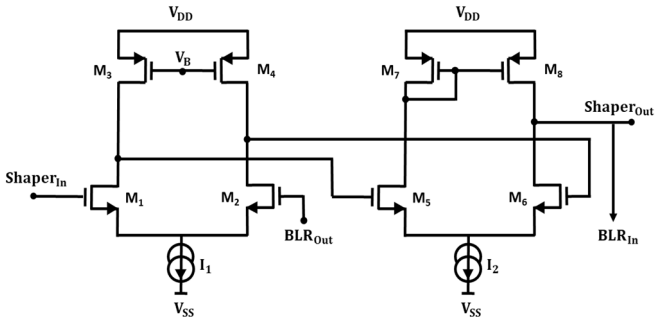


Fig. 6. Schematic of the amplifiers in the forward path.

### B. OTA and Slew-Rale Limited Buffer

The differential OTA generates voltage signals when the signal after the amplifiers in the forward path exceeds the reference voltage $V_{ref}$. The slew-rate limited buffer is a PMOS device in a common-source configuration with 1 uA bias current followed by a large capacitor to limit the slope of the OTA voltage signal while charging $C_{SR}$. The architecture, illustrated in Fig. 7, provides high-speed signal processing with reasonable power consumption. The critical design parameter for the OTA is its offset voltage, which is mitigated thanks to the overall negative loop and proper sizing of the transistor devices.

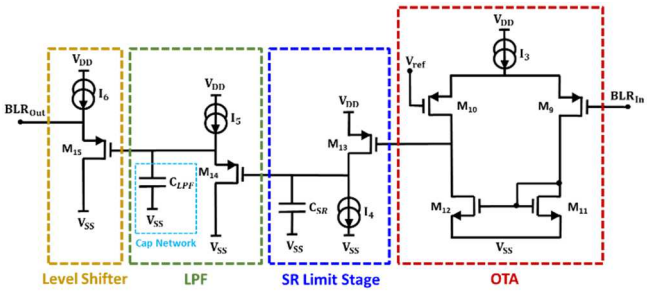


Fig. 7. Schematic of the OTA, slew-rate limited stage, low-pass filter, and level-shifter in the BLR chain.

### C. Low-Pass Filter

The low-pass filter sets the bandwidth of the BLR chain (zero of the overall transfer function $f_1$) by its pole. The low-pass filter is implemented, as shown in Fig. 7, by a source follower branch biased with 10 nA current and a programmable capacitor network in the range of 400 fF to 800 fF to set the pole at the desired frequency for tunability purposes. There is a level-shifter stage after the low-pass filter to retrieve the DC level of the BLR chain and close the loop.

## IV. Experimental Results

The goals of the qualification tests are to experimentally verify if the signal shaper block can compensate for the ISI-induced errors by eliminating the offset associated with both the CSA and sub-blocks of the signal shaper block, as well as to wipe out the tail of the CSA voltage signals in the time domain to fit them into time frames of 2.5 ns at the discrimination level. It is worth mentioning that the discrimination level is set at 8 times the noise power to attain the desired detection accuracy.

In this experiment, to only focus on the performance and the operation accuracy of the signal shaper block, the detector is substituted by an equivalent network emulating its characteristics [8], [14]. This equivalent network provides

current pulses with a desired equivalent charge at the CSA input as a function of the trigger pulses generated by an FPGA device. Thanks to the programmability of the CSA feedback components, it can be configured in high or low gain modes for $C_F = 5$ fF and $C_F = 10$ fF as well as slow and fast modes for $R_F \approx 11$ MΩ and $R_F \approx 5.3$ MΩ, respectively [8]. The CSA, programmed in high-gain and slow modes, converts the current pulses into voltage signals with an amplitude of $V_{Amp} = 29.45$ mV, a short rise time of $t_r = 2.56$ ns, and a relatively long time-width of $t_{width} = 286.91$ ns [8], [9].

Figure 8 illustrates the micrograph of the chip directly bonded to the PCB. The experimental tests are performed to evaluate the operation principle and characterize the performance of the signal shaper block for different sets of voltage signals generated by the CSA. It is worth mentioning that the experimental tests are repeated 100 times to reduce the noise and eliminate the high-frequency components of the signal during the characterization; thus, the reported values are averaged 100 times.

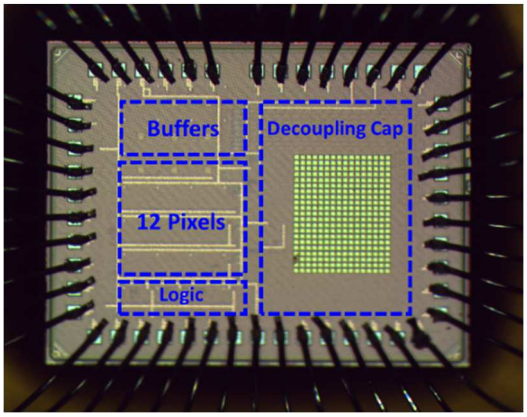


Fig. 8. Chip micrograph including 12 pixels, buffers, logic, and decoupling capacitors.

Thanks to the programmability of the parameters of the signal shaper block, the value of the reference voltage $V_{ref}$ and the frequency of the pole in low-pass filter are tunable. The $V_{ref}$ can be tuned by either a potentiometer implemented on the PCB or a resistive network implemented on the chip. The pole of the low-pass filter can be tuned in a range from 15 MHz to 28 MHz by changing the capacitance value ($C_{LPF}$), through programming a capacitive network, in a range from 400 fF to 800 fF.

Figure 9 presents the measured voltage signal of the signal shaper block for $C_{LPF} = 500$ fF and $V_{ref} = 450$ mV once the CSA is fired by a single trigger pulse from the FPGA. For a CSA programmed in high-gain and slow modes, the signal shaper block generates voltage signals of $V_{Amp} = 220.4$ mVand a time-width of $t_{Width} = 2.91$ ns. Moreover, for a CSA programmed in high-gain and fast modes, the signal shaper block generates voltage signals of $V_{Amp} = 200.2$ mV and a time-width of $t_{Width} = 3.04$ ns. As can be seen, the signal shaper block generates voltage signals with a short time-width by eliminating the tail of the CSA voltage signal in the time domain. In addition, regardless of the CSA operating mode, the generated voltage signals have a relatively equal time-width.

Table I summarizes the measured characteristics of the signal shaper block for $C_{LPF} = 500$ fF and $V_{Ref} = 450$ mV in different programming modes of the CSA. With regard to the numbers already presented in Table I, the time-widths of the voltage signals after the signal shaper block are larger than timeframes of 2.5 ns; however, as noted in Section II, the signal time-width at the discrimination level should be less than 2.5 ns. As reported in Table I and verified through experimental qualification tests, the time-width of the voltage signal after the signal shaper block at the discrimination level set at 8 times the noise power meets the target characteristic.

Figure 10 illustrates the signal time-width after the signal shaper block as a function of the trimmable capacitor of the low-pass filter $C_{LPF}$ in the BLR chain. As expected, the time-width of the voltage signal expands once the $C_{LPF}$ value increases. The signal shaper block has a power consumption of 0.17 mW and occupies an area of 34 µm × 18 µm.

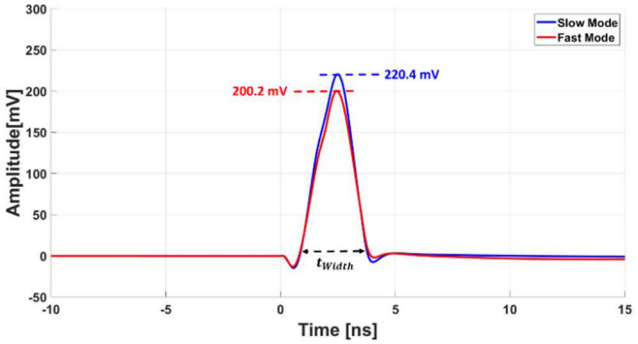


Fig. 9. Measured voltage signal of the signal shaper block for $C_{LPF} = 500$ fF and $V_{ref} = 450$ mV for a high gian CSA programmed in slow (blue line) and fast (red line) modes.

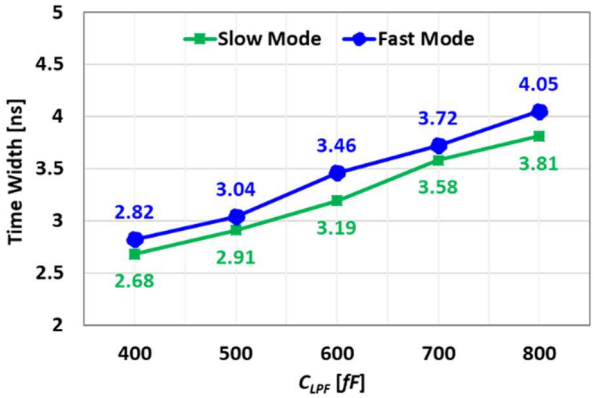


Fig. 10. Signal time-width as a function of a capacitor $C_{LPF}$ in a BLR chain for a CSA programmed in slow and fast modes.

TABLE I. MEASURED CHARACTERISTICS OF THE SIGNAL SHAPER BLOCK FOR $C_{LPF} = 500\,fF$ AND $V_{ref} = 450\,mV$ AND DIFFERENT PROGRAMMING MODES OF THE CSA

| CSA Program Mode | High Gain | | Low Gain | |
|---|---|---|---|---|
| | Slow | Fast | Slow | Fast |
| $V_{Amp}$ [mV] | 220.4 | 200.2 | 115.3 | 107.2 |
| $\sigma_{Noise}$ [$mV_{rms}$] | 16.08 | 14.32 | 14.87 | 13.44 |
| SNR | 13.7 | 13.9 | 7.75 | 7.97 |
| $t_{Width}$ [ns] | 2.91 | 3.04 | 2.27 | 2.43 |
| $t_{Width}$ @$8\sigma_{Noise}$ [ns] | 1.71 | 1.62 | - | - |

Probing the shaper performance for a set of consecutive trigger pulses is another important characteristic to be presented for this application. This qualification test illustrates how the introduced concept compensates the ISI-induce errors in such a harsh case. Figure 11 illustrates the voltage signals after the signal shaper block for a set of three consecutive trigger pulses while the CSA is programmed in slow and fast modes. As illustrated, there is still a small order of signal pileup after the signal shaper block which comes from the fact that the generated voltage signals do not ideally fit in timeframes of 2.5 ns . However, the amplitude of the remainder of the signal in the next time frame is 7% of the maximum value; hence, such a pileup is negligible. In this regard, the signal shaper block can compensate for the ISI-induced errors and generate voltage signals to be fit in timeframes of 2.5 ns after discrimination. Setting the threshold level $V_{Th}$ in the shown range, the discriminator would generate three digital pulses in three consecutive time frames with the desired accuracy. In addition, as seen in Fig. 11, the signal amplitude for the second and third signals does not follow a linear trend, although the ratio of the remainder of signal to pileup is expected to maintain a constant value. This is because the CSA does not provide the same gain for the signals in the second and third timeframes due to gain compression, as noted in [8].

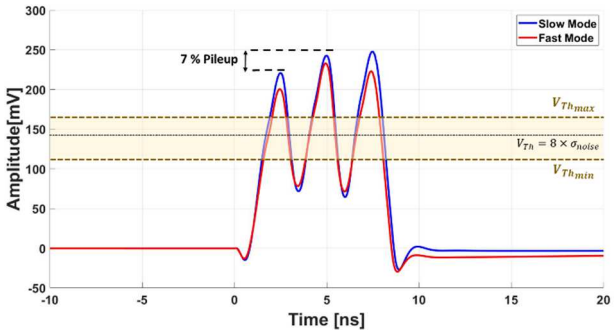


Fig. 11. Voltage signals after the signal shaper block for three consecutive trigger pulses and $C_{LPF} = 500$ fF for a high gain CSA programmed in slow (blue line) and fast (red line) modes.

Table II presents the drift of the DC voltage level (offset) after the CSA and the signal shaper block for different programming modes of the CSA. The offset associated with the DC baseline at the CSA output node is a large value compared to the amplitude of the voltage signal and also the noise power. However, this offset after the signal shaper block, thanks to the BLR chain and the internal negative loop, is diminished by a factor of 17, which helps to discriminate the voltage signals with a higher accuracy.

TABLE II. MEASURED DRIFT OF THE DC VOLTAGE LEVEL AFTER THE CSA AND SIGNAL SHAPER BLOCK

| CSA Program Mode | High Gain | | Low Gain | |
|---|---|---|---|---|
| | Slow | Fast | Slow | Fast |
| $V_{Offset\|CSA}$ [mV] | 2.7 | 5.1 | 2.4 | 5.6 |
| $V_{Offset\|Shaper}$ [mV] | 0.16 | 0.29 | 0.14 | 0.33 |

## V. CONCLUSIONS

This paper presented the design methodology and the experimental characterization of a state-of-the-art, high time resolution, low-offset, and power-efficient band-pass signal shaper block intended for fitting the voltage signals generated by a charge-sensitive amplifier (CSA). Verified through experimental qualification tests, the signal shaper block eliminates the tail of the low-bandwidth CSA voltage signal in the time domain in order to fit within timeframes of 2.5 ns, compensates for the ISI-induced errors, and realizes the particle-counting mode of operation. Moreover, thanks to the negative loop and the BLR chain, the signal shaper block attenuates the offset by a factor of 17 while consuming 0.17 mW of power. The presented solution is intended for accurate detection of a weak input signal comprising a beam of particles reaching the surface of a detector with a high time resolution of only a few nanoseconds.

## ACKNOWLEDGMENT

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