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A New Reliable Switched-Capacitor-Based High Step-Up Five-Level Inverter

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ABSTRACT This article presents a new transformerless switched-capacitor (SC) based five-level grid-connected inverter with inherent voltage-boosting capability. The proposed topology achieves a voltage gain factor of two without requiring an additional dc–dc boost converter or transformer, resulting in a more compact, cost-effective, and efficient design. A single SC cell is utilized to perform bidirectional capacitor charging during both positive and negative grid half cycles, thereby improving energy transfer efficiency and significantly reducing capacitor size and volume compared with the conventional topologies. The inverter employs a minimal number of components—only nine switches and one flying capacitor—while maintaining high performance. Only five switches operate at high frequency, which reduces switching losses, gate driver complexity, and electromagnetic interference. A straightforward control strategy ensures that the inverter delivers a high-quality sinusoidal current waveform to the grid and supports both active and reactive-power flow under various power factor conditions. The reliability of the proposed inverter is analyzed, and its performance is validated through detailed simulations and experimental results. A comparative study with the existing solutions highlights the advantages of the proposed topology in terms of efficiency, voltage gain, component count, and waveform quality.

INDEX TERMS Grid-connected, reliability, single-stage inverter, switched-capacitor (SC) based inverter, transformerless inverter, voltage-boosting feature.

I. INTRODUCTION

The increasing global demand for sustainable energy solutions, particularly in the residential and distributed photovoltaic (PV) markets, has driven extensive research in compact, efficient, and cost-effective power converter technologies. As the interface between the renewable energy source and the utility grid, the inverter plays a central role in shaping power quality, reliability, and system economics. Traditional two-level inverters are well established but suffer from major drawbacks, such as high switching losses and poor harmonic performance, particularly in high-power and low-voltage PV systems. To overcome these limitations, multilevel inverters (MLIs) have gained widespread adoption due to their ability to synthesize near-sinusoidal output waveforms, reduce the voltage stress on power switches, and lower electromagnetic interference (EMI) [1], [2].

Among various MLI architectures, five-level inverters offer a compelling compromise among output quality, efficiency, and system complexity [3], [4]. They achieve significant harmonic reduction with fewer components than higher level topologies and are particularly suited to single-phase residential PV systems, electric vehicle chargers, and other distributed generation applications. Furthermore, the emergence of transformerless inverter topologies has allowed designers to eliminate bulky and lossy grid-frequency transformers, enhancing power density and reducing both cost

and weight. However, transformerless designs introduce challenges related to leakage current, EMI, and the need for voltage boosting to interface with the grid from low PV voltages.

In recent years, significant advancements have been made in high step-up converters and grid-tied inverter topologies, especially for renewable energy applications [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. Various switched-capacitor (SC) and quasi-*Z*-source-based converters have been proposed to achieve high-voltage gain while minimizing input current ripple and capacitor charging spikes, improving the overall system efficiency and reliability [1], [2], [3], [4], [5], [6]. MLIs with high number of levels have been developed to reduce voltage stress, limit leakage current, and provide common-ground features, which are critical for PV grid integration [7], [8], [9], [10], [11], [12], [13], [14], [15]. In addition, transformerless topologies with common grounding and leakage current mitigation have gained attention due to their enhanced safety, compactness, and cost-effectiveness [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. These innovations collectively contribute to more robust and efficient grid-connected power electronic systems for renewable energy sources.

To address these issues, SC-based inverter topologies have gained considerable attention. These converters use capacitors and controlled switch configurations to dynamically transfer charge and generate stepped output voltages. Unlike inductive boost circuits, SC converters achieve voltage gain without magnetic components, leading to smaller, lighter, and lower cost solutions. Moreover, SC topologies are well suited for low-voltage PV sources, as they can directly boost the dc-link voltage to the required grid level while offering transformerless operation.

Numerous SC-based five-level inverter topologies have been proposed in the literature, each with unique tradeoffs.

1) [29], [30], [31], [32]: These early SC inverter designs demonstrated magneticless voltage boosting but relied on unidirectional capacitor charging, limiting energy utilization, introducing capacitor imbalance, and requiring large-sized capacitors.
2) [33]: Introduced a multistring five-level inverter with advanced pulsewidth modulation (PWM) and high-quality output, but the design suffers from control complexity and reliance on multiple current and voltage sensors, which increase cost and reduce reliability.
3) [34]: Presented a hybrid cascaded inverter architecture with reduced dc sources; however, voltage balancing across cascaded cells is nontrivial, and the topology has limited scalability.
4) [35]: Developed a transformerless five-level inverter with self-balancing and voltage gain, but leakage current and EMI remain challenges inherent to transformerless operation.
5) [36]: Designed a high-gain SC inverter for low-voltage PV systems. While the gain is sufficient to eliminate external dc–dc stages, the increased number of components and control loops impacts the overall system cost and reliability.
6) [37]: Proposed transformerless five-level designs that successfully reduce leakage current, but these topologies lack inherent voltage gain, requiring additional front-end stages in many applications.
7) [38]: Offered a simplified SC inverter with leakage suppression. However, EMI issues may arise due to the lack of galvanic isolation and fast-switching near-ground nodes.
8) [39]: A neutral-point-clamped quasi-*Z*-source inverter capable of boosting voltage with low switch stress, but control complexity and impedance network design pose practical implementation challenges.
9) [40]: Introduced soft-start and quasi-resonant SC charging to improve reliability. Nevertheless, higher switching losses and circuit complexity limit its suitability for high-power systems.
10) [41], [42]: Presented sensorless and modular SC topologies. While reducing sensing needs and improving integration, they require careful capacitor balancing and nontrivial control schemes.
11) [43], [44], [45], [46], [47], [48], [49]: Explored various dual-mode, flying inductor, and quasi-switched-boost inverters. These designs offer good performance but reintroduce inductive components or add complex control requirements.
12) [50], [51], [52], [53], [54], [55]: Focused on compact SC inverter designs with simple control and reduced switch count. However, these generally operate with unidirectional charging, low voltage gain, or high capacitor ripple, leading to larger and costlier capacitors.

Singh and Mandal [56] developed a closed–loop controlled, SC–based five–level inverter for grid–connected PV systems. Mondal et al. [50] presented a transformerless variant with enhanced voltage–boosting capability. Kumari et al. [57] explored a simplified topology utilizing a single dc source and fewer switching devices. The work by the authors in [58] and [59] focused on grid–integrated PV inverters with thorough modeling of performance and control dynamics. Lo and Lin [60] introduced a step–up SC topology optimized for grid applications, while Ardashir et al. [61] proposed a transformerless SC inverter designed to mitigate leakage current. The authors in [62] and [63] have recently reported novel boost–type five–level SC inverters with reduced capacitance and enhanced structural efficiency.

This growing body of work demonstrates the increasing interest in SC–based multilevel converters, especially transformerless designs, each offering various tradeoffs in terms of component count, boost capability, leakage suppression, and control complexity.

Despite the innovation across these topologies, key limitations remain prevalent.

1) Lack of sufficient voltage boosting to interface directly with the grid.

2) Inefficient or half-cycle-only capacitor charging strategies.
3) High component count or large capacitor sizes due to ripple current and voltage stress.
4) Control schemes that are not compatible with reactive-power delivery.
5) Limited discussion of system behavior under non-unity-power factor (PF) conditions.

A. MOTIVATION AND CONTRIBUTIONS

This article presents a new five-level SC transformerless inverter that addresses the above challenges. The topology introduces a unique SC cell capable of bidirectional capacitor charging across both positive and negative half cycles, resulting in enhanced energy transfer, lower voltage ripple, and significantly reduced capacitor size. The proposed inverter supports a voltage gain factor of 2, enabling operation from low PV voltages without requiring an auxiliary boost stage or transformer.

The inverter is composed of only nine switches, five of which operate at a high switching frequency, while the remaining four switch at grid frequency. This configuration significantly reduces switching losses, gate driver complexity, and EMI compared with topologies that rely entirely on high-frequency switching. The use of a single flying capacitor and minimal passive elements ensures a compact layout and reduced cost.

Unlike many prior SC topologies, the proposed design supports full four-quadrant operation with reactive-power control. Through a *dq*-frame control system, the inverter is capable of adjusting its PF dynamically, delivering both active and reactive power as required by the grid. This feature is increasingly important in smart grid scenarios, where inverters are expected to support voltage regulation, PF correction, and grid stability.

Extensive simulation and experimental testing have been conducted to validate the performance of the proposed inverter. The results demonstrate low total harmonic distortion (THD) (2.33%), high efficiency (96.5%), stable operation across PF ranges (±0.8), and compliance with grid-connected standards. A comparative study further highlights the superiority of the proposed topology in terms of component count, voltage gain, power density, and ease of control.

B. ARTICLE ORGANIZATION

The rest of this article is organized as follows. Section II introduces the proposed topology, switching modes, and operational analysis. Section III presents the design criteria for the passive components and filter. Section IV describes the control strategy and modulation scheme for grid synchronization and reactive-power control. Section V provides a reliability assessment based on thermal and electrical stress modeling. Section VI presents simulation results under various PF conditions. Section VII includes an efficiency breakdown and loss distribution. Section VIII provides a comparative analysis against state-of-the-art topologies. Section IX presents the experimental results and validation. Finally, Section X concludes this article.

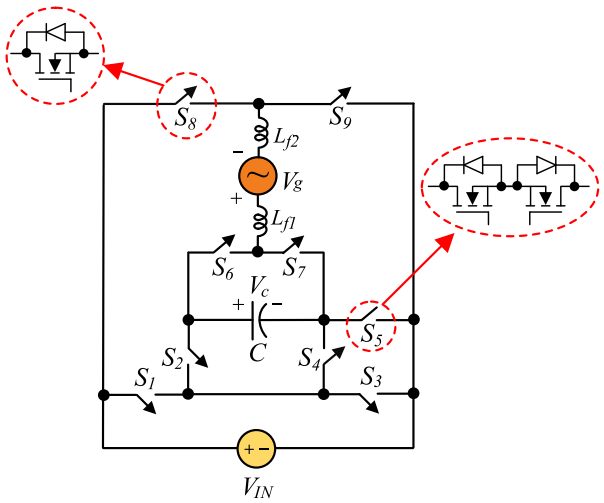

FIGURE 1. Proposed SC-based five-level grid-tied inverter.

II. PROPOSED TOPOLOGY AND DUTY CYCLE CALCULATION

Fig. 1 illustrates the proposed inverter architecture, comprising nine power switches (S_1–S_9) and one capacitor (C). All switches, with the exception of the four-quadrant switch S_5, are MOSFETs equipped with parallel diodes. In the proposed inverter, switch S_5 is implemented using a common-source back-to-back MOSFET configuration, enabling it to block voltage in both directions. This design allows S_5 to conduct current bidirectionally when required. Such a capability is essential for reactive-power control (both lagging and leading PFs), as well as bidirectional power flow during grid-connected operation and active rectifier mode.

The inclusion of inductors L_{f1} and L_{F2} serves the purpose of grid current filtration. This proposed five-level inverter operation encompasses six distinct modes in total, as delineated in Fig. 2(a)–(f). The red dashed lines indicate the path of the injected grid current, while the blue dashed lines represent the capacitor charging loop. The analysis in this section is performed under the assumption of unity PF (PF = 1) to simplify the derivation. Non-unity-PF conditions, including leading and lagging cases, are addressed in Sections VI and IX to confirm the inverter's full-range operating capability.

A. POSITIVE HALF CYCLE

During the positive half cycle of operation, the proposed inverter generates three distinct levels of output voltage waveform through its respective modes, each contributing to the overall voltage profile. These levels, namely the zero level, first level, and top level, are elaborated as follows.

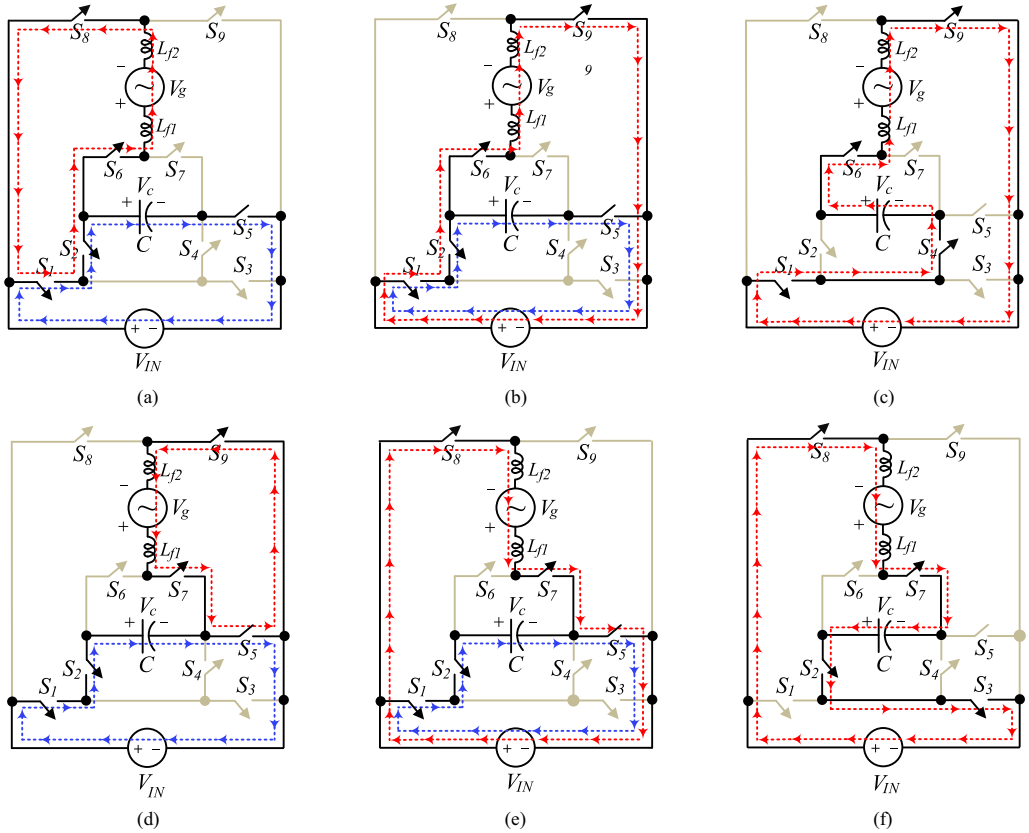

FIGURE 2. Operational mode of the suggested five-level grid-connected inverter. (a) First mode. (b) Second mode. (c) Third mode. (d) Fourth mode. (e) Fifth mode. (f) Sixth mode.

1) FIRST OPERATION MODE

In the first mode, as depicted in Fig. 2(a), the primary objective is to generate the zero-level voltage during the positive half cycle of operation. To achieve this, a specific configuration of switches is employed to facilitate the required voltage level within the inverter circuit. During this mode, switches S_1, S_2, S_6, and S_8 are activated, establishing the necessary circuitry for voltage generation. Among these switches, S_1, S_2, and S_5 play a pivotal role in charging C. By turning ON these switches, the capacitor is effectively connected in parallel to the input source, enabling it to be charged to a voltage level of $+V_{\text{IN}}$.

This charging process ensures that the capacitor attains the desired voltage potential. Through this strategic utilization of switches and capacitor charging mechanisms, the inverter effectively establishes the zero-level output voltage, laying the foundation for subsequent voltage transitions and waveform generation within the operational cycle.

2) SECOND OPERATION MODE

Fig. 2(b) illustrates the circuit for the second operational mode. In this mode, switches S_1, S_2, S_6, and S_9 are turned ON to generate the first level of the output voltage waveform. In this configuration, the input voltage source is indirectly connected to the output through the power stage, allowing energy transfer toward the grid via the output inductor. In addition, switches S_1, S_2, and S_5 are turned ON to connect the flying capacitor across the input voltage source, resulting in its charging to $+V_{\text{IN}}$. As shown in Fig. 2(b), switches S_3, S_4, S_7, and S_8 remain in the OFF-state during this interval.

3) THIRD OPERATION MODE

Fig. 2(c) shows the third operational mode of the inverter during the positive half cycle. With switches S_1, S_4, S_6, and S_9 turned ON, the output voltage's amplitude is the sum of C voltage (V_C) and the input voltage. In this mode, the capacitor discharges, resulting in an output voltage equal to $+2V_{\text{IN}}$, verifying the proposed topology's voltage-boosting capability. Regarding Fig. 2(c), in this mode, the switches S_2, S_3, S_5, S_7, and S_8 are in OFF-state.

B. NEGATIVE HALF CYCLE

1) FOURTH OPERATION MODE

Fig. 2(d) depicts the electrical circuit of the proposed inverter during the fourth operational mode. Turning ON switches S_5, S_7, and S_9 in this mode aims to generate a zero-voltage level during the negative half cycle. In addition, as indicated in Fig. 2(d), C is charged to input dc source voltage (V_{IN}) when switches S_1, S_2, and S_5 are activated. Considering Fig. 2(d), in this mode, the switches S_3, S_4, S_6, and S_8 are in the OFF-state.

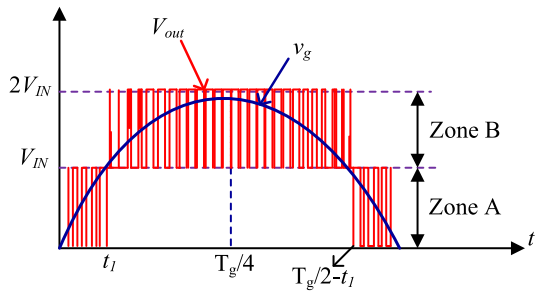

FIGURE 3. Waveforms of inverter's five-level output voltage and grid voltage in the positive half cycle.

2) FIFTH OPERATION MODE

Fig. 2(e) demonstrates the electrical circuit and current flow in the fifth operational mode. To generate the first level of the output voltage waveform during the negative half cycle, switches S_5, S_7, and S_8 are turned ON. As depicted in Fig. 2(e), with switches S_1, S_2, and S_5 in the ON-state, C, positioned parallel to the input dc power supply, charges to $+V_{\text{IN}}$. Regarding Fig. 2(e), the switches S_3, S_4, S_6, and S_9 are in the OFF-state during the fifth operation mode.

3) SIXTH OPERATION MODE

Fig. 2(f) illustrates the electrical circuit of the proposed inverter during the sixth operation mode. This mode is tasked with generating the top level of the output voltage waveform during the negative half cycle. By turning ON the switches S_2, S_3, S_7, and S_8, C is discharging, resulting in the output voltage being the sum of the amplitudes of the capacitor voltage and the input voltage. Consequently, the output voltage is twice the input voltage and equals $-2V_{\text{IN}}$.

Regarding Fig. 2, the blocked voltage of each switch in the OFF-state can be obtained as follows:

$$\begin{cases} V_{S1} = V_{S3} = V_{S5} = V_{S8} = V_{S9} = V_{\text{IN}} \\ V_{S2,} = V_{S4} = V_{S6} = V_{S7} = V_C = V_{\text{IN}}. \end{cases} \tag{1}$$

Regarding (1), the maximum blocked voltage of the proposed inverter is equal to V_{IN}. In this article, the total standing voltage (TSV) is defined as the sum of the maximum voltage-blocking requirements of all switches in the inverter. TSV serves as a key comparative metric for evaluating the overall voltage stress level of the topology and is useful for analyzing device utilization, cost, and insulation requirements. So, the TSV of the proposed inverter can be calculated as follows:

$$\text{TSV} = \sum_{i=1}^{9} V_{Si} = V_{S1} + \cdots + V_{S9} = 9V_{\text{IN}}. \tag{2}$$

Hence, the per-unit value of TSV ($\text{TSV}_{\text{P.U}}$) in relation to the input voltage can be derived as follows:

$$\text{TSV}_{\text{P.U}} = \frac{\sum_{i=1}^{9} V_{Si}}{V_{\text{IN}}} = \frac{9V_{\text{IN}}}{V_{\text{IN}}} = 9. \tag{3}$$

Fig. 3 shows the positive half cycle of the output voltage waveform of the inverter along with the grid voltage, featuring two operational zones (Zone A and Zone B) of the inverter. Regarding this figure, the control strategy for the proposed inverter can be obtained.

The inverter operates at a switching frequency of f_S. By applying the inductor volt-second balanced (IVSB) law to the inductor's voltage over a full operation period of the inverter (T_S), the switching duty cycles for the two mentioned zones (A and B) are determined in Section II-C and D. It is important to mention that V_{out} and v_g represent the inverter's five-level output voltage and grid voltage, respectively. The equations describing the voltage and current of the grid are formulated in (4) and (5). In this analysis, a unity PF (PF = 1) is assumed for simplification purposes. This assumption is commonly used in analytical models of grid-tied inverters to focus on the core active power transfer mechanism. Nonetheless, the inverter's capability to operate under non-unity-PF conditions (leading and lagging) is demonstrated through simulation and experimental validations in Sections VI and IX

$$v_g(t) = V_{g,m} \cdot \sin(\omega t) \tag{4}$$

$$i_g(t) = I_{g,m} \cdot \sin(\omega t) \tag{5}$$

where $V_{g,m,}$ and $I_{g,m}$ denote the maximum values of the grid voltage and the injected current into the grid, respectively.

C. FIRST OPERATION ZONE (A)

Considering Fig. 3, in this zone, the output voltage of the inverter ranges between 0 and V_{IN}. Utilizing the IVSB principle for the voltage across L_f (V_{Lf}) during zone A throughout the switching period, the switching duty cycle of the inverter in zone A (d_A) can be obtained as follows. It should be noted that the IVSB is considered within each switching cycle to ensure volt-second balance and proper operation of the converter under steady-state conditions. However, this condition does not extend over the entire grid cycle, especially in the presence of power transfer. Even under unity-PF conditions, a small phase shift between the synthesized converter voltage and the grid voltage is required to enable active power flow. The modulation strategy inherently provides this phase adjustment to maintain stable grid power injection

$$\int_0^{d_A T_s} (V_{\text{IN}} - v_g)dt + \int_{d_A T_s}^{T_s} (-v_g)dt = 0, \quad 0 \le t < t_1 \tag{6}$$

$$d_A(t) = \frac{v_g}{V_{\text{IN}}}, \quad 0 \le t < t_1. \tag{7}$$

By using (4) and (7), the duty cycle of the proposed inverter in zone A can be obtained as follows:

$$d_A(t) = \frac{V_{g,m} \cdot \sin(\omega t)}{V_{\text{IN}}}. \tag{8}$$

D. SECOND OPERATION ZONE (B)

Regarding Fig. 3, during zone B, the output voltage of the inverter falls within the range of V_{IN}–$2V_{\text{IN}}$. Employing the IVSB principle for the voltage across L_f (V_{Lf}) throughout zone

B across the switching period enables the calculation of the switching duty cycle of the inverter in zone B (d_B) as follows:

$$\int_0^{d_B T_s} (2V_{\text{IN}} - v_g)dt + \int_{d_B T_s}^{T_s} (V_{\text{IN}} - v_g) = 0, \quad t_1 \le t < \frac{T_g}{2} - t_1 \tag{9}$$

$$d_B(t) = \frac{v_g}{V_{\text{IN}}} - 1 = \frac{V_{g,m}.\sin(\omega t)}{V_{\text{IN}}} - 1, \quad t_1 \le t < \frac{T_g}{2} - t_1. \tag{10}$$

Considering (8), (10) can be rewritten as follows:

$$d_B(t) = d_A(t) - 1, \quad t_1 \le t < \frac{T_g}{2} - t_1. \tag{11}$$

Considering Fig. 3, the equation for time t_1 can be expressed as follows:

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{\text{IN}}}{V_{g,m}}\right). \tag{12}$$

III. DESIGN OF OUTPUT INDUCTOR-BASED FILTER AND CALCULATING CAPACITANCE OF UTILIZED CAPACITORS

In this section, the inductance values of L_{f1} and L_{f2} and the capacitance value of C are calculated in the following. It is important to note that the ripple calculations are performed under worst-case operating conditions. Specifically, unity PF (PF = 1) is considered, as it results in the highest overlap between the peak output current and voltage, thereby producing the maximum ripple across both the inductor and the capacitor. Furthermore, the analysis is conducted at the grid voltage peak ($\omega t = \pi/2$), where voltage stress across components is highest. Finally, the output power is set to the rated full load to ensure that ripple amplitudes are estimated under maximum current conditions. These assumptions lead to conservative component sizing and robust design.

A. INDUCTANCE VALUE OF OUTPUT FILTER (L_F)

The design of the output inductor-based filter (L_f) is considered in this section. It should be mentioned that the output filter consists of two inductors with the same values; so, the equation of L_f can be expressed as follows:

$$\begin{cases} L_f = L_{f1} + L_{f2} \\ L_{f1} = L_{f2} = L_f/2. \end{cases} \tag{13}$$

To design the output inductor filter (L_f), the current of the output filter inductor can be expressed as follows:

$$i_{Lf}(t) = \frac{1}{L_f}\int_0^t V_{Lf}dt + i_{Lf}(0), \quad t_1 \le t < \frac{T_g}{2} - t_1. \tag{14}$$

The current ripple of the inductor L_f can be obtained as follows:

$$\Delta I_{Lf} = i_{Lf}(t = d_B T_S) - i_{Lf}(0) = \frac{(2V_{\text{IN}} - v_g)\, d_B}{L_f f_S}, t_1 \le t < \frac{T_g}{2} - t_1. \tag{15}$$

As a result, by replacing (10) in (15), (15) can be rewritten as follows:

$$\Delta I_{Lf} = \frac{T_S}{L_f}\left[3V_{g,\,m}\sin(\omega t) - \frac{(V_{g,m}\cdot\sin(\omega t))^2}{V_{\text{IN}}} - 2V_{\text{IN}}\right]. \tag{16}$$

Finally, the desired inductance value of L_f can be obtained as follows:

$$L_f = \frac{1}{\Delta I_{Lf}\cdot f_S}\left[3V_{g,\,m}\sin(\omega t) - \frac{(V_{g,m}\cdot\sin(\omega t))^2}{V_{\text{IN}}} - 2V_{\text{IN}}\right]. \tag{17}$$

The maximum current ripple happens when the grid voltage reaches its maximum value. Thus, the calculation for the value of L_f to achieve the maximum inductor current ripple can be determined as follows:

$$L_f = \frac{1}{\Delta I_{If,\text{peak}}\cdot f_S}\left[3V_{g,\,m} - \frac{V_{g,\,m}^2}{V_{\text{IN}}} - 2V_{\text{IN}}\right]. \tag{18}$$

Regarding (13), the inductance values of L_{f1} and L_{f2} can be obtained as follows:

$$L_{f1} = L_{f2} = \frac{1}{2\left(\Delta I_{Lf,\text{peak}}\cdot f_S\right)}\left[3V_{g,\,m} - \frac{V_{g,\,m}^2}{V_{\text{IN}}} - 2V_{\text{IN}}\right]. \tag{19}$$

B. CALCULATION OF THE CAPACITANCE VALUE OF CAPACITOR C

In this section, the capacitance value of C is computed. Referring to Fig. 2(c), in the second-level operation mode during the positive half cycle, the current flowing through C matches the injected current into the grid. Consequently, the voltage across C can be determined using the following equation:

$$V_C(t) = V_C(0) + \frac{1}{C}\int_0^t i_C(t)dt. \tag{20}$$

Considering (10), the voltage ripple of the capacitor C (ΔV_C) can be expressed as follows:

$$\Delta V_C = \frac{1}{C}(i_C \cdot d_B \cdot T_S) = \frac{i_g}{C}\left(\frac{v_g}{V_{\text{IN}}} - 1\right)\cdot T_S. \tag{21}$$

At the peak values of grid voltage and injected current into the grid, the voltage ripple across capacitor C reaches its maximum. Therefore, the capacitance of capacitor C can be computed using the following equation:

$$C = \frac{I_{g,\,m}}{\Delta V_{C,\text{peak}}\times f_s}\left(\frac{V_{g,\,m} - V_{\text{IN}}}{V_{\text{IN}}}\right). \tag{22}$$

It should be noted that the capacitor ripple voltage is maximum at unity PF (PF = 1). Under non-unity-PF conditions (leading or lagging), the phase displacement between current and voltage results in reduced ripple. Therefore, PF = 1 is considered the worst-case scenario for capacitor sizing, ensuring a conservative design approach.

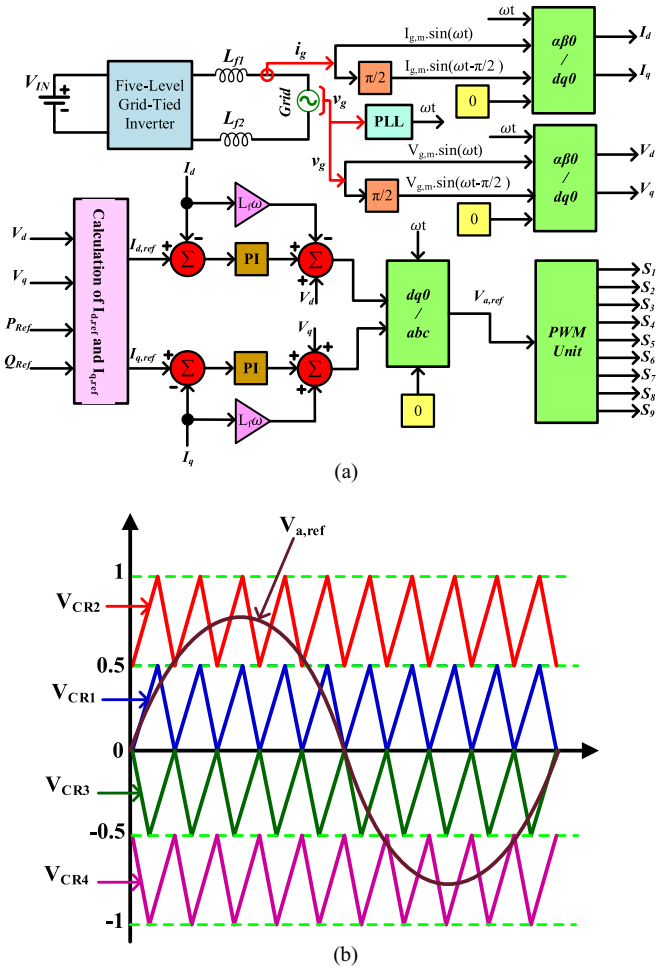

FIGURE 4. **(a) Closed-loop control system. (b) Typical PWM process with carrier waveforms.**

IV. CLOSED-LOOP CONTROL SYSTEM OF THE PROPOSED INVERTER

This section of the article presents the closed-loop control strategy for the proposed inverter, as depicted in Fig. 4(a). This control system enables the regulation of both active and reactive-power flows, as well as the generation of switching gate pulses for the switches. The conversion unit, as depicted in Fig. 4(a), facilitates the derivation of the d-axis injected grid current (I_d) and the q-axis injected grid current (I_q). In addition, it calculates the d-axis grid voltage (V_d) and the q-axis grid voltage (V_q). In this context, I_d and I_q represent the active and reactive-power flows, respectively. To effectively control both active and reactive-power flows, reference values for the d-axis ($I_{d,\text{ref}}$) and q-axis ($I_{q,\text{ref}}$) of current must be computed, as follows:

$$I_{d,\text{ref}} = \frac{2}{3} \cdot \left[\frac{P_{\text{Ref}} \cdot V_d + Q_{\text{Ref}} \cdot V_q}{V_d^2 + V_q^2} \right] \tag{23}$$

$$I_{q,\text{ref}} = \frac{2}{3} \cdot \left[\frac{P_{\text{Ref}} \cdot V_q - Q_{\text{Ref}} \cdot V_d}{V_d^2 + V_q^2} \right]. \tag{24}$$

The ac components are subsequently transformed onto the d–q axis, as illustrated in Fig. 4(a). To synchronize the output of the inverter with the power grid, phase-locked loop (PLL) has been used. Also, ωt is calculated in the control system by PLL.

By utilizing a proportional–integral current controller, the desired current is injected into the grid, ensuring that it aligns with the reference values of $I_{d,\text{ref}}$ and $I_{q,\text{ref}}$. Finally, the generated $V_{a,\text{ref}}$ is transferred to the PWM unit to generate gate pulses for the power switches (S_1–S_9). Fig. 4(b) provides an illustration of a typical PWM process, with V_{CR1}, V_{CR2}, V_{CR3}, and V_{CR4} representing the shifted-level carrier waveforms utilized in PWM modulation. This comprehensive approach guarantees the accurate control of active and reactive-power flows while promoting the efficient operation of the inverter system. In the following, a detailed explanation of the modulation technique and the allocation of PWM signals to the nine switches in the converter has been provided. In the phase disposition PWM (PD-PWM) approach, four level-shifted carrier signals are used to modulate the reference sinusoidal waveform. These carriers are uniformly distributed within the range of $\pm V_{\text{IN}}$, dividing the modulation into four distinct bands that determine the output voltage levels. The modulation signals are generated by comparing a sinusoidal reference voltage with these carriers, resulting in appropriate gating pulses.

To implement the control strategy effectively, a modulation technique must be adopted to translate the reference signals into appropriate switching patterns. In this work, a level-shifted pulsewidth modulation (LS-PWM) approach—specifically, the PD-PWM method—is utilized, as detailed in the following text.

A. MODULATION SCHEME

The proposed five-level grid-tied inverter utilizes an LS-PWM technique, specifically, the PD-PWM method. This method is well suited for MLIs as it minimizes THD while ensuring a balanced switching operation. In the PD-PWM approach, four level-shifted carrier signals are used to modulate the reference sinusoidal waveform. These carriers are uniformly distributed within the range of $\pm V_{\text{IN}}$, dividing the modulation into four distinct bands that determine the output voltage levels. The modulation signals are generated by comparing a sinusoidal reference voltage with these carriers, resulting in appropriate gating pulses.

B. CARRIER SIGNAL ARRANGEMENT

As depicted in Fig. 4, the modulation scheme employs four level-shifted triangular carriers, denoted as C_{R1}, C_{R2}, C_{R3}, and C_{R4}. These carriers define the switching states that determine the voltage level at the output. The reference sinusoidal waveform is compared with the carriers, and based on the crossing points, the switching states are generated.

1) *Carrier C_{R1}:* Defines the first switching transition for moving from level 1 to level 2.
2) *Carrier C_{R2}:* Defines the transition from level 2 to level 1.

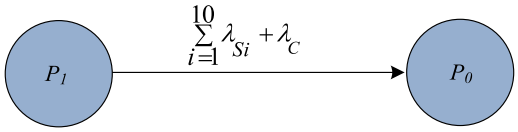

FIGURE 5. Markov chain for the proposed inverter.

3) *Carrier C_{R3}:* Defines the transition from level 3 to level 4.
4) *Carrier C_{R4}:* Defines the final transition from level 4 to level 5.

C. PWM SIGNAL ALLOCATION TO NINE SWITCHES

The proposed topology consists of nine power switches, denoted as S_1–S_9. The PWM signals derived from the modulation scheme are assigned to these switches in a way that ensures proper voltage-level transitions, achieving a five-level output voltage waveform with minimal distortion. The switching sequence is designed to do the following:

1) maintain a balanced switching operation;
2) ensure minimal switching losses;
3) the allocation of the four PWM signals to the nine switches follows a predefined switching logic table, ensuring that, at any instant, the required voltage level is generated at the output. The switching states of the nine switches are determined by logical combinations of the modulation signals, which are derived from the comparison of the reference signal with the four carriers.

V. RELIABILITY ANALYSIS

In this section, we examine the reliability of the proposed structure using the Markov approach, a well-established method for assessing system reliability, particularly suited for systems exhibiting memoryless behavior. A Markov chain, representing a limited class of random processes $\{Xn\}$ with a finite state space S, is employed. This approach is applicable when considering any positive integers k, n ($k \leq n$), and any selection of states $i_0, \ldots, i_{n+1}$ in S, where the following equation holds:

$$P\left(X_{n+1}=i_{n+1} \mid X_n=i_n, \ldots, X_{k+1}=i_{k+1}, X_k=i_k\right)=P\left(X_n, i_n\right). \tag{25}$$

In the proposed inverter, consisting of ten switches and one capacitor, the failure of any mentioned elements could compromise the entire system's functionality. Consequently, the Markov chain model for the inverter is illustrated in Fig. 5. Here, P_1 signifies the state where the inverter functions correctly with all components operational, while any fault in one or more components transitions the inverter to state P_0. λ_x denotes the failure rate of element x

$$\begin{bmatrix} \frac{dP_1}{dt} \\ \frac{dP_0}{dt} \end{bmatrix} = \begin{bmatrix} -\left(\sum_{i=1}^{10} \lambda_{Si} + \lambda_C\right) & 0 \\ \left(\sum_{i=1}^{10} \lambda_{Si} + \lambda_C\right) & 0 \end{bmatrix} \begin{bmatrix} P_1 \\ P_0 \end{bmatrix} \tag{26}$$

TABLE 1. Calculated Failure Rates of the Proposed Inverter Components

Component	*Failure Rates* ($*10^{-8}$)
S_1	4.37
S_2	4.37
S_3	0.74
S_4	0.74
S_5	3.69
S_{5p}	3.69
S_6	1.07
S_7	1.07
S_8	1.07
S_9	1.07
C	0.004

where P_1, P_0, and λ_x represent the occupational probability of state 1, occupational probability of state 0, and the failure rate of element x, respectively. Initially assuming the proposed inverter operates without issues, the starting state is defined as P_1

$$P(t=0)=\begin{bmatrix}1 & 0\end{bmatrix}. \tag{27}$$

Therefore, considering this initial state, the reliability function for the proposed converter can be articulated as follows:

$$R(t)=\exp\left(-\left(\sum_{i=1}^{10} \lambda_{Si} + \lambda_C\right) t\right). \tag{28}$$

In this study, the MIL-HDBK-217F standard is employed to estimate the reliability of key components under assumed steady-state operating conditions. While it is recognized that this method does not account for dynamic stress factors, such as thermal cycling or mission-specific loading, it remains widely used in the literature for first-level assessments and comparative evaluations. The aim here is to provide a relative indication of reliability advantages resulting from the proposed topology, such as reduced high-frequency switching stress and balanced capacitor charging.

Regarding the thermal behavior of the flying capacitor, it should be noted that the capacitor is not subjected to high ripple current or high-frequency switching transients. Infrared thermal imaging in the experimental setup (see Section IX) confirms that the capacitor operates at a temperature close to ambient, with less than 4 °C deviation under full-load conditions. Therefore, the assumption of stable capacitor temperature is justified in the context of this analysis.

The failure rates of the components in Table 1 were determined using the *MIL-HDBK-217F standard and* [26], which is widely adopted for reliability prediction in power electronics. The total failure rate of each component (λ_x) was calculated using the standard formulation

$$\lambda_x = \lambda_b \prod_{i=1}^{n} \alpha_i \tag{29}$$

where n represents the number of α factors affecting the component x's failure rate. In addition, λ_b denotes the basic failure rate of the components, expressed through a model accounting for electrical and thermal stresses' influence (for the switches, the basic failure rate is considered 5e-9 and 3e-11 for the capacitor). The temperature factor (α_T), environmental factor (α_E), quality factor (α_Q), and application factor (α_A) are factors influencing component failure rates. Assuming a ground environment (GB) and ideal material quality and application, the environmental, quality, and application factors are considered 1 (α_E=1 and α_Q= α_A=1). The failure rates for the components are mentioned according to Kurdkandi et al. [26] in Table 1.

In addition, *electrothermal stresses,* such as power dissipation, switching frequency, and voltage-blocking levels, were considered in determining the relative failure rates of switches. For example, switch S_5 handles bidirectional voltage stress and is used more frequently in multiple operating modes, resulting in a slightly higher calculated failure rate.

In Table 1, S_5 and S_{5p} denote the two common-source MOSFETs of the bidirectional switching device. Mean time to failure (MTTF) as a valid reliability metric can predict the expected lifespan of the proposed five-level inverter. The average time for the proposed inverter to fail under normal operating conditions is calculated as follows:

$$\text{MTTF} = \lambda^{-1} = \left(\sum_{i=1}^{10} \lambda_{Si} + \lambda_C \right)^{-1} = 4.57 \times 10^6 \quad \text{(Hours)}. \tag{30}$$

Analysis based on datasheets and failure rate calculations indicates that the switches used in this configuration have low failure rates. Moreover, since the temperature of the capacitor remains nearly constant and aligns with the ambient temperature during inverter operation, its temperature factor is considered to be 1. As a result, the failure rates for these components correspond to their basic failure rates.

The calculated failure rates for the capacitor are also presented in Table 1. Using (28) and (29), using the computed failure rates of all components, the reliability figure for the proposed inverter is shown in Fig. 6, showing the probability of proper functioning. For example, at a certain point in time when the reliability figure is rated at 0.95, the likelihood that the proposed inverter operates in a normal state is 95%. In addition, over time, the reliability function decreases due to the previously mentioned electrothermal failures. However, the proposed inverter maintains a healthy operational state for a significant duration, which is superior compared with similar MLIs.

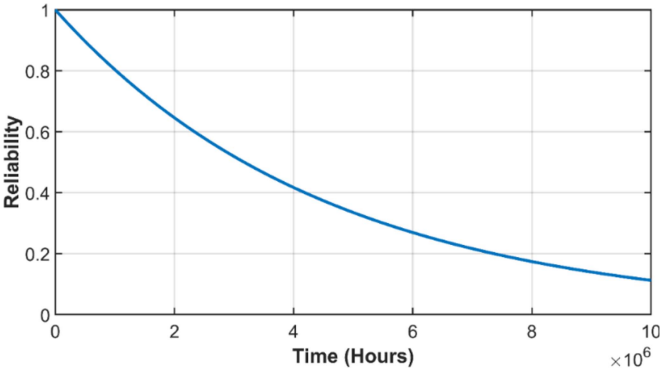

FIGURE 6. Reliability figure of the proposed inverter versus time.

TABLE 2. Simulation Parameters of the Proposed Converter

Parameter	*Value*
V_{IN}	200 V
$V_{g,max}$	311 V
Output voltage	400
P_{out}	1 kW
Switching frequency f_s	20 kHz
Capacitor C/r_{ESR}	20 μF/0.01
$r_{DS,\ MOSFET}$	0.1 Ω
L_{f1}+L_{f2}	3 mH, 0.4 Ω
t_r, t_f	125 ns, 88 ns
$C_{DS,\ MOSFET}$	0.36 nF

Considering that there is limited information regarding the MTTF of similar structures in the literature, based on the derived MTTF and the reliability versus time figure, indicating the probability that the inverter operates without failure at a certain amount of time in Fig. 6, it can be deduced that the proposed inverter shows a long-lasting performance and low failure rate for each of the power components in addition to high MTTF, ensuring its reliable operation.

VI. SIMULATION RESULTS

The proposed inverter is simulated in Simulink/MATLAB under the following conditions and the results are given in the following text. Regarding Fig. 2, switches S_6 and S_7 operate at the low grid frequency (∼100 Hz) rather than the high switching frequency (20 kHz), resulting in negligible switching losses. In contrast, switches S_1–S_5 operate at a high switching frequency and account for the majority of the converter's switching losses.

To address this point clearly, detailed simulations using the parameters, as listed in Table 2, have been conducted. In Fig. 7, the grid voltage is shown along with the injected

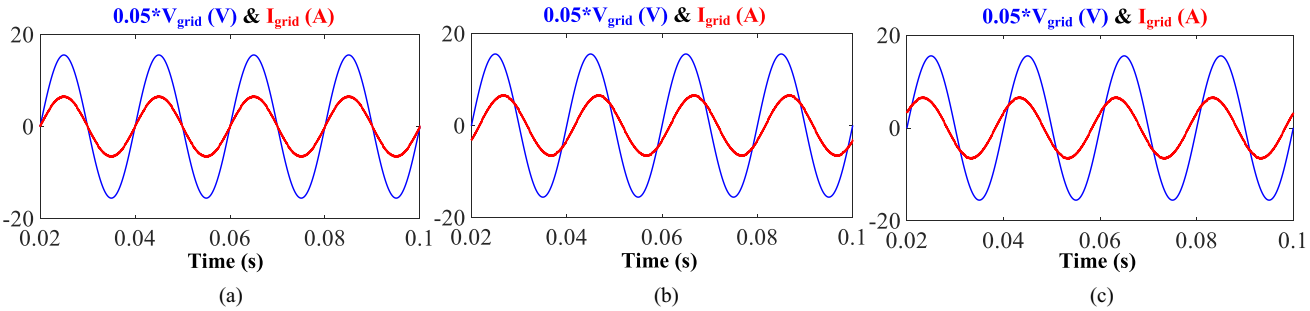

FIGURE 7. Simulation results of the proposed inverter, the grid voltage, and injected current to the grid with the input voltage of 200 V and output power of 1 kW. (a) In the unity PF. (b) In the lagging PF. (c) In the leading PF.

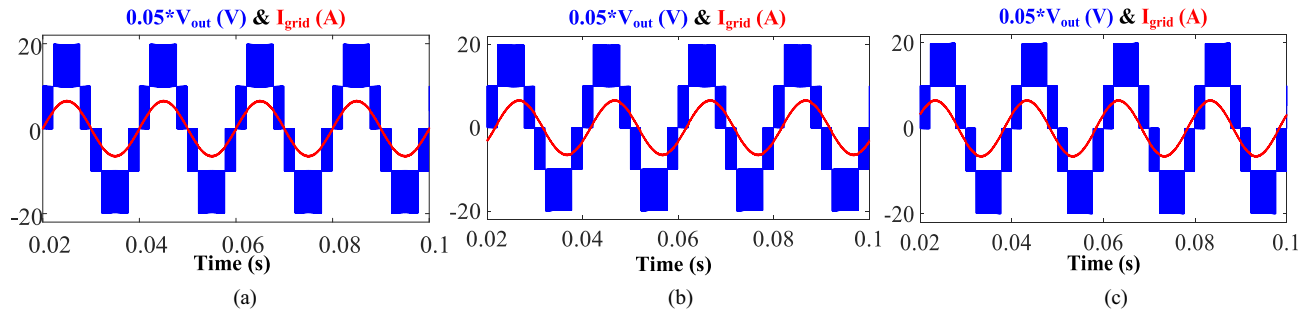

FIGURE 8. Simulation results of the proposed inverter, the output voltage of inverter, and injected current to the grid with the input voltage of 200 V and output power of 1 kW. (a) In the unity PF. (b) In the lagging PF. (c) In the leading PF.

current to the grid. In this figure, the simulation has been done in three modes: unity PF, lagging PF, and leading PF, which are shown in Fig. 7(a), (b), and (c), respectively.

According to this figure, it can be seen that the proposed inverter has the ability to control reactive-power and in non-unity-PF loads, and the quality of the current injected into the grid is suitable.

In Fig. 8, the five-level voltage of the inverter is shown along with the current injected into the grid. In Fig. 7, the simulation is shown in three modes: unity PF, lagging PF, and leading PF. Also, the output power is 1 kW.

In Fig. 9, the voltage stress of switches S_1–S_9 is shown. According to this figure, it can be seen that the voltage stress of all switches is unidirectional except for switch S_5, which is bidirectional.

The reason for using the bidirectional switch for S_5 in the proposed inverter is that its voltage stress is bidirectional.

It can be seen that the voltage stress of all switches is equal to the input voltage, which is one of the important advantages of the proposed inverter.

In Fig. 10, the voltage of capacitor C is shown for output power of 1 kW and input voltage of 200 V. Since the charging and discharging current of this capacitor is done at the switching frequency, it has made it possible to use a low value capacitor in this inverter so that, in the output power of 1 kW, only 20 μF capacitor is used and its voltage ripple has an acceptable value.

In Fig. 11, the THD of the current injected into the grid at the output power of 1 kW is shown. According to this figure, it can be seen that the THD of the grid current is 2.33%, which is a suitable value for inverters connected to the grid.

It should be noted that the values of L_{f1} and L_{f2} in Table 2 are both 1.5 mH. In other words, the total inductance of the output filter is 3 mH. Furthermore, in Section IX, the inductance of the output filter is 5 mH and the capacitance is 47 μF.

To verify the values of 3 mH and 20 μF, simulation results are used in accordance with (18) and (22). It should also be emphasized that these equations are applicable for the operation of the proposed inverter in open-loop mode with a local load, i.e., without any closed-loop control. This is because, in closed-loop mode, the control system actively reduces the grid current ripple and the output inductor current ripple, making it impossible to directly verify (18) and (22).

In the simulation of the local load scenario, the proposed inverter is connected to a resistive load of 48.4 Ω, and the output power is approximately 1 kW. The input voltage is 200 V, and the rms value of the output voltage is 220 V.

According to (18), if L_f=3 mH, switching frequency f_s=20 kHz, input voltage V_{IN}=200 V, and peak output voltage $V_{g,m}$=311 V are substituted, and the calculated maximum output current ripple $\Delta I_{Lf,\text{peak}}$ will be 0.8 A. This value is verified in the figure in the following text. In Fig. 12, it can be observed that the maximum inductor current ripple occurs

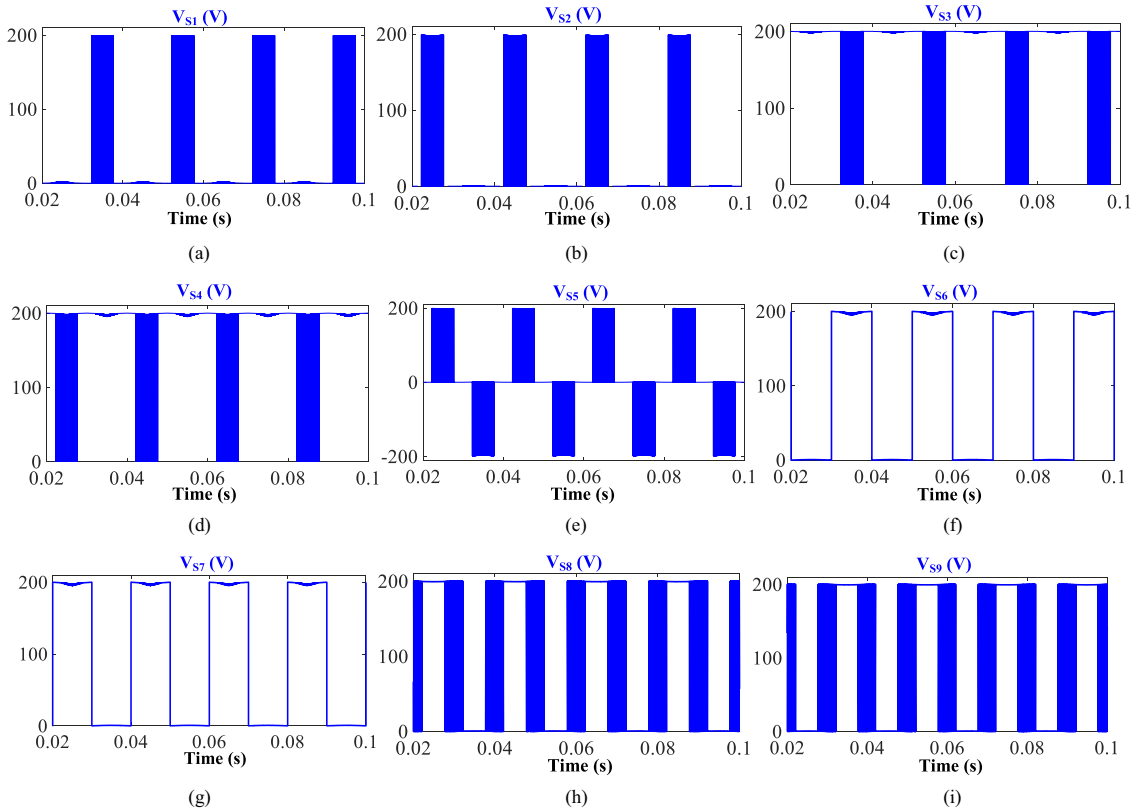

FIGURE 9. Voltage stress of switches in the input voltage of 200 V. (a) V_{S1}. (b) V_{S2}. (c) V_{S3}. (d) V_{S4}. (e) V_{S5}. (f) V_{S6}. (g) V_{S7}. (h) V_{S8}. (i) V_{S9}.

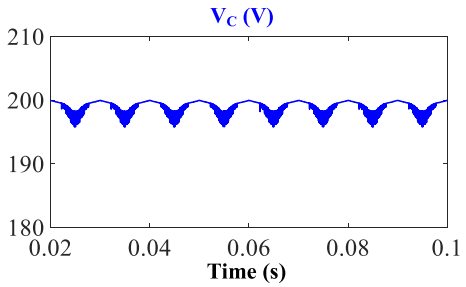

FIGURE 10. Voltage of capacitor C_3 in the output power of 1 kW.

around 90° and equals approximately 0.8 A

$$\Delta I_{Lf,\text{peak}} = \frac{1}{L_f \cdot f_s}\left(3V_{g,m} - \frac{{V_{g,m}}^2}{V_{\text{IN}}} - 2V_{\text{IN}}\right)$$
$$= \frac{1}{(1.5+1.5)\times 10^{-3}\times 20\times 10^{3}} \cdot \left(3\times\left(220\sqrt{2}\right) - \frac{\left(220\sqrt{2}\right)^2}{200} - 2\times 200\right) = 0.8\,\text{A}. \quad (31)$$

To prove the value of the capacitor C, (22) is used. At an output power of 1 kW, the peak output current is approximately 6.5 A. By substituting $I_{g,m}$=6.5 A, switching frequency f_s = 20 kHz, and capacitance C = 20 Mf into

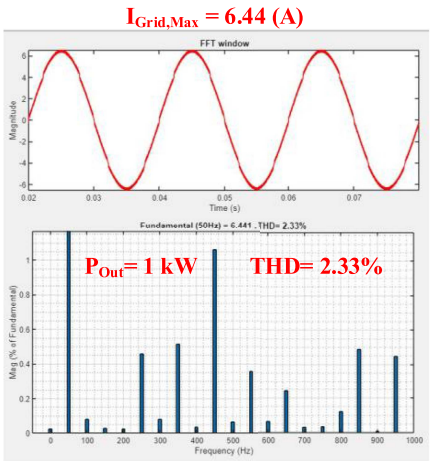

FIGURE 11. THD of the injected current to the grid in the proposed inverter.

(22), and assuming an input voltage of 200 V and an output voltage of 220 V rms, the maximum voltage ripple across the capacitor is calculated to be approximately 9 V. The capacitor voltage ripple is shown in Fig. 13, and this figure verifies the validity of (22).

In the proposed inverter, switch S_5 is implemented using two back-to-back switches in a common-source configuration to enable it to block voltage in both directions. As shown in

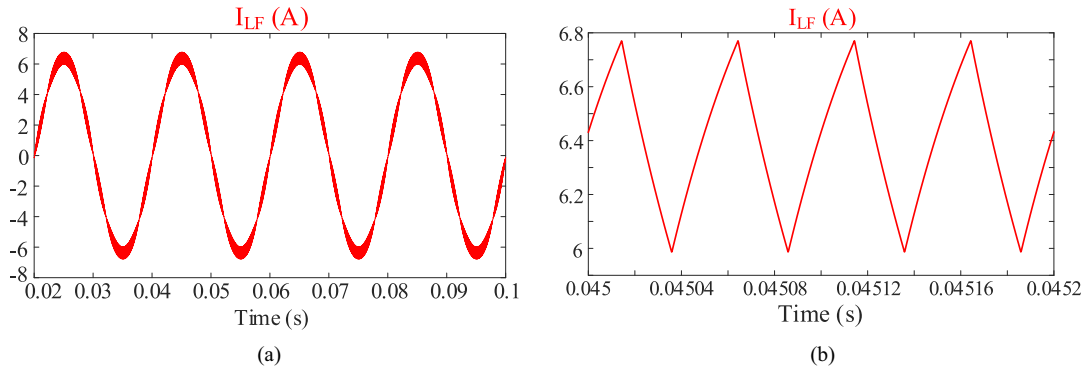

FIGURE 12. (a) Output inductor current in local load mode, at output power of 1 kW, output voltage of 220 V_{RMS}, and input voltage of 200 V. (b) Maximum ripple current of output inductor at ωt=90° and with value of 0.8 A.

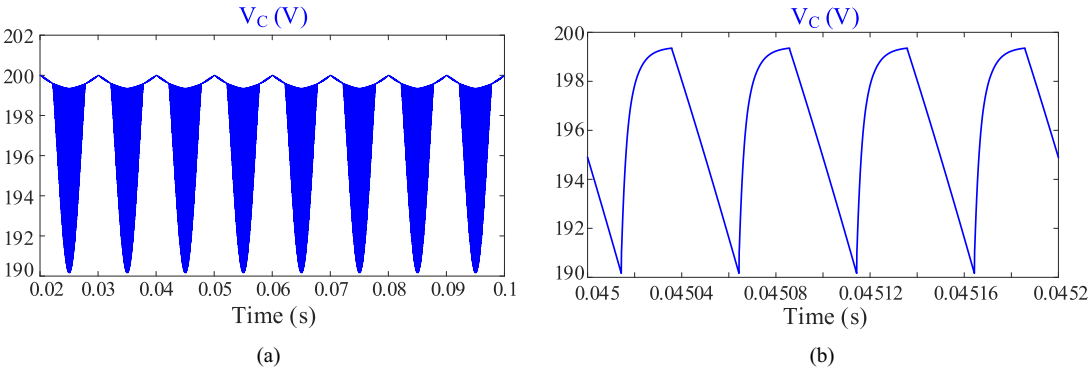

FIGURE 13. (a) Capacitor voltage in local load mode, at output power of 1 kW, output voltage of 220 V_{RMS}, and input voltage of 200 V. (b) Maximum ripple voltage of capacitor C at ωt=90° and with value of 9 V.

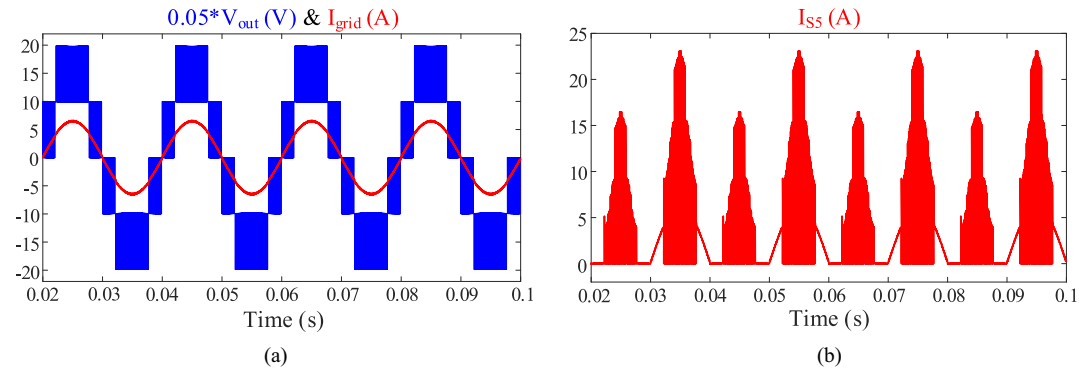

FIGURE 14. (a) Five-level inverter output voltage and injected grid current at unity PF. (b) Current of switch S_5 at unity PF.

Fig. 9(i) from the simulation results, the voltage blocked by switch S_5 is clearly bidirectional.

The operating modes, as presented in Fig. 2, correspond to the case where the inverter operates at unity PF (PF = 1). Under PF = 1, the current flowing through switch S_5 is unidirectional.

Fig. 14 illustrates the five-level inverter output voltage, the current injected into the power grid, and the current through switch S_5. As can be seen in this figure, under unity-PF conditions, switch S_5 conducts current only in one direction.

Since the proposed inverter is capable of controlling reactive power and can handle non-unity-PF loads, the current through switch S_5 becomes bidirectional under such conditions. To demonstrate this, in Section VI, the PF was set to zero (which represents the most extreme reactive-power condition for the inverter) in order to clearly show the bidirectional current behavior of switch S_5.

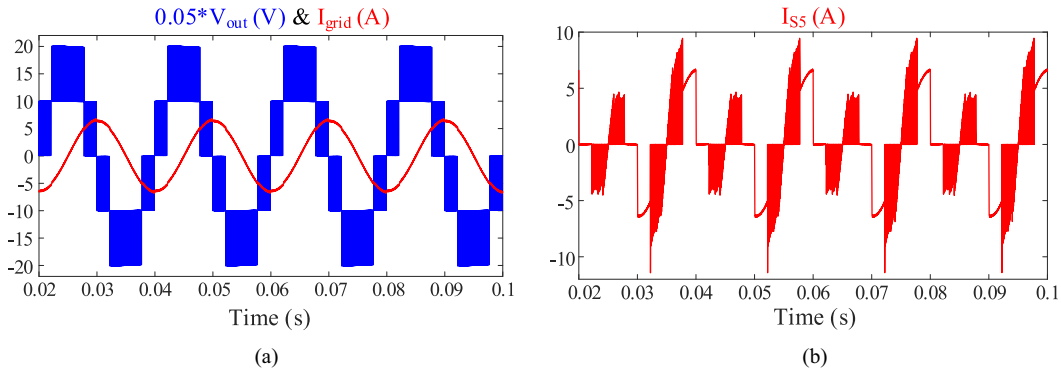

FIGURE 15. **(a) Five-level inverter output voltage and injected grid current at zero PF.**

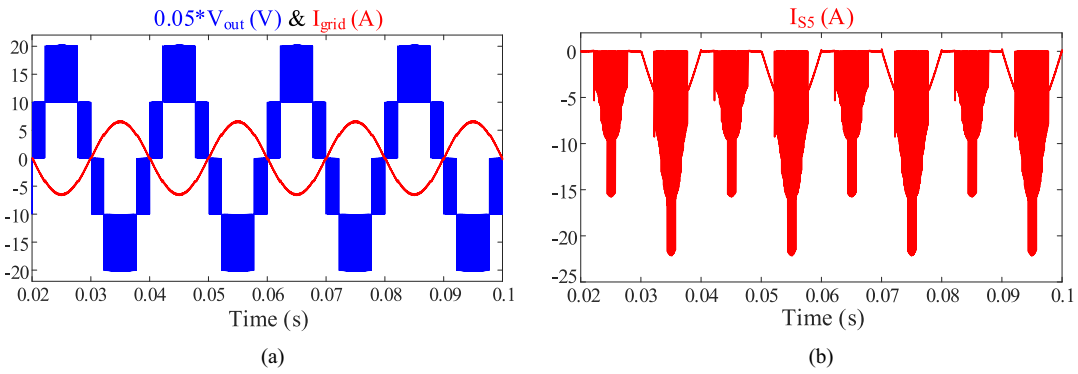

FIGURE 16. **(a) Five-level output voltage and grid current of the proposed converter in active rectifier mode. (b) Current of switch S_5 at active rectifier mode.**

The simulation results are presented in Fig. 15. In Fig. 15(a), the grid voltage and current are shown, while Fig. 14(b) illustrates the current flowing through switch S_5. As can be observed in Fig. 15(b), the current through switch S_5 is indeed bidirectional.

Another notable feature of the proposed inverter is its capability to operate as an active rectifier. In other words, the proposed five-level converter can also function as a five-level active rectifier.

In the active rectifier mode, the current flowing through switch S_5 is opposite in direction compared with the inverter mode. Fig. 16(a) shows the grid voltage and current in the active rectifier mode, while Fig. 16(b) illustrates the current flowing through switch S_5.

On the ripple behavior of the proposed inverter, specifically, at unity PF (PF = 1), the current and voltage waveforms are aligned, resulting in the highest inductor current ripple (0.8 A) and the largest capacitor voltage ripple (∼9 V). These conditions define the worst-case scenario for passive component stress and have been used as the basis for conservative filter and capacitor sizing. Under non-unity-PF conditions, such as PF = 0 and, in active rectifier mode, the phase shift between current and voltage reduces the peak ripple amplitudes, as observed in Figs. 15 and 16. Nevertheless, the inverter maintains stable performance, and the ripple levels remain within acceptable design margins. Therefore, the assumption of PF = 1 in the analytical design ensures reliable operation across all PF scenarios.

Based on the results, as shown in Figs. 15 and 16, it can be concluded that the current through switch S_5 is bidirectional, and therefore, a four-quadrant switch is required.

One of the key advantages of the proposed converter is that the capacitor in the circuit is charged and discharged at the switching frequency. This means that the required capacitance depends not only on the output power but also on the switching frequency. In other words, by increasing the switching frequency, the capacitor size can be reduced.

In SC converters where the capacitor charges and discharges at the switching frequency, it is possible to use film capacitors due to the relatively low required capacitance. The use of film capacitors enables the converter to be utilized in high-power applications.

In contrast to the proposed inverter, in other SC-based MLIs, the capacitors are charged and discharged at the grid frequency or a fraction of it, which limits their output power capability. Alternatively, for the same output power as the proposed inverter, those topologies require much larger capacitors.

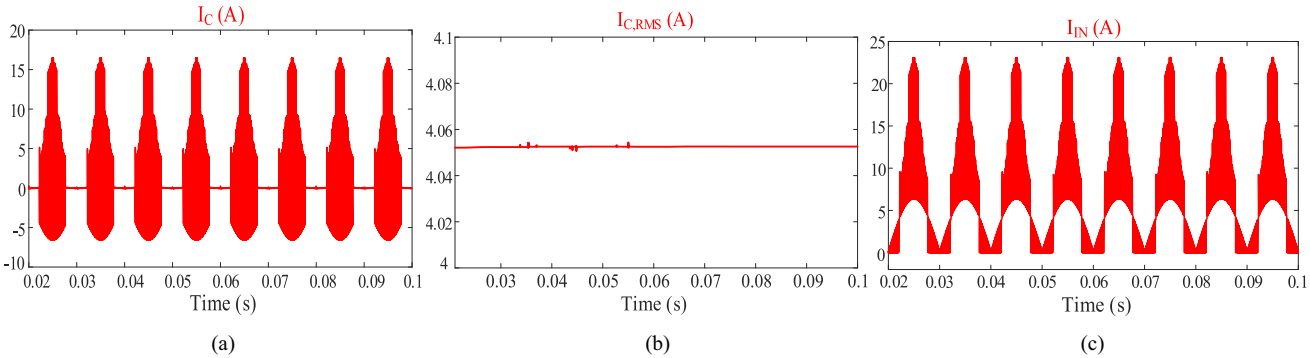

FIGURE 17. (a) Capacitor charging current waveform of the proposed inverter at 1 kW output power, switching frequency of 20 kHz, and capacitance of 20 μF, where the peak output current is approximately 6.5 A and the peak capacitorcharging current is about 16 A. (b) RMS value of the capacitor charging current from simulation, approximately 4.2 A. (c) DC input current in inverter mode at unity power factor, showing ripple at twice the grid frequency.

The capacitor charging current waveform of the proposed inverter at 1 kW output power, with a switching frequency of 20 kHz and a capacitor value of 20 μF, is shown in Fig. 17(a).

At 1 kW output power, the peak output current is approximately 6.5 A, the peak capacitor charging current reaches around 16 A, and the rms value is measured from the simulation, as approximately 4.2 A [see Fig. 17(b)].

As can be seen from this figure, even with a capacitor value of only 20 μF, the peak capacitor charging current remains below three times the peak grid current.

In single-phase systems, the power injected into the grid or the output load exhibits power ripple, with the frequency of the power fluctuations being twice the grid frequency. The proposed inverter is no exception to this rule and has power ripple as well. Since the proposed inverter does not use large capacitors, the power ripple is transferred to the dc input source.

To eliminate the power ripple from the input source, especially in PV systems, high-capacity decoupling capacitors are used. This method is known as passive decoupling. There is also another method known as active decoupling, where the energy storage elements are smaller than in the passive decoupling method, but this method is more complex compared with passive decoupling.

Fig. 17(c) shows the dc input current in inverter mode with a unity PF.

Since the grid frequency is 50 Hz, the fundamental current frequency of the dc input is, therefore, 100 Hz. By applying a decoupling capacitor at the input of the proposed inverter, the input current ripple can be filtered, resulting in smoother current from the input.

VII. EFFICIENCY ANALYSIS

To assess the power distribution and efficiency of the proposed inverter, this section focuses on analyzing the power losses associated with its components. The inverter consists of two primary types of losses: switching losses and conduction losses. The first category includes both turn-ON and turn-OFF switching losses, while the capacitor solely experiences conduction losses.

A. CONDUCTION LOSSES

Conduction losses generally stem from various factors during the operation of power switches, diodes, and passive components, such as ON-state resistance of switches (R_{DS}), forward-voltage drop of power diodes ($V_{\mathrm{Fw}\text{-}D}$), equivalent series resistance (ESR) of capacitors (R_C), and internal resistance of inductors (R_L). These factors in the proposed inverter are represented as follows:

$$P_{\mathrm{Cond-Switch}} = \frac{n(t)}{2\pi}\left[\int_0^{2\pi} R_{\mathrm{DS}} i^2(t) d(\omega t)\right] \tag{32}$$

$$P_{\mathrm{Cond-Capacitor}} = \frac{1}{2\pi}\left[\int_0^{2\pi} R_C i^2(t) d(\omega t)\right] \tag{33}$$

where $n(t)$ refers to the number of power switches in the current trajectory. The overall conduction losses of the proposed inverter are computed as follows:

$$P_{\mathrm{Cond-Total}} = \sum_{i=1}^{10} P_{\mathrm{Cond-Switch}_i} + P_{\mathrm{Cond-C}}. \tag{34}$$

B. SWITCHING LOSSES

Switching losses encompass both ON-state and OFF-state losses of switches. To simplify analysis, the voltage across and current passing through switches are linearized, yielding the ON-state and OFF-state switching losses for each power switch

$$\begin{aligned} P_{\mathrm{SW_{ON}}} &= \frac{1}{T_S}\left[\int_0^{t_{\mathrm{ON}}} V_{S-\mathrm{ON}}(t) i(t) d(t)\right] \\ &= \frac{n_{\mathrm{ON}} t_{\mathrm{ON}}}{6} f_S V_{\mathrm{ON}} I_{\mathrm{SW}} \end{aligned} \tag{35}$$

$$\begin{aligned} P_{\mathrm{SW_{OFF}}} &= \frac{1}{T_S}\left[\int_0^{t_{\mathrm{OFF}}} V_{S-\mathrm{OFF}}(t) i(t) d(t)\right] \\ &= \frac{n_{\mathrm{OFF}} t_{\mathrm{OFF}}}{6} f_S V_{\mathrm{Block}} I'_{\mathrm{SW}} \end{aligned} \tag{36}$$

I_{SW} and I'_{SW} represent the passing currents of each power switch after turning ON and just before turning OFF, respectively. Moreover, T_S and f_S denote the switching period and switching frequency of the inverter, respectively. The overall

TABLE 3. Comparison of the Proposed Five-Level Inverter With Other Similar Inverters

	P_{S1}	P_{S2}	P_{S3}	P_{S4}	P_{S5}	P_{S6}	P_{S7}	P_{S8}	P_{S9}	P_C	P_{Lf}
Switching loss	0.267	0.398	0.195	0.195	0.667	0	0	0.124	0.124	-	-
Conduction loss	3.57	3.56	0.4	0.4	6.33	0.992	0.992	0.992	0.992	0.254	7.953
Total loss	3.837	3.958	0.595	0.595	6.997	0.992	0.992	1.116	1.116	0.254	7.953

The bold values are highlighted only for visual emphasis and readability.

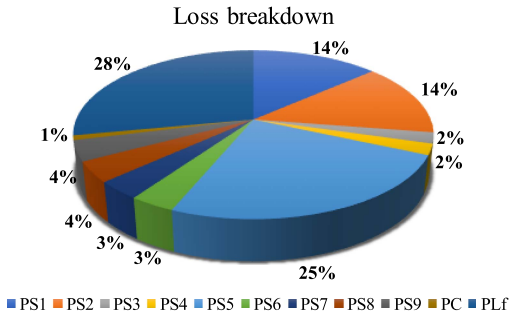

FIGURE 18. Pie chart of the share of loss percentage for the power switches.

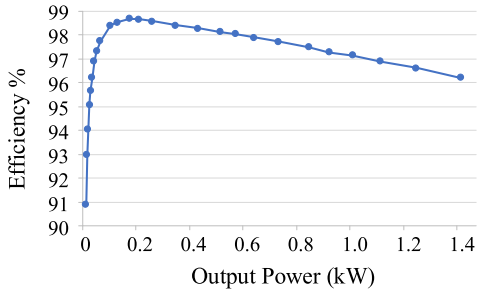

FIGURE 19. Simulation efficiency diagram of the proposed inverter for different output powers.

switching losses are determined as follows:

$$P_{\mathrm{SW-Total}} = \sum_{i=1}^{10} \left(P_{\mathrm{SW_{ON}}} + P_{\mathrm{SW_{OFP}}}\right). \tag{37}$$

Considering (32) and (35), the overall losses of the proposed inverter will be obtained as follows:

$$P_{\mathrm{Loss-Total}} = P_{\mathrm{Cond-Total}} + P_{\mathrm{SW-Total}}. \tag{38}$$

As mentioned, the simulation parameters used for calculating the losses, overall inverter efficiency, and the detailed loss breakdown between active and passive components are summarized in Table 2. These include the ESR of the flying capacitor and the series resistance of the output inductor, ensuring that their associated losses are accurately represented. The switching and conduction losses of each active and passive component have been calculated and are now presented in Table 3. The data confirm that S_6 and S_7 exhibit no significant switching losses; their total losses arise solely from conduction losses, as expected. Notably, the switching losses include both the turn-ON and turn-OFF transitions as well as the discharge of the MOSFETs drain–source parasitic capacitance.

Furthermore, the pie chart in Fig. 18, generated based on the data provided in Table 3, accurately illustrates the distribution of total losses—comprising both conduction and switching losses—across all active and passive components at an output power of 1 kW. It is also clarified that the switching loss calculations take into account both the turn-ON and turn-OFF transitions, as well as the capacitive discharge associated with the drain–source capacitance of the MOSFETs, thereby ensuring a comprehensive loss evaluation.

The efficiency curve, also shown in Fig. 19, presents the inverter's simulated efficiency across a wide output power range from 15 W to 1.4 kW. As observed, the inverter achieves a peak efficiency of 98.14% at 500 W output power under the simulation conditions, as specified in Table 2.

At the same output power, a higher input voltage leads to a lower input current, which reduces conduction losses and results in higher overall efficiency.

These results demonstrate that the proposed inverter achieves excellent efficiency performance while accounting for all significant loss components, including the ESR of the capacitor.

C. THERMAL DESIGN CONSIDERATIONS

Total power loss at a 500 W output power condition is observed. Given the experimentally measured efficiency of 96.5% at this point, the total power dissipation is approximately 18 W. Assuming a maximum allowable junction temperature of 120 °C and an ambient temperature of 25 °C, along with datasheet values of $R_{\theta jc}$= 0.3 °C/W (junction-to-case) and $R_{\theta cs}$= 0.5 °C/W (case-to-heatsink), the required heatsink-to-ambient thermal resistance is calculated using the following expression:

$$T_j = T_{\mathrm{amb}} + P \cdot \left(R_{\theta jc} + R_{\theta cs} + R_{\theta sa}\right) \tag{39}$$

$$120 = 25 + 18 \cdot (0.3 + 0.5 + R_{\theta sa}) \Rightarrow R_{\theta sa} \leq 4.48\,^{\circ}\mathrm{C/W}. \tag{40}$$

Therefore, a heatsink with a thermal resistance of 4.48 °C/W or lower is sufficient to maintain device junction temperatures within safe limits under continuous full-load operation.

VIII. COMPARISON STUDY

A thorough comparison has been conducted between the proposed five-stage inverter and several other existing solutions. The results obtained are meticulously analyzed to evaluate the performance, efficiency, and suitability of the proposed inverter.

The quantity of power switches, gate drivers, and diodes used, the number of inductors and capacitors (excluding the output filter), the total count of components (T.C.), the required input dc sources, the input voltage value (V), the voltage boost function, the voltage gain factor, and the output power (P_{out}), total cost (\$), cost per unit of output power (Cost/P_{out} %), efficiency (%), and evaluation of active and reactive-power support have been conducted to provide a comprehensive understanding of the comparative performance and feasibility of the proposed five-stage inverter in relation to its counterparts. It is worth noting that the "Cost/P_{out}" column, as presented in Table 4, does not reflect an absolute monetary value nor a literal percentage. Instead, it is a normalized cost–performance index, defined as the estimated relative cost of each topology divided by its rated output power. This metric enables a fair and scalable comparison across various inverter structures, especially since each prototype was designed for different voltage and power levels using components with specific ratings. The cost values take into account the quantity and type of active and passive components (e.g., power switches, capacitors, and gate drivers), as well as their voltage/current ratings. By dividing the total cost by the prototype's output power, we obtain a unitless value that facilitates objective comparison between designs with different power scales. This cost index helps to highlight the cost-effectiveness of the proposed inverter compared with other five-level SC-based topologies.

The summarized results are presented in Table 4. A careful approach was employed to determine the price of each inverter, obtaining individual component prices from reputable distributors of power electronic components. Each element used in the construction of the converter was sourced diligently, and its price was accurately documented. By summing the costs of all components, an overall estimate of the converter's price was obtained. The capacitor C used in the proposed inverter functions by charging and discharging at a high switching frequency.

This characteristic results in significantly reduced voltage ripple across the capacitor, enabling the use of a lower rated capacitor. As a result, this optimization contributes to a decrease in system volume and cost while simultaneously enhancing power density, which is another benefit of the proposed inverter.

By minimizing voltage ripple and optimizing capacitor selection, the proposed converter stands out by providing improved performance in a more compact design, offering considerable advantages in terms of cost-effectiveness and power density.

In addition to the comparative analysis, as presented in Table 4, a more detailed assessment is provided here to specifically compare the inverter topology proposed in [47] with the topology presented in this work. The topology in [47] demonstrates a lower initial cost and slightly higher conversion efficiency, attributed to its simplified structure, reduced number of active and passive components, and less complex control scheme. In addition, it offers a higher step-up ratio and supports reactive-power injection, making it an effective solution for applications that prioritize cost, simplicity, and basic grid support capabilities.

However, the proposed inverter, despite requiring a higher initial investment and a more sophisticated control approach, offers several significant advantages in terms of operational performance and system sustainability.

1) Improved current and voltage sharing among the switches, leading to reduced stress on individual devices and enhancing their operational lifetime.
2) Enhanced voltage regulation and output stability, particularly under dynamic or varying load and grid conditions.
3) Lower voltage stress across the switching devices, contributing to extended device lifespan and more reliable system operation.
4) Better control over common-mode voltage fluctuations, resulting in minimized leakage current and improved compliance with electromagnetic compatibility standards.
5) Increased control flexibility, enabling advanced grid support functionalities, including reactive-power control and dynamic current shaping.

Therefore, although the inverter proposed in [47] is favorable for scenarios where initial cost, efficiency, and simplicity are the primary concerns, the proposed inverter provides superior performance in applications requiring stable operation over a wide range of operating conditions, extended system lifespan, and improved safety in grid-tied environments.

Although the proposed inverter uses a total of 20 components, which is three times more than the topology in [40], it achieves a significantly lower cost-to-output-power ratio. This improvement is primarily attributed to the use of standard, low-cost components, such as 600 V, 20 A MOSFETs and a single low-value film capacitor. Unlike [40], which requires quasi-resonant charging circuits and potentially higher voltage or specialized switches and capacitors, the proposed topology operates with a simple and cost-effective control strategy, minimal auxiliary circuitry, and no additional voltage-balancing or soft-start circuits. Furthermore, the inverter's high efficiency and reduced thermal stress lower the need for expensive cooling or oversizing of components. These factors collectively result in a cost-effective design with an actual implementation cost of only \$43.5 for 500 W output, yielding a cost-to-output ratio of 7.7%, which is significantly lower than that of other compared SC-based inverters.

TABLE 4. Comparison of the Proposed Five-Level Inverter With Other Similar Inverters

Ref	Number of components					T.C	N_{IN}	V_{IN} (V)	High Step-Up	Step-Up factor	P_{out} (W)	Total cost ($)	Cost/P_{out}	RPS	Reported Rated Efficiency
	N_{SW}	N_{Driver}	N_{Diode}	N_{cap}	N_L										
[34]	8	8	7	2	3	28	3	100	Yes	2	600	284.3	0.48	No	86%@0.6 kW
[35]	8	8	4	3	2	25	2	100	Yes	1.5	1000	151.8	0.16	Yes	N.R
[36]	8		1	2	0	11	1	200	Yes	2	1000	189.3	0.2	Yes	NR
[37]	6	6	3	2	1	18	1	60	Yes	4	600	59.13	0.1	N.R	N.R
[38]	8	8	1	3	0	20	1	160	No	1	500	114.3	0.23	Yes	96.8%@9.5 KW
[39]	6	6	2	2	0	16	1	200	Yes	2	1000	250.2	0.252	Yes	98.1%@0.6 kW
[40]	6	8	0	2	2	18	1	100	Yes	$\frac{2D}{1-D}$	200	85.72	0.43	No	92%@1 kW
[41]	7	7	1	1	1	17	1	200	Yes	2	1000	165.8	0.17	Yes	98.8%@1 kW
[42]	6	6	0	1	0	13	1	200	No	1	770	208.1	0.27	Yes	N.R
[43]	12	12	0	4	0	28	1	50	Yes	4	250	165.3	0.67	No	94%@0.25 kW
[44]	8	8	3	4	2	25	1	200	Yes	2.8	2000	694.9	0.35	N.R	90%@1 kW
[45]	8	7	1	2	0	18	1	50	Yes	2	250	147.2	0.58	Yes	96%@1 kW
[46]	10	10	4	2	2	28	2	200	Yes	1.5	500	163.8	0.33	N.R	N.R
[47]	5	5	0	2	1	13	1	100	Yes	$\frac{D}{1-D}$	200	189.4	0.5	Yes	92.5%@0.2 kW
[48]	9	8	0	2	0	19	1	200	Yes	2	1000	74.1	0.074	Yes	98.5%@ 1 kW
[49]	10	10	0	1	1	22	1	100	Yes	2	360	150.3	0.42	No	N.R
[50]	11	11	0	2	2	26	1	360	No	1	1000	135.1	0.14	Yes	97.8%@1 kW
[54]	4	4	2	2	2	18	1	425	No	1	600	163.3	0.27	Yes	97%@0.6 kW
[55]	9	8	0	3	1	21	1	400	No	1	510	161.98	0.32	Yes	98.04%@0.51 kW
[57]	6	6	2	1	1	16	1	200	Yes	2	3424	130	0.04	Yes	98.58%@3.4 kW
[58]	7	7	0	1	1	16	1	200	Yes	2	2000	135	0.07	Yes	98.3%@20 kW
[59]	7	7	2	1	0	17	1	200	Yes	2	600	61.5	0.11	Yes	96%@0.6 kW
[60]	8	8	4	1	2	23	1	100	Yes	2	300	66.5	0.23	Not Evaluated	96.5%@0.3 kW
[61]	7	7	3	2	0	19	1	100	Yes	2	500	41.4	0.09	Not Evaluated	92@0.5 kW
[62]	6	6	0	2	0	14	1	100	Yes	2	500	41.5	0.09	Not Evaluated	97%@0.5 kW
[63]	8	8	1	2	0	19	1	100	Yes	2	1000	45.6	0.05	Yes	96%@1 kW
[64]	8	8	2	2	0	20	1	100	Yes	2	600	42.3	0.07	Yes	94%@0.6 kW
[65]	9	9	2	2	0	22	1	100	Yes	2	500	44.5	0.09	No	95%@0.5 kW
Prop	8	8	0	1	0	20	1	100	Yes	2	500	43.5	0.07	Yes	97.24%@1 kW

To ensure a more focused and meaningful evaluation of the proposed inverter, Table 4 has been updated to include a dedicated comparison with ten recently published *SC-based five-level inverters* [30], [31], [32], [33], [34], [35], [36], [37], [38], [39]. These newly added references are *highlighted in blue* to clearly distinguish them from other conventional MLI topologies. All selected designs are transformerless, grid-connected, single-phase inverters with step-up voltage capability, making them directly comparable with the proposed structure.

This refined comparison highlights the proposed inverter's advantages in terms of:

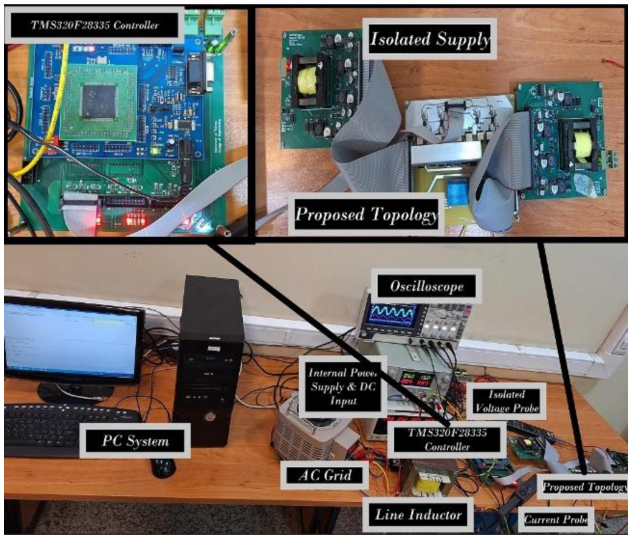

FIGURE 20. Photograph of the experimental prototype of the proposed five-level inverter.

TABLE 5. List of Utilized Components and Needed Descriptions of Laboratory Prototype

Component	*Type*	*Description*
S_1, S_2, S_3, S_4, S_5, S_6, S_7, , S_8, and S_9	FQPF20N60	600 V/20 A
Microcontroller (Texas Instruments)	DSP TMS320F28335	C2000
Current transducer	LA55P	Hall effect
Gate Driver	FOD3120	IC
Local grid frequency	50 Hz	-
Switching frequency	5 KHz	-
Input voltage	100 V	-
Output power	500W	-
Output voltage	200 V	-
Grid voltage	200 V (peak) / 141 V (rms)	-
C	Aluminum Electrolytic	2700 μF
Inductor L_f	Iron core	5 mH

1) lower total number of active and passive components;
2) built-in voltage boosting without additional dc–dc stages;
3) lower cost-per-watt ratio;
4) support for reactive-power delivery;
5) high reported efficiency (96.5% at 0.5 kW).

As a result, the proposed inverter demonstrates a well-balanced and competitive performance compared with other existing SC-based five-level inverters in the literature.

The analysis, as presented in the table, clearly illustrates that the proposed inverter outperforms the other five-level inverter topologies in terms of both cost and volume, boasting the lowest values in these categories. The examination of different structures emphasizes the unique benefits provided by the proposed inverter design.

IX. EXPERIMENTAL VERIFICATION

A laboratory prototype, as illustrated in Fig. 20, has been developed to achieve an output power of 500 W. The captured waveforms offer insights into its performance and summarize the specifications of the key components. Table 5 summarizes the specifications of the utilized components. It is important to note that the grid voltage is transformed from 220 V rms to 141 V rms using an autotransformer.

In Fig. 21(a), the graph depicts the five-level output voltage and the current injected into the grid, specifically at a unity PF. The peak values for both the inverter's output voltage and the current injected into the local grid are approximately 200 V and 5 A, respectively.

The five-level output voltage waveform, grid voltage, grid current, and voltage across capacitor C at the lagging PF are illustrated in Fig. 21(b).

Also, the same results are illustrated in Fig. 21(c) at the leading PF. Considering Fig. 21, by implementing the closed-loop control strategy, the proposed grid-tied inverter is capable of injecting a sinusoidal current into the grid under various PF conditions.

In addition, the voltage stress on the switches S_1–S_9 is shown in Fig. 22.

Due to the limited laboratory resources and to avoid damaging the power switches during testing, the experimental setup was configured to operate at reduced voltage and power levels. Specifically, the input and output voltages were set to 100 V and 200 V, respectively, resulting in a maximum experimental output power of 500 W. In contrast, the simulation results were obtained under rated conditions ($V_{\text{in}} = 200$ V and $V_{\text{out}} = 400$ V) to demonstrate full-load behavior.

To validate the simulation model, an additional simulation was performed under the same conditions as the experiment ($V_{\text{in}} = 100$ V, $V_{\text{out}} = 200$ V, and $P_{\text{out}} = 500$ W). Under these identical conditions, the simulated efficiency was found to be 97%, while the measured experimental efficiency was 96.5%, showing a close match with only 0.5% deviation. This difference is reasonable, considering the inherent limitations of simulation in capturing real-world parasitic and thermal behavior.

Furthermore, the step-response test from 500 W to 1 kW, briefly shown in Fig. 23, was conducted to evaluate the dynamic response of the closed-loop control system under large load transients. The change involves a shift from 4 to 8 A, leading to an increase in the injected current to the grid and active power from 500 to 1000 W, respectively. This indicates that the proposed inverter shows a positive response to the change in reference current amplitude from 4 to 8 A. Although 1 kW exceeds the continuous rating of the laboratory setup, the converter successfully handled this brief power step without instability or performance degradation, demonstrating the controller's robustness. The high quality of sinusoidal current injection and system stability was maintained, confirming the inverter's suitability for practical grid-tied applications.

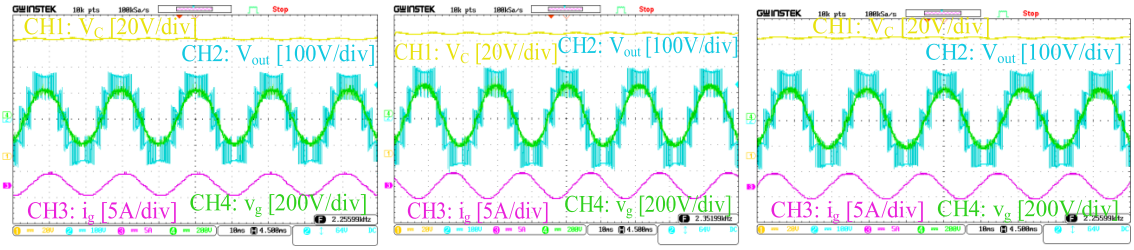

FIGURE 21. Experimental results at different conditions of PF. (a) Unity PF: CH1: Voltage across capacitor *C*, CH2: Five-level output voltage, CH3: Injected current to the grid, and CH4: Grid voltage. (b) Lagging PF: CH1: Voltage across capacitor *C*, CH2: Five-level output voltage, CH3: Injected current to the grid, and CH4: Grid voltage, leading PF: CH1: Voltage across capacitor *C*, CH2: Five-level output voltage, CH3: Injected current to the grid, and CH4: Grid voltage. (c) Leading PF . CH1: Voltage across capacitor C,CH2: Five-level output voltage, CH3: Injected current to the grid, and CH4: Grid voltage.

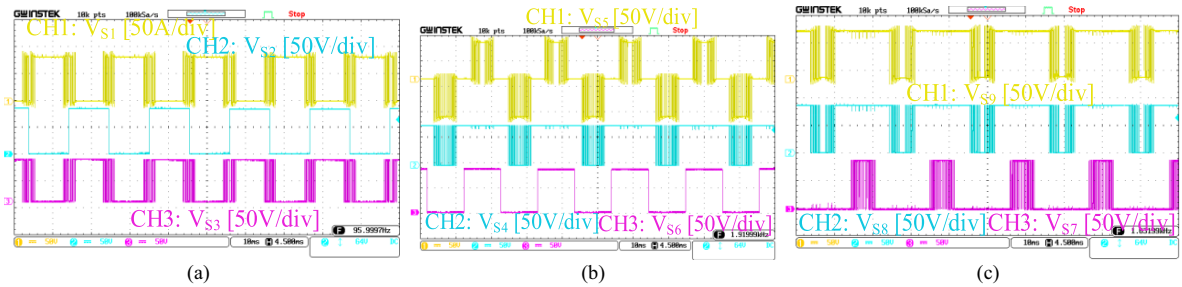

FIGURE 22. Voltage stress of switches. (a) CH1: V_{S1}, CH2: V_{S2}, and CH3: V_{S3}. (b) CH1: V_{S5}, CH2: V_{S4}, and CH3: V_{S6}. (c) CH1: V_{S9}, CH2: V_{S8}, and CH3: V_{S7}.

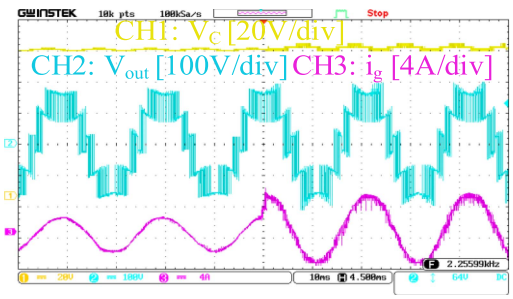

FIGURE 23. Experimental results under a step change in the amplitude of reference current. CH1: Voltage across capacitor *C*, CH2: Five-level output voltage, and CH3: Injected current to the grid.

TABLE 6. THD (%) of the Grid Current in the Experimental Results

PF load	*THD (%)*
Unity PF	3.17%
Leading PF	3.12
Lagging PF	3.34

Finally, the THD (%) values of the grid current in the experimental results for unity, leading, and lagging PFs are specified in accordance with Table 6.

X. CONCLUSION

In this article, a new transformerless five-level grid-connected inverter based on an SC topology has been proposed, analyzed, and experimentally validated. The inverter integrates a single SC cell that operates at high switching frequency and achieves effective capacitor charging/discharging in both half cycles. This design minimizes capacitor size, voltage ripple, and thermal stress while maintaining a voltage-boosting factor of 2, thereby eliminating the need for a separate dc–dc boost stage.

Unlike the conventional five-level inverters, the proposed topology does the following:

1) utilizes only nine switches, of which only five operate at high frequency;
2) supports bidirectional current conduction through a central four-quadrant switch (S_5), enabling reverse power flow from grid to dc source;
3) offers reactive-power support under both leading and lagging PF conditions.

The reliability analysis, based on the MIL-HDBK-217F model, confirmed a high MTTF of 4.57×10^6 h, thanks to reduced switching stress and balanced voltage operation. The experimental results demonstrated the practical feasibility of the proposed design at 500 W output power. A measured efficiency of 96.5% was recorded under $V_{in} = 100$ V and $V_{out} = 200$ V, while simulation under identical conditions yielded 97%, confirming the model's accuracy within 0.5%.

To showcase system stability, a dynamic step-load test from 500 W to 1 kW was performed, demonstrating effective regulation by the closed-loop control system. Furthermore, simulation studies up to 1 kW output confirmed that the inverter maintains a peak efficiency of 98.14% at 500 W and 97.15% at 1 kW when operating under nominal design voltage ($V_{in} = 200$ V and $V_{out} = 400$ V).

Overall, the proposed five-level SC-based inverter delivers an optimal combination of compactness, efficiency, voltage boosting, and reliability, making it a strong candidate for future grid-connected renewable energy systems and distributed generation architectures.

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