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Predictive DC Fault Ride-Through for Offshore MMC-Based MT-HVDC Grid

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ABSTRACT Unscheduled event handling capability and swift recovery from transient events are indispensable study areas to ensure reliability in offshore multiterminal high-voltage dc (MT-HVdc) grids. This article focuses on enhancing the reliability of half-bridge modular multilevel converters (HB-MMCs) in MT-HVdc grids by introducing a predictive dc fault ride-through (DC-FRT) recovery controller and fault separation devices. A novel dc protection-informed zonal DC-FRT scheme for HB-MMCs is proposed, incorporating a model predictive planner for optimized control inputs based on local and interstation measurements and converter constraints. A real-time digital simulator environment simulates the approach, which improves lower level control during fault interruption and suppression by utilizing fault detection and location information. In addition, the study examines two control schemes to assess the impact of communication delays in MT-HVdc grids, a critical factor for system stability and reliability during faults. These schemes include a centralized scheme with delays in input and output signals and a decentralized approach focusing on external signal delays. Both are compared against a baseline centralized control with no delays. These approaches explore alternatives for the placement of the proposed controller, considering potential delays in interstation high-speed communication. The findings underscore the significance of the proposed DC-FRT control in reinforcing MT-HVdc systems against faults, which contributes to efficient recovery and grid stability.

INDEX TERMS High-voltage dc (HVdc), modular multilevel converter (MMC), model predictive control (MPC), model predictive planner (MPP), real-time digital simulator (RTDS).

I. INTRODUCTION

While the ever-growing energy demands and the pursuit of zero carbon emissions present complex challenges, they also offer unique opportunities for transmission system operators (TSOs) in Europe [1], [2]. These challenges inspire TSOs to innovate and adapt, aligning their long-term plans toward achieving carbon neutrality and fostering a more sustainable and resilient energy infrastructure. The offshore multiterminal high-voltage dc (MT-HVdc) grid is preferred over its ac counterpart to overcome this crisis and achieve carbon neutrality. MT-HVdc is preferred because of its fast controllability, high power transmission over a larger distance, and good power quality, as well as its modular design due to the application of a modular multilevel converter (MMC). With inherent reliability and grid-connected features during dc faults, numerous MT-HVdc configurations are planned in Europe [3] and commissioned in Zhangbei, China [4].

MMC technology, based on the submodule (SM) topology, is classified into half-bridge (HB), full-bridge (FB), and hybrid configurations [5]. HB-MMCs are preferred because of their lower cost and carbon footprint. However, they require dc fault interruption capability, often addressed using dc circuit breakers (DCCBs) in MT-HVdc systems [6]. To ensure uninterrupted operation, HB-MMCs require rapid dc fault detection (< 1 ms) and rapid DCCB action (< 3 ms). However, equipment operation, fault detection, and communication delays often hinder this process, creating reliability challenges in fault interruption [7], [8], [9]. Passive fault current-limiting devices are commonly used to counteract these delays, but they increase system inductance, interact with converter control, and require more footprint and investment.

Fault suppression control (FSC) is an alternative control that manipulates converter state variables to manage fault currents effectively. Various studies have explored hybrid MMC with droop control and other techniques for this purpose, offering comparative insights into different methods [10], [11], [12], [13], [14], [15], [16]. These strategies typically use proportional-integral (PI) controls in the outer or lower level control loop, but mode-dependent strategies during faults may affect system stability [17]. Thus, while several solutions enhance fault response, careful consideration is required in their application to maintain system stability and efficiency.

In our previous work [26], we addressed the potential issue caused by mode-dependent strategies by suppressing fault current in MT-HVdc systems using a continuous setpoint based on local measurements and converter limits, achieving satisfactory performance in handling delayed fault interruptions. However, the system's reconfiguration due to DCCB operation led to new transient and steady states, challenging the control's ability to ensure smooth, damped recovery. Subsequent studies such as [22] have underscored the significance of the damping coefficient in postinterruption and introduced control methods, including a temporary active power stop mode, which risks frequency instability in grids with lower short circuit ratio (SCR) [27]. Other approaches involve blocking currents using diodes, as discussed in [23], although this has practical limitations in the actual MT-HVdc grids. Advances in control strategies for dc fault ride-through (DC-FRT) are evident in [9], [18], and[19], where the exploration of FB-MMC is provided and voltage rebalancing techniques, alongside rapid recovery methods [8] and innovative hybrid-MMC topologies for enhanced fault management [24], [25]. These collective efforts demonstrate the transition of the MT-HVdc system toward resilience and fault recovery strategies.

In this article, we propose a novel dc protection-informed zonal DC-FRT scheme for offshore MT-HVdc grids. In this scheme, each HB-MMC is driven by a model predictive planner (MPP) providing optimized control input to the lower level control. The planner receives the local and interstation measurements through two reference generators (i.e., during fault interruption and system recovery). Furthermore, fault detection and location information by the dc protection algorithm is applied to regulate the control energy of the lower level control during fault interruption and suppression period, integrating the ride-through control with the protection concept (detection and location). The improvement in the ride-through performance comes with the mathematical integration of control and protection. This article also proposes three schemes to highlight the impact of high-speed interstation communication delay.

This article addresses an enhanced DC-FRT strategy for offshore MT-HVdc systems. Section I highlighted the motivation behind the DC-FRT.

The rest of this article is organized as follows. Section II reviews existing methods; HB-MMC is described together with its applied controls in Section III; Section IV introduces the proposed DC-FRT control; Section V details fault identification and location; Section VI presents the MMC-MTDC grid test bench; Section VII discusses simulation results; and finally, Section VIII concludes this article.

II. EXISTING DC-FRT STRATEGIES FOR MT-HVDC

Table 1 summarizes the recently proposed DC-FRT strategies for MT-HVdc. Irrespective of the topology and SM technology of MMC, MT-HVdc goes through three stages of DC-FRT. Namely, through fault interruption, system recovery, and system attaining a new steady state as depicted in Fig. 1. In the fault interruption stage, the first dc fault occurrence results in local protection operation due to threshold violation of the arm current and dc-link voltage [8]. In addition, Kontos et al. [8] describe a communication-based centralized protection algorithm, which takes input from the local protection of converters. The flag raised by protection (i.e., centralized and/or local) can be used to "*temporary stop P & Q*"[8], or used as input to trigger an FSC [9]. With "*temporary stop P & Q*," the converters enter *block* state within 2–3 ms after fault [22]. With the converter blocking, the in-feed power support to the ac grid is removed temporarily, and the fault current is interrupted accordingly. Then, a dc disconnector and/or ac breaker isolate the faulty zone or a converter in the MT-HVdc grid. In the case of FSC, the control tries to minimize the fault current to zero, and then, DCCB is used to interrupt the fault and isolate the faulty zone. With FSC, the ac system is connected to the dc grid, allowing for control over power, a mode referred to as "*continuous P & Q*" [7].

After the fault current is interrupted, the MT-HVdc grid goes through *system recovery* stage. Depending upon which power mode (i.e., "*continuous P & Q*" or "*temporary stop P & Q*"), extra recovery steps are carried out [18]. In case *temporary stop P & Q*, STATCOM mode is activated to support the ac grid. This is followed by the dc voltage control in each converter by connecting the dc disconnector. This control regulates the dc-link voltage, eliminating the overvoltage and voltage transient in the dc link [9], [20]. In the case of "*continuous P & Q*," STATCOM mode is bypassed [9]. Besides, Wang et al. [21] provided a delayed reclose of converters to avoid dc voltage transients. Once the dc-link voltage is within the accepted system voltage band [9], [22], new droop/ramp characteristics [20] or new setpoints [19] are provided by the station control or centralized grid control, which results in *"new steady state."*

The majority of DC-FRT creates a prolonged power loss to the ac grid, which might result in frequency deviation. Furthermore, the MT-HVdc grid under investigation is grid-following and invalid in the current offshore network. Converter blocking could have adverse effects on the wind power park. Furthermore, fast dc fault interruption is observed in FB-MMC. However, considering the frequency of fault occurrence versus operational losses, FB-MMC has become uneconomical, and current projects focus more on HB-MMC. Similarly, each converter control only has information during system recovery. As a result, resynchronization with other converters leads to current and voltage transients and delayed

TABLE 1. Existing DC-FRT for the MMC-VSC HVDC System

Literature	SM topology	Converter control mode	HVDC topology	DC-FRT Method	DC-FRT power operation	DC-Zone based	New steady state time	Fault detection and localization
[9]	FB-MMC	Pac-Q, Vdc-Q	Mesh grid	Separate Vdc control at outer loop	Continuous operation	No-zone	71 ms	No, local protection
[18]	FB-MMC	Vdc-Pdc droop, Pac-Q	Mesh grid	Sequence-based	Temporary P & Q stop	No-zone	600 ms [a]	No, local protection
[19]	FB-MMC	Pac-Q, Vdc-Q	Mesh grid	Sequence-based	Temporary P & Q stop	No-zone	100 ms	No, local protection
[8]	FB-MMC	Pac-Q, Vdc-Q	Mesh grid	Sequence-based	Temporary P & Q stop	No-zone	158 ms	Yes, centralized protection
[20]	HB-MMC	Pac-Q, Vdc-Q	Mesh & Radial grid connected via DCCB	Sequence based	Temporary P & Q stop	Yes, but for DC selection	200-300 ms [b]	No, local protection
[21]	HB-MMC	Pac-Q, Vdc-Q	Radial grid	Sequence-based	Temporary P & Q stop	No-zone	20 s	No, local protection
[22]	HB-MMC	Vdc-Pdc droop, Pac-Q	Mesh grid	Vdc-control and CSCC control	Temporary P & Q stop	No-zone	100 ms	No, local protection
[23]	HB-MMC	Vac-f, Vdc-Q	Radial grid	Diode-based control	Continuous operation	No-zone	200 ms	No, local protection
[24]	Hybrid-MMC	Pac-Q, Vdc-Q	Mesh grid	Switch mode and sequence-based	Temporary P & Q stop	No-zone	100-200 ms	No, local protection
[25]	Hybrid-MMC	Pac-Q	NA	Energy-based control	Temporary P stop	No-zone	500 ms	No, local protection
Proposed method	HB-MMC	Vac-f, Vdc-Q	Mesh grid	Predictive control	continuous operation	Yes	20 ms	Yes, centralized protection

[a]Longer time due to System re-energised after fault interruption by converter and AC breaker
[b]Shorter time compared to [18] because faulty part of system is selectively isolated by DCCB

recovery. In addition, in great part, system recovery is not selective and is influenced by the converters' voltage and current parameters during transient phenomena.

This article strategically addresses research gaps in offshore MT-HVdc grids by introducing a novel approach. By applying an MPP for HB-MMC [28], [29], the proposed method ensures a rapid fault ride-through with a DCCB, and effectively minimizes power loss and frequency deviations. Integrating a dc protection algorithm enhances the fault detection and location, facilitating precise control regulation during fault interruption and recovery phases. This accelerates dc fault recovery and mitigates potential adverse effects on the wind power park. Two additional schemes are introduced to strengthen system resilience further and reduce reliance on high-speed interstation communication. These schemes contribute to $N-1$ contingency, enhancing overall grid reliability.

III. HB-MMC

As already mentioned, the HB-MMC is chosen for the implementation of the converters. This topology is depicted in Fig. 2. As visible from Fig. 2, an MMC has three legs, one per phase, and each leg has an upper and a lower arm. Furthermore, each MMC arm also contains the equivalent inductance and resistance, denoted as L_{arm} and R_{arm}, respectively.

The MMC's currents and voltages are usually in the equations used in $\Sigma-\Delta$ format as follows:

$$i_j^{\Delta} = i_j^U - i_j^L, \quad i_j^{\Sigma} = \frac{i_j^U + i_j^L}{2} \tag{1a}$$

$$v_{Mj}^{\Delta} = \frac{-v_{Mj}^U + v_{Mj}^L}{2}, \quad v_{Mj}^{\Sigma} = v_{Mj}^U + v_{Mj}^L \tag{1b}$$

where i_j^U and i_j^L are currents of the upper and the lower arm of the phase $j \in \{a, b, c\}$, while v_{Mj}^U and v_{Mj}^L are the upper and lower arm voltages of the phase $j \in \{a, b, c\}$.

The control loop framework of the converters is depicted in Fig. 3. The control principle for the onshore converter is based on the vector control method, where there is a cascaded connection of outer voltage control (OVC) and inner current control (ICC) along with circulating current suppression control (CCSC). The ICC derives its reference from OVC, while CCSC zeroes summation d and q currents and aligns zero current with the DC-FRT signal. These control loops are implemented as PI controllers on the way described in [30], and with the same parameters as in [30].

For synchronization, the phase-locked loop generates the necessary angle (θ), with the offshore converters adopting a direct voltage control method for the grid-forming converters and generating θ through a voltage-vontrolled oscillator.

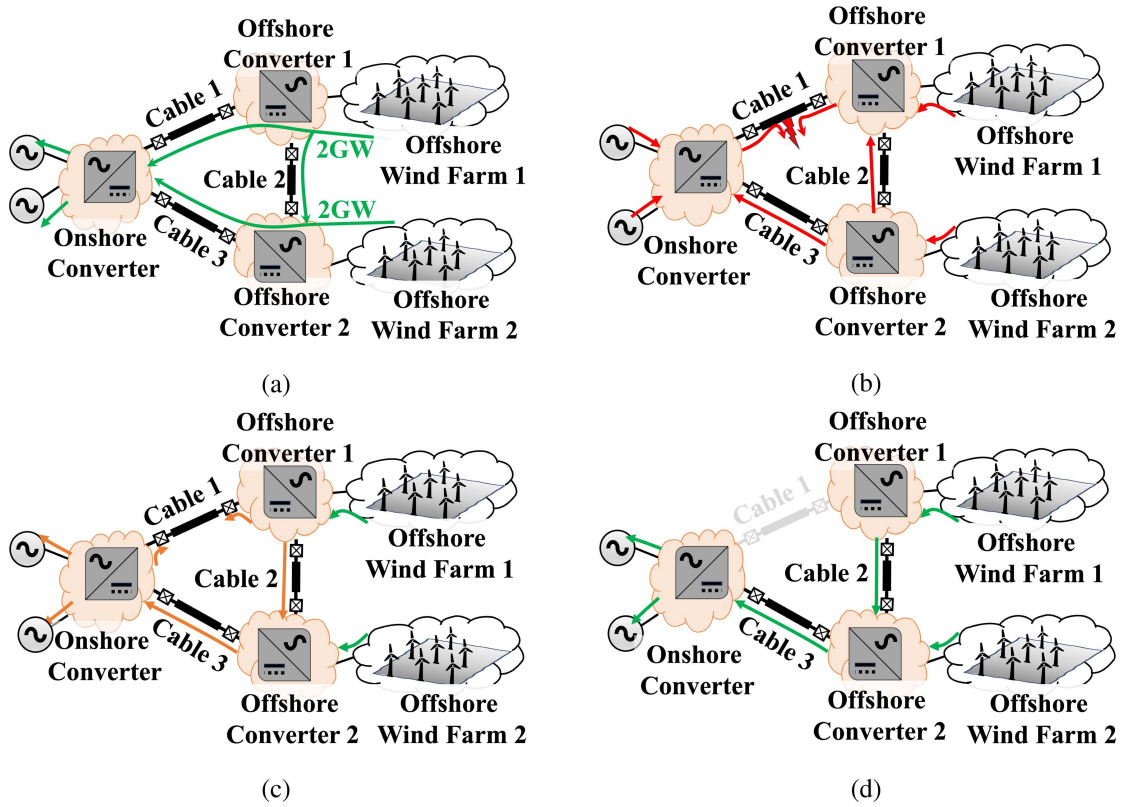

FIGURE 1. Illustration of the stages involved in DC-FRT. (a) Steady state. (b) Fault interruption. (c) System recovery. (d) New steady state.

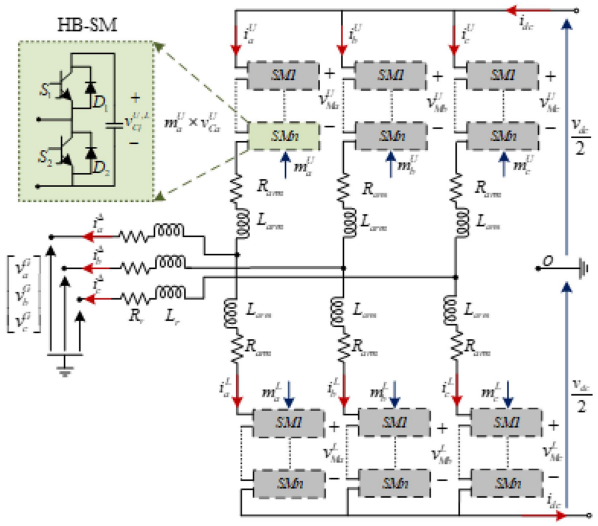

FIGURE 2. Mathematical model of an HB-MMC.

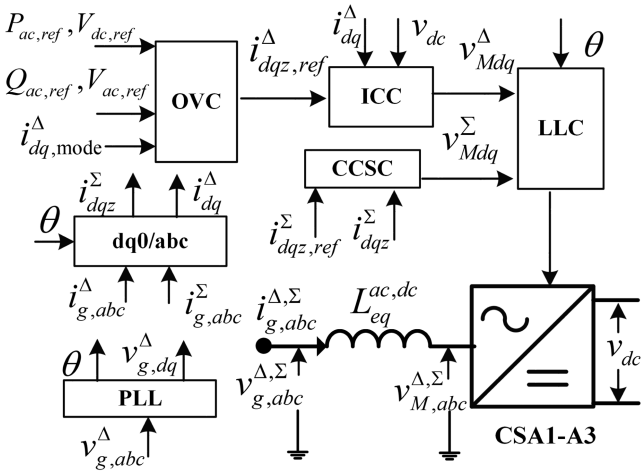

FIGURE 3. Generic block diagram representation of MMC converter control loops. The implementation of controlling loops and parameter values are given in [30].

IV. PROPOSED DC-FRT CONTROLLER

Fig. 4 illustrates the proposed DC-FRT control strategy. The proposed algorithm requires interconnection between converters for communication for the following reasons.

1) The fault identification and fault location algorithms, as implemented, require an exchange of currents and voltages from each terminal to perform the calculations.
2) Measurements of currents and voltages from each DC MMC's terminal are needed to calculate system matrices as described here.

Furthermore, the result of interconnection will simplify the algorithm calculation in real time.

The DC-FRT controller consists of the following four key elements:

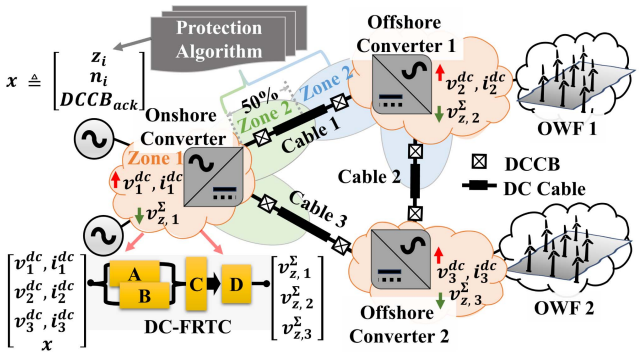

FIGURE 4. Proposed zone-based protection informed DC-FRT strategy, where A and B are prefault and fault suppression period reference generators, respectively. The C is an MPP and D is the dq frame CCSC.

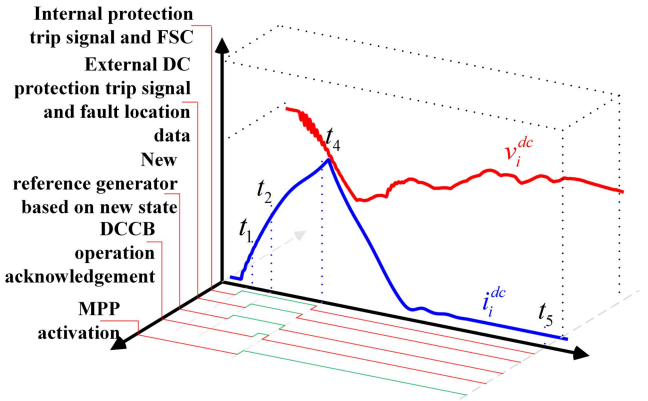

FIGURE 5. Graphical illustration of the proposed DC-FRT control.

1) **A**—Prefault reference generator;
2) **B**—Fault suppression period reference generator;
3) **C**—MPP;
4) **D**—Circulating current suppression control.

The primary function of **A** is to monitor current and voltage measurements from both local and interstation systems, providing a reference for **C**. Under normal conditions, the converter's current corresponds proportionally to the power injected or absorbed in the dc grid, maintaining an amplitude limitation for operational transients. Upon exceeding this boundary, indicating a fault, the reference generator in **A** freezes the last power (P_{ac} and Q_{ac}) set-point values. Consequently, **C** adjusts the converter currents back to the prefault conditions utilizing **D** for FSC. The role of **B** is to project a new steady state for the system after the fault. **B** calculates when the internal converter protection trip signal is set and dc protection information is communicated. The calculated value of **B** is applied to **C** when an acknowledged signal from the DCCB is available. To conclude, **C** takes as an input value provided either by **A** or **B** based on whether it is nominal behavior or the fault occurred, respectively.

Central to the DC-FRT control is **C**, which processes the information from the reference generator and dc protection to compute a controlled signal for **D**. The aim is to mitigate the fault impact and efficiently move the system to a new steady state. **D**, acting as a traditional CCSC, regulates the z-component of the summation current in the dqz frame based on references from **C**, with the output influencing the modulator. The detailed control strategy is outlined in algorithm 1 and visually represented in Fig. 5, illustrating the controller's sequential actions.

Note that Figs. 1 and 4 have the same operating stages. Namely, as described in Fig. 4, there are four parts of the algorithm: A and B solve the same matrices as represented in Section IV-A. Namely, for stage 1, Fig. 1(a), when everything operates nominally, then the reference is generated with A reference generator. In that case, the fault identification does not identify a fault, and thus, the fault location values n_i of (2) are zero, and the calculated voltages and currents correspond only to the terminal values. For stage 2, Fig. 1(b), the fault occurs. It is identified and interrupted. B is used as a reference generator with values n_i updates based on the fault location algorithm. For stage 3 in Fig. 1(c), the MPP is activated (part C in Fig. 4) and creates a new reference for D, i.e., circulating current suppression control. Finally, Fig. 1(d) depicts stabilization of the system with reference generator A, generated with new system connection (cable 1 disconnected).

Algorithm 1: Zone-Based Protection Informed DC-FRT Strategy.

INPUT: DC measurement point (v_i^{dc}, i_i^{dc}), fault zone (z_i), fault location (n_i), DCCB acknowledgement ($DCCB_{ack}$)
OUTPUT: Control actions and deblock signals
Detect fault by internal arm protection
Activate FCS via MPP with prefault reference generator (**A**)
while Acknowledgement of fault interruption not received from DCCB **do**
Wait for acknowledgment
if No acknowledgement received **then**
Block the converter
end if
end while
while Information on fault location and distance is updated from the protection algorithm **do**
Generate a new reference using the fault suppression period reference generator (**B**)
end while
Receive an acknowledgement signal from the DCCB
Apply the newly generated references from the reference generator **B** to the MPP

A. DC EQUIVALENT MTDC GRID AND REFERENCE GENERATOR

The reference generator, **A, B**, can be modeled as a simplified distributed system model. A simplified model of the distributed system is considered to reduce computation in real-time simulation as described in [31]. Considering the

three-terminal mesh grids and applying the KVL and KCL, we obtain the following:

$$\dot{\vec{V}}_{\mathrm{dc},f} = \boldsymbol{C}^{-1}\vec{I}_{\mathrm{dc},f} - \boldsymbol{C}^{-1}\boldsymbol{I_m}^{T}\vec{I}_{\mathrm{cable}} - \boldsymbol{C}^{-1}\boldsymbol{G}\vec{V}_{\mathrm{dc},f}$$
$$\dot{\vec{I}}_{\mathrm{dc},f} = \boldsymbol{L}^{-1}\boldsymbol{I_m}\vec{V}_{\mathrm{dc},f} - \boldsymbol{L}^{-1}\boldsymbol{R_l}\vec{I}_{\mathrm{cable}} \quad (1)$$

where $\vec{I}_{\mathrm{cable}} = [i^{1a}_{\mathrm{cable}},\ i^{2a}_{\mathrm{cable}},\ i^{3a}_{\mathrm{cable}},\ i^{1b}_{\mathrm{cable}},\ i^{2b}_{\mathrm{cable}},\ i^{3b}_{\mathrm{cable}}]^T$, $\vec{V}_{\mathrm{dc},f} = [v_1^{\mathrm{dc}},\ v_2^{\mathrm{dc}},\ v_3^{\mathrm{dc}},\ v_1^{f},\ v_2^{f},\ v_3^{f}]^T$, and $\vec{I}_{\mathrm{dc},f} = [i_1^{\mathrm{dc}},\ i_2^{\mathrm{dc}},\ i_3^{\mathrm{dc}},\ i_1^{f},\ i_2^{f},\ i_3^{f}]^T$. To provide fault information into the state-space representation of the MT-HVdc grid, a virtual node is set up, $v_i^f \forall i \in \{1, 2, 3\}$. Furthermore, i_i^{dc} and v_i^{dc} indicate converter current and voltage at i node. The distance between the virtual node and the actual node (v_i^{dc}) is determined by the fault location algorithm described in Section IV. This distance is defined by $n_i \in [0, 1]$. Considering the π model of cable, the diagonal matrix is derived as in (2), shown at the bottom of the page, where r_i, l_i, c_i, and g_i are total resistance, inductance, shunt capacitance, and shunt conductance, respectively, for cable. In this work, the mutual coupling between conductors is neglected for simplicity purposes.

The following case argument defines the incidence matrix:

$$\boldsymbol{I_m}(ix, n) = \begin{cases} 1, & \text{if } i^{ix}_{\mathrm{cable}} \text{ is flowing from node } n \\ -1, & \text{if } i^{ix}_{\mathrm{cable}} \text{ is flowing in node } n \end{cases}$$

where $n \in [1,\ 6]$ and $x \in \{a, b\}$. By applying the aforementioned case argument to the aforementioned MT-HVdc with the assumed current direction, we can formulate the following incidence matrix:

$$\boldsymbol{I_m} = \begin{bmatrix} \mathrm{diag}\{1\}_{3\times3} & \mathrm{diag}\{-1\}_{3\times3} \\ \begin{matrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{matrix} & \\ & \mathrm{diag}\{-1\}_{3\times3} \end{bmatrix}.$$

Rewriting (1), a state-space representation of MT-HVDC and derived in the following classical form: $\dot{\vec{x}}_{\mathrm{net}} = \boldsymbol{A}_{\mathrm{net}}\vec{x}_{\mathrm{net}} + \boldsymbol{C}_{\mathrm{net}}\vec{u}_{\mathrm{net}}$, $\vec{y}_{\mathrm{net}} = \boldsymbol{B}_{\mathrm{net}}\vec{x}_{\mathrm{net}} + \boldsymbol{D}_{\mathrm{net}}\vec{u}_{\mathrm{net}}$. The $\boldsymbol{A}_{\mathrm{net}}$, $\boldsymbol{B}_{\mathrm{net}}$, $\boldsymbol{C}_{\mathrm{net}}$, and $\boldsymbol{D}_{\mathrm{net}}$ matrices can be formulated using (1) and given by: $\boldsymbol{A}_{\mathrm{net}} = \begin{bmatrix} -\boldsymbol{C}^{-1}\boldsymbol{G} & -\boldsymbol{C}^{-1}\boldsymbol{I}_m^T \\ \boldsymbol{L}^{-1}\boldsymbol{I_m} & -\boldsymbol{L}^{-1}\boldsymbol{R_l} \end{bmatrix}$, $\boldsymbol{B}_{\mathrm{net}} = \begin{bmatrix} \boldsymbol{C}^{-1} \\ \boldsymbol{\emptyset} \end{bmatrix}$, $\boldsymbol{C}_{\mathrm{net}} = \boldsymbol{I}$, and $\boldsymbol{D}_{\mathrm{net}} = \boldsymbol{\emptyset}$, where $\emptyset$ indicates the empty matrix and $\boldsymbol{I}$ indicates the identity matrix. The state variables are $\vec{x}_{\mathrm{net}} = \begin{bmatrix} \vec{V}_{\mathrm{dc},f} & \vec{I}_{\mathrm{cable}} \end{bmatrix}^T$, and control vector is $\vec{u}_{\mathrm{net}} = \begin{bmatrix} \vec{I}_{\mathrm{dc},f} \end{bmatrix}$.

Considering the $v_{\mathrm{dc}} - Q$ operation mode of the converter at v_1^{dc} terminal, while the other converters operate in power mode, the first element of input vector $\vec{u}_{\mathrm{net}}$, can be written in terms of v_1^{dc}. Considering a steady-state condition, with converter dynamics described in [31], the state-space system equation can be written as $\dot{\vec{x}}_{\mathrm{sys}} = \boldsymbol{A}_{\mathrm{sys}}\vec{x}_{\mathrm{sys}} + \boldsymbol{B}_{\mathrm{sys}}\vec{u}_{\mathrm{sys}}$ and $\vec{y}_{\mathrm{sys}} = \boldsymbol{C}_{\mathrm{sys}}\vec{x}_{\mathrm{sys}}$, where $\vec{x}_{\mathrm{sys}} = \begin{bmatrix} \vec{x}_{\mathrm{net}} & i_{\mathrm{con}} & \alpha & \beta \end{bmatrix}^T$, $\vec{u}_{\mathrm{sys}} = [v_1^{\mathrm{dc}} \quad i_2^{\mathrm{dc}} \quad i_3^{\mathrm{dc}} \quad i_1^{f} \quad i_2^{f} \quad i_3^{f} \quad]^T$, and

$$\boldsymbol{A}_{\mathrm{sys}} = \begin{bmatrix} \boldsymbol{A}_{\mathrm{net}} & \boldsymbol{A_{12}} \\ \boldsymbol{A_{21}} & \boldsymbol{A_{22}} \end{bmatrix}, \boldsymbol{B}_{\mathrm{sys}} = \begin{bmatrix} \boldsymbol{B}_{\mathrm{net}} \\ \boldsymbol{B_{21}} \end{bmatrix}, \boldsymbol{C}_{\mathrm{sys}} = \boldsymbol{I},$$

$$\boldsymbol{A_{12}} = \begin{bmatrix} k_{\mathrm{con}} & 0 & 0 \\ 0 & 0 & 0 \\ \vdots & \vdots & \vdots \\ 0 & 0 & 0 \end{bmatrix}_{12\times3}, \boldsymbol{B_{21}} = \begin{bmatrix} k_{\mathrm{con}} & 0 & 0 \\ \frac{(k_{p1}k_{p2})}{L_{\mathrm{con}}} & 0 & 0 \\ k_{i2} & 0 & 0 \end{bmatrix}_{3\times3}$$

$$\boldsymbol{A_{21}} = \begin{bmatrix} \frac{-(k_{p1}k_{p2})}{L_{\mathrm{con}}} & 0 & \cdots & 0 \\ -k_{i1}k_{p2} & 0 & \cdots & 0 \\ -k_{i2} & 0 & \cdots & 0 \end{bmatrix}_{3\times12}$$

$$\boldsymbol{A_{22}} = \begin{bmatrix} \frac{-(R_{\mathrm{con}}+k_{p1})}{L_{\mathrm{con}}} & \frac{1}{L_{\mathrm{con}}} & \frac{k_{p1}}{L_{\mathrm{con}}} \\ -k_{i1} & 0 & k_{i1} \\ 0 & 0 & 0 \end{bmatrix}_{3\times3}.$$

The i_{con}, α, and β are current flowing in the inductance (L_{con}) and resistance (R_{con}) of the leakage transformer, and current and voltage controller state variables, receptively. The k_{p1} and k_{p2} are proportional gains of the inner and outer loops, respectively, and k_{i1} and k_{i2} are the integral gains of the inner and outer loops, respectively. The $k_{\mathrm{con}} = \frac{k}{C_{\mathrm{con}}}$, k is linearization factor and equivalent capacitor, $C_{\mathrm{con}} = \frac{6C_{\mathrm{sm}}}{N_{\mathrm{sm}}}$, where C_{sm} is capacitance of SMs and N_{sm} is number of SMs in the converter. The impact of the dc fault and other transients on the MMC switches is limited by the dc control. The current

$$\boldsymbol{R_l} = \mathrm{diag}\{n_1r_1,\ n_2r_2,\ n_3r_3,\ (1-n_1)r_1,\ (1-n_2)r_2,\ (1-n_3)r_3\}$$
$$\boldsymbol{L} = \mathrm{diag}\left\{n_1l_1,\ n_2l_2,\ n_3l_3,\ (1-n_1)\,l_1,\ (1-n_2)\,l_2,\ (1-n_3)\,l_3)\right\}$$
$$\boldsymbol{C} = \frac{1}{2}\,\mathrm{diag}\left\{\begin{bmatrix} n_1c_1 + (1-n_3)c_3 & 0 & 0 \\ 0 & n_2c_2 + (1-n_1)c_1 & 0 \\ 0 & 0 & n_3c_3 + (1-n_2)c_2 \end{bmatrix}, \begin{bmatrix} c_1 & 0 & 0 \\ 0 & c_2 & 0 \\ 0 & 0 & c_3 \end{bmatrix}\right\}$$
$$\boldsymbol{G} = \frac{1}{2}\,\mathrm{diag}\left\{\begin{bmatrix} n_1g_1 + (1-n_3)g_3 & 0 & 0 \\ 0 & n_2g_2 + (1-n_1)g_1 & 0 \\ 0 & 0 & n_3g_3 + (1-n_2)g_2 \end{bmatrix}, \begin{bmatrix} g_1 & 0 & 0 \\ 0 & g_2 & 0 \\ 0 & 0 & g_3 \end{bmatrix}\right\} \quad (2)$$

limiter saturation is incorporated in the current control which does not allow the current reference to go beyond a limit.

The prefault and fault suppression period reference generator (in Fig. 4 denoted as **A** and **B**, respectively) is defined by $\vec{x}_{\text{sys}}$ and $\vec{y}_{\text{sys}}$, and the corresponding fault distance and location. This set of equations is solved using the forward Euler numerical integration method to reduce the computational complexity in the real-time simulator. Furthermore, DCCB_{ack} determines the selection between the reference generators.

B. MODEL PREDICTIVE PLANNER (MPP)

An MPP is a model predictive control (MPC) [32] that provides an optimized reference path to the internal state of each converter based on the fault occurrence. As the name indicates, the system's behavior determines the MPC's prediction and accuracy. The mathematical model of the network is represented by the state-space model and is rewritten in an augmented matrix discrete form for $\vec{x}_m(k) = \begin{bmatrix}\Delta\vec{x}_{\text{net}}(k) & \vec{y}_{\text{net}}(k)\end{bmatrix}^T$ as

$$\begin{aligned}\vec{x}_m(k+1) &= \begin{bmatrix}\mathbf{F}(T_s) & o^T\\ \mathbf{F}(T_s) & 1\end{bmatrix}\vec{x}_m(k) + \begin{bmatrix}\mathbf{G}(T_s)\\ \mathbf{G}(T_s)\end{bmatrix}\Delta\vec{u}(k)\\ \vec{y}_m(k) &= \begin{bmatrix}0 & \mathbf{I}\end{bmatrix}\vec{x}_m(k)\end{aligned} \tag{3}$$

where $k \in \mathbb{N}$ indicates discrete time step, whereas $\mathbf{F}(T_s) = e^{\mathbf{A_{net}}\,T_s}$ and $\mathbf{G}(T_s) = \mathbf{A_{net}}^{-1}(e^{\mathbf{A_{net}}\,T_s} - \mathbf{I})\,\mathbf{B_{net}}$. The future control sequence, $\Delta\vec{u} \in [-1, 1]^3 \subset \mathbb{R}^3$, which is determined by solving the optimal control problem and minimizing the objective (cost) function, such that the change in network energy remains low at any given time, which is then subjected to the equality and inequality constraints

$$\begin{aligned}\min_{\Delta\vec{u}} J = &\sum_{j=1}^{N_p-1} \|\vec{x}_m(k+j|k)\|^2_{\mathbf{Q}} + \left\|\Delta\vec{u}\right\|^2_{\mathbf{R}} + I_d e(k)\\ &+ \left\|\vec{x}_m(k+N_p|k)\right\|^2_{\mathbf{Q_{LQR}}}\\ &\text{subject to } \mathbf{M}\Delta\vec{u} \le \vec{b}\\ \vec{x}_m(k+j|k) &= \vec{r}(k) - \vec{y}_m(k|k)\end{aligned} \tag{4}$$

where **Q** and **R** are given in (5), shown at the bottom of the following page. Here, $l_i \in \{0.25, 0.5, 1\}$ and $z_i \in \{0.25, 0.5, 1\}$ are the arbitrary weighting factor that indicates the priority and control afford depending upon fault location and zone (see Appendix). Q_{LQR} is a weighing factor calculated using an implicit solver for discrete-time Riccati equations. The $N_p = 20 \in \mathbb{I}^+$ is the prediction horizon. For variables $\vec{x}_m(k)$, vector $r(k) \in \mathbb{R}^6$ is a reference signal provided by the reference generator. The Matrix **M** and the column vector $\vec{b}$ are related to the control rate and amplitude constraint information. In reality, there will be an error due to the modeling or the signal noise. However, these disturbances can be considered in the optimal control problem, represented by $e(k)$. $e(k)$ denotes the error between the system's measured signal and the plant's predicted signal at kth instance. $I_d \succ 0$ is the weight matrix.

V. FAULT IDENTIFICATION AND LOCATION ALGORITHM

In the presence of a fault, the proposed control architecture uses fault distance, n_i to define the cable parameters, $\boldsymbol{R_l}$, $\boldsymbol{L}$, $\boldsymbol{C}$, and $\boldsymbol{G}$ [see (2)]. The calculated distance is also used for the weight selection criteria in MPC. The weight coefficients of the quadratic stage cost are defined with zones of fault location (see Appendix). Therefore, it is essential to know the instant of the fault occurrence, its behavior, and its location.

A. FAULT IDENTIFICATION

The externally placed current limiting reactors (CLRs) (shown in Fig. 6) are series inductors put to limit the rate of rise of dc fault current. They act as impeccable fault differentiators, accumulating much energy upon a fault's inception. If the voltages across them at the positive and negative poles are measured in real-time and compared to a threshold, U_{oset} (specific to the system configuration and rating), then the occurrence of a fault is determined almost instantaneously [33]

$$\begin{cases}|v^{\text{dc}}_{1p}(t) - v^{\text{CLR}}_{1p}(t)| = |u_{1p}(t)| & \text{(6a)}\\ |v^{\text{dc}}_{1n}(t) - v^{\text{CLR}}_{1n}(t)| = |u_{1n}(t)| & \text{(6b)}\end{cases}$$

1) pole-to-pole (PTP) fault: Both (6a) and (6b) violate threshold, U_{oset};
2) positive pole-to-ground (P-PTG) fault: Only (6a) violates threshold, U_{oset};
3) negative pole-to-ground (N-PTG) fault: Only (6b) violates threshold, U_{oset}.

B. FAULT LOCATION

The subsection explains the time-domain-based evaluation of fault distance for a PTP fault between terminals 1 and 2 (see Fig. 4). Here, $v_1^{dc}(t)$ and $v_2^{dc}(t)$ are the terminal dc bus voltages, $i^{1a}_{cable}(t)$ and $i^{1b}_{cable}(t)$ are the currents from terminals 1 and 2, respectively. In contrast, $v_1^{CLR}(t)$ and $v_2^{CLR}(t)$ are the voltages after CLRs, L_{m1} and L_{m2}. $v_1^f(t)$ is defined as the voltage across the fault resistance, whereas n_1 is defined as the percentage fault location for cable 1 with unit length. Using simplified R-L representation, r_1 is the resistance per unit length, whereas l_1 is the inductance per unit length of cable 1. For a PTP fault, the following equations are obtained by applying the KVL from terminals 1 and 2:

$$2r_1 n_1 i^{1a}_{\text{cable}}(t) + 2l_1 x_1 \frac{di^{1a}_{\text{cable}}(t)}{dt} + v_1^f = v_1^{\text{CLR}}(t) \tag{7}$$

$$2r_1(1-n_1) i^{1b}_{\text{cable}}(t) + 2l_1(1-n_1) \frac{di^{1b}_{\text{cable}}(t)}{dt} + v_1^f = v_2^{\text{CLR}}(t). \tag{8}$$

The current derivative terms can be obtained using the voltage drop across the CLR, avoiding additional WGN due to differential calculations. These terms are

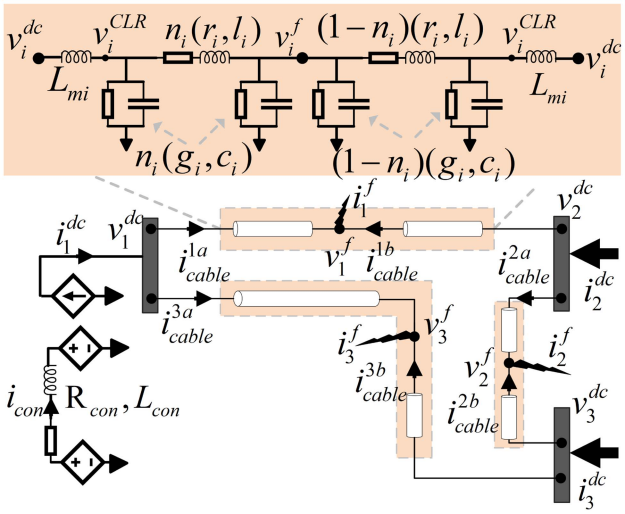

FIGURE 6. Simplified model of a test network with a π cable model and a simplified converter model connected to node v_1^{dc}.

$\frac{di_{\text{cable}}^{1a}(t)}{dt} = \frac{v_1^{\text{dc}}(t)-v_1^{\text{CLR}}(t)}{2L_{m1}} = \frac{u_1(t)}{2L_{m1}}$; $\frac{di_{\text{cable}}^{1b}(t)}{dt} = \frac{v_2^{dc}(t)-v_2^{\text{CLR}}(t)}{2L_{m2}} = \frac{u_2(t)}{2L_{m2}}$. Subtracting (8) and (9) negates the fault location dependence on fault resistance. Furthermore, substituting and rearranging them give n_1 as

$$n_1 = \frac{\left[v_1^{\text{CLR}}(t) - v_2^{\text{CLR}}(t)\right] + 2r_1 i_{\text{cable}}^{1b}(t) + \frac{l_1}{L_{m2}}u_2(t)}{2r_1\left[i_{\text{cable}}^{1a}(t) + i_{\text{cable}}^{1b}(t)\right] + \frac{l_1 u_1(t)}{L_{m1}} + \frac{l_1 u_2(t)}{L_{m2}}}. \quad (9)$$

Similar expressions can be derived for n_2, $n_3 \ldots n_i$ [34]. For a solidly grounded system, the computation of the fault location for PTG faults is the same as for PTP faults. For cases with grounding resistors, the expression of fault location contains different grounding resistors at the two faulty terminals. For $f_s = 20$ kHz (a comparatively low sampling frequency), the fault location window is 1–2 ms from the inception time. This makes the method's maximum detection and location time to be less than 2 ms [33], [34]. The implemented time-domain fault location reduces the computation burden. It complements the nature of MPC, which uses an optimized reference path to the internal state of each converter based on the fault location information.

VI. TEST MESH OFFSHORE MMC-BASED MT-HVDC GRID

A three-terminal bipolar metallic return MMC-HVdc network is used to test the proposed control strategies, utilizing the real-time digital simulator (RTDS) simulator. The system parameters and operating mode are detailed in Table 2, with the setup inspired by [30].

TABLE 2. Control Mode and Parameter of the Test HVDC System

Parameter	Converters		
	CSA 1	CSA2	CSA3
Active power [MW]	2000	2000	2000
Control mode	Vdc-Vac	Vac-f	Vac-f
Reactive power [MVAR]	-	-	-
Number of SMs per arm	240	200	200
MMC arm inductance [mH]	25	49.7	49.7
Transformer leakage reactance [pu]	0.18	0.15	0.15
AC Point of couple voltage [kV]	400	220	220
DC link Voltage [kV]		±525	
Rated power [MVA]		2000	
Capacitor energy in a SM [MJ]		30	
MMC arm resistance [Ω]		0.544	
Rated voltage/current of each SM [kV/kA]		2.5/2	
AC converter bus voltage [kV]		275	
Wind farm AC Point of couple voltage [kV]		66	

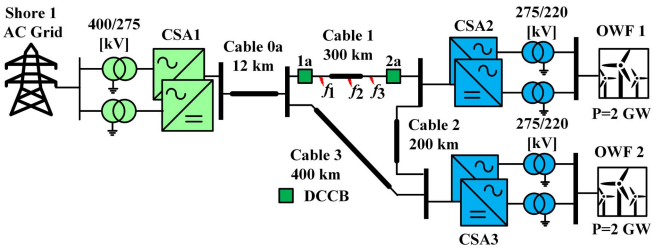

FIGURE 7. Test HVdc system is a ±525-kV bipolar DMR topology with two wind farms.

The HVdc test system is designed as a ±525-kV bipolar with a dedicated metallic return (DMR) topology as illustrated in Fig. 7. The network comprises three MMC-based converter units using HB SM, implemented as described in Section III: CSA1 (onshore converter connected to a strong ac grid), CSA2, and CSA3 (offshore converters), where CS denotes the converter station. The MMC's valve and lower level control in the converter station are implemented using five GTFPGAs (two per terminal), as depicted in Fig. 8, where it is visible that three FPGAs are used for MMC's legs and two for lower level controls (capacitor voltage balancing and SM firing pulses generation). Offshore converters are linked to aggregate type-4 wind farms via scaled-up transformers, each turbine having a 2-MW capacity at 16-m/s wind speed.

The system includes a mix of land and submarine DMR cables: a 12-km land cable (Cable 0a) connecting the onshore hub with a VSC assisted resonant current (VARC) HVdc breaker and six submarine cables of varying lengths (cable 1 at 300 km, cable 2 at 200 km, and cable 3 at 400 km).

$$\boldsymbol{Q} = \text{diag}\left\{\begin{bmatrix} l_1 r_1 & 0 & 0 \\ 0 & l_2 r_2 & 0 \\ 0 & 0 & l_3 r_3 \end{bmatrix}, 0.1\boldsymbol{I}_{3\times 3}, \begin{bmatrix} l_1 c_1 & 0 & 0 \\ 0 & l_2 c_2 & 0 \\ 0 & 0 & l_3 c_3 \end{bmatrix}, 0.1\boldsymbol{I}_{3\times 3}\right\}, \quad \boldsymbol{R} = \text{diag}\left\{\begin{bmatrix} z_1 r_1 & 0 & 0 \\ 0 & z_2 r_2 & 0 \\ 0 & 0 & z_3 r_3 \end{bmatrix}, 0.1\boldsymbol{I}_{3\times 3}\right\} \quad (5)$$

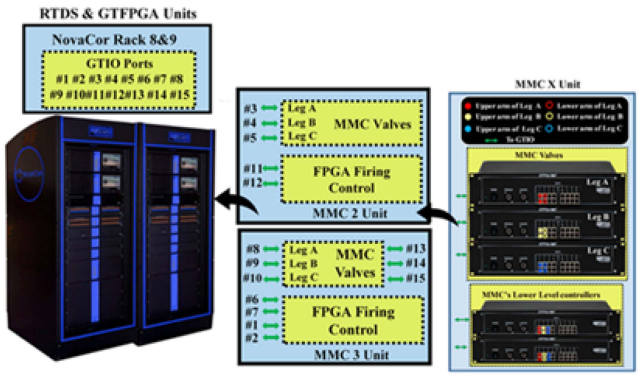

FIGURE 8. MMC implementation using RTDS GTFPGA.

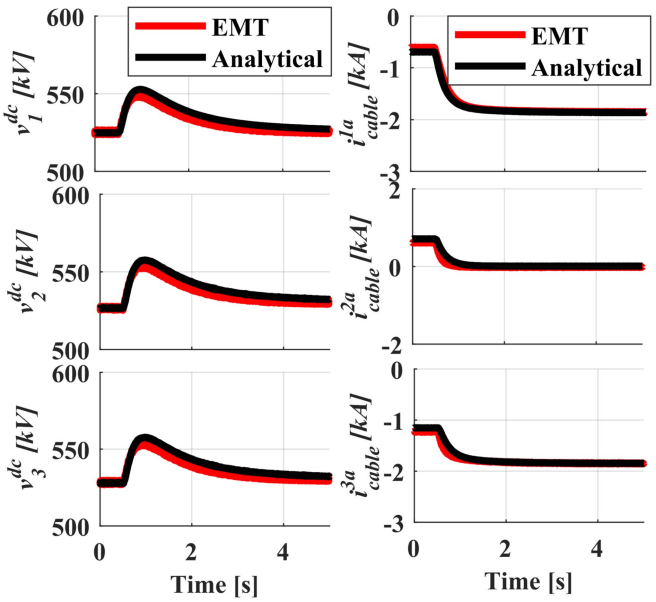

FIGURE 9. Comparison of EMT dc grid and dc-side equivalent circuit model under wind power changed from 100 to 2000 MW, obtained using RTDS-based hardware-in-the-loop setup.

This test includes a standard type-4 wind turbine control [35]. The DC-FRT control is implemented on a separate RTDS NovaCor chassis, simulating an external controller's role in the setup. This setup provides a comprehensive environment to validate and refine various DC-FRT strategies, ensuring robust and efficient performance of the HVdc system under test conditions.

VII. SIMULATION RESULTS

A. VALIDATION OF DC-SIDE EQUIVALENT CIRCUIT

To anticipate the dc grid's behavior accurately, the analytical model employed in the MPP must exhibit precise performance under steady-state conditions and during significant disturbances. Fig. 9 illustrates the performance of the analytical model derived from ordinary differential (4), validated against detailed electromagnetic transient (EMT) simulations during a wind power variation from 100 to 2000 MW. The analytical model, implemented through C-builder [36] with a time step of 3μs, successfully captures the system's dynamics. Notably, the wind power alteration initiates at 0.5 s, leading to a change in the dc cable currents according to the new power flow in the dc grid. The analytical model exhibits high conformity with the EMT models across various phases—before, during, and after the disturbance. This alignment underscores the analytical model's performance in predicting the dynamic behavior of the dc grid, establishing its credibility for advanced control law design.

B. DC CABLE FAULT

Figs. 10–12 illustrate the performance of cable 1 for a PTP fault at the beginning of cable 1, in the middle of cable 1, and at the end of cable 1, both with and without integrating a proposed controller. Without the controller, the terminal voltages and currents exhibit a dominant frequency oscillation of 100 Hz after the fault clearance by DCCBs. This persistent oscillation lasts for more than 100 ms, as evident in Figs. 10–12(a)–(f), here the plots show the voltage and current profiles of different converters. The recovery process is expedited by introducing a fast-acting DCCB. Similar can be achieved following the method outlined in [17], where converters are blocked, and an ac breaker, necessitating dc grid reenergization, accomplishes fault clearance.

Upon fault removal by the DCCB, a substantial current oscillation occurs with a reversal at offshore converters, resulting in a higher rate of rise of converter current during the interruption period. This places stress on the DCCB at the terminal's end, observed through the elevated energy stored in DCCB surge arresters, detailed in Table 3.

The implementation of the DC-FRT control yields a notable improvement. With the proposed method, a higher voltage transient is achieved, resulting in a lower current transient and faster settling time to reach a steady state for the voltage and current profiles. In addition, the dominant frequency oscillations for the voltage and current are effectively suppressed. Upon triggering the internal converter protection, FSC activates at 1.0015 s. This activation prompts a reference change at CCSC via MPP, as depicted in Figs. 10–12(j)–(l). The primary goal of this reference adjustment is to minimize the converter current rate, subsequently reducing the rate of rise of the fault current, as shown in Figs. 10–12(h). The regulation of the dc-link voltage at each converter terminal achieves this control, as illustrated in Figs. 10–12(a)–(c).

Simultaneously, as FSC is activated, the protection algorithm calculates fault distance and issues a trip command to the DCCBs, as seen in Figs. 10–12(m). The computed distance and location information are relayed to the reference generator (**B**) and MPP. Following successful fault interruption by the DCCB, a confirmation signal triggers the changes in the weight matrices in MPC, leading to the use of a new reference (**B**). Consequently, the converter current follows a nonoscillatory optimal trajectory, exhibiting a faster settling time than scenarios without a controller, as shown in Table 3.

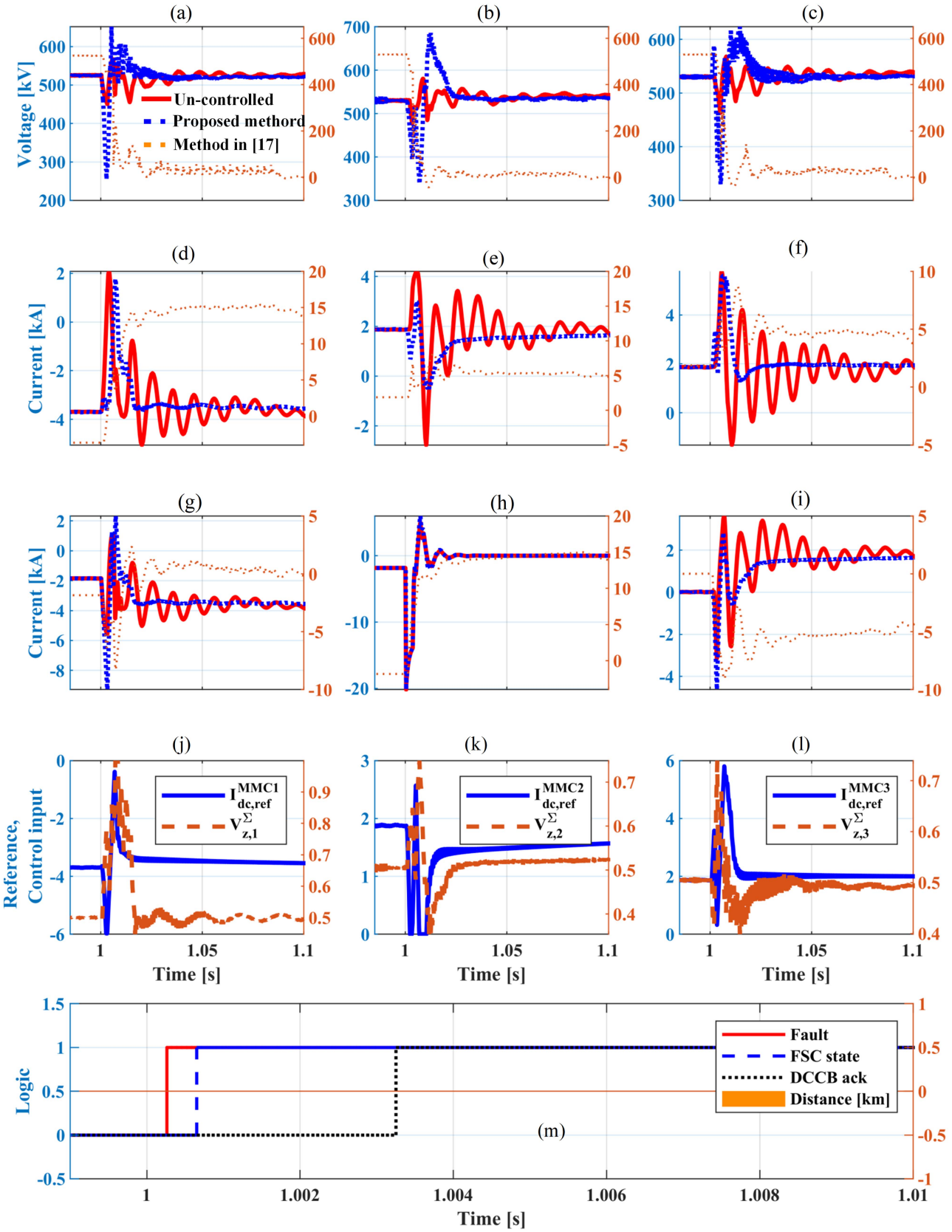

FIGURE 10. PTP fault with a fault resistance of 0.01 Ω at the beginning of the cable 1, i.e., 0% cable length, obtained using RTDS-based hardware-in-the-loop setup. (a)–(c) and (d)–(f) Converter voltages and currents. (j)–(l) Reference currents generated by the MPP and corresponding control actions. (m) Internal and external protection actions.

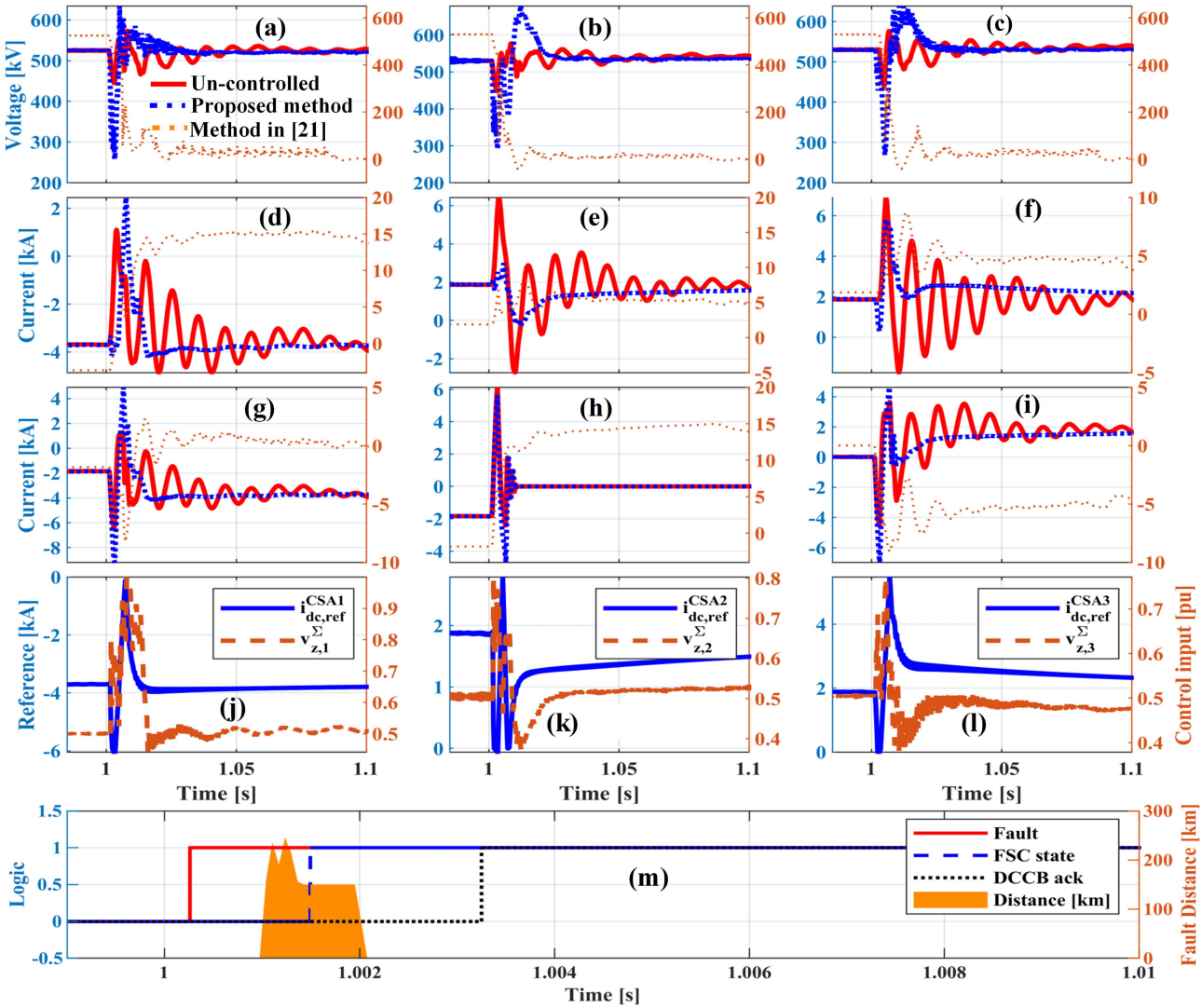

FIGURE 11. PTP fault with fault resistance of 0.01 Ω at the middle of the cable 1, obtained using RTDS-based hardware-in-the-loop setup. (a)–(c) and (d)–(f) Converter voltages and currents. (j)–(l) Reference currents generated by MPP and corresponding control actions. (m) Internal and external protection actions.

Moreover, the MPP enforces control amplitude constraints of [-6 kA, +6 kA] on the onshore converter and [0 kA, 6 kA] on the offshore converter. All converters maintain a controlled rate amplitude of 0.2 kA/ms, preventing offshore converters from experiencing current reversal. Despite observing overvoltage during the recovery process, it remains within the acceptable limit of the cable overvoltage profile [37], [38]. During FSC activation, a significant current amplitude is noted, attributed to the redirection of energy from the faulty segment, resulting in lower energy absorption in the DCCB and safeguarding its energy absorption element, as highlighted in Table 3.

Similarly, for a PTP fault at the dc terminal of converters CSA1 and CSA2, the DC-FRT control provides a damped and controlled response. The early activation of FSC, as shown in Figs. 10 and 12(m) is observed for PTP faults at the dc terminal of converters CSA1 and CSA2.

C. DIFFERENT DC-FRT CONTROL SCHEME

Three distinct schemes, as depicted in Fig. 13, have been scrutinized to assess the impact of communication delay (τ) on system performance, as illustrated in Fig. 14. DC-FRT control discussed in the previous section shows no communication delay in receiving intrastation measurement signals and external protection signals denoted as scheme 1. However, real-world conditions introduce a communication delay, set at 200 ms/km in this study [7].

In response to this delay, two additional schemes have been proposed. Scheme 2 involves a centralized configuration with communication delays affecting both input and output signals, while Scheme 3 employs a decentralized approach with delays specifically on external signals.

In Scheme 1, the DC-FRT control is centrally located, receiving converter voltages and currents from stations 400-km away, resulting in a 2-ms delay. This delay extends to

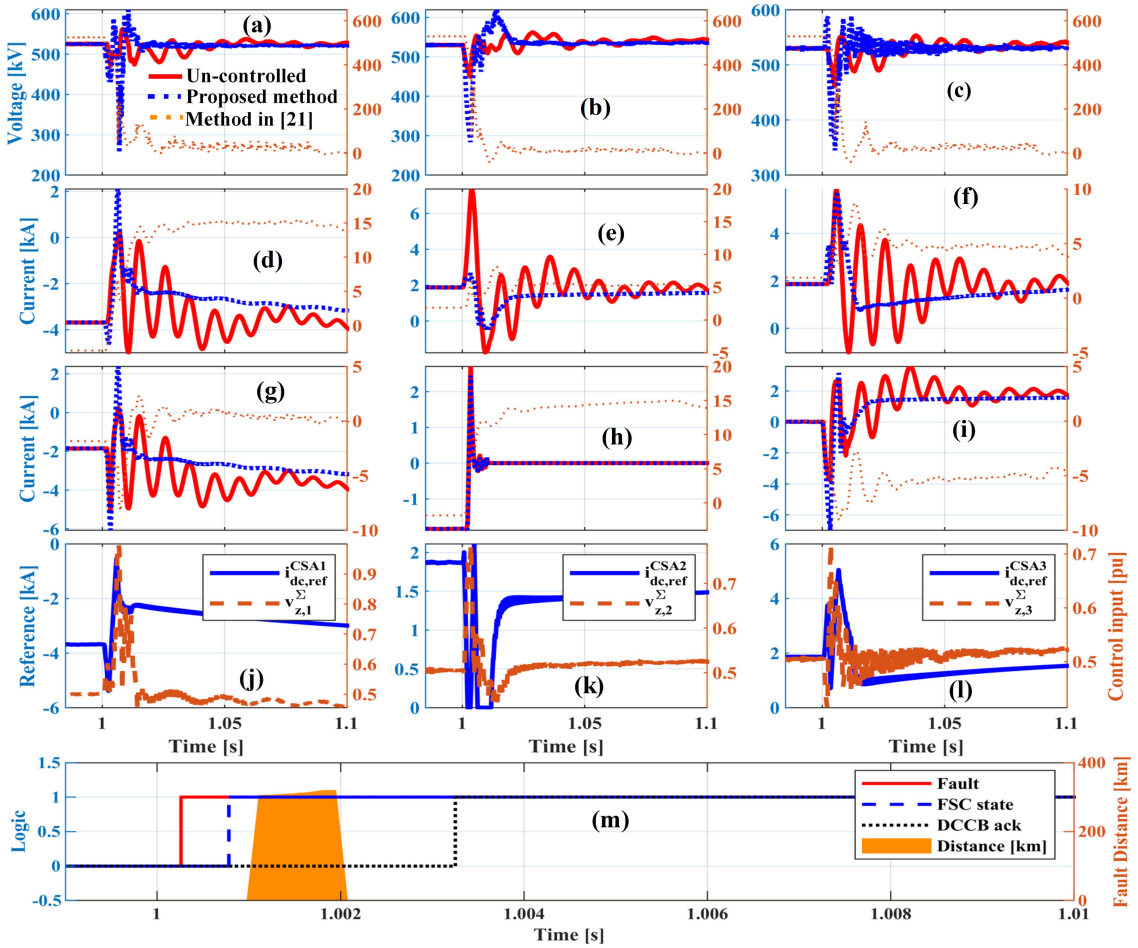

FIGURE 12. PTP fault with 0.01-Ω fault resistance near CSA2 terminal, i.e., 100% cable length, obtained using RTDS-based hardware-in-the-loop setup. (a)–(c) and (d)–(f) Converter voltages and currents. (j)–(l) Reference currents generated by MPP and corresponding control actions. (m) Internal and external protection actions.

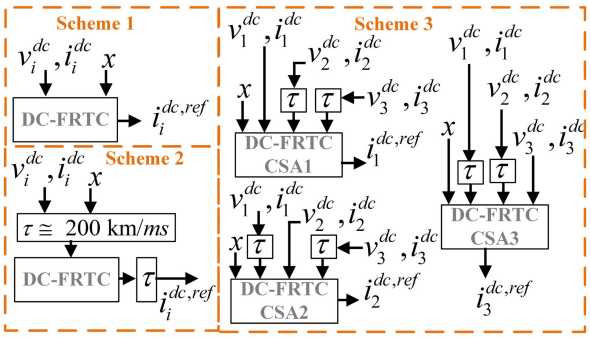

FIGURE 13. Different DC-FRT control schemes.

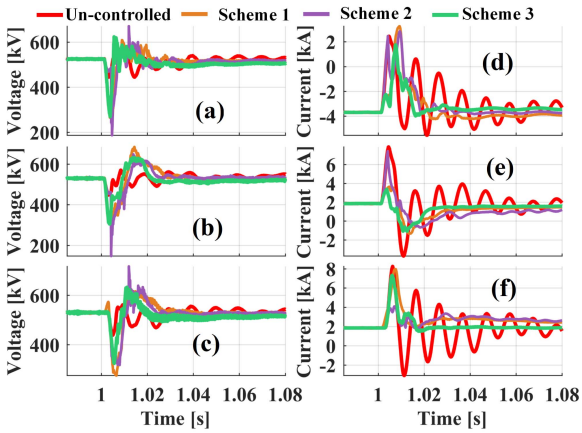

FIGURE 14. DC fault recovery for different Schemes, obtained using the RTDS-based hardware-in-the-loop setup.

information provided by the dc protection algorithm. Consequently, a delayed response by the controller is depicted in Fig. 14. During the initial 2-ms delay, all converters follow an uncontrolled trajectory. However, upon data reception, the MPP algorithm implements corrective measures, regulating converter currents and restoring the system to its optimal course. Despite the introduced delay, Scheme 1 exhibits a robust response compared to an uncontrolled system.

Scheme 2 represents a scenario where DC-FRT control is embedded at each converter station, receiving measurements from other converters with delays corresponding to the interstation distances. By leveraging local measurements, DC-FRT control can swiftly react to internal protection events,

TABLE 3. Comparison Between With and Without DC-FRT Controller During Pole-to-Pole Fault

PP-0-cable1	Converter Current	Dominated frequency [Hz]	$\frac{di}{dt}$ at t= 1.004 s [kA/ms]	Settling Time [ms]	Peak value [kA]	Energy absorbed in DCCB 1a [MJ]	Energy absorbed in DCCB 1b [MJ]
Without DCFRT	i_1^{dc}	100	0.407	118	3.697		
	i_2^{dc}	100	0.525	145	4.198	5.87	9.69
	i_3^{dc}	100	0.337	133	5.77		
With DCFRT	i_1^{dc}	-	0.133	15	3.627		
	i_2^{dc}	-	0.111	12	2.975	3.5	7.708
	i_3^{dc}	-	0.005	15	5.615		

PP-50-cable1	Converter Current	Dominated frequency [Hz]	$\frac{di}{dt}$ at t= 1.004 s [kA/ms]	Settling Time [ms]	Peak value [kA]	Energy absorbed in DCCB 1a [MJ]	Energy absorbed in DCCB 1b [MJ]
Without DCFRT	i_1^{dc}	100	0.650	118	4.467		
	i_2^{dc}	100	1.133	144	6.359	3.3	11.69
	i_3^{dc}	100	0.294	164	6.86		
With DCFRT	i_1^{dc}	-	0.038	16	4.859		
	i_2^{dc}	-	0.071	15	2.930	2.27	7.90
	i_3^{dc}	-	0.001	20	5.800		

PP-100-cable1	Converter Current	Dominated frequency [Hz]	$\frac{di}{dt}$ at t= 1.004 s [kA/ms]	Settling Time [ms]	Peak value [kA]	Energy absorbed in DCCB 1a [MJ]	Energy absorbed in DCCB 1b [MJ]
Without DCFRT	i_1^{dc}	100	0.545	118	4.984		
	i_2^{dc}	100	1.372	145	7.365	1.47	15.06
	i_3^{dc}	100	0.337	165	5.873		
With DCFRT	i_1^{dc}	-	0.190	16	4.626		
	i_2^{dc}	-	0.111	12	2.585	1.16	10.39
	i_3^{dc}	-	0.067	10	5.665		

activating the FSC. The DC-FRT control, based on historical measurements and protection information, provides a trajectory for each converter, facilitating a rapid system recovery, as illustrated in Fig. 14. Moreover, this scheme furnishes a backup control signal for converters in the dc grid, ensuring an N-1 contingency. This feature proves pivotal in multivendor scenarios, enhancing the overall system reliability.

VIII. CONCLUSION

This article proposed a protection zone-informed predictive DC-FRT controller. The simulation results highlight that the modified dc-side equivalent circuit model can accurately represent the MTDC grid's dynamics, especially during wind power ramping, and validate its utility for advanced control algorithms. The key findings of this article include the following.

1) A 3-μs time-step MT-HVdc grid analytical model in the C-builder of RSCAD/RTDS closely matches the real-time simulation model, confirming its credibility for control law formulation. Please note that the RSCAD is the specialized software for configuring and running simulations on the RTDS simulator hardware.
2) DC-FRT control enhances system stability under PTP faults by damping dominating frequency oscillations in dc-side voltage and current, facilitating faster guided recovery.
3) DC-FRT control effectively reduces the stress on the DCCBs by suppressing converter current peaks and improves system reliability.
4) Different DC-FRT control schemes, both centralized and decentralized, demonstrate resilience against interstation communication delays, proving the controller's adaptability and fidelity.

APPENDIX
WEIGHT SELECTION CRITERIA IN MPC

The weight coefficients of the quadratic stage cost are given by Algorithm 2. The influence of the regions on the weight coefficients is depicted in Fig. 15.

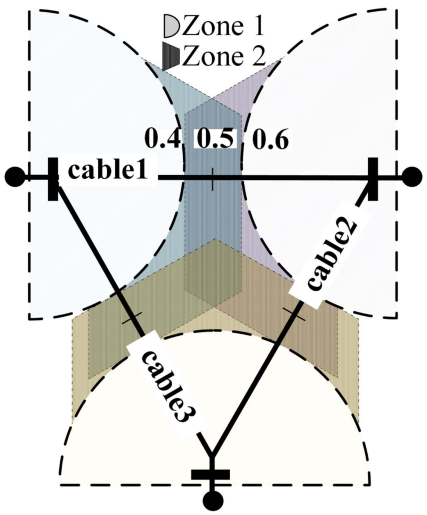

FIGURE 15. Illustration of control zones around three cables, indicating the varying influence regions for the weight coefficients in the quadratic stage cost function.

Algorithm 2: Algorithm for Weight Coefficients of the Quadratic Stage Cost.

Require: cable$_i$, $n_i | i \in \{1, 2, 3\}$
Ensure: z_i, $l_i | i \in \{1, 2, 3\}$
Initialize z_i, $l_i = 0.25$ for all $i \in \{1, 2, 3\}$
for $i \in \{1, 2, 3\}$ **do**
  if cable$_i$ == 1 **then**
    if $n_i < 0.4$ **then**
      $z_i = 1, l_i = 1, l_{(i \bmod 3)+1} = 0.5$
    else if $0.4 \leq n_i \leq 0.6$ **then**
      $z_i = 0.5, z_{(i \bmod 3)+1} = 0.5, l_i = 1,$
      $l_{(i \bmod 3)+1} = 0.5, l_{((i+1) \bmod 3)+1} = 0.5$
    else
      $z_{(i \bmod 3)+1} = 1, l_i = 1, l_{(i \bmod 3)+1} = 0.5$
    end if
  end if
end for

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