A Low-Voltage Ultra-Low-Power Translinear Integrator for Audio Filter Applications

Wouter A. Serdijn, Martijn Broest, Jan Mulder, Albert C. van der Woerd, and Arthur H. M. van Roermund

***Abstract*—In this paper, the design and measurement of a 1-V translinear integrator and its application in a controllable second-order lowpass filter for hearing instruments is presented. A semicustom version of the filter has been integrated in a standard 2-μm, 7-GHz, bipolar IC process and operates at voltages down to 1 V, consumes only 6 μA, and has a dynamic range of 57 dB for a total harmonic distortion below 2%. Its cutoff frequency is linearly adjustable in octaves from 1.6 to 8 kHz.**

***Index Terms*—Active filters, bipolar analog integrated circuits, current mode, low power, low voltage.**

I. Introduction

ELECTRONIC filters are important building blocks in electronic systems when it comes to the separation of desired signals from other signals and noise by making use of differences in their energy-frequency spectra. Especially in a low-voltage environment, the limited dynamic range of these active circuits is a problem. See, e.g., [1]. If also a (frequency) controllable transfer function is required and resistor values become too large for integration, which is the penalty for going to lower and lower currents, the situation becomes even more complicated [2]. It is the quest for a controllable transfer function that produced the idea of "log-domain filtering," first introduced by Adams in 1979 [3] and later thoroughly investigated by Seevinck [4], Frey, see, e.g., [5], Punzenberger and Enz [6], Toumazou and Lande [7], Perry and Roberts [8] and Mulder *et al.* [9], [10].

In this paper, a systematic approach to the design of a 1-V, "ultra-low-power," i.e., resistorless, translinear integrator, which can be considered to be a basic building block of log-domain filters, is presented. In the next section, attention is paid to the key idea behind the translinear integrator. Section III deals with its implementation in a low-voltage environment. As a design example, Section IV presents a controllable second-order lowpass filter for hearing instruments, of which the measurements are given in Section V.

II. Current Companding

The starting point of our discussion is the block diagram of a companding integrator, as mentioned by Seevinck in [4]; see Fig. 1. This integrator can be considered to be an implementation of a first-order linear differential equation $x(t) = dy(t)/dt$ by applying the chain-rule

$$x(t) = \frac{dy(t)}{dt} = \frac{dy(t)}{dv(t)} \cdot \frac{dv(t)}{dt} \tag{1}$$

with $v(t)$ being some internal quantity. Note that this differential equation is completely independent of $v(t)$. Moreover, if $y(t) = F(v(t))$ and F is an expanding function, the variation of v for a given variation of x will be less than for a linear F.

Since the only integratable integrating element is a capacitor, of which the output signal is a voltage, in practice, the internal quantity v will be a voltage. An expanding F will thus result in a reduced voltage swing across the capacitor, which is beneficial in a low-voltage environment.

Low-voltage ultra-low-power analog integrated circuits for preference operate in the current domain, i.e., use current as the information-carrying quantity as much as possible [11]. For this reason, current is the natural choice for the other quantities, i.e., x, y, dv/dt, and dy/dv.

From this perspective, translinear circuits are the natural choice for implementing the divider function, the expanding function F, and its derivative dF/dv.

A very convenient implementation of both F and dF/dv is the exponential relation between the base-emitter voltage V_{BE} and the collector current of a single bipolar transistor. MOS transistors, biased in weak inversion and driven at the gate and/or the back-gate (bulk) terminal [12], or even "compound transistors" [8], [13] may be valuable alternatives. Assuming a bipolar transistor, it follows that

$$y = F(v) = I_S \exp(V_{BE}/V_T) \tag{2}$$

and

$$dF/dv = \frac{I_S}{V_T} \exp(V_{BE}/V_T) = \frac{y}{V_T} \tag{3}$$

with I_S and V_T being the saturation current and the thermal voltage kT/q, respectively.

The translinear divider will, basically, consist of four transistors in a translinear loop that implements the function $I_{\text{in}} \cdot I_O = I_{\text{out}} \cdot C dv/dt$, with I_{in}, I_{out} and Cdv/dt being the input current (x), the output current (y), and the capacitor current (dv/dt), respectively, according to Fig. 1. I_O is a normalizing constant current. Some calculation yields for the input–output relation of this translinear integrator

$$I_{\text{out}} = \frac{I_O}{V_T C} \int I_{\text{in}} dt. \tag{4}$$

From this expression, it can be deduced that the time constant of the integrator thus can be electronically controlled by means of current I_O.

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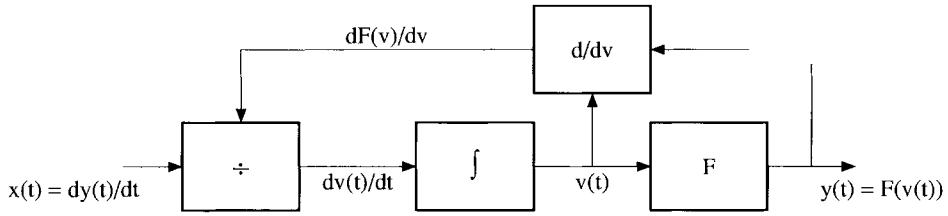

Fig. 1. General block diagram of a companding integrator.

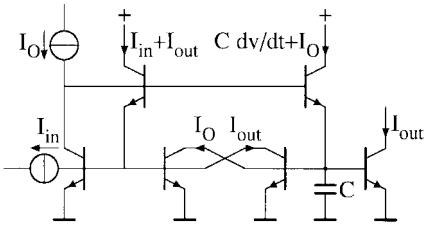

Fig. 2. Compact translinear integrator by Seevinck.

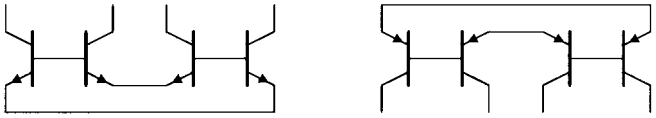

Fig. 3. Four transistors in a translinear loop in "up–down topology."

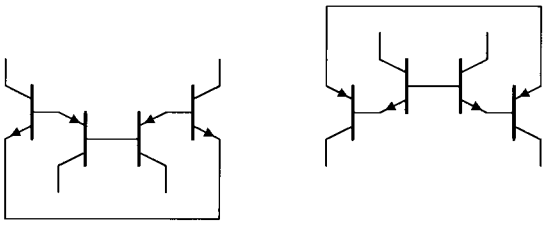

Fig. 4. Four transistors in a translinear loop in "alternating topology."

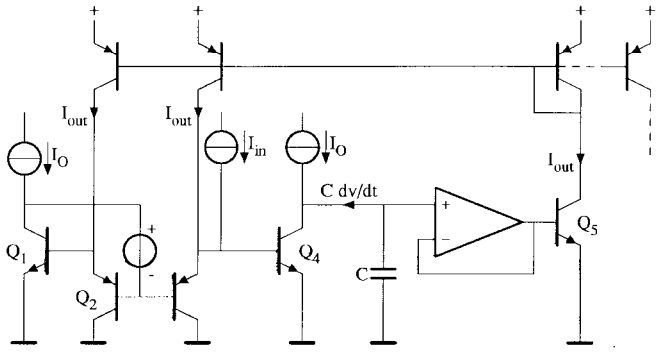

Fig. 5. Signal path of the 1-V translinear integrator with an ideal floating voltage source and an ideal voltage follower.

III. The Low-Voltage Translinear Integrator

A possible, very compact embodiment of a translinear integrator is presented in [4]; see Fig. 2. Although this circuit contains only six n-p-n transistors, thus indicating its potential to operate up to high frequencies, it also suffers from some major drawbacks.

First, the integrator dc gain A_{dc} is a function of the current gain factor β_F of the output transistors and the ratio I_O/I_{in}

$$A_{dc} = \frac{dI_{\text{out}}}{dI_{\text{in}}} \approx \frac{\beta_F}{\sqrt{8\beta_F \frac{I_{\text{in}}}{I_O} + 16}}. \tag{5}$$

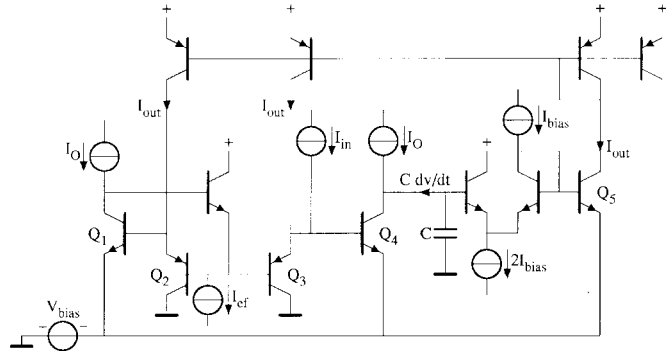

Fig. 6. The complete signal path of the 1-V translinear integrator.

TABLE I
Filter Requirements

Quantity	Value	Comment
supply voltage	1.1—1.6 V	
bandwidth	100 Hz—8 kHz	−3 dB
cutoff frequency	1.6 kHz—8 kHz	linearly adjustable in octaves
dynamic range	$>$ 56 dB	THD $<$ 2%
total (integrated) capacitance:	$<$ 200 pF	

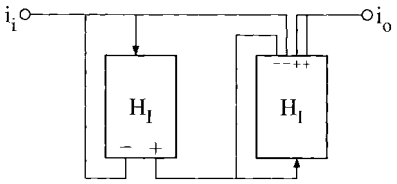

Fig. 7. Second-order lowpass leapfrog filter operating in the current domain, consisting of two integrators (H_I).

We see that the dc gain is small for small values of β_F and nonlinear for variations of the input current I_{in}.

Second, the circuit's output capability, i.e., the maximum output current that the circuit can deliver, equals I_O, which is also used to control the integrator's time constant. Since the maximal signal-to-noise ratio the circuit can handle is roughly proportional to the square-root of the supply current, this results in either an unnecessarily increased current consumption or chip area, or a deteriorated dynamic range.

Third, and finally, because of the two base-emitter voltages connected in series between the two supply rails, this integrator is not able to operate at very low supply voltages. Note that the 1-V constraint also results in giving up the combination of the divider and the output transistors in one circuit.

The first disadvantage can be overcome by connecting a voltage follower in series with the input of the output transistors. Overcoming the other disadvantages implies the use of a different translinear divider.

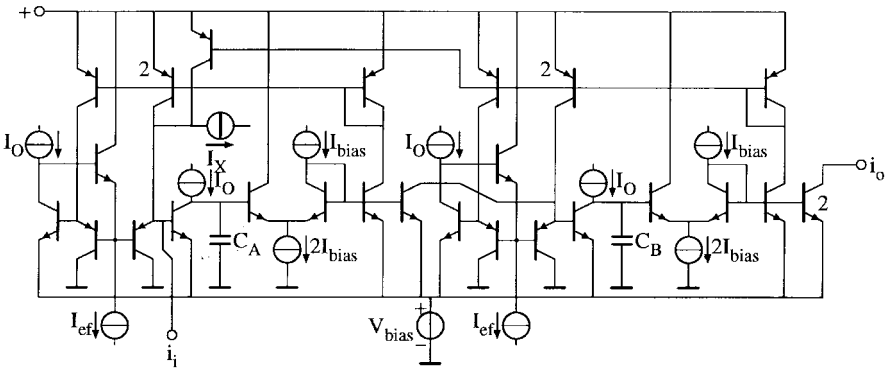

Fig. 8. Circuit diagram of the second-order lowpass filter.

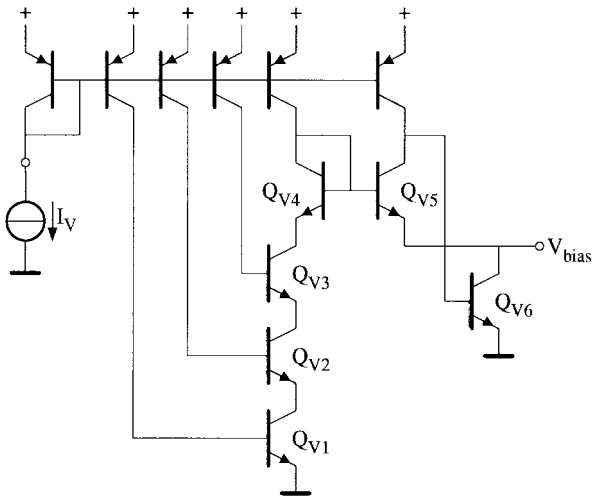

Fig. 9. Realization of the voltage source $V_{\rm bias}$. The output voltage is independent of the value of I_V.

For a 1-V translinear divider there are two possibilities. Either the four transistors can be connected in "up–down topology," i.e., every base is connected to another base and every emitter is connected to another emitter, or the four transistors can be connected in "alternating topology," i.e., the base of a transistor is connected to another base of the same type of transistor or to an emitter of a transistor of the opposite type. Both possibilities are depicted in Figs. 3 and 4.

Of the 16 possible ways to implement the divider in a 1-V translinear integrator—there are two possible topologies, two transistor types, and four ways to connect the four divider currents $I_{\rm in}$, $I_{\rm out}$, Cdv/dt and I_O—we choose the one that is single-ended,[1] requires only one additional floating voltage source, is symmetrically biased and—according to simulations, using realistic transistor models—has a satisfying high-frequency behavior. The resulting circuit diagram, including the above-mentioned voltage follower, is depicted in Fig. 5. The floating voltage source prevents transistor Q_1 from saturating. The PNP current mirror with two outputs delivers the two output currents with the correct sign to the divider. It can be seen that I_O no longer determines the maximum signal current the integrator can handle. These currents are determined in the complete filter structure, as described in Section IV.

[1]This circuit is also known as the log-antilog multiplier [14].

A. The Voltage Follower

A suitable implementation of the voltage follower is an ordinary differential pair of which the positive output and the negative input have been connected to each other.

To be able to drive the output transistor Q_5 (and possible additional parallel-connected output transistors), the collector bias currents, $I_{\rm bias}$, of the differential pair should be larger than the maximum base current of the output transistor(s). However, the base currents of the differential pair should be smaller than the collector current of Q_4, I_O. A very convenient value is the geometric mean of these two boundaries which equals the geometric mean of the collector bias currents of Q_4 and Q_5. Hence

$$I_{\rm bias} = \sqrt{I_O B_F \cdot \frac{I_{C,Q_5}}{B_F}} = \sqrt{I_O \cdot I_{C,Q_5}} \tag{6}$$

where I_{C,Q_5} and B_F are the collector bias current of Q_5 and the transistor current gain factor, respectively.

B. Integrator Biasing

A suitable embodiment of the floating voltage source, which additionally reduces the influence of base currents in the divider, is an ordinary emitter follower. Again, for the value of its biasing current, $I_{\rm ef}$, the geometric mean of I_O and I_{C,Q_5} is a suitable value. To create some room for the bias source of this emitter follower and for the tail-current source of the voltage follower, an additional voltage source, $V_{\rm bias}$, has been connected in series with the emitters of Q_1, Q_4, and Q_5. Note that the absolute value of this voltage source is not important since it does not appear in the translinear loop of the divider; 200 mV is a convenient value. The circuit diagram of the complete 1-V translinear integrator is depicted in Fig. 6.

IV. A Design Example: A Controllable Second-Order Lowpass Filter for Hearing Instruments

Subsequently, the translinear integrator is adopted for the design of a second-order lowpass Butterworth filter for hearing instruments. Table I shows the requirements which have to be fulfilled in this filter.

Starting point is the second-order lowpass leapfrog filter as depicted in Fig. 7. This filter operates in the current domain and consists of two integrators. The input–output relation H_F

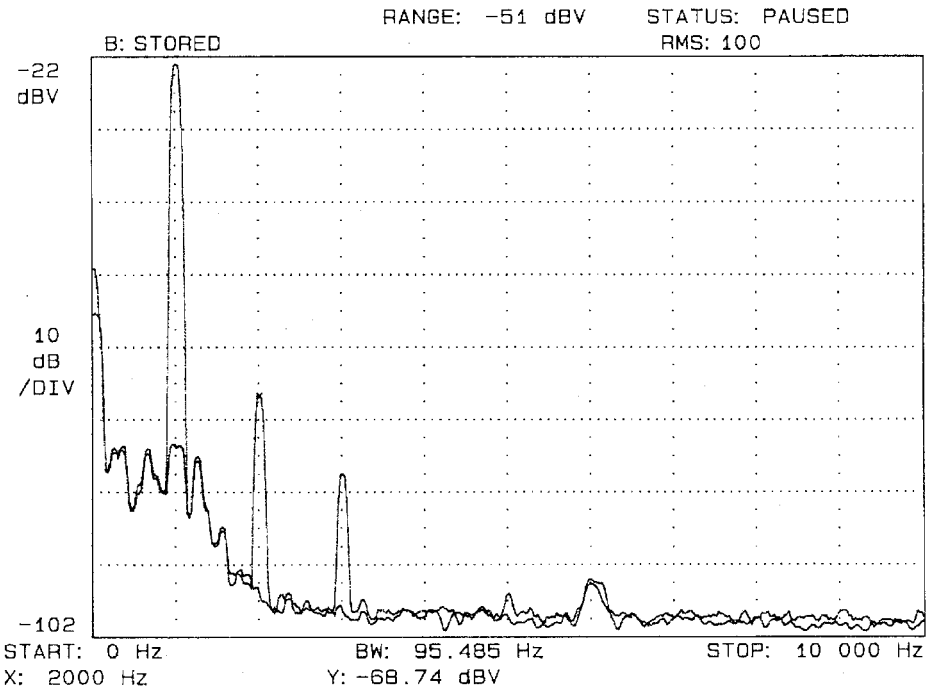

Fig. 10. Measured output frequency spectrum with and without a 1-kHz, 70-nA (peak value) sinewave input signal. The cutoff frequency and supply voltage equal 8 kHz and 1.3 V, respectively.

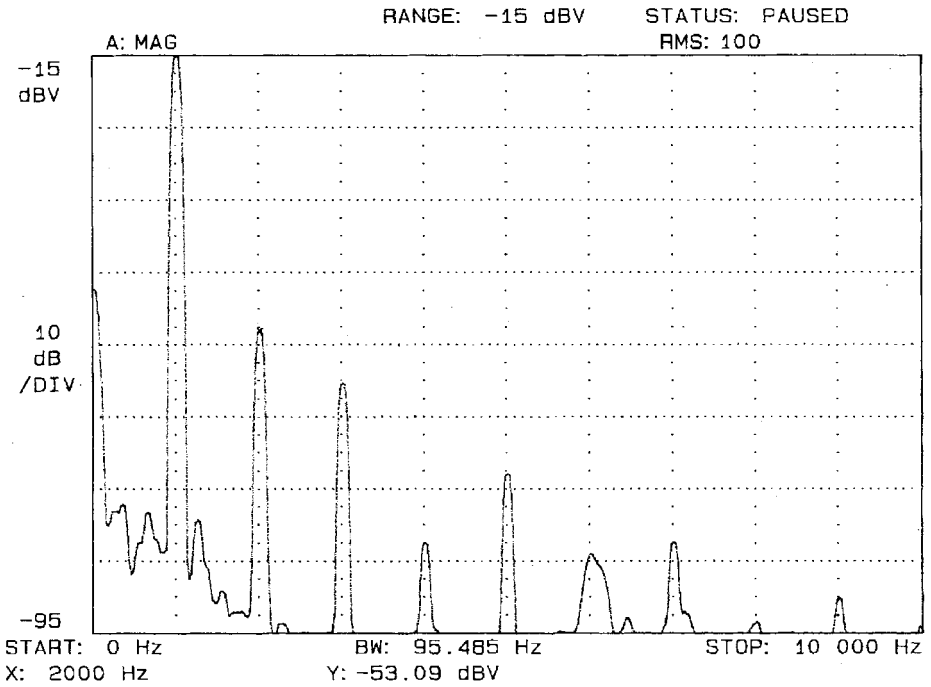

Fig. 11. Measured output frequency spectrum for a 1-kHz, 220-nA (peak value) sinewave input signal. The cutoff frequency and supply voltage equal 8 kHz and 1.3 V, respectively.

of the filter is given by

$$H_F = \frac{i_o}{i_i} = \frac{2H_I^2}{1+2H_I+2H_I^2} \tag{7}$$

with H_I being the transfer function of the integrator. With $H_I = I_O/j2\pi CV_T$, this yields a Butterworth lowpass filter with cutoff frequency $f_c = I_O/\pi\sqrt{2}V_T C$. Its circuit diagram is depicted in Fig. 8.

Only one bias current source, I_X, is necessary to ensure the correct biasing of the complete filter. Its value determines the maximum signal current the filter can handle and its dynamic range. Since the circuit is biased in class A, the noise sources inside the circuit can be considered to be almost independent of the signal levels inside the filter. To estimate the dynamic range of the filter, the major noise sources inside the filter, i.e., the collector shot noise sources, are shifted to the output. Then, the

TABLE II
FILTER SPECIFICATIONS

Quantity	Value	Comment
supply voltage	down to 1 V	
bandwidth	0—80 kHz	
passband transfer	+1.6 dB	
stopband attenuation	30 dB	
cutoff frequency:	1.6 kHz—8 kHz	linearly adjustable in octaves
maximum signal current	220 nA (peak value)	THD $<$ 2%, from 100 Hz to 8 kHz
dynamic range	57 dB	THD $<$ 2%, from 100 Hz to 8 kHz
supply current	6 μA	
PSRR	$>$ 120 dBΩ	from 100 Hz to 8 kHz
total (integrated) capacitance	100 pF	

equivalent output noise power density spectrum is integrated over the total frequency range (from 100 Hz to 8 kHz) and compared to the maximum signal power. For sinusoidal signals, with $I_X = 400$ nA, $I_{\text{bias}} = 80$ nA, $V_{\text{bias}} = 200$ mV, $I_{\text{in,max}} = 180$ nA (peak value), $C_A = C_B = 50$ pF, $T = 308$ K (35°C) and $I_O = 47$ nA ($f_c = 8$ kHz), this yields a dynamic range of 59 dB. This value has been confirmed by simulations. With respect to the 56-dB dynamic-range requirement, this means for the embodiment of the bias sources that they are not permitted to produce more noise than the signal path of the complete filter. Even in low-voltage applications, this requirement is easily met [16].

V. SEMICUSTOM REALIZATION AND MEASUREMENTS

The control current I_O has been realized by a porportional-to-absolute temperature (PTAT) current source with a scaled indirect output [2]. The scaled output is generated by a controllable voltage source in series with the emitter of the output transistor. This results in the desired exponential relation between the control quantity and the cutoff frequency of the filter.

All the other biasing currents were derived from two scaled current mirrors with indirect outputs. The embodiment of the voltage source V_{bias} was inspired by the one used in [17] and adapted for our purpose. Its circuit diagram is depicted in Fig. 9. Three saturated transistors, Q_{V1}, Q_{V2}, and Q_{V3}, generate a PTAT voltage of approximately 200 mV. Q_{V4}, Q_{V5}, and Q_{V6} are connected in voltage-follower configuration, to generate a low-impedance version of this voltage. A p-n-p current mirror with multiple outputs delivers the necessary bias currents. Note that, since, in general, a saturation voltage is a function of the ratio of the collector and the base current [16], the output voltage V_{bias} does not depend on the value of I_V. Also, noise originating from I_V does not penetrate into V_{bias}. For $I_V = 0.5\mu$A, the noise production of the voltage source itself appears to be sufficiently small.

A semicustom version of the active circuitry of the complete filter has been integrated in a standard 2-μm, 7-GHz process, fabricated at the Delft Institute of Microelectronics and Submicron Technology. Typical transistor parameters are $h_{\text{fe,NPN}} \approx 100$, $f_{T,\text{NPN}} \approx 7$ GHz, $h_{\text{fe,LPNP}} \approx 80$, and $f_{T,\text{LPNP}} \approx 40$ MHz. Experiments proved the correct operation of the filter. The filter characteristic is second-order Butterworth with the specifications shown in Table II.

Fig. 10 depicts the measured output frequency spectrum with and without a 1-kHz, 70-nA (peak value) sinewave input signal. The cutoff frequency and supply voltage equal 8 kHz and 1.3 V, respectively. The plot clearly indicates that, since the integrator is biased in class A, the output noise is not a function of the integrator input signal level.

Fig. 11 depicts the measured output frequency spectrum for a 1-kHz, 220-nA (peak value) sinewave input signal using the same settings. The total harmonic distortion (THD) mainly results from the second-order harmonic and equals 1.3%. Over the complete frequency range, i.e., from 100 Hz to 8 kHz, the THD remains below 2%.

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