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***Abstract*— The CMOS technology scaling faced over the past recent decades severe variability and reliability challenges. One of the major reliability challenges is bias temperature instability (BTI). This paper analyzes the impact of BTI on the sensing delay of standard latch-type sense amplifier (SA), which is one of the critical components of high performance memories; the analysis is done by incorporating the impact of process, voltage, and temperature variations (in order to investigate the severity of the integral impact) and by considering different workloads and four technology nodes (i.e., 45, 32, 22, and 16 nm). The results show the importance of taking the SA degradation into consideration for robust memory design; the SA degradation depends on the application and technology node, and the sensing delay can increase with 184.58% for the worst case conditions at 16 nm. The results also show that the BTI impact for nominal conditions at 16 nm reaches a 12.10% delay increment. On top of that, when extrinsic conditions are considered, the degradation can reach up to 168.45% at 398 K for 16 nm.**

***Index Terms*— Bias temperature instability (BTI), negative BTI (NBTI), positive BTI (PBTI), process variations, static RAM (SRAM) sense amplifier (SA).**

I. Introduction

TECHNOLOGY scaling poses major reliability challenges due to both intrinsic and extrinsic variations.

The variability of intrinsic device parameters are worsening in each CMOS technology generation; this is the result of unavoidable imperfections during fabrication and the introduction of new materials [1]. In addition, extrinsic variations in V_{dd} and temperature are consequences of changing operational and environmental conditions and also impact the transistors. On top of them, the intrinsic degradation of the devices causes major reliability challenges [2]–[4]. Bias temperature instability (BTI) [i.e., negative BTI (NBTI) in pMOS transistors and positive BTI (PBTI) in nMOS transistors] is a major reliability failure mechanism that affects the performance of MOS transistors by increasing their threshold voltage and reducing their drain current (I_d) over the operational lifetime [5], [9]. Hence, it impacts the robustness of both logic (such as CPUs) and memory [such as static RAM (SRAM)] circuits. Hence, analyzing the integral impact of all of these variables is needed in order to quantify the impact and degradation appropriate for the design for reliability solutions.

SRAM occupies a large fraction of semiconductor chip and plays a major role in the silicon area, performance, and critical robustness [10]. An SRAM system consists of an array of cells, its peripheral circuits such as row and column address decoders, control circuits, write drivers, and sense amplifiers (SAs).

Designing an optimal reliable memory system requires a deep understanding of the way it degrades in order to provide appropriate design-for-reliability schemes.

Many publications analyzed the BTI impact on SRAM cell array, while very limited work is published on the SRAM peripheral circuitry. Cheng and Brown [11] investigated the NBTI impact on static noise margin (SNM) and write noise margin degradation of the 6T SRAM cell. Kumar *et al.* [12] analyzed the impact of NBTI on the read stability and SNM of SRAM cells. Carlson [13] investigated the mechanism of NBTI degradation on SRAM metrics such as SNM. Kang *et al.* [14] studied the estimation of statistical variation in temporal NBTI degradation and its impact on lifetime circuit performance. Weckx *et al.* [15] analyzed the implications of BTI-induced time-dependent statistics on yield estimation of digital circuits. Bansal *et al.* [16] presented insights into the stability of an SRAM cell under the worst case conditions and analyzed the effect of NBTI and PBTI, individually and collectively. Rodopoulos *et al.* [17] investigated the atomistic pseudotransient BTI simulation with built-in workloads. Wang *et al.* [18] investigated the statistical reliability analysis of NBTI impact on FinFET SRAMs and mitigation technique using independent gate devices. Khan *et al.* [19] investigated the BTI analysis of FinFET-based SRAM cell.

On the other hand, few authors have focused on reliability analysis of the SRAM peripheral circuit. Khan *et al.* [20] investigated the impact of partial opens and BTI on an SRAM address decoder.

In addition to that, Menchaca and Mahmoodi [21] analyzed the BTI impact on different SA designs implemented on a 32-nm technology node using failure probability (i.e., flipping a wrong value) as a reliability metric. Agbo *et al.* [22]–[25] investigated the BTI impact on the SRAM drain-input latch-type SA design implemented on 90, 65, and 45 nm for different

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supply voltages using sensing delay and sensing voltage as reliability metrics. Agbo *et al.* [26] investigated a comparative BTI impact for SRAM cell and SA designs, while considering different applications and using swing delay and sensing delay as evaluation metrics.

The above statement clearly shows that most of the works focused on the SRAM cell. In addition, incorporating both variability and reliability are not explored very well. It is worth noting that understanding and quantifying the aging rate of each memory part/component is needed for an optimal reliable memory design; this is because the different parts may degrade with different rates depending on the workload (application).

This paper analyzes the degradation of the SA, a critical component of a memory especially for high-performance applications. This paper focuses on the standard latch-type SA design due to its superior performance [27] and analyzes process, voltage, and temperature (PVT) variations in combination with BTI for different workloads and technology nodes. The main contributions of this paper are as follows:

1) investigation of the BTI impact on the SA's sensing delay using eight realistic workloads;
2) thorough quantitative analysis of the BTI impact on the SA for four technology nodes, i.e., 45, 32, 22, and 16 nm;
3) investigation of the BTI impact on different workloads for different technology nodes;
4) different supply voltage impact analyses on SRAM SA sensing delay for different workloads;
5) investigation of different temperature impacts on SA for various technology nodes;
6) analysis of the integral impact of BTI and process variation on SA's sensing delay.

The rest of this paper is organized as follows. Section II introduces the functional model of SRAM system, the standard latch-type SA, the BTI mechanism and its model, and the variations targeted in this paper. Section III provides our analysis framework and analysis metric, and it also presents the performed experiments. Section IV reports, analyzes, and discusses the results. Finally, Section V concludes this paper.

II. Background

This section presents the electrical model of the SA considered in this paper.

Subsequently, it presents the BTI mechanism and its model. Finally, it models the process and environmental variations considered in this paper.

A. SRAM Sense Amplifier

Several implementations of SAs have been proposed. In this paper, the standard latch-type SRAM strobed SA will be addressed, which is representative of industrial SA designs [27].

The structure of such an SA is depicted in Fig. 1. The width/length ratio of each transistor is presented by W/L. The operation of the SA consists of two phases. In the first phase, when SAenable is low, the access transistors *Mpass* and *MpassBar* connect to the *BL*(*BLBar*) with the internal

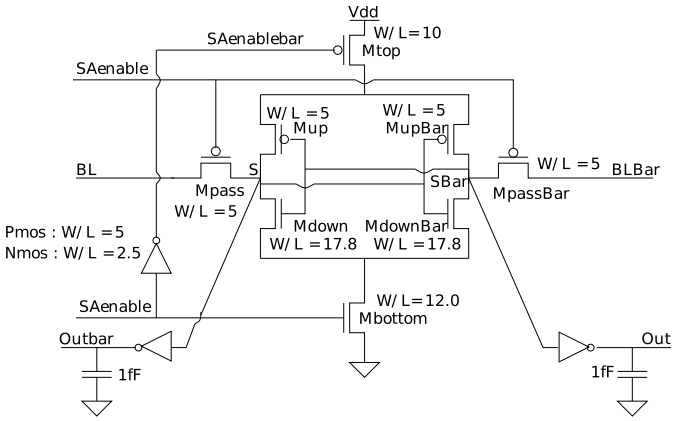

Fig. 1. Standard latch-type SA.

nodes *S*(*SBar*). In this phase, *Mtop* and *Mbottom* transistors are switched OFF. In the second phase, when SAenable is high, the pass transistors (i.e., *Mpass* and *MpassBar*) disconnect the *BL* and *BLBar* inputs from the internal nodes. The cross-coupled inverters get their current from Mtop and Mbottom and subsequently amplify the difference between *S* and *SBar* and produce digital outputs on *out* and *outbar*. The *S*(*SBar*) node is actively pulled down when *SBar*(*S*) exceeds the threshold voltage of Mdown. The positive feedback loop ensures low amplification time and produces the read value at its output. Moreover, all current paths are disabled when *S*(*SBar*) is at 0 V and *SBar*(*S*) is at V_{dd} or vice versa. This process is repeated for each read operation.

B. Bias Temperature Instability

The BTI mechanism takes place inside MOS transistors and causes a threshold voltage shift that negatively impacts the delay; its mechanism is described in the following section.

1) BTI Mechanism: BTI increases the absolute V_{th} value in MOS transistors. For pMOS, NBTI reduces the V_{th}, while for nMOS, PBTI increases the V_{th}.

Recently, exhaustive efforts have been put to understand NBTI [5], [9], [29]. Alam and Mahapatra [5] have modeled NBTI and presented the overall dynamics of NBTI as a reaction diffusion (RD) process. Nevertheless, this model seems to fail to explain the BTI degradation in the recovery phase [28]. Kaczer *et al.* [29] have analyzed NBTI using an atomistic model. The difference between the RD model and atomistic model is that the latter is based on the calibrations and its stochastic nature, while RD is based on deterministic nature. In [30], both the atomistic and RD models have been studied and compared. The results revealed that RD and atomistic models show similar trends. When only long-term reliability effects (across years) need to be studied, then the RD model is more suitable than the atomistic model because of its lightweight nature. In the context of this paper, this is our focus, so we opted for the RD model published in [5]. The model has two BTI phases, i.e., the stress phase and the relaxation phase.

Stress phase: In the stress phase, the silicon hydrogen bonds (≡Si–H) break at the silicon–oxide interface. The broken silicon bonds (≡Si−) remain at the interface (known as

interface traps) and the released H atoms/molecules diffuse toward the gate oxide. The number of interface traps ($N_{\rm IT}$) generated after applying a stress of time (t) is given by [5]

$$N_{IT}(t) = \left(\frac{N_o \cdot k_f \cdot E_{\rm ox}}{k_r}\right)^{2/3} \cdot \left(\frac{k_H}{k_{H_2}}\right)^{1/3} \cdot (6 \cdot D_0 \cdot t)^{1/6} \quad (1)$$

where N_o, k_f, k_r, k_H, and k_{H_2} represent the initial ≡Si–H density, ≡Si–H breaking rate, ≡Si− recovery rate, H to H_2 conversion rate, and H_2 to H conversion rate inside the oxide layer, respectively, while $E_{\rm ox} = (V_{\rm gs} - V_{\rm th})/T_{\rm ox}$ is the electric field across the gate oxide, which causes the breaking of silicon hydrogen bond at the interface, which is associated with k_f [6]–[8]. D_0=$D_{H_2} \cdot \exp(-E_A/kT)$ [31] is the diffusion coefficient of the produced H_2 species and E_A is the activation energy, k is the Boltzmann constant, and T is the temperature in Kelvin.

Relaxation phase: In the relaxation phase, there is no ≡Si–H breaking. However, the H atoms/molecules diffuse back toward the interface and anneal the ≡Si− bonds. The number of interface traps that *do not* anneal by the approaching H atoms during the relaxation phase is given by [12]

$$N_{IT}(t_o + t_r) = \frac{N_{IT}(t_o)}{1 + \sqrt{\frac{\xi \cdot t_r}{t_o + t_r}}} \quad (2)$$

where $N_{IT}(t_o)$ is the number of interface traps at the start of the relaxation, ξ is a relaxation coefficient with $\xi = 0.5$ [32], t_o is the duration of the previous stress phase, and t_r is the relaxation duration.

Threshold voltage increment: $N_{\rm IT}$ opposes the gate voltage, which results in a threshold voltage increment ($\Delta V_{\rm th}$). The relation between $N_{\rm IT}$ and $\Delta V_{\rm th}$ is given by [33]

$$\Delta V_{\rm th} = (1 + m) \cdot q \cdot N_{IT} / C_{\rm ox} \cdot \chi \quad (3)$$

where m, q, and $C_{\rm ox}$ are the holes/mobility degradation that contributes to the $V_{\rm th}$ increment [34], electron charge, and oxide capacitance, respectively. χ is a BTI coefficient with a value $\chi = 1$ for NBTI and $\chi = 0.5$ for PBTI [32]. CMOS technology scaling results in an apparent oxide field increment and this speeds up the covalent bond breaking phenomenon of BTI impact. Therefore, it is essential to evaluate the reliability of these technologies.

Delay increment: BTI-induced $\Delta V_{\rm th}$ of each individual MOS transistor has its contribution to the additional delay. A generalized first-order equation that relates BTI-induced $\Delta V_{\rm th}$ in a transistor to dataline/output signal delay is given by [33], [35]

$$\Delta D = \frac{n \cdot \Delta V_{\rm th}}{(V_{\rm gs} - V_{\rm th})} \quad (4)$$

where n is the velocity saturation index of majority carriers in MOS channels. Since NBTI causes $\Delta V_{\rm th}$ to the pMOS transistor and PBTI causes $\Delta V_{\rm th}$ to the nMOS transistor, this paper considers the threshold voltage shifts for both types of MOS transistors.

C. Variations

Variability has caused significant drifts from the predicted specification for a chip. These can be classified into intrinsic process, extrinsic environmental, and aging variations. Each is described next.

D. Process Variations

Process variation is an important concern for the SRAM SA's sensing delay [36] and caused by the imperfect circuit manufacturing process. They affect several transistor parameters including the effective channel length ($L_{\rm eff}$), oxide thickness ($t_{\rm ox}$), dopant concentration (N_a), and transistor width (w). There are two sources of variation: systematic variation and random variation. In this paper, only random variations are considered. The random variation can be described by a probability distribution. Here, we focus only on the $V_{\rm th}$ variation at time zero, which is the most important [36]. The standard deviation (SD) of the $V_{\rm th}$ shift is given by

$$\sigma_{V_{\rm th0}} = \frac{A_{\Delta V_{\rm TH}}}{\sqrt{2WL}} \quad (5)$$

where $A_{\Delta V_{\rm TH}}$ is Pelgrom's constant [37], and W and L are the transistor width and length, respectively. The integration of two independent random $V_{\rm th}$ values result in factor 2 at the denominator.

E. Environmental Variations

Variations also occur due to environmental sources. We focus on the impact of temperature and supply voltage in this paper.

1) Temperature Variation: The temperature parameter fluctuations impact the operating condition of MOS transistors; the dependence of threshold voltage and temperature (VT) is given by [38]

$$V_{\rm th} = C_{vt} - \frac{Q_{ss}}{C_o} + \Phi_{ms} \quad (6)$$

where $C_{\rm vt}$ is a constant that represents Fermi potential, the surface charge is $Q_{\rm ss}$ at the Si–SiO_2 interface, the gate oxide capacitance is C_o, and work function difference Φ_{ms} is a function of the temperature [38]

$$\Phi_{ms} = -0.61 - \Phi_F(T). \quad (7)$$

Here, Φ_F(T) is Fermi potential. Expression (8) shows that the work function difference reduces with respect to an increase in temperature and therefore leads to a threshold voltage decrement.

2) Supply Voltage Variation: The supply voltage fluctuations affect the operating speed of MOS transistors [36]. For example, variations in switching activity lead to uneven power/current demand across the die/circuitry and may cause logic failures [36]. In addition, transistor subthreshold leakage variations create an uneven load on the supply voltage network. A reduction in the supply voltage degrades the performance of the circuit/transistors and an increment in supply voltage enhances the performance.

F. Aging Variations

As already mentioned, BTI is one of the major mechanisms causing the aging of chips and induces $V_{\rm th}$ shifts. However, the BTI-induced $V_{\rm th}$ is a stochastic process for time $t > 0$.

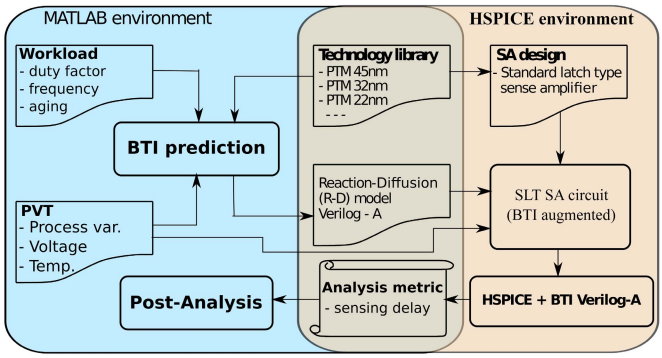

Fig. 2. Analysis framework for the standard latch SA circuit.

Si–H covalent bonds at the interface undergo stochastic fluctuations effected by random dopant fluctuations for time $t > 0$ (see equation 1).

The SD of the V_{th} variation caused by the interface traps is given by [14]

$$\sigma_{\Delta V_{\text{th}}(t)} = \sqrt{\frac{q t_{\text{ox}} \mu(\Delta V_{\text{th}})}{(1+m)\epsilon_{\text{ox}} A_G}} \tag{8}$$

where q is the charge, t_{ox} is the oxide thickness, μ is the mean of the BTI-induced threshold voltage shift, m is the mobility, ϵ_{ox} is the oxide electric field, and A_G is the effective area $(W * L)$.

Finally, the process and BTI-induced variation can be modeled together [18] using (5) and (8); the result is

$$\sigma_{V_{\text{th}}(t)} = \sqrt{\sigma^2_{V\text{th}0} + \sigma^2_{\Delta V_{\text{th}}(t)}}. \tag{9}$$

III. Analysis Framework

In this section, the analysis framework of the standard latch SA circuit is described. Thereafter, the output performance metric is presented. Finally, the conducted experiments are presented.

A. Framework Flow

Fig. 2 depicts a flexible and generic BTI framework for the standard latch-type SA circuit. The framework evaluates the BTI impact for different designs, technologies, and workloads under normal conditions and considering VT variations. The framework consists of MATLAB and HSPICE working environments. The MATLAB environment typically is used for preprocessing and postprocessing; it prepares BTI-augmented files to run in HSPICE. The results of HSPICE, which simulates the BTI-augmented netlist, are subsequently postprocessed in MATLAB. The analysis framework is divided into three blocks (i.e., input, processing, and output blocks) and they are explained next.

1) Input: The input blocks of the framework are the SA design, technology library, workload, and VT specification. They are explained as follows.

1) SA Design: In general, all SA designs can be used. In this paper, we focus only on the standard latch-type SA. The SA design is described by an HSPICE netlist. The differential input depends on the technology node. For example, implementing the above SA circuitry in 45 nm requires a differential input signal of 100 mV.
2) Technology Library: Different technology nodes are considered in this paper; they are 45, 32, 22, and 16 nm and are obtained from PTM library cards [39].
3) PVT: This block defines the process, temperature, and voltage variations. In this paper, we restrict ourselves to the random or local variations of the threshold voltage and use 1000 Monte Carlo runs for each experiment. We consider temperatures $T_1 = 298$ K, $T_2 = 348$ K, and $T_3 = 398$ K and supply voltages $V_1 = -10\%V_{\text{dd}}$, $V_2 = V_{\text{dd}}$, and $V_3 = +10\%V_{\text{dd}}$. Note that each technology has its own nominal voltage.
4) Workload: The shift in threshold voltage is a function of stress and relaxation durations of the transistors. This implies that BTI degradation depends on the number of ON and OFF (idle) states of the input patterns, which translates into workload. To perform realistic workload analysis, we assume that today's application consists of 10%–90% memory instructions and the percentage of read instructions is typically 50%–90%. We derive from this the following workload sequences: $S1$: $R0I^{99}$, $S2$: $R0R1I^{198}$, $S3$: $R0^4I^1$, $S4$: $(R0R1)^4I^2$, $S5$: $(R0)I^{24}$, $S6$: $(R0R1)I^{24}$, $S7$: $(R0)I^{50}$, and $S8$: $(R0R1)I^{50}$. In these sequences, $R0$ stands for read 0, $R1$ stands for read 1, and I for idle operation (which includes memory write operations). For example, $S1$: $R0I^{99}$ is the workload where read 0 is followed by 99 idle operations. The best and worst case sequences (i.e., $S2$ and $S3$, respectively) will be analyzed in most detail.

The workload inputs are typically characterized by their duty factor, frequency, and aging (or stress time). The BTI impact sensitivity is highly dependent on the input stimulus clock cycle (i.e., frequency), its aging, and duty factor (dc stress or ac stress) with respect to the affected device or circuitry.

1) *Frequency:* The BTI-induced degradation depends on the signal frequency to the SA design. In this experiment, the frequencies considered for the SA design are 1.32, 1.89, 2.70, and 3.86 GHz for the 45-, 32-, 22-, and 16-nm technology nodes, respectively. A design version is generated for each targeted frequency by scaling the device technology with a scale factor $>= 0.7$ and by selecting appropriate device dimensions [40].
2) *Aging:* The BTI-induced degradation strongly depends on the stress time. The stress time defines how long the workload sequence is being applied. A workload sequence is assumed to be repeated until the age time is reached.
3) *Duty Factor:* The input signal is a function of the duty factor that affects the BTI-induced degradation of the SA design. The duty factor of the input SAenable signal (see Fig. 2.) is approximately 0.48. This applies only to read operations. During write or idle operations, the SAenable signal is disabled. From the waveform analysis, we extract for all transistors individually their stress and relaxation cycles, thereby obtaining accurate duty

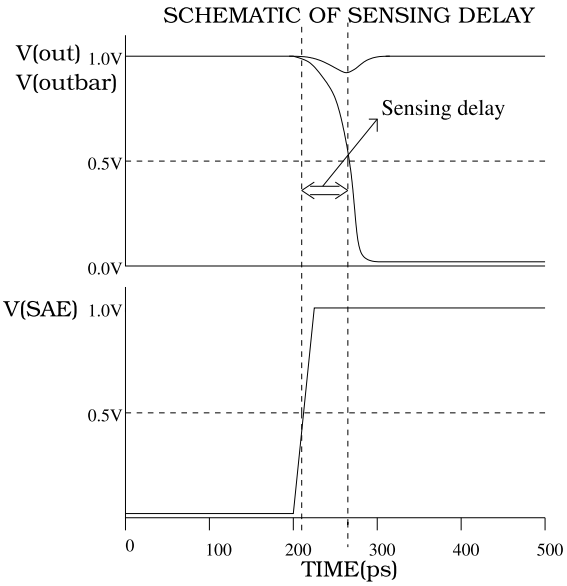

Fig. 3. Metric diagram of sensing delay.

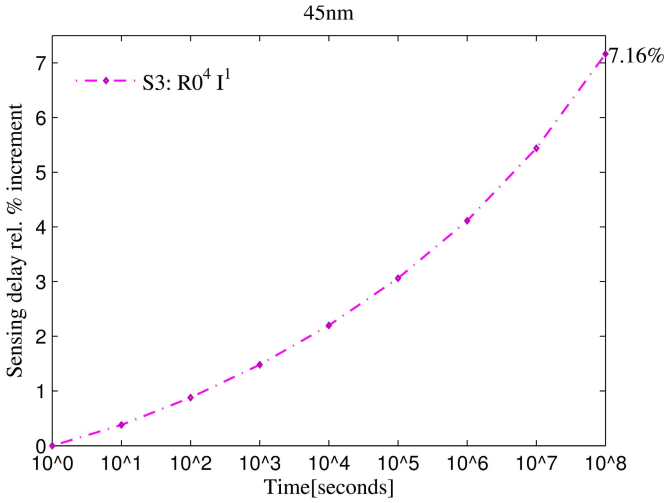

Fig. 4. BTI impact on Sensing delay for the 45-nm technology.

cycles for each transistor. This enhances the accuracy of our simulation results. Based on the duty factor and age time, interface traps ((3), (2)) or threshold voltage increments (3) can be attributed to all transistors in an accurate manner.

2) Processing: There are two processing blocks, the BTI predictor and the HSPICE simulation unit. The long-term BTI predictor uses the duty factor, frequency, and aging to predict the interface traps/threshold voltage increment of each device in the SA. In addition to workload inputs, inputs are required from the RD model (such as K_f, K_r, and D_H), technology parameters, and the VT. Once the BTI-induced V_{TH} increments are calculated per transistor, the original BTI-free netlist will be updated. This new netlist is simulated in HSPICE/Verilog-A.

3) Output: Finally, postanalysis of the results is performed for varying voltages and temperatures using the MATLAB environment.

B. Output Analysis Metrics

In this section, the sensing delay metric used for analyzing the BTI impact on SA is described.

1) Sensing Delay: The sensing delay metric is determined when the trigger signal (i.e., SAenable input signal) reaches 50% of the supply voltage and the target (i.e., either *out* or *outbar* falling output signal) reaches 50% of the supply voltage. The difference between the target and the trigger results in sensing delay as shown in Fig. 3. Furthermore, the relative variation of the sensing delay due to BTI is the difference between the measured sensing delay when BTI is added and referenced sensing delay when BTI is not added.

C. Simulation-Based Experiments Performed

In this paper, six sets of experiments are performed to analyze BTI impacts. These experiments are described as follows.

1) *Temporal BTI Impact Experiments:* The BTI impact on sensing delay of the SRAM SA is investigated.
2) *Workload-Dependent BTI Impact Experiments:* The BTI impact on the sensing delay of the SRAM SA for different workloads on different technology nodes is investigated.
3) *Technology-Dependent BTI Impact Experiments:* The BTI impact on sensing delay of the SRAM SA synthesized from different technology nodes is investigated.
4) *Supply-Voltage-Dependent Experiment:* The BTI impact on sensing delay of the SRAM SA for three supply voltages (i.e., from -10% of V_{dd} to V_{dd} and $+10\%$ of V_{dd}) for different technology nodes is presented.
5) *Temperature-Dependent Experiments:* The BTI impact on sensing delay of the SRAM SA for three temperatures (i.e., 298 K, 348 K, and 398 K) for different technology nodes is explored.
6) *Combined Impact of BTI- and PVT-Dependent Experiments:* The combined BTI and PVT impact on the SA sensing delay for the best and worst case workloads for different technology nodes, supply voltages, and temperatures is analyzed.

IV. Simulation Results

In this section, we present the analysis results of the experiments mentioned in the previous section.

A. Temporal BTI Impact

Fig. 4 shows the BTI impact of workload $S3$ on the sensing delay for different aging times for nominal supply VT. Fig. 4 shows that the sensing delay increases as the SA ages. For this workload, the sensing delay increases from 14.10 to 15.11 ps (7.16% increase) caused by the BTI only.

B. Workload-Dependent BTI Impact

The BTI-induced degradation is sensitive to the applied workloads.

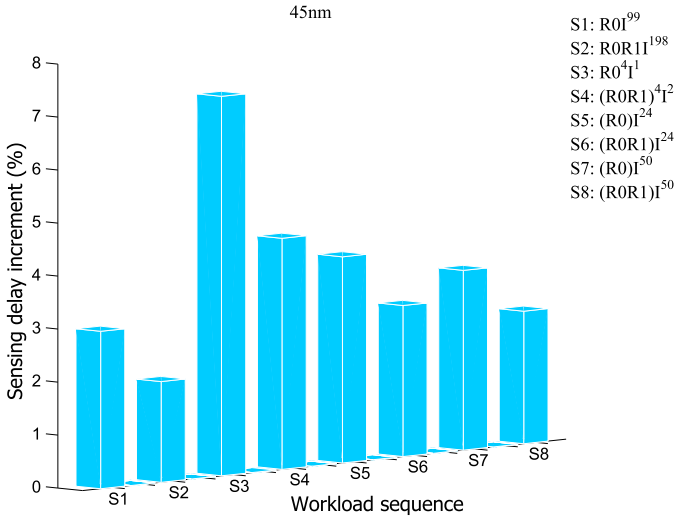

Fig. 5. Workload-dependent sensing delay.

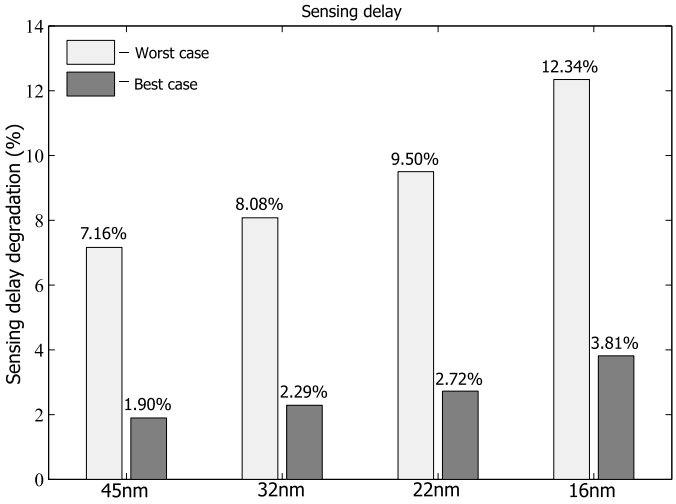

Fig. 6. BTI impact on sensing delay for all technology nodes.

Fig. 5 shows the BTI-induced degradation of the SA for the eight workloads defined in Section III at nominal supply VT for 3 operational years.

Fig. 5 shows a large variation in the relative sensing delay increment. For instance, workload $S2$ is impacted the lowest by BTI (1.90% degradation), whereas $S3$ the most (7.16% degradation). This can be explained by the severity of the workload. We define $S2$ and $S3$ as the best and worst case workloads, respectively.

C. Technology-Dependent BTI Impact

Fig. 6 depicts the relative BTI impact on the sensing delay for different technology nodes for the best case and worst case workloads at nominal supply VT. Note that the nominal supply voltage equals $V_{dd} = 1.0$ V for 45 nm, $V_{dd} = 0.9$ V for 32 nm, $V_{dd} = 0.8$ V for 22 nm, and $V_{dd} = 0.7$ V for 16 nm.

Fig. 6 shows that the sensing delay degradation is obviously dependent on the applied workload. For example, for the 22-nm technology node, the BTI-induced degradation is 9.50% for the worst case workload and only 2.72% for the best case workload, respectively.

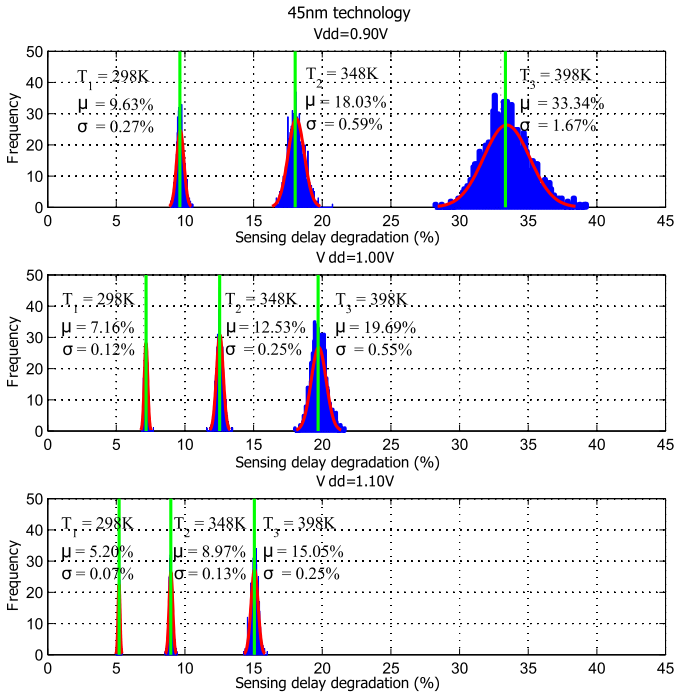

Fig. 7. Worst case sensing delay for supply VT variations for the 45-nm technology.

Fig. 6 also shows that the sensing delay degradation increases for smaller feature sizes irrespective of the two workloads. For instance, for the worst case workload, the degradation is 7.16% for the 45-nm technology node, 8.08% for the 32-nm technology node, 9.50% for the 22-nm technology node, and 12.34% for the 16-nm technology node. Especially at the lower nodes, the BTI may significantly impact the device reliability.

D. Supply-Voltage-Dependent BTI Impact

Figs. 7 and 8 depict the BTI-induced sensing delay for the 45-nm technology node, for the worst case and best case workloads at various supply voltages and temperatures. Figs. 7 and 8 show for each VT experiment the impact on the sensing delay (on the horizontal axis). Note that only 1000 Monte Carlo simulations have been performed for each experiment due to computational constraints. The 1000 simulations are grouped in 50 bins (see the blue curves in Figs. 7 and 8) with their frequency being plotted on the vertical axis. On top of these bins, a normal distribution is fit (see the red curves in Figs. 7 and 8), which reflects and follows the ΔV_{th} distribution due to BTI degradation. The vertical green lines in Figs. 7 and 8 present the mean degradation of the sensing delay (in percentage for each experiment). For example, for the worst case workload with $V_{dd} = 0.9$V and temperature $T_1 = 298$ K, the mean sensing delay $\mu = 9.63\%$ and the SD $\sigma = 0.27\%$. In this section, we discuss only the results of the voltage experiments for nominal temperature $T_1 = 298$ K.

From Figs. 7 and 8, we conclude that the BTI-induced degradation is significantly impacted by the voltage variations and workload. This is true for both the mean and SD. For instance, for the worst case workload (at T_1), the BTI-induced

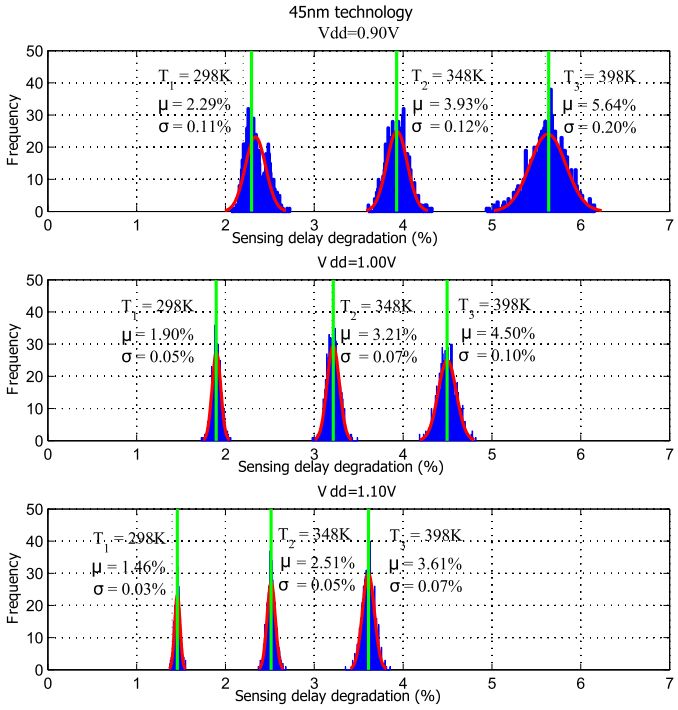

Fig. 8. Best case sensing delay for supply VT variations for the 45-nm technology.

mean degradation on sensing delay is 9.63% at 0.9 V, while only 5.20% at 1.1 V. For the best case workload, these values are 2.29%, 1.90%, and 1.46%, respectively. Moreover, the SD of the sensing delay for the worst case workload at T_1 is 0.27% at 0.9 V, while 0.12% at 1.0 V and 0.07% for $V_{dd} = 1.1$ V. For the best case workload, the SDs of the degradation equally are 0.11%, 0.05%, and 0.03% for supply voltages 0.9 V, 1.0 V, and 1.1 V, respectively. Hence, at a higher voltage, the *relative* degradation and its spread are lower for both workloads. Note that it is about relative impact and not the absolute one. The absolute impact at higher voltage is larger than at lower voltage.

Fig. 8 shows similar data as Fig. 7 but for the best case workload. We observe similar trends as for the worst case workload. The mean and SD of the degradation reduces for higher V_{dd} (for temperature fixed at $T_1 = 298$ K). However, they differ in amplitude with respect to the best case workload. For example, the mean and SD at T_1 and $V_{dd} = 0.90$V are 2.29% and 0.11%, respectively, for the best case workload, while 9.63% and 0.27%, respectively, for the worst case workload.

E. Temperature-Dependent BTI Impact

Figs. 7 and 8 also show the BTI impact for various temperatures. Note that the temperature is varied between 298 K and 398 K. Figs. 7 and 8 show that both the mean and SD of the degradation are significantly impacted by the temperature, especially at −10% supply voltage.

For example, for the worst case workload as shown in Fig. 7, the mean sensing delay degradation is 9.63% for $V_{dd} = 0.9$V and $T_1 = 298$ K and equals 18.03% for $T_2 = 348$ K and 33.34% for $T_3 = 398$ K. For the same conditions, the SD

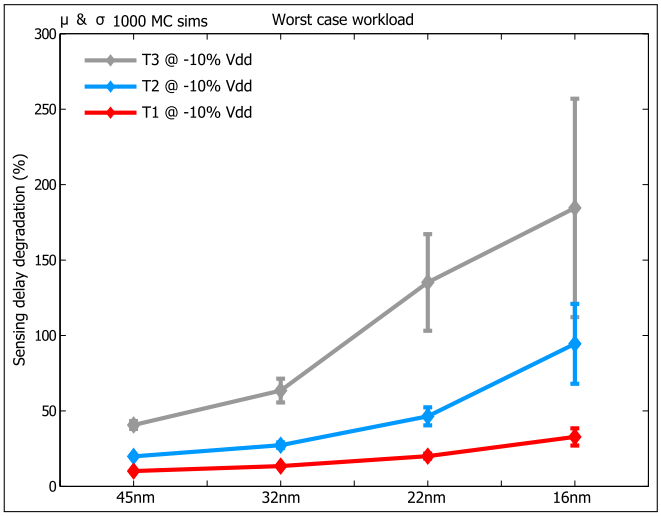

Fig. 9. Worst case SD for −10% Vdd for various nodes and temperatures.

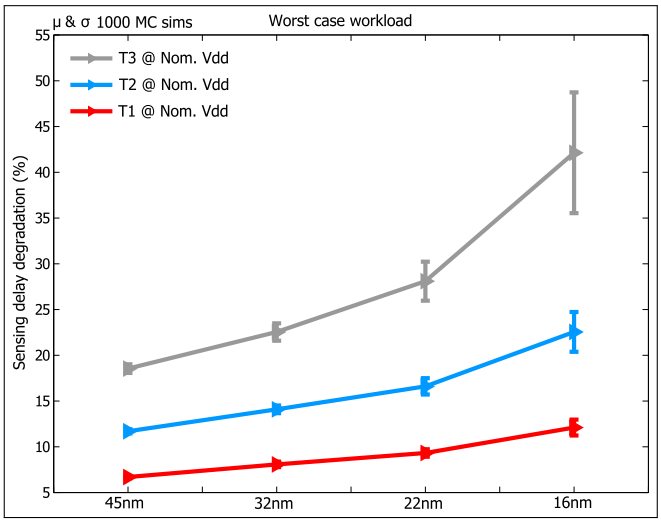

Fig. 10. Worst case SD for Nom. Vdd for various nodes and temperatures.

increases from 0.27% (at T_1) to 1.67% (at T_3). At a higher voltage, the same trends are observed with lower impact. For example, the mean degradations at $V_{dd} = 1.1$ V and T_1 equal 5.20% and 8.97% at T_3.

From this, we deduce that the lower the operational voltage, the higher the impact of temperature. Similar observations can be made from Fig. 8 for the best case workload.

F. Combined Impact of BTI- and PVT-Dependent Experiments

Figs. 9–11 depict the sensing delay for the worst case workload for the three supply voltages, respectively. In Figs. 9–11, our analysis focused on both the mean μ (denoted by the opaque markers) BTI-induced impact and the SD σ (denoted by the edges of the vertical lines). Figs. 9–11 show the impact of technology and temperature for each voltage value. Note that Figs. 7 and 8 depict only the VT impact for the 45-nm technology.

From Figs. 9–11, we conclude the following.

1) For newer technology, the BTI impact worsens; this conclusion is in line with Fig. 6. This conclusion can be

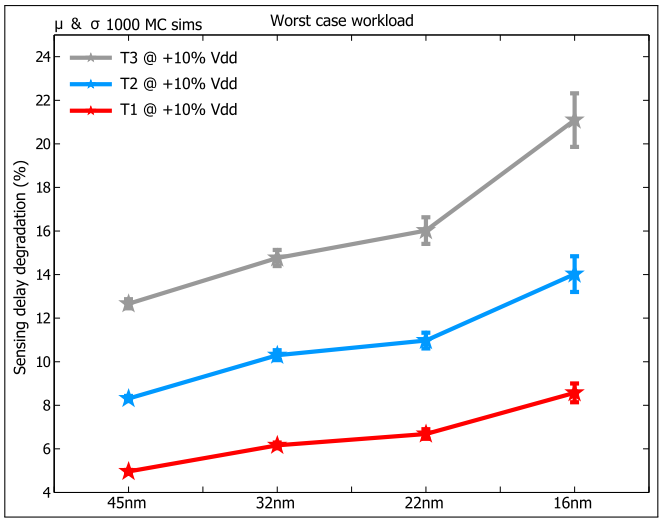

Fig. 11. Worst case SD for +10% Vdd for various nodes and temperatures.

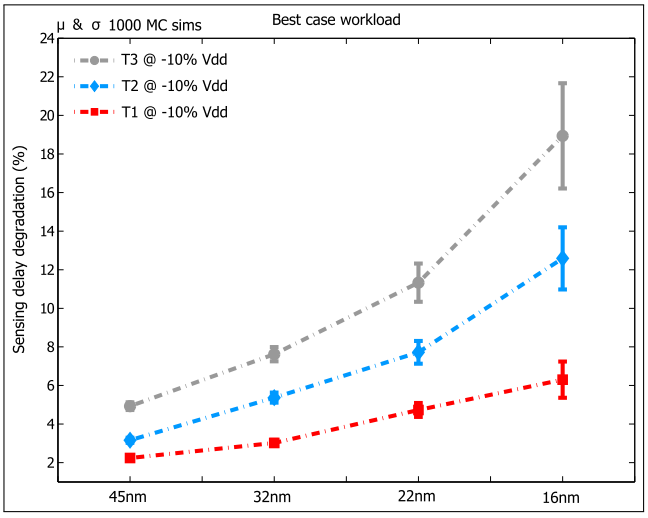

Fig. 12. Best case SD for −10% Vdd for various nodes and temperatures.

TABLE I
FAILING POINTS AT −10% V_{dd} FOR WORST CASE WORKLOAD

		Temperature		
		T1	T2	T3
Technology	$22nm$	0	0	663
	$16nm$	0	442	986

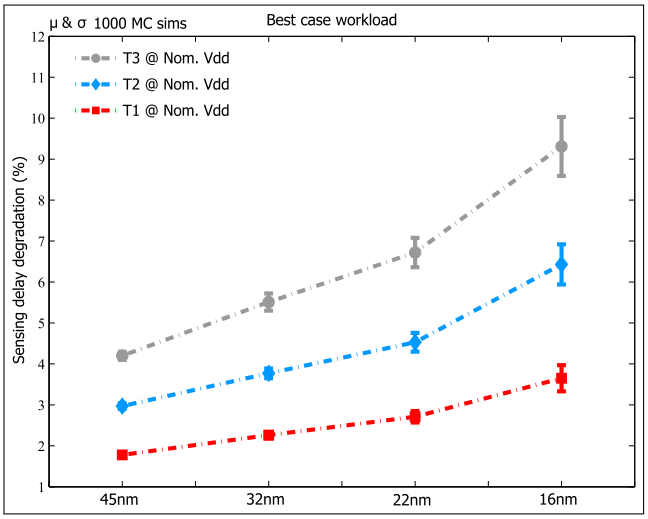

Fig. 13. Best case SD for Nom. Vdd for various nodes and temperatures.

easily made as all graphs are monotonically increases. However, the relative degradation increases with a higher temperature. For example, after an operation of 10^8 s for temperature $T1 = 298$ K, the BTI-induced mean degradation is 10.13% for 45 nm, while 13.42%, 20.02%, and 32.78% for 32, 22, and 16 nm, respectively. In addition, for temperature $T3 = 398$ K, the degradation is up to 4.00× more for 45 nm, while 4.73×, 6.75×, and 5.60× more for 32, 22, and 16 nm, respectively. Furthermore, the mean sensing delay degradation reduces with 10% increase in supply voltage. For example, the degradation reduces for $T1 = 298$ K up to 1.51× for 45 nm, while 1.66× for 32 nm, and 2.15× for 22 nm, and only 2.71× for 16 nm. Moreover, for T3 = 398 K, the BTI impact degradation reduces up to 2.20× for the 45-nm node, 2.82× for the 32-nm node, 4.81× for the 22-nm node, and only 4.38× for the 16-nm node.

2) The SD is the highest for lower technology nodes, higher temperatures, and lower voltages. For example, after an operation of 10^8 s of $T1$, the degradation distribution is 0.27% for 45 nm, while 0.60%, 1.64%, and 5.69% for the 32-, 22-, and 16-nm nodes, respectively. On top of that, the SD for a higher temperature, i.e., $T3 = 398$ K, is up to 9.63× more for the 45-nm node, while 13.15×, 19.51×, and 12.72× for the 32-, 22-, and 16-nm nodes, respectively.

Table I provides information regarding failed simulation (i.e., signal flipped at the output). They only occurred for the advanced nodes (i.e., 22 and 16 nm) at −10% V_{dd} and at high temperatures (i.e., 348 K and 398 K). This shows that scaling and bad operating conditions may significantly impact the reliability. For example, 663 out of 1000 points failed at 22 nm for $T3$. At 16 nm, even failing points have been observed at $T2$, while 986 (which includes almost the entire set) points failed at $T3$.

Figs. 12–14 show similar trends but for the best case workload. The impact of this workload on the sensing delay is, however, much less. For example, the mean degradation reduces up to 4.52× at 298 K to 8.26× at 398 K for 45 nm, while this is only 4.44× to 8.33×, 4.23× to 11.93×, and 5.20× to 9.75× for the 32-, 22-, and 16-nm nodes, respectively. On top of that, the degradation deviation reduces up to 3.86× at 298 K to 13.00× at 398 K for 45 nm, while 3.75× to 21.32× for the 32-nm node, 4.56× to 32.32× for the 22-nm node, and only 6.05× to 26.52× for the 16-nm node. Furthermore, the mean sensing delay and deviation degradation reduces as the supply voltage rises by 10%. For example, the relative mean degradation also reduces up to 3.47× at 298 K to 3.56× at 398 K for 45 nm, while 3.06× to 3.04×, 3.23× to 3.03×, and 2.78× to 2.84× for

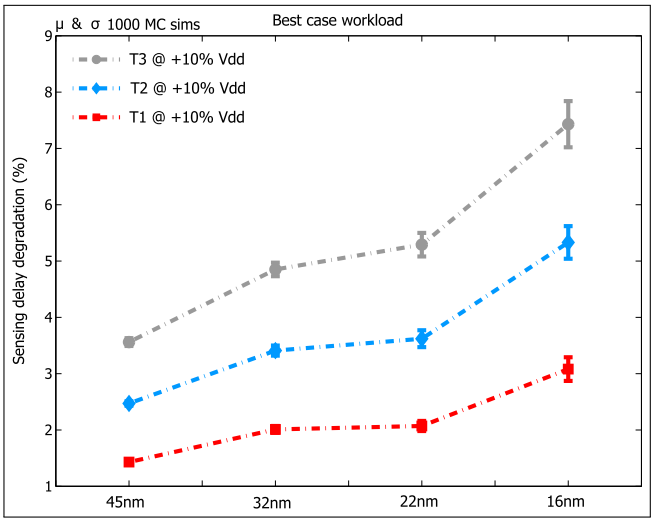

Fig. 14. Best case SD for +10% Vdd for various nodes and temperatures.

32, 22, and 16 nm, respectively. On top of that, the deviation degradation also reduces up to 2.33× at 298 K to 3.00× at 398 K, while this is only 2.17× to 3.08×, 2.44× to 2.90×, and 2.05× to 3.00× for the 32-, 22-, and 16-nm nodes, respectively.

G. Discussion

The SRAM SA robustness and reliability are critical for the overall design of memory systems. The present analysis shows that the BTI-induced sensing delay of standard latch-type SA is a function of process variations, varying supply voltages and temperatures, different technology nodes, and workloads. Evaluating the simulation results with respect to degradation, we observe the following.

1) The SA *sensing delay degradation* is clearly influenced or impacted by the application, *i.e., by the workloads* it is exposed to. In case an application is read intensive, a second parallel SA scheme can be exploited to minimize the performance loss, by sharing the read operations between the two SAs. This, however, doubles the area.
2) The BTI-induced degradation is more significant at lower nodes; this could lead to read failures at lower supply voltage. This suggests that there must be a tradeoff between performance and reliability.
3) A higher supply voltage reduces sensing delay's mean degradation irrespective of the workload and temperature. This indicates that a tradeoff is possible among BTI degradation, power consumption, and the latency.
4) A higher junction temperature increases sensing delay's mean degradation.
   Hence, proper cooling or reducing the SA activity may also reduce the degradation. For example, switching the SA OFF while using the secondary SA reduces the degradation impact.

Therefore, for future designs, SA designers need to consider proper safe margins for critical environmental conditions and long-term operations.

V. Conclusion

This paper investigated the combined impact of BTI, process variations, various supply voltages and temperatures, and different workloads on standard latch-type memory SA for different technologies. The results show that the sensing delay degradation is strongly workload dependent. Both the scaling and increase in temperature severely impact the BTI degradation. Increasing the supply voltage reduces the BTI-induced degradation leading to more reliable and robust SAs, but at the cost of a higher power consumption. Nevertheless, process and BTI variations reduce the reliability and may even cause failures. Optimizing a reliable memory system requires the consideration of all its subparts, i.e., their degradation rate depends on the application (e.g., workload and temperature), for instance, the aging rate of the SA may differ from those of the memory array and other peripheral circuits.

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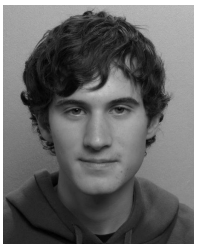

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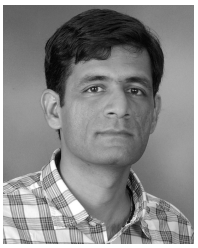

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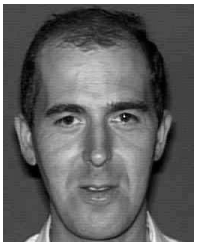
Dr. Raghavan is currently with the Technical Committee of CODES + ISSS, DATE, and IEEE DISPS.



Francky Catthoor (F'05) received the engineering degree and the Ph.D. degree in electrical engineering from Katholieke Universiteit Leuven (KU Leuven), Leuven, Belgium, in 1982 and 1987, respectively.

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Dr. Catthoor was a member of the Steering Board for the VLSI Technical Committee of the IEEE Circuits and Systems Society in 1997. He received the Young Scientist Award from the Marconi International Fellowship Council in 1986. He was the Program Chair of the 1997 IEEE International Symposium on System Synthesis (ISSS) and the General Chair of the 1998 ISSS. He was also the Program Chair and Main Organizer of the 2001 IEEE Signal Processing Systems Conference. He was an Associate Editor of the IEEE TVLSI in 1995–1998, and the IEEE TRANSACTIONS ON MULTIMEDIA in 1999–2001. Since 2002, he has been an Associate Editor of the "*ACM Transactions on Design Automation for Embedded Systems*," and since 1996, he has been an Editor of Kluwer's the "*Journal of Very Large Scale Integration Signal Processing*." Since 1999, he has been on the Steering Board for the IEEE TVLSI.