TU DELFT UNIVERSITY OF TECHNOLOGY

WAFER-SCALE FABRICATION OF GRAPHENE-BASED CONDENSER MICROPHONES

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Wafer-Scale Fabrication of Graphene-Based Condenser Microphones

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Abstract

The evolution of microphone technology can be linked to the growing multimedia and communication market. The first is linked to the music and audiovisual industry, while the latter is linked to smartphones, smart-mobility, and home automation. In all of these audio applications, the common trend is toward downsizing and performance improvement.

State-of-the-art silicon and nickel suspended membranes generally require a large diameter (in the millimeter range) to ensure high sensitivity. To this end, new materials have been studied. The properties of these materials should allow for miniaturization without losing performance. As a matter of fact, over the past decade, researchers have been studying how to implement graphene in sensing applications. The properties of graphene have enabled the realization of a number of devices capable of outperforming their silicon counterparts while decreasing the sizes of the sensors.
The properties of these new materials should allow for greater flexibility and a thinner membrane that will ensure a greater mechanical response. This will allow for the creation of a smaller membrane. On the other hand, suspended graphene-based as membranes of a capacitive microphone generally featured a low-yield process in which the graphene is transferred from the grown substrate to the target device using polymers. The low-yield is related to a not fully automated transfer method. These restrictions limit the mass production of these devices, making large-scale production difficult.

Therefore, a possible method to obtain a transfer-free, wafer-scale, high-yield process for the realization of a graphene-based capacitive microphone is presented. The use of graphene will allow for miniaturization and improved performance.

The presented work will be structured as follows:

- Chapter 1 - Introduction: The rationale for the thesis is provided, underlying the advantages of using graphene in the applications of capacitive microphones. The physics and history of capacitive microphones will be explored. A method to improve the sensitivity while scaling the device will be investigated. The research questions that started this thesis work are listed.
- Chapter 2 - Literature Review: A study on state-of-the-art capacitive microphones will be introduced, focusing on the transfer and transfer-free methods for the realization of graphene-based capacitive microphones. The knowledge gained will provide an overview of the beneficial properties of graphene in condenser microphone devices.
- Chapter 3 - Device Simulations & Concept Design: The device will be simulated with 2 different models. The used models will define the geometry of the final device. Subsequently, the design of the mask will be presented. An overview of the used materials and the reason behind their choice will be presented.
- Chapter 4 - Fabrication Results: Some test will be exposed and the process used for the realization of the final device will be presented, highlighting all the critical steps of the presented flowchart.
- Chapter 5 - Measurement of the Processed Device: The results and the measured data will be discussed.
- Chapter 6 - Final Conclusions & Future Perspective: The results of the presented work will be highlighted and suggestions for a future improvement of the device will be presented.

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Nomenclature

ρ	Membrane mass density
ϵ_0	Permittivity of Vacuum
ϵ_A	Air Permittivity
ϵ_{ox}	Silicon Oxide Permittivity
η_0	Membrane pretension
μ	Viscosity of Air
σ_0	Residual Tensile Stress
A	Back-plate Area
$A_\epsilon^{'}$	Effective Membrane Area minus Acoustic Holes Area
Ar	Ratio of Hole Area to Non-Hole Area
$B(Ar)$	Effective Back-plate Area Coefficient
C	Capacitance
f_{es}	Electrostatic Force
g	Air Gap Height
g_0	Air Gap Height at 0 Bias Voltage
h	Membrane Thickness
H_m	Internal Distance
I_{cap}	Capacitor Current
k	Effective Spring Constant
n	Number of Holes
P_{in}	Input Pressure
Q	Quiescent Charge
q	Small Signal Charge
R_{ag}	Damping resistance
R_{mem}	Membrane Radius
S	Electrostatic Sensitivity
S_m	mechanical Stress
t_{ox}	Oxide Thickness
u_m	Axial Membrane Velocity
$U_{0,av}$	Quiescent Average Deformation
U_{av}	Small Signal Deformation
u_{av}	Average Membrane Velocity
V_p	Maximum Pull-in Voltage
V_{bias}	Bias Voltage
V_{out}	Open Circuit Output Voltage
V_{pol}	Polarization Voltage

1 Introduction

Nowadays, the trend of electronics is following the path of miniaturization. The ability to scale devices attracts designers of different research fields. Scaling a particular component of a device means a smaller footprint, thus more free space on the PCB that can be occupied by other components or that can be used to decrease the size of the device. This miniaturization process has allowed the creation of Micro-Electro-Mechanical Systems (MEMS), thus creating the possibility of reducing the size of acoustic devices, such as microphones.

MEMS microphone technology is widely used in the consumer electronics market. These devices are generally found in smartphones and automotive applications. On the other hand, the physical limitation imposed by the use of silicon [1] will allow the realization of devices in the order of millimeters. Dimensions of this type are not in line with the trend towards miniaturization present, for example, in the smartphone industry. Therefore, the study of new materials is fundamental for the miniaturization goal of some manufacturers.

The use of materials other than silicon could overcome the physical problems associated with silicon (low flexibility and thick membrane). Using thinner materials will allow for a greater mechanical response at the same sound pressure. Some materials are particularly thin because they consist of a single layer of atoms. These materials (such as graphene) are called 2D materials and will allow for the ultimate miniaturization of the device. Therefore, a study was conducted on the properties of graphene.

This thesis will present the approach used for the realization of a graphene-based capacitive microphone. The final device will feature miniaturized dimensions and a process flow that could make it suitable for large-scale production. This thesis focus on the possibility of creating a wafer-scale, transfer-free process. Transfer methods are generally not completely automized leading to a sharp decrease in the process yield. Therefore, the use of transfer-free graphene could increase the process throughput and avoid the use of polymers.
This section discusses the principles of Condenser Microphone physics. The study of these principles will be carried out with particular attention to Graphene-based and Silicon-based devices.
The knowledge of this section will help the reader understand the steps performed during the processing and fabrication phases of the presented thesis. In addition, the limits of the current state-of-the-art of graphene are listed with proposals on how to overcome them. Furthermore, the research questions are presented.

1.0.1 History & Evolution of Microphones

Before the invention of the first microphone in 1925 (a carbon microphone), recording sessions followed a completely different process than what is known today. Orchestras and music collectives were recorded using a big cone[2]. The performers were placed in front of the widest part of the cone. The larger diameter part of the cone captured the ensemble of the acoustic waves and concentrated them at the rear exit. The rear exit was realized through a cone with a smaller diameter than that used to capture the ensemble of the acoustic waves. This small-diameter cone mechanically moved a membrane that realized a groove in a rotary wax disc. In this technology, the position of an instrument had to be considered. To obtain a cleaner sound, the amplitude and frequencies of acoustic waves emitted by an instrument should be considered with respect to the spatial distance from the "capturing" end of the cone.

Nowadays microphones are used to transduce a mechanical wave into an electrical signal. The advantages of modern microphone technology to "cone" technology are numerous. On the other hand, the new technology also has some important limitations that must be considered. For example, to perceive the audio signal as accurately as possible, the position of the musician is not of interest as in "cone" recordings, but a maximum flat response in the bandwidth of 20 Hz-20 kHz is required. This will ensure a faithful capture of the audio signal which will be correctly interpreted by the human auditory system.

1.1 Silicon Condenser Microphones Physics

Sound is defined as a vibration that can propagate in an elastic medium. Capacitive microphones are widely used and produced due to their flat response (which allows for good detection quality) and low noise level (which ensures a readable output signal).

1.1.1 Condenser Microphone Theoretical Response

Condenser microphones are a special type of microphones, widely used in MEMS applications. These systems are based on variations in the measured capacitance value between a fixed and a movable plate. The movable plate is thinner and acts like a diaphragm. The diaphragm will vibrate when a sound wave hits the device, thus changing the capacitance value. To bias the plate to a fixed voltage, a voltage source is required. A simple condenser microphone is polarized externally (bias voltage is supplied from an external power supply).
Fig.1 depicts the cross-section of a condenser MEMS microphone.

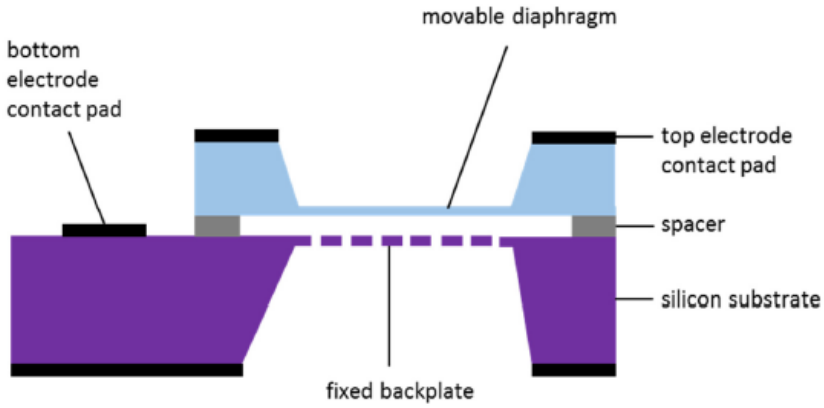


Figure 1: MEMS Silicon-based Condenser Microphone cross-section [1].

The two parallel plates (fixed and movable) are separated by an air gap as insulator (employed as a spacer). The resulting capacitance between the two parallel plates will behave like the following equation[1]:

$$C = \frac{\epsilon_0 A}{g} \tag{1}$$

Where, ϵ_0 is the permittivity of vacuum (which equals that of air), A the plate area and g the air gap thickness.
The back-plate is perforated with venting holes. These holes allow air to flow from the inlet to the outlet of the air gap when the movable plate (diaphragm) vibrates. In the absence of holes, the compressed air will behave as a mechanical damper. Therefore, at high frequencies, the diaphragm does not vibrate as the mechanical damping will dominate, creating a low pass filter (LPF) effect. This will reduce the sensitivity of the system.
The damping resistance will behave as described in the following equation[1]:

$$R_{ag} = \frac{12\mu}{n\pi g^3} B(Ar) \tag{2}$$

Where, μ is the viscosity of the air, g is the air gap thickness, n the number of holes and B(Ar) is the effective back-plate area coefficient. Considering Ar as the ratio of hole area to non-hole area:

$$B(Ar) = \frac{1}{4} ln(\frac{1}{Ar}) - \frac{3}{8} + \frac{1}{2}(Ar) - \frac{1}{8}(Ar)^2 \tag{3}$$

Therefore, the mechanical damping is reduced by increasing the number of holes and the air gap.
When pressure is applied, the air gap is reduced and the air in the chamber will behave like a resistor (R_{ag}). R_{ag} will follow the previous equation and dampen the vibrations. The magnitude of R_{ag} depends on the inverse of the volume of the back-chamber[1].
The maximum pull-in voltage (V_P) will cause the diaphragm collapse to the back-plate:

$$V_P = \sqrt{\frac{8}{27} \frac{k g_0^3}{\epsilon_a A'_\epsilon}} \tag{4}$$

Where k is the effective spring constant of the membrane. The spring constant value will be defined by the product of the stiffness of the material multiplied by the value of the deformation of the material. g_0 is the air

gap height at 0 bias voltage, ϵ_a is the air permittivity and $A_\epsilon^{'}$ is the effective area of the diaphragm (given by the total area of the membrane minus the total area of the venting holes. The latter is subtracted from the membrane area as it will be the main cause of the damping effect).
To avoid collapse, the bias voltage should be one third of the pull-in voltage[1].
The input sound pressure level (input SPL) is defined as the ratio of the audible sounds captured by the microphone (P_1) to the lowest pressure detected by human hearing (P_2 which is 20 μPa)[1]:

$$input_{SPL} = 20log\Big(\frac{P_1}{P_2}\Big) \tag{5}$$

The resonance frequency (defined by the membrane radius, the membrane pretension η_0, the membrane mass density ρ, and the membrane thickness) will limit the upper bandwidth.

$$f_0 \approx \frac{2.4}{2\pi r}\sqrt{\frac{\eta_0}{\rho t}} \tag{6}$$

Furthermore, the dominant noise mechanism is the squeezed-film effect due to damping of air which depends on the size of the acoustic holes. The noise floor will affect the minimum detectable sound level that will be captured by the microphone[1].
Therefore, it is possible to define an electroacoustical sensitivity that will obey the following equation[1]:

$$S_e = \frac{V_{bias}}{g} \tag{7}$$

Where V_{bias} is the bias voltage. The bias voltage and the thickness of the air gap will affect the electrical sensitivity, but the bias voltage in turn depends on g. The variation of the air gap pressure will affect the mechanical sensitivity of the system[1]. Furthermore, the displacement (which depends on the membrane rigidity) will have an impact on the definition of the sensitivity.
If a circular membrane is of interest, the mechanical sensitivity will be equal to:

$$S_m = \frac{R_{mem}^2}{8\sigma_0 h} = \frac{\Delta g}{\Delta P} \tag{8}$$

Where R_{mem} is the membrane radius, σ_0 is the residual tensile stress, h is the membrane thickness, Δg is the air gap change, and ΔP is the change in pressure.
Therefore, the total sensitivity (given by the product of the electrical and mechanical sensitivity) will depend on all the design parameters (the air gap, the membrane radius that will define its area, and the membrane thickness).

$$S = \frac{V_{bias}}{g}\frac{R_{mem}^2}{8\sigma_0 h} \tag{9}$$

The parameter that defines whether a microphone can detect sound waves from all directions or from a specific direction is called directionality. The directional pattern can be graphically represented by a polar pattern. Omnidirectional microphones are able of equally detecting sound waves from all directions. Conversely, directional microphones show the strongest output when sound waves arrive on a single axis (which is parallel or vertical to the moving membrane surface).
In the human auditory system, the eardrums act like a membrane. This diaphragm is approximately 100 μm thick. This limits the flat frequency response to 2 kHz and imposes a detection limit at 20 kHz. On the other hand, thinner and lighter membranes allow for better detection of sound waves at high frequency.

1.1.2 General Process for the Realization of a Condenser MEMS Microphone

A widely used manufacturing method is bulk-micromachining which produces certain structures within a silicon substrate. The substrate can be patterned using anisotropic etching or reactive ion etching (RIE). RIE can be employed using the Bosch or cryogenic method.
Another common method is surface micromachining. Here, the layers are etched on top of a substrate. It is a more complex technique than bulk-micromachining, but the process is more efficient due to its flexibility in structure design linked to the absence of the need for a front-to-back side alignment. The holes in a surface micro-machined microphone are typically realized through a combination of both methods.
The use of a silicon membrane allows no degradation of the performances of a condenser microphone in a temperature range between $-40\,^{\circ}$C and $120\,^{\circ}$C[4]. Furthermore, these devices will not be strongly impact by

humidity[4].
One of the fundamental building blocks of a MEMS condenser microphone is a flexible membrane electrode. The use of materials other than silicon could allow for greater flexibility, leading to higher mechanical responses. The cross-section of the transducer is depict in Fig.2.

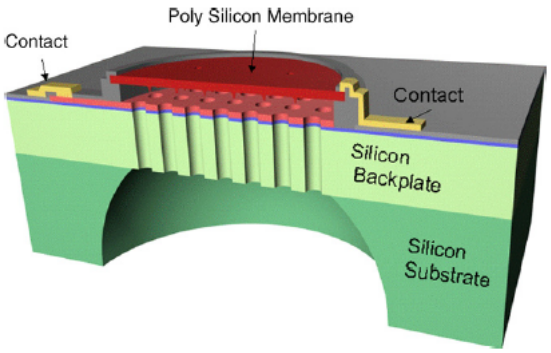


Figure 2: Cross-section of a MEMS Silicon-based Condenser Microphone [4].

In [4], on top of a bulk micro-machined cavity, a 5 μm tick rigid membrane is positioned. The rigid membrane is characterized by a series of holes that cover 19% of the area. Using surface micro-machining, a 2 μm height air gap was etched. Furthermore, a poly-Silicon membrane (with a thickness of 400 nm) was created. The size of the membrane is 1 mm and the final sensor will be defined by a size of 2 mm x 2 mm x 0.4 mm[4]. The dimensions of the sensor are in the millimeter range.

To achieve low noise and high sensitivity, a very flexible membrane characterized by low damping is required. Furthermore, the sensitivity can be controlled by doping and annealing[4].
Doping is the introduction of impurities into an intrinsic semiconductor. The purpose of this technique is to modulate the electrical and structural properties of the material.
Annealing is a heat treatment that changes the chemical and physical properties of a material. This technique is used to increase its ductility and reduce its hardness and involves heating a material above its re-crystallization temperature, maintaining an adequate temperature and then cooling.
Since silicon processing is studied in detail, all processes and materials are optimized to obtain the best device performance. On the other hand, the mechanical limits of silicon will allow for good detection, only at the expense of large membrane areas[4]. Using different materials for the membrane will result in different performance, as the device will have different parameters (such as Young's Modulus, Poisson ratios, thermal conductivity, density and thermal expansion coefficient).

Therefore, it was possible to observe that silicon-based condenser microphones are generally characterized by a large footprint that allows for a maximally flat response and a good sensitivity. Since this technology has been around for a long time, there are process optimizations for mass production. On the other hand, the trend toward miniaturization requires the use of new materials with mechanical properties that would allow for dimension reduction. An alternative would be to use nickel to make the membrane. Unfortunately, the use of such material will not allow for device miniaturization. Therefore, a thinner and more flexible material should be employed to create the diaphragm. The use of graphene can overcome these limitations due to its high mechanical compliance (spring constant ranging from 0.1 to 1 N/m)[5].

1.2 Research Questions

Based on the above considerations, a series of questions emerged about the critical steps of the project presented. The answer to these questions will clarify whether the realization of a transfer-free, wafer-scale graphene-based capacitor microphone is possible and what its limitations and advantages are.

- Is it possible to create a process flow to fabricate MEMS condenser microphones using graphene for large-scale production?
    1. Which materials will be suitable for the realization of the Back-plate?
    2. What dimensions can be obtained for the realization of graphene membranes?

3. Is it possible to realize a transfer-free process without compromising the properties of the graphene membrane?
4. Is a graphene-based membrane capable of increasing the microphone performances (sensitivity, dynamic range) while increasing the device scalability?

2 Literature Review

Telecommunications, automotive and home automation are only a small part of the audio electronics business which is oriented towards the device miniaturization. The state-of-the-art electronics inherent in this field is mainly based on silicon. As a disadvantage, the silicon membrane in capacitive microphones will occupy a large footprint which is in conflict with the downsizing trend.
Hence, a new material is needed to realize these membranes in order to obtain small dimensions, without compromising the overall performances of the device. Therefore, in this chapter, some graphene-based and silicon-based applications are presented. Comparing these two technologies will highlight the advantages and disadvantages offered by graphene-based devices.

2.1 Fabrication of MEMS Silicon-Based Condenser Microphone

Considering the work of [4], in a laminated board, a hole is present. On top of this hole, the microphone is mounted. To connect the MEMS die to an integrated circuit (IC) used for signal amplification, wire bond was used. A plastic cap encapsulates the chip and forms a back-volume with a size of $3\,\mathrm{mm}^2$ to $10\,\mathrm{mm}^2$. The back-volume dimension is used as a pressure reference for capacitive microphone operations. Fig.3 describes a directional MEMS Silicon-based condenser microphone realized in[4]. This device presented some laser drilled holes. These holes have a diameter of $100\,\mu\mathrm{m}$. This determines the phase shift value required for correct directivity. When the optimum number of holes is reached, a suppression of 18 dB on the background noise is obtained in the range from 400 Hz to 4 kHz. This range is compatible with the frequency range of the human voice. Therefore, this Silicon-based MEMS condenser microphone will exhibit good performances and good directivity[4].

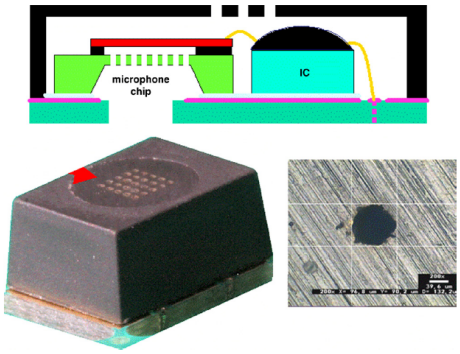


Figure 3: Directional MEMS Silicon-based Microphone[4].

A microphone process flow is presented in [6]. Here, MEMS Silicon-based Microphones are realized with two process:[6]

- Double Chip Microphones: They consist of 2 wafers, one for the back-plate and one for the membrane. The two wafers are processed separately and combined with different bonding techniques. Both wafers are single-crystal silicon wafers. Since tertamethylammonium hydroxide (TMAH) etching will be performed, the silicon thickness was preserved through the use of boron etch-stopper. In addition, a boro-silica glass (BSG) sacrificial layer was developed.
- Single Chip Microphones: They do not require bonding techniques. For these chips it is possible to realize the back-plate and the membrane in polysilicon (as presented in the single chip microphone process in Fig.5).

First a double chip microphone process is analyzed:
The thermal oxide layer was grown on both sides of the bonded wafer. An etching mask is used to create the membrane and the back-plate. The membrane and back-plate are finalized with TMAH solution etching. Finally, using HF, the BSG sacrificial layer has been removed. Aluminium electrodes are created.
This process is depicted in Fig.4.

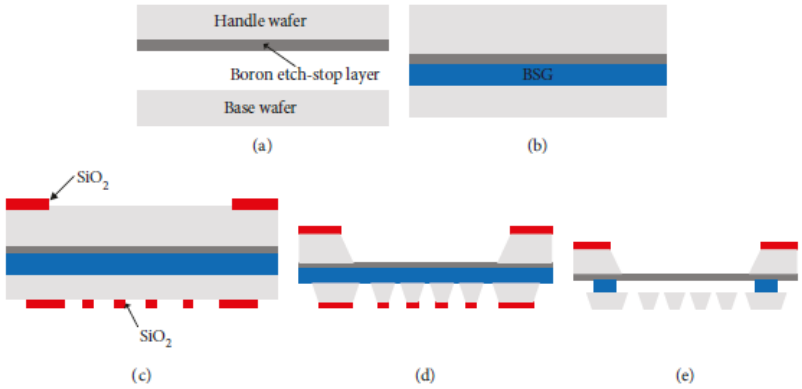


Figure 4: MEMS double chip Silicon-based Microphone process[6].

Regarding a single chip microphone process:
A p-type <100> silicon wafer was oxidized on both sides. The use of this oxide lies in the fact that it will insulate the electrodes. The membrane is deposit and patterned.
Another oxide layer deposition was performed.
A second polysilicon back-plate layer was deposited. This back-plate is perforated to properly manage the air flow. Silicon nitride was deposit and the contact holes have been etched. The top electrodes (poly-silicon and aluminium electrodes) are isolated by the silicon nitride layer.
Thermal oxide on the back side and a protective low-temperature oxide (LTO) on the front side were deposited in order to protect the wafer form etching in a TMAH solution. TMAH etching was performed. Therefore, the sacrificial layer was etched. A microphone with perforated back-plate is obtained as shown in Fig.5. This process is depicted in Fig.5.

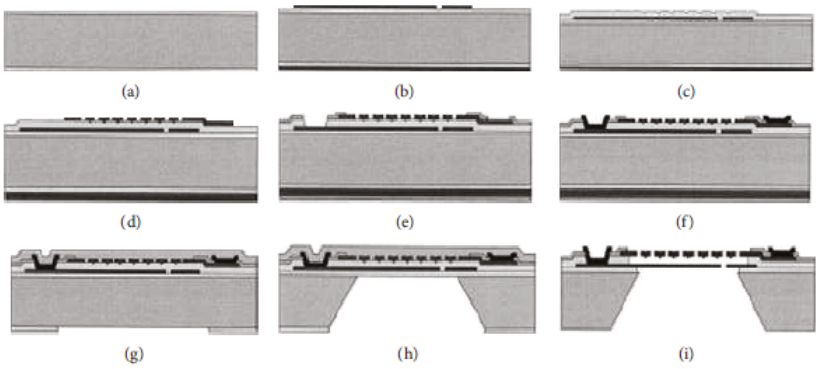


Figure 5: MEMS single chip Silicon-based Microphone process[6].

2.2 Graphene

Carbon atoms create a sigma covalent bond with other atoms. A sigma covalent bond is when atoms share electrons equally between one another. When equally sharing electrons, atoms create a particularly strong bond. Each carbon atom has 4 electrons which the atom is willing to share with other atoms to form covalent bonds. 3 of these electrons can be shared with another carbon atom to create the graphene honeycomb structure (Fig.6). The reason behind the formation of rings of six atoms of graphene is that these arrangements are the most thermally stable for carbon. Therefore, graphene is considered to be the strongest and thinnest material known in the Universe[7].

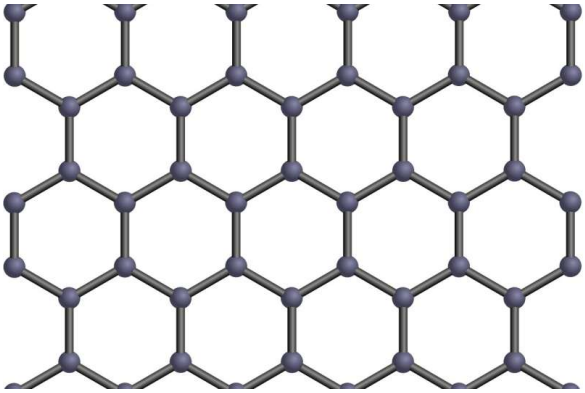


Figure 6: Graphene Honeycomb Structure

Since only 3 electrons are used for the creation of the covalent bonds, 1 electron of the carbon atom will be free to move. This property increases the conductivity of the material making graphene more conductive than copper. Consequently, the electrical properties of graphene are related to the charge carriers of graphene. These carriers are characterized by a very large intrinsic mobility. Furthermore, the carriers present an effective mass of zero. Therefore, graphene is able of tolerate current densities of greater magnitude than the current densities found in normal conductor materials[7].
In addition, the electron transport in graphene can be modeled as a Dirac function[7], allowing the study of quantum phenomena.

Because of its particular bonds, graphene is a 2-dimensional crystal. Therefore, graphene is considered a 2D material. Graphene is made up of a single layer of carbon atoms arranged in a 2D honeycomb structure. This property is particularly interesting in audio application where membranes are made of much thicker materials. Using a thinner material will allow a larger mechanical response to the same sound pressure leading to higher sensitivity.
As mentioned above, each atom in graphene is only connected to its 3 neighbors. In fact, graphene can be thought of as two surfaces without any intermediate bulk. Similarly to the surface of graphite, graphene can absorb various atoms and molecules (such as NO_2, OH, K and NH_3). Furthermore, the surfaces of graphene are not perfectly flat, but characterized by corrugations. These corrugations are typically in the nanometer range[7]. Therefore, graphene is a suitable material for different types of sensing applications.

Graphene can be produced in several ways. The most commonly used are epitaxial growth on silicon carbide (SiC), the Chemical Vapor Deposition (CVD) and mechanical exfoliation. In terms of the quality and yield of the final device, the CVD process is considered the most reliable and scalable [8].
CVD requires a carbon source as $CH_4 - H_2$ in gaseous form. The pyrolysis of materials generates carbon. The dissociated carbon atoms will generate a graphene structure on a suitable catalyst (a material used to enhance the reaction, without itself being consumed). Hence, the use of CVD for the growth graphene will require the use of a catalyst. Most of the catalysts are CMOS incompatible (such as copper. CMOS compatible materials can be produced with the same manufacturing processes used for silicon). Molybdenum is a CMOS compatible catalyst for graphene.

2.3 Graphene-based Condenser Microphones

The microphone structures presented above can be used for the realization of graphene-based condenser microphones. In these devices, the membrane is made of graphene and the graphene layer can be transferred or made on top of the same substrate (in a transfer-free method). Initially, the transfer method will be explored as studying these fabrication methods will provide an overview that will allow for the implementation of the transfer-free method used in the presented work. Three different methods for the transfer of graphene membranes were investigated. These processes have highlighted the methodology used for the transfer of graphene membranes and how the lack of a completely atomized system reduces the yield of the process.

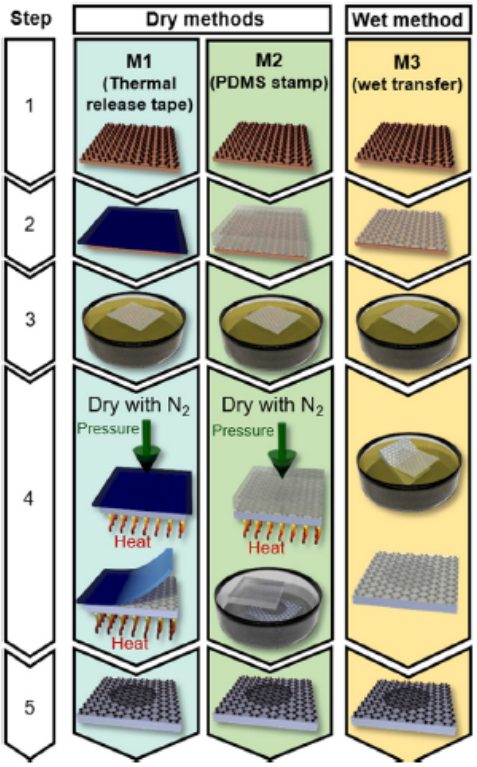


Figure 7: Transfer of Graphene on Prefabricated Holes [9].

In the work presented in [9], a device substrate is created. To this end, a 1.6 μm thermal oxide layer was etched. The etching was made to create 1.4 μm deep cavities. The diameter size of the cavities ranged from 2 μm to 10 μm. Chromium/gold (Cr/Au) contacts have been incorporated into the wafer surface. The contacts have been prefabricated to minimize any further processing after the graphene transfer. In parallel, CVD-graphene was grown on a copper foil. In [9] copper was used as a catalyst. Three transfer methods were presented in [9]:

Method 1: Thermal Release Tape Method:
200 nm of PMMA is coated on the graphene/copper substrate. Thermal release tape is applied on the graphene/copper substrate and the copper foil is etched. The graphene is transferred to the cavity by pressing the tape on the substrate. The substrate is heated so that the thermal tape can be released. The tape is peeled off and photoresist is applied. PMMA and graphene are patterned. Finally, the PMMA layer is removed. Using this method, only 8.3% of the membranes survived.

Method 2: Wet Transfer Method:
PMMA is coated on the graphene/copper stack. The copper is etched and the graphene layer is left floating in DI water. The device substrate is used to lift the graphene layer out of the water. Photoresist is applied. PMMA and graphene are patterned. Finally, PMMA is removed. Using this method, only 6.3% of the membranes survived.

Method 3: PDMS Stamp Method:
The PMMA is coated on the graphene/copper stack. A photoresist layer is applied on top of the PMMA. A PDMS stamp (a piece of polydimethylsiloxane) is pressed onto the stack. The PDMS stamp will act as a support layer. Copper is etched. The stack graphene/copper is pressed on the device substrate and the photoresist between the PMMA layer and PDMS layer is stripped. As a result, the PDMS layer is lift off the device substrate. The graphene is patterned and the PMMA layer is removed. Using this method, only 11% of the membranes survived.

For all these processes, the narrower the cavities, the higher the yield. Furthermore, the yield can be increased by using a stack of multi-layer graphene [9]. On the other hand, the yield is generally low due to the use of transferred graphene, making it impossible to apply this process in large-scale production.

The device in [8] was tested with the probe station. Furthermore, an LCR meter in a frequency range from 20 Hz to 20 kHz (audio range) was performed to measure the capacitance. The Eigenvalue analysis was performed and showed that the frequency response and the capacitance value will depend on the amplitude of the biasing voltage. To ensure that the diaphragm does not stick to the back plate, the bias voltage must not exceed the pull-in voltage [8].
It was observed that the transferring process creates a disordered graphene structure with corrugations in the nanometer range. This increases the thickness of the layer, thereby reducing the mechanical response of graphene.
Using a probe station measurement, a small conductivity of 0.2 nA was measured [8]. The LCR meter has shown a trend of the capacitance value in the audio range which agrees with the following equation [8]:

$$C = \frac{1}{2\pi f X_C} \tag{10}$$

Therefore, the capacitance value increased with increasing dimensions of the diaphragm. Also, the largest diaphragm (the one with largest diameter) showed the highest sensitivity. On the other hand, the smallest diaphragm (the one with smallest diameter) showed the longest flat frequency response.
To detect the change in capacitance, a bias voltage is applied to fixed electrode and membrane. As described in [1], the performance of a MEMS microphone will depend on the lowest input sound pressure level (input SPL). Furthermore, in the range of human hearing (20Hz to 20kHz), a flat response of the output signal relative to the sound pressure frequency is desirable. On the other hand, some microphones used in the audio industry as voice recorders, will feature higher sensitivity for frequency up to 1 kHz. In addition, using 60-layers of graphene will make the system 15 dB more sensitive than a commercial silicon-based microphone [8].
The following table will characterize the frequency behavior the sensitivity of transferred graphene-based capacitive microphones:

Device Name	**Membrane Thickness**	**Membrane Diameter**	**Frequency range**	**Sensitivity**
Wittmann, Sebastian, et al. Device[10]	5 nm	40 μm	From 5 Hz to 700 kHz	Comparable with commercial Si-based condenser microphones
Geim, Andre Konstantin Device[7]	20 nm	N.A.	From 20 Hz to 500 kHz	High
Todorovic, et al. Device[11]	25 nm	10 mm	From 0 Hz to 6.5 kHz	10 dB higher than commercial Nickel-based condenser microphones
Woo, et al. Device[12]	600 nm of graphene + 3 μm of PMMA	2.65 mm	From 5 Hz to 7 kHz	High
Graham S. Wood Device[13]	210 nm of graphene/poly(methyl methacrylate)	7 mm	From 100 Hz to 20 kHz	-47.5 dB V

Table 1: Frequency response & Sensitivity of Transferred-Graphene Microphones.

2.3.1 Fabrication of Transferred Graphene-Based Condenser Microphone

In the audio system presented in [13], the membrane shows a circular shape as depicted in Fig.9
The use of PMMA as a support layer result in less displacement when the membrane is vibrating. This will

prevent contact between the membrane and the fixed bottom electrode.
The fabrication process is depicted in Fig.9.
At first, the substrate is realized from a 75 mm Silicon wafer with a 380 μm thickness. Using PECVD, a 77 nm layer of silicon dioxide is deposited on the wafer. Lift-off process is used to pattern aluminium. This creates the fixed electrode. Using PECVD, a 8.8 μm layer of silicon dioxide was deposit. Photolithography is applied. The oxide is etched to create the cavity. A 10:9 solution of $NH_4F : CH_3COOH$ was used. The electrical connection has been created. The wafer is diced.

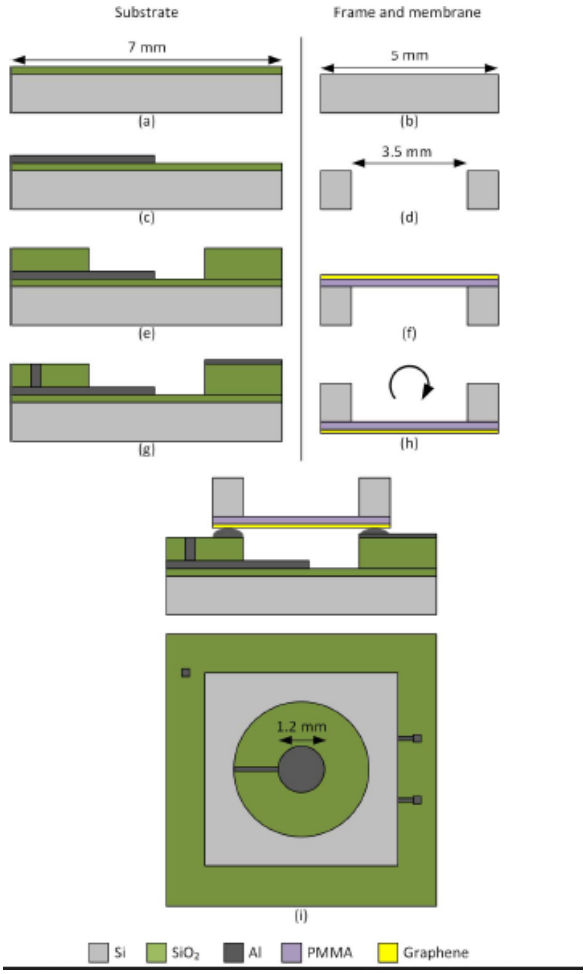


Figure 8: Transfer Graphene-based Microphone process[13].

There is a second phase of the process described graphically in Fig.9.b. Here, a frame to suspend the membrane is fabricated[13]. Another silicon wafer was patterned using photolithography. Using deep reactive ion etching (DRIE), the cavities were etched through the wafer. The wafer has been diced. Using CVD, a layer of membrane material was prepared. The layer was cut and positioned on the frame. To properly fix the membrane on the wafer, a small amount of deionized water was applied to the frame. The deionized water itself was subsequently evaporated using an hotplate. Droplets of silver adhesive were applied to the substrate chip. These droplets will help adhere the frame to the substrate chip and create a connection from the graphene layer to the bonding pads. The frame has been placed on top of the substrate chip[13].
The electrode is positioned under the membrane center. This will maximize the capacity change. Therefore, the output signal will be maximized.
The final chip size reported is 7 mm x 7 mm with a sensitivity between 0.1 mV/Pa and 10 mV/Pa, in a frequency range of 100 Hz up to 20 kHz[13].

Vapor Hydrofluoric acid etching can be employed to suspend graphene layers [14]. This was demonstrated in [14] where a silicon wafer was used as a substrate and thermal oxide was grown, followed by LPCVD of SiNx. In this process, the sacrificial layer was made of LPCVD TEOS, while the structural layer was realized with multi-stacked layers of polysilicon and silicon-on-insulator (SOI). The latter was patterned with photolithography and

etched through RIE. Subsequently, a metal conductive layer (Al-1% Si) was sputtered and patterned. Finally, VHF etching was used to successfully release the mechanical layer. Additionally, in the work presented in [15], free-suspended graphene was processed using VHF etching. Therefore, the VHF etching technique has previously been used with positive results. The relative advantage of VHF is that it is a dry etching technique, so it will avoid the use of liquid materials. The absence of liquids will minimize the capillarity forces introduced during the etching. Capillarity forces are inter-molecular forces between a liquid and the surrounding solid surfaces that could induce a collapse in the membrane layer [14].

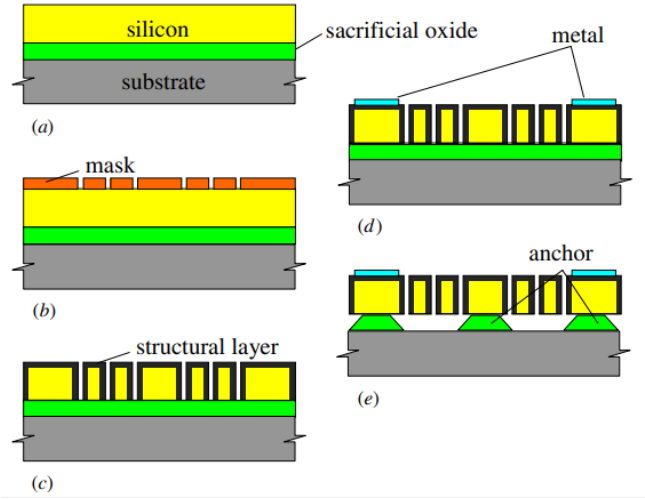


Figure 9: Transfer Graphene-based Microphone process using VHF for the release of the mechanical layer [14].

2.3.2 Graphene-based Capacitive Microphone Conclusions

As far as performance is concerned, a small footprint can be achieved at the price of a small reduction in sensitivity. Additionally, graphene microphones are capable of capturing sounds in the 20 Hz-0.5 MHz range. This range covers the human audible region and part of the ultrasonic region[7]. Also, the bias voltage must be tuned to avoid membrane collapse.
Regarding fabrication, growing graphene using CVD results in the best performing suspended graphene layers.[8][16]. A crucial parameter in fabrication is yield. The yield can be improved by decreasing the width of the cavity underneath the graphene layer at the expense of a reduction in sensitivity. Furthermore, the yield can be improved by using a stack of multi-layer graphene[9]. On the other hand, transferred graphene generally has a low yield [9] and creates disordered graphene structures [8]. Additionally, the transfer process increases polymer contamination, wrinkling, cracking and delamination [15]. These problems increase the difficulty of implementing the process in large-scale production.

2.4 Graphene-based Transfer-Free Condenser Microphones

To overcome the problems related to the transfer of graphene membranes, a transfer-free process is being investigated. This process should allow for the large-scale production of graphene-based condenser microphones. In [16], a graphene-based pressure sensor is presented. This device is not an actual microphone (it is a Pirani pressure sensor), but its process flow can be analyzed to understand how to implement transfer-free graphene in a capacitive microphone. The first step performed in [16] is the creation of the sacrificial layer by wet oxidation of silicon. Later, the molybdenum is sputtered and etched. CVD of graphene is performed. The chrome/gold (Cr/Au) lift-off is then performed to create the electrical contacts. By wet etching the sacrificial layer, the membrane is suspended and pressure can be detected. The process is depicted in Fig.10. Therefore, the use of a transfer-free process will reduce the number of steps and materials required for the fabrication of a microphone, thus enabling large-scale production. Additionally, the use of graphene will change the performance of the device, allowing for miniaturization.

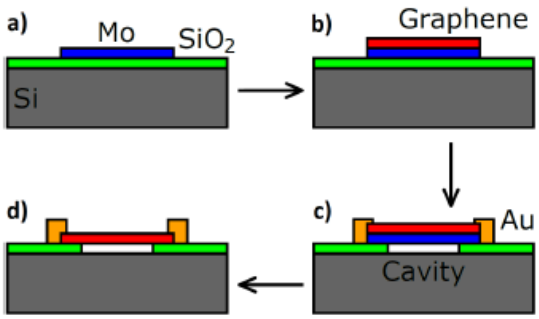


Figure 10: Fabrication Process for Transfer-free Suspended Graphene Pressure Sensor[16].

3 Device Simulations & Concept Design

Multiphysics simulations are presented in the following chapter. Comsol software was used and 2 models were modified to create a suitable model for graphene-based capacitor microphones. Subsequently, the design of the mask will be considered and the variations in the structures presented will be analyzed in detail. In addition, the materials used will be discussed and general considerations about the flowchart used will be given.

3.1 Simulations In Comsol Environment

From the analyzed papers and some state-of-the-art devices, it was possible to build a Table of parameters that characterize a Capacitive microphone. The values are depicted to better understand the results of the simulations and will help customize the model. Furthermore, the acquired results can be compared with those obtained in the literature. This will be necessary to better understand the results achieved during simulations. In Tab.2, "dBV" is "dB" relative to 1 V (such that 0dBV = 1V), while "dBFS" are the decibels relative to Full Scale (where 0 dBFS equals the maximum possible level).

Table 2: Silicon-Based Condenser Microphones

State Of The Art Si-Based Condenser Microphone Parameter List					
Device Name	**Sensitivity**	**Membrane Diameter**	**Gap height**	**Frequency range**	**Pressure Range**
STMicroelectronics IMP23ABSU MEMS Microphone	$-38dBV \pm 1dB$	1.625 mm	packaging of 1.08 mm	up to 80 kHz	$>$ than 130 dBSPL
STMicroelectronics MP23DB02MM MEMS Microphone	$-26dBFS \pm 1dB$	1.625 mm	packaging of 1.08 mm	up to 4 kHz (for MFM)	$>$ than 122 dBSPL
Infineon Technologies XENSIV™ MEMS Microphones IM69D130	$-36dBFS \pm 1dB$	2 mm	packaging 1.2 mm	up to 1 kHz	$>$ than 130 dBSPL
STMicroelectronics MP34DT06J MEMS Microphone	$-26dBFS \pm 1dB$	1.56 mm	packaging 1.3 mm	NA	122.5 dBSPL
STMicroelectronics IMP34DT05 Omnidirectional MEMS Microphone	$-26dBFS \pm 1dB$	1.56 mm	packaging 1.3 mm	NA	122.5 dBSPL

Table 3: Graphene-Based Condenser Microphones

Graphene-Based Condenser Microphone Parameter List						
Device Name	**Membrane Materials**	**Sensitivity**	**Membrane Diameter**	**Gap height**	**Frequency range**	**Pressure Range**
Mohd Ambri Mohamed's Capacitive Microphone [8]	Graphene	-89 dB	40 μm	200 nm	20 Hz - 20 kHz	up to 93.97 dBSPL
Graham S. Wood, Micro-Fabricated Graphene-Based MEMS Microphone [13]	Graphene + PMMA	-40 dBV	3.5 mm	8 μm	100 Hz - 20 kHz	from 70 dBSPL to 80 dBSPL
SeongTak Woo, High Sensitivity Microphone for a Hearing Aid [25]	Graphene + PMMA	-30 dB to 35 dB	4 mm	10 μm	up to 7 kHz	up to 94 dBSPL
C. N. Berger, Ultra-thin graphene–polymer heterostructure membranes [17]	Graphene + Parylene	NA	from 2 to 12 μm	NA	Low	192 dBSPL – 204 dbSPL

A graphene condenser model was created from the device parameters obtained in the previous chapter. Unfortunately, some inconsistencies were found during the simulation phase. The use of parameters from different articles led to some errors in the solution of the system of the equation that Comsol was handling. This was related to the fact that some articles analyzed a single-layer graphene structure, while other articles considered, for example, a mixture of graphene and parylene that will require a different topography than that used for a graphene-only membrane. Therefore, all geometries were fine-tuned to get a working device, but a trade-off could not be found. Hence, a study on consistent data sets was conducted.
Papers [23] and [24] consider a multi-layer graphene structure. The consistency of these data led to some acceptable solutions in the simulator.
The following table illustrates the set of parameters used during simulations. Some parameters are defined in a certain range. When the model is built, the parameters used will be considered in the range described and the value will be obtained from the works analyzed during the literature review.

Table 4: Simulation Parameters

Graphene-Based Microphone set of Parameters			
Name	**Value**	**Description**	**Unit**
H_m	From 200 nm to 100 μm	Air Gap Thickness	From nm to μm
R_{mem}	From 6 μm to 2 mm	Membrane Radius	From μm to mm
G	3*H_m	Slit Gap width	From nm to μm
T_{m0}	358 N/m [23]	Membrane Static Tension	N/m
E_m	965 GPa	Membrane Elastic Modulus	GPa
t_m	From 5 nm to 10 nm	Membrane Thickness	nm
ρ_m	2267 kg/m^3	Membrane Density	kg/m^3
V_{pol}	From 1 V to 100 V	Target Polarization Voltage	V
R_{preamp}	100 GΩ	Preamplification Output Impedance	$G\Omega$
v_m	From 0.17 to 0.23	Membrane Poisson Ratio	None

3.1.1 Comsol Model number 1: Generic Silicon Condenser Microphone

Using the guide provided on the official Comsol website [26], a model for a condenser microphone was created. The model was designed considering the following assumptions:

The deformation of the membrane will be linked to the variation of the electrostatic force during the charging of the capacitor, neglecting the pressure underneath the membrane. Furthermore, the variation in external pressure (linked to the uniform acoustic signal applied) was modeled with p_{in}.
The parameters used in the model are shown in the following table [26]. These parameters are illustrated in Fig.11

Table 5: Silicon-Based Capacitive Microphone Parameters

Silicon-Based Microphone set of Parameters		
Parameter Name	**Value**	**Parameter Description**
H_m	$18\,\mu$m	Air Gap Thickness
R_{mem}	2 mm	Membrane Radius
G	$54\,\mu$m	Slit Gap width
T_{m0}	3150 N/m	Membrane Static Tension
E_m	221 GPa	Membrane Elastic Modulus
t_m	$7\,\mu$m	Membrane Thickness
ρ_m	$8300\,\mathrm{kg/m^3}$	Membrane Density
V_{pol}	100 V	Target Polarization Voltage
R_{preamp}	$1\,\mathrm{G}\Omega$	Preamp. Output Impedance
v_m	0.4	Membrane Poisson Ratio

The membrane is backed by H_m and by the back-electrode. Since H_m is small ($18\,\mu$m), thermal and viscous losses play an important role in the characterization of the device. Therefore, a thermoviscous acoustic interface was considered in the model. The back-plate combined with the membrane creates a capacitor which is externally polarized by V_{pol} and R_{preamp}. Therefore, the membrane surface will experience a Q_m charge. The air gap acts as a damping layer for membrane movements. When the air gap changes, a voltage change is induced. This voltage will be the AC output of the microphone.
In the presented model, the membrane is designed using the "membrane interface" from the "structural mechanics module". The surface load on the membrane will be given by the sum of p_{in}, the internal pressure ($p = p(\vec{r})$, given by the thermoviscous acoustic model), and the electrostatic force related to the Maxwell surface stress ($\vec{n}\tau$). Furthermore, the incident pressure is considered uniform on the membrane.
Using the linear-perturbation frequency-domain solver, the system can solve a fully coupled problem. A stationary model defines the linearization point. The complete system of equations will then be linearized and solved around the linearization point. This will determine the harmonic small-signal response.

At first, the linearization point will be determined. To do so, the static model that determines the shape of the membrane after the application of V_{pol} has been solved. Since the capacitance value will be determined by the geometry of the system, this value was determined by a moving mesh.
The second step focused on solving the linear-perturbation frequency-domain model. This model is used to describe the time-harmonic small-signal deformation of the membrane. In addition, the model defines the interaction with the fluid inside the microphone. These interactions are described by a thermoviscous acoustic interface in the frequency domain. The constructed model is depicted in Fig.11. Moreover, the model can describe the change in sensitivity relative to frequency (as depicted in Fig.12). Finally, the model can describe the deformation of the membrane in 2D and 3D (as represented in Fig.13 and Fig.14). The x-axis in Fig.13 represents the displacement. The same displacement can be observed as parameter "U" in the model described in Fig.11.

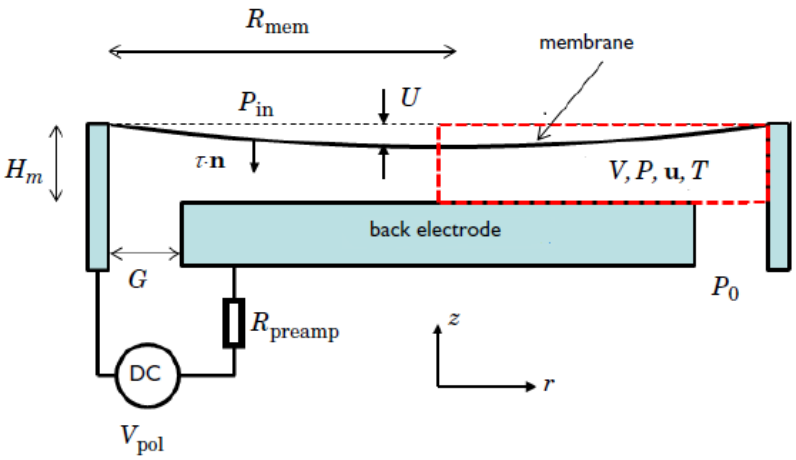


Figure 11: Model used for the first simulation from[26].

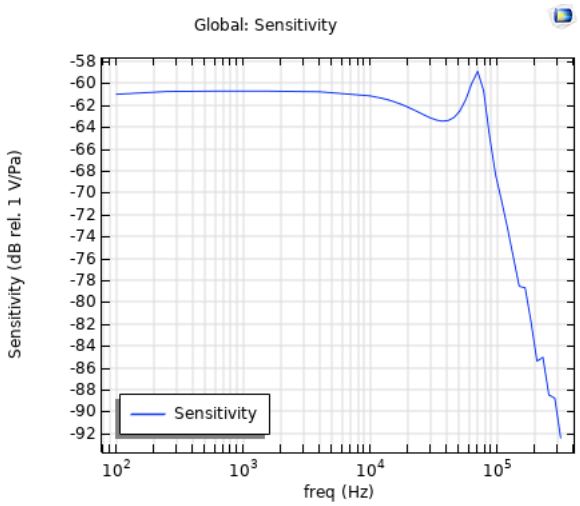


Figure 12: Sensitivity vs Frequency

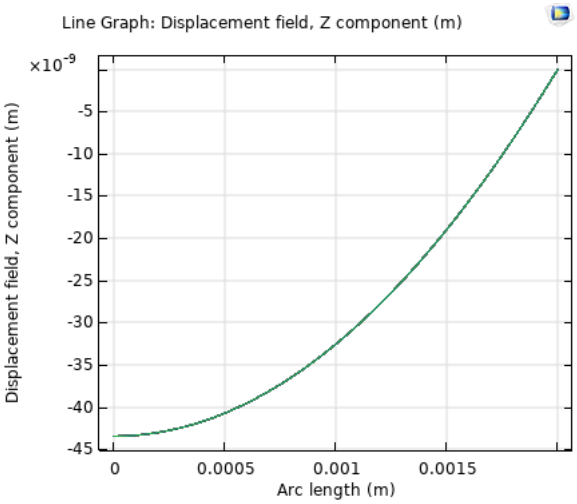


Figure 13: 2D surface displacement

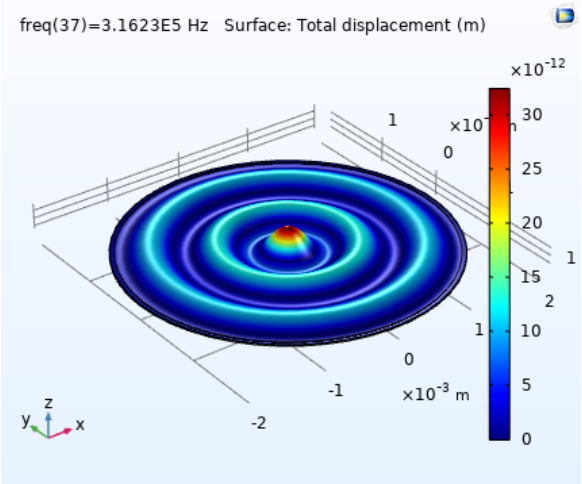


Figure 14: 3D harmonic membrane deformation at a frequency of 0.3 GHz

The drawback of the presented model is the absence of a perforated back-plate. The 3D deformation should occur at frequencies outside the audio bandwidth. Therefore, after a frequency sweep, it was calculated at a frequency of 0.3 MHz, since the magnitude of the deformations before that frequency was negligible. Furthermore, the displacement should occur (for a certain frequency) in one direction only. If the displacement occurs in 2 directions simultaneously, the change in capacitance could be compensated by the positive and negative deformations on the z-axis. In the simulations conducted, the displacement is present in only one direction of the z-axis. On the other hand, the used model may have some problems with small membranes. If the membrane radius is too small, HPF (high-pass filter) behavior will occur. This could be related to the over-damping imposed by the model. The smaller the air gap and the radius/thickness of the membrane, the greater the thermoviscous effect. This issue will be corrected by using a better-refined model that will deal with electrical lumping.

3.1.2 Comsol Model number 2: Condenser Microphone with Pressure Under the Membrane

The subsequent model is a finite element model. There is a quiescent (static) polarization (DC charge) analysis and deformation analysis in the model. The model combines static and dynamic analyses[27].
Small-signal finite element analysis of the dynamics and the thermoviscous acoustic behavior of the membrane is present in the model. The small-signal model is solved using a lumped model (an electric equivalent) combined with the finite element model[27].

Concerning the previous model, the constants describing an elastic solid (E_m elastic modulus and v_m Poisson's ratio) are neglected since the Lumped-element model (electric equivalent model) will be considered. The error introduced by neglecting Em and vm is corrected by the dynamic model that will consider the membrane displacement and by the lumped equivalent model. The external incident pressure (P_{in}) and the release pressure (P_0) are now considered. Furthermore, the areal membrane density (ρ_{ms} given by $\rho_m * t_m$; areal density is the mass per unit area) will be considered. The air gap thickness (H_m) can be reduced compared to the silicon-based model[13]. The maximum value used for H_m is 10 μm (which is 8 μm smaller than that used in model number 1). The membrane radius (R_{mem}) is now in the micron range (not in the millimeter range) and the membrane thickness (t_m) is in the nanometer range (not in the micron range) due to the large displacement generated when the pressure hits the graphene membrane. Finally, the values of T_m and ρ_m are fixed to the graphene ones.

As explained in the previous model description, the membrane and the back-electrode create a capacitor that is externally polarized by a DC voltage source. As the gap between the membrane and the back-electrode changes, a voltage change is induced which is coupled to a very large resistive load. The circuit used for the coupling is depicted in Fig.15.

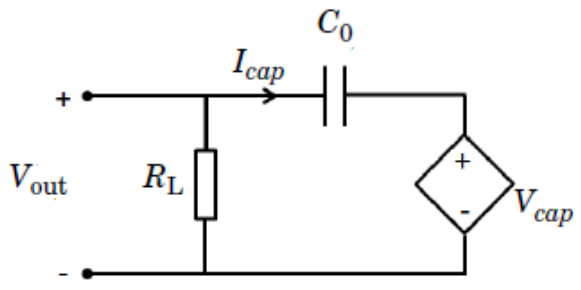


Figure 15: Coupling circuit form[27]

The sensitivity will be equal to the ratio of the open-circuit output voltage V_{out} and the inlet pressure P_{in}[27].

$$S = 20log(\frac{V_{out}}{P_{in}}) \tag{11}$$

Subsequently, a small-signal analysis of the electrical behavior of the condenser is led. The total charge will be equal to the sum of the quiescent charge Q and the small-signal charge q. The distance between the membrane and the back-electrode is the sum of the internal distance H_m, the quiescent average deformation $U_{0,av}$ and the small-signal deformation U_{av}. The total voltage will be given by the sum of the open-circuit output voltage V_{out} and the polarization voltage V_{pol}[27].
Considering a fixed air gap g and an area A, the parallel plate capacitance will follow the subsequent equation[27]:

$$C = \frac{\epsilon_0 \epsilon_1 A}{g} \tag{12}$$

If g is not fixed but changes its value through an average deformation U_{av}[27]:

$$C = \frac{\epsilon_0 \epsilon_1 A}{H_m + U_{0,av} + U_{av}} = \frac{\epsilon_0 \epsilon_1 A}{H_m + U_{0,av}} \Big(1 - \frac{U_{av}}{H_m + U_{0,av}}\Big) O(U_{av}^2) \tag{13}$$

Using a first order approximation, the average deformation will follow the subsequent equation[27]:

$$U_{av} = \frac{1}{A} \int U dA = \frac{2}{R_{mem}^2} \int_0^{R_{mem}-G} U(r) r \, dr \tag{14}$$

Since Q=CV and C follow the equation previously defined, the total voltage can be expressed as follows[27]:

$$V_{pol} + V_{out} = \frac{Q + q(t)}{C} \approx \frac{Q}{C_0} \Big(1 + \frac{U_{av}(t)}{H_m + U_{0,av}}\Big) + \frac{q(t)}{C_0} \tag{15}$$

Switching to the frequency domain and imposing $V_{pol} = \frac{Q}{C_0}$, the following equation can be found[27]:

$$V_{out} = \frac{I_{cap}}{i\omega C_0} + \frac{u_{av} V_{pol}}{i\omega \big(H_m + U_{0,av}\big)} \tag{16}$$

Where the average membrane velocity u_{av} is defined by the following equation[27]:

$$u_{av} = \frac{1}{A} \int u_m dA = \frac{2}{R_{mem}^2} \int_0^{R_{mem}-G} u_m(r) r \, dr \tag{17}$$

Where u_m is the axial membrane velocity. To complete the model, a study on the electrostatic force f_{es} is required. The force applied on the membrane as normal surface stress will be equal to $\frac{f_{es}}{2\pi R_{mem}^2}$ where the electrostatic force will follow the next equation[27]:

$$f_{es} = -\frac{V_{pol} I_{cap}}{i\omega \big(H_m + U_{0,av}\big)} \tag{18}$$

Note that the integrals considered above are calculated over the area of the membrane backed by the back electrode summed to a possible small correction. This small correction is used for edge effects. These

considerations are particularly important when the back electrode has holes. In this model, the back electrode is flat and uniform, so the damping effect will be present. After various simulations, the parameters depicted in Tab.6 were found to be suitable for the project due to the deformation and sensitivity obtained.

Table 6: Graphene Microphone parameters for Simulations

Graphene-Based Microphone set of Parameters				
R_{mem} (μm)	50	100	300	500
H_m (μm)	2.5	5	5	5
t_m (nm)	7	7	7	7
P_{in} (Pa)	1	1	1	1
T_m (N/m)	0.45	0.45	0.45	0.45
ρ_m (kg/m^3)	2267	2267	2267	2267
ρ_{ms}	$\rho_m * t_m$	$\rho_m * t_m$	$\rho_m * t_m$	$\rho_m * t_m$
V_{pol} (V)	1	1	1	1
P_0 (Pa)	0	0	0	0
R_L $(M\Omega)$	100	100	100	100
G	3*H_m	3*H_m	3*H_m	3*H_m

The graphene membrane thickness was considered to be 7 nm. This value was chosen based on the average thickness [15] value obtained with the same recipe and reactor that will be used for the presented thesis. Therefore, this parameter was fixed. Additionally, the mechanical parameters (T_m, ρ_m) were kept unchanged during the various simulations.
Concerning the geometry, if H_m (air gap thickness) is too small, the pull-in phenomenon may occur and the membrane may collapse. Concerning the membrane radius (R_{mem}), decreasing this value will allow for miniaturization. On the other hand, if R_{mem} decreases, the mechanical sensitivity will decrease (eq.8), thus decreasing the overall sensitivity. To improve sensitivity, H_m can be reduced (eq.8), but the pull-in phenomenon can occur. Therefore, a trade-off was found using the values depicted in Tab.6. Furthermore, thinner gaps were not investigated, since no information was known regarding the graphene sagging at the end of the fabrication. The presented thesis is based on the feasibility of the fabrication, thus it was important to obtain a working process flow with reasonable gaps to be able to observe a suspended diaphragm. Once the membrane will be suspended and the critical parameters of the transfer-free, wafer-scale graphene-based capacitive microphone will be known, the air gap thickness can be reduced.
The polarization voltage was kept at 1 V and the load resistor was kept at 100 MΩ to improve consistency in the various simulations. The load resistor value was changed between the 2 models. This is because less resistance was used in the model description of the second model. These parameters will be modified once the specifications of the final graphene microphone are known. On the other hand, as depicted in Fig.16, it has been shown that, as the polarization voltage increases, the sensitivity value can improve. The polarization voltage was changed from 10 V to 1 V, leading to a sensitivity reduction of approximately 20 dB. In Fig.16, the same membrane has been considered (same geometry and same parameters), but the polarization voltage has been changed from 10 V to 1 V leading to a change in the sensitivity. The air gap thickness was set to 5 μm.

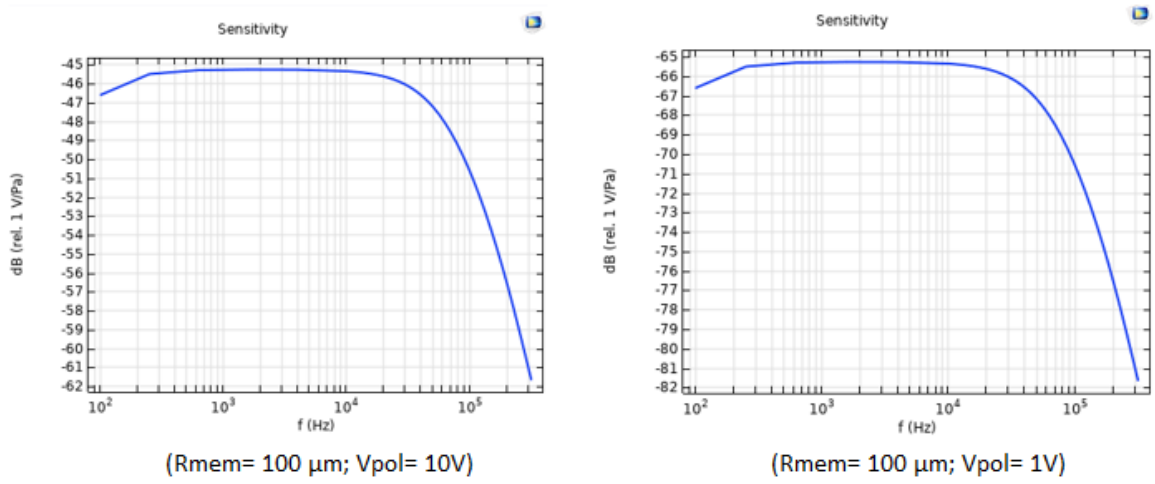


Figure 16: Polarization Voltage VS Sensitivity of a Graphene-based Microphone

Concerning the obtained sensitivity, the behaviors corresponding to silicon-based and graphene-based microphones are illustrated in Fig.17. An over-damped behavior was present in the sensitivity characteristic. The absence of the resonance frequency in the depicted behaviors is linked to the presence of a graphene membrane which will impose an over-damped behavior on the system, thus moving the resonance frequency out of the frequency bandwidth of interest[23].

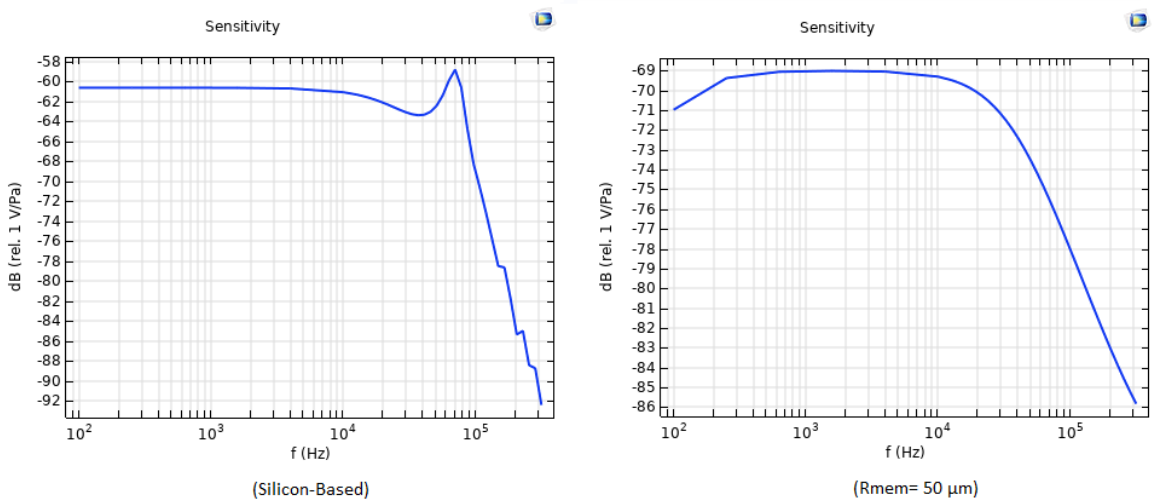


Figure 17: Sensitivity of Silicon-based and Graphene-based microphones simulated with model number 2.

Concerning the membrane static deformation, this deformation should show a “curved trend” for pressures at frequencies below 20 kHz. All oscillations should begin at frequencies outside the audio bandwidth.
As depicted in Fig.19, the oscillations will start at a frequency of approximately 97 kHz (96.977 kHz), which is in line with the mechanical requirements. Oscillations in the silicon membrane begin earlier as the system is not over-damped due to the absence of a graphene membrane which does not introduce the over-damped behavior. On the x-axis, the "r-coordinate" stands for the arc length (distance between two points along a section of a curve) of the membrane radius (Fig.18). The convergence point will be the center of the membrane and the deformations have been considered over the entire radius at different frequencies.

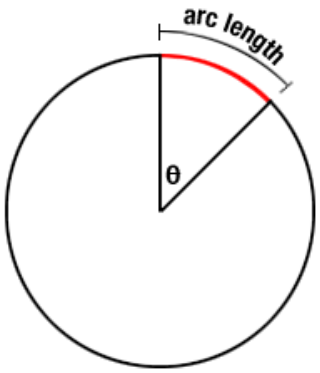


Figure 18: Arc Length of a Circumference.

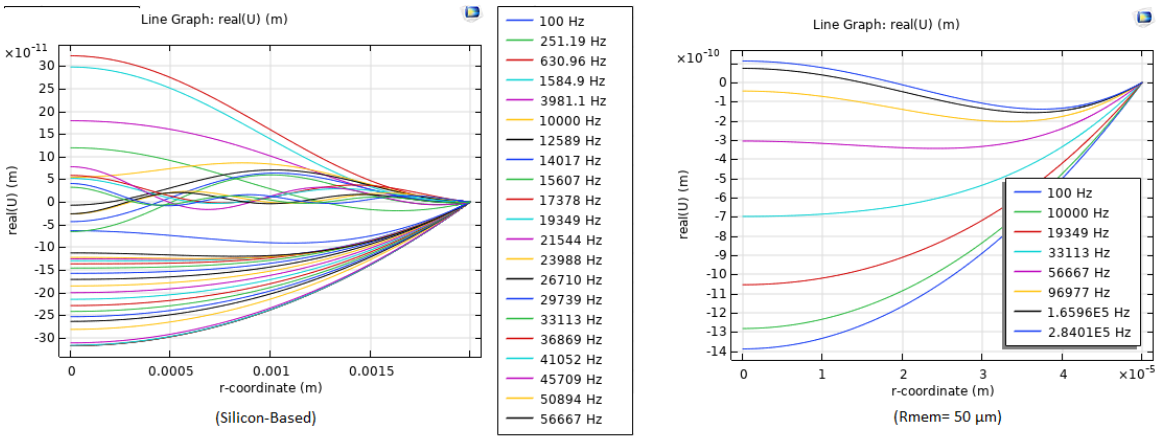


Figure 19: Membrane Static Deformations

The 3D displacement should occur at frequencies outside the audio bandwidth. Furthermore, the displacement should occur (for a certain frequency) in one direction only. If the displacement occurs in 2 directions at the same time, the capacitance change might be compensated by the positive and negative deformations on the z-axis. The plotted simulation was swept in a frequency range from 100 Hz to 0.3 MHz. The displacement was negligible until the last frequency was considered and the result at this frequency was plotted in Fig.20. Therefore, the 3D displacement was visible at 0.3 MHz which is outside the audio bandwidth. These requirements were satisfied by the simulations as depicted in Fig.20.

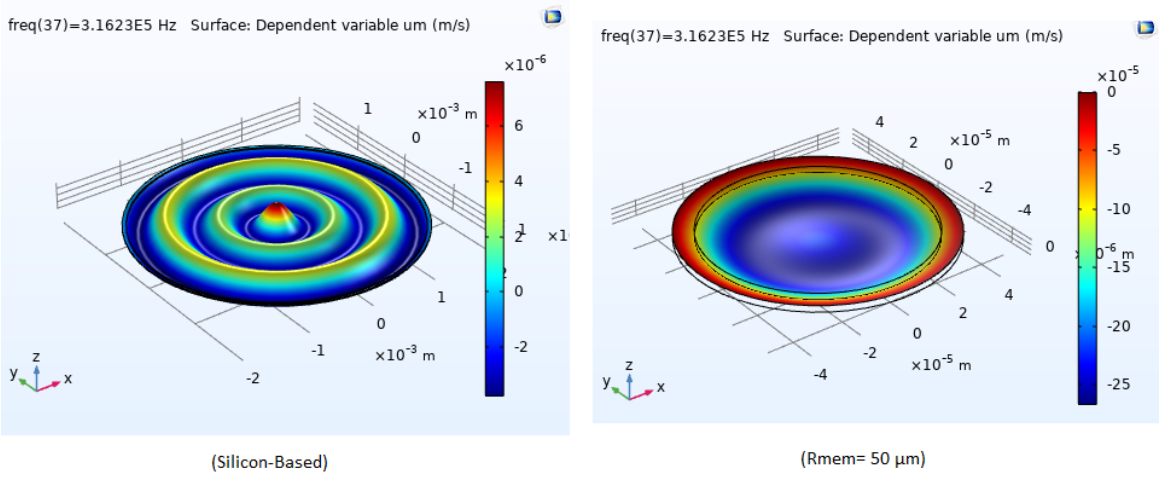


Figure 20: Membrane 3D Displacement

Concerning the average membrane deformation, the input pressure was set to 1 Pa. As depicted in Fig.21, on the y-axis the graph considered the $log_{10}(|U|)$. Therefore, the numbers on the y-axis represent the exponent value of the exponential with base 10. Since values of around -9 and -10 are present on the y-axis during simulations, the mean deformation will be in the range of $[10^{-10}; 10^{-9}]$. Therefore, the average displacement will be of the order of the nanometers. This result is in line with the mechanical requirements[24]. The analytical approximation plotted in Fig.21 is obtained from Eq.14.

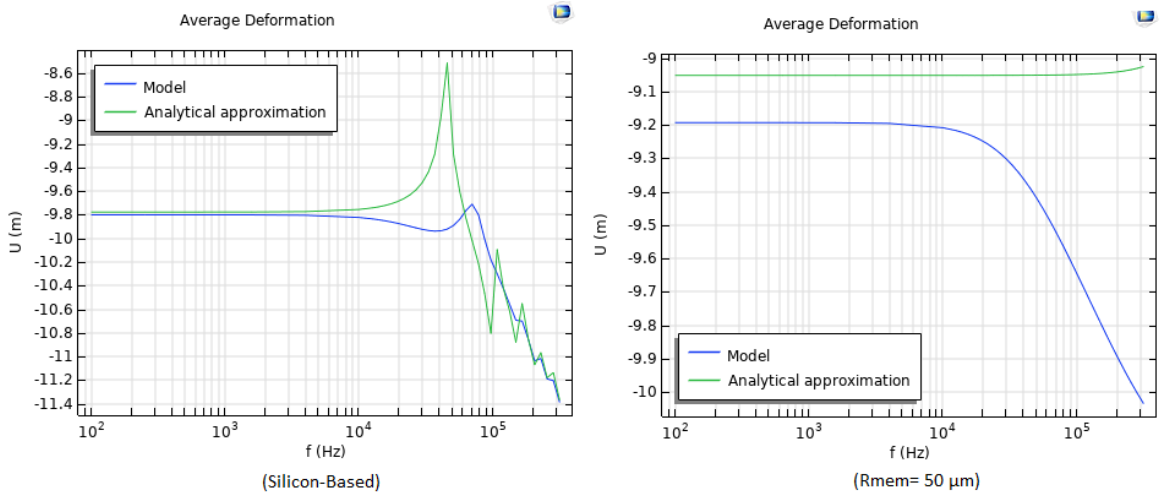


Figure 21: Average Membrane Deformations

3.2 Process Flow Design

During the design of the process flow, the process steps and the materials used were projected to successfully suspend a graphene layer. As mentioned above, a condenser microphone is made of 2 conductive layers separated by a dielectric. One electrode will be fixed and one will act as a diaphragm (thin diaphragm will be realized in graphene). The dielectric employed was air, so a cavity must be present between the top and bottom electrodes to create the condenser structure. The bottom electrode was designed to control the airflow. The realization of venting holes avoided the presence of compressed air that behaves like a mechanical damper. Furthermore, the back-plate must be conductive to allow a reading of the back electrode.

The materials used are now analyzed in detail. Considering the topside of the wafer, wet oxidation is initially performed to insulate the future polysilicon back-plate. Subsequently, the SiNx layer is deposited. This layer is used as an etching mask for the polysilicon when the backside etching will be performed. Then, a polysilicon layer is deposited for the realization of the bottom electrode. Polysilicon is generally used as a conductive layer since, during processing, a large thermal budget is required for CVD of graphene. It is therefore not possible to use a generic conductor since it cannot survive high temperatures and is CMOS incompatible in the general case. On the other hand, polysilicon, which is CMOS compatible, is not strongly affected by high temperatures and can be used as a conductive layer. Hence, polysilicon was used in the process for the realization of the back-plate. Therefore, this layer was doped and annealed to reduce its resistivity.

A TEOS sacrificial layer is then deposited. When this layer is etched, the layer of graphene will be suspended. Finally, the SiNx on the top surface will be used as a support for the graphene layer and as a mask for future Vapor Hydrofluoric acid (VHF) etching and Cr/Au (20/200 nm) is evaporated by electron-beam evaporation to create the metal contacts. This material has been used because, in previous works [15][9], its correct functioning (such as good contact and conformal coating) has been demonstrated. Regarding the backside, the TEOS layer is used as a mask for future Deep reactive-ion etching (DRIE). The final device structure is illustrated in Fig.22.

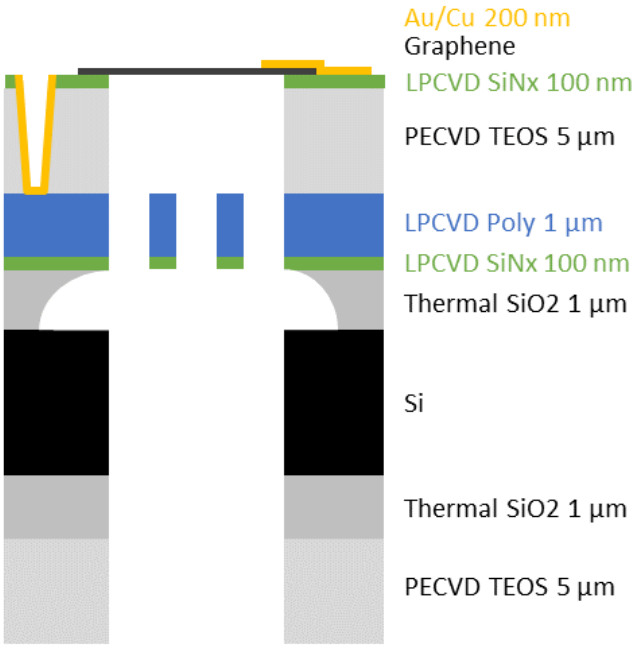


Figure 22: Final Device Cross Section

3.2.1 Process Considerations

During processing, all the micro-fabrication steps are realized by photolithography. To correctly fabricate the condenser microphone, a study on the various step of the process was led. The final process will require 7 masks to be completed. The final device is depicted in Fig.22. The first mask employed in the process was the one used to create the venting holes in an LPCVD SiNx layer, followed by the second mask, used for the realization of the bottom electrode in an LPCVD polysilicon layer. The third mask was used for the etching of the SiNx layer to create openings for future membranes. The back cavity which, with venting holes, will ensure proper airflow, was realized using mask number 4. This mask will be used to etch PECVD TEOS, thermal oxide, and silicon. The fifth mask defined the contact openings for the bottom electrode and was used to etch LPCVD SiNx and PECVD TEOS. The geometry of the membranes will be defined by mask number 6, used to etch a molybdenum layer. The last mask is used to create the contact layer realized in Cr/Au. All the mask are illustrated in Fig.23 and the final process flow is depicted in Fig.24.

1. Silicon Nitride Holes for the realization of Venting Holes.
2. Polysilicon definition for the realization of the bottom electrode.
3. Opening in the SiNx (used as VHF mask) to clamp the graphene in the SiNx area and suspend it in correspondence with the TEOS.
4. Backside opening for future silicon and sacrificial TEOS etching.
5. Openings for sacrificial PECVD annealed TEOS layer.
6. Mo pattern to create the designed geometry on the future graphene layer.
7. Lift-off of the metal contacts.

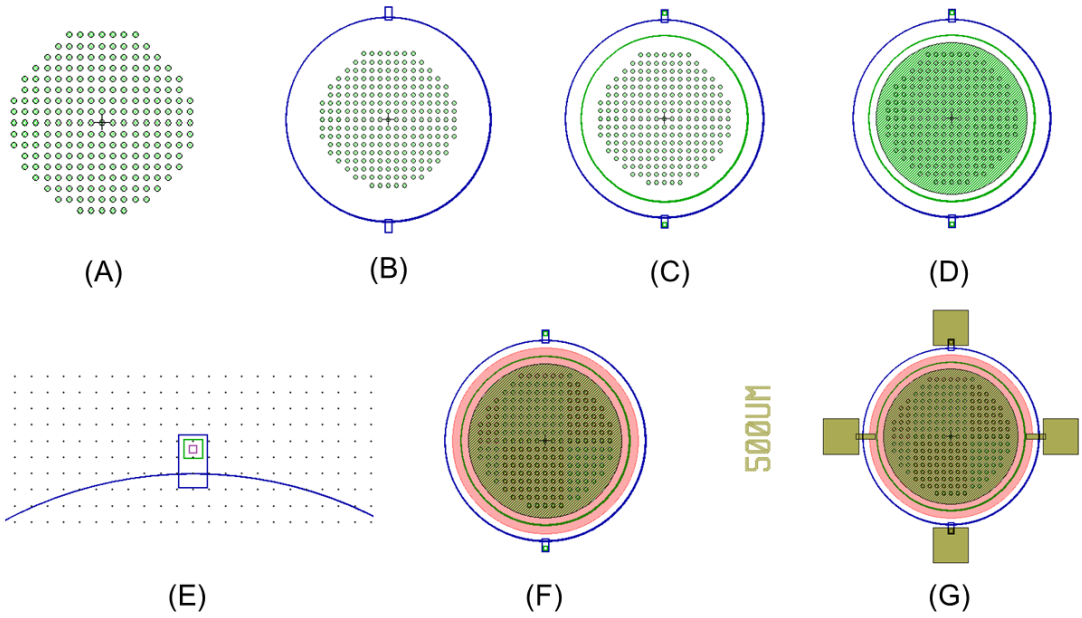


Figure 23: Mask used. (A): Venting hole. (B): Back-plate. (C): Opening for membrane. (D): Back cavity. (E): Contact opening for bottom electrode. (F) Molybdenum etching. (G): Cr/Au contact pads.

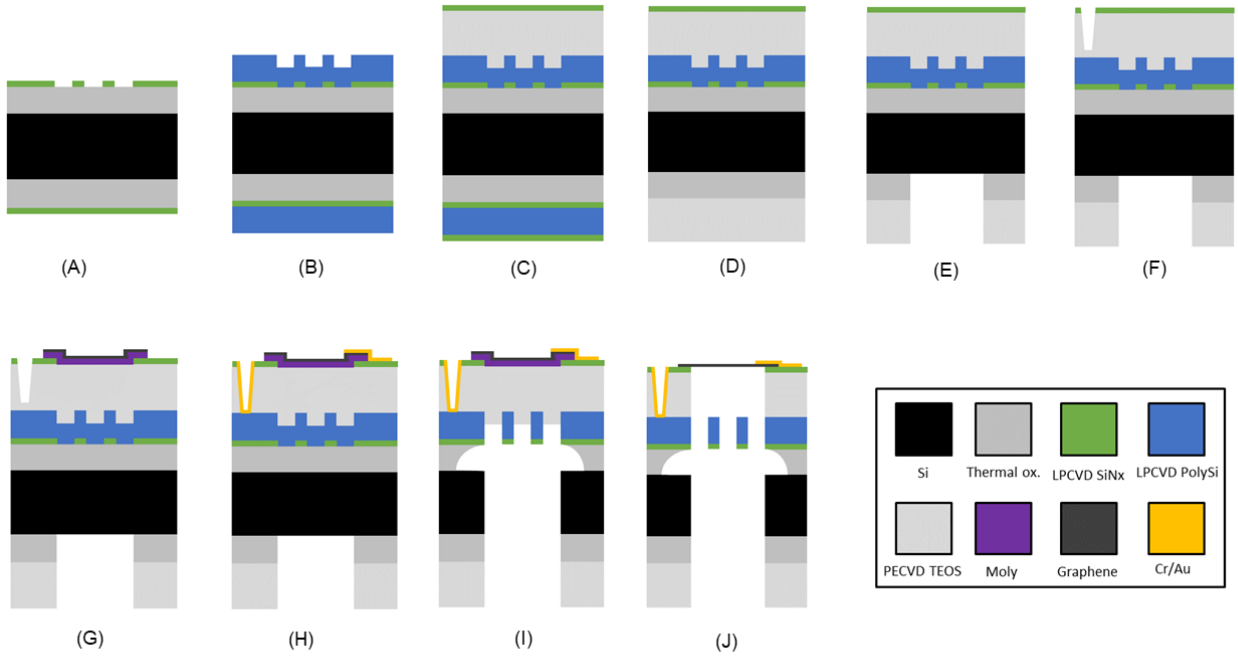


Figure 24: Final Process. (A): Wet oxidation was employed for thermal oxide growth; 100 nm of LPCVD SiNx were grown and patterned using dry etching. (B): 1000 nm of LPCVD polysilicon were deposited and patterned by RIE. (C): 5 μm of PECVD TEOS were deposited and annealed. LPCVD of 100 nm of SiNx was performed. (D): Back-side Dry etching of 100 nm SiNx, 1000 nm polysilicon, and 100 nm SiNx. PECVD of 5 μm of TEOS. (E): Back-side dry-etching 5 μm of TEOS and 1 μm of thermal oxide. (F): Top-side dry-etching of 100 nm of SiNx and 2.5 μm of TEOS followed by wet-etching of 2.3 μm of TEOS for the back-plate contact opening. (G): Dry-etching of 100 nm of SiNx. Sputtering and dry-etching of 50 nm of molybdenum. CVD of Graphene. (H): Wet etching remaining 200 nm of TEOS and Cr/Au (20/200 nm) electron-beam evaporation followed by lift-off. (I): DRIE of silicon, wet etching of 1000 nm of thermal oxide and DRIE of polysilicon. (J): Wet etching of 50 nm of molybdenum and VHF etching of 5 μm of sacrificial TEOS.

The thickness of the wafer should be small enough to allow the realization of small openings through DRIE performed on the backside of the wafer. A P-type 525 ± 15 μm wafer was used for this purpose. Thereafter, $1\,\mu$m of thermal oxide was grown to create an electrically insulating layer for the doped polysilicon layer. Furthermore, 100 nm of LPCVD Si-rich, Low-Stress SiNx will be deposited on the wafer surface to create a future masking layer for DRIE of the polysilicon layer. The etching of the polysilicon layer will be performed on the backside, so this SiNx layer will protect the polysilicon. This etching is performed on the backside because the graphene layer on the top-side must be suspended, so all the layers below the graphene will be removed. Additionally, as the graphene will be deposited on the top-side, back-side etchings will preserve the membrane layer. The first photolithography mask was used to create venting holes (each hole has a diameter of $10\,\mu$m or $20\,\mu$m, depending on the design) on the silicon nitride layer. The etching of this layer is performed by dry etching (in a fluorine chemistry).

$1\,\mu$m of LPCVD polysilicon was grown on the wafer. This layer was used as the bottom electrode. Therefore, the layer should be doped to realize a conductive layer (Doping concentration: $10^{19}/\text{cm}^3$; Doping dose: $5 * 10^{15}/\text{cm}^2$; Substrate depth: $1\,\mu$m; Diffusion Temperature: $1000\,^\circ$C; Ion energy: 45 keV; Dopant species: Boron). For this purpose, the resistivity of the LPCVD polysilicon layer should be small. The LPCVD polysilicon layer was annealed for 1 hour for dopant activation and recombination of the crystal lattice. The bottom electrode was patterned using dry etching. A deposition of $5\,\mu$m of PECVD TEOS was conducted. This thickness will define the final thickness of the air gap which will therefore be $5\,\mu$m. The PECVD TEOS layer was annealed for 1 hour at $950\,^\circ$C for the recombination of the crystal lattice which will avoid bending and braking of the wafer. This layer is used as a sacrificial layer to suspend the mechanical layer (in this case realized with graphene). LPCVD of 100 nm of SiNx was performed to create the graphene support layer. This layer will be also used as a VHF mask.

Dry etching was performed on the back-side to remove 100 nm of LPCVD SiNx, $1\,\mu$m of LPCVD polysilicon, and 100 nm of LPCVD SiNx. A deposition of $5\,\mu$m PECVD TEOS was conducted on the back-plate and dry etching was performed on the back of the wafer to create the opening for the future DRIE of Silicon. Hence, on the wafer back-side, $5\,\mu$m of PECVD TEOS and $1\,\mu$m of thermal oxide were etched. Thereafter, the realization of the back electrode openings was performed. Therefore, a mixture of dry and wet etching was performed to achieve a conformal coating of the metal at the sidewalls. An anisotropic etching would result in straight sidewalls that will not allow proper sidewall coverage of the metal layer, thus not connecting the bottom electrode to its pads. Therefore, a tapered sidewall structure should be obtained. The slope of the sidewall will allow good contact on the bottom electrode. To this end, 100 nm of SiNx and $2.5\,\mu$m of PECVD annealed TEOS were dry-etched, followed by wet-etching of $2.3\,\mu$m of PECVD annealed TEOS. 200 nm of TEOS on the top-side (out of the 5000 nm) were not etched to prevent the penetration of carbon atoms into the doped polysilicon layer, thus creating an unwanted silicon carbide (SiC) layer.

On the top-side, 100 nm of SiNx were dry etched to create the openings for the future membrane, followed by sputtering and dry etching of 50 nm of Molybdenum. Graphene was deposited by CVD at $935\,^\circ$C with CH_4 supplied to the tool for 20 minutes, and the remaining 200 nm of PECVD TEOS were etched. Cr/Au (20/200 nm) electron-beam evaporation and lift-off were performed. The molybdenum layer on the top-side was etched in hydrogen peroxide and the silicon layer was etched using DRIE from the back-side. Then, the wet etching of the thermal oxide layer was performed, and the polysilicon was etched using DRIE. VHF was performed to etch the sacrificial TEOS layer. The vapor has penetrated through the venting holes creating a suspended membrane. The obtained device is depicted in Fig.22.

3.2.2 L-Edit Designs

Due to the number of simulations performed in the Comsol environment, different membrane diameters were considered during the mask design. The use of different diameters for the membrane is related to risk mitigation. With different diameters, it will be possible to identify an optimal dimension, in terms of performance and yield, that can be implemented in future designs. The diameter values of the membranes implemented in the L-Edit mask design are the following.

1. $500\mu m$
2. $400\mu m$
3. $300\mu m$

4. $200\mu m$
5. $100\mu m$
6. $60\mu m$
7. $50\mu m$

Since a vast number of variations of the same geometry were required for risk mitigation, different structures for the same geometry were designed. Several variations of the same structure will indicate the most suitable solution for the capacitive microphone application. The list of variations is depicted in Fig.25.

Diameter	Venting holes 10um	Venting holes 20um	Gold Ring	Gold Pad	Ratio Area SiNx-Area VenintgHoles = 10	Ratio Area SiNx-Area VenintgHoles = 20	Ratio Area SiNx-Area VenintgHoles = 30	Ratio 10 & Gold Ring	Ratio 20 & Gold Ring	Ratio 30 & Gold Ring	Ratio 10 & Gold Pad	Ratio 20 & Gold Pad	Ratio 30 & Gold Pad	20um VH & Gold ring	20um VH & Gold Pad
500um	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
400um	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
300um	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
200um	✓	✗	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
100um	✓	✗	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
60um	✓	✗	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
50um	✓	✗	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗

Figure 25: Microphone Variations in L-Edit Environment

In all the variants presented, 3 macro categories can be identified: geometry, venting holes, and golden electrodes. The macro categories are studied as follows.
Concerning the geometry variations, The area of the membrane has been subject to several changes as it is necessary to identify the geometry that will avoid collapse or sagging of the membrane. Other than using the different diameters previously listed, a graphene diaphragm with a "trampoline" structure (as depicted in Fig.26) has been implemented in designs having 100 μm, 200 μm, 300 μm, and 400 μm diameters. This structure has been used in the literature to improve the membrane flexibility[15]. This variant is depicted in Fig.26.

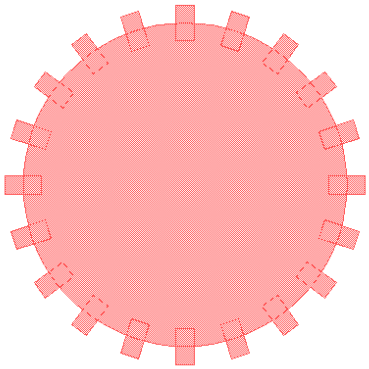


Figure 26: Graphene "trampoline" for capacitive microphone structures

As for the venting holes, the greater the area of the venting holes (given by the sum of the areas of each vent hole in the back-plate), the easier the access for VHF and future purging of residuals. Furthermore, with several different venting hole areas, it will be possible to identify the structure that will appropriately take care of the compressed air between the plates that will cause the mechanical damping.
Considering venting holes variations, the ratio between the Area of the SiNx and the Area of the Venting Holes has been changed to 10, 20, and 30. Therefore, the number of Venting Holes present in the back-plate was decreased to increase the value of the back-plate Area. Another variation for the design of a large membrane structure was to consider the diameter of the venting holes equal to 20 μm instead of 10 μm as depicted in Fig.27. The distance between the venting holes was kept equal to 20 μm in each design.
Hence, in Fig.25, two groups can be identified according to the type of venting holes present in the back-electrode. When the membrane diameter allowed to create 20 μm wide venting holes, the membrane was called

"large membrane". On the other hand, when this was not possible, the membrane was called "small membrane". The holes in the back-plate have a diameter of 10 μm (or 20 μm) and were placed at a distance of 20 μm. Therefore, large membranes were characterized by diameters of 500 μm, 400 μm and 300 μm, while small membranes were characterized by diameters of 200 μm, 100 μm, 60 μm and 50 μm.

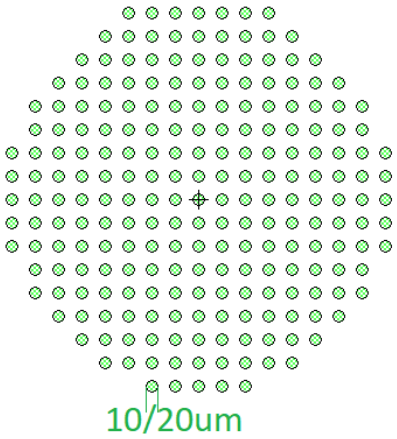


Figure 27: 500 μm Membrane Venting Holes

The electrodes are used for reading the capacitive output and clamping the diaphragm. Changes in electrode geometry will highlight whether clamping geometry can affect future suspension. The variations on the electrodes are now presented (Fig.28). A circular gold support was implemented in the structures to clamp the membrane. A radius difference of 2 μm between the gold and the membrane was considered to correct possible overlay problems. The structure of the circular gold support is depicted in Fig.28 (A).
A lateral gold support has been implemented in the structure to clamp the membrane during future release and also for electrical contact. The structure of the lateral gold support is depicted in Fig.28 (B).
All gold pads have been designed as squares with a lateral length of 100 μm. The pads connected to the back-electrode have been designed with an extension (which connects the gold pad to the back-electrode) having a width of 18 μm. The SiNx hole in the pad has not been centered to simplify the wire bonding step and presents a lateral length of 5 μm. Some holes in the TEOS have been implemented (with a lateral width of 12 μm) to impose a correct adhesion of the gold layer. The final structure of the gold pad connected to the back-plate is depicted in Fig.28 (C).
As for the pads connected to the Graphene membranes, once again the gold pads were designed as squares having a lateral length of 100 μm. The connection between the pads and the membranes was realized in gold having a width of 10 μm. This width value was chosen to avoid problems that could affect the final structure during the VHF etching step. The final structure of the gold pad connected to the membrane is depicted in Fig.28 (D).
When the wire bonding is performed, all pads will need to be at least 100 μm apart to obtain good connections and the same specification is required when measuring with a probe station. Therefore, the distance between the microphone and the pads has been changed to achieve a 100 μm spacing between each pad. The obtained distance between the pads varied from 115 μm to 230 μm as depicted in Fig.28 (E).
Furthermore, considering the large membranes (300 μm, 400 μm and 500 μm), the ratio of the areas (10, 20 & 30) was subsequently combined with the two new gold structures and these gold support structures were combined with designs having venting holes diameters of 10 μm and 20 μm.

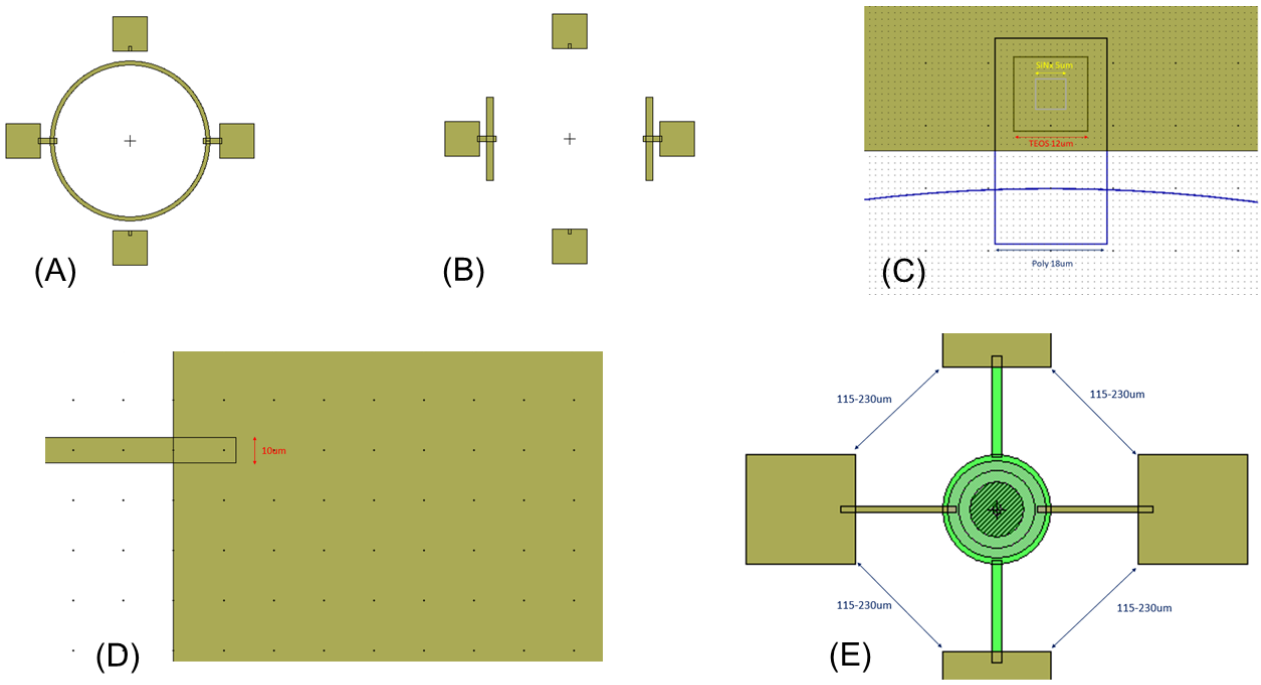


Figure 28: Electrodes Variations. (A): Circular gold clamping. (B): Lateral gold clamping. (C): Structure of the back-plate's gold pad. (D): Structure of the top-plate's gold pad. (E): Distance between the pads varied from 115 μm to 230 μm

Considering the distance between the membrane, the SiNx, and the back-cavity, when possible, a distance of 20 μm has been set (in a 50 μm membrane, such spacing was not feasible). The spacing in the 500 μm mask is depicted in Fig.29.

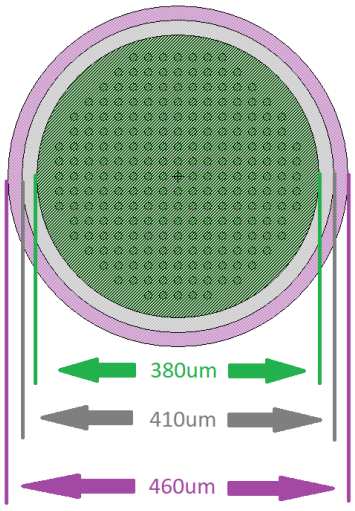


Figure 29: 500 μm Membrane, SiNx and Back-cavity spacing. The SiNx diameter is depicted in green. The TEOS diameter is depicted in grey. The Molybdenum diameter is depicted in purple. Each layer is at least 20 μm away from the next one.

The following image (Fig.30) illustrates the full mask design at the wafer level. On the left side of the wafer (green and blue chips) are the large membranes, while on the right side of the wafer (yellow and purple chips) are the small membranes. All the chips in white were not used for the presented design.

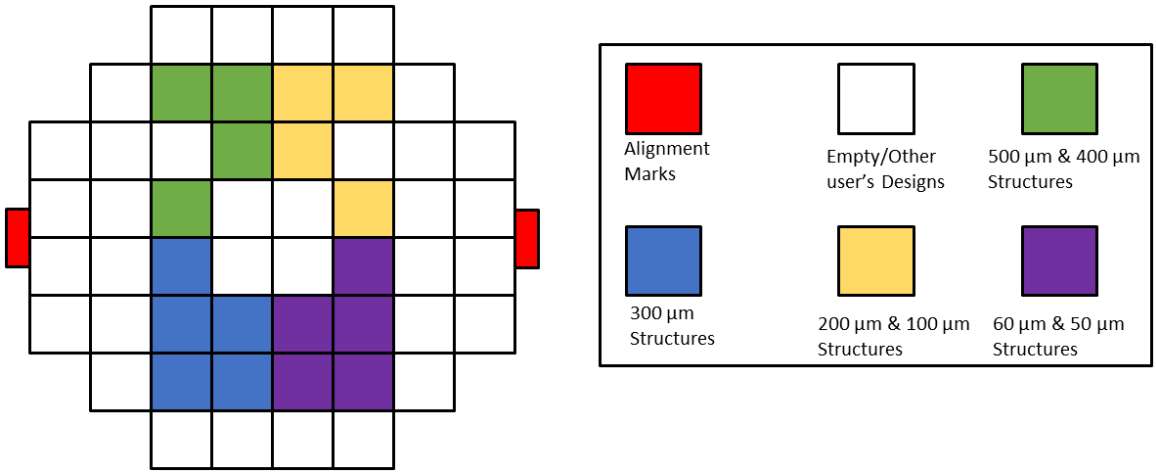


Figure 30: Wafer Level Mask Design. The withe chips were not used in the presented design. The alignment marks are illustrated in red. Chips containing 500 μm and 400 μm devices are depicted in green. Blue chips contain the 300 μm structures. The chips in yellow contain 200 μm and 100 μm devices, while the chips in purple contain 60 μm and 50 μm wide membranes.

4 Fabrication Results

In this chapter, the fabrication steps for the realization of a transfer-free, graphene-based capacitive microphone are presented. In addition, some tests necessary for the definition of the flowchart's crucial steps are described in detail in the appendix. In appendix D, VHF recipes will be tested to understand which is suitable for the release of graphene. A study on the penetration of VHF from the back-side openings and the graphene layer will be conducted. In addition, the etching of the TEOS, thermal oxide, and the silicon layer on the backside will be investigated to understand how the DRIE will affect the structure. This study was conducted because the thick silicon layer will be completely etched and could cause the wafer to crack or be damaged. This will be presented in appendix C.2.

4.1 Wafer-Scale Fabrication of Graphene-Based Capacitive Microphone

The following sections will discuss the flowchart used to make the final device presented in this work. All the steps will be described underlining the crucial ones. The final device will then be measured and characterized. The results of the characterization will be discussed in the next chapter.

4.1.1 Back-plate Implementation

A single-side polish, P-type silicon wafer was used. The wafer number was "MX19001-004" (hence, the wafer will be called "004" from now on). The zero layer was created by dry-etching and 1000 nm of thermal oxide were grown. The wafer was processed for the deposition of a layer of SiNx with a medium tensile stress (650 MPa) to prevent bending of the wafer. The target deposition was 100 nm of SiNx. Wafer 004 was dry-etched in a fluorine chemistry to create the venting holes on the SiNx layer. The wafer is depicted in Fig.31.

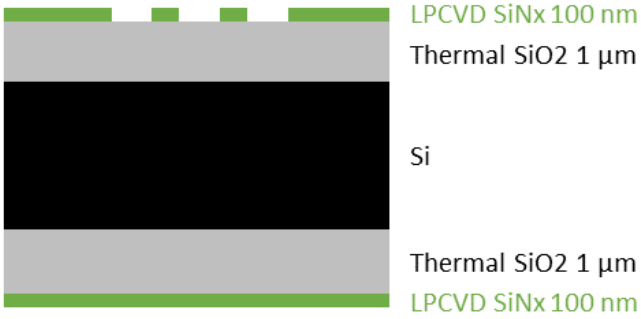


Figure 31: Wafer -004 after etching of the SiNx layer.

Subsequently, 1 μm of polysilicon was deposited on the wafer. The wafer was doped using a boron species with a doping dose of 10^{15}cm^{-2} and an energy of 45 keV (as discussed in the appendix "Polysilicon Doping Concentration" B). The wafer was annealed for 1 hour at 950 °C with a gas flow of Nitrogen and Argon and the sheet resistance was measured using the 4-probe station. The measured sheet resistance was 250 Ω/sq which is in line with the analytical result. Then, 1000 nm of polysilicon were RIE and the wafer was processed in Novellus to deposit 5 μm of TEOS. 004 was annealed for 1 hour at 1000 °C for lattice recombination of the PECVD TEOS layer. To minimize the wafer deflection, the same annealing recipe was used, but the final furnace temperature was reduced from 800 °C to 600 °C thus reducing the temperature excursion that the wafer underwent once the boat of the furnace was in the unloading state. Through naked eye inspection, it was possible to observe that the wafer was not bent, so it was possible to continue with the process as, if the wafer was bent, the tools were unable to handle it. Hence, 100 nm of SiNx were deposited. The obtained structure of wafer-004 is depicted in Fig.32.

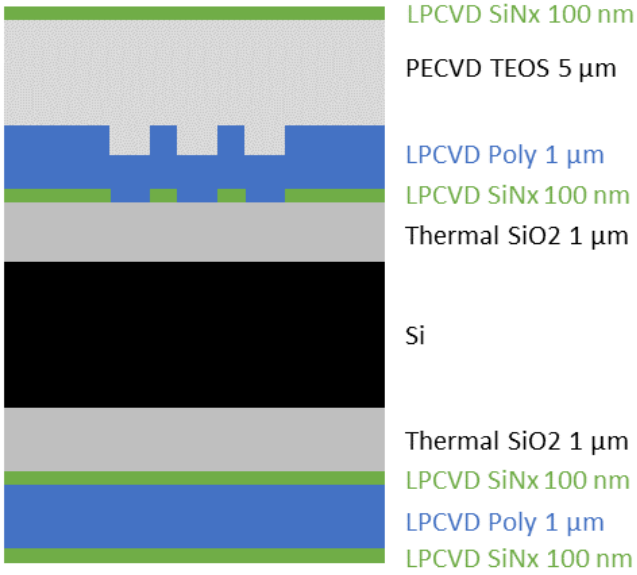
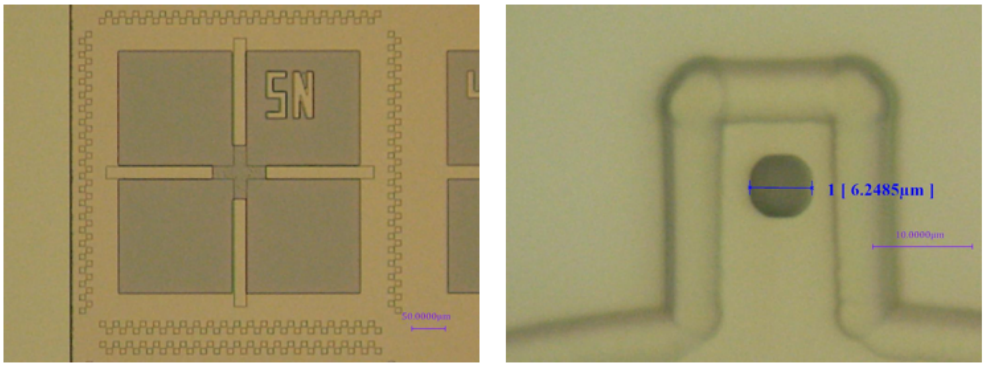


Figure 32: Wafer -004 after deposition of 5 μm of TEOS.

On the wafer backside, 100 nm of SiNx were dry-etched, followed by dry-etching of 1 μm of polysilicon and 100 nm of SiNx. Then 5 μm of PECVD TEOS were deposited on the back-side and the back-opening was realized by dry-etching 5 μm of PECVD TEOS and 1 μm of thermal oxide.

4.1.2 Contact Holes for the Bottom Electrode Implementation

Both dry and wet etching were performed to create the openings for the bottom electrode. To this end, wafer -004 was automatically coated with 8 μm of 10XT photoresist, photolithography was performed and the wafer was dry-etched. The SiNx layer on 004 was dry-etched to remove 100 nm with 100 nm of over-etching and the annealed PECVD TEOS layer was dry-etched. Since the TEOS layer thickness was equal to 5 μm, the dry etching was set to etch 2.5 μm. The wafer was rinsed in a solution of water and Triton and then etched in BHF for 27 minutes in 3 steps to etch 2.3 μm of PECVD annealed TEOS. Out of the total 5 μm layer of TEOS, 200 nm were not etched since the remaining 200 nm of TEOS will work as a protection during the CVD of graphene. This 200 nm will protect the polysilicon layer from carbon atoms, thus avoiding the creation of a SiC layer. To make sure that 200 nm of TEOS had not been etched, the wafer was inspected before and after BHF etching. If the TEOS layer has been fully etched, a color change should be observed after the BHF, but the color has not changed suggesting the presence of a TEOS layer. Additionally, the etching rate of TEOS in BHF was tested to ensure the presence of a residual layer of TEOS after the etching. After every step, the wafer was captured to monitor the etching and the halos created by the BHF. There was a small magnification in the hole diameter (the width designed for the contact openings for the bottom electrode was 5 μm), but the size of the enlargement was acceptable (Fig.33). The cross-section of the obtained structure is depicted in Fig.34.



(A) (B)

Figure 33: Wafer-004 after photoresist was stripped. (A) is the alignment mark. (B) is the measured width of the hole for the contact electrode.

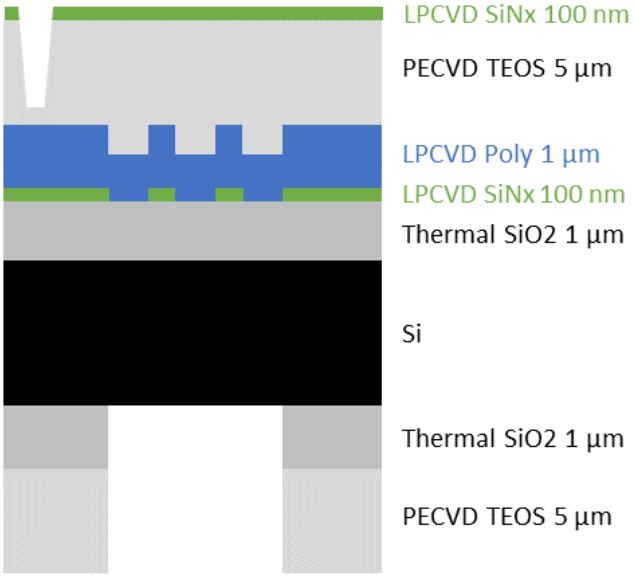


Figure 34: Wafer-004 after 5 μm of PECVD TEOS were deposited on the backside

4.1.3 Definition of the Top-electrode

The SiNx layer on wafer-004 was dry-etched to create the openings for the membrane. On the top side of -004, 50 nm of molybdenum were sputtered and dry-etched to create the geometry of the graphene membrane. Then, the wafer was inserted into the AIXTRON black magic tool for the CVD of graphene. The temperature was set to 935 °C, CH_4 was supplied to the tool for 20 minutes and the wafer was pre-annealed for 20 minutes in H_2. The graphene quality was promising. Raman tests on wafer -004 showed an $I_D/I_G < 0.6$. In some wafer spots, the I_D/I_G presented a value of 0.3 which is optimal for the study case presented[15]. These results will be analyzed in detail in the next chapter in section 5.4. The cross-section of the obtained structure is depicted in Fig.35.

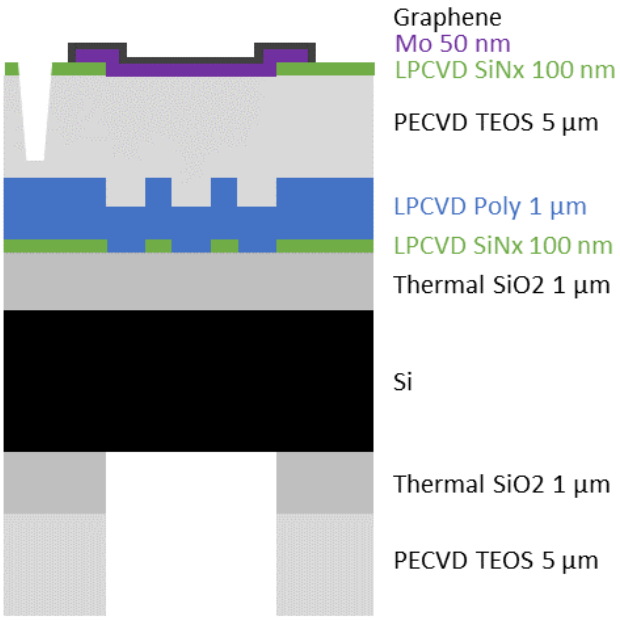


Figure 35: Wafer-004 after CVD of graphene.

4.1.4 Finalization of the Contact Holes for the Bottom Electrode & Gold Evaporation

Wafer -004 presented 5 μm of annealed PECVD TEOS, but in the contact holes openings for the bottom electrode, only 4.8 μm of oxide were etched. Therefore, wafer -004, was treated with HMDS for 10 minutes, manually coated with NLOF2020 photoresist, and baked for 90 seconds at 100 °C as described in C.3. The wafer was exposed with an energy of 78 mJ/cm^2 to pattern the top electrode, baked for 2 minutes and 15 seconds at 115 °C and developed in MF322 for 1 minute and 30 seconds. The remaining 200 nm of annealed PECVD TEOS were etched in BHF for 4 minutes and 45 seconds (with nearly 200 nm of over-etching). Before the wet etching, the wafer was kept in a solution of water and Triton for 5 minutes as discussed in C.2. After the wet etching, the wafer was rinsed in DI water and dried. The obtained structures were inspected using a digital microscope. Considering the dimension of the upper openings of the hole, the etched thickness, and the dimension of the lower opening of the hole, it was possible to estimate the tapering of the side walls. Fig.36 depicts the images acquired with a digital microscope.

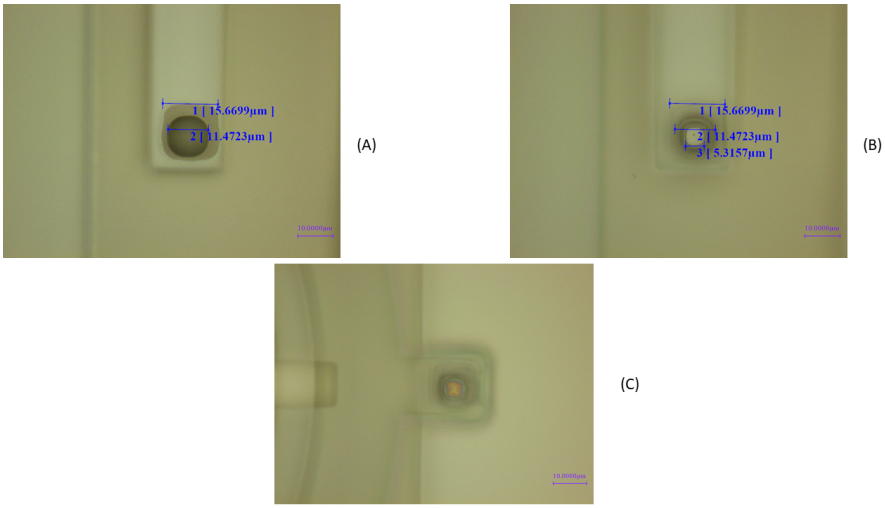


Figure 36: Wafer -004 after wet etching. (A): Top apertures width, SiNx opening for bottom electrode contact opening due to dry etching. (B): Top and bottom apertures width. (C): Hole where TEOS is still present. Some TEOS was still present in this opening since the bright grey color of polysilicon can't be observed.

The majority of the openings (around 80 %) showed an absence of the 200 nm of TEOS. Furthermore, the

computed tapering was equal to 58.3 °. This slope of the sidewalls allowed for good metal coverage.
A Cr/Au layer (20nm/200nm) was created by electron-beam evaporation and the Cr/Au lift-off was performed. The wafer featured a partial gold delamination where gold comes into contact with graphene. This could be related to the 200 nm of Au which created high stress in the layer causing its delamination. This was caused by different thermal expansion coefficients of gold, graphene, and molybdenum. Furthermore, a discontinuity occurred at the interface between SiNx and TEOS near the contact openings for the bottom electrode as depicted in Fig.37. This was related to using the same mask used to create the contact openings for the lower electrode when etching the 200 nm of TEOS. The use of a dedicated mask that will take into account the isotropic etching of the BHF can correct the discontinuity.

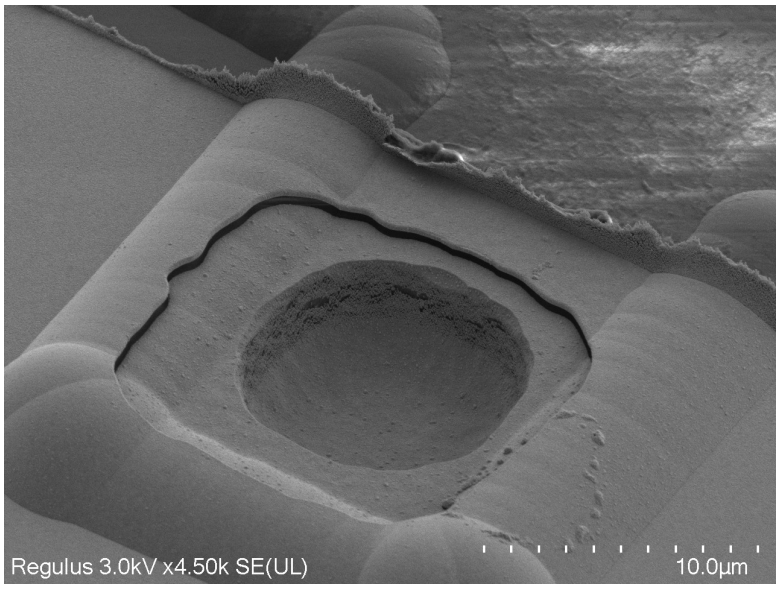


Figure 37: Wafer -004 after lift off. Gold presented a discontinuity.

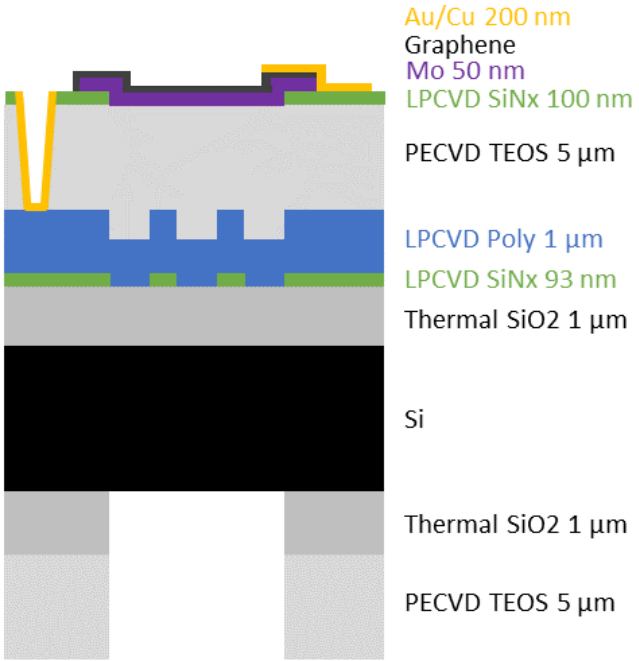


Figure 38: Wafer-004 after Cr/Au lift-off was performed.

4.1.5 Back-Side Etching for the Creation of the Venting Holes

Wafer -004 was plasma etched (using SF_6, C_4F_8 and O_2) in AMS110 to fully remove the silicon layer from the wafer's backside. Several runs were performed and in 50 minutes, all the 500 μm wide structures were fully open. Therefore, the next AMS110 run was short (5 minutes long) and performed to fully open the large residual structures. After this run, all the 400 μm wide structures were fully open, but most of the 300 μm were not. Therefore, another AMS110 run was performed with a time of 10 minutes. As a result, the 300 μm structures were almost fully opened. Therefore, the last run (lasting 5 minutes) was performed, thus achieving a final etching time of 70 minutes.
Wafer-004 was washed in a mixture of water and Triton for 5 minutes (for the reasons discussed in C.2). The wafer was wet etched in BHF for 15 minutes to remove the 1 μm layer of thermal oxide. To this end, the wafer was inserted into wet the etching holder with the backside exposed to BHF and the front side unexposed to protect the upper layer avoiding unwanted wet-etching. Some residuals were present, as shown in Fig.40. After 15 minutes, the thermal oxide was still present, so 2 minutes and 30 seconds of extra wet etching were performed (a total wet-etching time of 17 minutes and 30 seconds).

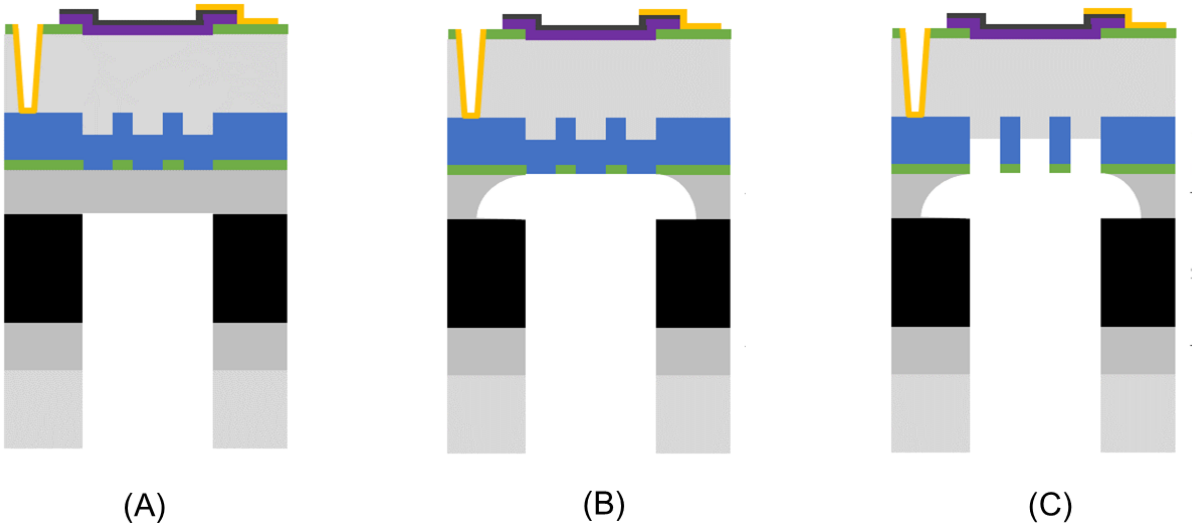


Figure 39: Steps described in this section. (A): DRIE of 525 μm of silicon. (B): Wet etching of 1 μm of thermal oxide. (C): DRIE LPCVD polysilicon.

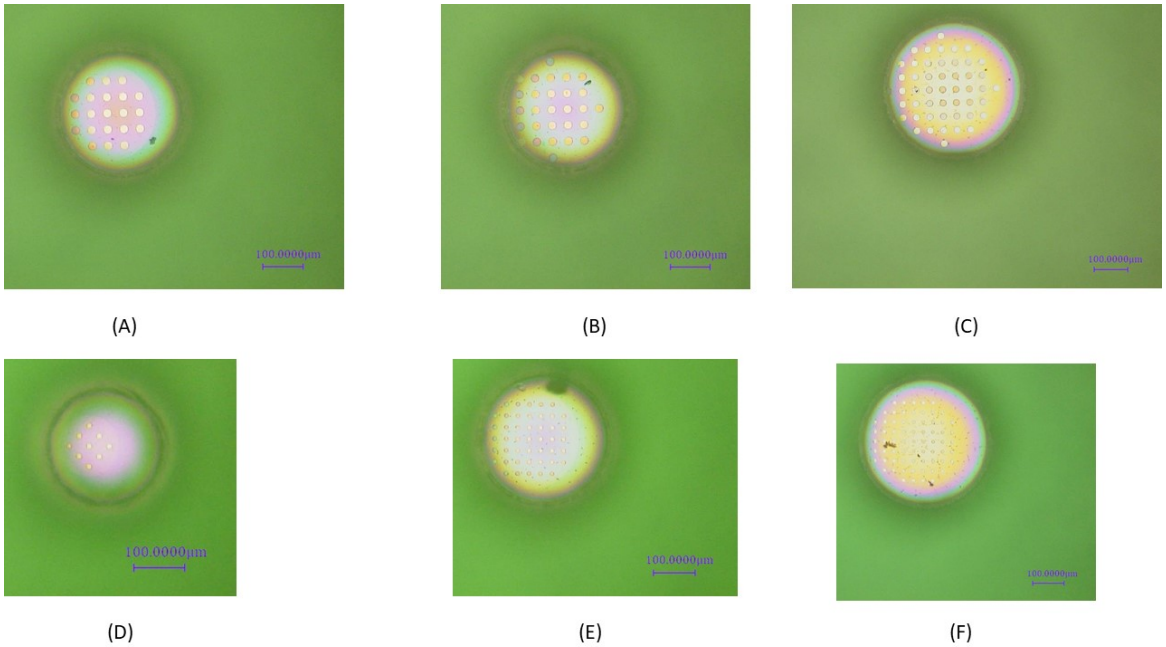


Figure 40: Wafer -004 after the 2 steps of BHF to etch the Thermal Oxide layer. (A): 300 μm structure on the backside after 15 minutes of etching. (B): 400 μm structure on the backside after 15 minutes of etching. (C): 500 μm structure on the backside after 15 minutes of etching. (D): 300 μm structure on the backside after 17 minutes and 30 seconds of etching. (E): 400 μm structure on the backside after 17 minutes and 30 seconds of etching. (F): 500 μm structure on the backside after 17 minutes and 30 seconds.

As shown in Fig.40, the etching of the thermal oxide was completed. This resulted in the presence of a color change between the holes and the surrounding environment. When the etching was not complete, this color difference could not be observed. Hence, once each venting hole presented a color change, the thermal oxide layer was completely etched. Therefore, the polysilicon layer of 1 μm was etched in AMS110. The etching time was set to 10 minutes and 10 seconds to fully etch the polysilicon present in the venting hole structures. After microscope inspections, it was possible to see that an excessive amount of polysilicon was removed in the 500 μm and 400 μm structures. This was deducted from the presence of large holes in the polysilicon layer and concentric holes in correspondence with the venting holes. The former are depicted in Fig.41 (A) in orange and are holes with a thickness equal to the one of the polysilicon layer, while the latter are illustrated in Fig.41 (B) in red. They are not as thick as the polysilicon layer but are an enlargement of the venting holes. These holes are linked to an over-etching of the LPCVD polysilicon layer when DRIE was applied.
Molybdenum was removed using hydrogen peroxide. The peroxide was placed on the wafer top surface for 5 minutes and the wafer was washed in DI water.
Wafer-004 was diced into two pieces. One side featured the small-diameter structures (100 μm, 200 μm and 300 μm which are the yellow and blue chips in Fig.30). On this side of the wafer, the polysilicon was not completely removed as the venting holes were not entirely created (it was observed that when a venting hole was successfully opened, it changed its color to black). Therefore, an additional etching in AMS110 was required on this part of the wafer to fully open the venting holes in the polysilicon layer. The other side of the wafer presented all the large-diameter structures (400 μm and 500 μm which are the green chips in Fig.30). This side of the wafer was split into 4 chips:

- Chip 1: The vast majority of the 400 μm wide structures presented a large hole (orange hole in Fig.41 and black hole in Fig.42 D) in the center of the structure. From digital microscope inspections, it appears that the polysilicon was fully removed in correspondence with the hole. This may have created a buckling in the 5 μm layer of PECVD annealed TEOS, but the same buckling can't be observed in other 400 μm wide devices. These devices seemed processed correctly, while all the 500 μm structures were ruined by the complete absence of the polysilicon layer.

- Chip 2: This chip presented the same structures described in chip 1. The difference can be observed in some 400 μm wide structures that featured a concentric hole (red hole in Fig.41) in correspondence with the venting holes in the polysilicon layer. This, like the large hole in the polysilicon layer, has been related to an over-etching of the polysilicon.

- Chip 3: All 500 μm structures were ruined by the absence of the polysilicon layer and all the 400 μm structures were processed correctly due to the presence of properly open venting holes.
- Chip 4: All the 500 μm structures were ruined by the absence of the polysilicon layer and all the 400 μm structures were processed correctly due to the presence of suitably open venting holes.

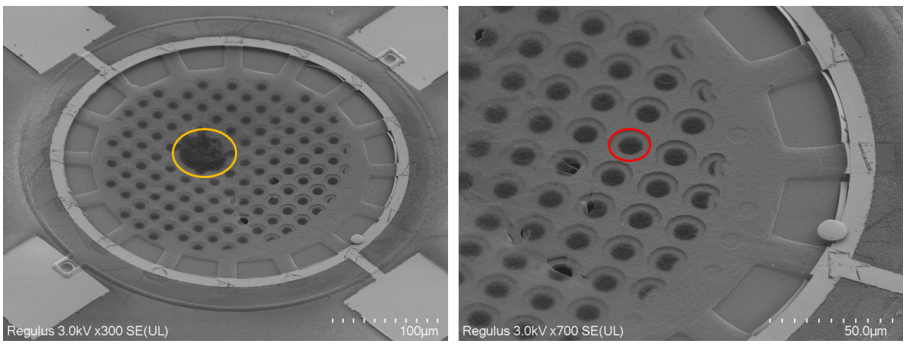


Figure 41: Unwanted holes in the back-plate. (A) is the large hole in orange with a thickness equal to that of the polysilicon layer. (B) are the concentric holes in red and are an enlargement of the venting holes.

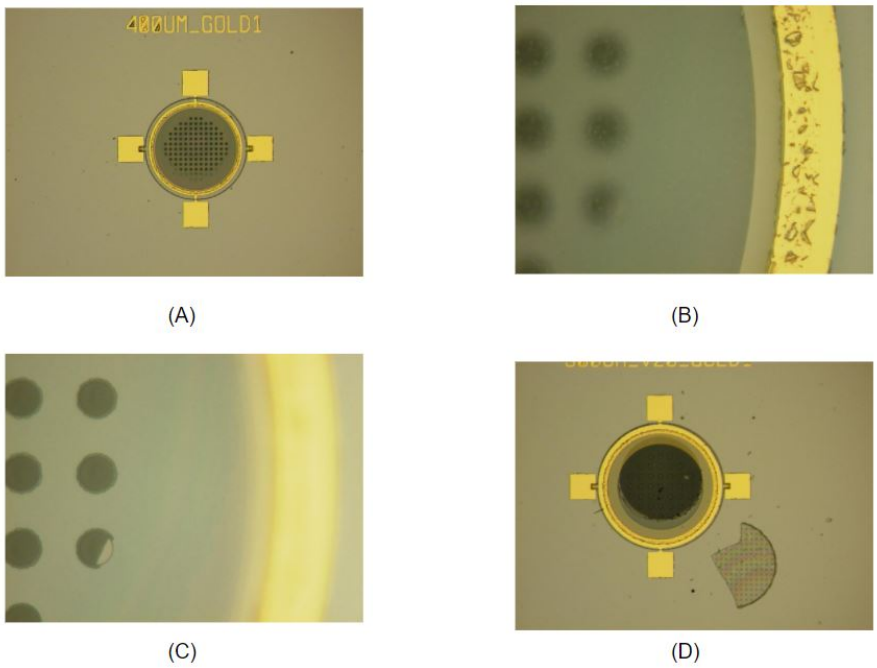


Figure 42: Chip 3 after dicing. (A): 400 μm wide structure with no hole in the centre. This structure seems to be processed correctly. (B): 400 μm wide structure. Focus on the gold layer. (C): 400 μm wide structure. Focus on the back-plate. (D): Broken 500 μm structure. The graphene layer was removed as well.

The part of the wafer having 300 μm wide structures was observed and captured using the digital microscope. Since the venting holes in the polysilicon layer were not fully etched on these structures, a run was performed in AMS110 for 1 minute. After the first etching, some structures had properly open venting holes in the polysilicon, but the vast majority of the venting holes were fully closed. Therefore another minute of etching in AMS110 was performed. Some structures presented some opened venting holes, but the vast majority had a non-etched polysilicon layer. Therefore another minute of etching in AMS110 was performed. The etch rate differences related to different membrane geometries (300 μm, 400 μm, and 500 μm structures) are related to the fact that considering larger openings, the etching rate was faster compared to the smaller ones.
After 3 runs, the vast majority of the structures presented a polysilicon layer that was fully opened in the

venting holes areas. This was assumed due to the color change seen in the venting holes which changed color after the etching, turning black. On the other hand, all the trampoline structures were almost fully closed, so another minute of etching in AMS110 was performed. Kapton tape was used to cover the structures that were not meant to be etched. After 5 minutes of etching, all structures were fully opened. The structures near the trampoline structures presented a central large hole in the polysilicon layer as the one depicted in Fig.43 (D). This could be related to the penetration of the etchant into the areas near the structures where the etching was needed (the trampoline structures area) as the etching in these areas was only blocked by manually applied Kapton tape.

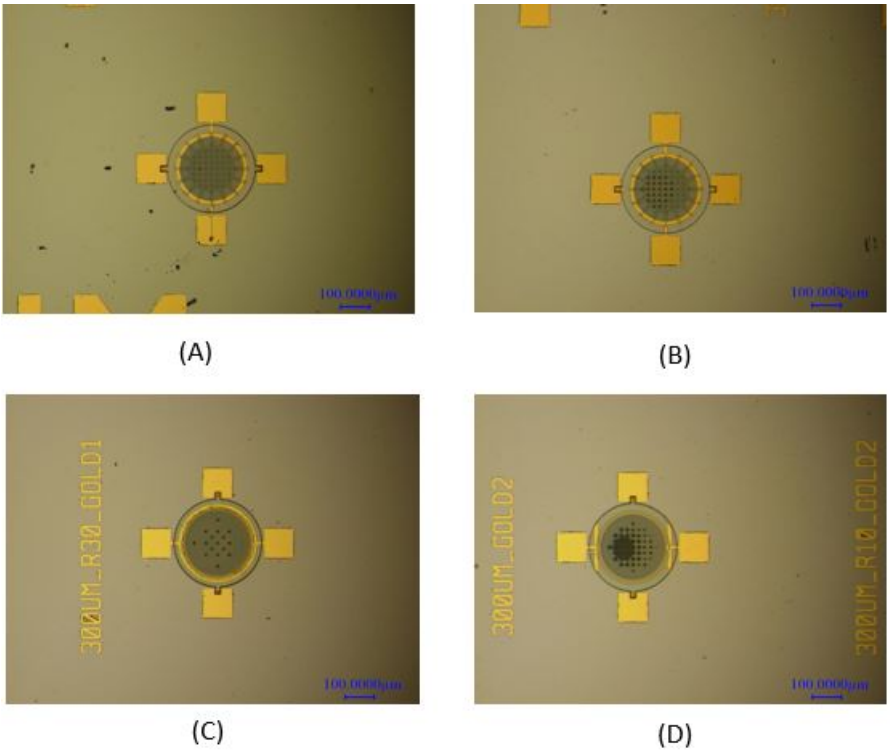


Figure 43: Wafer -004, 300 μm structure after 5 minutes of AMS110. (A): Trampoline structure, closed. (B): Trampoline structure, semi-open. (C): Trampoline structure, closed. (D): Structure near the trampoline structure. Despite the Kapton tape, the SF6 entered the structure, creating a large hole in the polysilicon layer.

4.1.6 Sacrificial TEOS Layer VHF Etching

Chip 1 was heated on the hotplate for 2 minutes at a temperature of 250 °C to remove any off-gassed polymer from the storage container. This helped to achieve a uniform etching. The first VHF was performed on chip 1. The VHF was used to remove the residual layer (5 μm of PECVD annealed TEOS). For this purpose, recipe 3 was used and the etching time was set to 25 minutes in 2 cycles.
The tool was purged for 16 minutes and the wafer was stored in a plastic container with litmus paper. Litmus paper was observed the next morning to understand the pH of the chip. After 15 hours in the box, the litmus paper shows no color changes, indicating the absence of HF residuals. Therefore, some images were taken to characterize chip 1 after the VHF and it was clear that the VHF started attacking the upper SiNx layer. Subsequently, the wafer was analyzed using the Scanning Electron Microscope (SEM) and some concentric rings in correspondence with the venting holes suitably processed on the polysilicon layer were observed (Fig.41). Some 400 μm structures have survived and, despite the presence of a large hole in the polysilicon layer of some structures, the graphene appeared to be suspended and correctly processed, suggesting the use of recipe 3 for the rest of the chips. Fig.44 illustrates the structures having a broken polysilicon layer.

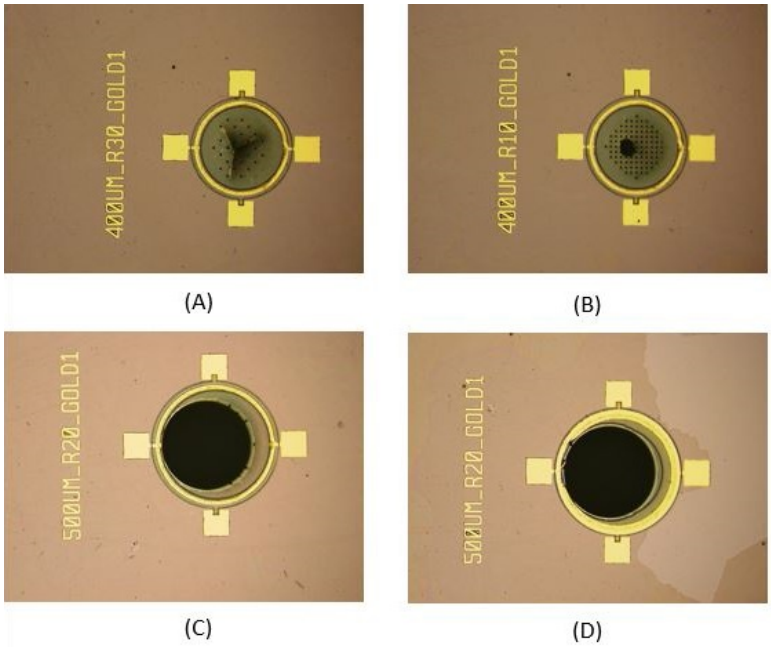


Figure 44: Chip 1 of wafer -004 after VHF. (A): 400 μm structure with a crack in the middle. (B): 400 μm structure with the large polysilicon hole in the middle. (C): 500 μm structure broken. (D): 500 μm structure broken. The silicon nitride layer on the top surface was etched by the VHF.

A VHF run was performed on chip 2. The etching was split into 2 runs (10 minutes each) using recipe 3. The wafer was placed over some diced pieces of a wafer that served as a shim. The shims were placed on a dummy wafer to avoid any contact between the chip and the backing as the graphene layer could delaminate as it could stick to the substrate. A total of 3 purging cycles was performed. The etching results were acceptable and comparable to those obtained for chip 1.

The part of the wafer having 300 μm structures was diced into chip 5, chip 6, chip 7, chip 8, chip 9, and chip 10. Chip 6 looked promising as the polysilicon layer was intact, so the PECVD TEOS layer was removed using VHF. The etching time was set to 25 minutes divided into 2 cycles and, after the etching, 3 purging cycles were performed. The VHF correctly suspended the graphene membranes.
The part of the wafer having small membranes (from 50 μm to 200 μm wide membranes) was diced. This side of the wafer was not processed in the VHF tool and was used to measure the capacitance seen between the top and the bottom electrodes. These chips were not processed because the venting holes were not open during DRIE and because of the absence of a chip holder for VHF etching. Without the hermetically sealed holder, it was impossible to selectively orient the VHF etching which penetrated simultaneously from the back and top-side. Furthermore, the VHF penetrated the interface between graphene and SiNx altering the final clamping since the SiNx layer was partially delaminated. With a hermetically sealed chip holder, the VHF penetrates only from the back-side, so the top surface will not be attacked leading to optimal clamping.

Therefore, the Cr/Au layer was successfully in contact with the top and the back electrodes. The small gap in the Cr/Au layer can be corrected by using a dedicated mask that considers the isotropy of BHF during wet-etching of the residual layer of TEOS (200 nm of TEOS used to prevent SiC formation). On the other hand, during measurements, this small gap allowed for measurements using the 4-probe station as capacitive measurements were performed by manually centering the needles in the contact openings. The back openings, venting holes, and the releases of the graphene layers were realized by back-side etching since the graphene was present on the top-side. The polysilicon presented large holes and enlargements of the venting holes, but once the problem was identified, it was corrected by masking with Kapton tape all the structures that were not meant to be etched with DRIE. The use of a dedicated mask for each membrane diameter will correct the problems related to the different etch rates of the DRIE of polysilicon related to different geometries. With a dedicated mask for each membrane diameter, on each wafer, there will be a single membrane geometry, thus nullifying the difference in etching rates as there will be only one geometry. The processed structures were then measured and the results of these measurements are explained in the next chapter.

5 Measurements of the Processed Device

The measurements made on the processed device are discussed in the following chapter. At first, SEM inspections will be studied. Subsequently, the capacitance of the devices will be measured and the resonance frequency identified. Finally, the results of Raman spectroscopy will be discussed.

5.1 SEM Inspection: Suspended Graphene Membranes

A Scanning Electron Microscope was used for detailed inspections. The following images show the suspended graphene structures. Transparency can be observed in some images illustrating the suspended thin graphene layer. This is due to the use of a higher voltage setting in the microscope which provided more energy to the electron beam. This makes the SEM capable of penetrating deeper into the material giving the effect of transparency. At 1 kV the graphene layer already shows its transparency due to its small thickness. In Fig.46 a higher voltage setting was used to be able to observe the polysilicon back-plate under the membrane. Fig.46 depicts the concentric hole around the venting holes that has been linked to an over-etching of the polysilicon layer. Fig.45 illustrates the large hole in the polysilicon layer (linked to an over-etching of the polysilicon layer) that has been found in some devices. Fig.47 illustrates some lines in the graphene layer. These lines could be caused by the handling of the wafers in AMS110. In Fig.47 the imprint of molybdenum in correspondence with the venting holes can be observed, indicating the absence of a catalyst layer under the membrane. Correct clamping can be observed, but the SiNx layer is almost delaminated. This delamination was related to the VHF etching which, without a sealed holder, attacked the wafer from the top-side.

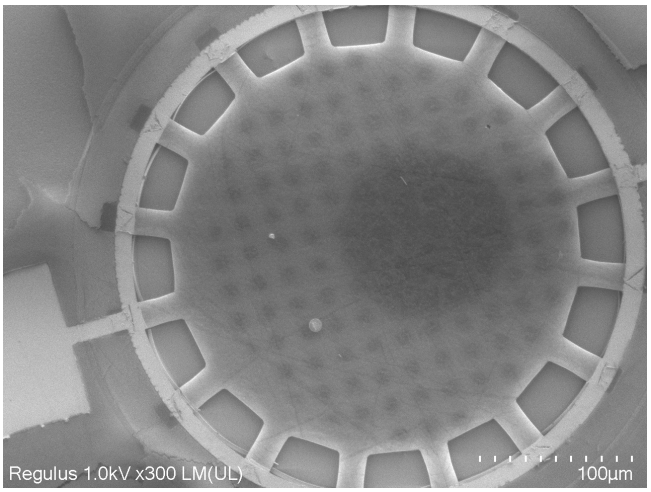


Figure 45: Top vision of a Graphene suspended membrane with large hole in the polysilicon layer.

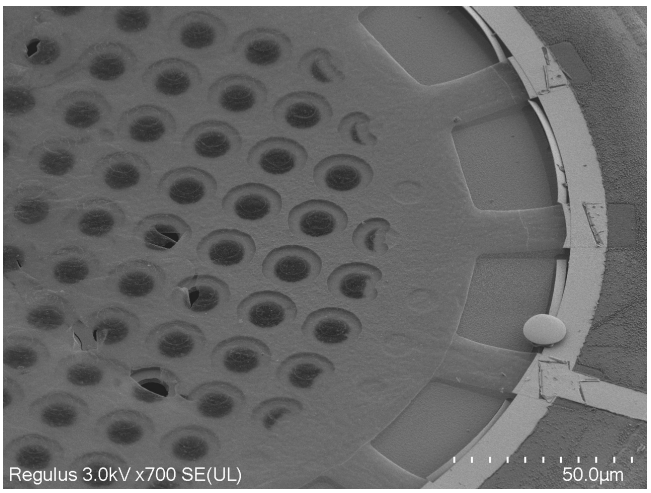


Figure 46: Concentric hole in the polysilicon venting holes linked to the over-etching in AMS110.

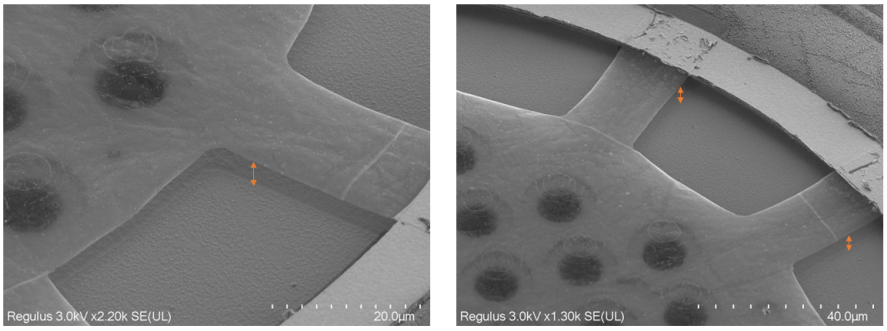


Figure 47: Gap between the membrane and the polysilicon back-plate.

5.2 Capacitive Readout

Using the Keysight Multi-frequency C-V measurements tool (Hewlett-Packard, Model 4284A, Precision LCR Meter), a capacitive readout was performed. A voltage was swept from -2 V to 2 V. The frequency was set to 300 kHz with 50 mV of amplitude and the Cp-G model was used. To carry out this test, several membranes were used. The used membranes were not etched in the VHF tool. As a result, these structures will present the back-cavity in the silicon layer and the venting holes in the thermal oxide and polysilicon layers, but the 5 μm layer of PECVD annealed TEOS underneath the membrane is still present. Considering equation 1 in a generic case, the dielectric can be any dielectric material (not necessarily air). In the generic case, ϵ_r is the relative dielectric permittivity. If air is the used dielectric, ϵ_r is equal to 1, so it can be neglected. On the other hand, when considering a material other than air, ϵ_r will differ from 1 and must be implemented in the equation. Therefore, the capacity equation can be written as follows:

$$C = \frac{\epsilon_0 \epsilon_r A}{g} \tag{19}$$

Considering $\epsilon_0 = 8.85 * 10^{-12}$ F/m, TEOS as a dielectric layer ($\epsilon_r = 3.9$), the area of a circular membrane given by the square of the membrane radius multiplied by π and the dielectric thickness equal to 5 μm, it was possible to calculate the capacitance of each structure (for 50 μm membranes, the computed capacitance was 0.0135 pF, for 100 μm was 0.0542 pF and for 300 μm was 0.488 pF). Then, the membranes were measured. Fig.48 illustrates the measured capacitances. The capacitances were measured when a voltage was swept between -2 V and +2 V and the average capacitance was calculated from the data obtained. In Fig.48 the x-axis represent the diameter of the membrane and the sample on which the capacitance was measured, while the y-axis considers the average capacitance of the respective membrane.

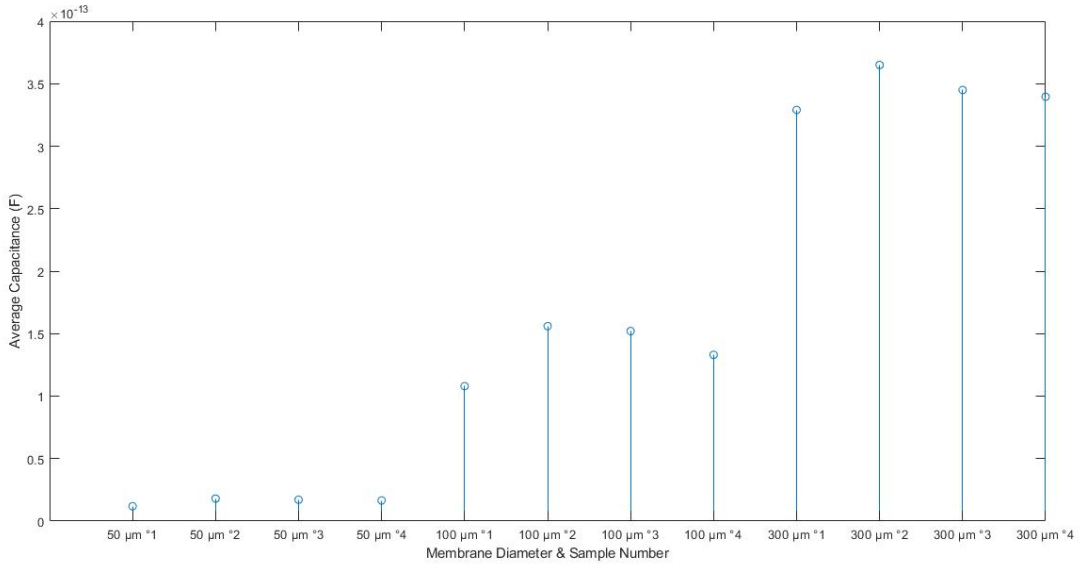


Figure 48: Capacitive readout conducted on 50 μm, 100 μm, and 300 μm structures. The x-axis represent the diameter of the membrane and the sample number. The y-axis considers the average capacitance of the membrane.

Consequently, as the membrane area increased, the measured capacitance increased. These results are in line with the analytical model described in equations 1 and 19. The difference in the computed values and the measured values is related to the use of a simplified model. In 19 the capacitance only considered the dimensions of the areas of the suspended graphene and the back-plate. The resulting capacitance exists in the device, but it is not the only capacitance present (C1 in Fig.49). A capacitance will exist in the region where the graphene membrane is not suspended (clamping region, C2 in Fig.49). This capacitance will have a SiNx insulator, the polysilicon as the back-plate, and the clamped graphene as the top-plate. There will also be capacitances in correspondence with the gold layer and the polysilicon layer (C3 in Fig.49). This capacitance will have a SiNx insulator, a Cr/Au top-plate, and a polysilicon back-plate. The parallel of these capacitances is needed to correctly compare the computed values with the measured ones. The use of a complete model also explained the difference in the measured capacitances in structures having the same diameter since the electrode area was not identical between the various samples having the same diameter.

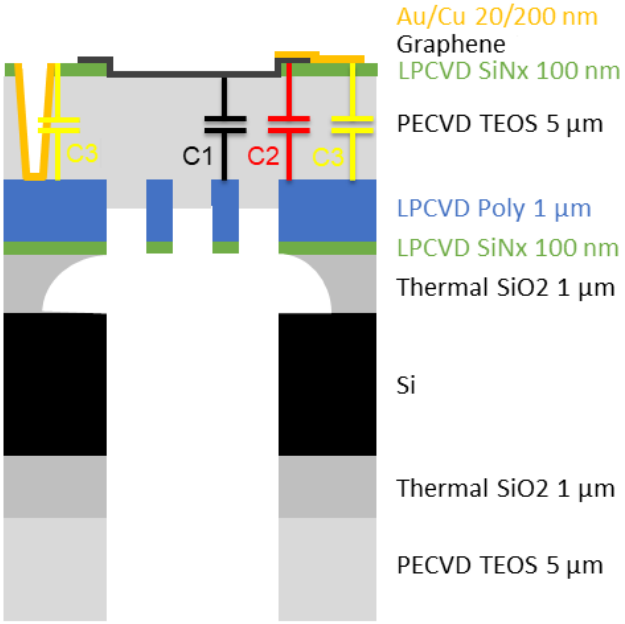


Figure 49: Capacitance of the Microphone

5.3 Resonance Frequency

To measure the resonance frequency, the setup described by Baglioni et al.[29] was used. The sample was placed at atmospheric pressure. The chip was mounted on a piezo-shaker stage where a voltage is applied. When modulating the voltage, the piezo will oscillate causing the membrane to move which, at some point, will reach its resonant frequency. A single-point Laser Doppler Vibrometer was used to measure the displacement of the membrane [29]. For the following measurements, 2 structures were considered. In Fig.50 and 51 the first 300 μm structure is considered. In this device, the graphene layer collapsed, but part of the membrane was suspended at the large polysilicon hole, so the laser was pointed in that spot. Considering the resonance frequency is inversely proportional to the membrane radius (Eq.6), the measured resonance frequency was expected to be high as the hole diameter was approximately 30 μm. As shown in Fig.50, the measured resonance frequency was 275 kHz. In Fig.51 the laser was aimed at a point where the back-plate was intact. It was possible to conclude that this membrane collapsed as no resonance frequency was measured. The peak in Fig.51 at 375 kHz was related to noise since, when the piezo did not oscillate as no voltage was applied, the same peak was still present. Furthermore, in Fig.50 the same peak at 375 kHz can be observed. Hence, it was concluded that the peak at 375 kHz was caused by noise.

Fig.52 illustrates the second 300 μm "trampoline" membrane. The laser was pointed at the back-plate and a peak at 22 kHz was measured. Hence, it was possible to conclude that the membrane was suspended. This was confirmed by the fact that the measured resonance frequency was smaller than that measured in Fig.50. The membrane in Fig.50 was suspended only at the large polysilicon hole, so its radius was approximately 10 times smaller than that of the membrane in Fig.52 where the entire 300 μm membrane was suspended. The difference in the value of the resonant frequency of the two membranes follows Eq.6. Therefore, it was possible to conclude that the membrane was suspended. Additionally, a 10 kHz audio signal was emitted by a telephone speaker and the signal was sensed by the suspended membrane. Fig.53 depicts its output spectrum and it is possible to observe a peak at that frequency.

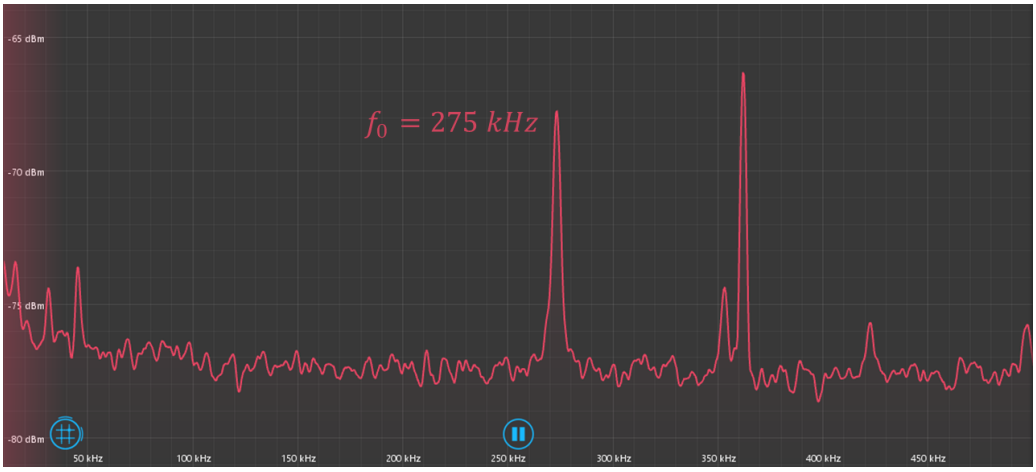


Figure 50: Collapsed Membrane. The resonance frequency was measured at the large hole in the polysilicon layer.

Figure 51: Collapsed Membrane. The resonance frequency was measured at the polysilicon back-plate.

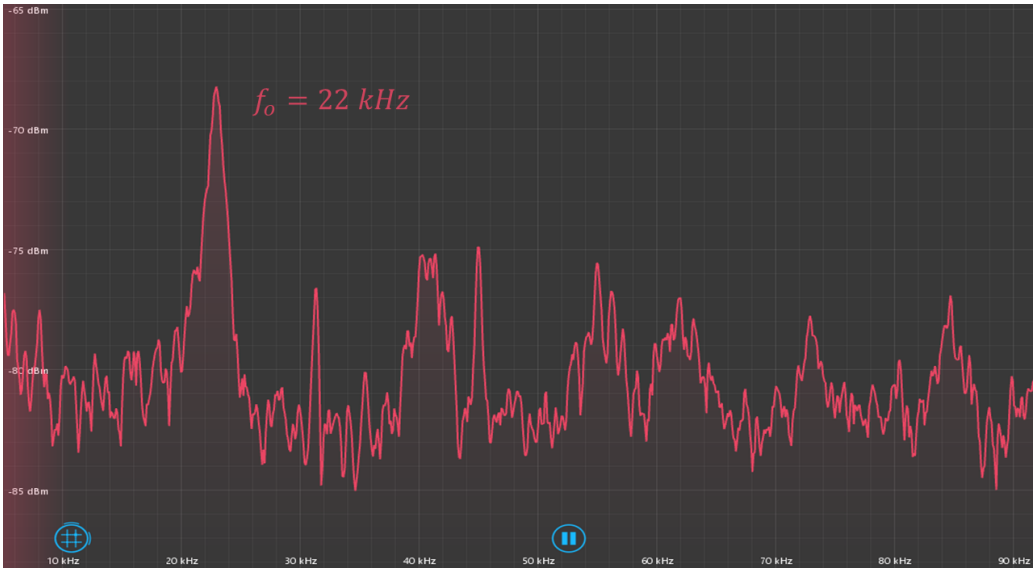


Figure 52: Suspended "Trampoline" Membrane. The resonance frequency was measured at the polysilicon back-plate.

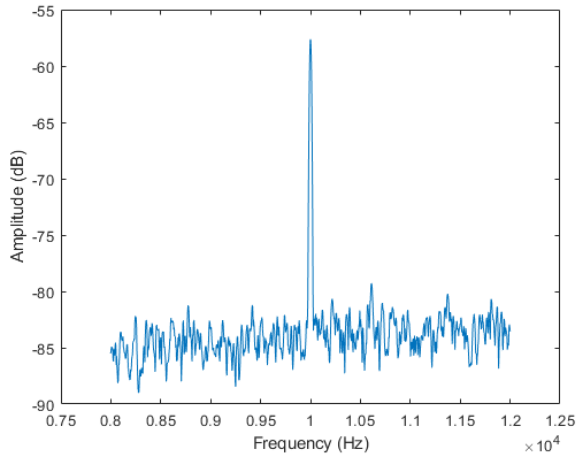


Figure 53: Spectrum when a 10 kHz audio signal is sensed by the membrane.

Since a resonance frequency was measured, it was possible to conclude that the graphene membrane was suspended. In the measurement, the resonance frequency was around 22 kHz so, it was outside the audio bandwidth, ensuring correct detection.

5.4 Raman Spectroscopy

Raman spectroscopy is a kind of molecular spectroscopy used to evaluate the purity of a certain material [30] and can be used for defect definition in a graphene layer. This measurement is based on the shift in frequency of the reflected light. Light reflection is generated by exposing a sample to a laser having a known wavelength. The measurement output is characterized by several peaks. The position of these peaks depends on the light reflected from the sample.
On the y-axis, intensity is expressed in an arbitrary unit. This is because the intensity is related to a detector capable of changing for different configurations and time intervals. The most insightful peaks are the D-peak (located at approximately $1350\,\mathrm{cm}^{-1}$), the G-peak (located at approximately $1580\,\mathrm{cm}^{-1}$), and the 2D-peak (located at approximately $2700\,\mathrm{cm}^{-1}$). The G-peak is related to the vibration in the plane of sp^2 hybridized carbon atoms[31]. The D-peak is related to defects on the graphene layer (wrinkles, corrugations...)[31]. The 2D-peak is related to the number of graphene layers[31]. In the performed measurements, the I_D/I_G ratio (ratio

between the intensity of the D-peak and G-peak) was always approximately 0.3. The intensity ratio of the D and G peaks provides an estimate of the defectivity of graphene samples.

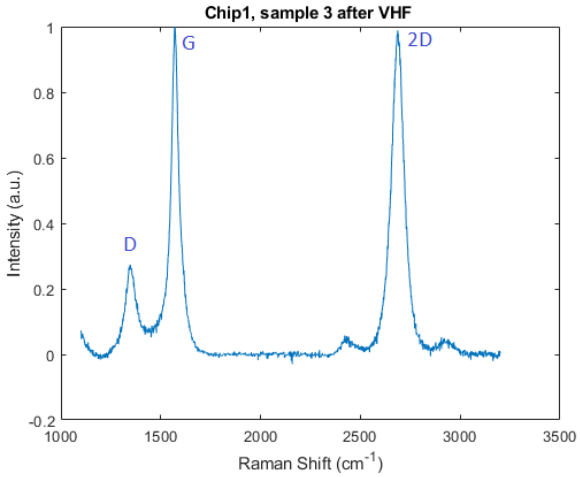


Figure 54: Wafer 004, chip 1, sample 3. The Raman measurement was performed after VHF using a laser with a wavelength of 514.5 nm and a 100× objective lens.

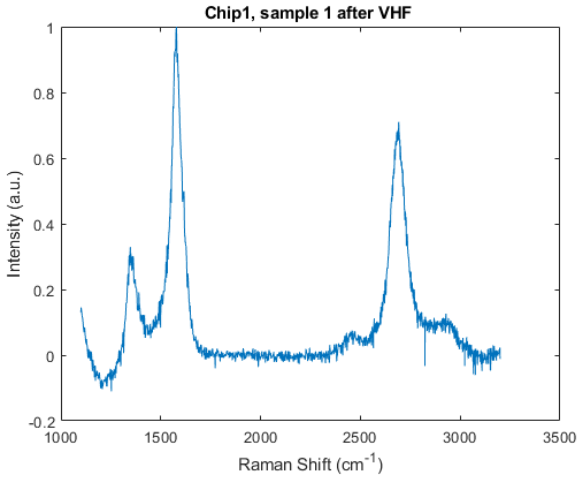


Figure 55: Wafer 004, chip 1, sample 1. The Raman measurement was performed after VHF using a laser with a wavelength of 666 nm and a 100× objective lens.

These measurements were performed on suspended membrane devices. The results obtained, regarding the I_D/I_G ratios and the I_{2D}/I_G ratios, are in line with those obtained in [15] that, for the CVD of graphene, used the same reactor and recipe used for the presented thesis. This confirmed that the defectivity of the graphene was acceptable, suggesting that the entire process flow did not affect the graphene quality. Additionally, considering the I_{2D}/I_G ratios, it was concluded that the realized layer was a multi-layer of graphene[15].

6 Final Considerations & Future Perspective

6.1 Conclusions

The resulting device featured a suspended graphene membrane and allowed miniaturization. The overall dimensions of a state-of-the-art silicon-based capacitive microphone are approximately 3 mm. The smallest device obtained in the presented work was 50 μm wide, thus 60 times smaller than the silicon counterpart.

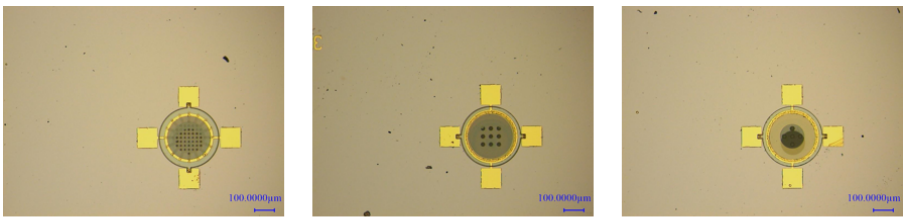


Figure 56: Wafer 004, 300 μm structures, chip number 5. (A) and (B) are membranes having the venting holes correctly open. (C) Is a membrane having a large hole in the polysilicon layer.

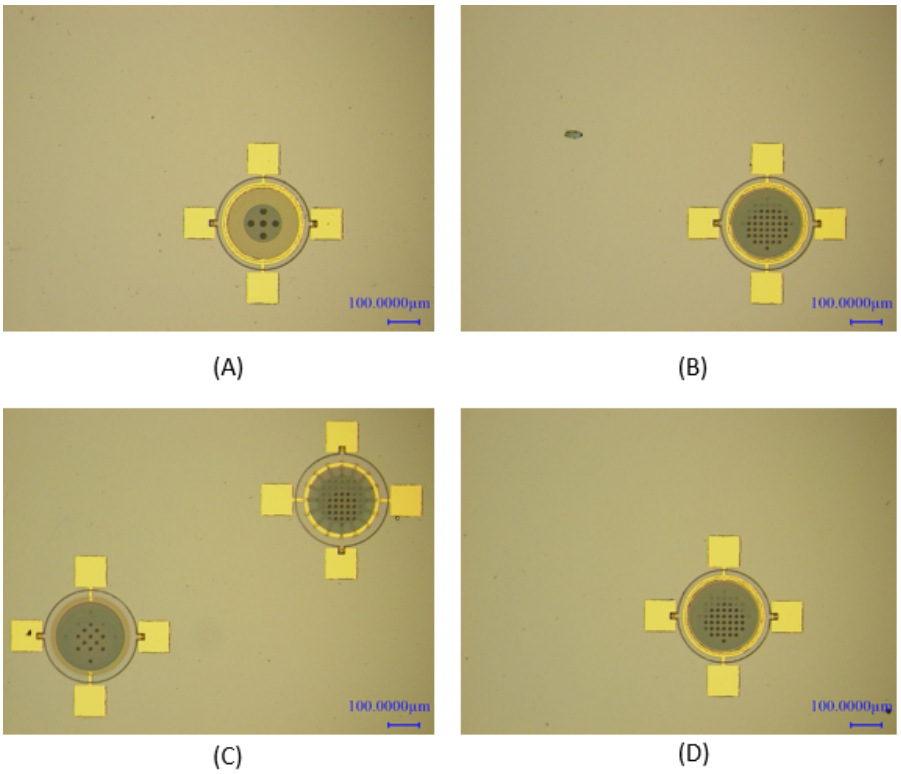


Figure 57: Wafer 004, 300 μm structures, chip number 6. (A)and (B) are membranes having the venting holes correctly open. (C) and (D) show 2 membranes having the venting holes correctly open, but the number of opened venting holes is smaller than the one of (A) and (B).

Thus, the presented process flow successfully created wafer-scale MEMS microphone devices with graphene membranes that did not require a transfer. A single wafer was fully processed and the DRIE of the polysilicon layer damaged a large number of structures, creating devices that broke before the membrane was released. On the other hand, once this critical step was identified, the process was conducted correctly, avoiding damage to the polysilicon back-plate. Furthermore, part of the membrane was suspended after the process. This indicates that the process flow is suitable for creating graphene membranes in a fully scalable process, without transferring the diaphragm.
Additionally, the bottom electrode was successfully contacted using gold evaporation, starting with a device with very large aspect ratios. The small discontinuity observed in the gold layer can be corrected by using a

dedicated mask.
In the presented process, many steps were performed when the graphene layer was already present on the substrate. On the other hand, this did not affect the graphene layer. The results of the Raman spectroscopy (regarding the D and 2G peak) were in line with the previous results obtained. Therefore, even though graphene has undergone several steps, it has retained its quality. Furthermore, graphene has been successfully used as an electrically conductive layer. The measured capacitances comply with the computed values. On the other hand, the capacitance was not measured after the release but was measured in the previous step (before VHF etching). Therefore, it can be concluded that the process did not affect the overall performance of the graphene layer. Furthermore, the measured resonance frequency was outside the audio bandwidth.

6.1.1 Answer to the Research Questions

Based on the results obtained in this thesis, an answer is now provided to the research questions presented.
A process flow could be created to fabricate MEMS condenser microphones for large-scale production using graphene as a membrane. The back-plate was realized in polysilicon and the dimensions of the device were reduced concerning its silicon counterpart. In fact, considering the smallest dimensions of the obtained devices and comparing them with the dimensions of a state-of-the-art device, the obtained microphone was approximately 60 times smaller. The graphene layer was not transferred and the quality of the layer was not compromised during processing. Unfortunately, it was impossible to measure the performance of the device since, to measure sensitivity, an external amplifier IC is required to successfully read the voltage shift related to a pressure wave hitting the diaphragm.

6.2 Future Prospective

To increase the yield of the process, it is possible to change the mask design. The DRIE of the polysilicon layer was a crucial step in the process and, by changing the mask design, this step can be controlled without taking care of the aspect ratios of different structures. In fact, by creating different masks for different microphone structures (different radius, different number of venting holes...) so that only one structure is present on each wafer, it may be possible to etch homogeneously during the DRIE of the polysilicon layer. Another possibility is to etch the polysilicon layer with different etching techniques.
Also, the VHF etching was of interest. The yield in the presented process was further reduced by VHF etching due to the absence of a chip holder. Without a chip holder, it was impossible to control the penetration of the HF vapor, so the VHF started attacking the SiNx layer in some areas. In fact, the VHF can penetrate the interface between graphene and SiNx altering the final clamping. After VHF, the SiNx partially delaminated determining possible damages or altering the membrane release. Hence, the boundary conditions of the clamping will not be uniform.
With a hermetically sealed chip holder, the VHF etching can be controlled on the back-side of the wafers, thus an increase in process yield is expected.
Another possible modification of the process is the use of a dedicated mask for the creation of the bottom electrode contacts. This will erase the discontinuity seen in the gold contact layer.
Finally, to fully characterize the device, the capacitance should be measured once the graphene is fully suspended and an amplification system should be designed. With a specifically designed IC amplifier, it will be possible to understand the performance of the realized microphone when the pressure wave hits the diaphragm.

Appendix A Implantation, Channeling & Diffusion

Implantation is a process used to incorporate dopant atoms into silicon. N-type dopants (As, P, Sb) and P-type dopants (B) are initially ionized and subsequently accelerated through a magnetic field. The magnetic field is responsible for mass separation due to the presence of the Lorentz force.
Depending on the bombardment energy, the ions will be stopped at a certain depth by the silicon atoms. This process will damage the crystalline structure of silicon, making the silicon amorphous.
Annealing is then used to fix the dopant atoms in the lattice. The distribution of the dopants in the lattice follows a Gaussian distribution.
The dopant distribution will depend on the number of ions and the ion energy.

When the wafer is bombarded, depending on the crystal orientation, channels are created in the crystal lattice. Therefore, the ions in the channel experience less scattering and are able to "channel" much deeper in the silicon.
The deviation from the Gaussian distribution is called the "channelling tail". The channelling can be reduced by means of several techniques. On the other hand, these techniques are unable to completely prevent channelling from happening.

Diffusion is a "species" based process . Atoms, holes, and electrons are called "species". If a concentration gradient is present, the species can migrate through the silicon.
There are 2 common diffusion cases:

1. Limited Source Diffusion: A fixed number of dopants are supplied to the silicon, similar to the implantation process. The dose is constant over the entire period.
2. Constant Source Diffusion: In this case, the dopants are applied to the silicon through a doped oxide. A constant source of dopant is present. In this case, more dopants are introduced into the silicon layer during the diffusion period.

Furthermore, the diffusion coefficient is temperature dependent. As a matter of facts, at temperatures smaller than 700° C the diffusion coefficient is almost equal to 0.

Appendix B Thermal Stability Of Polysilicon Resistors & Polysilicon Doping Considerations

Polysilicon is made from a series of mono-crystalline silicon grains with different sizes and orientations. Each grain is separated from its neighbors by the edges of the grains.
In the presented thesis, polysilicon will be used for the creation of the bottom electrode. Therefore, a conductive polysilicon layer is required to properly read the back-plate of the condenser microphone.

In [18], conventional furnace annealing (CFA) and rapid thermal annealing (RTA) were lead on polysilicon films of 100, 200 and 300 nm thickness. The polysilicon samples were doped with boron, arsenic and phosphorus. The RTA was performed before and after the CFA to study the impact on sheet resistance stabilization (the sheet resistance is a quantity that characterizes the electrical conduction properties, in particular for two-dimensional or almost two-dimensional samples. Two-dimensional or almost two-dimensional samples have a thickness H much smaller than the width W and the length L).

The effect of an RTA above 1100 °C will impact the conductivity of the final system[18]. The grain size change in arsenic doped films is present after an RTA at a temperature greater than 1100 °C. The cooling time will be of fundamental importance in stabilizing the sheet resistance. Therefore, due to its short duration, RTA is preferred for cooling as it will stabilize the resistance[18].

At first, the film deposition was initiated. A $12\,\Omega * \text{cm}$, p-type, <100> oriented silicon wafer was used. A 22.5nm oxidation was performed. Using LPCVD at 625 °C, polysilicon films were deposited. Subsequently, a 25nm LPCVD TEOS oxide was deposited.
Implantation was performed.
After implantation, CFA and RTA were performed in a nitrogen atmosphere.
A Prometrix FT500 four-point probe station was used for the device characterization[18].

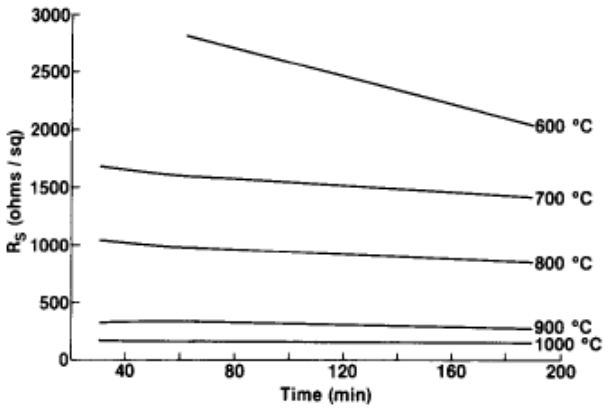


Figure 58: Film Resistance in respect to CFA for an arsenic doped wafer[18].

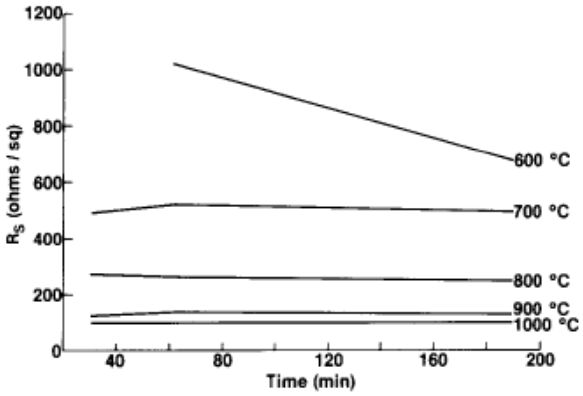


Figure 59: Film Resistance in respect to CFA for an phosphorus doped wafer[18].

As depicted in Fig.58 and Fig.59, the film resistance decreased for CFA at temperatures between 600° and 800°. The process is time dependent. Therefore, the film resistance will change with different process duration. For temperatures above 800° no change can be detected. The decrease of R_S is related to a combined effect of dopant activation and desegregation[18].

If a lower temperature (with a 550° limit) is used after a 1000° RTA (for 5 seconds), R_S changes its value, thereby increasing the film resistance.
A slow cooling-CFA process is less effective than a fast RTA in terms of polysilicon sheet resistance stabilization. Therefore, RTA is preferable to use in the cooling process follower by the CFA process[18].

The doping process can be performed using in-situ dopant deposition, spin-on source diffusion, or using ion implants as in[19].
Regardless of the doping technique, a highly doped poly-silicon in a CMOS process can create density defects of approximately $10\,\mathrm{cm}^2$ in the gate oxide[19].
However, when a low dose implant is performed on poly-silicon, the density of these defects is in the range of $0.002\,\mathrm{cm}^2$[19].

When using in-situ deposition or ion implantation, high temperatures annealing is required to activate the dopant and achieve low sheet resistance. This high-temperature annealing leads to an accumulation of dopant species at the interface between oxide and polysilicon. This accumulation can be crucial in the generation of defects in the oxide[19].

A capacitor yield is present when spin-on phosphorus doping for poly-silicon is used.
When using a high current beam, the maximum dielectric strength is reduced, but the possibility of creating defects is also decreased a[19]. Results from [19] showed that the oxide degradation is related to the poly-silicon doping: a longer time at high-temperature results in a lower capacity yield.
The same results were discovered when using an in-situ phosphorus-doped poly-silicon.

When BF_2^+ is used for implantation and activation of the poly-silicon, a capacitor yield loss is present. Considering a 15 minutes annealing, when the temperature is increased from 750 °C to 900 °C the capacitor yield is slightly decreased (from 95% to 90%)[19].
On the other hand, when a high-dose implant is performed, the capacitor yield decreases much faster. After 15 minutes of annealing in a high-dose implant, the yield is reduced from 65% at 800 °C to 33% at 900 °C. Therefore, this method generates more degradation problems regarding in-situ phosphorus-doped films when a high dose implant is performed.

When As^+ is used as poly-silicon implantation and activation, the capacitor yield decreases in 15 minutes from 85% at 800 °C to 70% at 900 °C[19].

Therefore, implantation and annealing of BF_2^+ at a high dose are more destructive than those of n-type dopants under the same conditions [19].

B.0.1 Electrical Measurements On Ion-Implanted LPCVD Polysilicon Films

A pyrolysis process of silane at a temperature of 647 °C was performed using LPCVD on an oxide-coated layer having a 0.6 μm thickness. Boron or phosphorus ions were used as dopants. An acceleration of 145 keV and a dose that ranged from $10^{12}cm^{-2}$ to $10^{15}cm^{-2}$ was used[20].
Both the dopant atom segregation and the carrier trapping at grain boundaries phenomena are of interest when defining the polysilicon electrical conduction properties.
On the other hand, experiments have shown that dopant atom segregation is influential for doses below $10^{13}cm^{-2}$. For doses between $10^{13}cm^{-2}$ and $5 * 10^{14}cm^{-2}$, carrier trapping effects are more pronounced. For doses above $5 * 10^{14}cm^{-2}$, conduction through a carrier tunneling through the potential boundaries at the grain boundaries starts to be influential in the film conductivity[20].

The Cowher and Fripp[20] dopant atom segregation model considers the impurity atoms segregated at the grain boundaries. As the dopant concentration increases, a grain boundaries saturation state is reached. Therefore, the excess dopant atoms are evenly distributed in the grain crystalline structure. Therefore, the resistivity of the layer decreases dramatically[20].
The Seto model assumes that grain boundaries contain a large number of trapping sites. The dopant atoms are uniformly distributed. When the dopant concentration is low relative to the trapping site density, most of the free carriers are trapped leading to a high resistivity[20].

A $10\Omega cm$, <100> N-type silicon wafer was used. A standard cleaning process was performed and a 600 nm SiO_2 layer was deposited via low-temperature CVD.
Using LPCVD, a 600nm polysilicon film was deposited.
The deposition process was performed at a temperature of 647 °C and a pressure of 360 milliTorrs with a nitrogen-diluted silane flow at 46 cm^3/min. A deposition rate of 10 nm/min was found[20]. Implantation-annealing was performed at 950 °C in O_2 and N_2 environment for 40 min[20].

Fig.60 depicts the measured resistivity relative to the doping concentrations for different temperature values. A significant decrease in resistivity occurs at a doping concentration of around $5 * 10^{13}cm^{-2}$.
The annealing environment and temperatures for the annealing process that occurs after implantation do not have an impact on the electrical properties of the polysilicon[20].

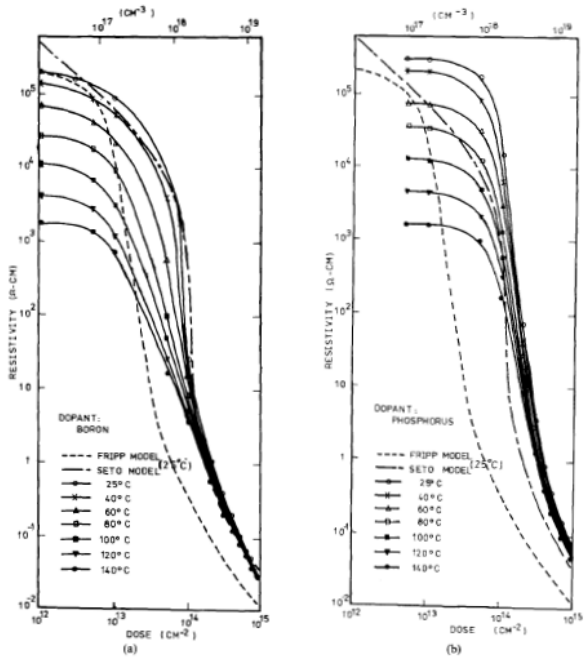


Figure 60: Resistance VS Doping concentration[20].

Both models predicted a drop in resistivity when the dopant concentration reaches some critical value. For doses below $5 * 10^{13}cm^{-2}$, the resistivity is rather independent of the doping concentration for the phosphorus-

doped samples[20]. On the other hand, resistivity decreases, in boron-doped samples, as the doping concentration is increased. These phenomena indicate that the characterization of electrical conductivity is influenced by both atomic segregation and by the carrier entrapment at the grain boundaries.

Therefore, it was possible to split the behavior of polysilicon into 3 sections:

1. When the dopant concentration is less than $10^{13}cm^{-2}$, the resistivity is almost independent of the doping concentration.
2. When the dopant concentration is between $10^{13}cm^{-2}$ and $5 * 10^{14}cm^{-2}$, the conductivity characteristic follows the carrier trapping model. Therefore, resistivity changes with temperature from 5 to 7 orders of magnitude.
3. When the dopant concentration is greater than $5 * 10^{14}cm^{-2}$, conduction through the potential barrier must be considered.

B.0.2 Polysilicon Doping Final Considerations

With the aid of an online simulator, [21], it was possible to define the value of the ionic energy that will be used for polysilicon doping. Since the design aims to achieve conductive polysilicon, the value of the sheet resistance must be small. Therefore, considering the plots depicted in Fig.60, a doping concentration of $10^{19}cm^{-3}$ (or a doping dose of $10^{15}cm^{-2}$) was used. This ensured that the polysilicon behaved as a conductor.

In the online simulator from [21], a substrate depth of $1\mu m$ has been selected. A diffusion temperature of $1000°C$ and an ion dose of $10^{15}cm^{-2}$ were used. Since P-type devices are easier to contact than N-type devices, a Boron dopant species were selected. Since polysilicon must behave as a conductor, all charges should be accumulated on the top surface. Therefore, in the plot of the concentration of impurities VS the depth in the substrate, an initial plateau at around 10^{19} should be achieved. Furthermore, the plot should, later on, show a roll-off.

The general value of the ionic energy used in the EKL laboratory ranges between 20 keV and 45 keV. Therefore, a sweep of the ionic energy was performed between these values while plotting the concentration of impurities VS the depth in the substrate. The results of these plots are depicted in Fig.61.

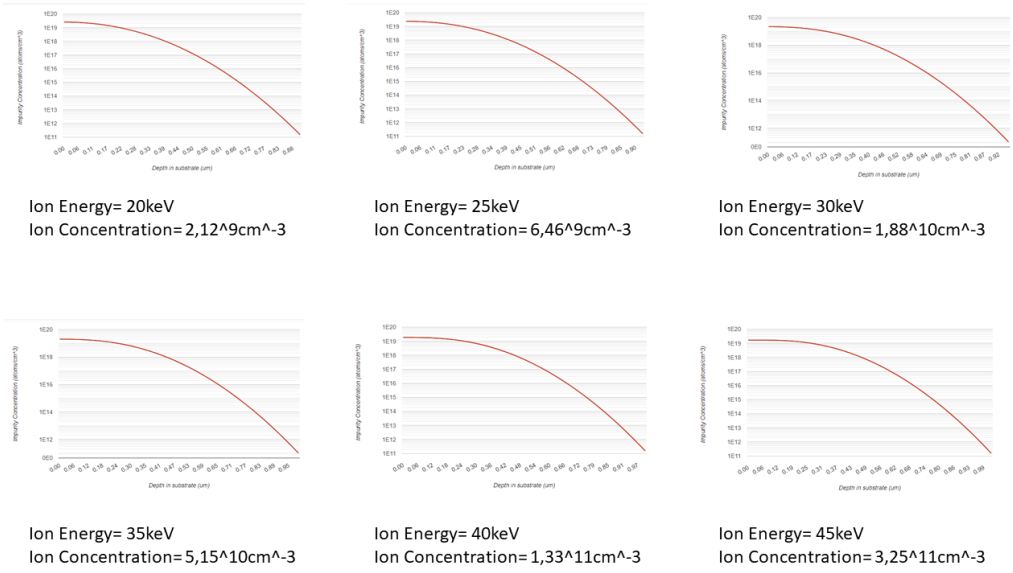


Figure 61: Concentration of Impurities With Respect to the Depth in the Substrate for Ion Energy ranging from 20 keV to 45 keV[21].

Therefore, as depicted in Fig.61, the best plateau and roll-off behaviors are achieved when ion energy of 45 keV is used. The behavior of the concentration of impurities with respect to the depth in the substrate when

ion energy of 45 keV is selected is depicted in Fig.62.

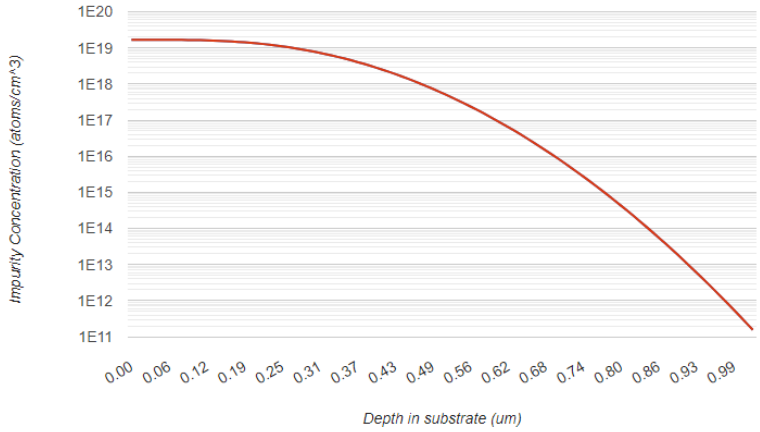


Figure 62: Concentration of Impurities With Respect to the Depth in the Substrate for Ion Energy equal to 45 keV[21].

Appendix C Processing Tests

C.1 Silicon Nitride & Polysilicon Etch Rates

This study aims to understand how much Poly-Si will be etched on a SiNx layer. On 2 N-type silicon wafers, a 150 nm layer of thermal oxide was grown. Wafers numbers are depicted as follows:

- MX19002-208
- MX19002-211

1000 nm layer of polysilicon (Poly-Si) and 1000 nm layer of SiNx were grown and the SiNx was patterned. MX19002-211 was inserted in Dektak. Four points were used to measure the height of the gap. The scan length has been set to 500 μm and the scan time has been set to 20 seconds, leading to a SiNx etching rate of 6.335 nm/s with a standard deviation of 0.58 nm/s and a variance of 0.336 nm/s.
Then all polysilicon was dry-etched. To better control the etching, the time has been divided into 4 smaller etchings. These 4 etching steps were performed on MX19002-211 and each time an etching step was completed, the height gap was measured using Dektak and reported in the following table:

Table 7: MX19002-211 polysilicon etch rates.

Etching Time	**Wafer's Left Point**	**Wafer's Right Point**	**Wafer's Upper Point**	**Wafer's Lower Point**
20 s	13.4 nm/s	13.4 nm/s	13.2 nm/s	13.3 nm/s
40 s	10 nm/s	10 nm/s	3 nm/s	9.21 nm/s
60 s	8.5 nm/s	8.5 nm/s	4.5 nm/s	8 nm/s
80 s	4.9 nm/s	13 nm/s	13 nm/s	4.9 nm/S

Thus, leading to a polysilicon etching rate of 9.21 nm/s with a standard deviation of 1.57 and a variance of 2.5.

Subsequently, Dektak was used to estimate the width of the holes of MX19002-211:

- Left point: The hole width was equal to 40 μm. The spacing was equal to 50 μm.
- Right point: The hole width was equal to 40 μm. The spacing was equal to 50 μm.
- Upper point: The hole width was equal to 100 μm. The spacing was equal to 100 μm.
- Lower point: The hole width was equal to 30 μm. The spacing was equal to 40 μm.

Later the MX19002-208 wafer was inserted in Dektak with the same conditions as the one used for MX19002-211 for a SiNx etching. Once more, 4 points were measured leading to a SiNx etching rate of 6.6 nm/s with a standard deviation of 0.37 nm/s and a variance of 0.136 nm/s.

Upon completion of the dry-etching of polysilicon, the gap heights were measured on MX19002-208 using Dektak resulting in a polysilicon etching rate of 12.2 nm/s with a standard deviation of 1.44 nm/s and a variance of 2.08 nm/s. Therefore, the etching rate was not uniform across the entire surface, but the variation in the etching rate was relatively small.

Concerning both MX19002-208 and MX19002-211, the best etching condition was found in the lower point of MX19002-208. The goal of this etching was to fully etch 810 nm of SiNx and 995 nm of Polysilicon. Therefore, the etched areas should reach a depth of 1805 nm. In the lower corner of MX19002-208, a gap height of 1570 nm was achieved. The difference between the achieved height (1570 nm) and the wanted etching height (1805 nm) was 235 nm. In the description of the Omega tool, it was found that the etch rate of the SiNx in the tool was equal to 3.33 nm/s. Since MX19002-208 was etched for 60 seconds, the Omega tool should have etched 199.8 nm of SiNx. Therefore, the gap height may have been reduced by the decrease in the thickness of the SiNx layer. If these assumptions are correct, the Polysilicon layer and the SiNx layer may have been fully etched. The etching of the SiNx in the Omega tool decreases the thickness of the SiNx. This may explain the results found from the height gap measurements on the wafer MX19002-211.

Subsequently, Dektak was used to estimate the width of the holes of MX19002-208:

- Left point: The hole width was equal to 40 μm. The spacing was equal to 50 μm.
- Right point: The hole width was equal to 40 μm. The spacing was equal to 50 μm.
- Upper point: The hole width was equal to 100 μm. The spacing was equal to 100 μm.
- Lower point: The hole width was equal to 30 μm. The spacing was equal to 40 μm.

Through a microscope inspection, it was possible to see that MX19002-208 achieved a better etching quality of the SiNx and polysilicon layer on the wafer. To understand the most precise etching, it was necessary to measure the original dimensions of the width of the holes in the pattern of the mask. To make this estimate, a wafer with the original masking pattern was measured under a microscope. The original pattern presented the following widths:

- Left point: The hole width was equal to 40 μm. The spacing was equal to 50 μm.
- Right point: The hole width was equal to 40 μm. The spacing was equal to 50 μm.
- Upper point: The hole width was equal to 100 μm. The spacing was equal to 100 μm.
- Lower point: The hole width was equal to 30 μm. The spacing was equal to 40 μm.

Therefore, the MX19002-208 wafer showed a more accurate etching.
The results of these tests are summarized as follows:

Wafer Number	LPCVD SiNx etch-rate	LPCVD Polysilicon etch-rate
208	6.6 nm/s	12.2 nm/s
211	6.335 nm/s	9.21 nm/s

C.2 Back-plate Deep Reactive Ion Etching

This test was performed to understand the critical steps involved when etching the wafer from the back-side. To this end, 1 single polished wafer was taken. The wafer was processed with photolithography to create the zero layer with the alignment marks that will be used in the future masking steps. Dry-etching was performed. Oxide growth time was calculated using the online simulator [28]. These wafers should have an oxide thickness of 1 μm. The number of the single polish wafer used is the following:

- 201911-1-1311

201911-1-1311 was processed with photolithography and dry-etched. The etching time was set to 38 seconds to etch 300 nm of thermal oxide. The etched depth was measured in Dektak and found to be 298 nm. The wafer was processed with photolithography and dry-etched. The wafer was left in the polysilicon furnace overnight so that 1 μm of polysilicon could be deposited. Therefore, the obtained structure that will be used for the realization of the back-plate is depicted in Fig.63.

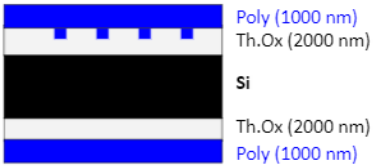


Figure 63: Wafer 201911-1-1311.

Wafer 201911-1-1311 was dry-etched to remove 1 μm of polysilicon on the back-plate. Subsequently, it was inserted in Novellus to deposit 5 μm of SiO_2 on the top surface. Then, it was placed in Novellus for a backside deposition of 3 μm of SiO_2.
The structure of the wafer is depicted in Fig.64.

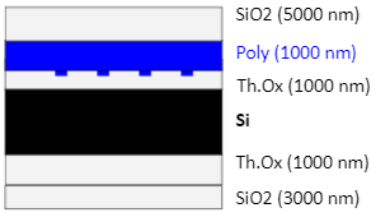


Figure 64: Wafer 201911-1-1311.

Wafer 201911-1-1311 was processed with lithography and dry-etched. The goal was to etch 3 μm of SiO_2 and 1 μm of thermal oxide on the back-side, thus 4 μm of oxide. Later on, AMS110 was used to perform DRIE on the silicon layer. Summing the various etching time, the wafers were etched by DRIE for 70 minutes. It was possible to see that the silicon was fully removed with a microscope inspection. On the other hand, it was assumed that some residual thermal oxide was still present (1 μm - 200 nm of residual etching, thus 800 nm of thermal oxide).
The structure of the wafer is depicted in Fig.65.

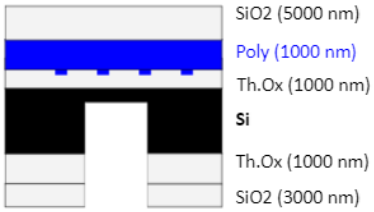


Figure 65: Wafer 201911-1-1311.

The wafers were inspected with a digital microscope to confirm the residual thermal oxide hypothesis. Some pictures of the large membranes depict different colors of the membranes suggesting the presence of different thicknesses. Also, for small holes on the backside and near the edge of the wafer, some membranes were completely closed or partially opened, so the thermal oxide was still present. The images obtained with the digital microscope are depicted in Fig.66.
To fully remove the thermal oxide layer on 1311 (the layer with 200 nm of residual etching, hence a layer of 800 nm of thermal oxide), a BHF (1:7) etching line was used. Wafer 1311 was inserted in a BHF (1:7) bath to fully remove 800 nm of thermal oxide (1 μm minus 200 nm of residual etching). Since the thermal oxide etching rate in BHF is approximately 75 nm/min, 11 minutes of etching were performed. On the other hand, the BHF will etch the SiO_2 on the top side (5 μm of SiO_2 grown in Novellus). The etch rate of SiO_2 in BHF is 275 nm/min. Therefore, in 11 minutes, 3 μm of SiO_2 will be etched on the top side. During a microscope inspection, it was impossible to see any white flakes on the top side of 1311. These flakes are a product of the BHF etching. If the wafer is placed in water for rinsing immediately after the BHF, these white flakes will be trapped inside the wafer cavities. Therefore, some water and Triton solution was used. Triton is a detergent, thus, when combined with water, it can cause the BHF flakes to escape the cavities. This will reduce the number of occluded cavities, allowing for proper airflow.

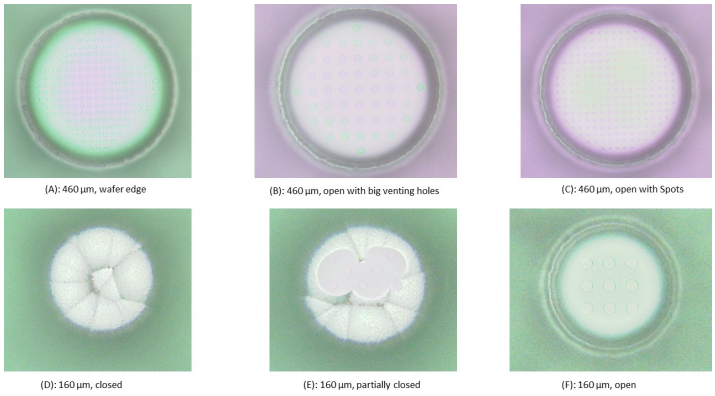


Figure 66: Back openings on wafer 201911-1-1311 after SF_6 plasma etching is AMS110. (A) is a 460 μm back opening on the edge of the wafer. (B) is a fully open 460 μm back opening. It is possible to see the 20 μm venting holes on top of the thermal oxide. (C) is a 460 μm back opening with some color spots indicating the presence of different thicknesses on the etched surface. (D) is a 160 μm closed back opening. (E) is a partially closed 160 μm back opening. As a matter of facts, some venting holes are visible from the back opening. (F) is a 160 μm fully open back opening.

Wafer 1311 was inspected using a digital microscope to depict the flakes created after BHF. The images of the cavities are depicted in Fig.67.

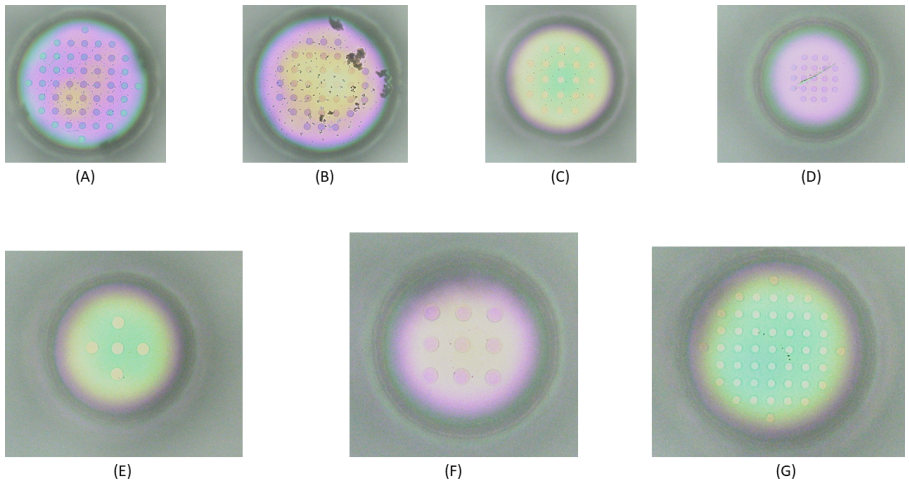


Figure 67: Back openings on wafer 201911-1-1311 after SF_6 plasma etching is AMS110 and BHF (1:7) etching. (A) is a 460 μm back opening with no BHF flakes. (B) is a 460 μm back opening with some BHF flakes. (C) is a 460 μm back opening with some small BHF flakes. (D) is a 160 μm back opening with some BHF flakes. (E) is a 160 μm back opening with no BHF flakes. (F) is a 160 μm back opening with no BHF flakes. (G) is a 160 μm back opening with some BHF flakes.

Wafer 1311 was inserted in AMS110 for DRIE of the polysilicon layer. Wafer 1311 was DRIE on the backside for 2 minutes and 30 seconds. As shown in Fig.69, some venting holes were completely open. Therefore, to fully open all the venting holes, 1 minute and 30 seconds of additional etching were performed using the same recipe. The width of these holes was not a decisive parameter since both the 10 μm and the 20 μm venting holes were open.

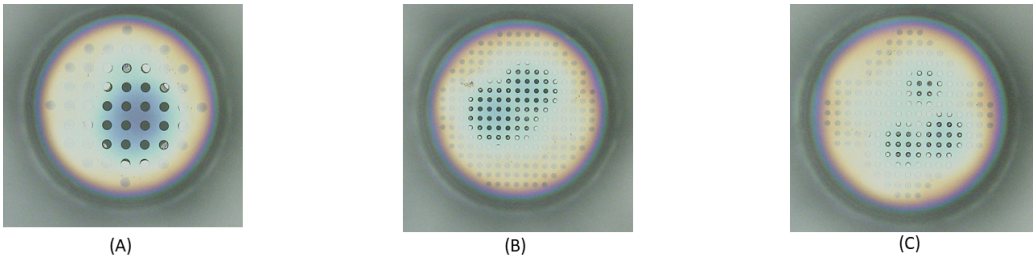


Figure 68: Back openings on wafer 201911-1-1311 after SF_6 plasma etching is AMS110, BHF (1:7) etching and SF_6 plasma etching. (A) is a 460 μm back opening partially Open. (B) is a 460 μm back opening partially Open. (C) is a 460 μm back opening partially Open.

Therefore, some holes were visible after performing BHF and plasma etching. To this end, 6 minutes and 11 seconds of SF_6 were required. After another 1 minute and 30 seconds (total etching time after BHF equal to 7 minutes and 41 seconds), most of the holes on the top and bottom part of the backside of the wafer were open. Not all the holes were open in the center as shown in Fig.69. This could be related to Drytek. 1311 presented a spot on the center of the wafer after Drytek etching was performed.

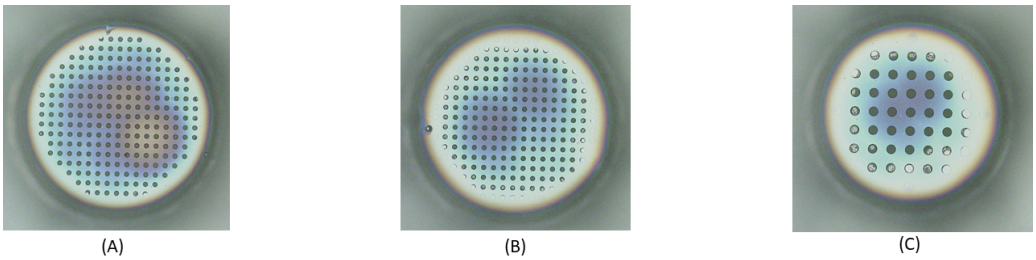


Figure 69: Back openings on wafer 201911-1-1311 after SF_6 plasma etching is AMS110, BHF (1:7) etching and two runs of SF_6 plasma etching. (A) is a 460 μm back opening Open. (B) is a 460 μm back opening Open. (C) is a 460 μm back opening Open.

Venting holes have been created. Therefore, a total etching time in DRIE of 10 minutes and 11 seconds was required to perforate the polysilicon layer. Later on, wafer 1311 was diced (including along the holes) to perform a cross-sectional inspection in an SEM microscope. Fig.70 depicts the large holes (460 μm) on the backside. The width of the holes varies in the image since the wafer was diced by hand.
Fig.71 depicts the width of the hols (19.6 μm) which is in line with the designed values.
Fig.72 shows that the polysilicon was 1.06 μm thick and that it was completely perforated. The holes have a width of 19.6 μm as expected. Furthermore, the PECVD oxide was reduced from 5 μm to 2.87 μm as correctly predicted from calculations using the BHF etch rate.

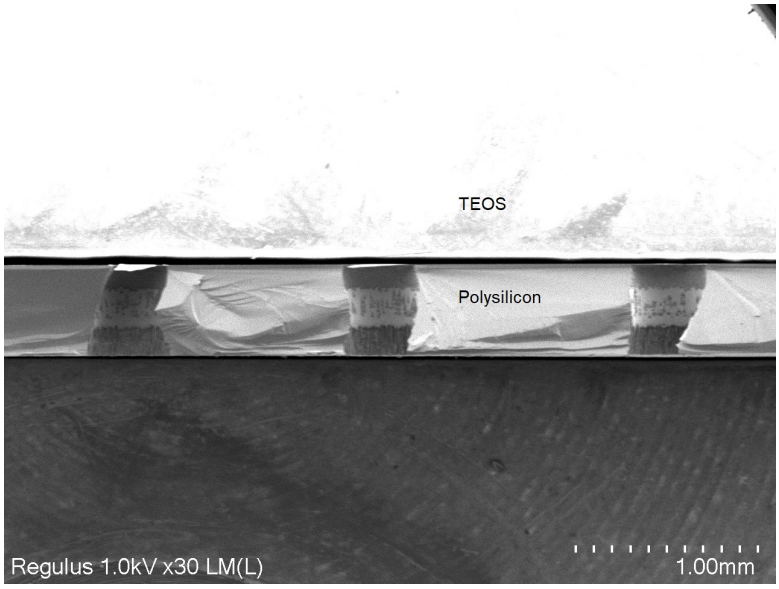


Figure 70: SEM Cross Section, Polysilicon perforation.

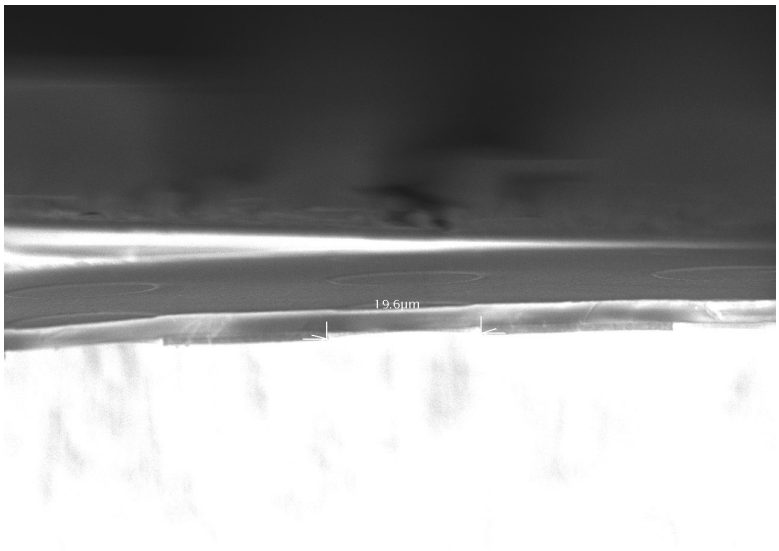


Figure 71: SEM Cross Section, Hole width.

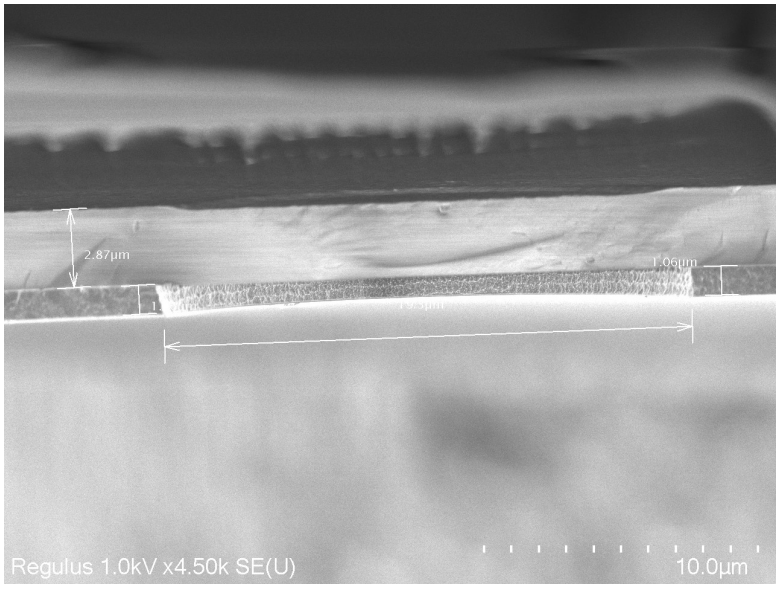


Figure 72: SEM Cross Section, various dimensions: Polysilicon is 1.06 μm; Holes Width of 19.5 μm and pecvd oxide of 2.87 μm.

Wafer 1311 was etched in VHF to remove 2.7 μm of PECVD SiO_2. Therefore, recipe 5 was used in 3 cycles each of 4 minutes. To work safely, the chip was purged multiple times once the process ended. Later on, the wafer was inspected using a digital microscope. This step was crucial as, if some PECVD oxide flakes are detected, the chip will be baked at a temperature of 200 °C for 1 minute. This test was performed to determine the quality and color of the polysilicon after the backside process. By observing the color changes, it was possible to determine the etching of the layer. Some flakes were observed during microscope inspection, so the chip was baked. The topside and the backside are depicted in Fig.73.

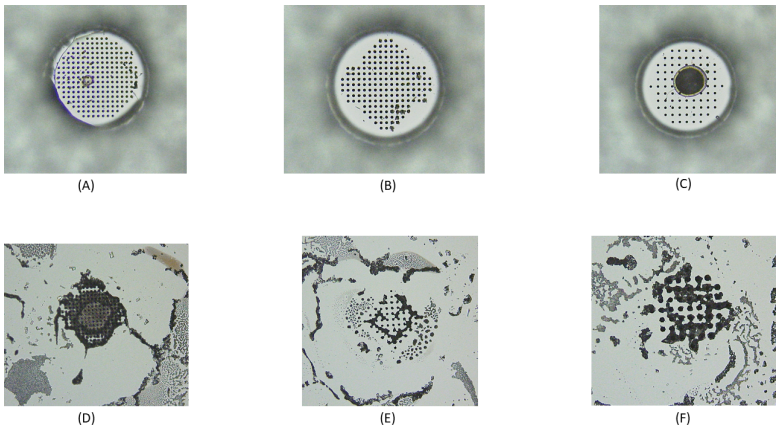


Figure 73: Chip from wafer 201911-1-1311 after SF_6 plasma etching is AMS110, BHF (1:7) etching,SF_6 plasma etching and VHF. (A) is a 460μm back opening.
(B) is a 460μm back opening. (C) is a 460μm back opening. (D) is a 160μm Venting Holes Top Side. (E) is a 160μm Venting Holes Top Side. (F) is a 160μm Venting Holes Top Side.

The chip, after baking, was captured using a digital microscope. The obtained images are depicted in Fig.74

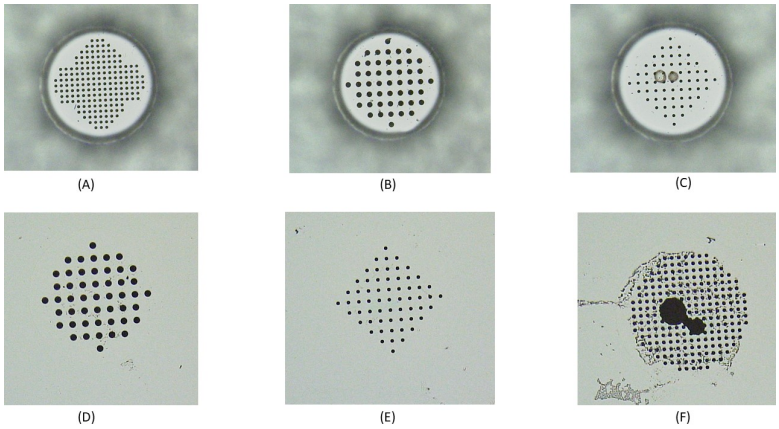


Figure 74: Chip from wafer 201911-1-1311 after SF_6 plasma etching is AMS110, BHF (1:7) etching,SF_6 plasma etching, VHF and Backing. (A) is a 460 μm back opening. (B) is a 460 μm back opening. (C) is a 460 μm back opening. (D) is a 160 μm Venting Holes Top Side. (E) is a 160 μm Venting Holes Top Side. (F) is a 160 μm Venting Holes Top Side at the edge of the chip.

Therefore, it was possible to successfully realize the venting holes and the back cavity using a back-side etching. The etching times and the recipes obtained will be used in the final process for the realization of a graphene-based condenser microphone.

C.3 Gold Adhesion & Tapered Sidewalls For Contact With The Bottom Electrode

To realize the gold pads, some tests should be conducted to understand the criticality of this process. The gold should enter in the substrate and reach the back-plate. To do so, gold lift-off is required. Unfortunately, with dry etching, straight walls will not allow gold to adhere to the lateral surfaces, while on the top and bottom surfaces the adhesion is guaranteed. On the other hand, with wet etching, the sidewalls will have an inclination that will allow the gold adhesion, but the etched surface area will increase.

C.3.1 Wet & Dry etching

A test on the slope of the side walls when the side walls were created from a mixture of wet and dry etching was conducted on a wafers. The number of this wafer is MX19004-004. The wafer was inserted in the Novellus tool for a PECVD TEOS deposition (5 μm). The test wafer was annealed for 1 hour at 1000 °C with a nitrogen flow. Subsequently, 150 nm of SiNx were deposited. The main objective of this test is to perform a mixture of dry and wet etching (which will create lateral walls that are not straight but have a slope) to understand the gold adhesion to the bottom electrode.

Wafer-004, was processed with photolithography and dry-etched to create openings for the molybdenum, so 150 nm of SiNx were removed on the top side of the wafers by dry-etching. Photolithography was performed on wafer-004. To etch 5 μm of PECVD TEOS in BHF, an etching time of 32 minutes was required. The etching time was divided into 3 steps. Halos and structures were measured after each wet etching. The results of these measures are depicted in Fig.75.

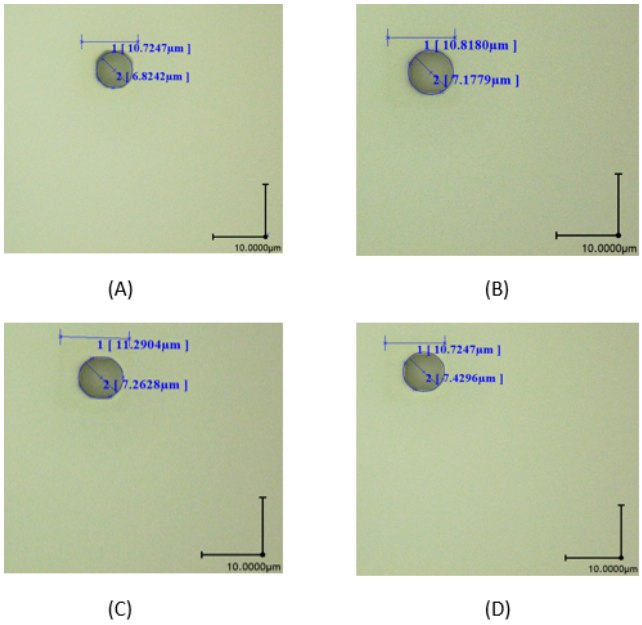


Figure 75: (A): Wafer -004 before BHF. (B): Wafer -004 after 12 minutes of BHF. (C): Wafer -004 after 22 minutes of BHF. (D): Wafer -004 after 34 minutes of BHF.

Wafer -004 was processed for 32 minutes in BHF to etch the TEOS. As already mentioned, this resulted in a TEOS etching of between 500 and 900 nm.
Furthermore, 4 minutes of Drytek removed 2500 nm of TEOS. Therefore, only between 2000 nm and 1600 nm of TEOS were found on the wafer surface. Therefore, 64 minutes of BHF (resulting in an etching having a range between 1000 nm and 1800 nm) will be performed in 2 steps of 22 minutes and 1 step of 20 minutes. At the end of every BHF etching, the wafer will be rinsed and inspected with a digital microscope to monitor the feature changes. Fig.76 depicts the wafer after 22 minutes of BHF. Fig.77 depicts the wafer after 44 minutes of BHF.

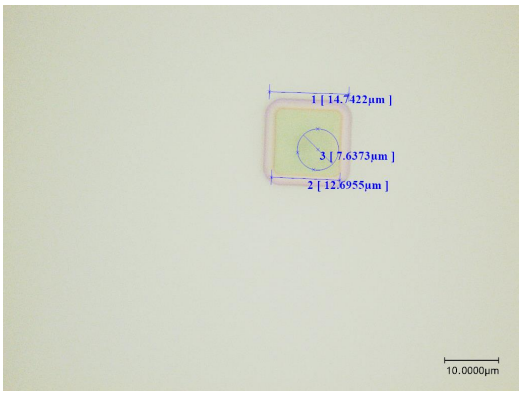


Figure 76: Wafer -004 after 22 minutes of BHF

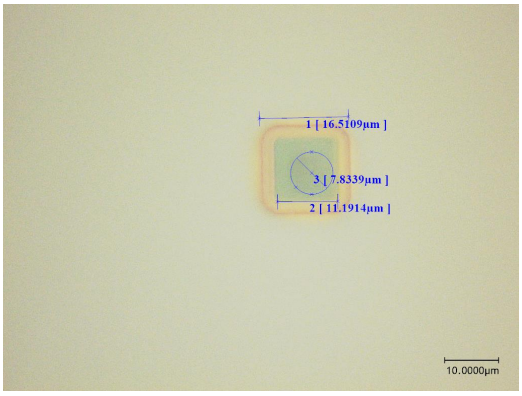


Figure 77: Wafer -004 after 44 minutes of BHF.

The side walls had a slope which was calculated to be approximately 58 °. This slope may be sufficient for proper metal coverage of the sidewalls.

C.3.2 Contact Holes for Bottom Electrode

Fig.78 depicts the test wafer -0145 and the ideal structure that should be obtained after processing. This test wafer was used to create the openings for the bottom electrode. These openings should be about 10 μm deep. Furthermore, the lateral walls must have a slope. This slope will facilitate the gold adhesion, thus creating a good contact hole. Due to the need for a large vertical depth and the need for a slope for these lateral walls, wet and dry etching were combined.

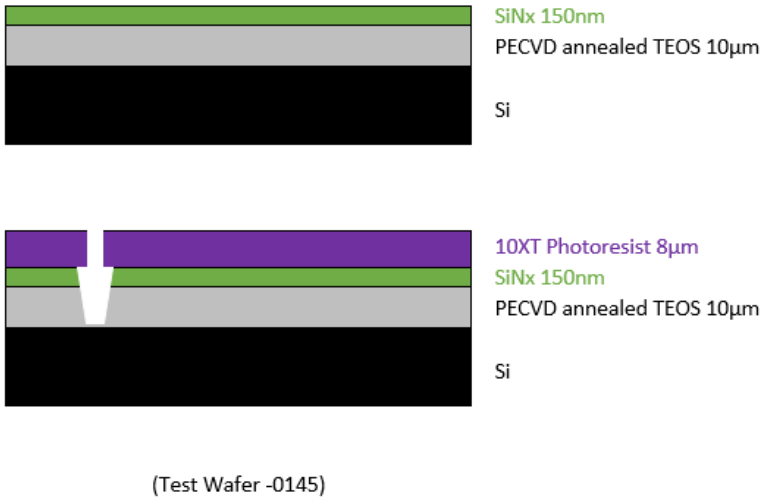


Figure 78: Top images depicts wafer -0145 while the bottom image depicts the ideal final result the process engineer would like to obtain on top of wafer -0145.

At first, the 12XT photoresist data-sheet [32] was studied to understand the exposure time of a 8 μm thick photoresist layer. After the exposure, the wafer was developed using recipe DEV 12XT. Using Dektak, the measured thickness was equal to 3 μm which was not sufficient. Therefore, another run of DEV 12XT was performed. The measured thickness was now 3.7μm which, again, was not sufficient. Therefore, the photoresist was stripped twice using recipe 1 in Tepla.

Once again, a 12XT photoresist with a thickness of 8 μm was coated on the top side of the wafer. Now, the wafer was exposed and developed using recipe DEV 12XT. Using a microscope, it was possible to observe some bubbles on the top surface of the wafer. Using Dektak, the depth on the alignment marks was measured as the

hole size for the bottom electrode was too small and did not allow for measurements. The measured depth was equal to 7 μm, but the surface was too rough. Therefore, using recipe DEV 12XT, another development was performed, but the quality was not promising so the photoresist was stripped.

Again, a 12XT photoresist with a thickness of 8 μm coated on the top side of the wafer. Now, the exposure time was set to 100 seconds. These 100 seconds of exposure were divided into 5 steps. Each step consisted of 20 seconds of exposure, followed by 10 seconds of no exposure. This was done because a single 100 seconds exposure of the wafer to UV light could raise the temperature of the wafer, thereby compromising the quality of the photoresist. Furthermore, the development was performed manually. The development was divided into 3 steps, each lasting 1 minute. Therefore, wafer -0145 was developed in a total time of 3 minutes in MF322 Developer. The surface was homogeneous. Furthermore, Dektak measured 7 μm of depth. This result was good in line with that expected.

Therefore, the wafer was dry-etched to remove 150 nm of SiNx and the wafer was dry-etched to remove approximately 6 μm of PECVD annealed TEOS. Therefore, using acetone, the photoresist was manually removed from the alignment marks on the right side of the wafer, so it was possible to measure the etched depth in Dektak. The depth measurement was 2 μm. Hence, the PECVD annealed TEOS was dry-etched for an extra 7 minutes and 15 seconds. Again the photoresist on the alignment marks was manually stripped in acetone to measure the etched depth since the depth of the alignment marks was the only measurable feature as the contact openings were too small (5 μm x 5 μm) to be detected by Dektak. On the alignment marks, the measured depth ranged between 6.2 μm and 6.5μm. This result was acceptable. Therefore, the wafer was inspected with a digital microscope to obtain some images. These pictures are depicted in Fig.79 and Fig.80.

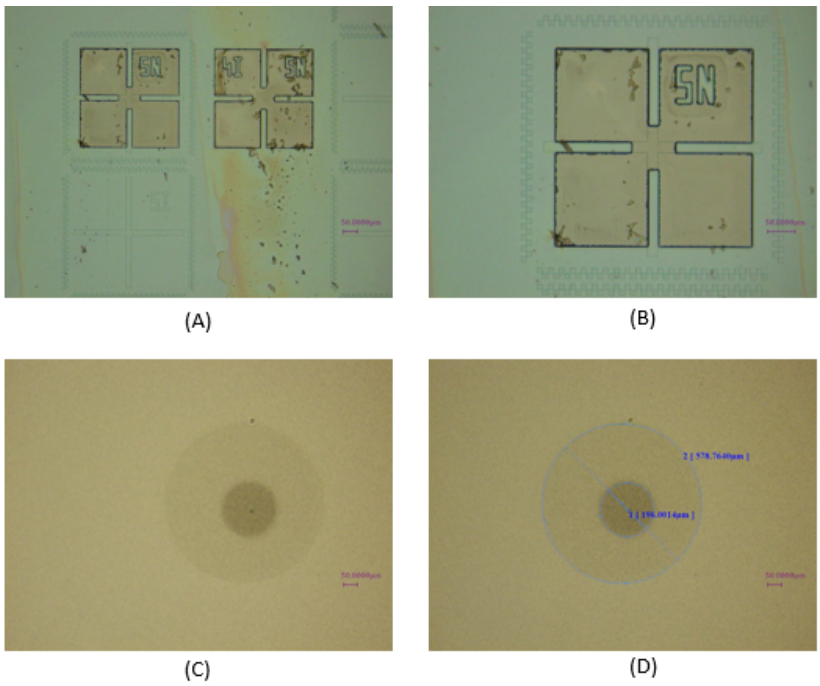


Figure 79: (A) and (B) depicts the alignment marks after the dry etching. (C) and (D) depicts the contact openings of the bottom electrode with the related halos.

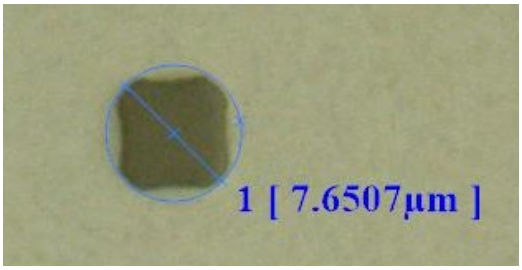


Figure 80: Contact openings of the bottom electrode.

Subsequently, the photoresist was stripped in Tepla using recipe 1 twice. The wafer was measured in Dektak. The measured etched depth ranged between 6.3 μm and 6.6 μm. The wafer was captured as depicted in Fig.81.

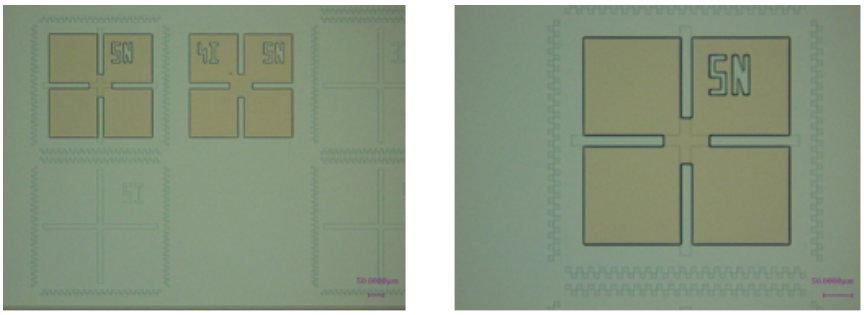


Figure 81: (A) and (B) depicts the alignment marks after the dry etching and after the photoresist strip.

Therefore, 3.5 μm of PECVD annealed TEOS were left on the wafer's contact openings. To fully remove this thickness, 50 minutes of BHF wet etching must be performed on the wafer. On the other hand, approximately 1 μm of PECVD annealed TEOS should be left in the contact openings to prevent SiC formation. Therefore, the wafer was etched in 10 minutes increments for a total time of 35 minutes. The wafer was captured and measured once every step was concluded. The results of these etchings are depicted in the following images.

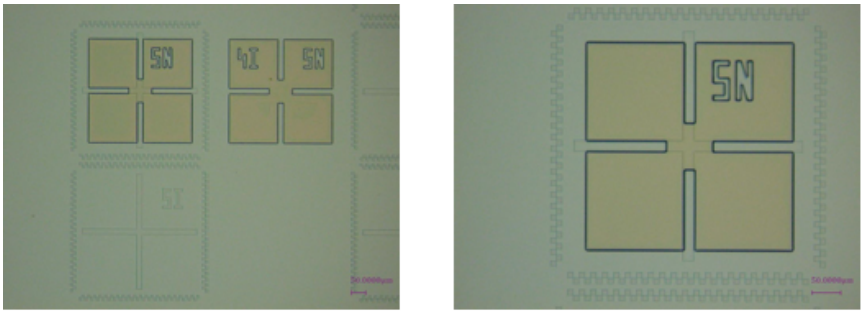


Figure 82: (A) and (B) depicts the alignment marks after the dry etching, after photoresist strip and after 10 minutes of BHF.

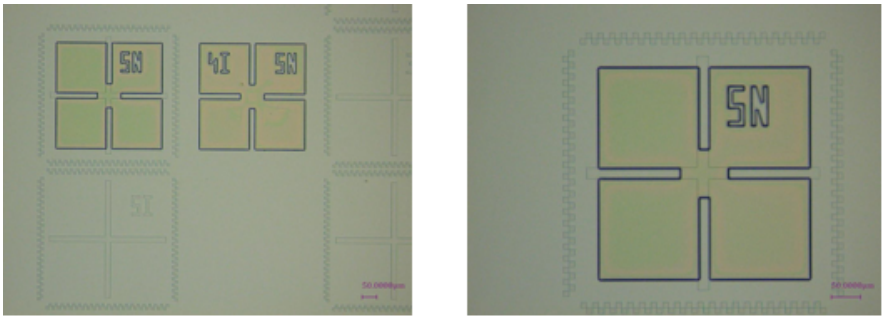


Figure 83: (A) and (B) depicts the alignment marks after the dry etching, after photoresist strip and after 20 minutes of BHF.

Figure 84: (A) and (B) depicts the alignment marks after the dry etching, after photoresist strip and after 30 minutes of BHF.

Figure 85: (A) and (B) depicts the alignment marks after the dry etching, after photoresist strip and after 35 minutes of BHF.

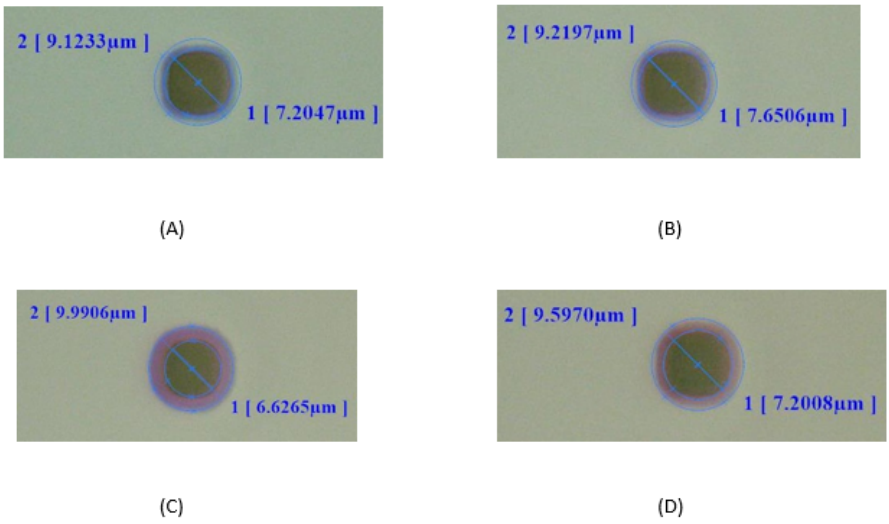


Figure 86: (A) Contact hole and relative halo after 10 minutes of BHF. (B) Contact hole and relative halo after 20 minutes of BHF. (c) Contact hole and relative halo after 30 minutes of BHF. (D) Contact hole and relative halo after 35 minutes of BHF.

Furthermore, after each wet etching step, the etched depth was measured in Dektak. The results are reported as follows:

- After 10 minutes of BHF etching: 7.3 μm.
- After 20 minutes of BHF etching: 8 μm.
- After 30 minutes of BHF etching: 8.8 μm.
- After 35 minutes of BHF etching: 9.2μm.

These results will be used in the main process to properly wet-etch the TEOS opening.

Appendix D VHF For The Release of The Mechanical Graphene Layer

The last part of the flowchart (release of the membrane through VHF etching) was considered for this test. Wafers 201911-1-1080 (also called "1080") and 201911-1-1086 (also called "1086") having the cross-section depicted in Fig.87 and Fig.88 were diced and processed using Vapor HF (VHF) with different recipes. In the final device, the TEOS thickness will be much higher than that of the SiNx. Therefore, a thickness difference was imposed on the test wafers in the TEOS and SiNx layers. The difference in the recipes is depicted in Tab.8 where uniformity is calculated on a thermal oxide layer. This test was performed to understand which recipe is the most suitable for the present process, to understand the under-etching, and understand how much TEOS will be etched. Furthermore, the VHF will not only attack the wafer from the back-side, but the top-side will also be etched. A study on the top-side etching will clarify the condition of the SiNx upper layer after the etching.

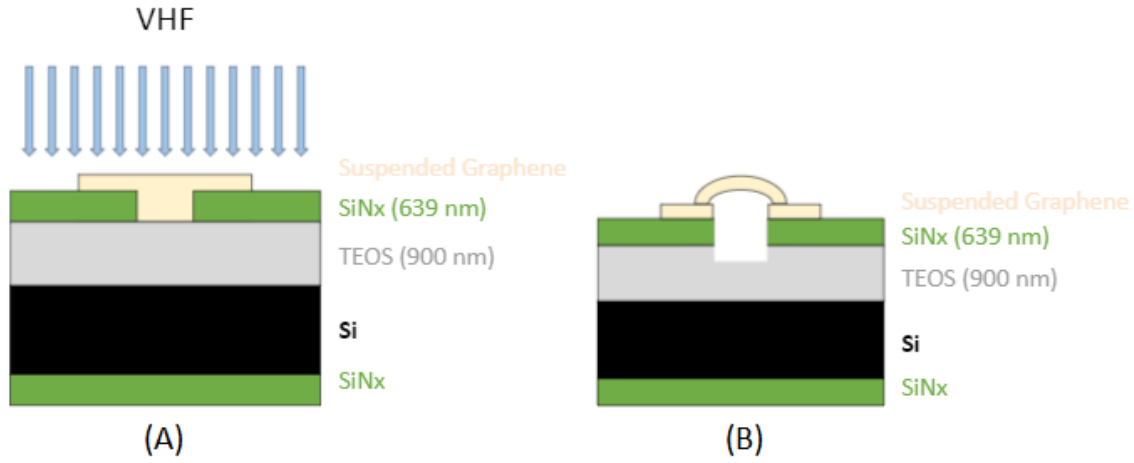


Figure 87: Cross section of wafer 1080. (A) depicts the structure before VHF. (B) depicts the structure after VHF.

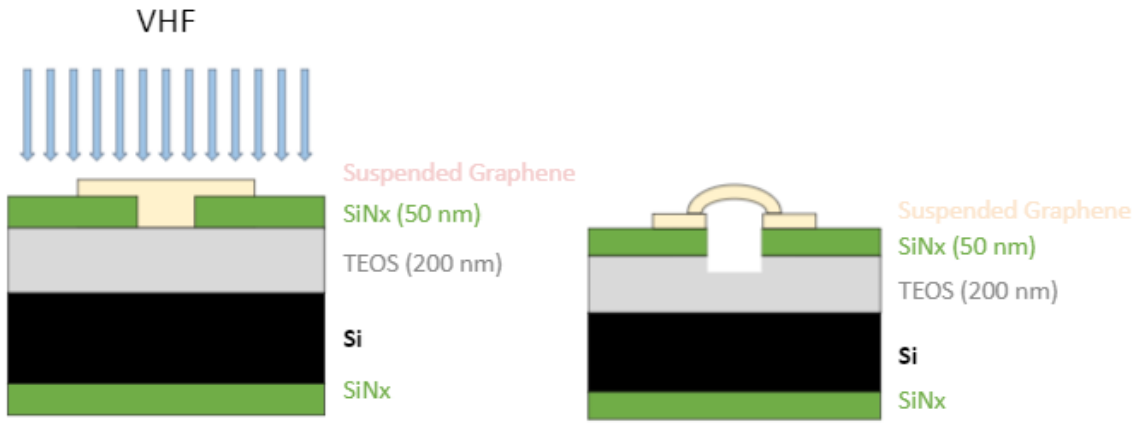


Figure 88: Cross section of wafer 1086. (A) depicts the structure before VHF. (B) depicts the structure after VHF.

Recipe Number	**Pressure (Torr)**	**HF (sccm)**	**EtOH**	N_2 **(sccm)**	**Regulator**	**Uniform** $R/2x\%$
1	125	190	210	1425	7.5	2.9%
2	125	310	3500	1250	7.5	5.2%
5	125	720	325	880	7.5	1.3%

Table 8: VHF recipes Parameters

Not all recipes were successful. Suspended graphene was observed when two recipes were used: Recipe 1 for 300 seconds in 2 cycles and Recipe 2 for 300 seconds in cycles. After the etching, a pH test was performed on some samples of 1086. Since the VHF tool uses a hydrofluoric acid (HF) vapor, the processed chips may have some hydrofluoric acid particles on the surface. Hydrofluoric acid is a highly corrosive material, therefore some specific tests have been performed to ensure the highest safety standards.
Once 1086 was diced and molybdenum was removed, recipe 1 for 300s in 2 cycles was run on 2 chips. Later, one of the two chips was sealed in a closed box with litmus paper. The other chip was baked at 250 °C for 2 minutes. Once the baked chip completely cooled, it was sealed in a closed box with litmus paper. The two sealed boxes were left for several hours in a safe environment. After around 24 hours, the sealed boxes were opened and the two pieces of litmus paper were observed. The unbaked chip had a pH of about 4 which corresponds to an acidic material. On the other hand, the baked chip exhibited a neutral pH. To increase safety, the VHF purge time can be increased from 5 minutes 30 seconds to 15 minutes or more. Another possibility is to place the chips into a vacuum chamber. The hydrofluoric acid left on the chips is generally mixed with water and can be trapped between the graphene and the SiNx layer. A vacuum chamber would help eliminate the remaining hydrofluoric acid as it will force the water to evaporate.
The depth of the etched holes was measured using Dektak.
The results are depicted in Fig.89 and Fig.90 which analyze wafer 1080 and 1086 respectively.

Wafer Number	Recipe Number (#)	Recipe Time (s)	Recipe Cycles (#)	SiNx Thickness (nm)	TEOS Thickness (nm)	Measured Depth (nm)	Yield (%)
201911-1-1080	1	150	1	630	889	753	Low
201911-1-1080	1	300	1	630	889	1144	Low
201911-1-1080	1	300	2	630	889	944	≈80
201911-1-1080	2	150	1	630	889	866	Low
201911-1-1080	2	300	1	630	889	1040 (1028 small-holes)	Low
201911-1-1080	2	300	2	630	889	1333 (smooth surface)	≈60
201911-1-1080	5	150	1	630	889	734	Low
201911-1-1080	5	300	1	630	889	1440	Low

Figure 89: Processed data for wafer 1080.

Wafer Number	Recipe Number (#)	Recipe Time (s)	Recipe Cycles (#)	SiNx Thickness (nm)	TEOS Thickness (nm)	Measured Depth (nm)	Yield (%)
201911-1-1086	1	150	1	53	193	99	Low
201911-1-1086	1	300	1	53	193	184	Low
201911-1-1086	1	300	2	53	193	228	≈80
201911-1-1086	2	150	1	53	193	146	Low
201911-1-1086	2	300	1	53	193	206	Low
201911-1-1086	2	300	2	53	193	241	Unknown
201911-1-1086	5	150	1	53	193	Too Rough To Measure	Unknown
201911-1-1086	5	300	1	53	193	Not Measurable (no structures)	Unknown

Figure 90: Processed data for wafer 1086.

Additionally, the etching rates of 1080 and 1086 were plotted in 2 graphs. These graphs can be found in Fig.91 and Fig.92 which show the etching rate of 1080 and 1086 respectively.

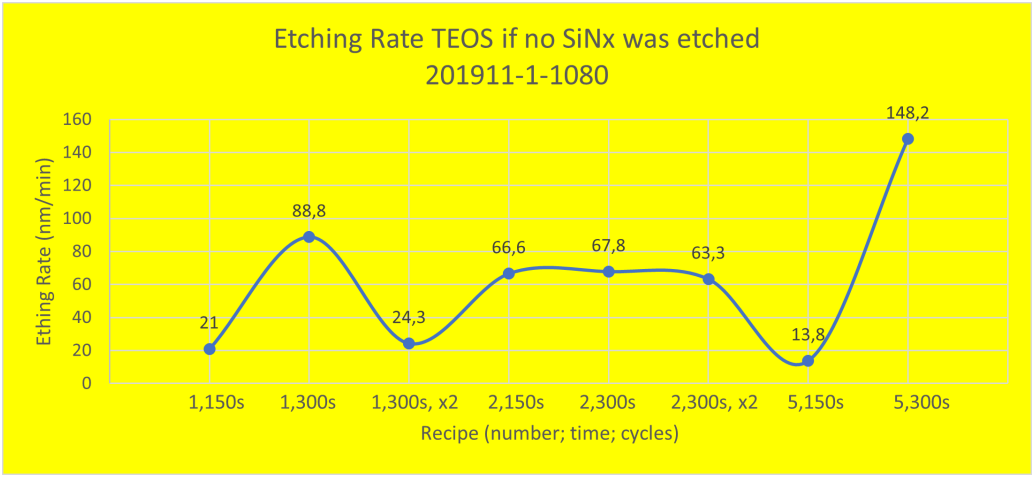


Figure 91: Etching rates of 1080. On the X-axis, the recipe number, the etching time in seconds and the number of cycles is depicted. On the Y-axis, the ethcing rate (nm/min) is depicted.

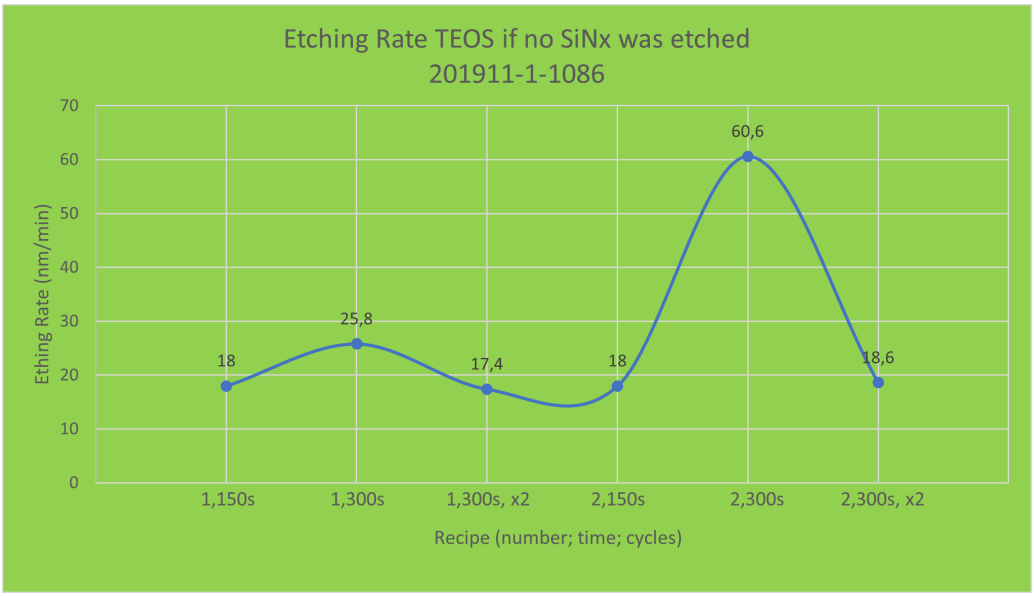


Figure 92: Etching rates of 1086. On the X-axis, the recipe number, the etching time in seconds and the number of cycles is depicted. On the Y-axis, the ethcing rate (nm/min) is depicted.

Unfortunately, this test was not completely successful as the VHF etching was too non-uniform, but the yield and the etching produced by recipe 1 seemed to be best suited to the presented process. The difference in the obtained results on the 2 wafers may be linked to the non-uniformity of the etching.

Appendix E Flowchart

1. COATING AND BAKING: top-side (“CO 3012 – 1.4 um – no EBR" photoresist).
2. ALIGNMENT AND EXPOSURE (120 mJ/cm2).
3. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
4. PLASMA ETCHING – Alignments markers on Silicon.
5. THERMAL OXIDATION (wet oxidation. target thickness 1 um).
6. LPCVD SiNx (100 nm)
7. COATING AND BAKING: top-side (“CO 3012 – 1.4 um – no EBR" photoresist).
8. EXPOSURE (11.4 mJ/cm2).
9. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
10. PLASMA ETCHING SiNx (holes for future Poly-Si perforated bottom electrode).
11. LPCVD Poly-Si (1000 nm).
12. DOPING + ANNEALING (activation of Poly-Si: Boron, Doping dose 5E15/cm2, Ion energy 45 keV).
13. 4-PROBE MEASUREMENT (Rsheet of the Poly-Si).
14. COATING AND BAKING: top-side (“CO 3027 – 3.1 um – no EBR” photoresist).
15. EXPOSURE (11.4 mJ/cm2).
16. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
17. PLASMA ETCHING (remove all Poly-Si).
18. PECVD TEOS (5 um).
19. ANNEALING (Improve crystalline structures for future VHF).
20. LPCVD SiNx (100 nm).
21. PLASMA ETCHING of SiNx and Poly-Si (backside).
22. PECVD TEOS (5 um on backside for future etching mask for DRIE of Si).
23. COATING AND BAKING: top-side (“CO 3012 – 1.4 um – no EBR" photoresist).
24. EXPOSURE (11.4 mJ/cm2).
25. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
26. PLASMA ETCHING SiNx (opening for future Mo).
27. COATING AND BAKING: top-side (“CO 3027 – 3.1 um – no EBR” photoresist).
28. EXPOSURE (11.4 mJ/cm2)
29. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
30. PLASMA ETCHING TEOS (opening for future DRIE of Si).
31. SPUTTERING 50 nm Molybdenum.
32. COATING AND BAKING: top-side (“CO 3027 – 2.4 um – no EBR” photoresist).

33. EXPOSURE (11.4 mJ/cm2)
34. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
35. PLASMA ETCHING molybdenum.
36. COATING AND BAKING: top-side ("CO 3027 – 3.1 um – no EBR" photoresist).
37. EXPOSURE (11.4 mJ/cm2)
38. DEVELOPMENT (post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer and a hard bake at 100°C for 90 seconds).
39. DRY/WET ETCHING (creation of the contact for bottom electrode).
40. CVD Graphene.
41. MANUAL COATING AND BAKING (NLOF2020 photoresist).
42. CONTACT ALIGNER EXPOSURE (100 seconds in 5 steps).
43. BAKING and DEVELOPMENT (MF322 developer).
44. WET-ETCHING (residual layer of annealed PECVD TEOS).
45. CR AND AU EVAPORATION.
46. LIFT-OFF.
47. DRIE SILICON (AMS110).
48. Mo WET ETCHING (Hydrogen peroxide).
49. WET ETCHING (thermal oxide layer).
50. DRIE (Poly-Si).
51. VHF (PECVD annealed TEOS).

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