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# A Comprehensive Classification of State-of-the-Art Distributed Maximum Power Point Tracking Architectures for Photovoltaic Systems

AFSHIN NAZER  <sup>1</sup>, OLINDO ISABELLA  <sup>1</sup>, AND PATRIZIO MANGANELLO  <sup>2</sup>

<sup>1</sup>Delft University of Technology, 2628 CD Delft, The Netherlands

<sup>2</sup>Hasselt University, 3500 Hasselt, Belgium

CORRESPONDING AUTHOR: AFSHIN NAZER (e-mail: A.Nazer@tudelft.nl)

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**ABSTRACT** In photovoltaic (PV) systems, unavoidable factors, such as partial shading, nonoptimal mounting angles of PV modules, and accumulation of dust result in mismatches, consequently diminishing energy yield. A promising solution to mitigate these issues is to use distributed maximum power point tracking (DMPPT) architectures. To alleviate mismatch-related losses, many DMPPT architectures, including full power processing (FPP) and differential power processing (DPP), have been documented in the literature. FPP encompasses techniques, such as microinverters, modular multilevel cascade inverters, and dc architectures, such as parallel, series, and total cross-tied. DPP variants include series DPP, parallel DPP, and series-parallel DPP architectures. Moreover, novel DMPPT architectures, such as hybrid and hierarchical architectures, along with advancements in converter topologies and control strategies, continue to emerge, aiming to improve levelized cost of energy. Each novel solution brings distinct advantages and challenges, but the extensive number of architectures, power converters topologies, and control methods have led to confusion and complexity in navigating the literature. This article systematically categorizes, reviews, and compares various DMPPT architectures, associated converters, and control strategies, providing a comprehensive overview of the evolving landscape of DMPPT development. By elucidating existing advancements and identifying gaps for further research, this review aims to offer clarity and guidance in advancing DMPPT technology for enhanced PV system performance.

**INDEX TERMS** DC optimizers, distributed maximum power point tracking (DMPPT), differential power processing (DPP), full power processing (FPP), mismatch conditions, modular multilevel cascade inverters (MMCI), parallel differential power processing (PDPP), partial shading, photovoltaic (PV) systems, photovoltatronics, series differential power processing (SDPP).

## NOMENCLATURE

2L-VSI	Two-level voltage source inverter.	DSFC	Double-star full-bridge cell.
3L-ANPC	Three-level active neutral-point-clamped.	DSHC	Double-star half-bridge cell.
3L-NPC	Three-level neutral-point-clamped.	EMI	Electromagnetic interference.
ALC	Array level converters.	FPP	Full power processing.
CIC	Cell integrated converters.	HFT	High-frequency transformer.
DMPPT	Distributed maximum power point tracking.	<i>I</i> - <i>V</i>	current-voltage.
DPP	Differential power processing.	LCOE	Levelized cost of energy.
DSCC	Direct switched-capacitor converter.	LPPT	Least power point tracking.
		LSCC	Ladder-type switched-capacitor converter.

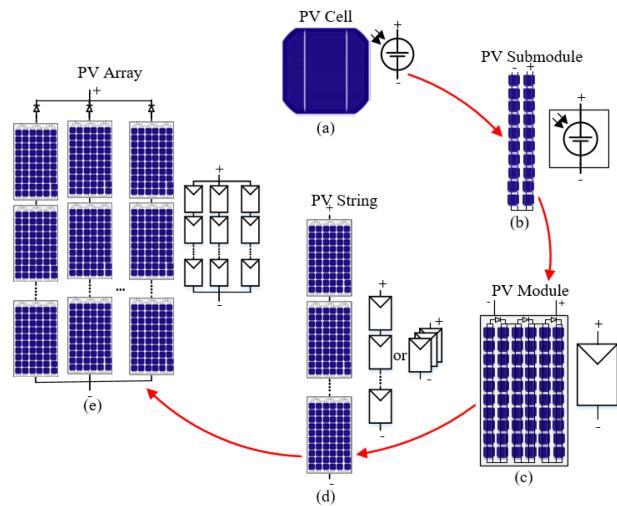
MIC	Module integrated converters.
MIMO	Multiinput–multioutput.
MISO	Multiinput–single-output.
MMCI	Modular multilevel cascade inverters.
MPP	Maximum power point.
MPPT	Maximum power point tracking.
MSBB	Multistage buck–boost.
NEC	National Electrical Code.
PDPP	Parallel DPP.
PV	Photovoltaic.
PV2B	PV to bus.
PV2PV	PV to PV.
PV2VB	PV to virtual bus.
PWM	Pulsewidth modulation.
SDFC	Single-delta full-bridge cell.
SDPP	Series DPP.
SLC	String level converters.
SMIC	Submodule integrated converters.
SPDPP	Series–Parallel DPP.
SSFC	Single-star full-bridge cell.
STATCOM	Static synchronous compensator.
TCT	Total Cross Tied.
THD	Total harmonic distortion.
VE	Voltage equalization.
ZSC	Zero-sequence current.
ZSV	Zero-sequence voltage.

## I. INTRODUCTION

The growing global population increases energy demand, prompting a shift to renewable sources, such as PV technology to reduce fossil fuel-related environmental impact [1], [2], [3], [4]. PV technology has broad applications, spanning from small-scale wearable devices to large utility-scale power systems [5], [6], [7]. The generated current and voltage from PV cells may not always meet the load's needs. Moreover, to reduce LCOE, it is crucial that PV cells work at their MPP, which varies with operating conditions. Therefore, PV systems must employ dc–dc and dc–ac converters to connect the PV generator to loads or the grid, ensuring efficient power delivery [8].

Fig. 1 illustrates the hierarchy of PV groups, starting from individual PV cells and progressing through PV submodules, modules, strings, and arrays [9], [10], [11]. PV cells, typically 20, 24, or 32 [12], are electrically interconnected to form PV submodules, which are then combined to create PV modules via lamination processes as we find them on the market. Often, multiple PV modules are connected in series to create PV strings and parallel connections of strings form PV arrays. Yet, to effectively connect these PV groups to the load or to the grid and operate at MPPs, power converters are essential. These converters can operate at various levels within the PV system, including the cell, submodule, module, string, and array levels, named CIC [13], [14], SMIC [15], [16], MIC [17], [18], SLC [19], [20], and ALC [21], [22], [23], respectively.

Early approaches to connecting PV arrays to the grid involved the use of ALCs, also known as central inverters,



**FIGURE 1.** Visual description of the various PV groups: (a) PV cell, (b) PV submodule, (c) PV module, (d) PV string, and (e) PV array.

which connect the entire PV system to the grid [21]. However, conventional PV systems with a single ALC track only the MPP of the entire PV array, leading to mismatch losses under conditions, such as partial shading, PV modules at different tilt angles, dust accumulation, or PV cell degradation [24]. For instance, partial shading can lead to significant power losses across the array due to the activation of bypass diodes in parallel to the shaded PV cells. This also results in local MPPs, complicating the operation of the MPPT algorithm. Moreover, parallel connection of PV strings can further exacerbate mismatch-related losses by forcing strings to operate away from their MPP [25]. To mitigate them, DMPPT can be employed, which aims to minimize mismatch-related losses by enhancing the granularity of power conversion [24], [26].

The literature introduces DMPPT architectures at various levels of granularity, including string, module, submodule, and cell levels [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. However, each level has limitations in addressing mismatches among PV groups with higher granularity. For instance, while SLCs can mitigate mismatches among PV strings, they are ineffective at the module level. On the other hand, CICs have low dc–ac conversion efficiency due to technological limitations in efficiently amplifying a PV cell's very low voltage. Moreover, having one converter per cell would escalate system complexity and cost. Generally, higher granularity reduces mismatch-related losses but increases power conversion losses. Thus, MIC and SMIC have got significant attention from researchers and industry.

Research on DMPPT has primarily focused on two main architectures: FPP [27], [28], [29], [30] and DPP [31], [32], [33]. FPP comprises ac-FPP and dc-FPP, with microinverters and MMCI belonging to the former, and parallel, series, and TCT architectures to the latter. DPP is further divided into SDPP, PDPP, and SPDPP architectures. Also, hybrid and hierarchical DMPPT solutions have been proposed [34],

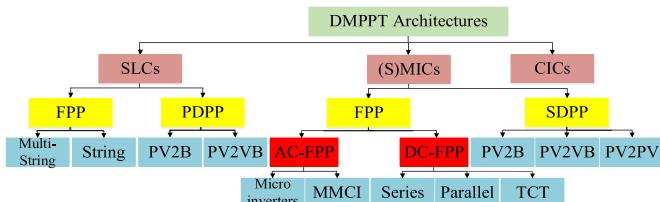


FIGURE 2. Taxonomy of DMPPT architectures.

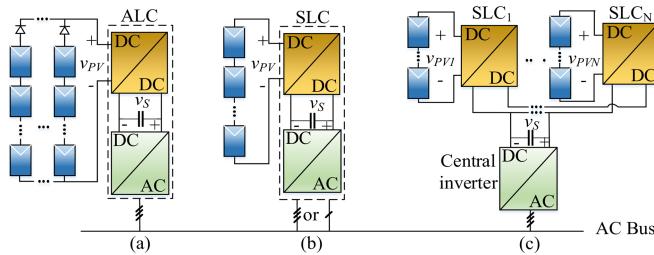


FIGURE 3. Array-level and string-level MPPT architectures. (a) MMPT at array level with a double-stage ALC. (b) DMPPT at string level with a double-stage SLC. (c) DMPPT at string level with SLCs and a central inverter.

leading to a plethora of new architectures. Various converter topologies and controllers have been developed for these architectures, each with their unique advantages and drawbacks. The selection of the most suitable architecture depends on the specific application's requirements, such as reliability, simplicity, efficiency, and cost-effectiveness, which vary across different PV applications. Navigating the extensive literature on DMPPT architectures, converter topologies, and controllers can be confusing due to the multitude of options available. Therefore, there is a critical need for a comprehensive survey that provides a broad overview of these techniques.

As shown in Fig. 2, this article aims to fulfill this need by presenting and categorizing recent DMPPT techniques along with their associated converters and controllers. It also discusses the advantages and challenges for each architecture and gaps in the literature.

The rest of this article is organized as follows. Section II gives an overview of MPPTs at the array and string levels, followed by an exploration of module-level and submodule-level DMPPT through FPP converters in Section III. Section IV delves into different DPP-based DMPPT architectures, while Section V discusses the integration of these architectures to create hybrid and hierarchical DMPPT PV systems. Finally, Section VI concludes this article and summarizes this work and discusses its findings.

## II. MPPT AT ARRAY LEVEL AND DMPPT AT STRING LEVEL

Fig. 3(a) shows a PV array connected to an ALC. These systems are known for their simplicity and low construction costs [21], making them attractive and widely used in open areas with uniform sunlight and minimal mismatches, as they

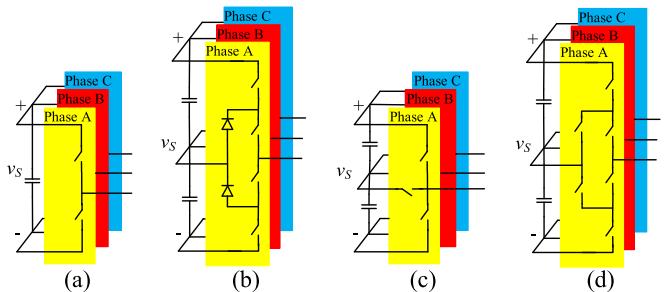
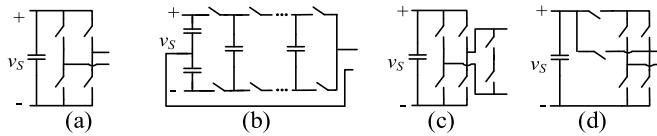


FIGURE 4. Three-phase dc-ac stage converter topologies for SLC or ALC. (a) 2L-VSI. (b) 3L-NPC. (c) T-type. (d) 3L-ANPC.

can achieve a low LCOE. ALCs often categorized into single-stage and double-stage topologies [23], [35]. In a double-stage topology, a dc–dc converter tracks the PV array's MPP, while a dc–ac converter keeps a fixed dc-link voltage ( $v_S$ ) and ensures that grid requirements, such as power quality, islanding operation detection, and grounding are met [22]. The high capacitance of the dc-link decouples the performance of dc–dc and dc–ac converters. Conversely, a single-stage ALC integrates both dc–dc and dc–ac functions into a single converter, thus performing all duties in a unified manner [36], [37].

In dc–ac converters, maintaining a sufficiently high dc-link voltage ( $v_S$ ) is crucial to avoid entering the overmodulation region of PWM. In single-stage architectures, the PV array's voltage ( $v_{PV}$ ) corresponds to the dc-link, potentially leading to overmodulation if the PV array's MPP voltage is too low. In contrast, double-stage topologies incorporate a dc–dc converter between the PV array and the dc–ac converter, broadening the MPPT range. In addition, the fixed dc-link voltage in double-stage architectures enables designers to optimize components for the dc–ac stage, enhancing efficiency [38], [39], [40]. However, processing power twice through both converters in double-stage architectures results in additional losses and complexity. Efforts to improve efficiency include proposals for partial power processing (PPP) converters in the dc–dc stage [38], [41]. Conversely, single-stage topologies offer reduced component count, cost, and size, albeit with a variable dc-link voltage [36], [37].

In array-level MPPT, mismatches within the PV array lead to reduction of energy yield. In addition, challenges, such as high-voltage dc cables, losses in string blocking diodes, and limited scalability, further diminish the effectiveness of array-level MPPT [42], [43], [44]. These obstacles can be addressed through two main string-level MPPT architectures. The first involves connecting each PV string directly to the grid via SLCs [see Fig. 3(b)] [45], also known as string inverters, which come in both single-stage and double-stage topologies [19], [46]. Alternatively, the PV strings can be connected to a common dc-link through SLCs before being connected to the grid via a central inverter, in so-called multistring architectures [see Fig. 3(c)] [4], [20], [47]. As shown in Fig. 4, various converter topologies, including 2L-VSI, 3L-ANPC, are commonly employed for the 3L-NPC, T-type, and three-level active neutral-three-phase dc–ac stage in both SLCs and



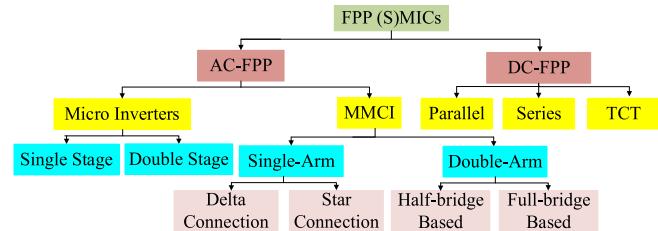
**FIGURE 5.** DC-AC stage of string inverter for single-phase topologies. (a) Full-bridge. (b) Multilevel. (c) HERIC. (d) H6.

ALCs, with associated power module packages commercially available for PV applications [48], [49]. While three-level power converters offer higher efficiency, the 2L-VSI topology has higher reliability due to its lower component count [4], [50]. Notably, also MMCIs, which will be discussed in Section III, can be used as SLCs or ALCs.

Infineon [51] has introduced power modules for four popular topologies used in the single-phase dc-ac stage of SLCs (see Fig. 5). The conventional full-bridge topology, while simple in structure, suffers from high power losses, THD, and leakage current, necessitating larger cooling systems and ac filters, which in turn increase inverter size and weight. To address these issues, other topologies, such as multilevel, highly efficient and reliable inverter Concept (HERIC), and H6 have been developed, offering reduced filter size, EMI, and improved power quality, along with higher efficiency and lower system cost, size, and weight. Further details can be found in relevant literature [51], [52].

### III. DMPPT AT MODULE AND SUBMODULE LEVELS WITH FPP MICS AND SMICS

The limitations of string-level DMPPT architectures in addressing mismatches among PV modules within the same string have led to the exploration of module-level and submodule-level DMPPT architectures as a solution. Literature highlights energy yield improvements achieved through the use of SMICs and MICs. For instance, SMA reports efficiency gains of approximately 1%–4% with microinverters compared to SLCs, with the actual gain depending on the degree of partial shading [53]. The report indicates that when considering factors, such as cost, expenses, and reliability, a microinverter typically offers a shorter payback time compared to a string inverter system for PV systems under 3 kW. However, it is important to note that this is not a universal conclusion; results can vary significantly based on different testing areas and considerations. For example, another study has shown significant energy yield enhancements with SMICs and MICs, reporting increase of up to 9.13% and 4.01%, respectively, compared to SLCs [24]. Thus, the energy yield enhancements reported in [24] are higher than those indicated in [53]. Therefore, although energy yield enhancement is normally expected under partial shading conditions when microinverters, SMICs or MICs are used, the effective energy yield gain and payback time should be preferably evaluated case-by-case by the designer, based on the actual operating conditions of the PV system under analysis.



**FIGURE 6.** Taxonomy of FPP (S)MCIs, branching out ac-FPP and dc-FPP solutions.

Besides, MICs offer better enhanced protection, monitoring, fault diagnosis capabilities, facilitating quicker repairs, and improving system availability [54], [55]. Furthermore, MICs and SMICs help prevent system interruptions in case of a single failure and are expected to see reduced manufacturing costs with mass production. MICs, in particular, simplify the MPPT algorithm by reducing the number of local MPPs, making them suitable for complex environments, such as building-integrated PV systems. Consequently, many industrial companies have introduced and continue to innovate these technologies in the market [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68]. The most straightforward way to implement (S)MCIs is through FPP converters. A general classification of FPP solutions is presented in Fig. 6. They can be subdivided into two main categories: 1) ac-FPP and 2) dc-FPP.

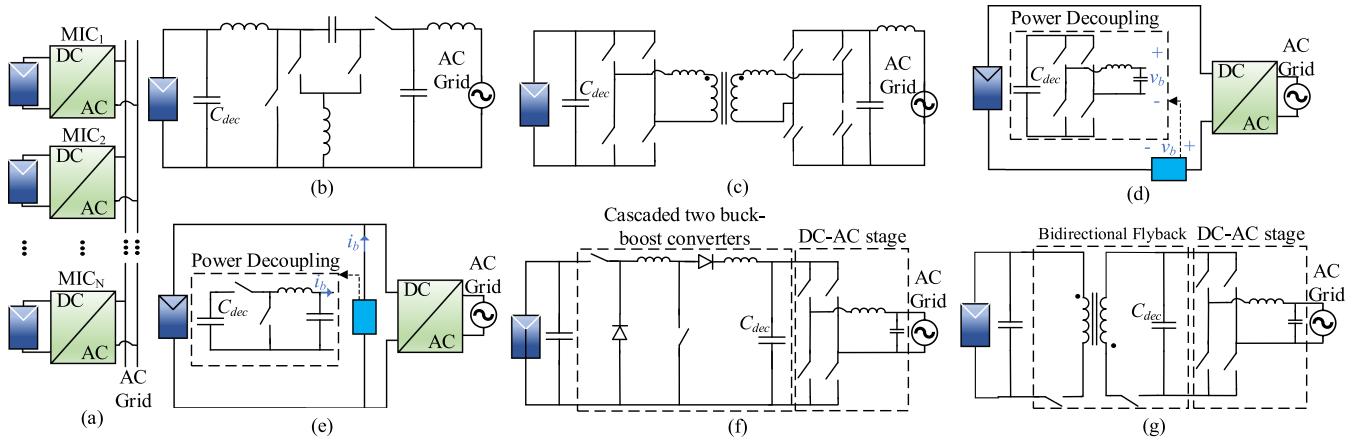
#### A. AC-FULL POWER PROCESSING (FPP)

AC-FPPs perform the conversion of dc input voltage to ac, allowing direct connection to the ac grid without requiring a central converter. AC-FPPs are categorized into two groups: 1) microinverters and 2) MMCIs.

##### 1) MICROINVERTERS

Microinverters represent one of the earliest approaches to achieving DMPPT at the module level, as depicted in Fig. 7. They offer several unique advantages, including easy attachment to the back of PV modules, independent tracking of the MPP of each module without cross-coupling effects, and resilience to failure or shading of individual modules or microinverters, ensuring continued system operation with minimal reduction in total power production [27]. Microinverters also have plug-and-play functionality, facilitating straightforward installation and maintenance of PV systems. These features enhance system flexibility, modularity, scalability, and reduce installation costs [27], [69], [70]. Such benefits have led companies [56], [57], [58], [59], [60], [61], [62], [63], [64] to industrialize and researchers stage [71], [72], [73], [74], [75], [76], [77], [78], [79] to explore and propose new microinverter topologies for this architecture.

Despite their promising advantages, microinverters face challenges, such as the need for high voltage gain, resulting in increased complexity and conversion losses. Moreover, in single-phase microinverters, grid power ripple flows in the



**FIGURE 7.** Microinverters: (a) system's configuration and (b)–(h) topologies. (a) Every module is connected to the ac grid through its own MIC. (b) Nonisolated single-stage [71], (c) isolated single-stage [73], (d) isolated single-stage with series power decoupling, (e) isolated single-stage with parallel power decoupling [74], [75], (f) nonisolated double-stage [77], and (g) isolated double-stage [56].

dc-link, causing a double line frequency ripple at the dc-link voltage [80]. This disturbance in the ripple deteriorates MPPT performance and efficiency. To mitigate this issue, the use of electrolytic high-capacitance capacitors for power decoupling is essential, but these capacitors shorten the lifetime of microinverters and reduce their power density [27], [69].

Various converter topologies have been proposed for microinverters, which can be categorized into four classes: 1) nonisolated single stage [see Fig. 7(b)] [71], [72], 2) isolated single stage [see Fig. 7(c)] [73], [74], [75], 3) nonisolated double stage [see Fig. 7(f)] [76], [77], and 4) isolated double-stage topologies [see Fig. 7(g)] [78], [79]. In single-stage topologies, one stage fulfills various duties of microinverters, including MPPT, voltage amplification, current grid control, dc-ac conversion, and compliance with grid requirements. The nonisolated single-stage topology, requiring fewer components and no transformers, offers a low-cost, low-complexity, and highly efficient solution [71], [72]. However, it needs decoupling capacitors on the PV modules' side, where the nominal voltage is relatively low. Thus, to enhance MPPT efficiency, voltage ripple should be limited to a small amplitude, necessitating a large decoupling capacitance in nonisolated single-stage topologies, thereby shortening their lifetime.

The literature proposes decoupling circuits single-stage microinverters, which usually come in two types [81]: series power decoupling [see Fig. 7(d)] or parallel power decoupling [see Fig. 7(e)] [74], [75], with a PV module. These auxiliary circuits, positioned between the PV module and inverter, reduce decoupling capacitance while introducing extra components and associated power losses. They enable the replacement of high-capacitance electrolytic capacitors with high-reliability film capacitors, thereby enhancing the lifetime of microinverters [70].

In double-stage microinverters, two cascaded converters are utilized. The first stage, a dc-dc converter connected to the PV modules, handles MPPT and voltage amplification, while the

**TABLE 1.** Comparison of Microinverters Topologies

Topologies	Quality	Efficiency	Power density	Lifetime	Cost	THD
Non-isolated single-stage [71], [72]	High	High	Short	Low	Mod	
Isolated single-stage [73]	High	Mod*	Short	Mod	Good	
Isolated single-stage with decoupling circuit [74], [75]	Mod	Mod	Long	High	Good	
Non-isolated double-stage	High	High	Long	High	Mod	
Isolated double-stage [76], [77]	Mod	Mod	Long	High	Good	
Microinverter with low-frequency transformer [78], [79]	Low	Low	Var**	High	Good	

\* Moderate.

\*\* Variable: it depends on the location of the decoupling capacitor.

second stage, a dc-ac converter, manages current grid control, dc-ac conversion, and grid requirements. In this architecture, decoupling capacitors are typically placed at the dc-link, benefiting from its high voltage to reduce the required capacitance. Utilizing a transformer is a straightforward solution in double-stage microinverters to eliminate leakage current and meet the NEC standard's dual-grounding requirement [82]. Moreover, isolated microinverter topologies exhibit lower THD in the output current compared to nonisolated ones [27]. Isolation with line-frequency and HFT are the two basic families of isolated microinverters, while HFTs offer greater efficiency, compactness, and cost-effectiveness compared to line.

Frequency transformer still introduces losses, costs, and space constraints. Thus, research also explores nonisolated double-stage topologies to reach high efficiency, compactness, and low cost. A comparison of microinverter topologies is summarized in Table 1, and further details can be found in relevant literature [27], [69], [70], [83], [84].

## 2) MODULAR MULTILEVEL CASCADE INVERTERS (MMCI)

In the 1990s, MMCIIs debuted for high-power motor drives, featuring multiple series-connected dc-ac inverters known as inverter cells (see Fig. 8). These systems have advantages, such as reduced EMI, THD, acoustic noise, and switching

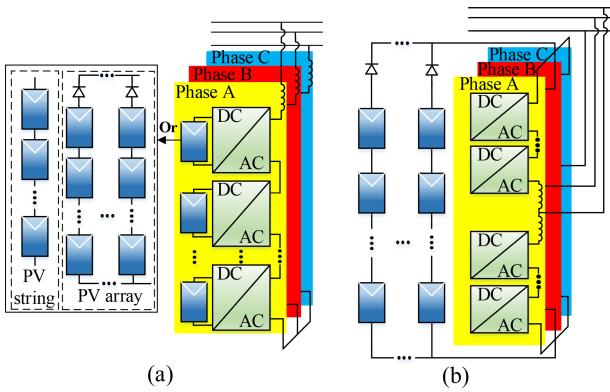


FIGURE 8. MMCI in PV applications. (a) MMCI inverter cells as MICs, SLCs, and ALCs. (b) MMCI as an ALC.

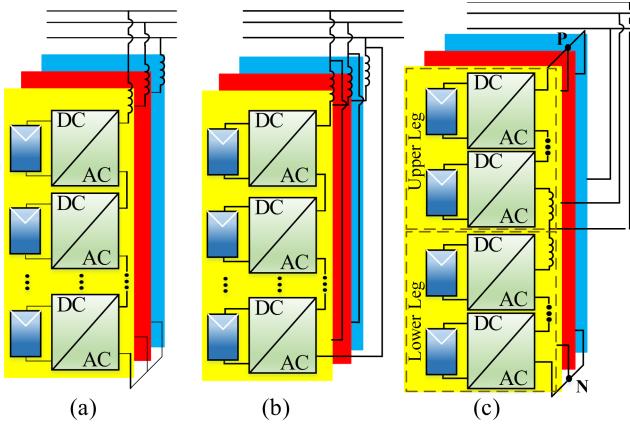


FIGURE 9. MMCI architectures. (a) SSFC. (b) SDFC. (c) DSFC and DSHC.

stress, alongside compact ac filter size, high power density, modularity, and scalability. Many companies, including ABB, TMEIC, GE, and Siemens, swiftly integrated MMCIIs into various applications, such as STATCOM, active power filters, and electric drives.

A key drawback of MMCIIs lies in their requirement for isolated multiple dc voltage sources, necessitating complex multiwinding phase-shifted line-frequency transformers to distribute electric power among the floating inverter cells [85]. Despite this limitation, MMCIIs prove beneficial for PV systems, enabling DMPPT due to the availability of multiple independent and isolated dc sources, such as PV modules, strings, or arrays. In addition, as shown in Fig. 8(b), MMCIIs can serve as ALCs with a common bus, offering potential cost, weight, and volume savings by eliminating conventional medium voltage transformers [86], [87]. Thus, MMCIIs present a promising solution for both DMPPT and ALC architectures. MMCIIs architectures are classified based on the number of leg inductors per phase. In terms of leg inductors, architectures include single-leg [see Fig. 9(a)] [88], [89], [90], [91] and double-leg [see Fig. 9(b)] [92], [93], [94]. The appropriate inverter cell topologies for MMCIIs are further categorized based on the following:

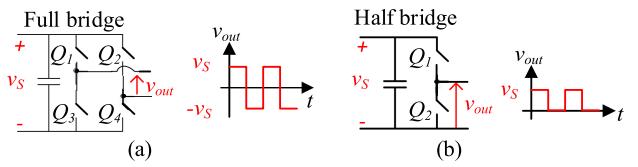


FIGURE 10. MMCI cells. (a) Full-bridge. (b) Half-bridge dc-ac converter topologies and their output voltage waveforms.

1) The number of power processing stages and 2) the use of HFTs for isolation. In medium- and high-voltage PV systems, the utilization of [94] HFT [94], [101], [102] becomes indispensable due to the maximum system voltage specified in PV module datasheets. This voltage parameter is determined by the sum of the maximum open-circuit voltages of all PV modules within a string, typically ranging from 600 to 1500 V. However, in architectures like MMCI with single-stage [89], [90] or nonisolated inverter cells [88], [103], PV modules are interconnected in series through certain switching sequences. Consequently, if the total string voltage exceeds the maximum system voltage threshold, which is common in medium- and high-voltage PV systems, not only does the PV system fail to meet standards, but it also risks damaging the PV modules [101], [102].

Focusing specifically on the dc-ac processing stage, as illustrated in Fig. 10, two main topologies are commonly used: half-bridge and full-bridge inverters. Half-bridge cells generate only zero and positive voltages, leading to a dc component in single-leg architectures. In contrast, double-leg architectures, which utilize two legs per phase, mitigate dc component and can accommodate both full-bridge and half-bridge topologies [92], [98]. Another difference between single-leg and double-leg architectures is the presence of a common dc link, connected to the phases' upper (P) and lower (N) sides [see Fig. 9(c)] in double-leg architectures, enabling their application as ALC without additional components, as shown in Fig. 8(b) [99]. Given that three single-leg architectures can be connected in either star or delta connection, MMCIIs architectures are classified into four groups [104]: 1) SSFC [87], [95], 2) SDFC [96], [97], 3) DSFC [98], and 4) DSHC [99], [100]. Table 2 compares three-phase MMCIIs based on the assumption that components with same voltage and current ratings are used in the four architectures. MMCIIs face various challenges caused by mismatches, including power imbalances among inverter cells or phases, called inter-bridge and interphase power imbalances [86], [105]. In addition, in double-star architectures, interleg power imbalances arise [28]. Addressing interphase power imbalances necessitates the injection of additional ZSV or ZSC into each phase, with their application varying depending on the architecture. However, the severity of power imbalances dictates the injected ZSV/ZSC and subsequently impacts the required voltage or current rating of the inverter cell. The SSFC architecture exhibits the narrowest range in addressing power imbalances [28], [96]. Eventually, MMCIIs face the challenge of necessitating high capacitance when utilized for DMPPT, as the structure must filter the

**TABLE 2.** Comparison Among the Four MMCI Architectures, Under the Assumption That Components Possess Identical Blocking Voltage and Power Ratings

Feature	Number of inverter cells	Number of switches	Circulating current	Balancing control	Balancing limitation	Balancing capability
Config.						
SSFC [87], [95]	$N$	$4N$	No	ZSV	Maximum available DC-link voltage	Average
SDFC [96], [97]	$\sqrt{3}N$	$4\sqrt{3}N$	Yes	ZSC	Maximum inverter cell current	Good
DSFC [98]	$2N$	$4N$	Yes	ZSV or Circulating current injection	Maximum available DC-link voltage or maximum inverter cell current	Good
DSHC [99], [100]	$N$	$4N$	Yes	ZSV or Circulating current injection	Maximum available DC-link voltage or maximum inverter cell current	Good

\*All architectures have the same grid voltage and inverter cell voltage

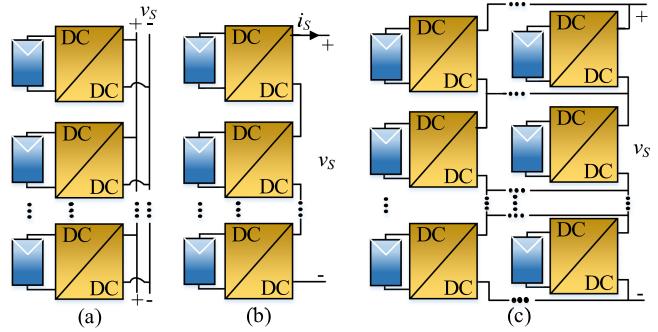
**TABLE 3.** Comparison of AC-FPP/DC-FPP Architectures. Microinverters and Parallel DC-FPP, as Well as MMCIs and Series DC-FPP, Share Similarities, so They are Compared Together in a Single Table

Architecture	Microinverters/ Parallel DC-FPP [71], [72], [73], [76], [78], [79], [106], [107]	MMCIs/ Series DC-FPP [95], [96], [97], [108], [109]
Phase Number	Single phase	Single/or Three phase
EMI	High	Low
AC filter size	Large	Small
Switching frequency*	High	Low
Power processing*	Full	Full
Applicable in medium-voltage PV system*	No	Yes
High gain converters*	Required	Not required
Improving efficiency of switching converters*	Challenging	Easy
Cross-Coupling Effects*	No	Yes
Availability against failure of several modules *	Excellent	Vulnerable
Flexibility	High	Low
Components voltage rating *	High	Low

\*These features can be extended to compare parallel with series DC-FPP.

double-line frequency for each floating inverter cell, regardless of if it is three-phase or single-phase. Ultimately, MMCIs are rarely employed in actual installations. Their complexity is only justified when the PV plant is directly connected to a medium-voltage grid without a transformer. However, as previously discussed, MMCI presents significant isolation coordination challenges. Consequently, despite being a topic of research, the practical application of MMCIs in PV systems remains limited.

In this section, we have introduced two approaches for ac-FPP: microinverters and MMCIs, each with its distinct characteristics outlined in Table 3. MMCIs offer advantages such as generating multilevel output voltages enabling low switching frequency, small ac filter size, and low EMI. However, their series connection of inverter cells can lead to increased conduction loss and issues with power imbalances during mismatch conditions. On the other hand, microinverters provide benefits, such as resilience to single failures or mismatch conditions, ensuring continuous operation with only a slight reduction in power production. In contrast, MMCIs require careful attention to fault detection, redundancy,

**FIGURE 11.** DC-FPP architectures. (a) Parallel. (b) Series. (c) TCT.

and their impact on system performance to ensure that a failure of a single device does not compromise the overall system [110], [111]. In addition, while the installation of microinverters is typically plug-and-play, MMCIs demand more extensive considerations such as electrical integration, control, communication, and compliance with standards like NEC. As a result, microinverters provide greater modularity and flexibility compared to MMCIs. Eventually, while MMCIs consist of series-connected inverter cells that necessitate low-voltage components, microinverters require high-voltage components. For example, these factors must be taken into account when selecting the most suitable approach for a given PV system.

## B. DC-FULL POWER PROCESSING (FPP)

In dc-FPP architectures, the requirement to comply with distributed ac grid connection standards, such as filtering, protection, control, and double-line frequency ripple, is effectively addressed by means of a central dc-ac converter. However, such a central dc-ac converter, which is mandatory in grid-connected dc-FPP architectures, could potentially pose a bottleneck for the PV installation due to the single-failure-point problem [112], [113]. Generally, dc-FPP architectures can be categorized as follows: parallel, series, and TCT architectures (see Fig. 11).

### 1) PARALLEL DC-FPP

In a parallel dc-FPP architecture, illustrated in Fig. 11(a), MICs, also known as parallel optimizers, are connected to PV

modules and share a common dc bus. They have traits similar to microinverters, including immunity to the cross-coupling effect, flexibility, modularity, and scalability [44], [107]. In addition, with only a single stage for dc–dc conversion, they require fewer components. EIQ Energy and other companies have industrialized this solution [65]. However, challenges include the need for high step-up dc–dc conversion and high efficiency. To address these challenges, literature has reported on many high step-up converters, which can be used in Parallel dc-FPP architectures [114].

## 2) SERIES DC-FPP

In series dc-FPP architecture, depicted in Fig. 11(b). MICs, also known as series optimizers, are in series to create a dc bus. This architecture offers several benefits, including reduced voltage gain requirements for MICs due to the stack structure. This results in more efficient, smaller, less expensive, and simpler MICs than that of parallel architectures [29]. Notably, Series dc-FPP has been industrialized by several companies, such as SolarEdge [67], Tigo Energy [66], Taylor [115], and Xandex [68]. Converters employed in series dc-FPPs can be classified into three categories: 1) buck-based [108], 2) boost-based [44], [109], and 3) buck-boost-based [18], [116]. These categories differ primarily in their response to partial shading and their ability to maintain matching between the current of shaded PV modules and the string current ( $i_S$ ).

During mismatch conditions, buck-based converters regulate the voltages of shaded PV modules downward, increasing their output currents to match those of unshaded PV modules. This process lowers the dc link voltage ( $v_S$ ) compared to uniform operating conditions, necessitating a minimum number of PV modules per string to maintain a specified minimum dc link voltage during mismatch. In addition, the string current must consistently exceed the currents of all PV modules to ensure that those with MPP currents higher than the string current operate at their MPP. The maximum number of PV modules with associated buck converters per string, for a given dc-bus voltage, is determined by the converters' maximum output current rating.

Boost-based converters operate by increasing the voltage of unshaded PV modules, reducing their output currents to match those of shaded modules. This results in an increase in converter output voltage. The maximum number of PV modules per string is determined by the converters' maximum output voltage for a given string voltage. However, to ensure maximum power extraction, the string current must always be lower than the currents of individual PV modules. Failure to meet this criterion may prevent PV modules with lower MPP currents from operating at their MPP.

In buck-based and boost-based architectures, the PV string voltage varies to achieve the MPP, so even in dc grids, additional stage is necessary to maintain a constant output voltage equal to the dc grid voltage. Buck-boost-based converters offer a solution to this issue. Without limitations on the PV

string current range, the total voltage of series-connected converters can remain constant, allowing for a wider range of PV modules per string. The upper and lower limits for the number of PV modules per string are determined by the maximum output current and voltage ratings of the MICs [18], [117]. These advantages come with typical disadvantages associated with buck-boost converters: lower converter efficiency, increased complexity, more components, and susceptibility to load variation [117].

The features of parallel and series dc-FPPs share similarities with microinverters and MMCI, respectively. Hence, the star-marked features represented in Table 3 can be extended to compare parallel and series dc-FPP architectures.

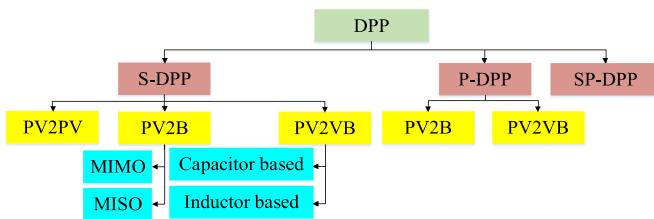
## 3) TCT DC-FPP

Series and parallel dc-FPP architectures have their own advantages and challenges. On one hand, series dc-FPPs are susceptible to cross-coupling effects, potentially leading to PV modules operating away from their MPP and reducing system output power [30], [44]. On the other hand, parallel dc-FPPs are immune to cross-coupling but require high voltage step-up ratios for MICs, leading to higher voltage stress on switches and reduced conversion efficiency. To address these challenges, the recently proposed TCT dc-FPP architecture [see Fig. 11(c)] [30] offers a potential solution claimed reducing cross-coupling compared to series dc-FPP. However, the TCT architecture introduces complexities due to its combination of series and parallel connections among MICs, making scalability and implementation challenging.

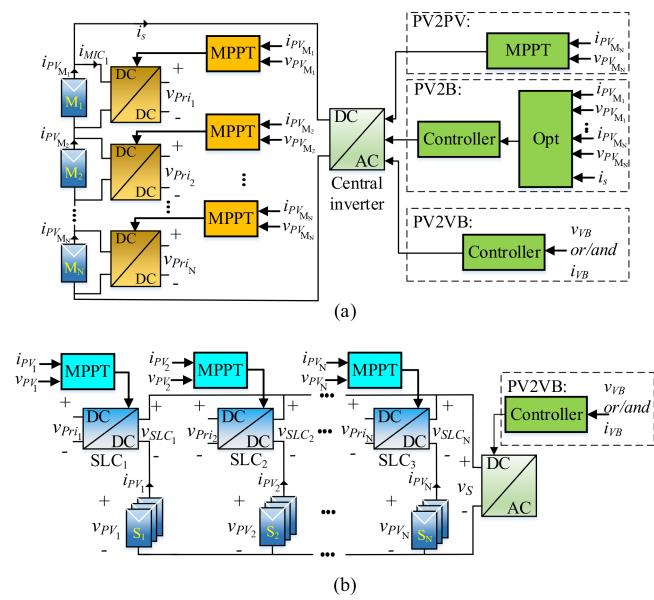
Both nonisolated and isolated topologies can be applied for dc-FPP architectures. Nonisolated topologies include buck, boost, buck-boost, zeta, SEPIC, Ćuk, and derivatives. Isolated topologies mainly consist of forward, push-pull, flyback, half-bridge, full-bridge, and resonant converters [29], [112]. Notably, it is possible to use partial power converters in the architectures shown in Fig. 11, enhancing overall system efficiency and reducing system costs. In this case, they are classified as PPP architectures [41], [112].

## IV. SDPP (S)MICS AND PDPP SLCS

In FPP architectures, while mismatch-related losses among PV modules or submodules are eliminated, the MICs handle all the power generated by the PV modules even under uniform conditions. This leads to increased power conversion losses, size, and cost of MICs. To address these issues, the concept of DPP, initially proposed for electric vehicle battery charge equalization, has been extended for PV applications. DPPs are categorized into SDPP, PDPP, and SPDPP, as depicted in Fig. 12. Further details on these approaches are provided in the following sections, primarily discussing module-level MICs and occasionally SMICs depending on the paper's focus. However, the described approaches, architectures, topologies, and methods, along with their advantages, drawbacks, and challenges, are equally relevant at both module and submodule levels.



**FIGURE 12.** Taxonomy of DPP architectures, branching out SDPP, PDPP, and SPDPP solutions.



**FIGURE 13.** PV systems using DPP architectures. (a) SDPP. (b) PDPP.

#### A. SDPP

In SDPP architectures, depicted in Fig. 13(a), MICs specifically manage the differential current between individual PV modules and the overall PV string current ( $i_S$ ). Under uniform conditions where there is no mismatch among PV modules, MICs remain inactive, reducing their operational load and enhancing their reliability and lifespan. During mismatch conditions, MICs only process a fraction of the power, while the majority of the power generated by the PV modules flows directly to the output without local processing. This offers two key advantages: first, it reduces MICs' operational time and increases system efficiency, even if the efficiency of SDPP MICs is lower than FPP MICs. Second, it alleviates stress on components, resulting in improved reliability and lifespan. Although the concept is new, due to their advantages, SDPP has already been patented [118], [119], [120] and industrialized by the company Optivolt [121].

In SDPP architectures, the need to increase the power rating of MICs to address heightened mismatch conditions can lead to an increase in both the size and cost of the MICs. However, severe mismatch conditions are rare, rendering it economically unjustifiable to increase the power rating of MICs. When MICs are assigned an infinite power rating, the  $I-V$  curve at

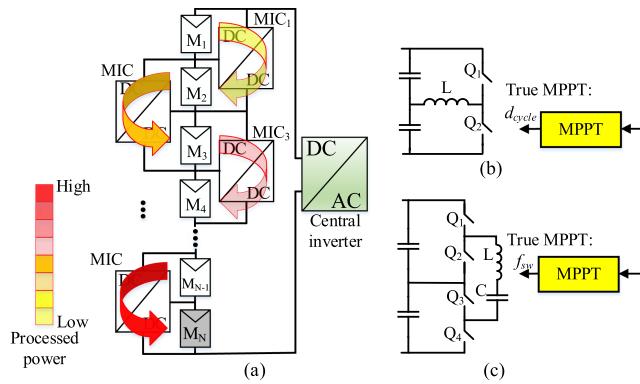
**TABLE 4.** Comparison of VE and True MPPT

Approaches	VE [16], [125]	True MPPT [123], [124]	
<b>Features</b>			
<b>Control</b>	Open loop	Closed loop	Closed loop
<b>Dynamic Performance</b>	Quick	Medium	Slow
<b>Complexity</b>	Low	Medium	High
<b>Impact on Reliability</b>	No	Low	High
<b>Cost</b>	Low	Medium	High
<b>Type of Loss</b>	Mismatch losses	Mismatch & sensors losses	Sensors losses
<b>Steady-state perturbation oscillation</b>	No	No	Yes
<b>Ability to limit processed power</b>	No	Yes	Yes

the central inverter's input simplifies, featuring only a single peak, which streamlines its MPPT algorithm. Conversely, when the converter rating is restricted to a fraction of PV modules' MPP, MICs' operation is confined to nominal power during severe mismatch conditions. This limitation prompts the appearance of local peaks in the  $I-V$  curve at the central inverter, necessitating MPPT algorithms capable of tracking the global peak and introducing mismatch losses. Thus, research endeavors to determine the optimal MICs ratings for the design of SDPP PV systems [24], [122].

The ideal operation for SDPP MICs aims at ensuring each PV module operates at its true MPP. Achieving true MPP tracking often involves additional local sensors or complex communication systems, both of which come with drawbacks, such as increased power losses, higher costs, reduced reliability, and added complexity [123], [124]. An alternative approach, known as VE, forces all PV modules to operate at the same voltage level, minimizing mismatch losses. While VE methods still encounter some mismatch losses, they benefit from the low sensitivity of PV modules' MPP voltage to changes in the environmental conditions, keeping modules near their MPP. Indeed, as demonstrated in [24], VE at submodule level results in additional energy yield losses of less than 2% compared to True MPPT, even in extreme worst-case scenarios. For instance, even with a significant temperature difference of 25 °C between PV submodules, power losses lower than 1.7% were achieved experimentally. Furthermore, the effects of reduced irradiance and lower temperature tend to offset each other, leading to smaller power losses in PV systems. VE strategies can be either open-loop [125] or closed-loop [16]. Open-loop control, although simple and cost-effective, lacks the ability to limit MIC power during extreme mismatch conditions and is susceptible to inaccuracies and external disturbances. Closed-loop control offers the advantages of precise regulation but requires additional sensors or communication capabilities. The choice between VE and true MPP approaches depends on factors, such as system complexity, cost, and reliability. Table 4 provides a comparison of these two methods.

All DPP MICs are linked directly to PV modules. The SDPP architecture varies based on where each MIC's primary



**FIGURE 14.** PV2PV SDPP architecture with  $N$  PV modules.  
(a) Accumulation effect on MICs power processing (in this example, the bottommost PV module is shaded whereas the others are unshaded).  
(b) Switched-inductor MIC. (c) Resonant switched-capacitor MIC.

is connected, resulting in three subcategories: 1) PV2PV, 2) PV2B, and 3) PV2VB. These architectures will be thoroughly examined in the subsequent sub-subsections.

### 1) PV TO PV (PV2PV)

In the PV2PV architecture [see Fig. 14(a)], each SDPP MIC's primary is connected to a PV module, while its secondary connects to the subsequent PV module in the string. It ensures that each MIC regulates the operating point of only one PV module, focusing solely on achieving MPP operation for that PV module. One advantage of this architecture is that the voltage rating of the MIC components is determined solely by the PV module's voltage. In addition, nonisolated MICs can be utilized, leading to improved efficiency and reduced cost and size. However, despite these benefits, this architecture faces a significant drawback known as the accumulation effect [see Fig. 14(a)]. This effect arises from the fact that power transfer occurs exclusively between adjacent PV modules, causing the MICs to process the same power multiple times as it is transferred from unshaded to shaded modules. This effect is exacerbated in longer PV strings, resulting in increased power ratings, losses, and costly MICs [122], [126].

Controlling a PV string with  $N$  PV modules requires defining  $N$  objectives, necessitating at least  $N$  actuators. In PV2PV, with  $N-1$  MICs serving as actuators, an additional actuator is required. The central converter can serve as the  $N$ th actuator, tracking the MPP of the  $N$ th PV module. In the PV2PV SDPP architecture, two main MIC topologies are commonly utilized: switched-inductor [123], [124], [127], [128], [129] and resonant switched-capacitor [130], [131], [132]. The switched-inductor architecture, shown in Fig. 14(b), comprises two switches, one inductor, and two capacitors. In PV2PV SDPP architectures with switched-inductor topologies, when employing the VE technique for MPPT, the duty cycle of the switches must be set to 0.5, achievable without additional control mechanisms. For true MPP, a closed-loop controller adjusts the duty cycle based on the PV module voltages.

Given the widespread adoption of switched-inductor topologies in PV2PV architectures, various approaches have been proposed to efficiently perform distributed MPPT. In the centralized approach presented in [124], no local sensors are required, but communication with the central control unit is needed. In this method,  $2^N$  duty ratio perturbations are required during each tracking step to locate the MPP. This becomes less practical for long PV strings due to the high number of perturbations per step, potentially leading to slower MPP tracking. Moreover, failures of the control unit or communication links could lead to malfunctions at best and complete system faults at worst. This limitation impacts the reliability of such an approach.

In [123], a distributed algorithm that relies solely on neighbor-to-neighbor communication between adjacent MICs to achieve true MPPT at the submodule level is proposed. This approach eliminates the need for a central control unit and local current sensors, enhancing reliability by removing the single point of failure. Although only  $N$  duty ratio perturbations are needed per DPP tracking step to locate the MPP, the tracking process still becomes slower with longer PV strings. Schaeff and Stauth [129] introduced a multilevel DMPPT control for DPP-based systems, which is claimed to converge in less than 20 perturbations regardless of PV string length, improving algorithm speed to locate the MPP. Although it reduces communication requirements compared to [124], synchronization between power converters is necessary, and local current sensing is still needed for the first MIC. Another strategy suggested in [128] is a flexible double-stage time-sharing MPPT control, ideal for SMICs, where the MIC acts as the central controller. This approach eliminates the need for communication but requires central current and voltage sensors, along with additional sensors in two out of three PV submodules, leading to extra costs and losses. In addition, Al-Smadi and Mahmoud [133] presented a solution achieving fast transient response and accurate steady-state MPP without requiring communication between converters or distributed current sensing. However, it relies on optical cameras per PV module to estimate irradiances.

Table 5 provides a comparison of these true MPP approaches with VE.

Resonant switched-capacitor converters represent another topology for PV2PV SDPP MICs. This topology, depicted in Fig. 14(c), comprises four switches, three capacitors, and one inductor. Offering zero voltage switching, it has higher efficiency compared to the switch-inductor converter.

In addition, its circuit implementation eliminates the need for large magnetic components, resulting in a compact vertical footprint. However, the increased switch count in this converter adds complexity, as each switch needs a gate driver consisting of a driver IC, auxiliary power source, and ancillary components [54], [130], [131], [132], [134].

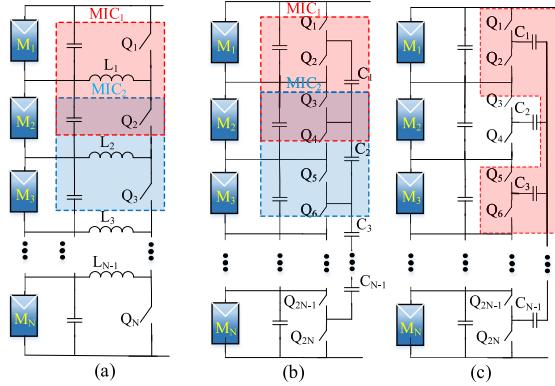
Both VE and true MPP control strategies have been applied to resonant switched-capacitor converters. VE is achieved through a straightforward open-loop control involving two switching states. During the first state,  $Q_1$  and  $Q_3$  are activated

**TABLE 5.** Comparison of DPP Control Approaches for the Bidirectional Switched-Inductor Topology

Features	Approaches	VE	Centralized [124]	Neighbour to Neighbour [123]	Time-sharing [128]	Multilevel MPPT [129]	Image-Based [133]
<b>Tracking</b>	Near MPP	true MPP	true MPP	true MPP	true MPP	true MPP	true MPP
<b>Distributed algorithm</b>	No	No	Yes	Yes	Yes	Yes	Yes
<b>Local current/voltage sensors</b>	No/No	No/No	No/Yes	Yes/Yes	No**/Yes	No/Yes	No/Yes
<b>Central current/voltage sensors</b>	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	No/No	No/No
<b>Requiring communication</b>	No	Yes	Yes	No	Yes	No	No
<b>Algorithm tracking speed</b>	Fastest	Slow	Slow	Slow	Medium	Fast	Fast
<b>Steady-State Oscillation</b>	No	Yes	Yes	Yes	Yes	Yes	No

\* Some of the (S)MICs require local sensing

\*\*Only the first MIC requires current sensing

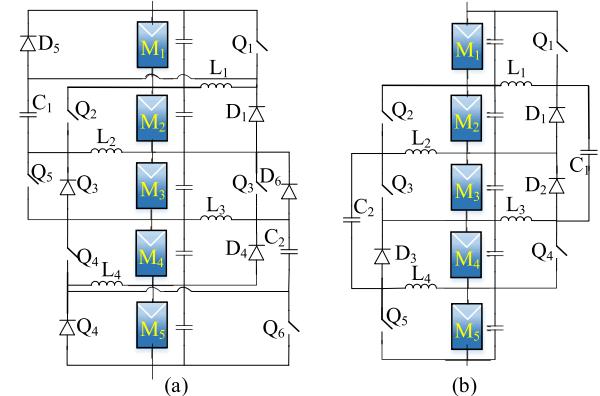


**FIGURE 15.** PV2PV SDPP architecture with (a) MSBB, (b) LSCC, and (c) DSCC Converters as MICs.

while the other two switches remain OFF, and vice versa for the second state [130], [132]. This allows for energy transfer between PV modules during the charge and discharge states of the MICs' operation period. To implement true MPPT, two additional steps are necessary: introducing a third switching phase and controlling the switching frequency. In the third switching phase,  $Q_2$  and  $Q_3$  are activated while  $Q_1$  and  $Q_4$  are deactivated, and the differential current or power is regulated by adjusting the switching frequency. The sequence of switch activations dictates the direction of power flow, enabling bidirectional step-up/down operation [130], [131].

Various other topologies have been introduced to optimize the number of switches shared among adjacent MICs, such as MSBB [135], [136], [137], LSCC [138], [139], [140], and DSCC [141], [142], as depicted in Fig. 15. MSBB employs  $N-1$  bidirectional buck-boost choppers with  $N$  switches and  $N-1$  inductors [see Fig. 15(a)]. This topology, with one switch per MIC, enables true MPPT. However, a single switch failure could lead to system shutdown, compromising system availability. In addition, switches require a high-voltage rating tied to the dc bus voltage, and their duty cycle increases with longer PV strings, as switches are turned OFF one-by-one sequentially within a single switching cycle [135], [136], [137].

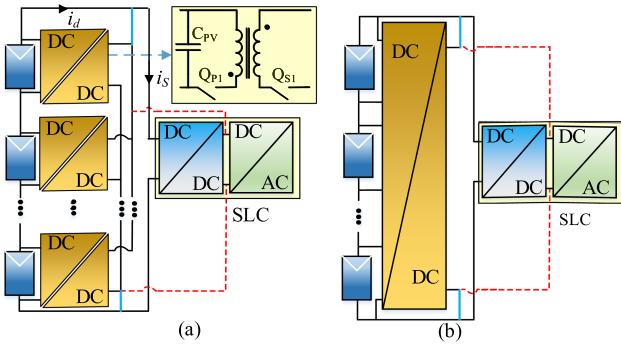
In both LSCC [138], [139], [140] and DSCC [141], [142] topologies [depicted in Fig. 15(b) and (c)], a set of  $2N$  switches and  $N-1$  capacitors in addition to the capacitors in parallel with PV modules are employed. These topologies operate with a fixed 50% duty cycle in a complementary manner.



**FIGURE 16.** Combination of switched-inductor and switched-capacitor MICs proposed by (a) Uno et al. [143] and (b) Tahmasbi-Fard et al. [144].

In LSCC, the voltage ratings of switches and capacitors match that of a single PV module, allowing for easy extension of the ladder structure by adding new rungs. This modularity aids the rapid extension of the PV string by connecting additional PV modules. However, similar to other PV2PV SDPPs, LSCC suffers from accumulation effects. To tackle this issue, DSCC is introduced, where all capacitors are connected to a common node, enabling direct power transfer between any two PV modules [141], [142].

A combination of switched-inductor and switched-capacitor MICs, as depicted in Fig. 16, is proposed by Tahmasbi-Fard et al. [143] and Shams et al. [144]. In [143], switched-inductor MICs are employed for VE in a downward path, while switched-capacitor converters facilitate power transfer in an upward path. In [144], the proposed architecture combines switched-inductor and switched-capacitor MICs to form a VE. The operating principle of the VE can be categorized into two parts: 1) charging and discharging of the inductor, similar to the switched-inductor MICs, and 2) charging and discharging of the capacitor, similar to the switched-capacitor MICs. While Shams et al. [144] reported high efficiency and reduction in the switches count, the solution lacks modularity.



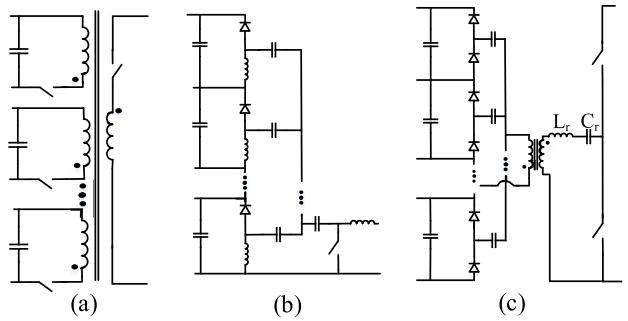
**FIGURE 17.** PV2B SDPP. (a) MIMO with an exemplary flyback MIC topology. (b) MISO architectures. SDPP MICs' primary can be connected either to the input (blue continuous lines) or to the output (dashed red lines) of the dc-dc stage of the SLC.

## 2) PV TO BUS (PV2B)

In the PV2B SDPP architecture, illustrated in Fig. 17, SDPP MIC's primaries are connected to a dc bus, which can be either the input or output of the central converter dc-dc stage. This architecture allows for N MICs and an SLC to act as actuators for a string of N PV modules, offering a degree of freedom in architecture control to enable reducing converter size and cost. To utilize this degree of freedom effectively, the architecture must feature bidirectional MICs. This allows some MICs to transfer power from PV to the bus, while others transfer power in the opposite direction at the optimal point [16], [17], [26], [145], [146], [147].

Regarding the connection of MICs primaries, two approaches are common: direct connection to the input of the SLC's dc-dc stage [148], [149], [150], [151], [152], [153], [154], [155], [156] or the output of the SLC's dc-dc stage [16], [26], [145], [146], [147]. The former ties the PV string's current ( $i_S$ ) to the PV modules' current, limiting the utilization of the SLC's additional degree of freedom. To utilize this degree of freedom, in [17], the output current flowing from PV modules [ $i_d$  in Fig. 17(a)] is controlled. The latter offers the advantage of decoupling PV modules and PV string currents, enhancing control flexibility [134]. Yet, connecting to the SLC's output results in higher voltage requirements for the MIC components due to the typically elevated voltage level at the output of the dc-dc stage of the SLC compared to its input.

Generally, two main PV2B SDPP architectures exist: MIMO and MISO. MIMO requires isolated MICs to prevent short-circuiting PV modules during operation. A potential MIC topology for MIMO is the dual active full-bridge, albeit complex due to many switches. Alternatively, flyback converters, known for high voltage gain, simplicity, and galvanic isolation, are suitable. Both unidirectional [148], [157] and bidirectional [16], [26], [145], [146], [147] flyback MICs have been reported for MIMO PV2B SDPP architectures. For the latter, some control approaches divided into two levels: DMPPT and central controller have been proposed. DMPPT, managed by the MICs, tracks the MPP of each PV module,



**FIGURE 18.** Possible MIC's topologies for MISO PV2B SDPP. (a) Multiwinding transformer flyback. (b) Multistacked. (c) Resonant-based topologies.

while the central controller adjusts the PV string current for overall power optimization [16], [26], [145], [146], [147].

In the LPPT method [145], [147], the central controller aims to minimize total power processing by setting the PV string current. This technique employs independent MPPT control for each PV module but it faces issues, such as uneven power distribution in DPP converters and steady-state oscillations. The unit-minimum LPPT control [146] addresses the former problem by distributing power evenly among the converters, albeit still exhibiting steady-state oscillations. A hybrid control approach combining LPPT and power rating balancing based on VE has been proposed to mitigate oscillations [16]. However, it falls short in achieving true MPP operation of the PV modules. An improved power-rating balance control technique ensures true DMPPT using finite-state-machine-based MPPT while also providing power rating balancing, but increasing complexity [26]. Moreover, a distributed digital controller has been developed to achieve DMMPT for unidirectional flyback MICs [148], but it sacrifices optimal power processing.

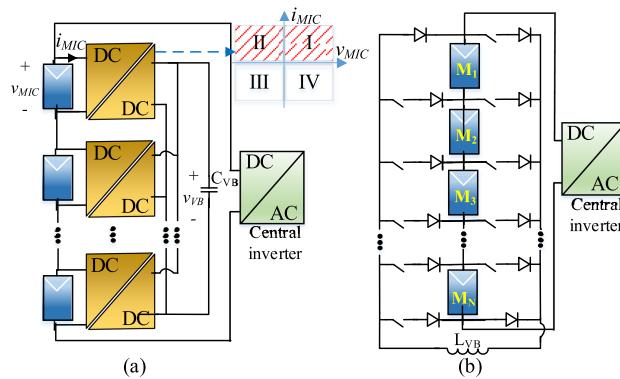
Table 6 provides a comparison of various control techniques for the MIMO PV2B SDPP architecture.

Fig. 18 shows several potential MIC topologies for MISO PV2B SDPP. Examples include multiwinding transformer flyback [156], multistacked topologies [149], [150], and resonant-based topologies [152], [153], [154], [155]. Literature also reported the multiwinding transformer active full-bridge [135]. While the multiwinding flyback and active full-bridge exhibit fewer switches compared to their MIMO counterparts, they require a multiwinding transformer, complicating implementation and scalability. In the multistack topology, MICs utilizing two inductors like SEPIC, Zeta, and isolated Ćuk are applicable [149], [150]. However, the Zeta-based topology necessitates a floating gate driver, and the Ćuk-based one is unfeasible without a transformer, favoring the SEPIC-based option. For resonant-based topologies, two-switch [151], [152] or four-switch [153] voltage equalizers using a resonant converter and voltage multiplier have been proposed, offering simplified architectures but suffering from limitations such as the inability to work with true MPPT

**TABLE 6.** Comparison of Control Techniques for MIMO PV2B SDPP Architectures With Bidirectional Flyback Topology

Features	Approaches	Hybrid control [16]	Least power point tracking [17], [145]	Direct power point tracking [147]	Unit-least power point tracking [146]	Improved power rating balance [26]	Distributed Coordination <sup>(*)</sup> [148]
<b>Module level tracking</b>	Near MPP	True MPP	True MPP	True MPP	True MPP	True MPP	True MPP
<b>Power distribution among MICs</b>	Even	Uneven	Uneven	Even	Even	Even	Uneven
<b>Local current/voltage sensing</b>	Yes/No	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
<b>Central current/voltage sensing</b>	Yes/No	Yes/No	Yes/No	Yes/No	Yes/No	Yes/No	---
<b>Algorithm tracking speed (Module/System level)</b>	Fast/Fast	Slow/Medium	Medium/Fast	Slow/Medium	Medium/Fast	Fast/Fast	
<b>Interfacing between algorithms at (modules and system)</b>	No	Yes	Yes	Yes	No	Yes	
<b>Steady-state oscillations (Module/System level)</b>	No/No	Yes/Yes	Yes/No	Yes/Yes	No/No	Yes/---	

<sup>(\*)</sup> This reference used unidirectional flyback topology.



**FIGURE 19.** PV2VB SDPP architecture with (a) capacitive virtual bus or (b) inductive virtual bus with corresponding appropriate MICs.

algorithms, unidirectional power flow, component rating dependence on position in the PV string, and poor scalability.

Unlike PV2PV architectures, PV2B avoids the accumulation effect, ensuring that MICs' maximum power ratings remain below the PV module's MPP, even in worst-case scenarios. Yet, the primary challenges in PV2B SDPP architectures revolve around high-voltage step-up ratios required by MICs, posing hurdles in designing efficient and cost-effective MICs. In addition, components on the MICs' dc bus side face heightened voltage stress, leading to increased power losses and costs. Moreover, scalability is limited as expanding the system with more PV modules necessitates MIC redesign. A solution to mitigate these challenges is the segmented PV2B SDPP structure [161].

### 3) PV TO VIRTUAL BUS (PV2VB)

In the PV2VB SDPP architecture, the MICs primaries and secondaries are connected to a common virtual bus and PV modules, respectively, as shown in Fig. 19. In this architecture, MICs connected to PV modules with high power generation inject power into the virtual bus while the others draw power. The virtual bus incorporates either capacitive or inductive storage elements. In capacitive PV2VB architectures [see Fig. 19(a)], bidirectional-current and isolated MICs are essential to manage power flow and prevent short-circuiting among PV modules. In a PV string with  $N$  PV

modules,  $N+1$  actuators consisting of  $N$  MICs and one SLC exist; the latter enables regulation of the virtual bus voltage to maintain power balance and stabilize its voltage, whereas the  $N$  MICs track the MPP of the  $N$  PV modules. Therefore, unlike PV2B architectures, PV2VB architectures lack an extra degree of freedom for power optimization. Moreover, capacitive PV2VB systems require high-energy storage capacity to mitigate voltage fluctuations, necessitating high-capacitance capacitors. However, PV2VB offers advantages over PV2B, such as the ability to set an appropriate voltage for the virtual bus independently of PV module characteristics. Besides, unlike PV2PV, PV2VB architectures are not affected by the accumulation effect. Consequently, the maximum required MICs power rating in the worst-case scenario aligns with PV2B counterpart [158]. In PV2VB SDPP architectures, bidirectional isolated MICs are required [24], [125], [158], [159], [160], [162], and bidirectional flyback topologies are commonly preferred due to their noted advantages.

Various control strategies have been explored in the literature for achieving both VE and True MPP using flyback topologies. In one approach [125], VE with open-loop control is implemented for each SDPP converter, employing bidirectional flyback topologies with a HFT ratio of 1.

Moreover, a near MPPT closed-loop control approach is introduced in another study [158], where the current flow in the MICs is regulated based on the voltage error between the primary side (PV modules) and secondary side (virtual bus) voltage with a dc gain ( $i_{pri} = K(V_{VB} - V_{PV_i})$ ). Olalla et al. [24] emphasized the importance of the dc gain for proper balancing and efficiency of MPP tracking. A similar closed-loop control strategy is proposed in [159], where the switch duty cycle is adjusted proportionally to the voltage difference between the PV modules and the virtual bus ( $D_{pri} = K(V_{VB} - V_{PV_i})$ ). In addition, Bell and Pilawa-Podgurski [160] suggested a distributed asynchronous algorithm to achieve True MPP, reducing cross-coupling effects among MICs with a sufficiently large bus capacitance. In [160], an approach in which an inner loop track the MPP of PV submodules by adjusting the operation of the MICs while an outer loop regulates the virtual bus voltage over a slower perturbation period is proposed. In all these control approaches [125], [158], [159], [160], maintaining the average power of the virtual bus at zero is crucial

**TABLE 7.** Comparison of Control Approaches for Capacitive PV2VB SDPP Architectures With Bidirectional Flyback Topology

Features	Approaches	VE [125]	$i_{pri} = K(V_{VB} - V_{PVi})$ [158]	$D_t = K(V_{VB} - V_{PVi})$ [159]	Distributed asynchronous MPPT [160]
<b>Module level tracking</b>	Near MPP	Near MPP	Near MPP	Near MPP	True MPP
<b>Local current/voltage sensor</b>	No/No	No/Yes	No/Yes	No/Yes	Yes/Yes
<b>Central current/voltage sensor</b>	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
<b>Steady state perturbation oscillation*</b>	No	No	No	No	Yes
<b>Communication requirement</b>	No	No	No	No	No
<b>Algorithm tracking speed</b>	Fast	Fast	Fast	Fast	Slow
<b>Capacitance of Virtual Bus per SMIC</b>	2200 uF	40 uF	66 uF	17 mF	

\* Here, only the oscillation arising from DMPPT controllers is considered. Any possible oscillations due to the central controller are not accounted for.

**TABLE 8.** Comparison of SDPP Architectures

		Advantages	Challenges
PV- PV	[123], [124], [128], [129], [133]	1- Voltage rating depends only on PV module's voltage 2- Allows using non isolated converter topologies 3- High efficiency and compact MICs	1- Accumulation effect 2- Cross-coupling effect
PV2B	<b>Bidirectional</b> [16], [17], [145] [26], [146], [147]	1- Extra degree of freedom to optimize size, cost, and losses 2- No accumulation effect 3- Low current at the MICs' DC Bus	1- Complex converter topologies 2- Requires high voltage gain 3- Voltage rating depends on Bus voltage 4- Poor scalability 5- Cross-coupling effect
	<b>Unidirectional</b> [148], [149], [150], [151], [152], [153]	1- Simpler topologies compared to Bidirectional counterpart 2- No accumulation effect 3- Low current at the MICs' DC Bus	1- Unable to optimize overall power processing 2- Requires high voltage gain 3- Voltage rating depends on Bus voltage 4- Poor scalability 5- Cross-coupling effect
PV2VB	<b>Capacitive VB</b> [125], [158], [159], [160]	1- Lower Components voltage rating compared to PV2B 2- Lower power processing compared PV2PV architecture (in long PV strings)	1- Requires isolated converters 2- Requires high-capacitance capacitors in Virtual Bus 3- Cross-coupling effect
	<b>Inductive VB</b> [163], [164], [165]	1- High reliability 2- Allows using non isolated converter	1- Complex controller 2- Unable to cope with fast changing mismatch conditions. 3- Cross-coupling effect

for achieving a constant virtual bus voltage and stable operation. A comparison among capacitive PV2VB SDPP control techniques is presented in Table 7. The inductive PV2VB architecture proposed in [163], [164], and [165] [see Fig. 19(b)] offers an alternative approach to capacitive PV2VB architectures. Here, unshaded PV modules charge an inductor, which then redistributes stored energy to support shaded PV modules by connecting them in parallel. This method allows all PV modules to operate at their MPP by providing an alternative path for excess MPP current. By replacing capacitors with inductors at the virtual bus, this architecture helps to enhance reliability. In addition, it eliminates the need for HFTs, thereby improving both cost-effectiveness and efficiency of the MICs. However, implementing this architecture requires highly complex control algorithms to manage switching strategies, set duty cycles, and detect shadows. In some instances, optimizing the switching architecture may be time-consuming, leading to challenges in adapting to rapidly changing mismatch conditions. Moreover, the size of the inductor is dependent on the length of the PV string, and the presence of diodes at both ends of the PV string can hinder scalability.

A summary outlining the primary advantages and challenges of various SDPP architectures is presented in Table 8. In [24] and [122], it is shown that even when considering 98% efficiency for dc-FPP converters and 90% efficiency for SDPP converters, the PV2PV, PV2B, and PV2VB architectures

exhibit efficiency improvements of 0.3%, 1.6%, and 1.3%, respectively, over their FPP architecture counterparts. Furthermore, these efficiency gains are achieved while the power ratings of SDPP converters in PV2PV, PV2B, and PV2VB are 33%, 16%, and 33% of those of the dc-FPP converters. These results demonstrate potential for reducing initial costs and improving the LCOE of PV systems through SDPP architectures.

### B. PARALLEL DIFFERENTIAL POWER PROCESSING (PDPP)

In a PV system, each PV group must operate under the same voltage when connected in parallel. However, varying operating conditions may lead to different MPP voltages, making it impossible to reach all PV groups MPP simultaneously. As shown in Fig. 13(b), PDPP architectures provide the required differential voltage between PV groups and a common bus to eliminate mismatch losses among parallel-connected PV groups. Since parallel connections suffer lower power losses due to mismatches compared to series connections, limited literature is available about PDPP, especially in comparison to SDPP. Nonetheless, PDPP architectures offer promising advantages over traditional FPP SLCs. They typically require lower component ratings, resulting in reduced system costs, and operate with lower primary-side voltages or secondary-side currents, thereby enhancing system efficiency [32]. It is important to note that PV string current passes through

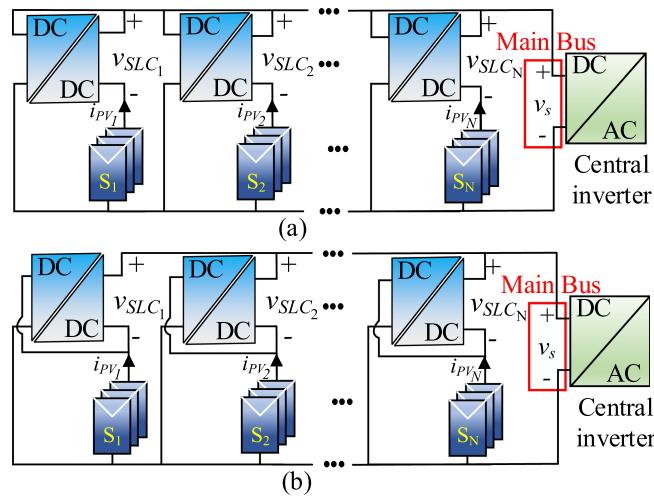


FIGURE 20. PV2B PDPP architectures. (a) PV2B-I . (b) PV2B-II.

DPP converters in PDPP architectures, resulting in conduction losses even under uniform operating conditions.

Although PDPP can be applied at various levels of granularity, here, it is primarily referenced as the SLC. The literature has introduced PV2B and PV2VB PDPP architectures, while PV2PV architectures are absent. The advantages and disadvantages of PDPP architectures closely resemble those of their SDPP counterparts. Below, we provide a concise overview of PDPP.

### 1) PV TO BUS PARALLEL DPP (PV2B PDPP)

In the PV2B PDPP architecture, each SLC's primary is connected to the dc bus (see Fig. 20). Typically, the output voltage of each SLC and the dc bus voltage act as control actuators. However, with only  $N$  PV string voltages as control objectives, there are  $N$  control objectives and  $N+1$  control actuators. Consequently,  $i$ th PV string operates at its MPP by adjusting the duty cycle of the  $i$ th SLCs, while the additional degree of freedom from the central converter helps minimize power losses by regulating the dc bus voltage. To the best of the authors' knowledge, only SLCs generating positive voltage have been proposed for PV2B PDPP architectures [32], [166], [167], [168], [169]. However, with SLCs exclusively generating positive voltage, the dc bus voltage must consistently exceed the voltage of the PV string with the highest MPP voltage. Ideally, the dc bus voltage should match the highest actual MPP string voltage. While this assumption can reduce processed power, achieving it is challenging as it necessitates some SLCs to operate at extremely low duty ratios. To overcome this issue, the dc bus voltage must increase, leading to a significant rise in processed power [167]. Consequently, despite the additional degree of freedom, when SLCs only operate with positive voltages, optimization of power processing remains unrealized. DPP architectures are classified based on how the primary side of the SLCs is connected. The commonly analyzed PV2B architectures are further divided

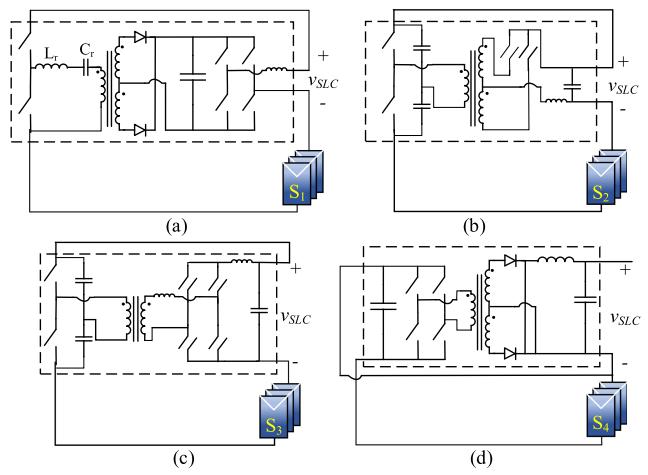


FIGURE 21. Topology for PV2B PDPP: (a) series resonant converter [170]. (b) current fed resonant push-pull [171], (c) current-fed full-bridge [172], and (d) full-bridge [176].

into two types: PV2B-I [32], [170], [171], [172], [173] and PV2B-II [38], [174], [175], [176]. In PV2B-I, the primary side of the SLCs connects to the main bus [see Fig. 20(a)], whereas in PV2B-II, the primary side connects directly to the PV strings [see Fig. 20(b)]. The optimal architecture for any application is the one that results in the lowest maximum power processing losses [41].

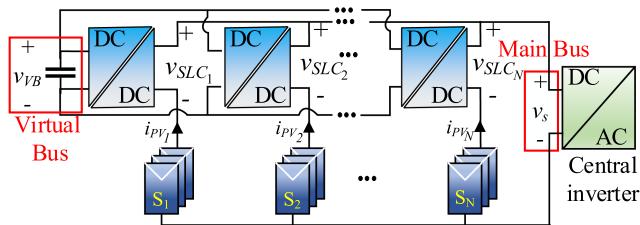
In [175], a buck-boost converter was chosen as the SLC for the PV2B-II architecture. While these SLCs are designed to compensate for the voltage differences between the PV strings and the main bus, they must also manage the full current produced by the PV strings. This requirement necessitates that the components endure the voltage from the PV strings, leading to SLCs with power ratings similar to those of FPP converters. In [32], [173], and [174], a flyback converter is employed in both PV2B-I and PV2B-II architectures. Although flyback converters are favored for their simplicity, their application is generally restricted to power outputs of a few hundred watts. Consequently, other research works [38], [170], [171], [172], [174], [176] have explored various topologies, including series resonant converters [170], current-fed resonant push-pull converters [171], current-fed full-bridge converters [172], and full-bridge converters [176] to improve power handling capabilities (see Fig. 21), although this often comes at the cost of simplicity.

Although high efficiency has been reported for PV2B architectures, directly connecting SLCs to the main bus or PV strings presents three main disadvantages. Firstly, the voltage rating of SLCs is determined by the PV strings or main bus voltage. Second, the scalability of the PV system is limited: adding PV modules to a PV string increases the string's voltage, necessitating SLCs with higher voltage ratings. These first two issues also exist in FPP SLCs. Lastly, PV2B PDPP require SLCs with high-voltage conversion ratio ( $\frac{v_{SLC}}{v_s}$ ).

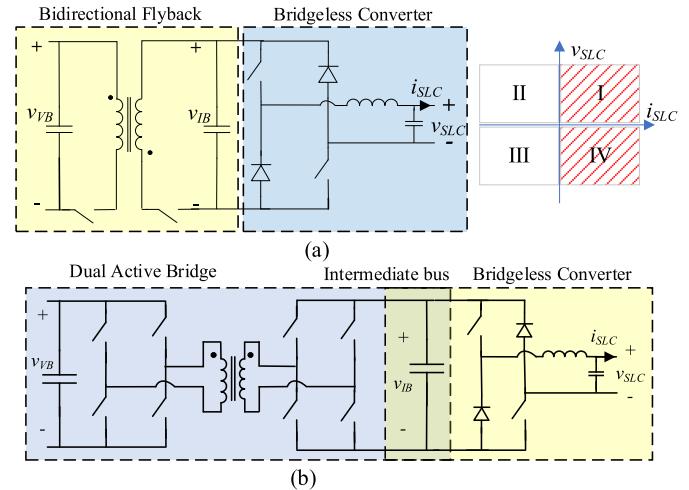
**TABLE 9. Comparison of PDPP Architectures [177]**

Ref.	Architecture	SLCs topology	Bidirectional SLCs	Isolated SLCs	CVR <sup>1</sup>	Scalability	VCR <sup>2</sup>	Power level	Reported efficiency (%)
[32]	PV2B-I	Flyback	No	Yes	High/low <sup>3</sup>	Low	High	50 W	89-97
[170]	PV2B-I	Series resonant converter	No	Yes	High/low	Medium	Medium	4 kW	97.75-98.82
[171]	PV2B-I	Current fed resonant push-pull	Yes	Yes	High/low	Low	High	2.2 kW	97.8-98.8
[172]	PV2B-I	Current-fed full-bridge	Yes	Yes	High/low	Low	High	2.2 kW	95.5-98.2
[173]	PV2B-I	Flyback	No	Yes	High/low	Low	High	25 W	98.5
[175]	PV2B-II	Buck-boost	No	No	High	Low	High	3.5 kW	96-98.9
[174]	PV2B-II	Flyback	No	Yes	High/low	Low	High	100 W	70-90
[38]	PV2B-II	Full-bridge	No	Yes	High/low	Low	High	821 W	98-99
[176]	PV2B-II	Full-bridge/Push-pull	Yes	Yes	High/low	Low	High	750 W	98.6-99.58
[177]	PV2B-II	Full-bridge	No	Yes	High/low	Low	High	750 W	98.8
	PV2VB	DAB/BL	Yes	Yes	Low	High	Low	4 kW	96.4-99

1: CVR: Components' voltage rating. 2: VCR: Voltage conversion ratio. 3: High/low: There exist components with high and low voltage rating



**FIGURE 22. PV2VB PDPP architecture.**



**FIGURE 23. Converter topology for PV2VB PDPP architecture: (a) Flyback converter followed by a BL converter and (b) DAB converter followed by a BL converter.**

## 2) PV TO VIRTUAL BUS PARALLEL DPP (PV2VB PDPP)

The PV2VB PDPP architecture is a novel approach where SLC inputs connect to a common isolated dc bus known as the virtual bus, instead of the main bus (see Fig. 22). This architecture offers flexibility by allowing for a lower voltage selection for the virtual bus compared to the dc bus, resulting in cost savings and reduced passive component sizes during SLC design and construction. Moreover, lower voltage converters emit less EMI and RFI, simplifying compliance with EMC standards. Moreover, this architecture has superior scalability compared to traditional FPP architectures, so it allows for the addition of new PV modules to strings without being limited by SLC component voltage tolerance. This facilitates mass production and reduces manufacturing costs [31]. The PDPP converters in PV2VB PDPP architectures must be voltage-source converters for connecting to the virtual bus, and be isolated to enable the independent control of PV strings.

Moreover, to maintain a constant virtual bus voltage in a steady state, the average power of the virtual bus must be zero. This necessitates the use of bidirectional converters. Given that PV strings' current is always positive, some SLCs must produce negative output voltage, while others must produce positive output voltage. Therefore, SLCs for PV2VB PDPP must generate both positive and negative output voltages, functioning in both the 1st and 4th quadrants of the  $V$ - $I$  curve.

An appropriate SLC architecture, comprising a bidirectional flyback converter and a bridgeless converter [see Fig. 23(a)], has been proposed in [31]. However, high power rating converter must be usually designed for SLCs, and for

high power rating SLCs, other topologies, such as dual active bridge converters, are preferable [see Fig. 23(b)] [177]. Finally, a comparison of PDPP architecture with associated topologies has been done in Table 9.

## C. SERIES-PARALLEL DPP (SPDPP)

SDPP strings cannot be paralleled effectively due to voltage mismatch issues, leading to reduced power production. One solution is connecting each SDPP string to a separate FPP SLC, but this adds losses and cost to the system [16], [178]. Similarly, PDPP architectures face challenges in effectively connecting PV modules in series due to current mismatch issues. An emerging solution to these challenges is the SPDPP architecture, depicted in Fig. 24. SPDPP allows for optimal power extraction from a PV array under mismatch conditions while ensuring that MICs and SLCs process only a fraction of the total power. Despite being relatively under-explored, the SPDPP concept holds promise for high-power PV systems with enhanced efficiency. Various architectures can be implemented within the SPDPP framework, for example: combining PV2PV SDPP and PV2B PDPP converters to

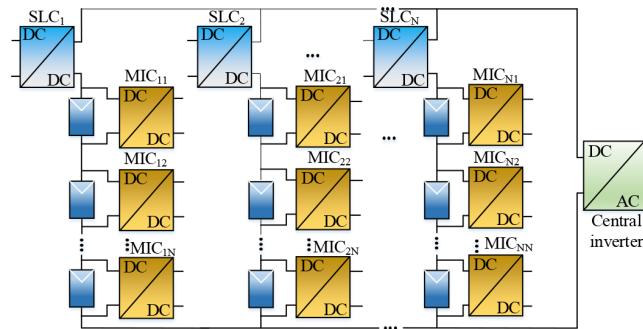


FIGURE 24. SPDPP architecture.

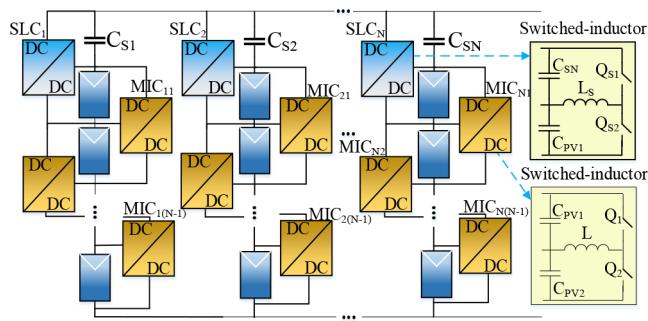


FIGURE 25. Modular SPDPP architecture.

achieve an SPDPP architecture, as demonstrated in [179] and [180].

A distinct SPDPP topology, based on a modular DPP concept, has been presented in [33], [181], and [182] (see Fig. 25). This architecture enhances modularity and scalability through the utilization of switched inductors in all SPDPP MICs and SLCs. However, the component ratings of the SLCs differ from those of the MICs [33]. In this architecture, PV2PV SDPP MICs are deployed to mitigate mismatches among series-connected PV modules, while the inputs of the SLCs are connected to one of the PV modules to allow for parallel connection of PV strings. The top converter (SLC) handles the full string current and the differential voltages between the PV string voltages and the bus voltage in parallel strings. Meanwhile, all other converters (MICs) manage the differential currents between the series PV modules. Moreover, to diminish cross-coupling effects among the PV modules, a novel control strategy employing a voltage inner loop and a power outer loop has been proposed for tracking the PV modules' MPP [33], [181].

## V. HYBRID AND HIERARCHICAL DMPPT ARCHITECTURES

DMPPT operates at various levels within PV systems, each with its unique requirements. For instance, the number of PV modules per PV string can vary based on the application, while PV modules typically consist of three fixed PV submodules. Hence, modularity and scalability are often desired at the module level rather than the submodule level. Another crucial distinction among different levels is their power and voltage

ratings, resulting in varying rated voltages for SMICs, MICs, and SLCs components. These distinctions can be leveraged to devise hybrid and hierarchical DMPPT architectures that operate at different levels, streamlining the design and operation of PV systems.

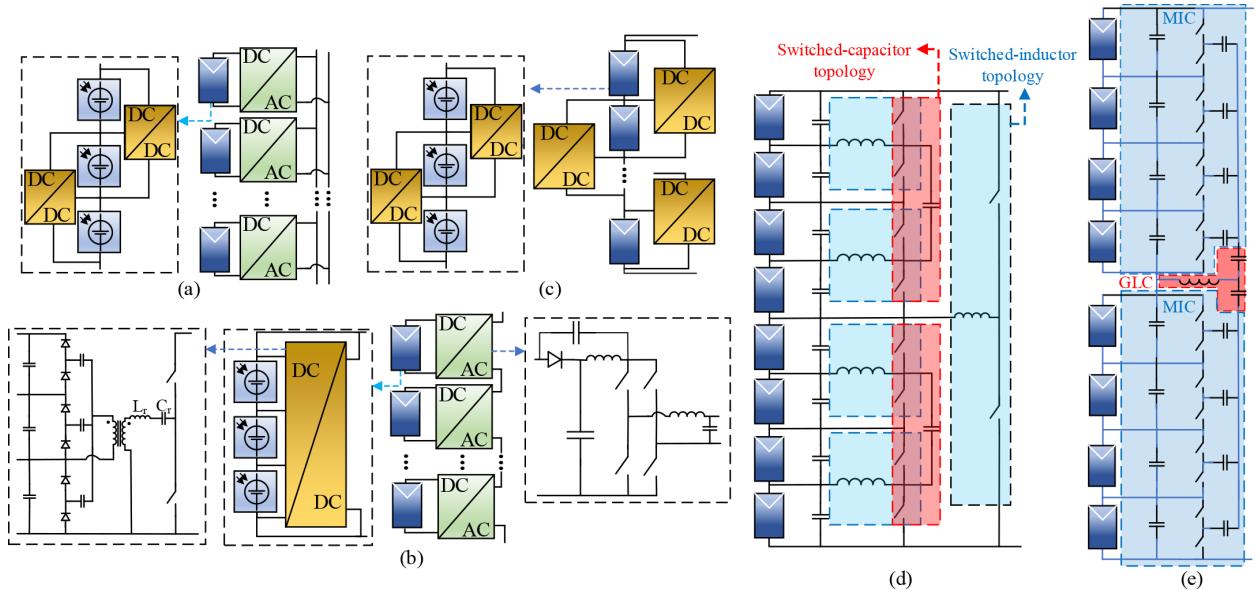
Sections III and IV have provided detailed insights into various DMPPT techniques, each presenting distinct advantages and challenges. For instance, microinverters exhibit immunity to cross-coupling effects and offer robustness against MIC and PV module failures. However, they necessitate high-gain converters, with the required gain escalating as granularity increases, particularly at the submodule or cell level. Conversely, PV2PV SDPPs are more suitable when the number of PV groups is low due to the accumulation effect, such as at the level of PV submodules. To leverage the strengths of both approaches, a hybrid solution is proposed that integrates PV2PV SDPP architectures with switch inductor topology as SMICs. This architecture aims to reduce mismatch-related losses at the submodule level while incorporating microinverters as MICs to enhance modularity within the PV system [see Fig. 26(a)] [128], [183].

In scenarios where PV2B SDPPs are employed as SMICs, connected directly to the PV string, challenges associated with high-voltage PV strings emerge. Addressing these challenges, a recent study proposed a novel approach combining MMCI with PV2B SDPP [see Fig. 26(b)] [184]. In this architecture, PV2B SDPPs function as SMICs, while MMCI serves as MICs, facilitating power injection into the grid. Each SDPP output is connected to an inverter cell within the MMCI. This innovative architecture mitigates both the demand for high voltage gain and the need for components with elevated voltage ratings.

In [185], an architecture resembling PV2PV SDPPs is proposed, operating at both module and submodule levels [see Fig. 26(c)]. This architecture aims to alleviate accumulation effects inherent in conventional PV2PV SDPP approaches for two primary reasons. First, MICs handle differential power among PV modules, while SMICs manage that of PV submodules. In addition, SMICs associated with different PV modules operate independently, resulting in reduced overall power processing and converter ratings.

In [34], a hierarchical architecture is proposed, utilizing PV2PV SDPP switched-inductor topologies in combination with resonant switched-capacitor concepts, shown in Fig. 26(d). This architecture connects PV groups at different hierarchies, reducing the number of switches by sharing them between adjacent levels. However, a key limitation is its applicability only when the number of PV groups is a power of 2, leading to constraints on scalability. Moreover, varying voltage ratings across hierarchies diminish modularity, posing challenges for component selection and system design.

In [141] and [142], a hierarchical DMPPT approach utilizing various SDPP architectures at different levels is introduced. At the submodule level, SDPP is employed, while PV2PV SDPP architecture with DSCC MICs is used for groups of four PV modules. These groups are interconnected



**FIGURE 26.** Combination of different DMPPT techniques at different hierarchies (a) PV2PV with microinverter, (b) PV2B with MMCI, (c) PV2PV with PV2PV, hierarchical architecture proposed (d) by the authors in [34], and (e) [141] and [142].

using either a switchless group-level converter SDPP [141] or a modular SDPP [142] architecture [see Fig. 26(e)].

The hierarchical DMPPT approach is innovative and offers distinct advantages, indicating significant potential for future research to delve deeper into its capabilities and applications.

## VI. SUMMARY AND FUTURE WORKS

### A. SUMMARY OF CONTRIBUTIONS

This article classifies, reviews, and compares the various state-of-the-art DMPPT architectures with different levels of granularity, from string-level DMPPT down to module level, submodule level, and cell level. In modern and customized PV systems for integration in both urban and open environment, a highly granular DMPPT of PV (sub)modules—when economically feasible—is inherently able to minimize the effect of any nonuniformity and maximize the energy yield of the system. A highly granular control is not only beneficial for those sources of nonuniformity related to the position of the sun or to the geometry of the surroundings, but also to other conditions, such as fouling, soiling, and uneven degradation. Some studies [186], [187] indicate that microinverters achieve a more favorable LCOE, while another [188] suggests that string inverters can provide a lower LCOE. Generally, microinverters tend to perform better in complex or shaded environments, whereas string inverters may offer a more advantageous LCOE in simpler installations with uniform illumination over the PV modules. The selection of the best suited architecture and the required level of granularity depend strongly on the application, the characteristics of the PV system, the location, and the expected operating conditions.

The lower level of granularity of DMPPT is the string level, in which typically string/multistring inverters are used to independently control the different PV strings within a PV

system. Like the centralized MPPT through central inverters, string-level DMPPT architectures offer advantages, such as low complexity, cost-effectiveness, and high system efficiency in open environments, when nonuniformities within the PV system arise mostly among different PV strings, whereas each string is subject to (quasi-)uniform conditions. One example of such an application is east-west-oriented PV systems installed in an open environment, which does not cast dynamic shades over the PV systems during most of the day. However, the efficiency of string-level DMPPT architectures significantly decreases in applications like building-integrated PV systems, where different PV modules in a PV string are subject to different operating conditions, e.g., due to substantial dynamic partial shading. Similarly, in vehicle-integrated PV applications nonuniformities within small groups of cells may arise owing to 1) curvature of the modules, 2) different location of cells on the vehicle surface, 3) movement of the vehicle and corresponding changes in the irradiation of the various cells due both the variation of the relative position of the cell with respect to the sun and dynamic shading from the varying surroundings. To increase energy yield, the granularity of DMPPT must be increased, and module- or submodule-level architectures are preferable. They not only mitigate mismatch-related losses but also offer enhanced protection, monitoring capabilities, modularity, scalability, and simplification of the MPPT algorithm. Fig. 27 compares DMPPT at string level with module level architectures.

DMPPT architectures at the module and submodule levels are classified into two main categories: FPP and DPP. Focusing on FPP solutions, as shown in Table 10, microinverters and parallel dc-FPP architectures, which rely on parallel connection of the converters' output either to the ac grid (microinverters) or to a common bus/dc grid (parallel dc-FPP),

**TABLE 10.** Comparison of DMPPT Architectures

Feature	Architecture		AC-FPP		DC-FPP		SDPP				PDPP	
	Micro inverters	MMCIs	Parallel	Series	TCT	PV2PV	Bidirectional PV2B	Unidirectional PV2B	Capacitive PV2VB	Inductive PV2VB	PV2B	PV2VB
<b>Cross-coupling effect</b>	None	Mod	None	Mod	Mod	Sig	Min	Min	Min	Min	Min	Min
<b>Availability against failure</b>	High	Low	High <sup>1</sup>	Low <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>	Mod <sup>1</sup>
<b>Processed power</b>	Sig	Sig	Sig	Sig	Sig	Min - Sig <sup>2</sup>	Min	Min	Min	Min	Mod	Mod
<b>Accumulation effect</b>	No	No	No	No	No	Yes	No	No	No	No	No	No
<b>System efficiency</b>	Poor	Fair	Poor	Fair	Fair	Fair - Exc <sup>2</sup>	Good	Good	Good	Good	Fair-Good	Fair-Good
<b>Scalability</b>	Exc	Fair	Exc <sup>1</sup>	Fair <sup>1</sup>	Fair <sup>1</sup>	Poor <sup>1</sup>	Poor <sup>1</sup>	Exc <sup>1</sup>	Poor <sup>1</sup>	Poor <sup>1</sup>	Exc <sup>1</sup>	Exc <sup>1</sup>
<b>Converters voltage gain</b>	High	Low	High	Low	Low	Low	High	High	Low-Ave <sup>3</sup>	N/D	High	Low-Ave <sup>3</sup>
<b>Converters voltage rating</b>	High	Low	High	Low	Low	High	High	High	High	High	High	Low-Ave <sup>3</sup>
<b>Converter Simplicity</b>	Fair	Good	Good	Exc	Exc	Exc	Fair	Good	Fair	Good	Fair	Fair
<b>Converter Cost</b>	Poor-Fair	Fair	Poor-Fair	Fair	Fair	Fair - Exc <sup>2</sup>	Fair-Good	Good-Exc	Good	Good	Fair-Good	Fair-Good
<b>Isolated Converter</b>	OP	OP	OP	OP	OP	NR	RQD	OP	RQD	NR	OP	RQD
<b>Bidirectional Converter</b>	NR <sup>4</sup>	NR <sup>4</sup>	NR	NR	NR	RQD	RQD	NR	RQD	RQD	OP	RQD
<b>Recommended MPPT granularity level</b>	M	M	M	SM/M	M	C/SM/M	M	M	SM/M	M	S	S

Min: Minimal, Mod: Moderate, Sig: Significant.

Ave: Average.

Exc: Excellent.

OP: Optional (it adds extra features and options).

RQD: Required, NR: Not Recommended.

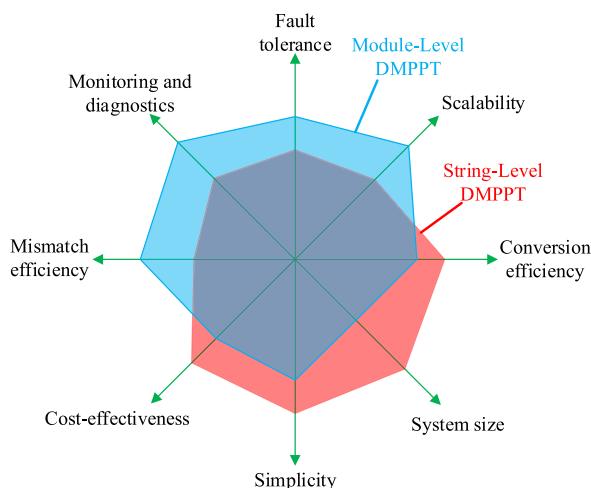
C/SM/M/S: Cell/Submodule/Module/String.

1: Without taking the central converter into account.

2: It depends on the length of the PV string.

3: It depends on the voltage defined for the virtual bus.

4: Here, "not recommended" refers to the DC-DC stage of the inverter.

**FIGURE 27.** Comparison between module-level MPPT (blue) and string level MPPT (red).

offer independent tracking of the MPP of each module without cross-coupling effects, remarkable resilience to failure, high flexibility, modularity, scalability, plug-and-play functionality, and high availability. These features make them suitable for applications in which PV modules are often subject to nonuniform conditions and high availability and low installation costs are crucial. However, it is not recommended to use microinverters for granularity higher than the module level because the required voltage gain becomes excessively

high (typically with an input of around 20 V at the submodule level and an output of 400 V on the dc bus).

On the other hand, the converters' output can be connected in series. The corresponding ac-FPP architectures are based on MMCIs, which generate multilevel output voltages, enabling low switching frequency, small ac filter size, low EMI, and higher efficiency compared to microinverter. Nevertheless, MMCIs present significant isolation coordination challenges. Consequently, despite being a topic of research, the practical application of MMCIs in PV systems remains limited. In application where the PV system is connected to a common bus or a dc grid, series dc-FPP systems offer higher efficiency and cost-effectiveness than their parallel counterparts, eliminating the need for high step-up voltage converters. However, both MMCIs and series dc-FPP architectures require series-connection of the converters' output, which results in cross-coupling effects and deteriorates flexibility and scalability.

As an alternative DMPPT approach, DPP architectures have attracted attention due to their ability to reduce power conversion losses, size, and cost of converters. DPP architectures are primarily divided into three groups: 1) SDPP, 2) PDPP, and 3) SPDPP. In DPP-based architectures, SDPP can only mitigate mismatches among PV elements connected in series. The SDPP PV2PV architecture offers several advantages, including low-voltage rating and the use of nonisolated MICs, which enhance efficiency, simplify the design, and reduce cost and size. In addition, since both the input and output

of SDPP PV2PV converters are connected to PV groups, they can be implemented at a very high granularity level [13]. However, this architecture suffers from the so-called accumulation effect, making it less suitable for long PV strings. Yet, it may suit well PV wearable applications, with low power and short PV strings.

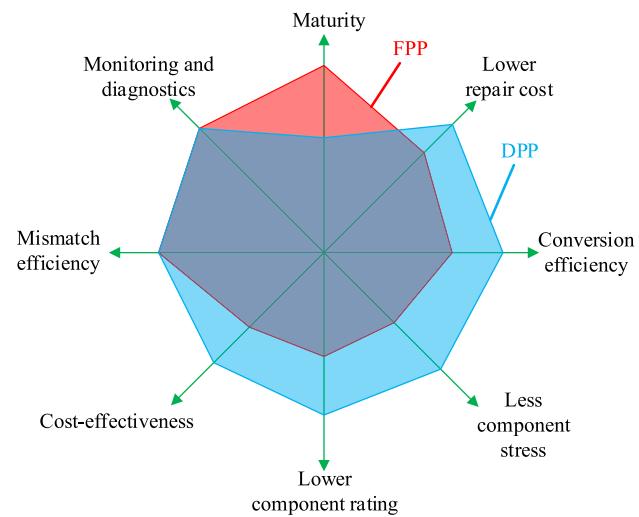
Unlike SDPP PV2PV architectures, PV2B eliminates the accumulation effect but introduces other challenges: 1) it requires high-voltage-rated converters, especially when the MICs' primary side is connected to the output of the dc–dc stage of the SLC (see Fig. 17); 2) it may necessitate isolated and bidirectional converters to fully utilize the architecture's potential; 3) PV2B architectures require very high gain converters for granularity levels higher than the module level; and 4) it reduces scalability, as adding new PV modules increases the dc bus voltage when the MICs' primary side is connected to the input of the dc–dc stage of the SLC (see Fig. 17), which may require new MICs and/or SLCs with a higher voltage rating.

The PV2VB architecture eliminates the accumulation effect while utilizing low-voltage-rated converters. However, it still requires isolated, bidirectional converters, and additional components, primarily capacitors, at the virtual bus. Since the virtual bus voltage can be user defined, it is possible to select a voltage lower than the dc bus. However, selecting a very low voltage may necessitate extremely high capacitance to maintain minimal voltage ripple, making it unsuitable for highly granular (e.g., cell level) DMPPT. In addition, since the voltage rating of the converters is independent of the dc bus voltage, the architecture enhances scalability.

On the other hand, PDPP architectures can only mitigate mismatch among PV elements connected in parallel, such as string/multistring inverters. PDPP architectures, especially PV2VB, need lower voltage SLCs and offer superior scalability, facilitating mass production compared to conventional counterparts. These features make them a suitable alternative for applications in which string/multistring inverters are typically used. However, the converters proposed for these architectures remain more complex than those in string/multistring FPP architectures. SPDPP, which combines the features of SDPP and PDPP, inherits the advantages and disadvantages of both. This approach enables optimal power extraction from PV elements connected in either series or parallel under mismatch conditions. This makes SPDPP more suitable for large PV systems in complex environments where partial shading occurs regularly.

## B. FUTURE DIRECTIONS AND EMERGING TRENDS

At present, solar panels are installed in both open and urban environments. Especially in the latter, there is still much to be gained, since every suitable building roof and facade will eventually have solar panels. Furthermore, beyond building integration, solar panels are expected to be seamlessly integrated into any type of infrastructure (canopies, ...), as well as on electric vehicles.



**FIGURE 28.** Comparison between FPP (red) and DPP (blue) architectures.

All these applications share a common major issue: dynamic shading through the day, which leads to a deterioration of conversion efficiency and thus of the LCOE. To enable the envisaged level of integration of PV technology—in other words, to massively deploy PV technology in the urban environment—researcher, companies, and designers of integrated PV systems are expected to shift their focus toward smart interconnection of cells within PV modules and intelligent and distributed power processing. As a result, the use of DMPPT architectures, which react immediately if an individual component is not working properly and can therefore increase the energy yield and consequently reduce the LCOE, is expected to become more and more common in the coming future.

A general comparison among FPP and DPP DMPPT architectures are shown in Fig. 28. While FPP architectures are established, proven technologies with a wide range of power converters available for both dc-FPP and ac-FPP at the submodule, module, string, and array levels, DPP is still in the research phase. However, some initial industrial products have emerged, and the market for DPP solutions is anticipated to expand, catering to both mass production and mass customization of PV modules and systems. The following analysis illustrates the substantial potential for reducing the LCOE in PV systems using the DPP architectures instead of their FPP counterparts in the future.

- 1) *Initial cost analysis:* The complexity of the DPP architecture, particularly in terms of topologies and controllers, is greater than that of FPP architectures. However, the voltage and current ratings—or both—of the components may be lower than those found in FPP systems. This feature, combined with enhanced scalability that supports mass production, is anticipated to lead to reduced production costs.
- 2) *Repair costs:* Due to the lower voltage and current ratings of components in DPP architectures compared to FPP systems, these components are generally less

expensive, which may also lead to reduced repair costs in the event of a component failure.

3) *Financial losses due to the downtime:* Generally, DPP architectures have the advantage of processing only a portion of the power generated by the PV strings, allowing most of the power to be directly delivered to the output. DPP architectures reduce stress on the components, leading to high availability, thereby potentially minimizing financial losses associated with downtime.

4) *Financial losses due to Conversion losses:* By only processing a portion of the power generated by the PV strings, DPP architectures result in lower conversion losses. Consequently, as reported in numerous articles, these architectures achieve high system efficiency, which helps mitigate financial losses associated with conversion inefficiencies.

These features highlight the significant potential to reduce the LCOE in PV systems when employing DPP architectures.

In conclusion, this article offers researchers valuable insights for future studies but also aids designers in choosing the most suitable architectures for their specific applications and needs. Ultimately, designers can perform a quantitative comparison of LCOE among only a few, promising candidates and choose the best architecture for their target application, together with the corresponding converter topologies and control strategy.

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