Multi-bit IDAC input Class D Amplifier

Master of Science Thesis

by

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Abstract

Class D amplifiers (CDA) have been used considerably in audio applications due to their high-efficiency behavior. Compared to standalone analog input CDAs, digital input CDAs are less sensitive to electromagnetic interference (EMI), which is preferred in automotive applications. For digital input CDAs, multi-bit current-steering DACs using tri-level units offer high dynamic range (DR) compared with other types of DAC. The main challenge in designing low total harmonic distortion plus noise (THD+N) and high DR IDAC lies in noise, mismatch, and ISI reduction. In this project, a new ISI resilient dynamic element matching technique is developed for mismatch shaping and ISI reduction in IDAC.

Index items: Class-D amplifier, current-steering DAC, mismatch shaping, THD+N, DR.

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Content

Chapter 1 Introduction

Speakers have become a crucial part of many modern applications, including smartphones, computers, cars, etc., by transferring electrical audio signals into their corresponding sounds. These electrical audio signals are usually at line level, but without amplification, these signals might lead to weak and distorted speaker output. Power amplifiers are usually needed in audio systems to not only increase the signal level but also deliver power to the speakers, which typically have a resistive component in the order of a few ohms.

The most common audio amplifier classes are A, B, AB, and D [1]. Class A amplifiers exhibit low distortion and noise, which makes them suitable for applications such as guitars, but their efficiency is poor due to the large quiescent current at the output stage [2]. The class-B amplifier's efficiency is better than class A since there is no quiescent current, but the crossover from positive to negative signal currents causes distortion [1]. To mitigate the crossover distortion, a small quiescent current is implemented in class-AB amplifiers, which allows them to operate as class-A amplifiers at small signals and class-B amplifiers at large signals. Although a theoretical efficiency of 78.5% can be achieved at maximum output by class AB amplifiers, typical audio music has a 10~20dB crest factor, and thus, class-AB amplifiers are mainly used in low-power applications [3]. While the power transistors in other amplifiers are mainly used in the saturation region, the power transistors in CDAs are either off or operate in the triode region. This minimizes the current when voltage exists across the transistor and reduces the voltage when current flows through the transistor, which makes their efficiency stand out from other amplifier counterparts. Typically, power efficiency of 90% can be achieved with CDAs [4], making them especially favored in high-power applications such as car audio systems.

1.1 Background

1.1.1 Class D amplifier

A conventional CDA consists of the loop filter, modulator, output stage, lowpass filter, and speaker, as shown in Fig. 1. Since the power transistors in the output stage operate as switches to ensure high efficiency, they create a square wave output. In order to carry audio information, a modulator is needed to change the duty cycle of the square wave according to the audio signal. Usually, this is realized by pulse-width modulation (PWM). This PWM square wave contains not only the audio signal but also the high-frequency carrier components. Thus, a lowpass filter is often needed for the recovery of the audio signal, which is often realized by an LC filter since capacitors and inductors do not dissipate energy. The loop filter suppresses the in-band unwanted tones by providing a high loop gain [5].

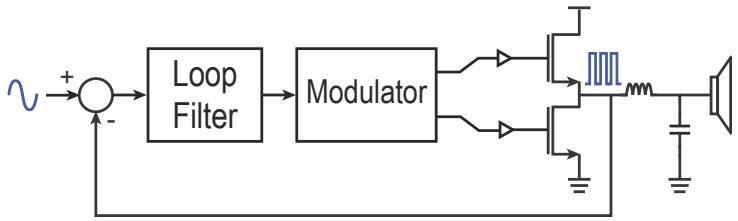

Fig. 1. Conventional class D amplifier

PWM signal can be generated by comparing an audio band signal (20~20kHz) to a triangle wave signal with a high switching frequency. Fig. 2 shows the generation of a natural PWM signal. When the signal input intersects with the triangle wave, the PWM output changes the polarity. The duty cycle of the PWM signal increases as the signal input level increases.

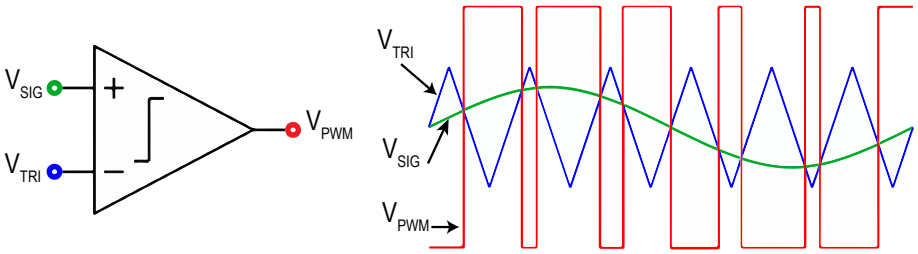

Fig. 2. Pulse width modulation

The spectrum of a PWM signal with a 2kHz sinusoidal signal and a 100kHz PWM carrier is shown in Fig. 3. Since there is no harmonic in the audio band, the PWM signal is considered to be inherently linear [4]. The audio signal can be recovered without distortion by a lowpass filter that has a cutoff frequency near the audio band.

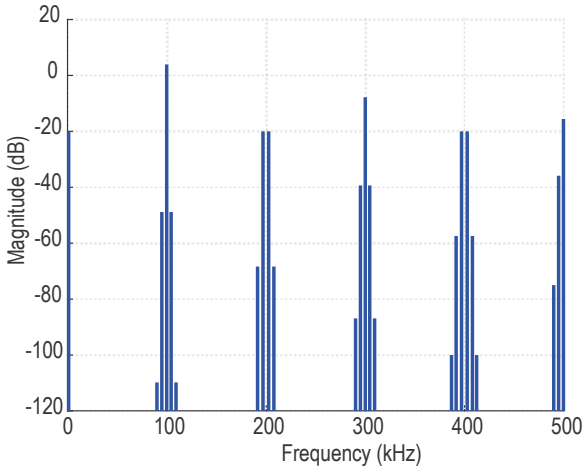

Fig. 3. PWM spectrum

Most audio sources nowadays are digital, while the audio signals are analog by nature. This suggests that a conversion between digital and analog signals has to be conducted. For the aforementioned analog input CDA, a standalone DAC is used to feed the CDA's input. However, this topology has two drawbacks. First, the analog input makes the CDA more susceptible to radio frequency interferences [6]. Second, as a discrete component in the system,

the standalone DAC increases the system area. Thus, integrated digital input CDAs are preferred.

For digital input CDAs, two common structures are shown in Fig. 4. In Fig. 4 (a), an on-chip DAC converts the digital input into an analog waveform and compares it with the feedback from the output stage. In Fig. 4 (b), the loop filter and PWM work in the digital domain, and an ADC ensures digital feedback from the output stage. However, this topology usually demands a high-performance ADC, whose nonidealities may become the bottleneck of the system [7]. Therefore, the analog feedback structure is chosen in the proposed architecture.

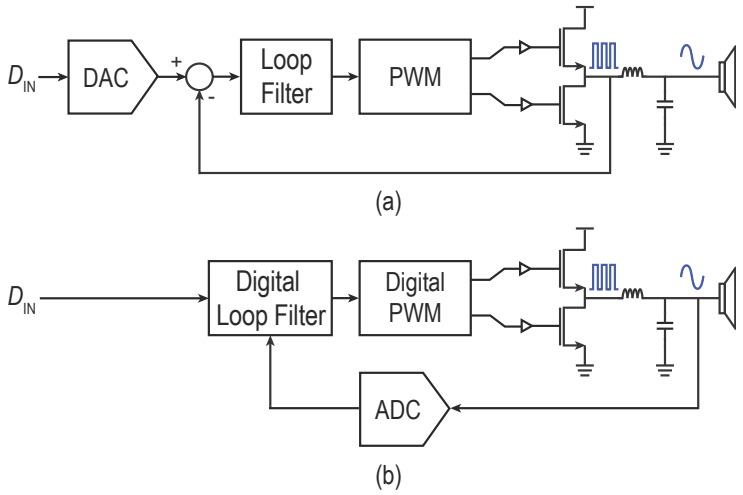

Fig. 4. Digital input class D amplifier: (a) analog feedback structure (b) digital feedback structure

1.1.2 DAC

In the architecture of Fig. 4 (a), DAC design is crucial for good total harmonic distortion plus noise (THD+N) and dynamic range (DR) performance.

A DAC produces an accurate summation of analog electrical unit quantities according to the given digital input code. A DAC unit generates a summable electrical unit quantity and is controlled by switches to connect to the common circuit node [8]. Dividing by the electrical unit circuitry, the DACs can be roughly classified into three categories: current-steering DACs (IDACs), resistive DACs (RDACs), and capacitive DACs (CDACs). Dividing by sampling methods, the DACs can be classified into Nyquist rate converters and over-sampled converters. Dividing by quantization levels, the DACs can be classified into single-bit and multi-bit converters. Due to component nonidealities, some mismatch and inter-symbol interference (ISI) are expected, and methods to reduce their effects on the system performance are often used.

1.1.2.1 DAC electrical unit circuitry types

An illustration of IDAC, RDAC, and CDAC is shown in Fig. 5. IDACs control their output by changing the polarities of the current units. RDACs control their output by different voltage or current divisions on the resistor array. CDACs control their output by charge redistribution between capacitors. Compared to IDACs, RDACs and CDACs often need precise low-noise

voltage references to drive the resistor or capacitor array [8]. IDACs often have fast speed, which may give IDACs an advantage over ISI. Tri-level IDACs usually exhibit good DR by only having the noise of the amplifier at zero inputs [9], which will be discussed in 2.2.2. However, with the same area, the mismatches of the transistors are worse than the resistors or capacitors, and the mismatch error of IDACs may need special consideration [10].

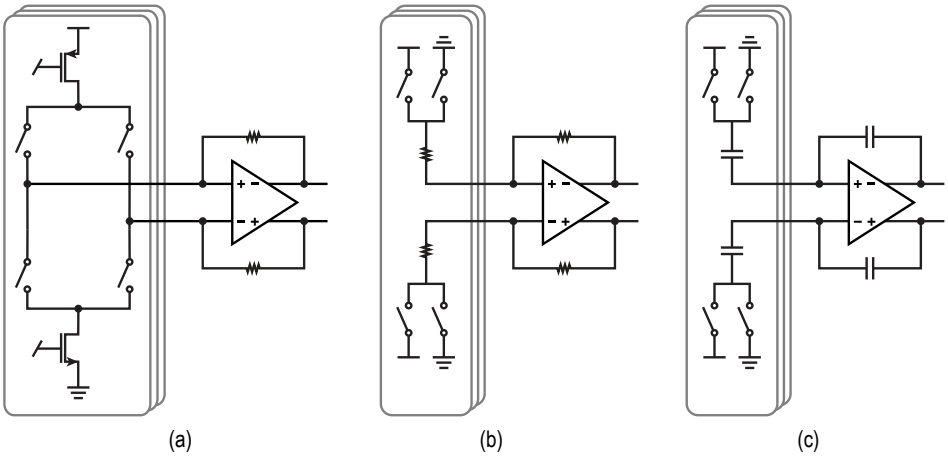

Fig. 5. DAC illustration: (a) current-steering DAC (b) resistive DAC (c) capacitive DAC

1.1.2.2 DAC sampling methods

Nyquist-rate converter's sampling rate can be as low as twice the bandwidth of the input signal. They exhibit a flat quantization noise spectrum, and their linearity and precision are mainly determined by the matching accuracy of the analog components (resistors, capacitors, and current sources) [8]. This, in practice, is limited to about 0.02%, which suggests that their effective number of bits (ENOB) is about 12 [8]. However, higher linearity and resolution of as much as 18 bits may be required for applications like digital audio. Although some Nyquist-rate converters can reach this accuracy, they may need long clock periods to convert a single sample or expensive trimming [10].

Oversampled data converters, or delta-sigma converters, use sampling rates typically 8 to 512 times higher than the Nyquist sampling rate [10]. Delta-sigma modulators (DSMs) can enable over 20 ENOB resolutions by concentrating the major part of the quantization noise outside of the signal band. Since almost all communication systems require a certain amount of oversampling, for instance, to facilitate the necessary analog filtering, oversampled data converters are more commonly used [8].

1.1.2.3 Quantization levels

One-bit quantizer has the advantage of inherent linearity and circuitry simplicity. However, it is prone to instability in DSM with order ≥ 2 and creates a large quantization error, which may lead to a smaller maximum stable amplitude (MSA) compared to a multi-bit quantizer. Since the error waveform produced by a one-bit quantizer has a larger magnitude, a more linear post-DAC filter is needed than a multi-bit counterpart [11]. Also, a higher oversampling ratio

(OSR) is required for a one-bit quantizer to realize the same signal-to-quantization noise ratio (SQNR) as a multi-bit quantizer. The multi-bit quantizer is also less sensitive to jitter. However, the multi-bit quantizer is also more sensitive to mismatch, and thus, mismatch shaping methods have been developed [11].

1.1.2.4 Mismatch and ISI shaping technique

Mismatch and ISI errors are caused by component nonidealities. The mismatch error is a static error where DAC units exhibit electrical quantities that deviate from the desired value. Although mismatch, being inversely proportional to the element sizing, can be scaled down at the cost of increasing area [12], this is undesired for high-resolution converters, and instead, mismatch shaping techniques are usually applied [11]. ISI is a transition-based dynamic error due to the asymmetry in the rise and fall time in the DAC output waveform. It may result from DAC switch parasitic, gate drive circuitry, etc. Methods to balance ISI errors are often implemented [11].

Data weighted averaging (DWA) [13], a common dynamic element matching (DEM) method, is shown in Fig. 6. Each column represents one DAC unit usage according to time. DAC units connected to positive reference are indicated in blue, and their selection is rotated with time, which produces a 1st-order mismatch error shaping [12]. However, this method creates signal-dependent transitions (shown as arrows), making it vulnerable to ISI error.

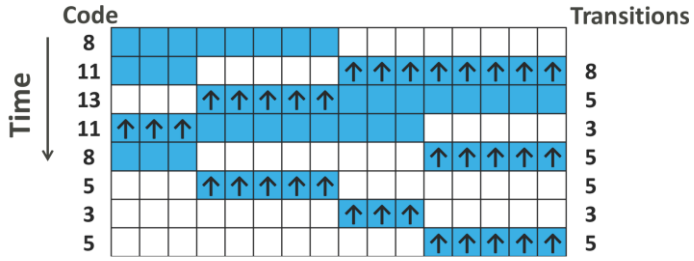

Fig. 6. Data weighted averaging [12]

Return-to-zero (RZ) DAC is a common solution to ISI errors. Fig. 7 is an illustration of a RZ DAC output. Every DAC unit that transfers to non-zero values must return to 0 within a clock period. This makes transitions and ISI proportional to the desired output without introducing distortion. However, since the output waveform experiences large transitions each clock period, RTZ DAC is sensitive to jitter and has a higher linearity requirement on the subsequent amplifier [12].

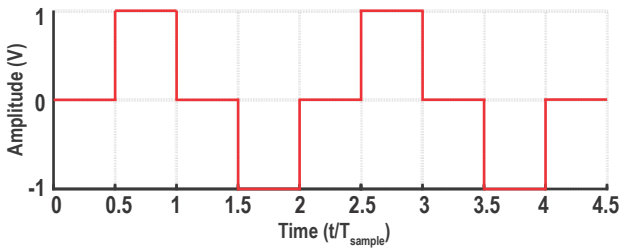

Fig. 7. Return-to-zero DAC output waveform

Real-time DEM (RT DEM) [15] can deal with both mismatch and ISI errors. Shown in Fig. 8 is an example of a 4-unit DAC. To create the desired output, each element is used in one sample period and the pulse width of each element is proportional to the desired output [12]. The mismatch is averaged out in each sample and the ISI error is reduced by introducing about 4 zero-to-one transitions in each sample period. This method requires higher clock frequency due to the clock division in each sample period.

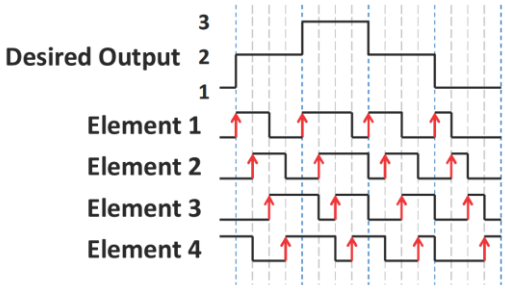

Fig. 8. Real-Time dynamic element matching [15]

1.2 Innovation and goal

In the proposed architecture, a multi-bit current steering DAC input Class D amplifier is implemented. This project aims at achieving a low THD+N of less than -110dB and a high DR of around 126 dB. To achieve this performance, a main innovation of a transition-rate-balanced real-time dynamic element matching technique is developed for mismatch shaping and ISI reduction in the IDAC. A new IDAC switch control circuitry is also developed.

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Chapter 2 CDA Architecture

2.1 High-level architecture

The block diagram of the high-level chip architecture is shown in Fig. 9. The digital audio source produces a 24-bit digital input signal with a 48kHz/s sample rate. This signal is up-sampled to 768kHz/s and fed into a 6th-order DSM, which truncates the signal into a 5-bit digital input code D_{IN}. The IDAC turns D_{IN} into differential analog current output that passes through a closed-loop analog feedback CDA structure. This structure consists of a 3rd-order loop filter with feedback resistors (R_{FB}), PWM, and the output stage. Finally, the output fully differential signal $V_{OUT} = V_{SWP} - V_{SWN}$ drives a speaker.

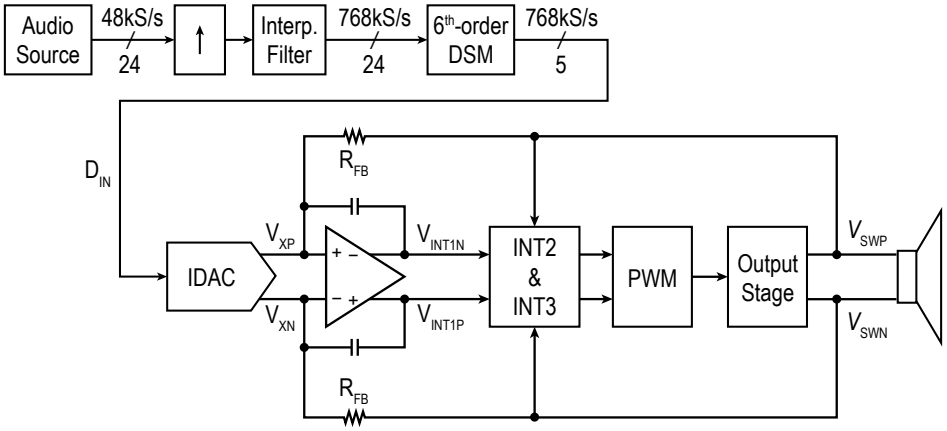

Fig. 9. High-level architecture

2.2 Digital input architecture

2.2.1 DSM

To simplify up-sampling, the sampling frequency of DSM f_S is picked to be an integer multiple of the audio source sample rate of 48kHz. With $f_S = 768\,\text{kHz}$, an OSR of 19.2 is provided. The quantization level is 33 to avoid the complexity in the DEM, digital control circuitry, and wiring [1]. Fig. 10 (a) shows the achieved SQNR versus different out-of-band gains (OBGs) and orders, and Fig. 10 (b) shows the same plot when a 10ps RMS jitter is added. To be comparable with [2], where a 135dB primary noise shaping SQNR and a 126.8dB SQNR with 10ps RMS jitter are achieved, the order of the DSM is picked as 6. Fig. 11 shows the MSA versus OBG with this 6th-order DSM (without jitter). To reach an MSA of 0.43dBFS (95% of full scale), an OBG of 2.8 is required. The red marker in Fig. 10 and Fig. 11 shows the design point (6th-order, 33-level DSM with OBG = 2.8). The achieved SQNR with and without jitter are 128.9dB and 130.9dB respectively. This also ensures the DSM design is not the most dominant factor in distortion and noise by leaving some margin for the THD+N goal of -110dB, and the DR goal of 126dB.

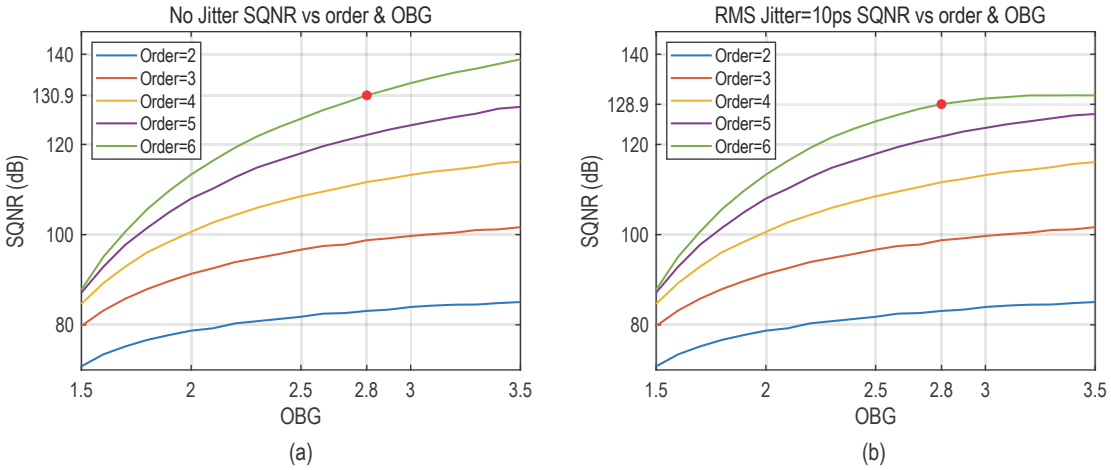

Fig. 10. SQNR versus OBG for a 33-level DSM with an OSR of 19.2: (a) No jitter (b) With 10ps RMS jitter

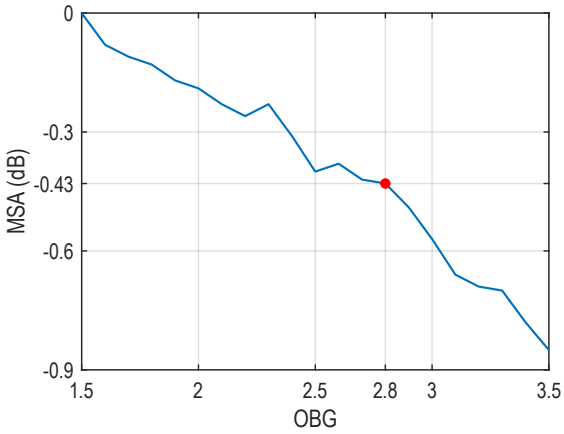

Fig. 11. Maximum stable amplitude versus OBG for a 6th-order 33-level DSM with an OSR of 19.2

2.2.2 Current-steering DAC

2.2.2.1 IDAC topology

There are 3 common topologies of IDACs: bi-level DAC, complementary DAC, and tri-level DAC [3]. Fig. 12 shows 2-bit equivalent circuitries for each topology. The Bi-level DAC is implemented with 4 sink current sources (CSs) and 2 constant offset CSs. By enabling the switch connection to V_{XP} or V_{XN}, each DAC unit, can change its current output value to $\pm I_D$. The complementary DAC removed the 2 constant offset CSs by changing them to a source CS for each DAC unit and doubling the number of switches. The tri-level DAC added an additional dump state, which allows the current output of each slice to be not only $\pm I_D$, but also 0 when the dump state is enabled.

The noise contribution of the CSs in different DAC topologies sets the fundamental limit for SNR. Since in bi-level DAC, the 2 offset CSs are always connected to the output, its current noise is the largest. Complementary DAC has fewer CSs and less current flowing to the output, so its noise performance is better than Bi-level DAC. For tri-level DAC, the noise contributed by CSs depends on the number of slices that use the dump state. This leads to a signal-dependent

noise, where the closer the input code is to 0, the less CS current noise is connected to the output. This gives tri-level DAC a noise advantage when the input signal swing is small, which is especially beneficial for DR.

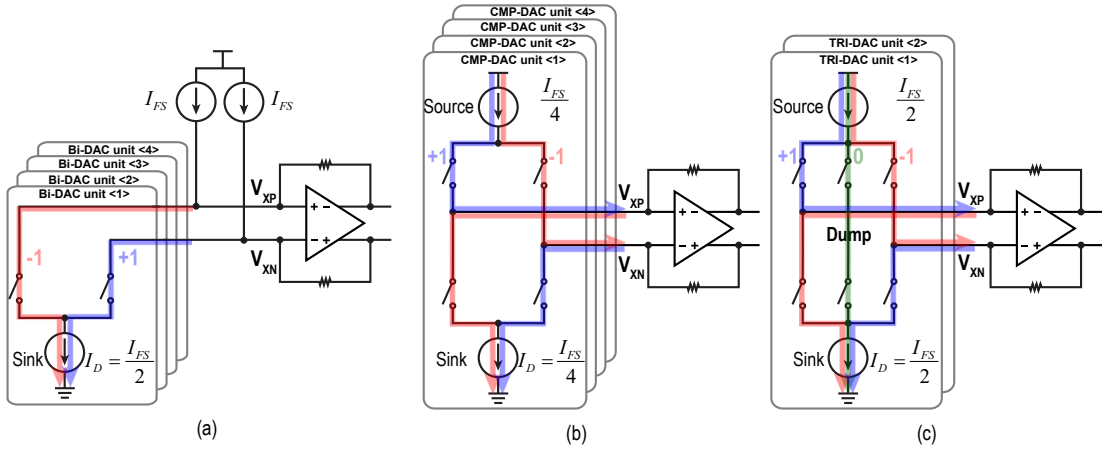

Fig. 12. IDAC topologies: (a) Bi-level (b) Complementary (c) Tri-level

Table 1 summarizes the comparison between N-bit equivalent circuitries for the 3 aforementioned topologies. With the largest number of switches, tri-level DAC needs complex digital control circuitry. However, tri-level DAC has the smallest total current, number of CSs, and the best DR performance. Therefore, in this project, the tri-level DAC structure is selected.

Table 1. N-bit equivalent circuitry comparison for 3 common topologies of IDACs

	Bi-level DAC	Complementary DAC	Tri-level DAC
Total current of DAC units	$2I_{FS}$	I_{FS}	I_{FS}
CS number in DAC units	$2+2^N$	2^{N+1}	2^N
Switch number in DAC units	2^{N+1}	2^{N+2}	3×2^N
Noise from DAC units at zero input	All DAC units	All DAC units	Near zero

2.2.2.2 IDAC unit specification

IDAC, together with a fully differential transimpedance amplifier (TIA), which is a CDA in this work, turns the digital code into a voltage signal, as shown in Fig. 13. To realize the 33 levels, 16 tri-level DAC units with unit current value $I_D = 1/16\, I_{FS}$ are needed. Due to the DEM in 2.2.3, 4 more dummy DAC units with the same I_D are added. The common mode voltage (V_{CM}) of the TIA virtual ground is defined by the output stage, which is 7.2V. The IDAC is implemented with the same supply voltage V_{DD} of 14.4V and its current output nodes are directly connected to 7.2V. Although the DAC can also be implemented in lower voltage domain with pull-down resistors [2], the noise performance may be degraded.

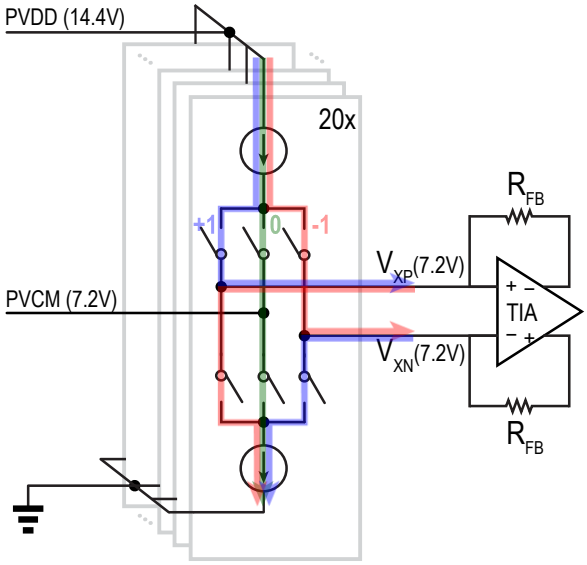

Fig. 13. Illustration of DAC and TIA

The full-scale current of the IDAC should satisfy the following relationship with the feedback resistor R_{FB} in the TIA:

$$I_{FS} \cdot R_{FB} + V_{CM} = V_{DD}$$

In order to determine I_{FS}, R_{FB} needs to be first obtained based on the DR requirement. DR is the ratio of full-scale input signal power $P_{sig,FS}$ and the noise floor P_{noise}. $P_{sig,FS}$ is assumed to be a sine wave with a peak-to-peak swing of 14.4V, and P_{noise} is the voltage noise density V_n times the audio bandwidth $f_b = 20kHz$. This results in the DR calculation:

$$DR = 10 \cdot \log_{10}\left(\frac{P_{sig,FS}}{P_{noise}}\right) = 10 \cdot \log_{10}\left(\frac{0.5 \times (14.4V)^2}{V_n^2 \cdot f_b}\right)$$

V_n contains noise from biasing, DAC units, the op-amps of TIA, and the 2 R_{FB} (for differential output), where the biasing noise can be filtered, and DAC unit noise at near-zero input is ignorable. By an assumption of op-amp noise being typically 4x lower than the noise contribution of the 2 R_{FB}, the voltage noise density can be estimated as:

$$V_n^2 \approx R_{FB}^2\left(I_{n,OPAMP}^2 + I_{n,RFB}^2\right) = R_{FB}^2\left(\frac{1}{4}+1\right)\left(2 \times \frac{4kT}{R_{FB}}\right)$$

Fig. 14 (a) and (b) shows the I_{FS} versus DR plot, and the I_{FS} versus R_{FB} plot, respectively. In order to reach the DR goal of 126dB, $I_{FS} = 240\mu A$ and $R_{FB} = 30k\Omega$ are picked in the design, shown as red markers in both plots. For each DAC unit, $I_D = 1/16\, I_{FS} = 15\mu A$.

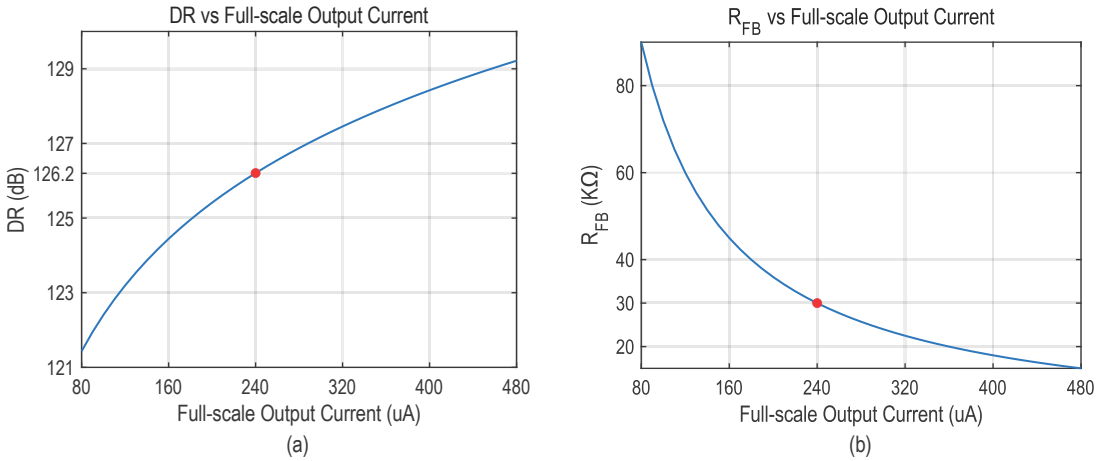

Fig. 14. (a) Full-scale current vs DR plot (b) Full-scale current vs feedback resistor plot

2.2.3 DEM

The RT DEM [4] is a promising solution to ISI since it ensures approximately the same number of $0 \rightarrow 1$ transitions for each data sample in 2-level DACs. However, it suffers from severe ISI distortion when it is applied to tri-level DAC units. Fig. 15 (a) is an illustration of the RT DEM. When the input data is positive, the DAC unit output current is either 0 or +1 LSB, suggesting only $0 \rightarrow +1$ or $+1 \rightarrow 0$ transitions. Vice versa, when the data is negative, the DAC unit output current is either 0 or -1 LSB, suggesting only $0 \rightarrow$-1 or $-1 \rightarrow 0$ transitions. Since there exist ISI differences between "+1" and "-1", this data polarity-dependent transition nature creates distortion. (Simulation results are shown in 3.1.5.)

To solve this issue, the dummy one-directional RT DEM is developed, where the dummy DAC units force each type of transition ($0 \rightarrow +1$, $+1 \rightarrow 0$, $0 \rightarrow$-1, $-1 \rightarrow 0$) to occur regardless of input data polarity. To maintain the same signal output, the same number of "+1" and "-1" are needed for the dummy pattern. To avoid introducing new transition types ($+1 \rightarrow$-1, $-1 \rightarrow$ +1) which have larger ISI and may lead to other types of signal-dependent transitions, "0" is needed to separate "+1" and "-1". Thus, a dummy pattern of (+1, 0, -1, 0) is added at the end of each input data $\geqslant 0$, and (0, +1, 0, -1) at the beginning of each input data <0, as shown in Fig. 15 (b). The dummy pattern, together with the original thermometer code, rotates through all DAC units without changing the total DAC output current. To realize 33 output levels, 16 tri-level DAC units are needed. Upon adding the dummy pattern, 20 DAC units in total are implemented, with their input codes rotating at $20 f_s$ (15.36MHz). Although the DAC can also be implemented with more than 4 dummy units, adding more of them means more divisions in one sample period, and thus even higher frequency clock. Also, since the dummy pattern always enables "+1" and "-1" LSB current connected to the TIA even with input data =0, the DAC output noise is slightly increased, but it turned out to be 5.5x less compared to the thermal noise of the CDA.

Moreover, instead of using a fixed direction of code rotation, a bidirectional RT DEM is employed, where the rotation direction is reversed for every other data sample, as shown in Fig.

15 (c). This bidirectional nature can be seen as producing double-sided PWM signals driving each DAC unit, which has lower PCM-to-PWM distortion compared to the single-sided PWM signals produced by the conventional RT DEM [4]. It should be pointed out that the proposed dummy bidirectional RT DEM effectively reduces the RT DEM's PWM frequency by 2x, resulting in some quantization noise folding. However, this only leads to an insignificant increase in the quantization noise floor and hardly affects the thermal noise limited DR. Therefore, the dummy bidirectional RT DEM is implemented in the proposed architecture.

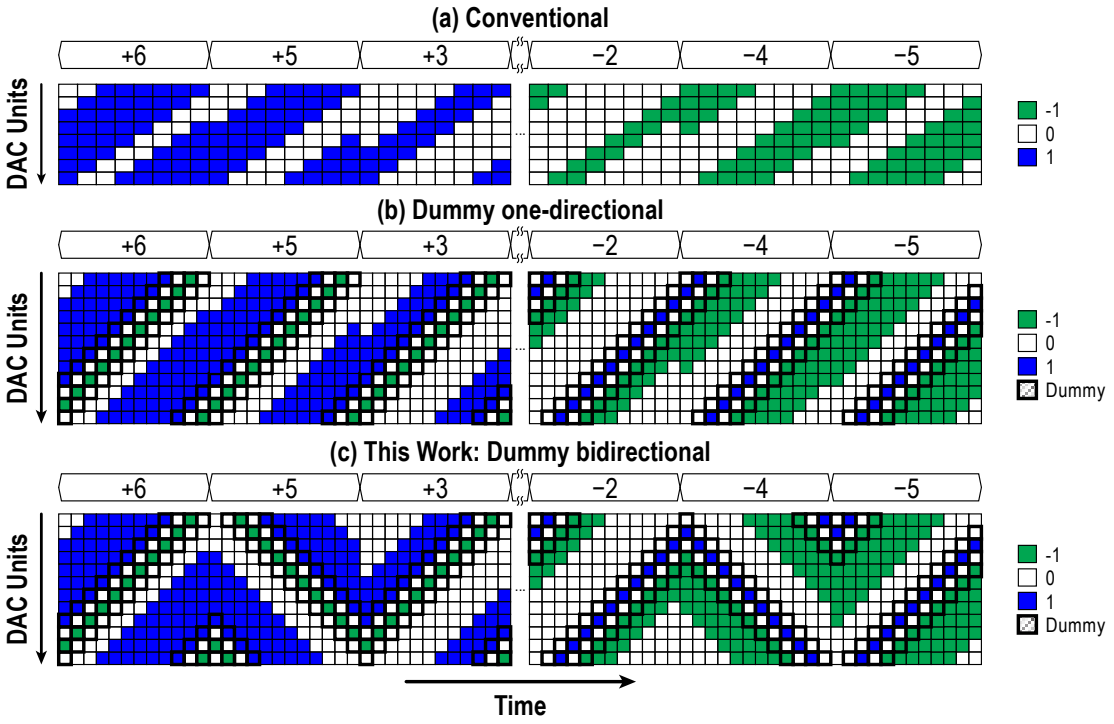

Fig. 15. Illustrations of (a) conventional RTDEM (b) dummy one-directional RTDEM (c) dummy bidirectional RTDEM applied to IDAC with tri-level units

2.3 Class D amplifier architecture

2.3.1 Output stage

The output stage of the proposed architecture is reused from the work of [5]. When used in the 3-level mode, this output stage can drive 14W into an 8-Ω load, with a peak efficiency of 91% and only draws 7 mA quiescent current during idle operation [5].

2.3.2 Loop filter

In order to meet the THD+N requirement of less than -110dB, a ≥ 70 dB in-band loop gain is needed for the suppression of the output stage distortion. The PWM frequency is $f_{PWM} = 4.608MHz$. For stability, the unity gain frequency of the loop filter f_{UG} should satisfy $f_{UG} \leq f_{PWM}/\pi = 1.47MHz$ [6]. In order to reach a 70dB in-band loop gain while keeping the f_{UG} within the stable range, a 3rd-order loop filter is needed.

Fig. 16 shows the 3 common topologies of a 3rd-order loop filter: CIFB, CIFF, and CIFF-

B structures (cascade of integrators with feedback or feedforward or feedforward-feedback structure) [7].

CIFB structure is shown in Fig. 16 (a). The outputs of 1st and 2nd integrators contain large input components to nullify the audio-band component injected by the output stage feedback [7]. This problem could be solved by adding input feed-ins to the input of the integrators, but this needs 3 DACs to realize, which leads to more system complexity and area consumption.

In the CIFF structure, as shown in Fig. 16 (b), the outputs of 1st and 2nd integrators do not contain the input component, which results in reduced output swings compared with the CIFB counterpart [7]. However, the summation structure of the integrator outputs also suggests extra circuitry for the summing node.

CIFF-B structure, as shown in Fig. 16 (c), combines the benefits of the CIFF and CIFB loops. Compared to CIFF, the summation of integrator outputs in the CIFF-B structure can be easily implemented with resistors feeding currents into the same virtual ground. Due to the feed-forward path, the low-frequency swing at 1st integrator output is smaller than in the CIFB structure, which leads to reduced distortion and noise from the rest of the loop filter when referred to the input [7]. Therefore, CIFF-B topology is used in the proposed architecture.

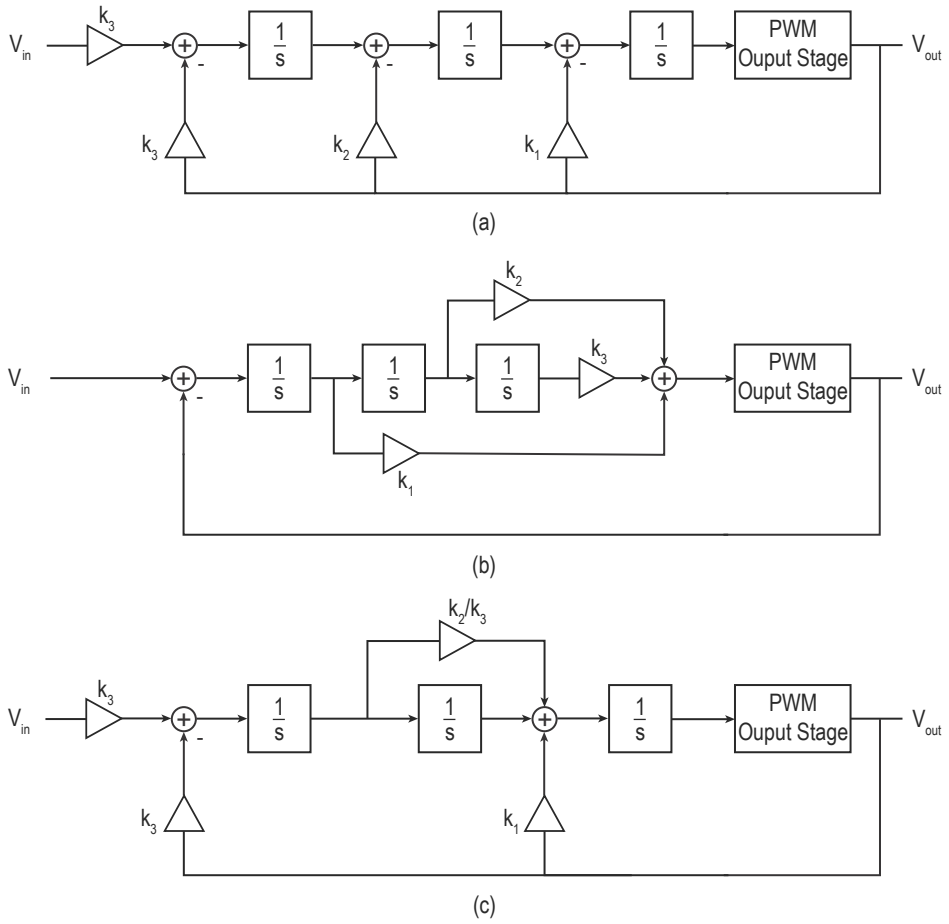

Fig. 16. Loop filter topologies: (a) CIFB (b) CIFF (c) CIFF-B

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Chapter 3 Circuit Design

3.1 Current-steering DAC

3.1.1 IDAC unit design

The IDAC unit circuitry is shown in Fig. 17. The unit circuitry consists of source current source (CS) (M_{Pcas}, M_{Pmain}, R_{PD}), sink CS (M_{Ncas}, M_{Nmain}, R_{ND}), and switches (M_{S1}~M_{S6}).

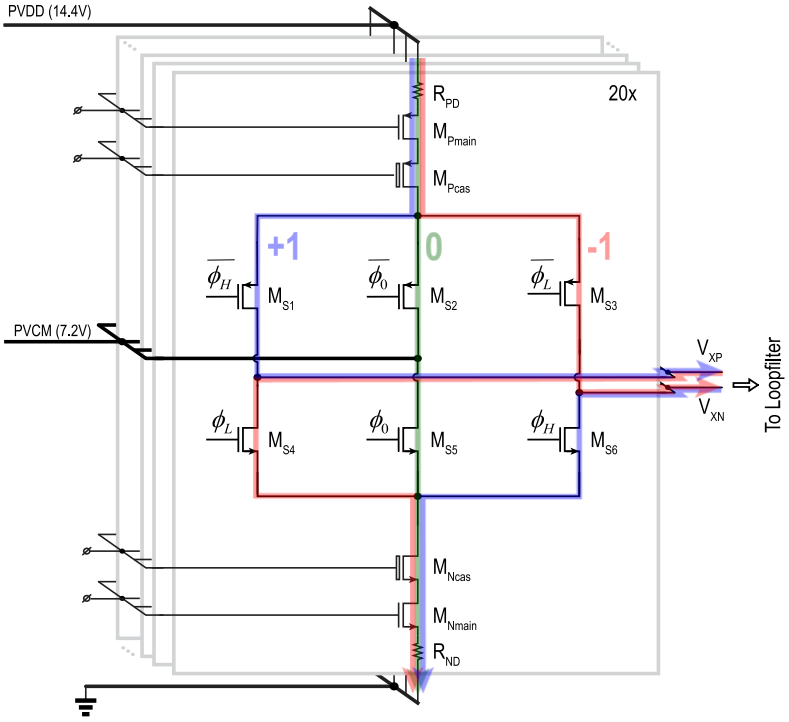

Fig. 17. IDAC unit circuit

The current switches M_{S1}~M_{S6} are implemented with minimum size 2V MOSFETs to ensure fast switching for low ISI, and minimize their charge injections. Since the drains of these switches are connected to the virtual ground of the TIA, which is 7.2V, the gate of M_{S1}~M_{S6} cannot be directly controlled by digital control signals that work in the 1.8V domain. The gate control signals (ϕ_L, ϕ_0, ϕ_H for the sink CS, and $\overline{\phi_L}$, $\overline{\phi_0}$, $\overline{\phi_H}$ for the source CS) are therefore generated by level-shifting the digital control signal to a floating voltage domain, which will be further discussed in 3.1.2.

The source and the sink CSs consist of main transistors M_{Pmain} and M_{Nmain}, cascode transistors M_{Pcas} and M_{Ncas}, and source degeneration resistors R_{ND} and R_{PD}, respectively. The main transistors are implemented with 2V MOSFETs since 2V MOSFETs exhibit less flicker noise compared to other MOSFET counterparts. The cascode transistors boost the output impedance of the CSs and shield the main transistors for less drain voltage variation, while hardly increasing the output current noise. The cascode transistors are

implemented with 5V MOSFETs for safe operation since the total headroom for sink or source CS is 7.2V. While higher voltage MOSFETs can also be used, they suffer from higher flicker noise and occupy a larger area.

Source degeneration is used for better noise performance. If the CSs are implemented with only cascode and main transistors, the current noise is dominated by the main transistors. In this case, the main transistors are usually biased in the strong inversion saturation region, presenting a current noise density of:

$$i_n^2 = 4kT\gamma g_m = 4kT\gamma I_D \cdot \frac{2}{(V_{GS} - V_{TH})} \geq 4kT\gamma I_D$$

Since the main transistors are 2V MOSFET, $V_{GS} - V_{TH}$ cannot exceed 2V. Therefore, the current noise density is always larger than $4kT\gamma I_D$. With source degeneration, however, the current noise can be estimated by the noise of the degeneration resistor R_D:

$$i_n^2 = \frac{4kT\gamma}{R_D} = 4kT\gamma I_D \cdot \frac{1}{V_{RD}}$$

Here, the V_{RD} denotes the voltage headroom across the degeneration resistor. Since V_{RD} can be designed to be larger than 1V, the current noise density can be smaller. To maximize V_{RD}, the transistors are biased in weak inversion saturation for low headroom consumption.

The mismatch between CSs can also be reduced by source degeneration. For transistors biased in weak inversion with source degeneration, the drain current satisfies:

$$I_D = I_{D0} \cdot e^{\frac{V_{GS} - V_{TH}}{nU_T}} = I_{D0} \cdot e^{\frac{V_G - I_D R_D - V_{TH}}{nU_T}}$$

Since I_{D0} has a minor effect on mismatch [1], the mismatch can be derived as:

$$\left(\frac{\sigma_{\Delta I_D}}{I_D}\right)^2 \approx \left(\frac{1}{I_D} \cdot \frac{\partial I_D}{\partial R_D}\right)^2 \sigma_{\Delta R_D}^2 + \left(\frac{1}{I_D} \cdot \frac{\partial I_D}{\partial V_{TH}}\right)^2 \sigma_{\Delta V_{TH}}^2$$
$$= \left(\frac{I_D}{nU_T + I_D R_D}\right)^2 \sigma_{\Delta R_D}^2 + \left(\frac{1}{nU_T + I_D R_D}\right)^2 \sigma_{\Delta V_{TH}}^2$$

Since nU_T is in the order of $10^{-2}V$, its contribution in the denominatior can be ignored. This leads to a mismatch of:

$$\left(\frac{\sigma_{\Delta I_D}}{I_D}\right)^2 \approx \left(\frac{1}{R_D}\right)^2 \sigma_{\Delta R_D}^2 + \left(\frac{1}{I_D R_D}\right)^2 \sigma_{\Delta V_{TH}}^2 = \left(\frac{1}{R_D}\right)^2 \left(\frac{R_D}{\sqrt{WL}} A_R\right)^2 + \left(\frac{1}{V_{RD}}\right)^2 \left(\frac{1}{\sqrt{WL}} A_{VT}\right)^2$$

Here, the A_R and A_{VT} denote the mismatch coefficients of resistor and threshold voltage, respectively. With a large V_{RD}, the mismatch contribution from the transistor threshold voltage can also be reduced.

A large V_{RD} is preferred for both smaller noise and smaller mismatch. However, a trade-off exists between the available V_{RD} and the PVDD supply voltage range. In automotive applications, the battery voltage supply may vary due to charging and discharging. Although smaller noise and mismatch can be achieved with larger V_{RD}, the available supply range will shrink due to the larger headroom requirement. The headroom on R_{ND} (or R_{PD}) is designed to be 4V, to keep the transistors in saturation region safely when the supply varies from 10V to 20V. (It has to be pointed out that due to time constraints, the other circuitries are not designed for the supply variation, but the design of the IDAC unit was fixed.)

Since the unit DAC current I_D is $15\mu A$, R_{ND} (or R_{PD}) is $266.8k\Omega$. The main transistor lengths are $1\mu m$ and 400nm for NMOS and PMOS respectively, and all of their widths are $48\mu m$ to bias them in weak inversion saturation and ensure noise performance. For minimizing chip area, the cascode transistors are minimum length 5V NMOS and PMOS. Their widths, also $48\mu m$, can ensure weak inversion saturation biasing and layout easiness.

3.1.2 Level shifter design

Fig. 18 is an illustration of the digital input, level shifters, and DAC units. The digital input signal D_{IN} first pass through the DEM, to generate 120 control signals for all the switches in the 20 DAC units. This signal is then retimed by D-flip-flop (DFF) to align their timing. To avoid a discharge of the cascode transistors' drain nodes, the current switch transistors (M_{S1}~M_{S6}) should never be simultaneously off, which is ensured by the DAC drivers. The overlapping DAC drivers provide 1.8V control signals for each switch and the level shifters are required to move the 1.8V digital control input to a floating voltage domain near PVCM (7.2V) for safe operation.

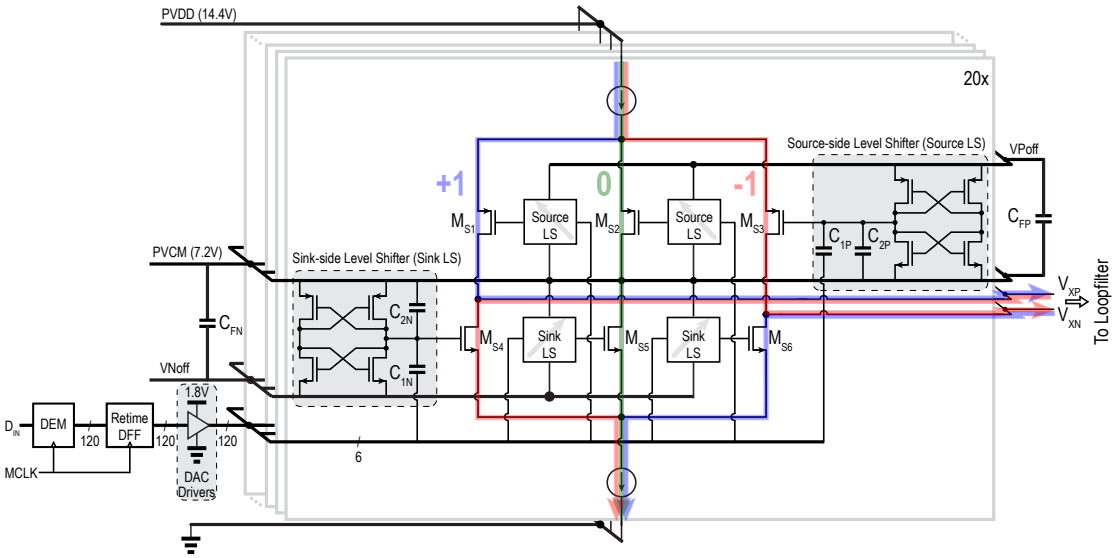

Fig. 18. Level shifters with DAC units

For each DAC unit, there are 3 PMOS switches for source CS and 3 NMOS switches for sink CS, controlled by 3 source-side level shifters and 3 sink-side level shifters, respectively.

To control the switches, the level shifters need to provide 2 voltage output levels for turning on and off the switches. The "on voltage" is provided by PVCM, which means no additional voltage supply is required for turning the switches on, and since the switches work as additional cascode transistors, they further boost the output impedance of the CSs. The "off voltages" for the source and sink sides need to be generated separately. To avoid increasing the static power consumption, the "off voltages" (VNoff, VPoff) are provided by capacitors C_{FP} and C_{FN}, which are shared between all the DAC units. They are implemented by MIM capacitors on top of the DAC switches, thus consuming no extra chip area. The 1.8V DAC driver signal is attenuated to the 1.2V range using a capacitive divider with $C_{1P/N} : C_{2P/N} = 2:1$. The DAC drivers, $C_{1P/N}$, and the latches also function as charge pumps, establishing the voltage across $C_{FP/N}$. Thanks to dummy bidirectional RT DEM, at least 1 DAC unit switches during one DEM clock period. Thus, the charge in C_{FP} and C_{FN} are constantly refreshed.

If the 1.8V driver signal is directly shifted to the 7.2V domain without a voltage divider, the level shifter transistor may experience overvoltage during power-up. Fig. 19 (a) shows the 1.8V range level shifter in one DAC unit on the sink side. Fig. 19 (b) shows an example of the voltage waveforms of the gate control voltage ϕ_H and the node VNoff. Due to the power-up procedure in 3.3.2, before the switches start toggling, VNoff is 7.2V, D_H is 0V and ϕ_H is 7.2V. When the switches start toggling, VNoff slowly settles to the wanted "off voltage" with a staircase pattern when the switches in 20 DAC units toggle in turn, since C_{FN} can only receive charges when the switches toggle. However, due to the RT DEM scheme, there exists a possibility that a switch, for instance M_{S6}, may have never toggled while VNoff has already decreased to a value that can cause overvoltage. As shown in the example in Fig. 19 (b), when VNoff is 6.4V, ϕ_H experiences the first toggle. Since ϕ_H and D_H have always remained 7.2V and 0V before the first toggle, C_{1N} holds 7.2V. When D_H turns to 1.8V, ϕ_H sees a spike to 8.67V, making M_{L4} experience a V_{DS} overvoltage. Thus, for safe operation, a capacitor divider is added to attenuate the 1.8V driver signal.

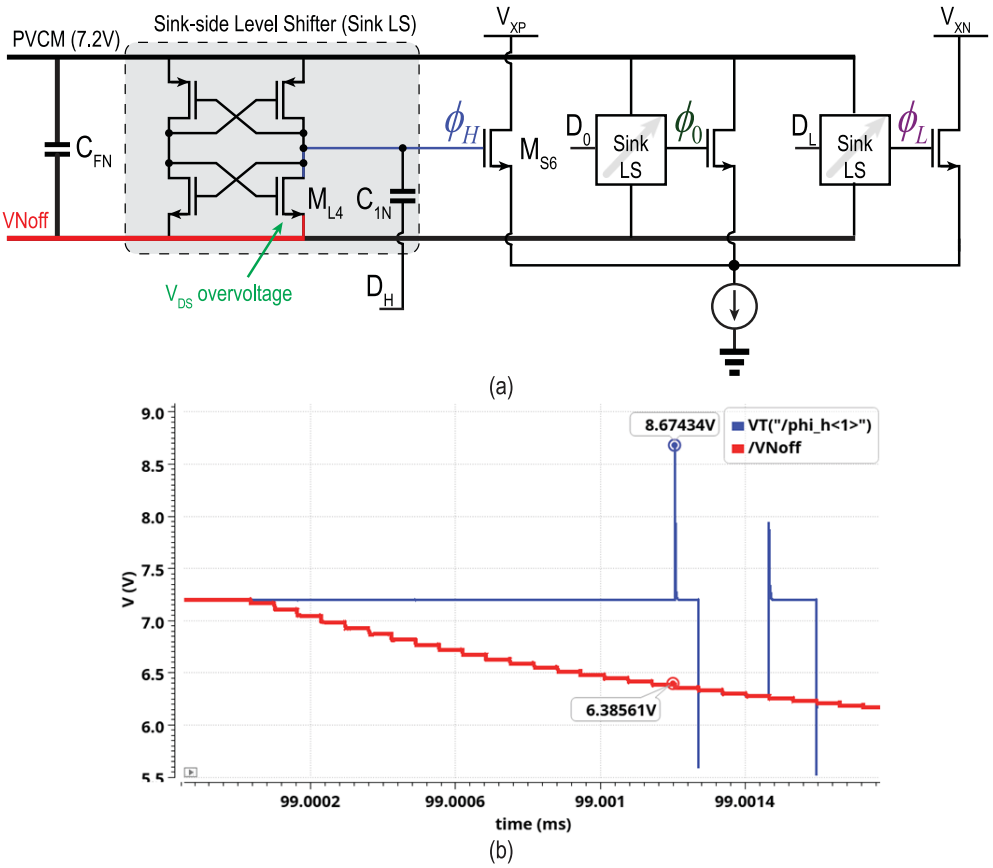

Fig. 19. Level shifter on sink side (a) 1.8V range level shifter (b) an example of the 1.8V range level shifter waveforms

If the 1.8V driver signal is attenuated even more, for instance, to the 0.9V range with $C_{1P/N}:C_{2P/N}=1:1$, the switches can still conduct current when they are supposed to be off. This signal-dependent current leakage is especially troublesome when the threshold voltage of the transistors becomes smaller due to high temperature or corner. Fig. 20 (a) and Fig. 21 (a) show the worst-case scenario of the sink-side switch drain current leakage at the fast corner, 125℃. Fig. 20 (a) shows that when the switches are off, the source and gate voltages of the switches are 6.6V and 6.4V. This makes the "off" switches conduct a current leakage of 81.9pA, as shown in Fig. 21 (a). With this leaky current, the 0.9V range level shifter, together with the DAC and an ideal TIA, produces an SNDR of 105.6dB in the fast corner at 125℃, when the input signal is 1kHz -1dBFS. When the 1.2V range level shifter is applied, as shown in Fig. 20 (b) and Fig. 21 (b), the current leakage is reduced to 1.3pA, and an SNDR of 124.3dB is achieved with the same simulation condition. It has to be pointed out that with $C_{1P/N}:C_{2P/N}=2:1$, the "1.2V range level shifter" outputs are not exactly $1.2V_{PP}$ because of the parasitic capacitances of the level shifters and the keep-alive circuitry. While other attenuation ratios may also work for this application, the 1.2V range level shifter can already enable a safe operation, a good SNDR performance, as well as an easy matching between $C_{1P/N}$ and $C_{2P/N}$.

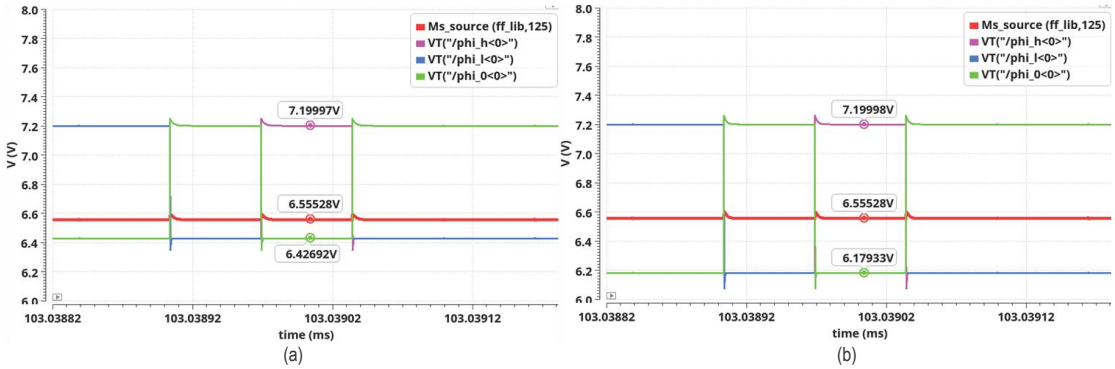

Fig. 20. Level shifter outputs (the switch gate voltage waveforms) and the switch source voltage waveforms for the sink side at the fast corner, 125℃: (a) 0.9V range level shifter (b) 1.2V range level shifter

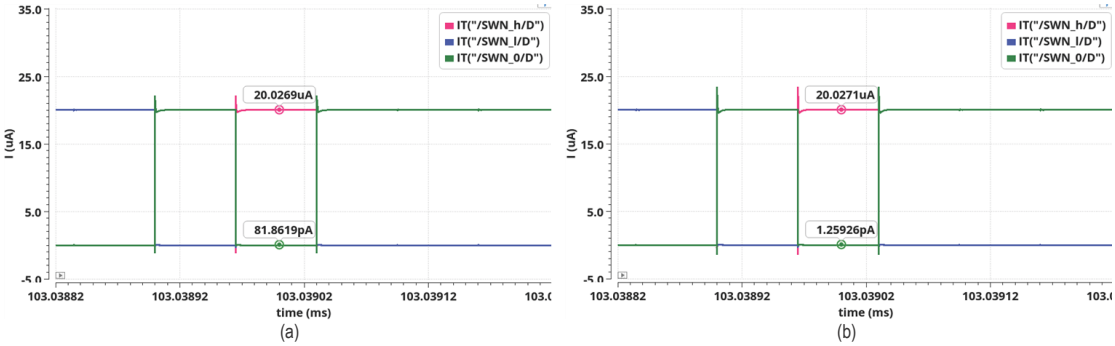

Fig. 21. Drain current waveforms of sink side switches at fast corner, 125℃: (a) 0.9V range level shifter (b) 1.2V range level shifter

The nominal DAC driver output waveforms are shown in Fig. 22 (top). The crossing point is shifted towards PVCM to ensure overlapped switch control [2]. The nominal level shifter output waveforms are shown in Fig. 22 (bottom). It can be seen that the 1.8V domain signal is shifted to the floating domain, while the overlapping nature of the switch is maintained.

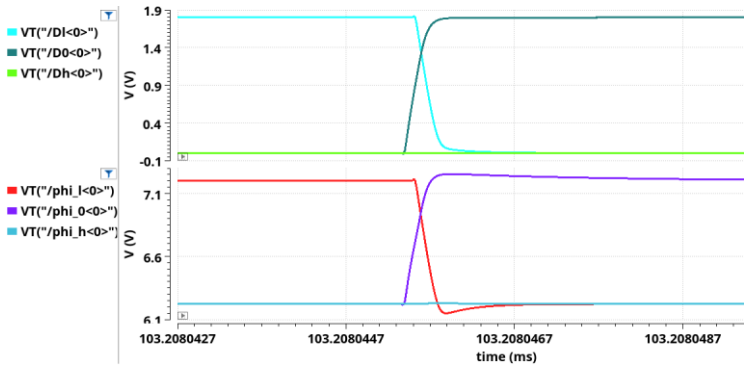

Fig. 22. Top: DAC driver outputs, Bottom: Level shifter outputs

3.1.3 IDAC biasing design

The biasing design is shown in Fig. 23. The reference current is generated by a 4V voltage reference (VREF) and the degeneration resistor R_D. VREF is supplied from an off-chip low-noise LDO chip and buffered by a unity gain buffer. This buffer also provides the bulk voltages for the 5V and 2V transistors of sink CSs. Although their bulks can be connected to their own

sources, this will cause large area consumption because of the separate isolation rings. By connecting to the same 4V bulk supply, the isolation rings for all the sink side transistors can be shared, approximately saving an area of $0.047mm^2$ compared to the former method. The buffer is a 5-transistor OTA powered by a 5V supply, and its output is connected to the gate of a depletion mode 5V transistor M_1 since the V_{GS} is -0.32V during nominal operation. All the other 2V and 5V transistors, and the degeneration resistors $R_{BD1} \sim R_{BD9}$ are of the same size as their counterparts in the DAC units and the current in M_1 is then mirrored 1:1 to all the biasing branches and the DAC units. $R_{T1} \sim R_{T2}$ are $16.1k\Omega$ resistors for biasing and 2 noise filters are applied for noise requirements. In order to avoid overvoltage, $M_2 \sim M_7$ are implemented with 20V transistors.

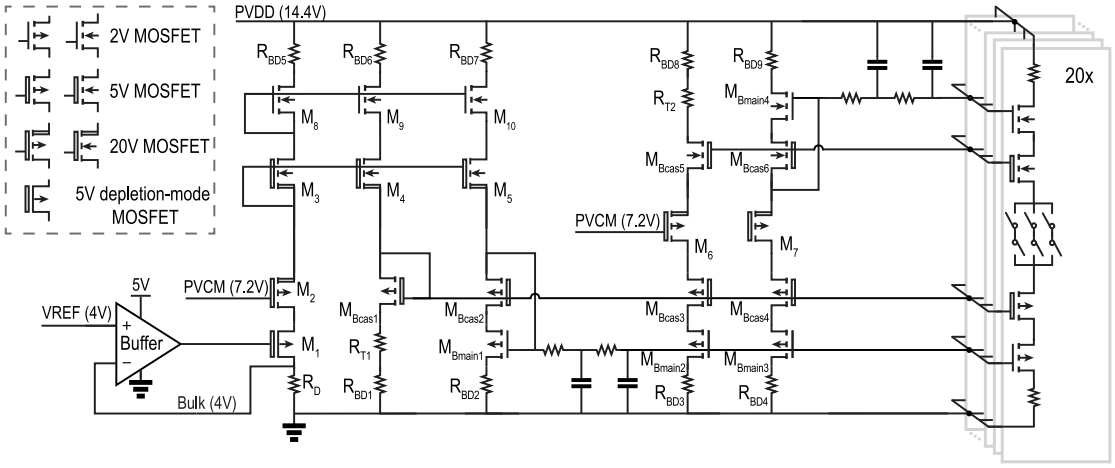

Fig. 23. IDAC biasing design

3.1.4 Noise filter

If the biasing circuit is directly connected to the DAC units, the achieved SNR at -1dBFS input is 106.0dB. Thus, a filter is added to decrease the in-band noise. Fig. 24 (a) shows the noise filter illustration. The biasing of the main transistor is filtered with a lowpass noise filter, while a noise filter is not needed for the cascode transistor biasing since the voltage noise at their gate nodes has a minor influence on the output noise. The biasing current is modeled by a current source without considering other biasing branches and the buffer due to design order and time constraints. I_1 is a current-controlled current source (CCCS) that models the biasing current by 1:1 copying the current generated by a 4V reference V_{ref} and R_D.

The noise filter has 3 important specifications: cutoff frequency, noise, and area consumption. With ideal current biasing, a 1st-order RC filter ($R = 44.2M\Omega, C = 180pF$) can achieve an SNR of 119.3dB at -1dBFS, consuming a noise filter area of $0.108mm^2$ (1 resistor and 1 capacitor area only). For the goal of a smaller area and similar noise performance, the 2nd-order filter topology is studied since it may offer higher in-band noise suppression. Since there are 4 degrees of freedom (2 resistors and 2 capacitors) in a 2nd-order filter, and the effect of A-weighting also needs to be considered, tweaking these resistors and capacitors is tricky.

To quickly determine the optimal 4-value solution set of resistance and capacitances, noise estimation is conducted and fed into the Matlab optimization tool "fmincon". "fmincon" starts with an initial guess of the 4-value solution set, then iterates and converges to a minimum noise solution with the constraint of a cutoff frequency $\leq 20Hz$, and an area budget of $0.05mm^2$.

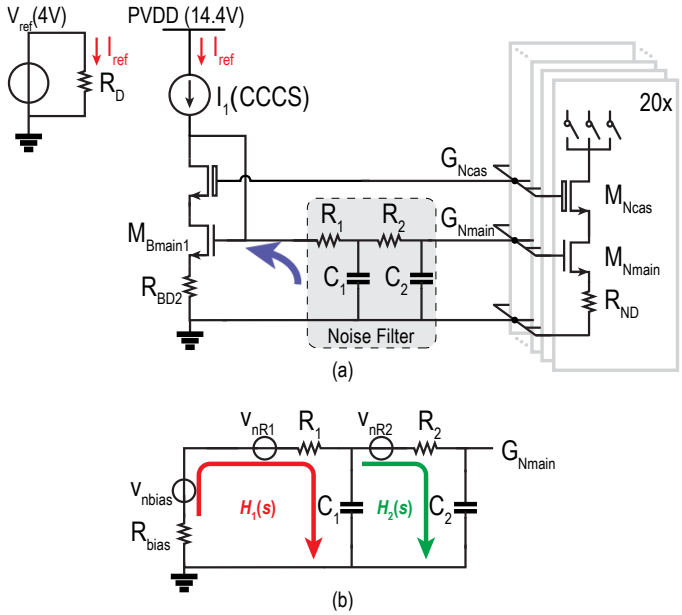

Fig. 24. Noise filter on sink-side (a) illustration (b) noise estimation model

Fig. 24 (b) shows the simplified noise model for the noise at G_{Nmain} node. Seeing into the gate of the main biasing transistor M_{Bmain1}, the circuitry on the left can be modeled as a Thevenin equivalent of a resistor R_{bias} approximately equal to R_{BD2} $(=R_D)$ and a noise source v_{nbias}^2. Since the current source I_1 copies the current generated by 4V reference and R_D, v_{nbias}^2 can be estimated as:

$$v_{nbias}^2 = \frac{4kTR_{BD2}^{\ 2}}{R_D} + 4kTR_{BD2} = 8kTR_D$$

The resistors R_1 and R_2 also contribute to noise, which are:

$$v_{nR1}^2 = 4kTR_1, \quad v_{nR2}^2 = 4kTR_2$$

v_{nbias}^2 and v_{nR1}^2 pass through the transfer function $H_1(s)$:

$$H_1(s) = \frac{1}{(R_1+R_D)R_2C_1C_2 \cdot s^2 + ((R_1+R_D)C_1 + (R_1+R_D)C_2 + R_2C_2) \cdot s + 1}$$

v_{nR2}^2 pass through transfer function $H_2(s)$:

$$H_2(s) = \frac{1}{(\frac{1}{C_1 \cdot s + \frac{1}{R_1+R_D}} + R_2)C_2 \cdot s + 1}$$

With the A-weighting transfer function being $H_{A-weight}(s)$, the total a-weighted noise at the node G_{Nmain} can then be estimated as:

$$v_{ntotal,A-weighted}^2 = \left[\left(v_{nbias}^2 + v_{nR1}^2\right)\cdot\left|H_1(s)\right|^2 + v_{nR2}^2\cdot\left|H_2(s)\right|^2\right]\cdot\left|H_{A-weight}(s)\right|^2$$

Since the same noise model can be applied to the source side, the noise filters are the same for both sides. After 100 attempts of searching, the design solution is found as $R_1 = 28.53M\Omega$, $R_2 = 99.37M\Omega$, $C_1 = 1.09pF$, $C_2 = 62.11pF$. (In hindsight, a 1st-order noise filter with an equivalent resistor value of $130M\Omega$ and a capacitor of $60pF$ can also meet the area budget with similar noise performance.) Fig. 25 shows the noise versus area estimation plot of 1000 groups of randomly generated 4-value solution sets and the design point is marked as a red dot. With this 2nd-order noise filter, an SNR of 119.1dB at -1dBFS is achieved with a smaller area. Including the isolation rings in the layout, the noise filter on each side (sink or source side) consumes an area of $0.065mm^2$, which in total takes up 1.7% of the die size.

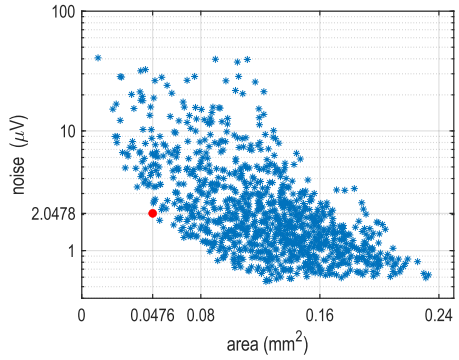

Fig. 25. Sink-side main transistor gate noise vs area estimation

3.1.5 IDAC simulation results

Monte Carlo simulation can be used for testing the influence of mismatch and ISI on the IDAC performance and compare the DEM methods. Since a full FFT analysis in Cadence requires a lot of computation resources and time consumption, a Cadence-Matlab joint Monte Carlo simulation is conducted during the design stage. Instead of simulating a full DAC with 20 DAC units in the Cadence Monte Carlo simulations, it is much quicker to extract a single DAC unit's mismatch and ISI error in its 200 Monte Carlo Cadence simulations and feed them to Matlab to form whole DAC simulations.

The mismatch error e_{mis} of a DAC unit is obtained by the difference between an ideal current $I_{D,ideal}$ and the real current modeled by $I_{dif} = 1/2\left(I_{source} + I_{sink}\right)$, with I_{source} and I_{sink} being source and sink currents. It is then normalized by $I_{D,ideal}$ to get the percentage:

$$e_{mis} = \frac{\left(I_{dif} - I_{D,ideal}\right)}{I_{D,ideal}}\cdot 100\%$$

The ISI error can be modeled as the error area between the ideal pulse waveform and the

real output waveform [3]. For each DAC unit, 4 error areas of 4 types of transitions (0→+1, +1→0, 0→-1, -1→0) are acquired, as shown in Fig. 26.

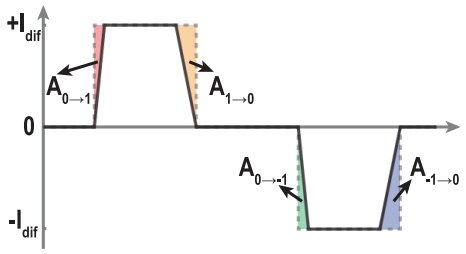

Fig. 26. 4 types of ISI error illustration

These error areas $A_{0\to1}$, $A_{1\to0}$, $A_{0\to-1}$, $A_{-1\to0}$ are then normalized by the DEM clock frequency and I_{dif}, resulting in the ISI errors for each DAC unit:

$$e_{ISI}:\begin{cases} e_{ISI\,0\to1} = A_{0\to1}\cdot f_{DEMCLK}\cdot\dfrac{1}{I_{dif}}\cdot 100\% \\ e_{ISI\,1\to0} = A_{1\to0}\cdot f_{DEMCLK}\cdot\dfrac{1}{I_{dif}}\cdot 100\% \\ e_{ISI\,0\to-1} = A_{0\to-1}\cdot f_{DEMCLK}\cdot\dfrac{1}{I_{dif}}\cdot 100\% \\ e_{ISI\,-1\to0} = A_{-1\to0}\cdot f_{DEMCLK}\cdot\dfrac{1}{I_{dif}}\cdot 100\% \end{cases}$$

With 200 Monte Carlo simulations of a single DAC unit, 200 current output waveforms are obtained. Since with each simulation, the current waveform determines both the DAC unit's mismatch and ISI, the mismatch and ISI data are correlated. Thus, to properly form a whole DAC, 20 groups of correlated mismatch and ISI data are randomly selected from the 200 current output waveform database. 100 Monte Carlo simulations in Matlab are conducted with 100 attempts of these whole DAC forming.

Fig. 27 and Fig. 28 show some typical spectra of the conventional RT DEM and the proposed dummy bidirectional RT DEM in the Monte Carlo simulations. These simulations are done with both mismatch and ISI error, and the input amplitudes are -1dBFS and -60dBFS, respectively. With the proposed scheme, the in-band tones are below -134.4dB and the typical achieved THD+N and DR are -127.92dB and 130.88dB, respectively. Compared with the conventional RT DEM, the proposed scheme shows a typical improvement in THD+N and DR of 18.7dB and 10.0dB, respectively. The proposed scheme also shows smaller harmonic tones in the audio band.

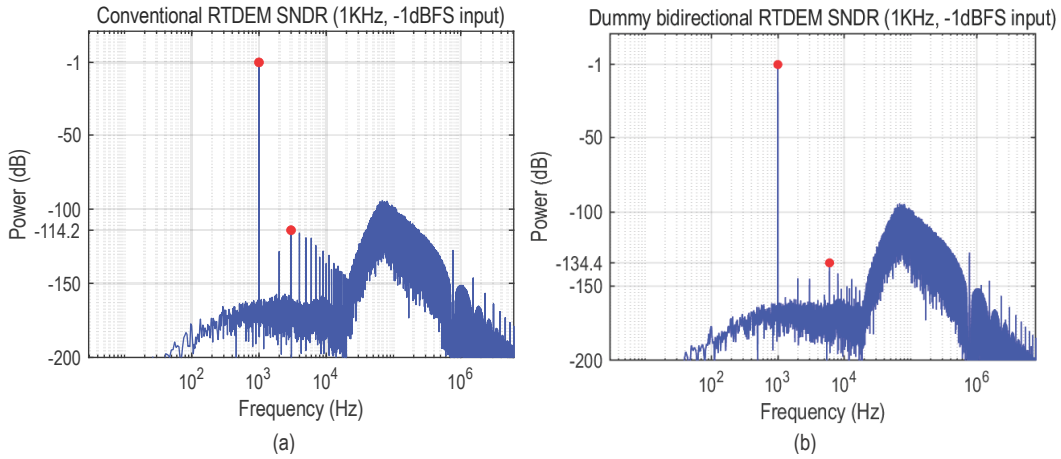

Fig. 27. SNDR at 1kHz, -1dBFS input: (a) conventional RT DEM (b) dummy bidirectional RT DEM

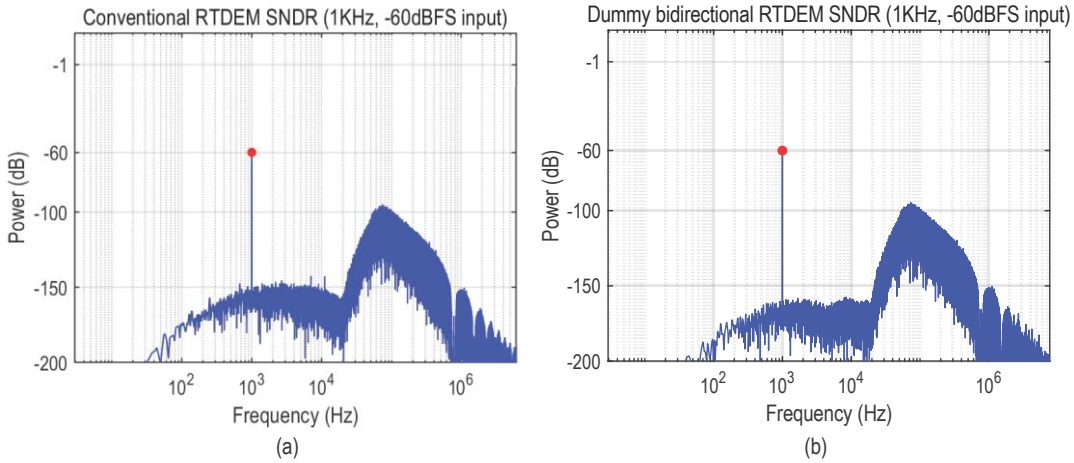

Fig. 28. SNDR at 1kHz, -60dBFS input: (a) conventional RT DEM (b) dummy bidirectional RT DEM

To examine the impact of DEM methods' transition patterns on the SNDR results, FFT analyses are conducted to examine the signal dependency of transitions. Since the signal dependency is better reflected as tones with a large input, an input signal of 1kHz -1dBFS was used. DAC units with certain transitions can be detected and FFT analyses are conducted with the detected units outputting 1LSB. Fig. 29 (a) and (b) show the FFT spectra of $0 \rightarrow -1$ transition patterns of the conventional and the proposed DEM methods. The conventional RT DEM transitions have a stronger signal dependency, which can be reflected on the 3rd harmonic tone of -43.6dB. The proposed scheme, however, shows a 2nd harmonic tone of -85.8dB, which means less signal dependency. Other transition types also exhibit similar results.

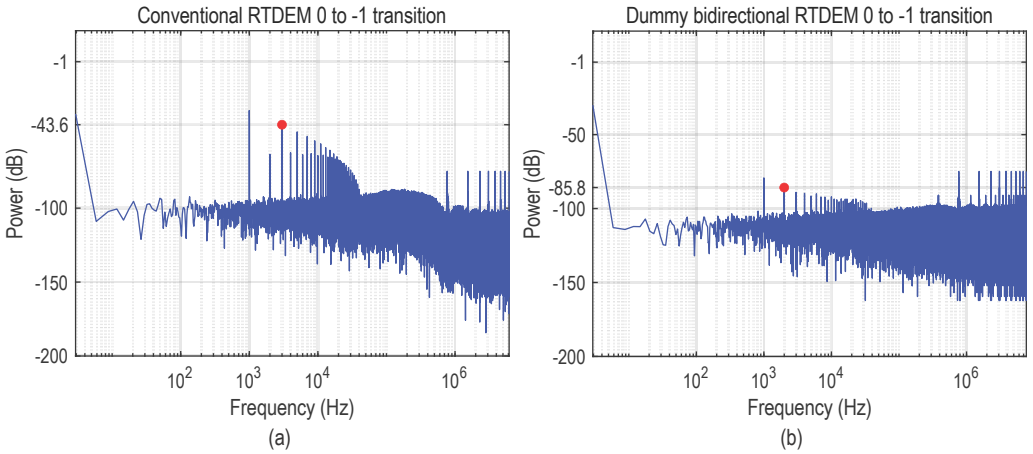

Fig. 29. 0 to -1 transition FFT analysis (a) conventional RT DEM (b) dummy bidirectional RT DEM

The distribution of the 100 Monte Carlo Matlab simulation results is shown in Fig. 30 (a) and (b) for -1dBFS and -60dBFS input at 1kHz, respectively. The proposed scheme has higher SNDR results compared to the conventional RT DEM and the dummy one-directional RT DEM. The dummy one-directional RT DEM method has higher DR compared to the proposed method. As mentioned in 2.2.3, the proposed bidirectional RT DEM can be seen as reducing the RT DEM's PWM frequency by 2x, resulting in some noise folding, which is shown in the typical FFT spectra in Fig. 31. However, this insignificant increase in the noise floor has little effect on the thermal-noise-limited DR. The proposed scheme has an average DR of 130.9dB, which already meets the requirement and stands out with the highest SNDR performance.

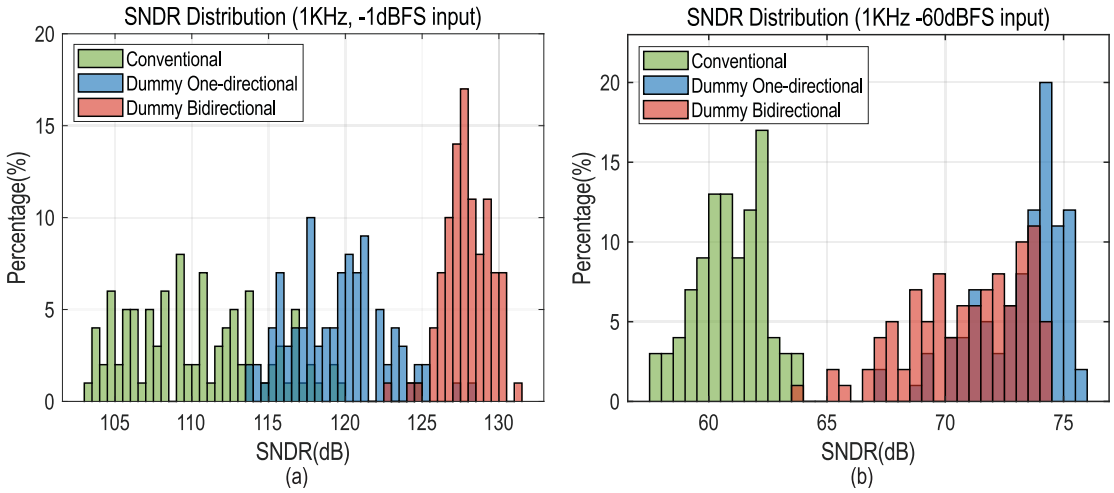

Fig. 30. SNDR distribution of three RT DEM method with: (a) 1kHz, -1dBFS input (b) 1kHz, -60dBFS input

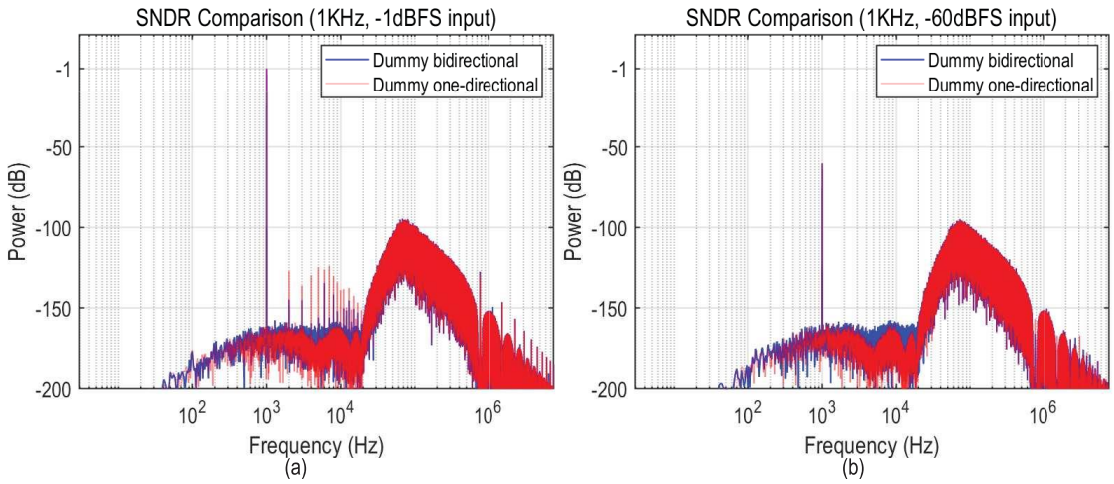

Fig. 31. SNDR Comparison of dummy bidirectional RT DEM and dummy one-directional RT DEM with: (a) 1kHz, -1dBFS input (b) 1kHz, -60dBFS input

3.2 Loop filter Design

3.2.1 Loop filter schematic

The schematic of the fully differential loop filter is shown in Fig. 32. Only half of the circuitry is shown for simplicity and the other half is exactly symmetrical. As mentioned in 3.1.1, the input common-mode (CM) voltages of the 1st integrator (V_{XP} and V_{XN}) are 7.2V. In order to accelerate the design progress, the 2nd and 3rd integrators are reused from [4], working in the 1.8V domain with CM voltage at 0.9V. The 1st integrator, contributed by Mengying Chen, transfers the signal from the 7.2V domain to the 0.9V domain. In order to further suppress the in-band distortion, an additional resistor $R_{resonate}$ is implemented across the second and the third integrator to create a resonator and boost the in-band loop gain. A resonator can also be generated by adding a feedback resistor across the first and the second integrator. However, since the input CM voltage of 1st integrator is defined by the output stage through R_{FB}, R_{FB} and this feedback resistor will act as a voltage divider between the 7.2V CM voltage of the output stage and the 0.9V CM voltage of the 2nd integrator output, making V_{XP} and V_{XN} deviate from 7.2V.

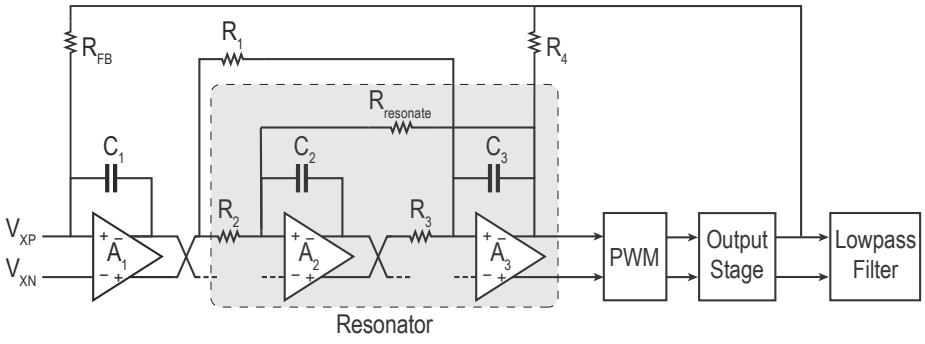

Fig. 32. Loop filter with resonator

The component values in the loop filter are sized so that the noise contribution meets the DR requirement and each amplifier output is within its linear range. The component values

(except the $R_{resonate}$) are listed in Table 2.

Table 2. Components value in the loop filter

Component	R_{FB}	R_1	R_2	R_3	R_4	C_1	C_2	C_3
Value	$30k\Omega$	$160k\Omega$	$460k\Omega$	$41.7k\Omega$	$480k\Omega$	$63.6pF$	$10.6pF$	$10.6pF$

The optimal value of $R_{resonate}$ can ensure the largest integrated in-band loop gain with A-weighting, so that in-band unwanted tones can be best suppressed according to human hearing characteristics. To find this optimal value, $R_{resonate}$ is swept in Cadence and the loop gain is integrated and A-weighted in Matlab. The resonant frequency is estimated by considering the transfer function $H_R(s)$ of the resonator shown in grey:

$$H_R(s) = \frac{R_{resonate}}{s^2 C_2 C_3 R_2 R_3 R_{resonate} - R_2}$$

When the denominator is zero, there will be a peak in the loop gain, thus, the resonant frequency $f_{resonate}$ can be calculated as:

$$f_{resonate} = \frac{1}{2\pi}\sqrt{\frac{1}{C_2 C_3 R_3 R_{resonate}}}$$

The $R_{resonate}$ versus average integrated loop gain with A-weighting is shown in Fig. 33. When $R_{resonate} = 27.75M\Omega$, the maximum average integrated loop gain with A-weighting is achieved. The calculated in-band resonant frequency is at 13.1kHz. The Cadence simulation result with ideal amplifiers further proves the correctness of the Matlab model, achieving a 13.2kHz resonant frequency, which has only a 0.8% difference in the resonant frequency.

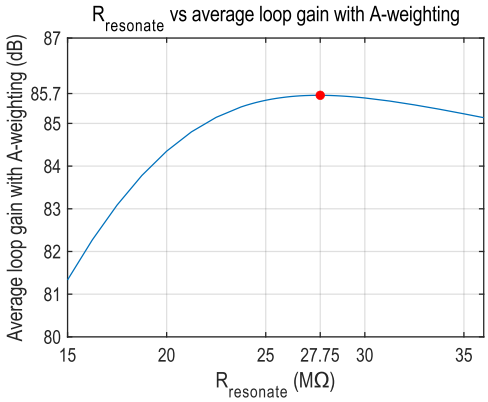

Fig. 33. $R_{resonate}$ versus average loop gain with A-weighting plot

However, $R_{resonate}$ is quite large and due to the differential structure, the two of them may occupy an area of $0.046mm^2$ if implemented with poly resistors. In order to save the area, a T-network equivalent of $R_{resonate}$ is applied with series connected R_5 and R_6, as well as R_7 which is directly connected to its differential counterpart, as shown in Fig. 34.

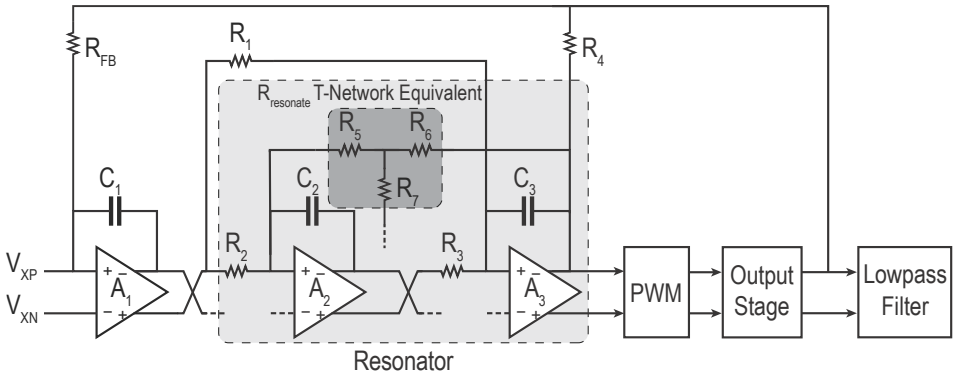

Fig. 34. Loop filter with T-network equivalent

The resonator transfer function with T-network can be estimated as:

$$H_R(s) = \frac{R_5R_6 + R_5R_7 + R_6R_7}{s^2C_2C_3R_2R_3\left(R_5R_6 + R_5R_7 + R_6R_7\right) - R_2R_7}$$

Thus, $f_{resonate}$ can be calculated as:

$$f_{resonate} = \frac{1}{2\pi}\sqrt{\frac{R_7}{C_2C_3R_3\left(R_5R_6 + R_5R_7 + R_6R_7\right)}}$$

The value of R_5, R_6, and R_7 are $725.3k\Omega$, $725.3k\Omega$, and $19.1k\Omega$ respectively. The equivalent $R_{resonate}$ can be estimated as $R_5 \cdot R_6/R_7$, which is $27.5M\Omega$. The calculated $f_{resonate}$ is 12.8 kHz. The nominal resonant frequency with ideal amplifiers, as shown in Fig. 35, is 12.9kHz, which has a 0.8% difference from the calculation.

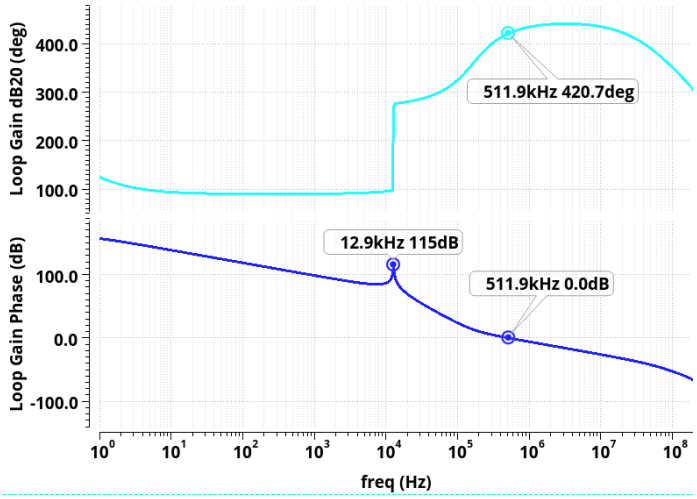

Fig. 35. Loop filter with ideal amplifiers nominal case stability analysis

The aforementioned values of resistors ensure a near maximum in-band loop gain, and a DR of 127.2dB with ideal amplifiers. They also make the matching of R_5, R_6, and R_7 easy, since their matching will determine the accuracy of the equivalent $R_{resonate}$, and thus affect the loop gain. With the T-network, the area consumption of the $R_{resonate}$ can be reduced to $2900\mu m^2$, which is 6.7% of the original size. Although it comes with an increase in the total

noise contribution (including quantization noise), they only take up 6.5% of noise for a -60dBFS input, and 1.3% of noise for a -1dBFS input.

3.2.2 Loop filter stability

The loop filter stability analysis is shown in Fig. 36. The nominal unity gain frequency is 540.9kHz, with a phase margin of 57.7°. The minimum phase margin in different corners is 54.6°, and the unity gain frequency varies from 437.6kHz to 686kHz.

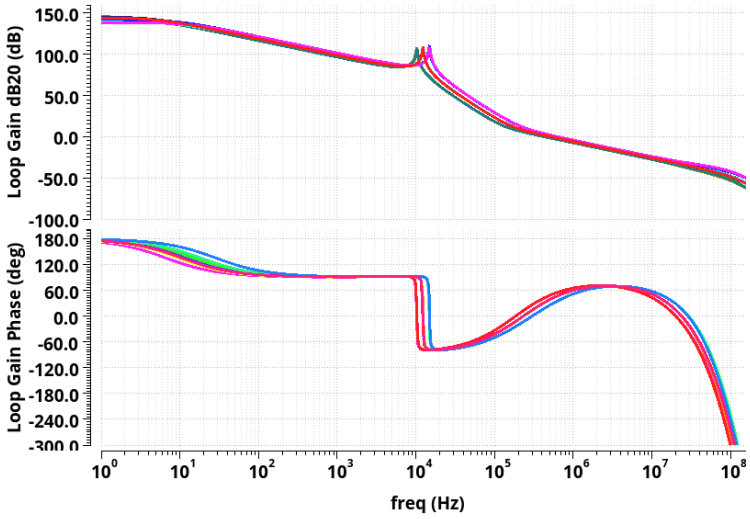

Fig. 36. Loop filter stability analysis

3.2.3 Loop filter noise analysis

The noise analysis of the loop filter is crucial for the estimation of DR since at small input, the noise is dominated by the noise from the loop filter. The Cadence simulation result shows that the total noise of the loop filter is $4.9\mu V$, which suggests the DR is limited to 126.4dB. The noise contribution is shown in Fig. 37, with the dominating noise contributor being the R_{FB}, which contributes to 62% of the total noise.

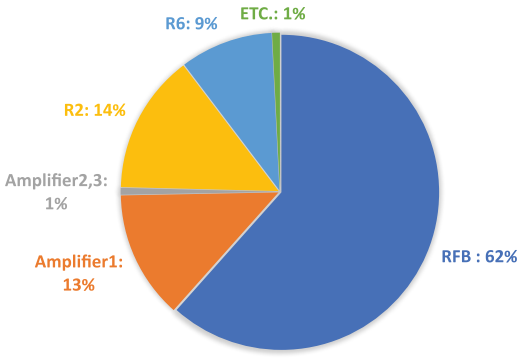

Fig. 37. Loop filter noise analysis

3.3 Power-up and power-down

The safety of the power-up and power-down of the chip is a crucial part of reliable operations. Special care is taken for the design of DAC, power supply sequencing, and digital

controls, to keep all transistors in their safe working region.

3.3.1 Supply sequencing during power-up and power-down

There are 4 voltage levels that are used in the chip: 1.8V, 4V, 5V, and 14.4V. The 1.8V supply is used for the digital circuitry, and amplifiers in the loop filter. The 4V reference is used for creating the reference current for the DAC. The 5V supply is used for the buffer, isolation rings, and digital IO. The 14.4V supply is used for the DAC and the output stage. Since the DAC and the loop filter amplifiers contain some 2V or 5V MOSFETs that are used in the 14.4V supply circuitries, the 14.4V voltage needs to be established after all the other voltage levels. The other supplies are generated with commercial off-the-shelf linear regulators and their order does not affect the safe operation. The power-up supply order is 1.8V, 4V, 5V, and in the end 14.4V, and for power-down, the supply order is reversed.

3.3.2 DAC power-up and down

There are 2 main issues in the power-up and power-down procedure of the DAC: switch controls in level shifters, and the capacitor charging of the noise filters.

3.3.2.1 Switch controls in level shifters

If the level shifter is naturally powered up. The latches in the level shifters are latched to an unknown state that depends on parasitic capacitance and resistance, which varies across different temperatures and corners. This could lead to unwanted level shifter outputs and thus incorrect current outputs. Keep-alive circuits are added to establish a predictable safe initial condition of the level shifters.

Fig. 38 shows the structure of the keep-alive circuit. A transistor (M_{K2} or M_{K3} for the source or sink side respectively) pulls up the level shifters output to 7.2V, which ensures that all the switches in the DAC are “on” during power-up, so that the headroom of the CSs in each DAC unit is correct. Also, another transistor (M_{K1} or M_{K4} for the source or sink side respectively) provides a current path to charge the capacitor (C_{FP} or C_{FN}) before the switches start toggling. The keep-alive transistors are biased by V_{KP} and V_{KN} for the source and sink side respectively [5]. Each of them is generated by a diode-connected MOSFET, a resistor and a capacitor. This is to ensure that the keep-alive transistors are only conductive during power-up or power-down, but do not lead to current leakage during the level shifter’s normal operation. During power-up, the keep-alive transistors are on, and the capacitor (C_{FP} or C_{FN}) will be charged until 7.2V. When the 7.2V is held on the capacitors, V_{KN} and V_{KP} are around 7.2V, disabling the conductivity of the keep-alive transistors.

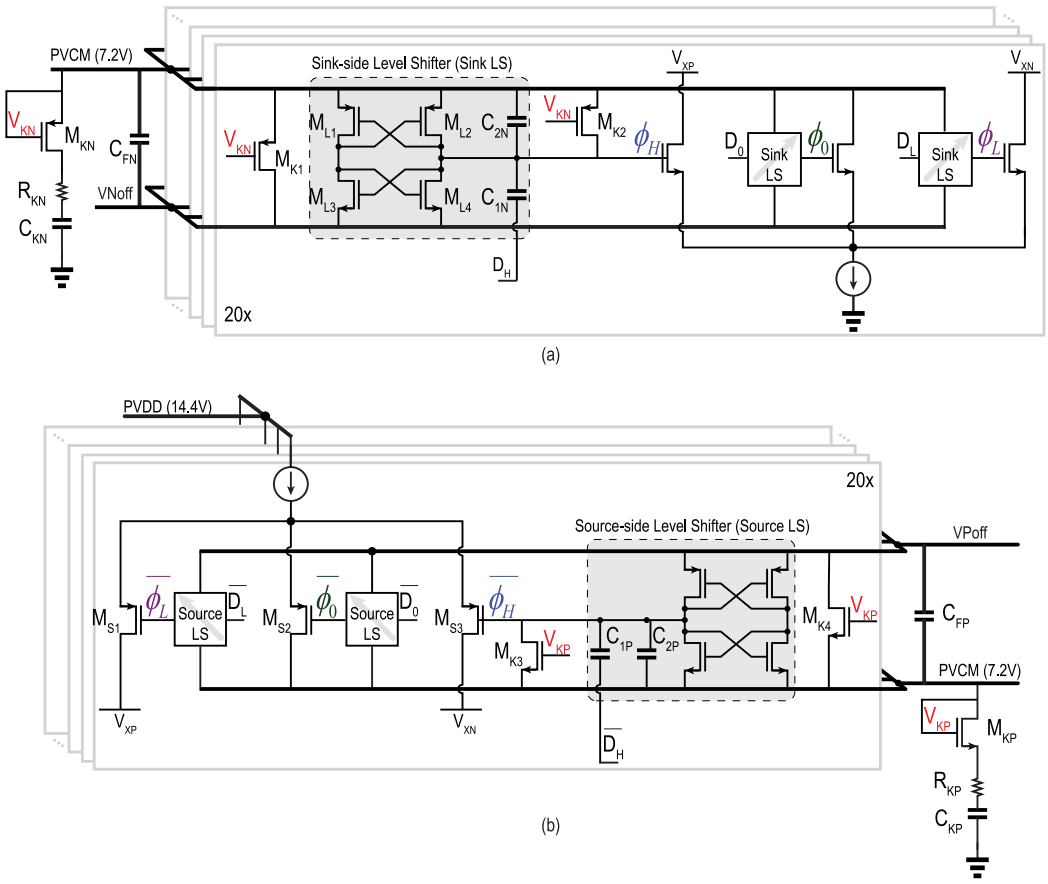

Fig. 38. Keep-alive circuit: (a) sink side (b) source side

The waveforms of the level shifter with the keep-alive circuit is shown in Fig. 39. There is no overvoltage during power-up and the level shifter outputs are correctly established.

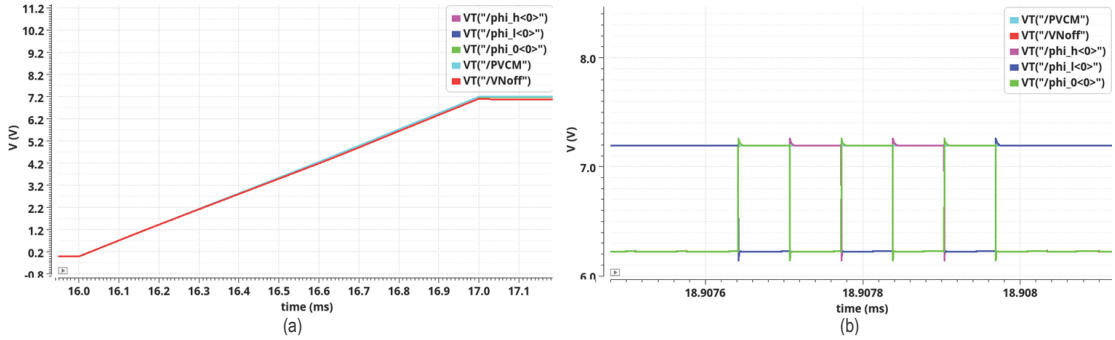

Fig. 39. Level shifter waveforms with the keep-alive circuit: (a) power-up waveforms (b) zoomed-in power-up waveforms

3.3.2.2 Noise filter shorting circuit

The noise filter can lead to overvoltage during power-up. Fig. 40 shows the power-up waveforms and Fig. 41 shows the circuit illustration. G_{NB} can rise to 7.8V while the bulk of the transistors are about 4V, leading to an overvoltage on V_{GB} of the main transistor M_{Nmain}. This is because the G_{Nmain} is charging so slowly that the bulk voltage (Bulk) is larger than the source voltage, making the bulk-source PN junctions shown in Fig. 41 conduct leaky currents. With 23 branches (3 biasing and 20 DAC units), an extra current of $243\mu A$ is injected to

M_1, making the biasing node voltages, including the G_{NB} deviate from the normal value. Although with a longer simulation, the biasing nodes are able to return to the desired value, the overvoltage will first damage the transistors in reality.

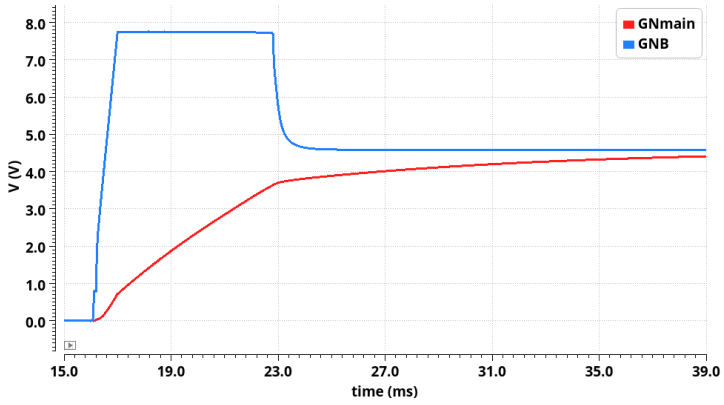

Fig. 40. Voltage waveforms of biasing nodes without shorting transistor

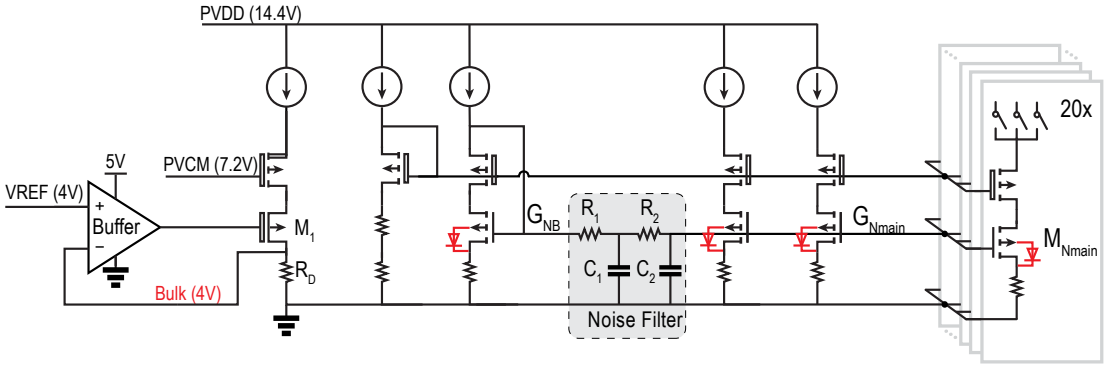

Fig. 41. Biasing circuit with bulk-source diode illustration

In order to ensure a safe operation, a switch is added to short the noise filter during power-up, and then the noise filter starts filtering after all biasing voltages are established. As shown in Fig. 42, a minimum size PMOS transistor is used to short the noise filter, which has an on-resistance of $25.2K\Omega$. Although a larger width can make the on-resistance smaller, the area consumption is larger and the temporary choice can already ensure the G_{Nmain} node follows the G_{NB} without overvoltage.

During power-up, G_{NB} and G_{Nmain} are first shorted for safe operation and then this shorting connection is disabled by G_{RSTN} so that the noise filter is enabled. When the noise filter starts working, this transistor contributes a parallel off-resistance of $552G\Omega$, having an ignorable effect (0.006dB difference on DR, 0.018dB difference on THD+N) on the noise filtering effectiveness.

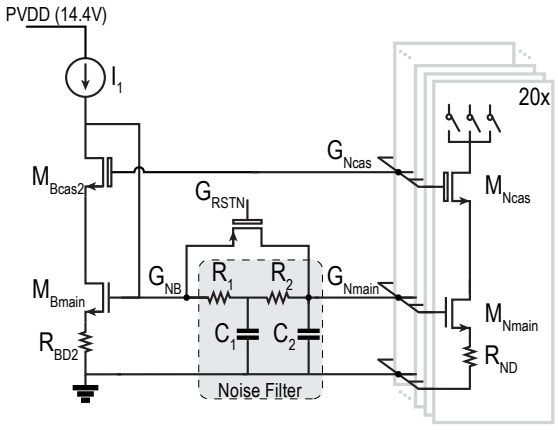

Fig. 42. Noise filter with the shorting transistor

3.4 Layout

The proposed CDA is fabricated in a 0.18μm BCD process and occupies a die area of $7.9mm^2$. The layout floorplan of the chip is shown in Fig. 43.

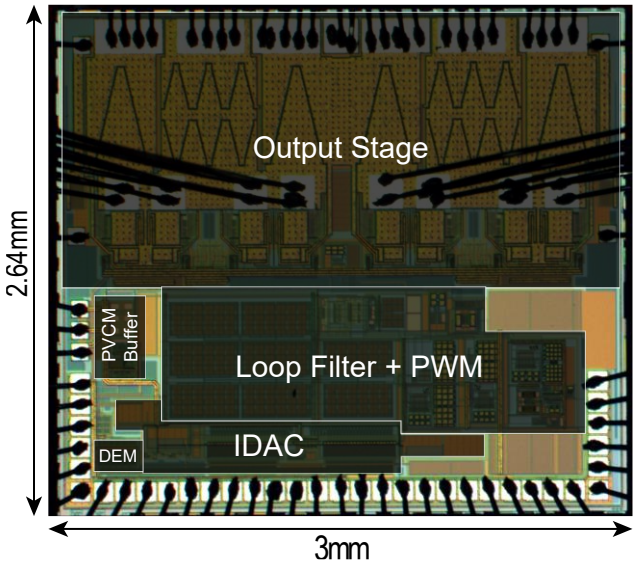

Fig. 43. Layout floorplan of the chip

3.5 Post-layout simulation results

In order to save time and computing resources, noise simulation for post-layout simulation is conducted with AC noise sweep instead of enabling transient noise. The noise contributions of the loop filter and the DAC are shown in Fig. 44. Fig. 44 (a) shows the small signal input noise contribution when 2 DAC units are used for current output and Fig. 44 (b) is the large signal input noise contribution when all DAC units are used for current output. Since with a larger input, more DAC units are connected to the output, the noise from the biasing, noise filter, and DAC units increases. The achieved SNDR with -1dBFS input is 117.76dB and the DR is 124.47dB. If the noise filter is disabled, the SNDR has a drop of 14.1dB and the DR has a drop of 3.2dB.

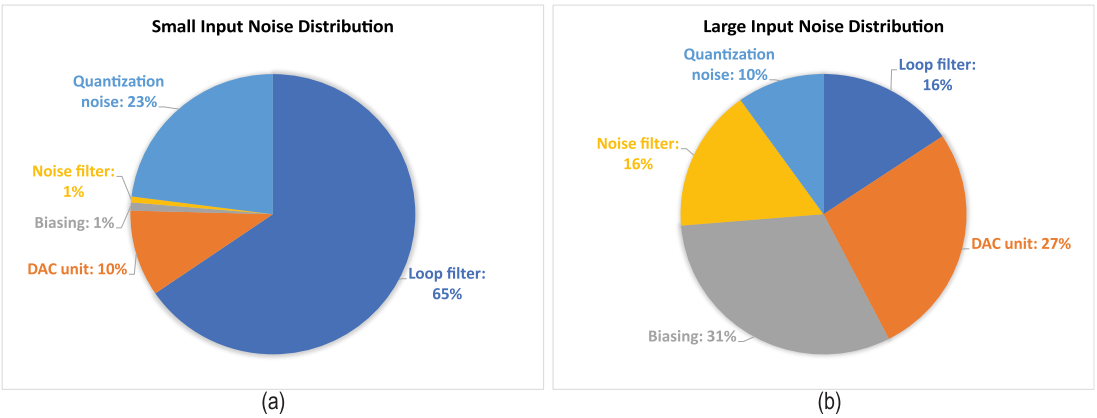

Fig. 44. Loop filter with IDAC noise analysis: (a) small input (b) large input

To simulate distortion, the parasitic capacitors of the chip layout are extracted and added to the simulation. In order to save simulation time while having sufficient in-band harmonics, the input signal frequency for post-layout transient simulation is 5kHz. The normalized (by 14.4 V full scale) FFT spectrum with a 5kHz, -4.5dBFS input signal is shown in Fig. 45. An SNDR of 115.3dB is achieved with a small 3rd harmonic tone of -126.8dB. If combined with the thermal noise and quantization noise, the THD+N is -111.7dB.

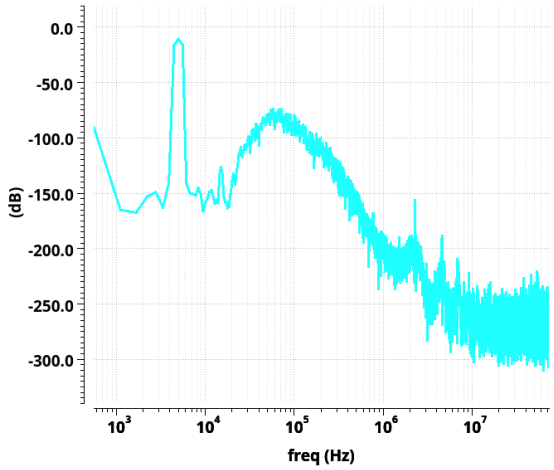

Fig. 45. FFT spectrum with 5kHz -4.5dBFS input signal, nominal case

The simulation results for different corners and temperatures are shown in Table 3. The THD+N result varies from -105.2dB to -112.6dB across corners and temperatures.

Table 3. Post layout simulation results of different corners and temperatures

	SNDR (without transient noise)	THD+N
Nominal	115.3dB	-111.7dB
Slow corner, 25°C	105.8dB	-105.2dB
Slow corner, 125°C	107.3dB	-106.5dB
Fast corner, 25°C	117.5dB	-112.6dB
Fast corner, 125°C	114.1dB	-111.2dB

References

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Chapter 4 Chip measurement

4.1 External supportive equipment

4.1.1 PCB design

For the chip measurement, some external supply voltages and signals are provided through the PCB test boards. The PCB test boards consist of a daughterboard as well as a motherboard. The motherboard is mainly reused from a previous design in [1], where the 1.8V reference signals for PLL, and the 5V isolation (ISO) ring are generated, and the digital audio input is fed in from the FPGA. The daughter board, shown in Fig. 46, is where the chip is directly wire-bonded, and small changes can be easily made without adjusting the motherboard.

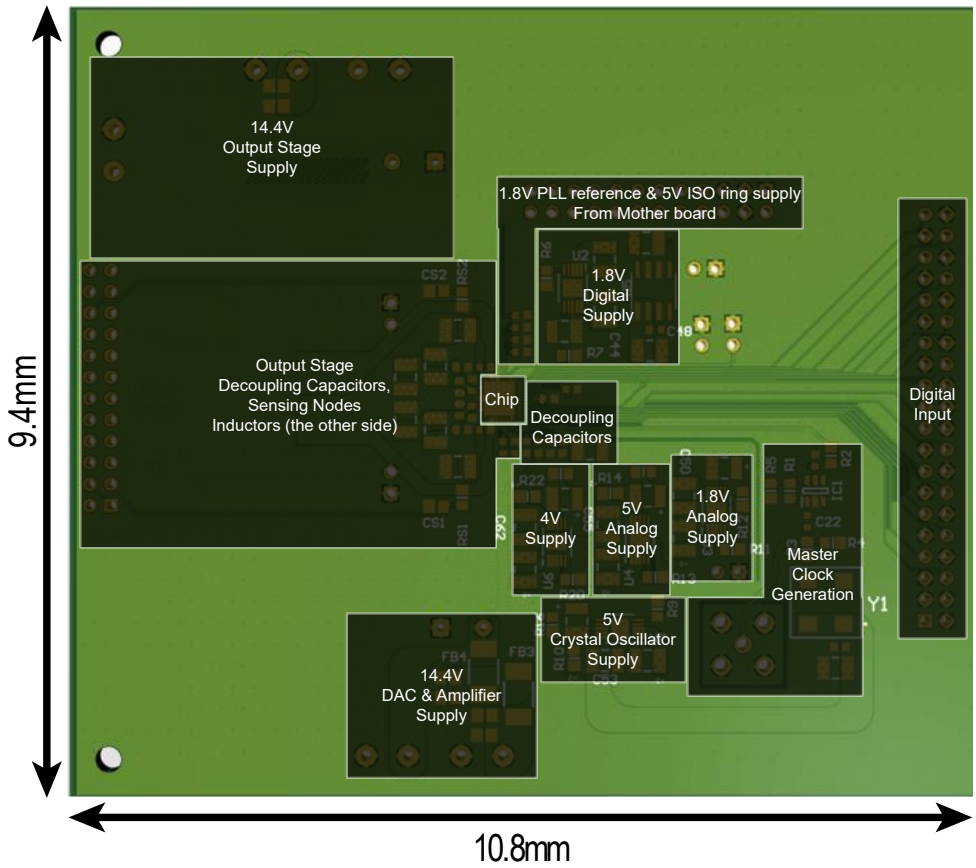

Fig. 46. Daughter board PCB floorplan

The daughter board is designed to ensure that the crucial supply voltages and their decoupling capacitors are located closest to the chip. The most crucial supply voltages are the 4V and 5V supplies for the IDAC reference. They are located the closest to the chip so that the wire between the supply and the chip has minimum resistance for low noise and minimum inductance for low interference. The 1.8V and 5V supplies for analog and digital circuits are generated separately to ensure a clean analog supply. The 14.4V supply for the output stage and the DAC can also be supplied by separate sources so as to minimize the supply voltage

fluctuation of the DAC and the amplifier brought by the output stage. All the analog supply voltages are star-connected to the same ground node near the chip so that the minimum influence between supplies is ensured.

4.1.2 Other external equipment

The chip measurement equipment setup is shown in Fig. 47. The 24-bit digital input source and the CDA output measurement are both provided by the APx555 audio signal analyzer. The interpolation filter and digital DSM are provided by the FPGA. The measurements for different test nodes are probed on an oscilloscope.

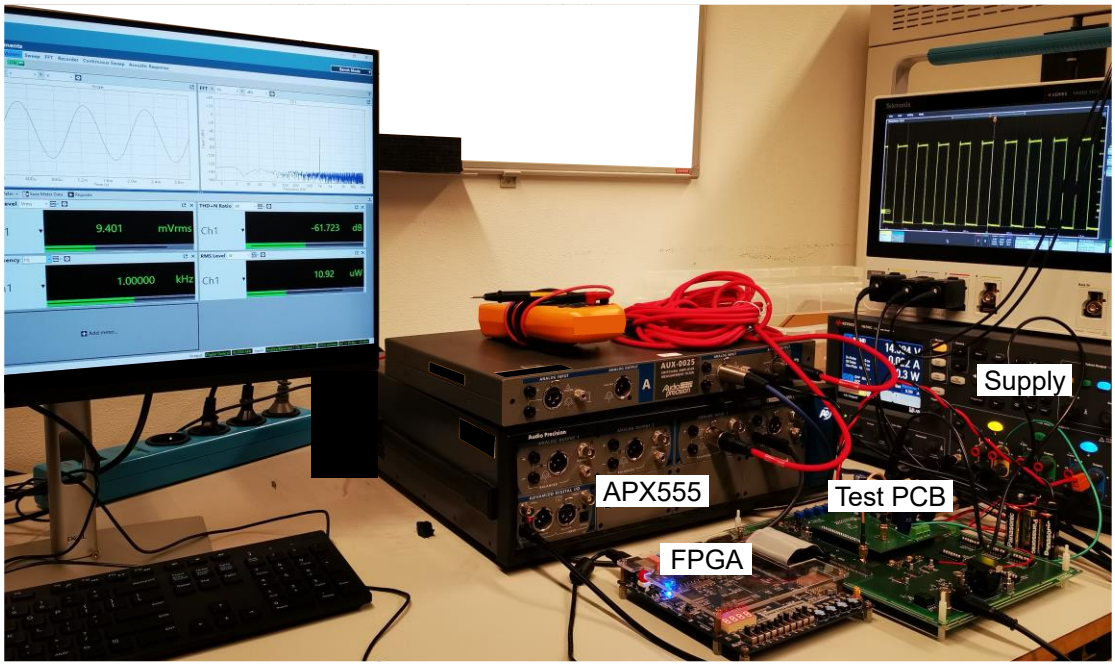

Fig. 47. Chip measurement equipment setup

4.2 Measurement results

When measured with the 3-level mode of the output stage in [1], the measured THD+N can only reach a peak of 96.5dB. This might be the combined result of using real voltage references, the PCB-induced parasitic and interference, and corner effects in contrast with the ideal voltage sources in the post-layout simulations. To reduce the influence of the output stage on the common mode voltage for the DAC, further measurements for the chip are conducted with the 2-level mode of the output stage. The CDA is loaded with an 8Ω resistor in series with a 44μH inductor, which represents the speaker. Fig. 48 shows the measured FFT spectra when the CDA delivers a 1kHz sinewave. A THD+N of -102.3dB is achieved at 1W. At -60dBFS input, an SNR of 61.7dB is measured, indicating a DR of 121.7dB. Fig. 49 (top) shows the measured THD+N vs. output power, achieving peak THD+N of -104.0dB and -109.0dB for 1kHz and 6kHz inputs, respectively. Fig. 49 (bottom) plots the power efficiency and a peak efficiency of 90% is achieved.

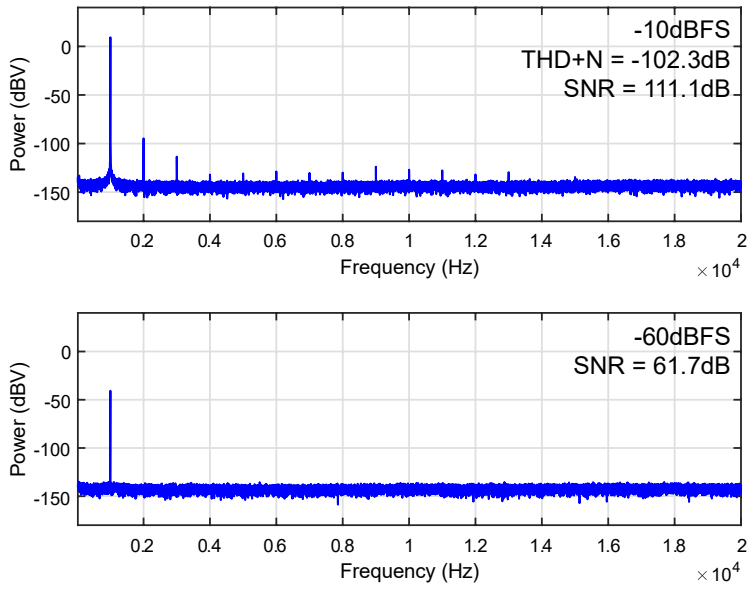

Fig. 48. Measured output spectra (128-point FFT, 4x averaged)

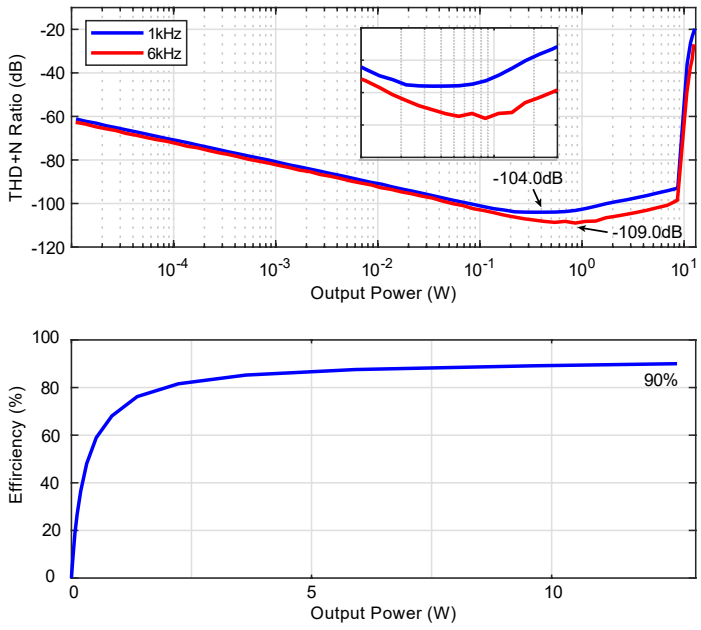

Fig. 49. Measured THD+N vs. output power (top) and power efficiency (bottom)

Fig. 50 compares the performance of this work with state-of-the-art digital-input CDAs using IDAC or RDAC. It achieves the highest DR by >6.2dB. Thanks to the dummy bidirectional RTDEM scheme, it achieves a competitive THD+N: >6.8dB and >11.3dB better than other HV CDAs for 1kHz and 6kHz signals, respectively. Compared to a low voltage CDA employing tri-level IDAC units [3], it achieves 8.7dB higher DR, and 11dB and 19dB better peak THD+N for 1kHz and 6kHz signals, respectively.

	This Work	A. Matamura ISSCC 2021	E. Cope ISSCC 2018	D. Schinkel JSSC 2017	T. Ido ISSCC 2006
Process	**180nm BCD**	40nm CMOS	180nm BCD	140nm BCD	-
Area (mm^2)	**7.9**	1.33	4.3	-	23[1]
DAC Type	**Tri-level IDAC**	Tri-level IDAC	RDAC	2-level IDAC	2-level IDAC
Supply (V)	**14.4**	1.8	8~20	25	35
DR (dB)	**121.7**	113	115.5	115	113
Output Noise (μV_{RMS})	**8.0**	-	20	34	-
THD+N (dB) at 1kHz	**-104.0**	-93	-97.2[2]	-88.6	-94.9
THD+N (dB) at 6kHz	**-109.0**	-90[2]	-97.7	-90[2]	-90[2]
Efficiency	**90%**	93%	90%	>90%	81%
$I_{Q,PVDD}$ (mA)	**22**	1.23	20.5	-	-
R_{LOAD} (Ω)	**8**	16	8	4	4/6/8
$P_{OUT,MAX}$ (W)	**12.7**	0.086	20	80	130/99/74[1]
PSRR (Frequency [Hz])	**93~71 (20~20k)**	94 (1k)	80~50 (20~20k)	88~60 (100~20k)	-

[1] Output stage is off-chip
[2] Estimated from figure

Fig. 50. Comparison with state-of-the-art digital-input CDAs using an IDAC or RDAC

References

[1] H. Zhang, M. Berkhout, K. A. A. Makinwa and Q. Fan, "3.1 A 120.9dB DR, -111.2dB THD+N Digital-Input Capacitively-Coupled Chopper Class-D Audio Amplifier," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 54-56, doi: 10.1109/ISSCC42615.2023.10067400.

[2] H. Zhang et al., "A −107.8 dB THD+N Low-EMI Multi-Level Class-D Audio Amplifier," 2020 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 2020, pp. 1-2, doi: 10.1109/VLSICircuits18222.2020.9162793.

[3] A. Matamura et al., "An 82mW ΔΣ-Based Filter-Less Class-D Headphone Amplifier with -93dB THD+N, 113dB SNR and 93% Efficiency," in ISSCC, Feb. 2021, pp. 432-434.

Chapter 5 Conclusion and future improvement

5.1 Conclusion

This project presents a 14.4V digital-input CDA that achieves high DR and low THD+N by employing a high-voltage multi-bit IDAC. A new dummy bidirectional RT DEM scheme is proposed to suppress nonlinearity due to mismatch and ISI. Implemented in a 180nm BCD process, the prototype achieves 121.7dB DR, -104.0dB, and -109.0dB peak THD+N for 1kH and 6kHz signals, respectively. It can deliver 12.7W at 10% THD into an 8-Ω load with 90% efficiency.

5.2 Future improvement

Due to the time and resource limitations, the design of the chip still needs some improvements. The following aspects may require more future work.

First, the chip could be redesigned to ensure all the subcircuits meet the battery requirements of automotive applications. Some voltage regulators or references could be developed such that even when the 14.4V battery supply varies in a wider range, the chip can still work properly.

Second, the chip relies on 3 different supply voltages (1.8V, 4V, 5V), which are generated by some commercial off-the-shelf low noise references. To achieve good noise and distortion performance, the layout of the PCB has a lot of restrictions. The voltage references could be integrated into the chip so that less total PCB area and potentially better performance can be achieved. Also, these voltage supplies might be merged such that a simpler and more reliable power-up and power-down is possible.

Third, the chip is only simulated under 25℃ and 125℃ conditions, and tested in the lab only under room temperature due to limited CPU and equipment resources. However, in the real application case, the chip may need to offer a good performance when the temperature is as low as -40℃. Further design considerations should be taken to ensure this, and simulations should also be conducted at -40℃. A fridge and an oven are also needed so that the chip can be tested in the lab with different temperature conditions to verify the performance.

Fourth, the chip is measured with the 2-level output stage for a clean common mode voltage for the DAC. However, the 3-level mode of the output stage exhibits lower idle power. Further simulations and measurements should be done to explore the full potential of the 3-level mode output stage.