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TOPICAL REVIEW

A Review of High-Step-Up Non-Isolated DC–DC Converters Focusing on the Topology Methodology and Features

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ABSTRACT Power electronic converters are essential components in modern electrical systems, with dc–dc converters being particularly crucial for their extensive variety and widespread applications, notably in renewable energy systems and electric vehicles. For applications such as Photovoltaic (PV) arrays, fuel cells, and microgrids, a critical requirement is the need for non-isolated, high step-up dc–dc converters capable of providing a high-voltage gain while mitigating significant practical challenges, including high semiconductor stress and degraded efficiency at extreme duty cycles. This study proposes a comprehensive, structural-based review of over 100 non-isolated high step-up dc–dc converters, specifically excluding topologies that rely on coupled inductors. Our primary contribution is a novel categorization and comparative analysis framework that delves into the fundamental topological details and features, going beyond the focus of recently suggested reviews. The methodology begins with a systematic analysis of classical non-isolated converters (Boost, Buck-Boost, Ćuk, SEPIC, and Zeta) to establish a baseline and highlight their limitations, such as the semiconductor voltage stress being greater than the output voltage in most cases, which reduces their suitability for high-gain applications. The paper then systematically classifies advanced topologies into 23 distinct groups based on their unique structural characteristics. The comparison is rigorously quantitative and systematic, focusing on structural details and key performance metrics such as voltage gain and density, semiconductor stress, and current continuity and component count. The comprehensive analysis is conducted by deconstructing each topology into its constituent sub-converters to reveal how structural combinations influence key performance metrics. Finally, the findings facilitate a discussion on the practical applications of each topology, matching their inherent characteristics to specific real-world systems like PV arrays, Electric Vehicles (EVs), Vehicle-Integrated PV (VIPV) systems, and electrolyzers.

INDEX TERMS Boost converter, classic non-isolated dc–dc converters, non-isolated high-step-up dc–dc converters.

I. INTRODUCTION

Power electronics converters are fundamental to modern electrical systems, enabling four primary types of signal conversion: AC-to-AC, AC-to-DC, DC-to-DC, and DC-to-AC. Among these, DC-DC converters stand out due to their extensive variety and widespread applications. However, their design and operation present significant challenges, particularly concerning control and topology. Effective control is paramount to ensuring stable and desired output in the face of disturbances. Topologically, several critical factors influence performance, including voltage gain (the ratio of

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output to input voltage), current stress on semiconductors (the average current during activation), voltage stress on semiconductors (the applied voltage during inactivation), and the continuity of input/output currents. The vast number of DC-DC converter topologies has led to numerous review studies in the field. For instance, the comprehensive review in [1] categorizes converters into switch-inductor, switch-capacitor, voltage multiplier-based, coupled-inductor-based, interleaving-based, multi-stage, and cascaded topologies, covering both isolated and non-isolated designs. These diverse converters are then rigorously compared based on component count, ripple, device stress, and voltage gain characteristics.

Building upon the foundational understanding of DC-DC converters, various review studies delve deeper into specific topologies and performance aspects. For example, [2] offers a comprehensive discussion of classic converters, including half-bridge, full-bridge, dual-active bridge, buck, boost, multi-phase buck/boost, Cuk, SEPIC, and Zeta converters, analyzing them by their power flow modes, soft-switching capabilities, transient response, and typical applications. Further expanding the scope, [3] investigates stacked, multiplier-based, coupled-inductor-based, and switch-cell-based topologies, evaluating them based on crucial metrics such as component count, physical dimensions, power density, cost, control complexity, and component stress. The specific challenges of isolated bidirectional CLLC resonant converters are a central theme in [4], which thoroughly examines their modeling, Zero Voltage Switching/Zero Current Switching (ZVS/ZCS) regions, magnetic tank design, synchronous rectification (SR) control, and the comparative merits of variable-frequency versus variable-duty phase control. Turning to broader bidirectional applications, [5] provides an overview of various bidirectional DC-DC converters, comparing them in terms of power rating, static gain, device technology (e.g., Si vs. SiC or GaN), and control design trends pertinent to propulsion systems. Notably, high-gain non-isolated topologies, particularly suitable for rectified HVDC bus to battery interfaces, are the focus of [6], where the inherent trade-offs between voltage gain and efficiency are also explored. Finally, the specialized domain of multi-port non-isolated DC-DC converters is thoroughly examined in [7].

Beyond specific converter types, other reviews categorize them by their control methodologies. These studies often discuss the application of various control methods, including traditional PID, advanced sliding mode control (SMC), model predictive control (MPC), fuzzy logic, and maximum power point tracking (MPPT) techniques. From a topological perspective, factors such as component count reduction, efficiency, and reliability are frequently analyzed. A specialized review in [8] focuses on PV-oriented topologies, comparing them based on component count, soft-switching capabilities, and their suitability for microgrid configurations (AC, DC, or hybrid). This study also highlights the distinct advantages offered by coupled-inductor-based and interleaved topologies within the solar energy context.

Further refining the understanding of DC-DC converters, several studies address specific design challenges and applications. For instance, [9] explores various techniques for increasing voltage gain in non-isolated step-up and step-down converters. In the context of renewable energy integration, [10] provides crucial guidance on the selection of non-isolated multi-port DC-DC converters, examining their circuit structure, operation, component count, complexity, and efficiency. Another significant trend is the development of bidirectional DC-DC converters, particularly those facilitating grid-vehicle energy exchange systems, which is the focus of [11]. A broader taxonomic review in [12] delves into a wide array of isolated and non-isolated topologies relevant to Hybrid Energy Storage Systems (HESS) and solar DC microgrids, comparing them based on efficiency, compactness, power handling, and voltage gain. Moving to specific applications and comparisons, [13] contrasts non-isolated converters like buck, boost, and Cuk, alongside classic isolated DC-DC converters, evaluating their power ratings and the efficacy of various control methods such as MPC, SMC, and fuzzy logic. For isolated multi-port converters, [14] investigates modulation methods, port stresses, power decoupling, and transformer design considerations under high power density requirements. Notably, [15] focuses on quadratic boost topologies suitable for electric vehicles (EVs), analyzing their device stress, voltage gain, and efficiency. Concurrently, the challenges of isolated DC-DC converters for simultaneous EV battery charging, including high-frequency transformer design and testing, and power quality issues on the grid side, are thoroughly examined in [16].

Advancing into more specialized applications, [17] delves into advanced isolated DC-DC converters designed for renewable energy resources, critically comparing their efficiency, synchronous rectification capabilities, ZVS/ZCS operation, and the adoption of Wide Band Gap (WBG) semiconductors. Moving to smaller-scale grids, [18] investigates modern topologies specifically tailored for nano/pico grids, also addressing hybrid control strategies and MPPT under dynamic conditions. Parallel to this, [19] focuses on the topology, modulation, and design procedures of DC-DC converters with a strong emphasis on photovoltaic (PV) applications. Echoing themes from earlier discussions, [20] provides a comparative analysis of buck, boost, SEPIC, and Cuk converters, particularly focusing on their efficiency and ripple characteristics. An intriguing concept explored in [21] is mathematical MPPT, which leverages the relationship between converter input resistance and duty cycle, discussing its application across both isolated and non-isolated topologies for PV MPPT. A landmark review in [22] comprehensively covers non-isolated high-gain PV-based converters, including switch-capacitor-based, switch-inductor-based, voltage-multiplier-based, and coupled-inductor-based

topologies, with a particular focus on component stress and the inherent gain-efficiency trade-off. Finally, [23] addresses DC-DC converters suitable for electrolyzers, detailing the procedure for topology selection based on electrolyzer dynamics and the specific requirements for their current control.

Further expanding the converter landscape, [24] explores multi-stage step-up isolated and non-isolated converters, categorizing them by their voltage/current fed configurations and hard/soft switching techniques. The crucial role of bidirectional DC-DC converters in Hybrid Energy Storage Systems (HESS) is extensively detailed in [25], with particular attention paid to power ripple mitigation and effective control strategies. Significantly, non-isolated high-step-up DC-DC converters serve as vital front-end links for renewable energy resources, and [26] provides a comprehensive discussion of numerous topologies suited for this application. The growing prevalence of Electric Vehicles (EVs) introduces challenges, especially regarding fast charging. Addressing this critical need, [27] extensively discusses both isolated and non-isolated converter solutions designed to meet the demanding requirements of EV fast charging.

Delving into more complex system integrations, [28] offers a comparative review of multi-port topologies, highlighting challenges in control and presenting recent MPPT/dispatch strategies for renewable energy sources combined with storage equipment. Complementing this, [29] provides a focused review of energy management and advanced control methods, specifically within the context of bidirectional EV-based DC-DC converters. Another significant consideration in DC-DC converter design is the extendability versus non-extendability of the topology. Reference [30] conducts a comparative analysis of high-voltage-gain isolated and non-isolated PV-based converters through this specific lens. Furthermore, DC-DC converters are integral to the battery balancing systems of EVs, facilitating cell-to-cell, cell-to-pack, multi-winding, and modular structures, and are often integrated with Battery Management System (BMS) strategies. This comprehensive topic is presented in [31]. Finally, [32] reviews the widespread usage of non-isolated multi-port DC-DC converters in hybrid EVs, underscoring their importance in these complex systems.

Exploring further into specialized applications, multi-input DC-DC converters are widely employed in hybrid EVs, offering the advantage of reduced component count compared to traditional series/parallel stacking. Reference [33] provides a comprehensive review of this topic, specifically comparing the control complexity of these converter types. Expanding on the application within renewable energy, [34] focuses on non-isolated DC-DC converters and their associated control techniques. For a broader perspective, [35] offers an extensive review encompassing the topology, control, design, and diverse applications of DC-DC converters. Returning to multi-input designs for hybrid EVs, [36] specifically examines converters suitable for this demanding environment. In the realm of renewable energy optimization, [37] delves into advanced MPPT techniques, array configurations, and the corresponding DC-DC converter topologies, a topic further explored in [38] with a focus on classic non-isolated DC-DC converters. Concluding this overview of specialized reviews, [39] focuses exclusively on high-conversion-ratio DC-DC converters, irrespective of their specific types or isolation characteristics.

This paper provides a focused review of non-isolated, high step-up DC-DC converters, specifically excluding topologies that utilize coupled inductors. Our discussion systematically explains each topology by deconstructing it into its constituent classic non-isolated converters, such as boost, buck-boost, Cuk, SEPIC, and Zeta. We further analyze various modified forms of these classic converters within the improved topologies, and explore modern designs incorporating diverse inductor-based and diode-capacitor-based voltage multiplier cells (VMCs).

For each converter, we express its voltage gain and critically compare the maximum semiconductor voltage stress against the output voltage. A significant aspect of our review is the examination of input and output current continuity, considering the influence of sub-converters on filter capacitor requirements. We also analyze the voltage gain in conjunction with component count, introducing various voltage gain density metrics to effectively illustrate each converter's gain capabilities. A novel contribution of this paper is the rigorous categorization of studied topologies based on their distinct topological features. Finally, we discuss the practical applications of these topologies across various fields, linking their utility directly to their inherent topological characteristics. The structure of the paper is illustrated in Fig. 1. According to this figure, in the second section, the classic converters and discussed converters are explained. In the third section, the comparison of the discussed converters is done. The fourth section belongs to the suitable application and the final section explains the conclusion of the paper.

II. TOPOLOGICAL DISCUSSION OF THE NON-ISOLATED DC–DC CONVERTERS

Figure 2 presents the fundamental non-isolated DC–DC converter structures, including the boost converter in Fig. 2(a), the buck–boost converter in Fig. 2(b), the Ćuk converter in Fig. 2(c), the SEPIC topology in Fig. 2(d), and the Zeta converter in Fig. 2(e). Despite their functional differences, all five converters share a simple single-switch configuration in the power stage. A primary distinction among these topologies is the placement of the active switch: the boost, Ćuk, and SEPIC converters adopt a low-side switch configuration (with the switch source terminal referenced to ground), whereas the buck–boost and Zeta converters employ a high-side switch (with the source terminal not directly grounded). This structural difference has direct implications for driving circuitry, electromagnetic interference (EMI) behavior, and potential integration in low-voltage applications.

From the perspective of current characteristics, the boost, Ćuk, and SEPIC topologies inherently provide continuous input current. This feature substantially reduces the current ripple at the input port, thereby lowering the stress on the input filter capacitor and enabling the use of smaller-capacitance devices with reduced parasitic effects. In contrast, the buck–boost and Zeta converters draw a discontinuous input current, which increases ripple and consequently requires a higher-capacitance input filter to maintain acceptable input-side performance.

On the output side, continuous current is maintained in the Ćuk and Zeta converters, contributing to improved output voltage quality and reduced stress on the output filter components. Additionally, the converters differ in their output voltage polarity: the boost, SEPIC, and Zeta topologies produce a non-inverting (positive) output voltage, whereas the buck–boost and Ćuk converters generate an inverting output voltage with reversed polarity relative to the input.

Among these topologies, the boost converter is the only one that provides a purely step-up voltage gain over the entire duty-cycle range. In contrast, the buck–boost, Ćuk, SEPIC, and Zeta converters exhibit a dual-mode behavior: they operate as step-down converters for duty cycles below 50%, achieve a unity (pass-through) gain at a duty cycle of 50%, and transition to step-up operation for duty cycles above 50%. Table 1 summarizes these characteristics together with the previously discussed electrical features of the classical non-isolated converters. The voltage conversion ratio of the boost converter is expressed as:

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{1}$$

The voltage gain of the buck-boost, Cuk, SEPIC, and Zeta converters is as follows:

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{2}$$

Figure 3 provides a comparative illustration of the voltage gain characteristics of the classical converter topologies based on their analytical expressions. As shown, the boost converter consistently achieves a higher voltage conversion ratio across the entire duty-cycle range when compared with the buck–boost, Ćuk, SEPIC, and Zeta converters. All of these classical converters employ only one active switch and one diode in their power stage, which contributes to their structural simplicity and ease of implementation. The corresponding voltage and current stresses imposed on the semiconductor devices for each topology are summarized as follows:

$$\begin{cases} V_s = \dfrac{V_{in}}{1-D}, V_D = \dfrac{V_{in}}{1-D} \\ I_s = \dfrac{D}{1-D} I_o, I_D = I_o \end{cases} \tag{3}$$

This analysis shows that, in the boost converter, the voltage stress on both the switch and diode is equal to the output voltage. In contrast, the buck–boost, Ćuk, SEPIC, and Zeta converters impose a voltage stress greater than the output voltage on their semiconductor devices, which reduces their suitability for high-gain applications. Regarding current stress, the boost converter exhibits a switch current lower than the input current, whereas the corresponding current stress in the buck–boost, Ćuk, SEPIC, and Zeta topologies is equal to the input current. Ideally, for enhanced performance, improved efficiency, and extended device lifetime, the semiconductor voltage stress should remain below the output voltage, and the current stress should be lower than the input current. According to these criteria, the classical non-isolated converters generally do not meet the desired voltage-stress condition, although the boost converter demonstrates comparatively better current-stress characteristics.

Figure 4 presents the normalized maximum voltage and current stresses experienced by the semiconductor devices in the classical converter topologies. As shown, these elevated stress levels impose substantial constraints on the applicability of the classic converters in high–voltage-gain designs. Although the theoretical voltage-gain curves in Fig. 3 indicate that large gains can be achieved at high duty cycles, practical implementation rarely permits operation at such extreme duty-cycle values due to the resulting efficiency degradation, excessive conduction and switching losses, and increasingly severe device stress. Consequently, Fig. 3 does not fully reflect the practical gain characteristics of these converters.

When parasitic elements—such as the inductor winding resistance and the on-state resistances of the switch and diode—are considered, the effective voltage gain of the boost converter is more accurately expressed as:

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} - \frac{r_L}{R}\frac{1}{(1-D)^3} - \frac{r_s}{R}\frac{D}{(1-D)^3} - \frac{r_D}{R}\frac{1}{(1-D)^2} \tag{4}$$

Figure 5(a) provides a comparative evaluation of the boost converter's voltage gain under ideal and non-ideal operating conditions. The results highlight a pronounced divergence between the ideal and non-ideal curves, with the discrepancy increasing at higher duty-cycle values. Moreover, the practical voltage gain is strongly influenced by variations in output power and component characteristics. Figures 5(b)–(e) further illustrate the impact of these factors, showing that fluctuations in output power have the most significant effect on the non-ideal voltage gain. These observations indicate that simply increasing the duty cycle is neither an efficient nor a practical approach to achieving high voltage gain. Therefore, it is necessary to explore alternative converter topologies and techniques capable of providing higher voltage gains while mitigating efficiency loss and excessive semiconductor stress.

Building on the foundational overview of classical converter topologies, the following subsections focus on advanced non-isolated DC–DC converters. These improved designs are examined with particular emphasis on how they

TABLE 1. Summary of the features in the presented topologies of Fig. 1.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	I_S
Boost	Purely continuous	Discontinuous	+	Step-up	equal to V_o	less than I_{in}
Buck-boost	Discontinuous	Discontinuous	−	Step-up/down	More than V_o	equal to I_{in}
Cuk	Purely continuous	Purely continuous	−	Step-up/down	More than V_o	equal to I_{in}
SEPIC	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	equal to I_{in}
Zeta	Discontinuous	Purely continuous	+	Step-up/down	More than V_o	equal to I_{in}

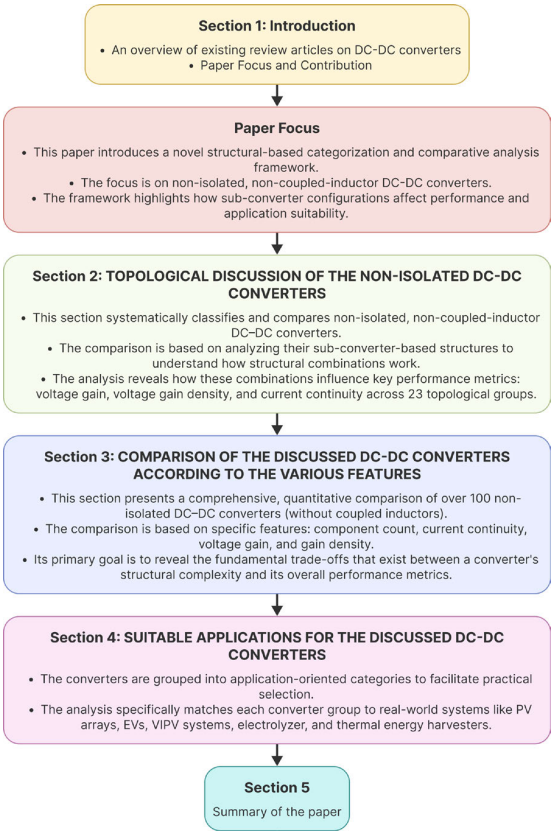

FIGURE 1. Structure of this study.

overcome the limitations and capitalize on the advantages of the classical topologies discussed previously. To provide a systematic analysis, the improved topologies have been categorized into 23 distinct groups according to their unique structural characteristics. Within each group, the benefits and drawbacks of the respective topologies are evaluated in detail, with explicit identification of the specific challenges inherent to classical converters that each design addresses.

A. FIRST GROUP OF NON-ISOLATED DC–DC CONVERTERS

The first family of improved non-isolated topologies is illustrated in Fig. 6. All converters within this group share a common voltage gain characteristic, which can be mathematically expressed as follows:

$$\frac{V_o}{V_{in}} = \left(\frac{D}{1-D}\right)^2 \tag{5}$$

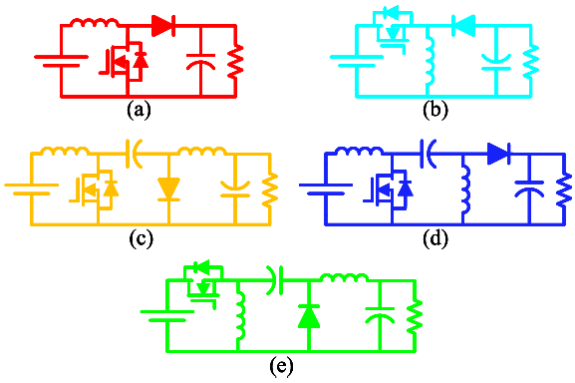

FIGURE 2. (a) Boost converter, (b) buck-boost converter, (c) Cuk converter, (d) SEPIC converter, (e) Zeta converter.

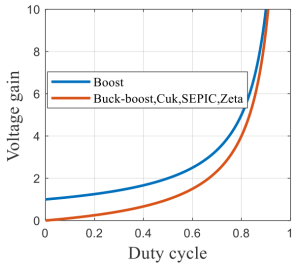

FIGURE 3. Voltage gain comparison of the presented topologies in Fig. 1.

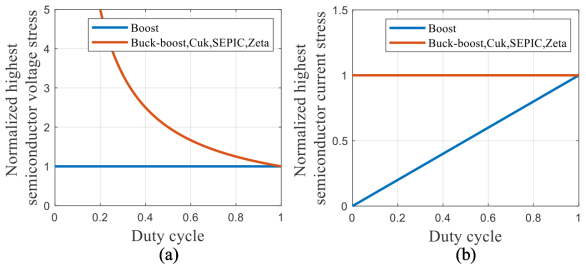

FIGURE 4. Semiconductors' normalized highest: (a) voltage stress, (b) current stress.

The converter topologies presented in this family provide a significantly broader range of voltage gains in both step-up and step-down modes compared with the conventional buck–boost, Ćuk, SEPIC, and Zeta converters, as illustrated in Fig. 7. However, when compared to the classical boost converter, these topologies exhibit certain limitations. In particular, for duty cycles below 62%, the voltage gain achieved by these converters remains lower than that of the boost

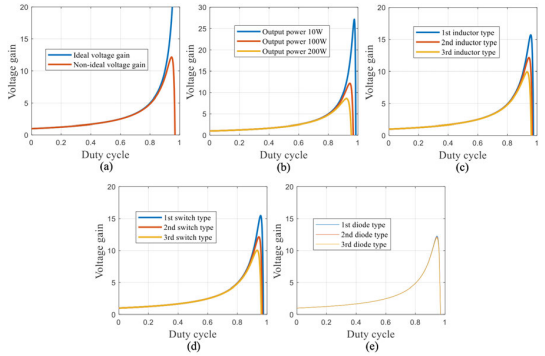

FIGURE 5. (a) Comparison of the ideal and non-ideal voltage gains, Voltage gain behavior according to the change of (b) output power, (c) inductor type, (d) switch type, (e) diode type.

converter (see Fig. 8(a)), indicating that within this operating range, they do not offer a substantial improvement in voltage amplification over the traditional boost topology.

The input current characteristics of these improved converters are primarily determined by the topology employed in their first stage. For example, the converter shown in Fig. 6(a) utilizes a standard buck–boost topology at the first stage, resulting in a discontinuous input current. In contrast, the topologies illustrated in Figs. 6(b) and 6(c) incorporate modified buck–boost structures at both stages, which ensures continuous input current. Similarly, the converter in Fig. 6(d) achieves continuous input current through a modified buck–boost first stage; however, the use of a conventional buck–boost in the second stage increases the input current ripple. The topologies in Figs. 6(e) and 6(f) integrate a boost converter at the first stage combined with a converter exhibiting continuous output current at the second stage, thereby maintaining continuous currents at both the input and output. It is also important to note that the theoretical voltage gain, obtained by multiplying the gains of the sub-converters, is generally higher than the actual measured voltage gain of the complete converter due to non-idealities and parasitic effects.

Despite their benefits, the topologies in this family share several notable drawbacks. A primary concern is the elevated voltage stress imposed on the semiconductor devices, which exceeds the converter's output voltage. Another significant limitation is their voltage-gain performance relative to the number of components employed. These converters require at least twice the number of components compared with a conventional boost converter, yet they deliver lower voltage gain for duty cycles below 62%. As a result, Fig. 8(b) demonstrates that these topologies exhibit a lower voltage-gain density than the classical boost converter. A detailed summary of the advantages and disadvantages of these improved converters is presented in Table 2.

B. SECOND GROUP OF NON-ISOLATED DC–DC CONVERTERS

The converter topologies discussed in [45], [46], [47], [48], [49], and [50] are illustrated in Figs. 11 through 15. The

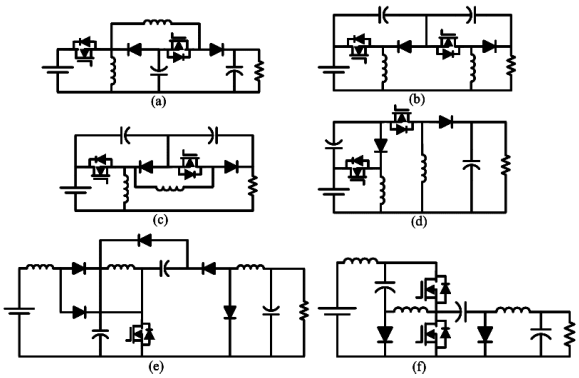

FIGURE 6. The proposed topology in: (a) [40], (b) [41], (c) [42], (d) [43], (e) [44], and (f) [45].

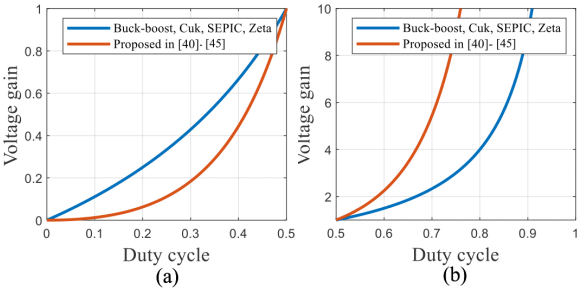

FIGURE 7. Voltage gain comparison of the buck-boost, Cuk, SEPIC, and zeta converters with proposed topologies in [40], [41], [42], [43], [44], [45], [46], [47], and [48] in: (a) step-down mode, (b) step-up mode.

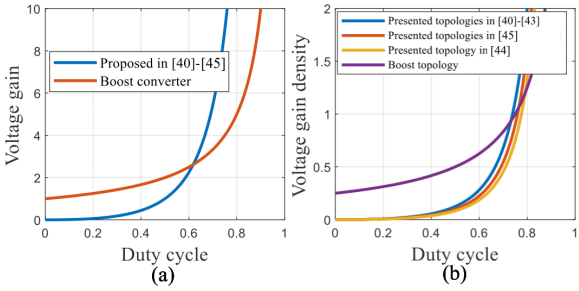

FIGURE 8. Comparison of (a) Voltage gain in the boost converter with the proposed topologies in [40], [41], [42], [43], [44], and [45], (b) voltage gain density.

TABLE 2. Summary of the features in the presented topologies of Fig. 7.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[40]	Discontinuous	Discontinuous	+	Step-up/down	More than V_o	$\left(\frac{D}{1-D}\right)^2$
[41]	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	$\left(\frac{D}{1-D}\right)^2$
[42]	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	$\left(\frac{D}{1-D}\right)^2$
[43]	Continuous	Discontinuous	+	Step-up/down	More than V_o	$\left(\frac{D}{1-D}\right)^2$
[44]	Purely continuous	Purely continuous	−	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[45]	Purely continuous	Purely continuous	+	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$

corresponding voltage gain characteristics of these topologies are given as follows:

$$\frac{V_o}{V_{in}} = \frac{D}{(1-D)^2} \tag{6}$$

Based on this equation, Fig. 10(a) compares the voltage gain of the converters discussed in [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], and [50] with the classical boost converter. As illustrated, the topologies presented in [46], [47], [48], [49], and [50] achieve higher voltage gains than those in [40], [41], [42], [43], [44], and [45] across the entire duty-cycle range. However, for duty cycles below 50%, the voltage gain of the converters in [46], [47], [48], [49], and [50] remains lower than that of the boost converter. This limitation is particularly noteworthy given that the topologies in [46], [47], [48], [49], and [50] employ a larger number of components compared with the simple boost converter. To account for this, Fig. 10(b) presents a comparison of voltage-gain density between the boost converter and the topologies in [46], [47], [48], [49], and [50]. The curves indicate that, for duty cycles below 70%, the boost converter exhibits higher voltage-gain density. These results suggest that, despite their increased complexity, the topologies in [46], [47], [48], [49], and [50] do not offer a substantial improvement in voltage gain relative to the conventional boost converter.

The topology shown in Fig. 9(a) combines a boost converter in the first stage with a Ćuk converter in the second stage. Owing to the low-side switch configuration of both sub-converters, the switch of the first stage can be eliminated, resulting in an overall single-switch architecture. The use of a boost stage at the input and a Ćuk stage at the output ensures continuous currents at both the input and output terminals. Additionally, the incorporation of the Ćuk converter at the output stage inverts the output voltage polarity. However, the maximum voltage stress on the semiconductor devices exceeds the output voltage, similar to the stress observed in a standalone Ćuk converter.

The topology presented in [47], depicted in Fig. 9(b), employs a boost converter as the first stage and a SEPIC converter as the second stage. This configuration inherits all the inherent limitations of the SEPIC topology. Similar to the topology in Fig. 9(a), this design maintains a single-switch structure, preserving simplicity despite its two-stage configuration.

The topology presented in [48] employs a modified boost converter in the first stage. The use of this modified boost configuration increases the input current ripple; however, the overall input current remains continuous due to the second stage, which utilizes a modified buck–boost converter with inherently continuous input current. In comparison, a standard boost topology exhibits a discontinuous input current.

The topology in [49], shown in Fig. 9(d), consists of a modified buck–boost converter at the input stage followed by a boost converter in the second stage. This arrangement ensures a fully continuous input current, although the output current becomes discontinuous because of the boost stage. Furthermore, the use of a buck–boost topology at the input stage introduces elevated voltage stress on the semiconductor devices.

TABLE 3. Summary of the features in the presented topologies of Figs. 9.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[46]	Purely continuous	Purely continuous	–	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[47]	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[48]	Continuous	Disontinuous	–	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[49]	Purely continuous	Discontinuous	–	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[50]	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$

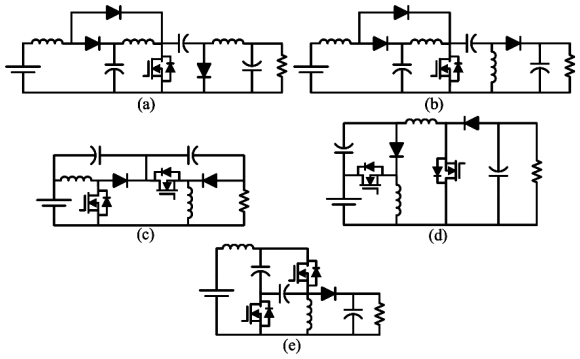

FIGURE 9. The presented topologies in: (a) [46], (b) [47], (c) [48], (d) [49], and (e) [50].

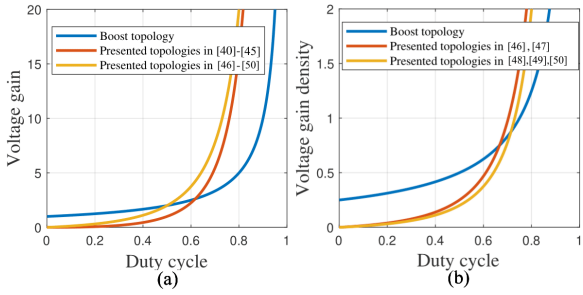

FIGURE 10. Comparison of the boost topology with the presented topologies in [46], [47], [48], [49], and [50]: (a) voltage gain, (b) voltage gain density.

The topology in [50], illustrated in Fig. 9(e), integrates a boost converter at the input and a buck–boost converter at the output. While the input current remains continuous due to the boost stage, the output current is discontinuous because of the buck–boost stage. Similarly, the use of the buck–boost converter contributes to high voltage stress on the semiconductors.

A notable commonality among the topologies in [46], [47], [48], [49], and [50] is that the overall voltage gain of the complete converter equals the product of the voltage gains of the constituent sub-converters, a feature not achieved by all converters discussed in the previous subsection. A comprehensive summary of the advantages and disadvantages of these topologies is presented in Table 3.

C. THIRD GROUP OF NON-ISOLATED DC–DC CONVERTERS

The converter topologies presented in [51], [52], [53], [54] are illustrated in Fig. 11. The corresponding voltage gain

TABLE 4. Summary of the features in the presented topologies of Figs. 18 and 19.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[51]	Continuous	Discontinuous	–	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[52]	Purely continuous	Purely continuous	–	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[53]	Purely continuous	Purely continuous	–	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[54]	Continuous	Purely continuous	+	Step-up/down	More than V_o	$\left(\frac{D}{1-D}\right)^2$

characteristics of these topologies are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{D(2-D)}{(1-D)^2} \tag{7}$$

The voltage gain of the topologies presented in [51], [52], [53], and [54] is compared with that of the classical boost converter and the previously discussed topologies in Fig. 12(a). As shown, these topologies achieve higher voltage gain than the converters in [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], and [50]. However, at low duty-cycle percentages, the voltage gain of the boost converter remains superior to that of the topologies in [51], [52], [53], and [54]. This advantage becomes even more pronounced when considering voltage-gain density, as illustrated in Fig. 12(b), which shows that the boost converter exhibits higher voltage-gain density than the topologies in [51], [52], [53], and [54] for duty cycles below 60

The topologies in Figs. 11(a), (c), and (d) employ a modified boost converter at the input stage. In Fig. 11(a), a buck–boost converter is used in the second stage, which increases the input current ripple and results in a discontinuous output current. In contrast, the topologies in [52] and [53] use a Ćuk converter at the second stage, ensuring continuous output current, inverting the output voltage polarity, and producing semiconductor voltage stress that exceeds the output voltage.

The topology in Fig. 11(d) also employs a modified boost converter at the input, followed by a Zeta converter at the output stage, which provides continuous output current. Nonetheless, the maximum voltage stress on the semiconductor devices in all the topologies shown in Fig. 11 exceeds the output voltage.

It is noteworthy that the topologies in Fig. 11 achieve overall voltage gains greater than the product of their sub-converter gains, a feature not observed in all previously discussed designs. A detailed summary of the advantages and disadvantages of the topologies in [51], [52], [53], and [54] is presented in Table 4.

D. FOURTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The converter topologies presented in [55], [56], [57], [58], [59], [60], and [61] are illustrated in Fig. 13. The corresponding voltage gain characteristics of these topologies are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \tag{8}$$

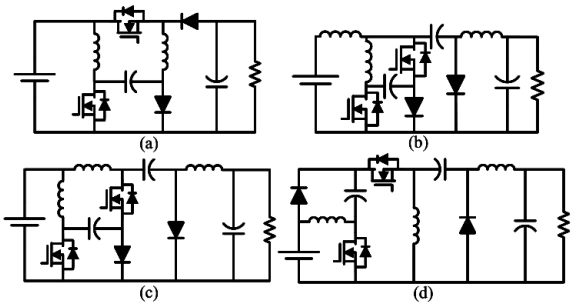

FIGURE 11. The presented topologies in: (a) [51], (b) [52], (c) [53], and (d) [54].

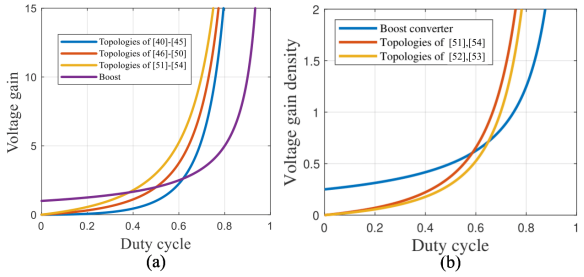

FIGURE 12. Comparison of the boost topology with the presented topologies in [51], [52], [53], and [54]: (a) voltage gain, (b) voltage gain density.

The voltage gain of the converters presented in [55], [56], [57], [58], [59], [60], and [61] is compared with that of the classical boost converter and previously discussed topologies in Fig. 14(a). As shown, these converters achieve higher voltage gains than both the boost converter and the topologies in [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], and [54]. However, this advantage diminishes when voltage-gain density is considered. Fig. 14(b) presents a comparison of voltage-gain density between the boost converter and the topologies in [55], [56], [57], [58], [59], [60], and [61], indicating that for duty cycles below 50

The topology in Fig. 13(a) represents an improved boost converter, with modifications to the classic boost structure. In this design, the input current is continuous while the output current remains discontinuous. The maximum voltage stress on the semiconductor devices exceeds the output voltage, similar to classical boost converters.

The topologies in [56], [57], [58], [59], [60], and [61] generally employ a modified boost converter in the first stage, except for [59]. In [56] and [57], the modified boost topology is also used in the second stage, which increases input current ripple. However, the combined voltage of the input and intermediate capacitors forms the output voltage, reducing voltage stress on the output capacitors and allowing them to serve a dual function, thereby improving overall efficiency. The topology in [58] uses a standard boost converter at the second stage, resulting in lower input current ripple compared with [56] and [57]. The maximum voltage stress on the semiconductors in [56], [57], and [58] is equal to the output voltage.

TABLE 5. Summary of the features in the presented topologies of Fig. 13.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[55]	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	$\left(\frac{D}{1-D}\right)^2$
[56]	Continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{1}{(1-D)^2}$
[57]	Continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{1}{(1-D)^2}$
[58]	Continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{1}{(1-D)^2}$
[59]	Purely continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{1}{(1-D)^2}$
[60]	Purely continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{1}{(1-D)^2}$
[61]	Continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{1}{(1-D)^2}$

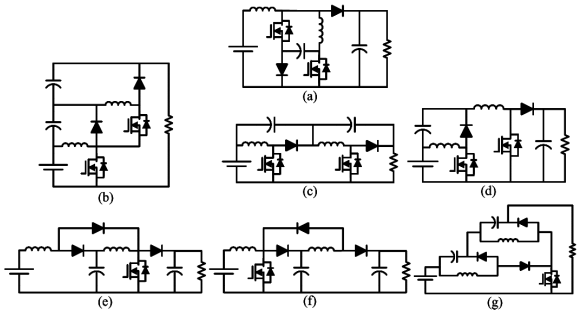

FIGURE 13. The presented topologies in: (a) [55], (b) [56], (c) [57], (d) [58], (e) [59], (f) [60], and (g) [61].

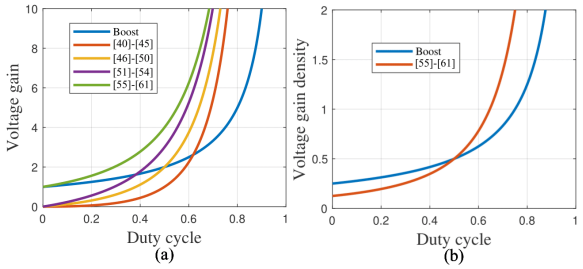

FIGURE 14. Comparison of the boost topology with the presented topologies in [55], [56], [57], [58], [59], [60], and [61]: (a) voltage gain, (b) voltage gain density.

The topologies in [59], [60], and [61] are single-switch designs featuring two boost stages at the input and output. The input current is fully continuous in [59] and [60], whereas [61] exhibits significantly higher input current ripple. Notably, the maximum voltage stress on the semiconductor devices in [59], [60], and [61] is equal to the output voltage. Among these, the topology in [60] is the first to achieve a switch voltage stress lower than the output voltage.

In all topologies from [55], [56], [57], [58], [59], [60], and [61], the overall voltage gain of the converter is equal to the product of the gains of the sub-converters. A comprehensive summary of the advantages and disadvantages of these topologies is provided in Table 5.

E. FIFTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies discussed in this subsection are based on the positive output super lift Luo converter (POSLLC). The structure of the POSLLC is illustrated in Fig. 15(a). As shown, this converter includes one additional capacitor and diode compared with the classical boost converter. The POSLLC employs a voltage-lift technique to achieve higher voltage gain than the boost topology. In this approach, during one operational mode, certain capacitors are connected in parallel with other capacitors or voltage sources. In the subsequent mode, these previously parallel capacitors are reconfigured in series, resulting in a summed voltage that contributes to the overall output. The resulting voltage gain of the POSLLC is expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2-D}{1-D} \tag{9}$$

Based on this equation, Fig. 16(a) compares the voltage gain of the POSLLC with that of the classical boost converter. As illustrated, the POSLLC achieves higher voltage gain than the boost converter across the entire duty-cycle range. However, when considering voltage-gain density (Fig. 16(b)), the boost converter exhibits superior performance for duty cycles below 50

It is noteworthy that the maximum voltage stress on the semiconductor devices in the POSLLC remains below the output voltage. This represents a significant advantage, in addition to providing higher voltage gain than the boost converter. Nonetheless, the achieved voltage gain is not sufficiently high for certain high-gain applications, indicating the need for further enhancement or integration with other topologies.

The topologies presented in [62], [63], and [64], illustrated in Figs. 15(b)–(d), combine the boost converter with the POSLLC. In these designs, the boost converter serves as the first stage, while the POSLLC is employed in the second stage. The input current is continuous in all of these topologies; however, the input current ripple is higher in [62] compared with [63] and [64]. The topologies in [62] and [64] utilize two switches, whereas the topology in [63] maintains a single-switch configuration. The corresponding voltage gains of the converters in [62], [63], and [64] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{3-3D+D^2}{(1-D)^2} \tag{10}$$

$$\frac{V_o}{V_{in}} = \frac{2-D}{(1-D)^2} \tag{11}$$

$$\frac{V_o}{V_{in}} = \frac{2-D}{(1-D)^2} \tag{12}$$

In the topology presented in [62], the overall voltage gain exceeds the product of the gains of the individual sub-converters. In contrast, for the topologies in [63] and [64], the overall voltage gain is equal to the product of the sub-converters' gains. Based on these relationships, Fig. 17(a) compares the voltage gain of the topologies in [62], [63], [64] with that of the classical boost converter, showing that all three topologies achieve higher voltage gain than the boost converter. Furthermore, Fig. 17(b) illustrates that the voltage-gain density of these topologies is also superior to that of the boost converter. Notably, the semiconductor voltage-stress challenge is effectively addressed in [63].

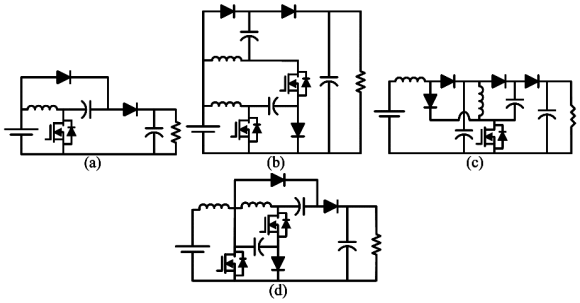

FIGURE 15. The presented topologies in: (a) super lift Luo (POSLLC), (b) [62], (c) [63], (d) [64].

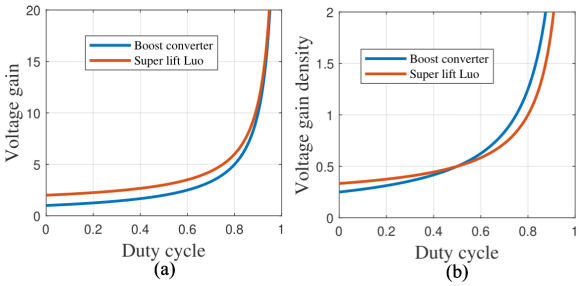

FIGURE 16. Comparison of the boost and POSLLC: (a) voltage gain, (b) voltage gain density.

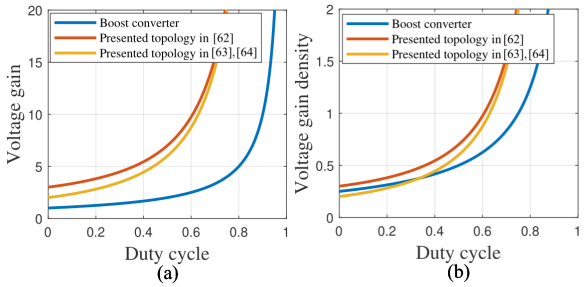

FIGURE 17. Comparison of the boost topology with the presented topologies in [62], [63], and [64]: (a) voltage gain, (b) voltage gain density.

TABLE 6. Summary of the features in the presented topologies of Fig. 15.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[62]	Continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{2-D}{(1-D)^2}$
[63]	Purely continuous	Discontinuous	+	Step-up	Less than V_o	$\frac{2-D}{(1-D)^2}$
[64]	Purely continuous	Discontinuous	+	Step-up	Equal to V_o	$\frac{2-D}{(1-D)^2}$

A comprehensive summary of the key features and performance characteristics of the topologies in [62], [63], and [64] is presented in Table 6.

F. SIXTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [65], [66], [67], and [68] are illustrated in Fig. 18. These converters combine different classical topologies: boost and buck–boost (Fig. 18(a)), boost and boost (Fig. 18(b)), boost and SEPIC (Fig. 18(c)), and boost and Zeta (Fig. 18(d)). Notably, these designs employ the voltage-lift technique without utilizing the POSLLC. The

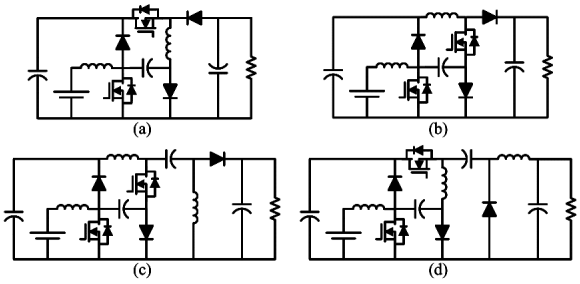

FIGURE 18. The presented topologies in: (a) [65], (b) [66], (c) [67], and (d) [68].

TABLE 7. Summary of the features in the presented topologies of Fig. 18.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[65]	Purely continuous	Discontinuous	−	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[66]	Purely continuous	Discontinuous	+	Step-up	More than V_o	$\frac{1}{(1-D)^2}$
[67]	Purely continuous	Discontinuous	+	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$
[68]	Purely continuous	Purely continuous	+	Step-up/down	More than V_o	$\frac{D}{(1-D)^2}$

use of a boost converter at the first stage ensures continuous input current. In the topology presented in [68], the Zeta converter in the second stage provides continuous output current.

All of the converters in this subsection use two switches, which is considered a drawback due to increased complexity and cost. Moreover, the challenge of semiconductor voltage stress persists, with the maximum voltage stress exceeding the output voltage in each topology. The corresponding voltage gains of the topologies in [65], [66], [67], and and [68] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2D}{(1-D)^2} \tag{13}$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{(1-D)^2} \tag{14}$$

$$\frac{V_o}{V_{in}} = \frac{D(1+D)}{(1-D)^2} \tag{15}$$

$$\frac{V_o}{V_{in}} = \frac{D(1+D)}{(1-D)^2} \tag{16}$$

It is noteworthy that the overall voltage gain of the converters in [65], [66], [67], and [68] exceeds the product of the gains of their sub-converters. Based on the corresponding equations, Fig. 19(a) compares the voltage gain of these topologies with that of the classical boost converter, showing that all four converters achieve higher voltage gain than the boost converter. However, when voltage-gain density is considered (Fig. 19(b)), these topologies do not demonstrate a significant advantage over the boost converter. A comprehensive summary of the advantages and disadvantages of this group of converters is provided in Table 7.

G. SEVENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

Another approach to implementing the voltage-lift technique is through the use of a Voltage Multiplier Cell (VMC). VMCs

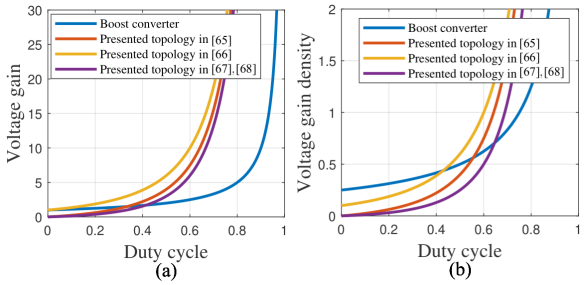

FIGURE 19. Comparison of the boost topology with the presented topologies in [65], [66], [67], and [68]: (a) voltage gain, (b) voltage gain density.

typically consist of combinations of diodes and inductors, diodes and capacitors, or diodes, capacitors, and inductors, enabling voltage boosting and increasing the voltage gain of the underlying converter topology.

The topologies proposed in [69], [70], [71], [72], and [73] are illustrated in Fig. 20. In these designs, an inductor-based VMC replaces the inductor in the base topology, including boost converters (Figs. 20(a)–(c)), a buck–boost converter (Fig. 20(d)), and a POSLLC (Fig. 20(e)). The use of these VMCs ensures continuous input current in [69], [70], [71], and [73], although it leads to increased input current ripple. Importantly, replacing the base inductors with VMCs does not mitigate semiconductor voltage stress; the maximum voltage stress relative to the output voltage remains the same as in the corresponding base topology. The resulting voltage gains of the topologies in [69], [70], [71], [72], and [73] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{17}$$

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \tag{18}$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} \tag{19}$$

$$\frac{V_o}{V_{in}} = \frac{D(2-D)}{(1-D)^2} \tag{20}$$

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{21}$$

The overall voltage gain of each topology in [69], [70], [71], [72], and [73] exceeds that of its corresponding base converter. Fig. 21(a) compares the voltage gain of these topologies with the classical boost converter. Except for the topology in [72], all of the presented converters achieve higher voltage gain than the boost converter across the entire duty-cycle range. Fig. 21(b) shows the comparison of voltage-gain density, indicating that for duty cycles below 50%, the boost converter exhibits superior voltage-gain density relative to the topologies in [69], [70], [71], [72], and [73]. This implies that while these converters may outperform the boost converter at higher duty-cycle percentages, such operating points are generally not desirable for practical applications.

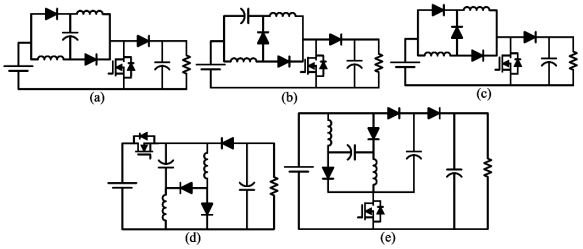

FIGURE 20. The presented topologies in: (a) [69], (b) [70], (c) [71], (d) [72], and (e) [73].

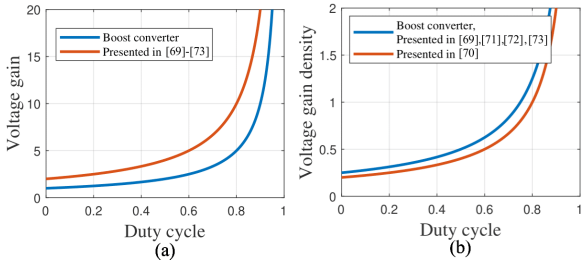

FIGURE 21. Comparison of the boost topology with the presented topologies in [69], [70], [71], [72], and [73]: (a) voltage gain, (b) voltage gain density.

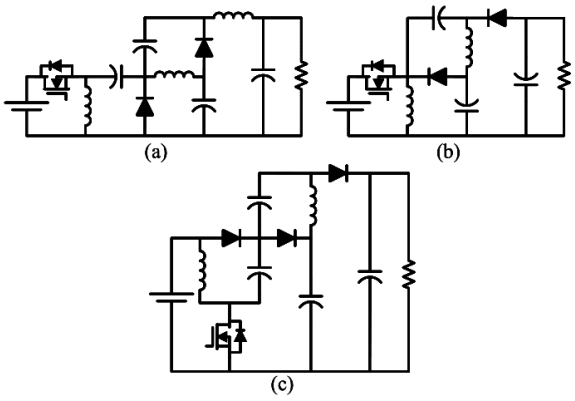

FIGURE 22. The presented topologies in: (a) [74], (b) [75], and (c) [76].

TABLE 8. Summary of the features in the presented topologies of Fig. 24.

Topologies	I_{in}	I_o	Output polarity	Gain behaviour	$Max(V_S or V_D)$	Subconverters' gain production
[77]	Purely continuous	Discontinuous	+	Step-up	Less than V_o	$\frac{2}{1-D}$
[78]	Purely continuous	Discontinuous	+	Step-up	Less than V_o	$\frac{2}{1-D}$
[79]	Purely continuous	Discontinuous	+	Step-up	Less than V_o	$\frac{2}{1-D}$
[80]	Purely continuous	Discontinuous	+	Step-up	Less than V_o	$\frac{2}{1-D}$
[81]	Purely continuous	Discontinuous	+	Step-up	Less than V_o	$\frac{2}{1-D}$

H. EIGHTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

This section discusses the proposed topologies in [74], [75], and [76], which are illustrated in Fig. 22. The topology in [74] is based on a Zeta converter, [75] is based on a buck–boost converter, and [76] is based on a POSLLC. All of these designs incorporate a diode–capacitor–inductor-based Voltage Multiplier Cell (VMC) at the output stage of

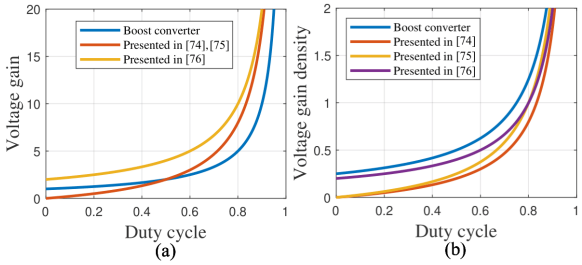

FIGURE 23. Comparison of the boost topology with the presented topologies in [74], [75], and [76]: (a) voltage gain, (b) voltage gain density.

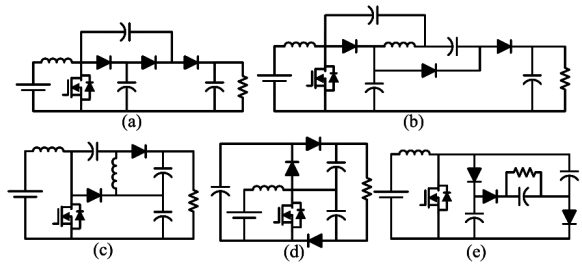

FIGURE 24. The presented topologies in: (a) [77], (b) [78], (c) [79], (d) [80], and (e) [81].

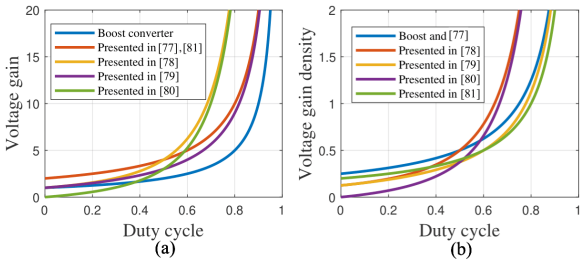

FIGURE 25. Comparison of the boost topology with the presented topologies in [77], [78], [79], [80], and [81]: (a) voltage gain, (b) voltage gain density.

the base topology. As a result, the inherent advantages and disadvantages of the respective base topologies are largely preserved. The corresponding voltage gains of the topologies in [74], [75], and [76] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2D}{1-D} \tag{22}$$

$$\frac{V_o}{V_{in}} = \frac{2D}{1-D} \tag{23}$$

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{24}$$

The provided voltage gains indicate that, for the buck–boost-based topology, the overall voltage gain equals the sum of the gains of its base sub-converters. This feature is achieved through the incorporation of a VMC at the output stage of the base topologies. Importantly, the use of the VMC also addresses the challenge of semiconductor voltage stress. Based on these voltage gains, Fig. 23(a) compares the voltage gain of the topologies in [74], [75], and [76] with that of the classical boost converter, showing that the POSLLC-based topology in [76] achieves higher voltage gain than the boost converter across the entire duty-cycle range. Fig. 23(b) presents a comparison of voltage-gain density, illustrating that the boost converter maintains superior voltage-gain density relative to all other discussed topologies for the full duty-cycle range.

I. NINTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in Fig. 24 combine various Voltage Multiplier Cells (VMCs) with a boost converter, with all VMCs positioned at the output stage of the base converter. As shown in Fig. 24, the topologies in [77], [80], and [81] employ diode–capacitor-based VMCs at the output of a boost converter. Notably, the VMCs used in [77] and [80] eliminate the common ground connection between the load and the input source. In contrast, Figs. 24(b) and (c) illustrate topologies that use inductor–diode–capacitor-based VMCs with a boost converter. These configurations preserve the common ground between the load and the input source, though they require a greater number of inductors compared with the conventional boost topology.

It is noteworthy that the input current remains fully continuous in all of these topologies due to the boost converter at the first stage. Furthermore, each topology utilizes only a single switch with a simple drive circuit. The semiconductor voltage-stress challenge is effectively addressed, with the maximum voltage stress reduced to half of the output voltage. The corresponding voltage gains of all the aforementioned converters are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{25}$$

Based on the corresponding equations, Fig. 25(a) compares the voltage gain of the topologies in [77], [78], [79], [80], and [81] with that of the classical boost converter. As shown, all of these topologies achieve higher voltage gain than the boost converter across the entire duty-cycle range. In terms of voltage-gain density, the topologies in [77] and [79], [80], and [81] exhibit values comparable to the boost converter, whereas the topology in [78] demonstrates lower voltage-gain density relative to the others. A comprehensive summary of the advantages and disadvantages of these converters is provided in Table 8.

J. TENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies proposed in [82] and [83] are illustrated in Fig. 26. Both designs are based on the Cuk converter, with modifications implemented through the use of Voltage Multiplier Cells (VMCs). Specifically, [82] employs a diode–capacitor–inductor-based VMC, while [83] uses a diode–capacitor-based VMC to replace the diode in the original Cuk topology. These modifications do not affect the inherent advantages or disadvantages of the input stage. Importantly, the semiconductor voltage-stress challenge is resolved in both topologies. Additionally, the VMC in [83] eliminates the common ground between the load and the input source, while

the continuity of both input and output currents is preserved. The resulting voltage gains of the topologies in [82] and [83] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2D}{1-D} \tag{26}$$

$$\frac{V_o}{V_{in}} = \frac{D(1+D)}{1-D} \tag{27}$$

The voltage gain achieved by each topology in [82] and [83] exceeds that of its corresponding base converter. Based on these relationships, Fig. 27(a) compares the voltage gain of these topologies with that of the classical boost converter. As shown, for duty cycles below 50%, the boost converter provides higher voltage gain than the topologies in [82] and [83]. Similarly, the comparison of voltage-gain density in Fig. 27(b) indicates that the boost converter maintains superior performance relative to [82] and [83] across the entire duty-cycle range.

K. ELEVENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topology presented in [84] is illustrated in Fig. 28 and is based on a SEPIC converter. In this design, a diode–capacitor–inductor-based Voltage Multiplier Cell (VMC) replaces the second inductor of the standard SEPIC topology. This modification does not affect the inherent characteristics of the SEPIC converter, namely the continuity of the input current and the discontinuity of the output current. Importantly, the semiconductor voltage-stress challenge is effectively addressed in this topology. The resulting voltage gain is expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2D}{1-D} \tag{28}$$

Based on the corresponding equation, Fig. 29(a) compares the voltage gain of the topology in [84] with that of the classical boost converter. As shown, [84] achieves higher voltage gain than the boost converter for duty cycles exceeding 50%. However, this increase in voltage gain is not necessarily desirable, as indicated by the voltage-gain density comparison in Fig. 29(b), which demonstrates that the boost converter maintains more favorable voltage-gain density across practical duty-cycle ranges.

L. TWELFTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

This group comprises topologies that employ an inductor-based Voltage Multiplier Cell (VMC) at the input stage of the base converter, replacing the original inductor, and a diode–capacitor-based (Figs. 30(a), (b), and (d)) or diode–capacitor–inductor-based (Fig. 30(c)) VMC at the output stage. These designs maintain a common ground connection between the load and the input source. The resulting voltage gains of the topologies in [85], [86], [87], and [88] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{4}{1-D} \tag{29}$$

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{30}$$

$$\frac{V_o}{V_{in}} = \frac{2+D}{1-D} \tag{31}$$

$$\frac{V_o}{V_{in}} = \frac{4}{1-D} \tag{32}$$

As shown in Fig. 31(a), the voltage gains of the topologies in [85], [86], [87], and [88] exceed that of the classical boost converter. In terms of voltage-gain density (Fig. 31(b)), the topologies in [85] and [88] outperform the boost converter across the entire duty-cycle range.

The use of a VMC at the output stage effectively addresses the challenge of semiconductor voltage stress, reducing the maximum voltage stress to half of the output voltage in all four topologies. Additionally, incorporating an inductor-based VMC at the input stage ensures continuous input current, albeit with increased ripple. Importantly, this technique does not alter the number of switches or the complexity of their drive circuits relative to the base topologies.

M. THIRTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [89], [90], [91], [92], and [93], illustrated in Fig. 32, employ an inductor-based Voltage Multiplier Cell (VMC) at the input stage to replace the original inductor of the boost converter, as well as an additional VMC at the output stage. Notably, these configurations eliminate the common ground connection between the load and the input source. The input-stage VMC maintains continuous input current, although with increased ripple. Meanwhile, the output-stage VMC effectively addresses the challenge of semiconductor voltage stress. The resulting voltage gains of the topologies in [89], [90], [91], [92], and [93] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{4}{1-D} \tag{33}$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{(1-D)^2} \tag{34}$$

$$\frac{V_o}{V_{in}} = \frac{(1+D)^2)}{1-D} \tag{35}$$

$$\frac{V_o}{V_{in}} = 2\frac{1+D}{1-D} \tag{36}$$

$$\frac{V_o}{V_{in}} = \frac{6}{1-D} \tag{37}$$

Fig. 33(a) presents a comparison of the voltage gain for the topologies in [89], [90], [91], [92], and [93] based on the corresponding equations. As shown, all of these topologies achieve higher voltage gain than the classical boost converter. Regarding voltage-gain density (Fig. 33(b)), the topologies

in [89] and [93] demonstrate superior performance compared with the boost converter across the entire duty-cycle range.

N. FOURTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [94], [95], [96], and [97], illustrated in Fig. 34, are primarily based on the boost converter, with the topology in [97] derived from the POSLLC. In all these designs, two combined inductor-based Voltage Multiplier Cells (VMCs) replace the inductor of the base topologies. This modification does not affect the output stage, the number of switches or their driving circuitry, the challenge of semiconductor voltage stress, or the output polarity. The resulting voltage gains of the topologies in [94], [95], [96], and [97] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{38}$$

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^3} \tag{39}$$

$$\frac{V_o}{V_{in}} = \frac{1+2D}{1-D} \tag{40}$$

$$\frac{V_o}{V_{in}} = \frac{2+D}{1-D} \tag{41}$$

Fig. 35(a) compares the voltage gain of the topologies in [94], [95], [96], and [97] with that of the classical boost converter. As shown, the voltage gain of the boost converter is lower than that of all the presented topologies across the entire duty-cycle range. However, when considering voltage-gain density (Fig. 35(b)), topologies [94] and [95] demonstrate superior performance relative to the boost converter for duty cycles exceeding 50

O. FIFTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

This subsection covers the topologies presented in [98], [99], [100], [101], and [102], illustrated in Fig. 36. Each of these topologies employs two Voltage Multiplier Cells (VMCs) at the output stage of the base converter, including boost converters in [98], [99], and [100], a buck–boost converter in [101], and a SEPIC converter in [102]. The inherent advantages and disadvantages of the base topologies remain unchanged. Furthermore, the number of switches and their driving circuitry are identical to those of the respective base topologies. The resulting voltage gains of the topologies in [98], [99], [100], [101], and [102] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2-D}{(1-D)^2} \tag{42}$$

$$\frac{V_o}{V_{in}} = \frac{2+D}{1-D} \tag{43}$$

$$\frac{V_o}{V_{in}} = \frac{3}{1-D} \tag{44}$$

$$\frac{V_o}{V_{in}} = \frac{3D}{1-D} \tag{45}$$

$$\frac{V_o}{V_{in}} = \frac{3D}{1-D} \tag{46}$$

Based on the corresponding equations, Fig. 37(a) compares the voltage gain of the topologies in [98], [99], [100], [101], and [102] with that of the classical boost converter. As shown, the boost converter exhibits lower voltage gain than all the presented topologies. Furthermore, the voltage-gain density comparison in Fig. 37(b) highlights the superior performance of topology [98] relative to the others.

P. SIXTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [103], [104], [105], [106], and [107], illustrated in Fig. 38, are based on the boost converter. Each design incorporates an inductor-based Voltage Multiplier Cell (VMC) at the input stage, replacing the original inductor, and two VMCs at the output stage. All converters employ a single switch with a simple drive circuit, similar to the classical boost topology. Despite the increased input current ripple, the input current remains continuous. The inclusion of VMCs at the output stage effectively addresses the semiconductor voltage-stress challenge. Notably, topology [106] eliminates the common ground between the load and the input source. The resulting voltage gains of the topologies in [103], [104], [105], [106], and [107] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{6}{1-D} \tag{47}$$

$$\frac{V_o}{V_{in}} = \frac{6}{1-D} \tag{48}$$

$$\frac{V_o}{V_{in}} = \frac{2-D^2}{D(1-D)^2} \tag{49}$$

$$\frac{V_o}{V_{in}} = \frac{6}{1-D} \tag{50}$$

$$\frac{V_o}{V_{in}} = \frac{(1+D)(2+D)}{1-D} \tag{51}$$

Based on the corresponding equations, Fig. 39(a) compares the voltage gain of the topologies in [103], [104], [105], [106], and [107] with that of the classical boost converter, while Fig. 39(b) presents the comparison of voltage-gain density. As shown, the topologies in [103], [104], [105], [106], and [107] demonstrate superior performance relative to the boost converter in terms of both voltage gain and voltage-gain density.

Q. SEVENTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [108], [109], and [110], illustrated in Fig. 40, employ a combination of three Voltage Multiplier Cells (VMCs) at the output stage of the base converters: a boost converter in Fig. 40(a) and buck–boost converters in Figs. 40(b) and 40(c). All input-side characteristics, including advantages and disadvantages of the base topologies, remain unchanged. The number of

switches and their driving circuits are identical to those of the respective base topologies. The use of VMCs at the output stage effectively addresses the semiconductor voltage-stress challenge. The resulting voltage gains of the topologies in [108], [109], and [110] are expressed as follows:

$$\frac{V_o}{V_{in}} = 2\frac{1+D}{1-D} \tag{52}$$

$$\frac{V_o}{V_{in}} = \frac{4D}{1-D} \tag{53}$$

$$\frac{V_o}{V_{in}} = \frac{3D}{1-D} \tag{54}$$

Figs. 41(a) and 41(b) present the voltage gain and voltage-gain density of the topologies in [108], [109], and [110] based on the corresponding equations. As shown, these topologies achieve higher voltage gain than the classical boost converter. However, the voltage-gain density of these converters remains relatively low, indicating that the improvement in voltage gain comes at the cost of increased component usage or reduced efficiency in practical implementation.

R. EIGHTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topology presented in [121], illustrated in Fig. 42, is based on the classical boost converter and employs a combination of three diode–capacitor–inductor-based Voltage Multiplier Cells (VMCs) in place of the original inductor. This arrangement ensures continuous input current, albeit with increased ripple. Importantly, this modification does not alter the number of switches or the driving circuitry of the base topology, nor does it affect the semiconductor voltage-stress challenge, the common ground connection between the load and input source, or the discontinuity of the output current. The resulting voltage gain of this topology is expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{1}{(1-D)^4} \tag{55}$$

Comparison of the voltage gain of the topology in [121] with that of the classical boost converter, as shown in Fig. 43(a), reveals a rapid increase in voltage gain. However, this non-linear behavior also increases the converter's sensitivity to duty-cycle fluctuations, complicating its control. Fig. 43(b) presents the voltage-gain density comparison with the boost converter. As illustrated, achieving a higher voltage-gain density than the boost converter requires operating at duty cycles above 40

S. NINTEENTH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topology presented in [121], illustrated in Fig. 44, is based on the classical boost converter. It incorporates a combination of two diode–inductor-based Voltage Multiplier Cells (VMCs) at the input stage, replacing the original inductor, and a diode–capacitor VMC at the output stage. The

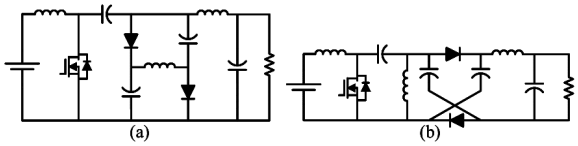

FIGURE 26. The presented topologies in: (a) [82] and (b) [83].

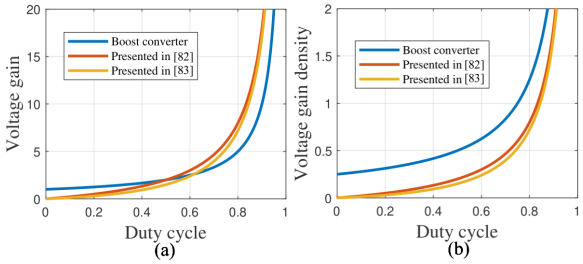

FIGURE 27. Comparison of the boost topology with the presented topologies in [82] and [83]: (a) voltage gain, (b) voltage gain density.

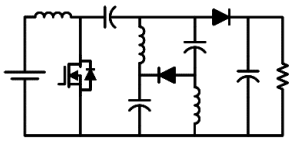

FIGURE 28. The presented topologies in: [84].

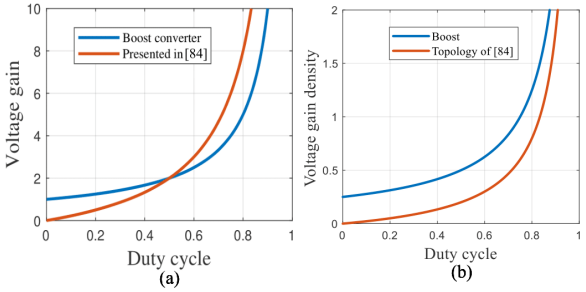

FIGURE 29. Comparison of the boost topology with the presented topologies in [84]: (a) voltage gain, (b) voltage gain density.

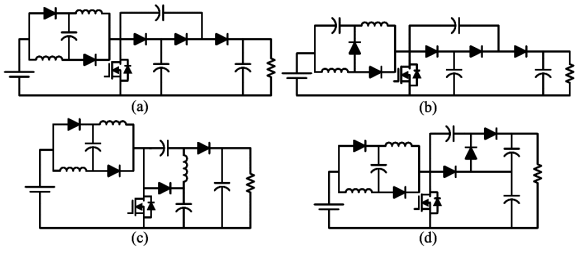

FIGURE 30. The presented topologies in: (a) [85], (b) [86], (c) [87], and (d) [88].

number of switches and the drive circuitry remain identical to those of the base boost converter. This configuration effectively addresses the semiconductor voltage-stress challenge, reducing the maximum voltage stress to half of the output voltage. While the use of two inductor-based VMCs increases input current ripple, it preserves input current continuity. The

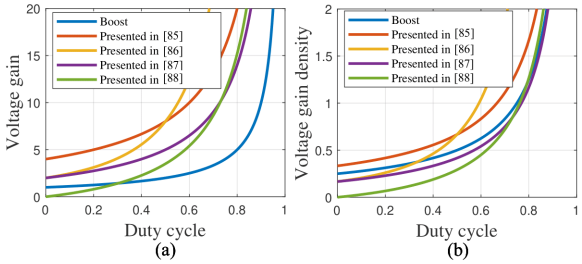

FIGURE 31. Comparison of the boost topology with the presented topologies in [85], [86], [87], and [88]: (a) voltage gain, (b) voltage gain density.

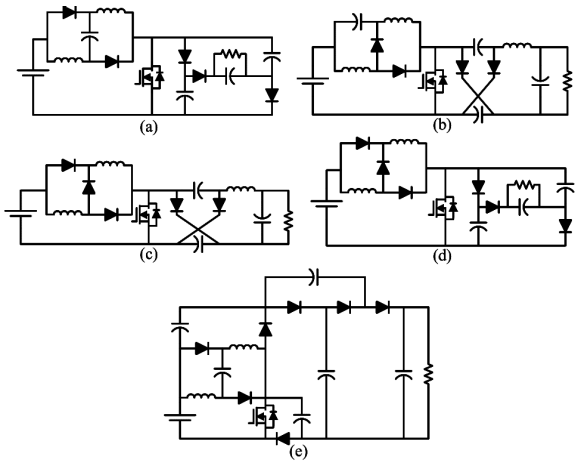

FIGURE 32. The presented topologies in: (a) [89], (b) [90], (c) [91], (d) [92], and (e) [93].

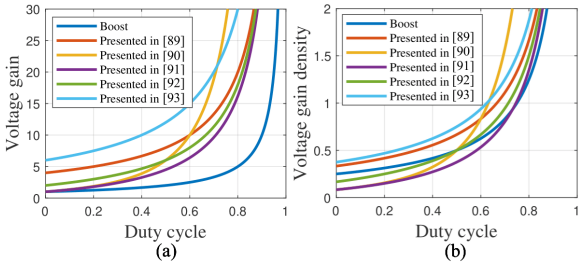

FIGURE 33. Comparison of the boost topology with the presented topologies in [89], [90], [91], [92], and [93]: (a) voltage gain, (b) voltage gain density.

resulting voltage gain of this topology is expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2(1+2D)}{1-D} \tag{56}$$

Fig. 45(a) illustrates that the voltage gain of the topology in [121] exceeds that of the classical boost converter. However, this advantage becomes less significant when considering the voltage-gain density, as shown in Fig. 45(b), where the topology demonstrates comparatively lower performance.

T. TWENTIETH GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in Fig. 46 are cascaded structures that employ a Voltage Multiplier Cell (VMC) at the output of the first stage and another VMC at the input of the second stage. Both topologies utilize a single-switch configuration with a simple drive circuit. They ensure continuous input

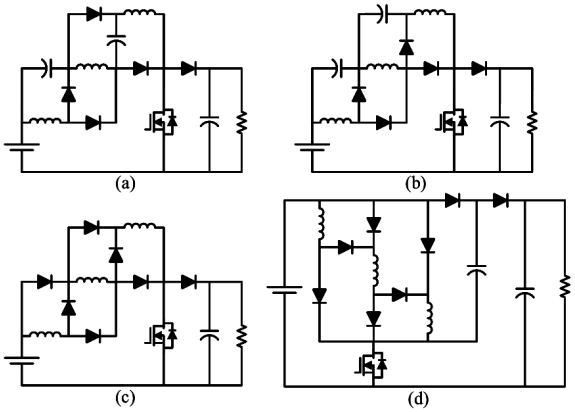

FIGURE 34. The presented topologies in: (a) [94], (b) [95], (c) [96], and (d) [97].

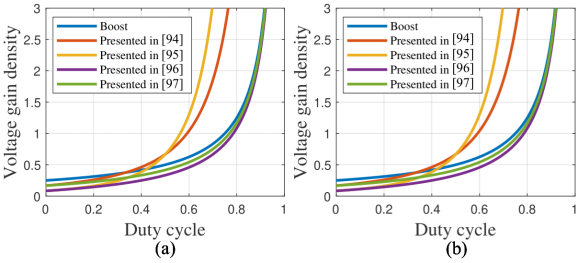

FIGURE 35. Comparison of the boost topology with the presented topologies in [94], [95], [96], and [97]: (a) voltage gain, (b) voltage gain density.

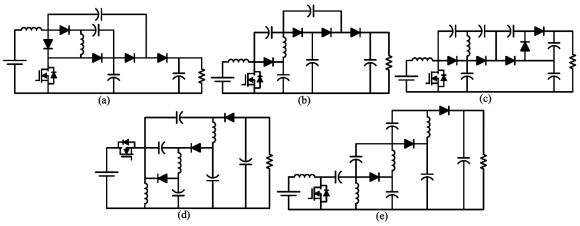

FIGURE 36. The presented topologies in: (a) [98], (b) [99], (c) [100], (d) [101], and (e) [102].

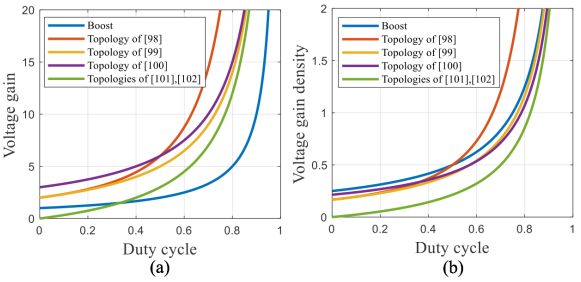

FIGURE 37. Comparison of the boost topology with the presented topologies in [98], [99], [100], [101], and [102]: (a) voltage gain, (b) voltage gain density.

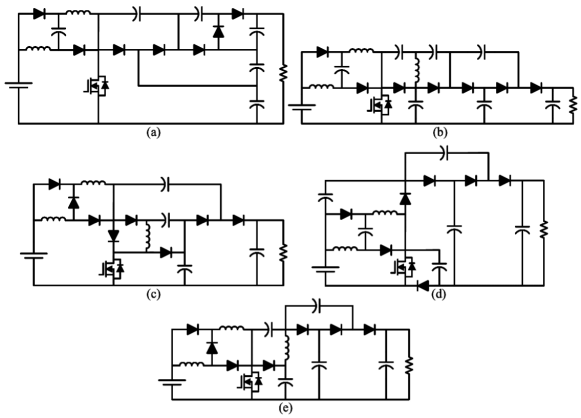

FIGURE 38. The presented topologies in: (a) [103], (b) [104], (c) [105], (d) [93], and (e) [107].

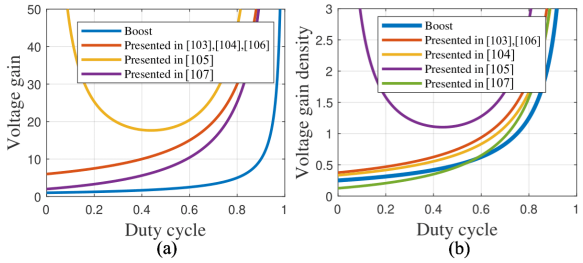

FIGURE 39. Comparison of the boost topology with the presented topologies in [103], [104], [105], [93], and [107]: (a) voltage gain, (b) voltage gain density.

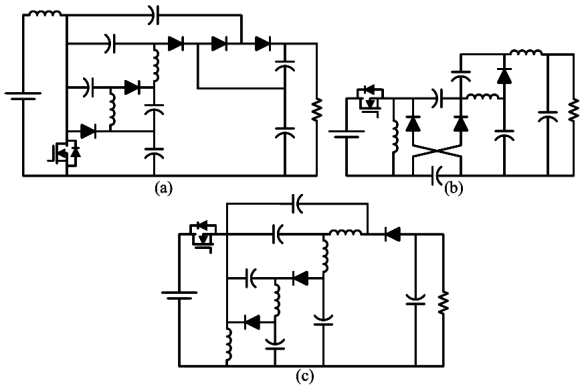

FIGURE 40. The presented topologies in: (a) [108], (b) [109], and (c) [110].

current with negligible ripple and maintain the common ground between the load and the input source. In terms of semiconductor voltage-stress management, topology [113] effectively addresses this challenge. Conversely, topology [114] provides continuous output current, which is absent in [133]. The resulting voltage gains of the topologies in [133] and [134] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2(2-D)}{(1-D)^2} \tag{57}$$

$$\frac{V_o}{V_{in}} = \frac{4D}{(1-D)^2} \tag{58}$$

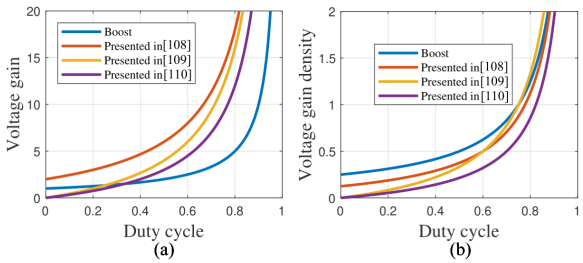

FIGURE 41. Comparison of the boost topology with the presented topologies in [108], [109], and [110]: (a) voltage gain, (b) voltage gain density.

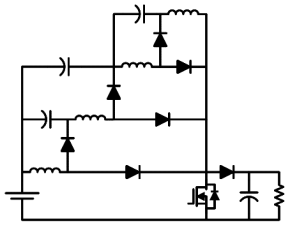

FIGURE 42. The presented topologies in: [111].

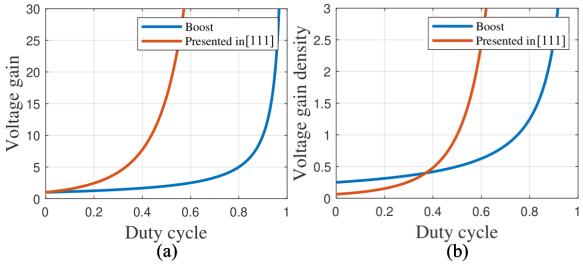

FIGURE 43. Comparison of the boost topology with the presented topologies in [111]: (a) voltage gain, (b) voltage gain density.

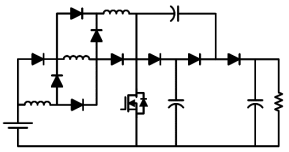

FIGURE 44. The presented topologies in: [112].

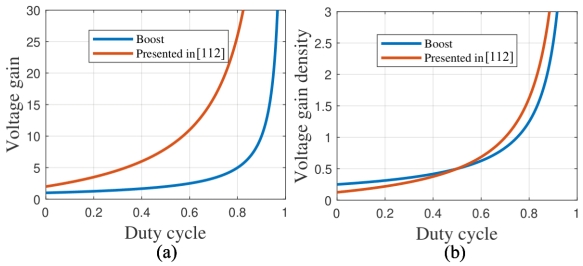

FIGURE 45. Comparison of the boost topology with the presented topologies in [112]: (a) voltage gain, (b) voltage gain density.

Fig. 47(a) presents the voltage-gain comparison of topologies [113] and [114] with the classical boost converter.

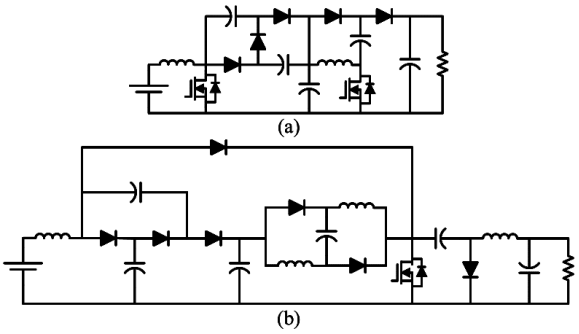

FIGURE 46. The presented topologies in: (a) [113] and (b) [114].

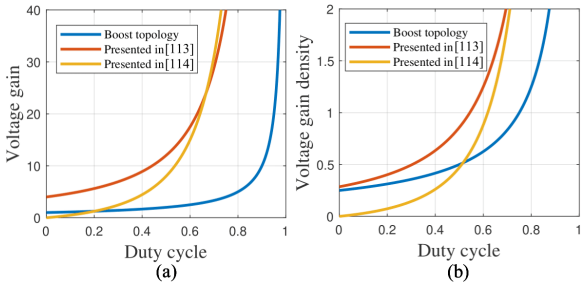

FIGURE 47. Comparison of the boost topology with the presented topologies in [113] and [114]: (a) voltage gain, (b) voltage gain density.

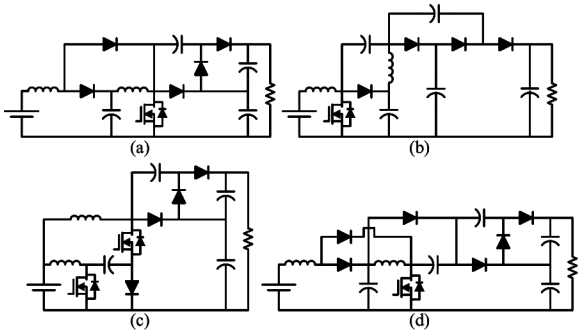

FIGURE 48. The presented topologies in: (a) [115], (b) [116], (c) [117], and (d) [118].

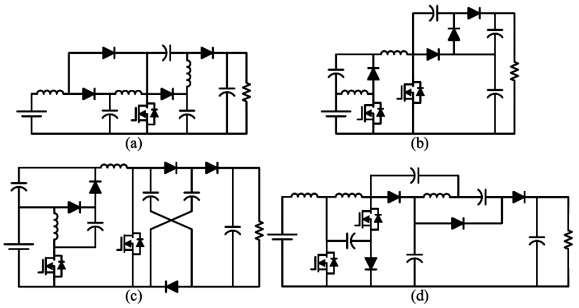

FIGURE 49. The presented topologies in: (a) [119], (b) [120], (c) [121], and (d) [121].

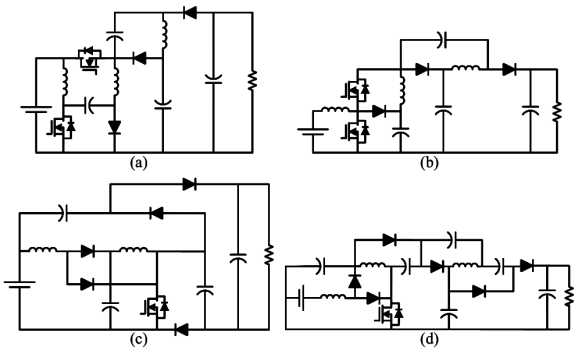

FIGURE 50. The presented topologies in: (a) [123], (b) [124], (c) [125], and (d) [126].

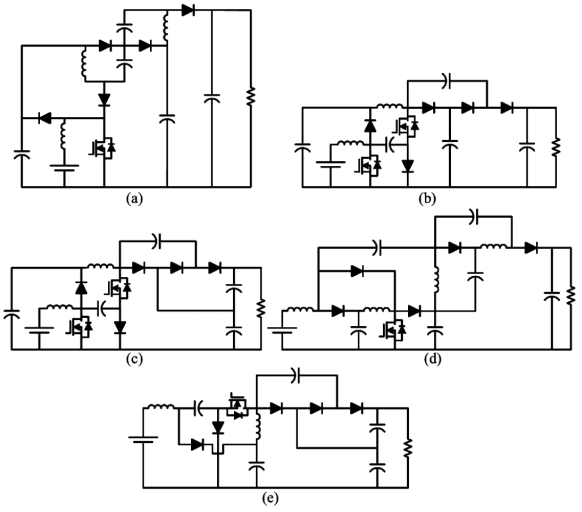

FIGURE 51. The presented topologies in: (a) [127], (b) [128], (c) [129], (d) [130], and (e) [131].

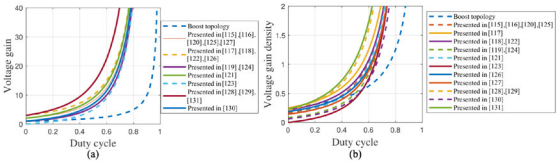

FIGURE 52. Comparison of the boost topology with the presented topologies in [115], [116], [117], [118], [119], [120], [121], [121], [123], [124], [125], [126], [127], [128], [129], [130], and [131]: (a) voltage gain, (b) voltage gain density.

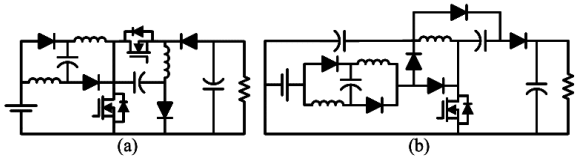

FIGURE 53. The presented topologies in: (a) [132] and (b) [133].

As shown, both topologies achieve higher voltage gain than the boost converter across all duty cycles. However, when considering voltage-gain density (Fig. 47(b)), topology [113] demonstrates superior performance compared to both the boost converter and topology [114] over the entire duty-cycle range. The relatively lower voltage-gain density of [114] can

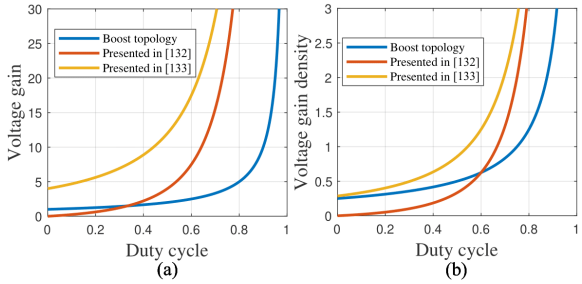

FIGURE 54. Comparison of the boost topology with the presented topologies in [132] and [133]: (a) voltage gain, (b) voltage gain density.

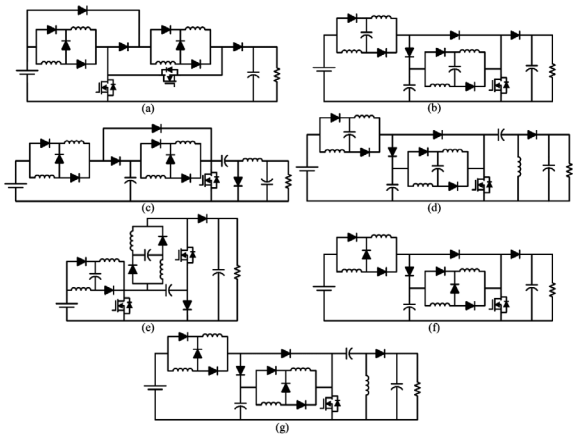

FIGURE 55. The presented topologies in: (a) [134], (b) [135], (c) [136], (d) [137], (e) [138], (f) [139], and [140].

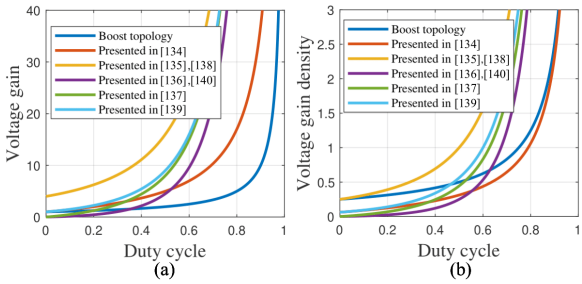

FIGURE 56. Comparison of the boost topology with the presented topologies in [134], [135], [136], [137], [138], [139], and [140]: (a) voltage gain, (b) voltage gain density.

be attributed to the increased number of inductors employed in its design.

U. TWENTY-FIRST GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [117], [118], [119], [120], [121], [121], [123], [124], [125], [126], [127], [128], [129], [130], and [131], illustrated in Figs. 48 to 51, are cascaded structures that incorporate a Voltage Multiplier Cell (VMC) at the output of the second stage. The first stage of these topologies employs either a conventional boost or a modified boost configuration. Some of these converters utilize a single-switch design, while others use a dual-switch arrangement. All the presented topologies maintain continuous input current and address the semiconductor voltage-stress challenge. Notably, among the topologies in [115], [116], [117], [118], [119], [120], [121], [121], [123], [124], [125], [126], [127], [128], [129], [130], and [131], those in [121] and [125] eliminate the common ground between the load and the input source. The resulting voltage gains of the topologies in [115], [116], [117], [118], [119], [120], [121], [121], [123], [124], [125], [126], [127], [128], [129], [130], and [131] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{59}$$

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{60}$$

$$\frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} \tag{61}$$

$$\frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} \tag{62}$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{(1-D)^2} \tag{63}$$

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{64}$$

$$\frac{V_o}{V_{in}} = \frac{(2-D)(1+D)}{(1-D)^2} \tag{65}$$

$$\frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} \tag{66}$$

$$\frac{V_o}{V_{in}} = \frac{D(3-D)}{(1-D)^2} \tag{67}$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{(1-D)^2} \tag{68}$$

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{69}$$

$$\frac{V_o}{V_{in}} = \frac{3-D}{(1-D)^2} \tag{70}$$

$$\frac{V_o}{V_{in}} = \frac{2}{(1-D)^2} \tag{71}$$

$$\frac{V_o}{V_{in}} = \frac{3+D}{(1-D)^2} \tag{72}$$

$$\frac{V_o}{V_{in}} = \frac{3+D}{(1-D)^2} \tag{73}$$

$$\frac{V_o}{V_{in}} = \frac{1+2D-2D^2}{(1-D)^2} \tag{74}$$

$$\frac{V_o}{V_{in}} = \frac{3+D}{(1-D)^2} \tag{75}$$

Based on the expressed equations, Fig. 52(a) presents the voltage-gain comparison of the topologies in this group with the classical boost converter, while Fig. 52(b) illustrates the corresponding comparison of voltage-gain density. As shown, all topologies in this group achieve higher voltage gain than the boost converter. Notably, the topologies in [128], [129], and [131] exhibit the highest voltage gain within the group, a superiority that is also reflected in their voltage-gain density.

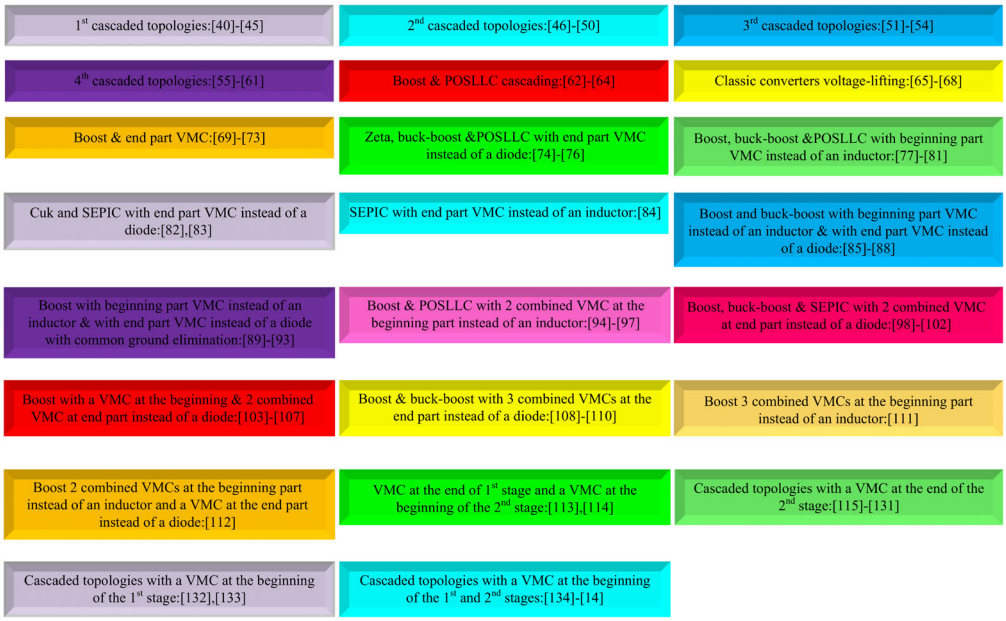

FIGURE 57. Categorizing the discussed converters.

V. TWENTY-SECOND GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [132] and [133], illustrated in Fig. 53, are cascaded structures that employ a Voltage Multiplier Cell (VMC) in place of the inductor at the input stage. Both topologies maintain continuous input current, although the current ripple increases. Topology [133] features a single-switch configuration, whereas [132] employs a dual-switch design. The semiconductor voltage-stress challenge is not addressed in [132] due to the use of a buck-boost converter in the second stage; conversely, topology [133] resolves this challenge by incorporating a POSLLC in the second stage. The resulting voltage gains of [132] and [133] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{2D}{(1-D)^2} \tag{76}$$

$$\frac{V_o}{V_{in}} = \frac{2(2-D)}{(1-D)^2} \tag{77}$$

Based on the expressed equations, Figs. 54(a) and 54(b) present the comparisons of voltage gain and voltage-gain density among topologies [132], [133], and the classical boost converter. As shown, topology [133] demonstrates superior performance compared to the boost converter across all duty cycles.

W. TWENTY-THIRD GROUP OF NON-ISOLATED DC–DC CONVERTERS

The topologies presented in [134], [135], [136], [137], [138], [139], and [140], illustrated in Fig. 55, are cascaded structures that employ inductor-based converters at the input stage of both the first and second levels. Topologies [134] and [138] utilize a dual-switch configuration, while the remaining converters are single-switch structures. Despite an increase in input current ripple, input current continuity is maintained across all these topologies. A common limitation among them is the unresolved semiconductor voltage-stress challenge. The resulting voltage gains of the topologies in [134], [135], [136], [137], [138], [139], and [140] are expressed as follows:

$$\frac{V_o}{V_{in}} = \frac{1+3D}{1-D} \tag{78}$$

$$\frac{V_o}{V_{in}} = \frac{4}{(1-D)^2} \tag{79}$$

$$\frac{V_o}{V_{in}} = D\left(\frac{1+D}{1-D}\right)^2 \tag{80}$$

$$\frac{V_o}{V_{in}} = \frac{4D}{(1-D)^2} \tag{81}$$

$$\frac{V_o}{V_{in}} = \frac{4}{(1-D)^2} \tag{82}$$

$$\frac{V_o}{V_{in}} = \left(\frac{1+D}{1-D}\right)^2 \tag{83}$$

$$\frac{V_o}{V_{in}} = D\left(\frac{1+D}{1-D}\right)^2 \tag{84}$$

As shown in Fig. 56(a), the topologies presented in [134], [135], and [137], [138], and [139] achieve higher voltage gain than the boost converter across all duty-cycle percentages. Notably, topologies [135] and [138] exhibit the highest voltage gain within this group. In terms of voltage-gain density (Fig. 56(b)), [135] and [138] also outperform both the boost converter and the remaining topologies in this group.

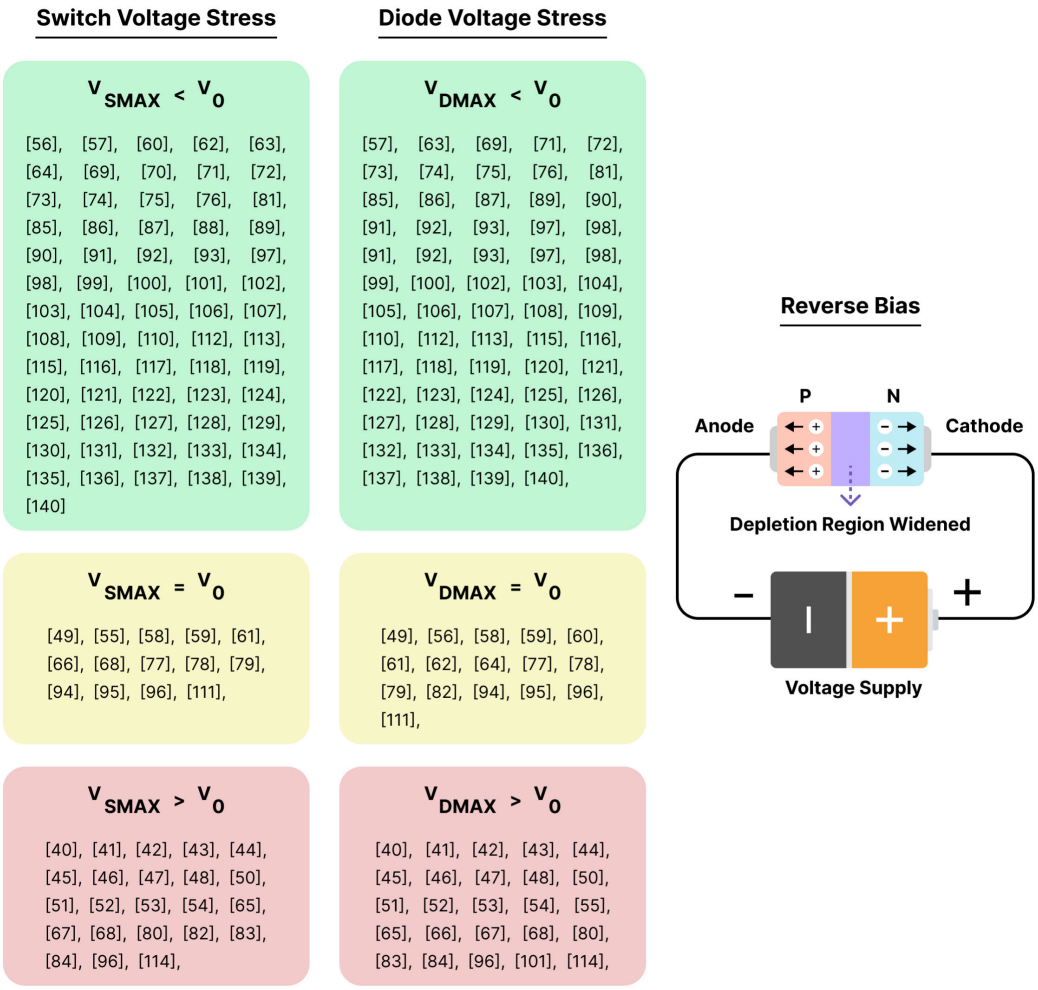

FIGURE 58. Comparison of the highest voltage stresses.

III. COMPARISON OF THE DISCUSSED DC–DC CONVERTERS ACCORDING TO THE VARIOUS FEATURES

In this section, the discussed topologies are compared with each other from various perspectives. Before the capability comparison of the presented topologies in [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75], [76], [77], [78], [79], [80], [81], [82], [83], [84], [85], [86], [87], [88], [89], [90], [91], [92], [93], [94], [95], [96], [97], [98], [99], [100], [101], [102], [103], [104], [105], [93], [107], [108], [109], [110], [111], [112], [113], [114], [115], [116], [117], [118], [119], [120], [121], [121], [123], [124], [125], [126], [127], [128], [129], [130], [131], [132], [133], [134], [135], [136], [137], [138], [139], and [140], a categorization must be done according to the structure of each topology in the mentioned converters. Fig. 57 presents the common topological features of the converters in each group. Notably, the presented categorization displays the topological advantages and disadvantages of the converters.

Table 9 presents the status of the input current continuity in the mentioned topologies. Three states are considered in this table. The (Purely continuous) state belongs to converters, whose input current ripple is low and negligible. The (Continuous) state belongs to converters, whose input current is continuous with a high current ripple. Finally, the (Discontinuous) state belongs to converters, whose input current becomes zero during one of the operating modes. The state of (Purely continuous) is achieved in converters, which use a simple boost, a simple Cuk, a simple SEPIC, or a modified buck-boost topology at the beginning of the converter. The state of (Continuous) is achieved in converters, which use a modified boost, a modified Cuk, a modified SEPIC, or a POSLLC at the beginning. Notably, this state can be achieved during the use of inductor-based VMCs at the beginning of the boost, Cuk, and SEPIC topologies. The state of (Discontinuous) is the result of using a simple

TABLE 9. Continuity and discontinuity of I_{in}.

Topologies	I_{in}	Topologies	I_{in}
[40]	Discontinuous	[41]	Purely continuous
[42]	Purely continuous	[43]	Continuous
[44]	Purely continuous	[45]	Purely continuous
[46]	Purely continuous	[47]	Purely continuous
[48]	Continuous	[49]	Purely continuous
[50]	Purely continuous	[51]	Continuous
[52]	Purely continuous	[53]	Purely continuous
[54]	Continuous	[55]	Continuous
[56]	Purely continuous	[57]	Continuous
[58]	Continuous	[59]	Continuous
[60]	Purely continuous	[61]	Purely continuous
[62]	Continuous	[63]	Continuous
[64]	Purely continuous	[65]	Purely continuous
[66]	Purely continuous	[67]	Purely continuous
[68]	Purely continuous	[69]	Purely continuous
[70]	Purely continuous	[71]	Purely continuous
[72]	Purely continuous	[73]	Purely continuous
[74]	Purely continuous	[75]	Discontinuous
[76]	Discontinuous	[77]	Continuous
[78]	Continuous	[79]	Continuous
[80]	Continuous	[81]	Discontinuous
[82]	Continuous	[83]	Purely continuous
[84]	Purely continuous	[85]	Purely continuous
[86]	Continuous	[87]	Continuous
[88]	Continuous	[89]	Continuous
[90]	Continuous	[91]	Continuous
[92]	Continuous	[93]	Continuous
[94]	Continuous	[95]	Continuous
[96]	Continuous	[97]	Continuous
[98]	Continuous	[99]	Purely continuous
[100]	Purely continuous	[101]	Purely continuous
[102]	Discontinuous	[103]	Purely continuous
[104]	Continuous	[105]	Continuous
[106]	Continuous	[107]	Continuous
[108]	Continuous	[109]	Purely continuous
[110]	Discontinuous	[111]	Discontinuous
[112]	Continuous	[113]	Continuous
[114]	Purely continuous	[115]	Purely continuous
[116]	Purely continuous	[117]	Purely continuous
[118]	Purely continuous	[119]	Purely continuous
[120]	Purely continuous	[121]	Continuous
[122]	Continuous	[123]	Purely continuous
[124]	Continuous	[125]	Purely continuous
[126]	Continuous	[127]	Purely continuous
[128]	Purely continuous	[129]	Purely continuous
[130]	Purely continuous	[131]	Purely continuous
[132]	Purely continuous	[133]	Continuous
[134]	Continuous	[135]	Continuous
[136]	Continuous	[137]	Continuous
[138]	Continuous	[139]	Continuous
[140]	Continuous		

TABLE 10. Continuity and discontinuity of I_o.

Topologies	I_o	Topologies	I_o
[40]	Discontinuous	[41]	Discontinuous
[42]	Discontinuous	[43]	Discontinuous
[44]	Purely continuous	[45]	Purely continuous
[46]	Purely continuous	[47]	Discontinuous
[48]	Discontinuous	[49]	Discontinuous
[50]	Discontinuous	[51]	Discontinuous
[52]	Purely continuous	[53]	Purely continuous
[54]	Purely continuous	[55]	Discontinuous
[56]	Discontinuous	[57]	Discontinuous
[58]	Discontinuous	[59]	Discontinuous
[60]	Discontinuous	[61]	Discontinuous
[62]	Discontinuous	[63]	Discontinuous
[64]	Discontinuous	[65]	Discontinuous
[66]	Discontinuous	[67]	Discontinuous
[68]	Discontinuous	[69]	Purely continuous
[70]	Discontinuous	[71]	Discontinuous
[72]	Discontinuous	[73]	Discontinuous
[74]	Discontinuous	[75]	Purely continuous
[76]	Discontinuous	[77]	Discontinuous
[78]	Discontinuous	[79]	Discontinuous
[80]	Discontinuous	[81]	Discontinuous
[82]	Discontinuous	[83]	Purely continuous
[84]	Discontinuous	[85]	Discontinuous
[86]	Discontinuous	[87]	Discontinuous
[88]	Discontinuous	[89]	Discontinuous
[90]	Purely continuous	[91]	Purely continuous
[92]	Discontinuous	[93]	Discontinuous
[94]	Discontinuous	[95]	Discontinuous
[96]	Discontinuous	[97]	Discontinuous
[98]	Discontinuous	[99]	Discontinuous
[100]	Discontinuous	[101]	Discontinuous
[102]	Discontinuous	[103]	Discontinuous
[104]	Discontinuous	[105]	Discontinuous
[106]	Discontinuous	[107]	Discontinuous
[108]	Discontinuous	[109]	Purely continuous
[110]	Discontinuous	[111]	Discontinuous
[112]	Discontinuous	[113]	Discontinuous
[114]	Purely continuous	[115]	Discontinuous
[116]	Discontinuous	[117]	Discontinuous
[118]	Discontinuous	[119]	Discontinuous
[120]	Discontinuous	[121]	Discontinuous
[122]	Discontinuous	[123]	Discontinuous
[124]	Discontinuous	[125]	Discontinuous
[126]	Discontinuous	[127]	Discontinuous
[128]	Discontinuous	[129]	Discontinuous
[130]	Discontinuous	[131]	Discontinuous
[132]	Discontinuous	[133]	Discontinuous
[134]	Discontinuous	[135]	Discontinuous
[136]	Purely continuous	[137]	Discontinuous
[138]	Discontinuous	[139]	Discontinuous
[140]	Discontinuous		

buck-boost or a simple zeta converter at the beginning. Moreover, using a modified boost topology at the beginning and a zeta or a buck-boost topology at the second stage leads to the (Discontinuous) state. The presented Table systematically categorizes the reviewed DC-DC converter topologies (references [40] to [140]) based on the nature of their input current (I_{in}). The continuity of the input current is a crucial performance indicator, as a continuous input current simplifies the required input filtering, minimizes conducted electromagnetic interference (EMI), and reduces stress on the input source, which is particularly vital when interfacing with sensitive energy sources such as fuel cells or photovoltaic arrays. The table utilizes three classifications: "Purely continuous," "Continuous," and "Discontinuous." A dominant trend is the preference for converter designs that inherently offer a continuous input current. Specifically, 54 out of 101 listed topologies (approximately 53.5%) are classified as "Purely continuous" (e.g., [41], [44], [60]) and an additional 38 topologies (approximately 37.6%) are classified as "Continuous" (e.g., [48], [54], [77]). Converters designated as "Purely continuous" typically integrate an inductor directly in series with the input voltage source, such as in boost-derived topologies, which is the most effective means of maintaining low input current ripple. "Continuous" topologies may achieve current continuity via alternate configurations or coupled inductors, potentially

Ref	Converter / Key Features	Advantages	Disadvantages
40	A new transformerless buck–boost converter with positive output voltage.	Non-Inverting: Provides positive output voltage (unlike conventional Buck-Boost). Buck-Boost Capability: Operates in both step-up and step-down modes.	Likely has a higher component count than a conventional Buck-Boost. Voltage gain is generally limited compared to quadratic types.
41	Quadratic buck–boost converter with positive output voltage and minimum ripple point design.	Quadratic Gain: Achieves a much wider range of voltage conversion. Minimum Ripple: Input current and output voltage ripples are simultaneously reduced/cancelled at a specific operating point. Non-Inverting: Positive output polarity.	Higher complexity and component count. Ripple cancellation is often highly effective only near the designed minimum ripple point.
42	Quadratic buck-boost converter with positive output-voltage and continuous input-current.	Continuous Input Current (CIC): Low ripple is suitable for sources like PV or fuel cells. Quadratic Gain & Non-Inverting: Wide conversion range with positive polarity.	Increased number of components (inductors/capacitors/diodes) for the continuous input feature.
43	Non-cascading quadratic buck-boost converter for photovoltaic applications.	Non-Cascading: Simpler structure and potentially higher efficiency than cascaded QBB designs. Quadratic Gain: High step-up/step-down capability.	Still has a higher component count than basic converters. May not achieve the lowest stress or highest gain compared to cascaded versions.
44	Single-switch quadratic buck–boost converter with continuous input port current and continuous output port current.	Continuous Input/Output Current (CIC/COC): Very low ripple on both sides, ideal for input source and output load. Single Switch: Simplifies the gate drive and control circuit.	Increased component count (L, C, D) due to the continuous current features. Switch stress might be higher than in multi-switch designs.
45	Continuous input and output current quadratic buck-boost converter with positive output voltage.	Continuous Input/Output Current (CIC/COC): Excellent for minimizing ripple on both source and load. Quadratic Gain & Non-Inverting: Wide conversion range with positive polarity.	High component count is typically required to achieve continuous currents on both sides.
46	Modified high voltage conversion inverting cuk DC-DC converter.	High Voltage Gain: Significantly higher step-up ratio than a conventional Cuk. Continuous Input Current (CIC): Inherited from Cuk, low input ripple.	Inverting Output: Produces a negative output voltage, which is undesirable for many applications. High component count due to modification.
47	A new structure of high voltage gain SEPIC converter.	High Gain: Achieves much higher step-up ratio than a conventional SEPIC. Non-Inverting & Continuous Input Current (CIC): Inherited from SEPIC.	Increased number of passive components (L/C/D) to achieve high gain. Complexity of the added structure.
49	A DC–DC converter with quadratic gain and input current ripple cancelation at a selectable duty cycle.	Quadratic Gain: Provides a wide conversion range. Ripple Cancellation: Achieves very low input current ripple, making it ideal for PV/fuel cells.	Higher component count. Ripple cancellation may degrade as the operating point (duty cycle) moves away from the ideal cancellation point.
52	Design and implementation of a new Cuk-based step-up DC–DC converter.	High Step-Up Gain: Achieves high voltage boost ratio. Continuous Input Current (CIC): Inherited from the Cuk topology. Likely non-inverting (as it's described as a "step-up" for general use).	Increased component count compared to conventional Cuk. Complexity in the added step-up cell.
91	Three topologies of a non-isolated high gain switched-inductor switched-capacitor step-up Cuk converter.	Ultra-High Gain: Uses both switched-inductor (SL) and switched-capacitor (SC) networks for massive voltage boost. Continuous Input Current (CIC): Inherited from the Cuk topology.	Very high component count (multiple L, C, D). Increased losses due to many components in the conduction path.
101	A new SEPIC-based single-switch buck–boost DC–DC converter with continuous input current.	Non-Inverting & Continuous Input Current (CIC): Inherited SEPIC advantages. Single Switch: Simple control and driver circuit. Buck-Boost Capability: Can step up and down.	Gain is typically lower than quadratic or high-order cascaded versions. Higher component count than conventional SEPIC.
119	High step-up single switch quadratic modified SEPIC converter.	Single Switch: Simplifies control. Quadratic Gain: High step-up ratio at a low duty cycle. Non-Inverting & Continuous Input Current (CIC): Inherited SEPIC advantages.	High component count to achieve the "quadratic" and "modified SEPIC" features.
55	A novel quadratic Boost converter with low current and voltage stress on power switch.	Low Switch Stress: Allows for a low $Rds_{(on)}$ MOSFET, boosting efficiency. Quadratic Gain & CIC: High step-up ratio with low input ripple.	Higher component count than conventional boost. Stress may be shifted to other components (diodes/capacitors).
56	Two-tier converter: A new structure of high gain DC-DC converter with reduced voltage stress.	High Gain & Low Stress: Achieves high step-up while keeping the voltage across the main switch low.	Requires two tiers/stages, increasing component count and complexity.
61	Quadratic boost converter based on stackable switching stages.	Modularity/Stackability: Allows easy extension to achieve ultra-high gain with proportional stress distribution. Continuous Input Current (CIC): Inherited from the boost structure.	High component count for high-stage versions. Complex control for multiple stages if not synchronously switched.

FIGURE 59. First group advantage and disadvantage discussion.

Ref	Converter / Key Features	Advantages	Disadvantages
63	Design and implementation of a single-switch step-up DC-DC converter based on cascaded boost and Luo converters.	Single Switch: Simple gate drive and control. Very High Gain: Achieves high step-up from the combination of boost and Luo cells.	High number of passive components due to the cascaded structure.
70	A high voltage ratio and low stress DC–DC converter with reduced input current ripple.	High Gain & Low Stress: Excellent for high step-up with high efficiency (due to low $Rds_{(on)}$ switch). Low Input Ripple: Good for source longevity.	Requires additional components to achieve all three benefits simultaneously.
73	Transformerless high gain boost and buck-boost DC–DC converters based on extendable switched capacitor (SC) cell.	Extendable Gain: The gain can be easily increased by adding more SC stages. Transformerless: Low volume, weight, and cost compared to isolated. Buck-Boost Capability: Highly versatile.	The voltage stress on components (especially switches) increases with the number of SC cells. Susceptible to current spikes and losses from the switched capacitor network.
86	Transformerless high step-up DC-DC converter based on conventional boost converter and voltage multiplier cells.	Ultra-High Gain: Achieved through the multiplicative effect of Voltage Multiplier Cells (VMCs). Single Switch (often): Simple control. Transformerless: No magnetic coupling issues.	Very high component count (Diodes, Capacitors) from VMCs. Efficiency may drop at high load due to conduction losses through many components.
94	Transformer-less double quadratic boost converter with positive output polarity and non zero input current.	Ultra-High Gain: Double quadratic gain offers extremely high step-up capability. Non-Zero Input Current (CIC): Low input ripple.	Very complex structure with a high number of passive components.
104	Ultra-step-up DC–DC converter with low-voltage stress on devices.	Ultra-High Gain & Low Stress: Best of both worlds, enabling high step-up with high-efficiency, low-voltage switches.	Likely a very high component count to achieve both ultra-high gain and low stress simultaneously.
118	A single switch high gain DC-DC converter with reduced voltage stress.	Single Switch & Reduced Stress: Simple control and high efficiency from a low $Rds_{(on)}$ switch.	The gain is likely high, but may not be as extreme as "ultra-step-up" converters. Higher passive component count than basic Boost.
48	Quadratic gain converter with output voltage ripple mitigation.	Quadratic Gain: High step-up ratio. Ripple Mitigation: Improved output quality over standard converters.	Higher complexity than a standard quadratic converter.
50	A new transformerless DC/DC converter with dual operating modes and continuous input current port.	Versatility (Dual Modes): Can operate under different conditions or control strategies. Continuous Input Current (CIC): Good for source lifetime.	Complexity in control and mode-switching.
51	A new negative output buck–boost converter with wide conversion ratio.	Wide Conversion Ratio (Buck-Boost): Versatile for input variations. Transformerless: Compact.	Negative Output: Only suitable for loads requiring a negative DC bus.
53	High-gain buck-boost converter suitable for renewable applications.	Buck-Boost & High Gain: Wide input voltage range and high step-up capability.	Likely higher component count than conventional.
54	New continuous input buck-boost converter with quadratic voltage conversion ratio.	Continuous Input Current (CIC): Ideal for PV/fuel cells. Quadratic Gain & Buck-Boost: Very wide input-output range.	High component count.
57	New enhanced family of QBC topologies: Mitigating capacitor stress and increasing voltage gain.	Low Capacitor Stress: Extends capacitor lifetime, improves reliability. High Gain: Improved conversion ratio over base QBC.	Topology is part of a family, implying multiple structures; likely higher component count than conventional QBC.
58	Design and implementation of a modified boost topology with high voltage ratio and efficiency besides the lower semiconductors' stresses.	High Gain, High Efficiency, Low Stress: Excellent overall performance metrics (the ultimate goal of most papers).	Increased component count and complexity to achieve all three objectives.
59	High step-up DC–DC converter with input current ripple cancellation.	High Step-Up & Ripple Cancellation: Ideal for high-power PV/Fuel Cell systems.	Ripple cancellation may be duty cycle dependent, leading to performance degradation off the ideal point.
60	Improving conventional cascaded DC-DC boost converters with reduced voltage stress on switches.	Ultra-High Gain (Cascaded): High voltage step-up. Low Switch Stress: Addresses the main drawback of conventional cascaded Boost converters.	Inherently high component count and complex control due to the cascaded stages.
62	Novel high step-up DC–DC converter with increased voltage gain per devices and continuous input current.	High Gain Density: Achieves high gain with a comparatively low component count (gain/device ratio). Continuous Input Current (CIC).	Still a moderate component count compared to basic topologies.
64	A power converter based on the combination of Cuk and positive output super lift Lou converters.	Ultra-High Gain: Combines two gain-enhancing techniques. Positive Output & CIC: Likely non-inverting with low input ripple.	Very high component count and very high-order dynamics, making control challenging.

FIGURE 60. Second group advantage and disadvantage discussion.

with a higher ripple magnitude than "Purely continuous" designs. In contrast, only 9 topologies (approximately 8.9%) are classified as "Discontinuous" (e.g., [40], [75], [81]). The discontinuous input current state is characteristic of buck-derived topologies or those employing only a capacitive input filter, leading to high pulse currents, large input ripple, and greater complexity in filtering requirements. The overall high prevalence of continuous-input topologies underscores the importance placed on power quality and compatibility with modern distributed generation sources in contemporary DC-DC converter design.

Table 10 presents the state of the output current in the mentioned converter. The state of (Purely continuous) is achieved in converters, which use a zeta or a Cuk topology at the end of the converter or employ inductor-based VMCs at the end of the converter. The state of (Discontinuous) is achieved in converters, which use a boost, buck-boost, SEPIC, POSLLC, or diode-capacitor-based VMCs at the end of the converter. In stark contrast to the high prevalence of continuous input current topologies observed in previous analysis, the data reveals a strong inclination toward "Discontinuous" output current operation. A total of 82 out of 101 listed converters (approximately 81.2%) fall into the "Discontinuous" category. This characteristic often stems from the use of a simple output capacitor filter without a series inductor, or from topologies where the energy transfer element is a discontinuous voltage or current source. Conversely, only 19 topologies (approximately 18.8%) achieve either "Purely continuous" or "Continuous" output current. These specific topologies typically incorporate an output inductor or utilize circuit arrangements, such as full-bridge rectifiers or specific coupled-inductor configurations, that force the output current to flow continuously into the load. The high incidence of discontinuous output current underscores a common design trade-off in high-gain converters: achieving high voltage lift often involves complex multiplier cells or single-switch configurations that inherently lead to pulsed energy delivery to the output, thereby necessitating a large output capacitor to smooth the current waveform.

Fig. 58 presents the comparison of the highest voltage stress of the switch and diodes in the discussed converters. The reported references in the green region are topologies which the highest switch or diode voltage stress is less than the output voltage. Additionally, the reported topologies in the light brown region have a highest switch/diode voltage stress equal to the output voltage. Finally, the reported topologies in the pink region, are the topologies which their highest switch or diode voltage stress is more than the output voltage.

The summary of the advantages and disadvantages of the disscussed converter have been illustrated in Figs. 59

Ref	Converter / Key Features	Advantages	Disadvantages
65	A non-isolated buck-boost DC–DC converter with continuous input current for photovoltaic applications.	Buck-Boost & Continuous Input Current (CIC): High versatility and low input ripple.	Gain may be lower than quadratic types.
66	Non-isolated high gain quadratic boost converter based on inductor's asymmetric input voltage.	High Gain (Quadratic) & CIC: High step-up with low input ripple. Asymmetric Input: Novel design approach, potentially optimizing component use.	Novel structure introduces unique modeling/control challenges.
67	A non-isolated buck-boost DC–DC converter with continuous input current and wide conversion ratio range.	Continuous Input Current (CIC) & Wide Range: High versatility for varying input sources.	Likely has higher component count than non-CIC versions.
68	A non-inverting transformerless semi-quadratic buck-boost converter.	Semi-Quadratic Gain: High gain, but slightly less than full quadratic, which might lead to fewer components. Buck-Boost & Non-Inverting.	Reduced component count may come at the expense of slightly higher switch stress than full-quadratic low-stress designs.
69	New high gain transformer-less single switch boost DC-DC converter with lower switch stress and less passive elements.	Optimal Component Balance: A rare claim to achieve high gain, low stress, and low component count simultaneously. Single Switch.	The term "fewer passive elements" is relative; component stress may be higher than multi-switch, ultra-low stress designs.
71	A modified high step-up non-isolated DC-DC converter for PV application.	High Step-Up: Suitable for low-voltage PV input. Non-Isolated: High efficiency and compact.	General claim; specific stress/ripple metrics are unknown without the full paper.
72	A new high gain modified boost converter for renewable energy application with closed loop control.	High Gain & CIC (Boost-based): Good for renewable energy interface. Closed Loop Control: Ensures good steady-state and dynamic performance.	The gain enhancement method is not specified in the title, likely leading to increased component count.
74	Single-switch high step-up Zeta converter based on coat circuit.	Zeta-Based: Inherently non-inverting. Single Switch: Simple control. High Step-Up: Enhanced gain over conventional Zeta.	Conventional Zeta has discontinuous input current. High component counts due to the "coat circuit" and gain.
75	Low-voltage stress buck-boost converter with a high-voltage conversion gain.	Low Switch Stress & High Gain: Achieves high step-up while maintaining high efficiency due to low $Ros_{(on)}$ switch. Buck-Boost: Versatility.	Higher component count to achieve both high gain and low stress.
76	A modified positive output super-lift Luo DC-DC converter with improved voltage boost ability.	Ultra-High Gain: Uses Super-Lift Luo technique. Positive Output: Non-inverting.	Very high component count (inductors/capacitors). High-order dynamics, making control challenging.
77	A high gain novel double-boost converter for DC microgrid applications.	High Gain: Achieves the square of the conventional boost gain (high step-up). Continuous Input Current (CIC).	Higher voltage stress on switches than low-stress designs.
78	Quadratic boost converter with low buffer capacitor stress.	Low Capacitor Stress: Extends capacitor lifetime. Quadratic Gain & CIC: High step-up with low input ripple.	Component count higher than conventional boost.
79	Single switch non-isolated high gain DC-DC converter for PV applications.	Single Switch & High Gain: Simple control, high step-up capability.	Likely higher component count than basic Boost.
80	A novel single switch transformerless quadratic DC/DC buck-boost converter.	Single Switch & QBB: Simple control and wide, non-inverting voltage conversion range. Transformerless: Compact and high efficiency.	Likely higher stress on the switch than multi-switch, low-stress designs.
82	A high conversion ratio transformerless buck-boost converter with continuous input current.	High Gain, CIC, Buck-Boost: Excellent versatility for renewable sources.	Higher component count than conventional converters.
83	A novel high gain single-switch DC-DC buck-boost converter with continuous input and output power.	Single Switch & Continuous Power: Ensures stable power transfer from source to load. Buck-Boost & High Gain: Wide operating range.	High component count to manage continuous power flow on both sides.
84	High-efficiency transformerless buck-boost DC–DC converter.	Buck-Boost & High Efficiency: Focuses on minimizing power losses. Transformerless.	Efficiency goal may limit the achievable voltage gain.
85	Switched inductor-capacitor network based non-isolated DC-DC converter: A Double D^2 gain converter with single switch.	Very High Gain (Double D^2): Extremely high step-up capability. Single Switch: Simple control.	Very high component count. Very high-order dynamics, making control difficult.
87	Design and implementation of a new high step-up DC-DC converter for renewable applications.	High Step-Up: Suitable for low-voltage renewable sources.	General title; specific stress/ripple advantages unknown.

FIGURE 61. Third group advantage and disadvantage discussion.

Ref	Converter / Key Features	Advantages	Disadvantages
88	Design and analysis of extendable switched-inductor and capacitor-divider network based high-boost DC-DC converter.	Extendable Gain: Modular design for ultra-high voltage applications. High Boost: High step-up ratio.	High component count for high gain stages. Control complexity increases with stages.
89	Active and reactive power control of grid-connected PV power systems based on HGNISS DC-DC converter and SMDPC strategy.	HGNISS (High-Gain Non-Isolated Single-Switch): Excellent for grid-tie PV applications.	The specific converter architecture is general; detailed pros/cons depend on the specific HGNISS design.
90	A new efficient step-up boost converter with CLD cell for electric vehicle and new energy systems.	High Efficiency & High Step-Up: Good for EV applications. CLD (Coupled-Inductor/Diode) Cell: Effective high-gain mechanism.	Coupled inductors introduce leakage inductance issues.
92	High gain boost converter with reduced switching stress.	High Gain & Low Stress: Enables high efficiency with low $Rds_{(on)}$ switch. Continuous Input Current (CIC).	Higher component count than conventional Boost.
93	A new transformerless ultra high gain DC–DC converter for DC microgrid application.	Ultra-High Gain: Achieves a massive voltage boost. Transformerless: High efficiency, compact.	Very high component count. Very high-order dynamics.
95	A novel extendable single-switch quadratic-based high step-up DC-DC converter.	Extendable Gain: Modular for ultra-high voltage. Single Switch & Q-based: Simple control with high gain.	High component count for extended versions.
96	Switched-inductor-based non-isolated large conversion ratio, low components count DC-DC regulators.	Low Component Count & High Gain: A strong balance between complexity and performance.	"Low components count" is relative; may still be higher than basic topologies.
97	Integrated PV–BESS-Fed high gain converter for an LED lighting system.	Integration: Manages power flow from both PV and Battery Energy Storage System (BESS). High Gain: Suitable for low PV voltage.	Complex control for managing two input sources.
99	High step-up DC-DC converter using voltage lift techniques for renewable applications.	Ultra-High Gain: Voltage lift techniques are highly effective for extreme voltage boosting.	High number of passive components (inductors/capacitors) required for multiple lift stages.
100	Analysis of high voltage gain DC-DC boost converter for renewable energy applications.	High Gain & CIC (Boost-based): Suitable for low-voltage sources.	General title; specific component count and stress advantages unknown.
102	High gain DC-DC converter for PV applications.	High Gain: Suitable for low-voltage PV input.	General title; specific component count and stress advantages unknown.
103	A voltage hexa-lift and output triple stacked boost converter.	Ultra-High Gain: Extremely high step-up from the hexa-lift and triple-stacked structure. CIC (Boost-based).	Extremely high component count. Very high-order control dynamics.
106	A new transformerless ultra high gain DC–DC converter for DC microgrid application.	Ultra-High Gain & Transformerless: Excellent step-up in a compact design.	Very high component count.
108	Single-active switch high-voltage gain DC–DC converter using a non-coupled inductor.	Single Switch & High Gain: Simple control without coupled-inductor complexities (e.g., leakage).	High component count likely needed for high gain without coupled inductors.
110	A buck-boost converter; design, analysis and implementation suggested for renewable energy systems.	Buck-Boost: Highly versatile for wide input voltage variations. Transformerless.	Conventional Buck-Boost has a negative output and discontinuous input/output currents.
111	Switched Q network-based multistage ultra gain DC-DC converter.	Ultra-High Gain: Achieved through multi-stage Switched LC cells.	Very high component count and complexity.
112	Analysis and design of a switched-capacitor and switched-inductor network based high-gain DC-DC converter.	Ultra-High Gain: Combines the benefits of Switched-L and Switched-C for massive gain.	High component count.
113	A new high gain boost converter with common ground for solar-PV application and low ripple input current.	Common Ground: Simplifies gate drive and control (no high-side measurement needed). CIC & High Gain: Ideal for PV.	Higher component count than a standard Boost.
115	A new non-isolated high-gain DC-DC converter for the PV application.	High Gain & Non-Isolated: Suitable for low-voltage PV input.	General title; specific component count and stress advantages unknown.
116	High step-up DC/DC converter with low input current ripple and low voltage stress on semiconductors.	Optimal Performance: Excellent combination of high gain, low ripple, and high efficiency (low stress).	High component count is typically necessary to achieve all three benefits.
117	A switched capacitor DC-DC boost converter with high voltage gain.	High Gain: Switched-capacitor network boosts voltage significantly.	High pulsating currents/current spikes inherent to SC networks.

FIGURE 62. Fourth group advantage and disadvantage discussion.

Ref	Converter / Key Features	Advantages	Disadvantages
120	Non-isolated high step-up DC–DC converter based on switched-inductor switched-capacitor network for photovoltaic application.	Ultra-High Gain: Combines switched-L and switched-C for massive gain.	Very high component count and complexity.
121, 122	Modified LUO high gain DC-DC converter with minimal capacitor stress for electric vehicle application.	Minimal Capacitor Stress: Extends capacitor lifetime, improves reliability. High Gain: Enhanced step-up ratio.	High number of components due to Luo Super-Lift and modification.
123	A new transformerless semi-quadratic buck–boost converter based on combination of Cuk and traditional buck–boost converters.	Buck-Boost & Semi-Quadratic: Wide range and high gain with versatile functionality. Hybrid Topology: Combines Cuk (CIC) and Buck-Boost features.	High component counts due to the hybrid structure.
124	A quasi-Z-source (QZS) network-based quadratic boost converter.	QZS & Q-Boost: Inherits the shoot-through protection of QZS. Quadratic Gain & CIC.	Very high component count due to the addition of the QZS network.
125	A family of transformerless quadratic boost high gain DC-DC converters.	High Gain (Quadratic) & CIC: Multiple variations offer design flexibility.	General design; specific variation needed for detailed pros/cons. High component count in all variations.
126	An ultra-high step-up DC-DC converter based on the boost, Luo, and voltage doubler structure.	Ultra-High Gain: Combines three gain-enhancing structures for massive step-up.	Extremely high component count. Very high-order dynamics and control complexity.
127	A boost and Luo based non-isolated DC-DC converter suitable for DC link of high voltage applications.	Ultra-High Gain: Combination of Boost and Luo principles. Non-Isolated.	High component count.
128	A family of transformerless step-up DC-DC converters: Analysis, comparison and experiment.	Analysis & Comparison: Provides a framework for evaluating multiple topologies. Step-Up & Transformerless.	General title; specific pros/cons depend on the individual converter within the family.
129	DC–DC boost converter with a wide input range and high voltage gain for fuel cell vehicles.	Wide Input Range & High Gain: Addresses the varying output voltage of fuel cells. Continuous Input Current (CIC).	Higher component count than conventional Boost.
130	Design and analysis of a non-isolated DC-DC converter with a high-voltage conversion ratio.	High Gain & Non-Isolated.	General title; specific stress/ripple advantages unknown.
131	A novel high quadratic gain boost converter for fuel cell electric vehicle applications.	Quadratic Gain & CIC: Excellent high step-up for low fuel cell voltage.	Higher component count than conventional boost.
133	An ultra-high step-up DC-DC converter based on VMC, POSLLC, and boost converter.	Ultra-High Gain: Uses a combination of Voltage Multiplier Cell (VMC), Positive Output Super-Lift Luo Converter (POSLLC), and Boost.	Extremely high component count and very complex dynamics.
134	Novel non-isolated quad-switched inductor double-switch converter for DC microgrid application.	High Gain: Utilizes four switched inductors for significant voltage boost. Double Switch: May allow for better stress distribution than a single switch.	Very high component count (four inductors and two switches).
135	Novel immense configurations of boost converter for renewable energy application.	High Gain & CIC (Boost-based): Offers multiple options for design flexibility.	General title; specific pros/cons depend on the chosen configuration.
138	A non-isolated quadratic DC-DC converter improved by voltage-lift technique.	Ultra-High Gain: Combines quadratic gain with a voltage-lift technique. Non-Isolated & CIC.	Very high component count and complex dynamics.
139	Modified boost with switched inductor different configurational structures for DC-DC converter.	High Gain & CIC (Boost-based): Offers flexibility by providing different configurations.	General title; each configuration has a unique component count/ stress profile.

FIGURE 63. Fifth group advantage and disadvantage discussion.

to 63. Additionally, the comparison of the efficiency has been illustrated in Figs. 64 to 66.

Fig. 67 presents the number of each type of component in the discussed topologies. The accompanying comparative figure furnishes a quantitative metric for assessing the inherent complexity across a diverse array of DC-DC converter topologies, spanning the references from [40] to [140]. This assessment is based on the enumeration of the four primary circuit constituents: Inductors (L), Capacitors (C), Active Switches (S), and Diodes (D). The total component count, designated as $N_{all} = L + C + S + D$, serves as a direct proxy for evaluating converter fabrication cost, physical volume, power density, and potential system reliability. The analysis reveals distinct trends in component utilization correlated with the targeted voltage conversion capability and architectural complexity, allowing the topologies to be grouped into three primary categories.

- Low-Complexity Architectures ($N_{all} \leq 8$): This category is defined by the lowest total component counts, primarily featuring $N_{All} = 8$. The topologies in this group represent fundamental converter structures, prioritizing simplified control logic and minimal implementation complexity. Most exhibit a balanced distribution, most commonly$(2L, 2C, 2S, 2D)$, as seen in [40] and [48]. Conversely, some achieve $N_{all} = 8$ with a single active switch, such as the $(2L, 2C, 1S, 3D)$ configuration in [59] and [77], indicating a shift

Ref	Converter Title / Key Features	Expected Peak Efficiency Range (Approx.)	Rationale
40	New transformerless buck-boost with positive output voltage.	92% - 95%	Modified standard topology; expected moderate complexity and high efficiency.
41	Quadratic buck–boost with positive output & minimum ripple point design.	91% - 94%	Quadratic gain adds complexity. Ripple mitigation suggests a focus on component choice, which can boost efficiency.
42	Quadratic buck-boost with positive output and continuous input-current.	91% - 94%	Quadratic gain adds complexity. Continuous current suggests more passive components.
43	Non-cascading quadratic buck-boost.	92% - 95%	Non-cascading often implies simpler structure (fewer components), leading to higher expected efficiency.
44	Single-switch quadratic buck–boost with continuous input/output.	93.9% (Reported)	High complexity, but single switch simplifies gate drive and often optimizes control.
45	Continuous input and output current quadratic buck-boost.	90% - 93%	Very high component count to achieve continuous current on both sides, accumulating losses.
46	Modified high voltage conversion inverting Cuk.	90% - 93%	High gain modification increases component count. Cuk-based with accumulated losses.
47	New structure of high voltage gain SEPIC converter.	91% - 94%	SEPIC-based (CIC/Non-inverting). High gain modification adds components.
48	Quadratic gain converter with output voltage ripple mitigation.	91% - 94%	Focus on ripple adds complexity/components; efficiency is usually a secondary metric to ripple.
49	Quadratic gain with input current ripple cancelation.	91% - 94%	Focus on ripple cancellation. High component counts due to quadratic gain.
50	New transformerless DC/DC with dual operating modes and continuous input current.	90% - 93%	Dual mode and continuous input add structural complexity and potentially more components.
51	New negative output buck–boost with wide conversion ratio.	92% - 95%	Modified basic topology; medium complexity.
52	New Cuk-based step-up DC–DC converter.	91% - 94%	Cuk-based high gain.
53	High-gain buck-boost converter.	90% - 93%	High gain in a buck-boost configuration implies high complexity and component count.
54	New continuous input buck-boost with quadratic gain.	90% - 93%	High component count for CIC and QBB.
55	Novel quadratic Boost with low current and voltage stress on power switch.	90% - 93% (Reported range)	Low Stress design aims for high efficiency, often achieving 93% +
56	Two-tier converter with reduced voltage stress.	92% - 95%	Low-stress design targets high efficiency, despite being multi-tier (two switches).
57	Enhanced family of QBC topologies: Mitigating capacitor stress and increasing voltage gain.	91% - 94%	Reduced stress helps efficiency. QBC is inherently complex.
58	Modified boost with high voltage ratio and efficiency besides the lower semiconductors' stresses.	93% - 96%	Claims high efficiency and low stress, suggesting high performance targets.
59	High step-up DC–DC converter with input current ripple cancellation.	90% - 93%	Complexity of ripple cancellation often slightly impacts efficiency.
60	Improving conventional cascaded boost with reduced voltage stress on switches.	89% - 92%	Cascaded topologies inherently have many components, leading to accumulated losses (even with stress reduction).
61	Quadratic boost based on stackable switching stages.	89% - 92%	High complexity/component count for high gain.
62	High step-up DC–DC converter with increased voltage gain per devices.	91% - 94%	Good component utilization suggests focus on efficiency.
63	Single-switch step-up based on cascaded boost and Luo converters.	89% - 92%	High component count and complexity from cascading two high-gain circuits.
64	Combination of Cuk and POSLLC converters.	88% - 91%	Extremely high component count due to complex hybrid topology.
65	Non-isolated buck–boost with continuous input current.	92% - 95%	Modified standard topology, medium complexity.
66	High gain quadratic boost based on inductor's asymmetric input voltage.	91% - 94%	Quadratic gain and complexity.
67	Non-isolated buck-boost with continuous input current and wide conversion ratio.	90% - 93%	High component count for continuous input and wide range.

FIGURE 64. First group efficiency comparison.

Ref	Converter Title / Key Features	Expected Peak Efficiency Range (Approx.)	Rationale
68	Non-inverting transformerless semi-quadratic buck-boost.	91% - 94%	High gain modification.
69	New high gain single switch boost with lower switch stress and less passive elements.	93% - 96%	Claims high efficiency due to low stress and low component count.
70	High voltage ratio and low stress DC–DC converter with reduced input current ripple.	93% - 96%	Explicitly aims for low stress (high efficiency) and high gain.
71	Modified high step-up non-isolated DC-DC converter.	90% - 93%	High gain modification.
72	New high gain modified boost converter.	91% - 94%	Boost-based high gain.
73	Transformerless high gain boost and buck-boost based on extendable switched capacitor (SC) cell.	88% - 92%	SC circuits often have lower efficiency due to losses from high-frequency current spikes.
74	Single-switch high step-up Zeta converter based on coat circuit.	90% - 93%	Zeta-based high gain.
75	Low-voltage stress buck-boost converter with a high-voltage conversion gain.	92% - 95%	Low-stress design targets high efficiency.
76	Modified positive output super-lift Luo with improved voltage boost ability.	88% - 91%	Super-Lift Luo is a very high-gain, high component count topology.
77	High gain novel double-boost converter.	90% - 93%	High gain, complexity.
78	Quadratic boost converter with low buffer capacitor stress.	92% - 95%	Low stress on a component helps lifetime, often correlating with high efficiency.
79	Single switch non-isolated high gain DC-DC converter.	91% - 94%	Single switch simplifies control. High gain adds components.
80	Novel single switch transformerless quadratic DC/DC buck-boost converter.	90% - 93%	Quadratic gain and complexity.
82	High conversion ratio transformerless buck-boost with continuous input current.	90% - 93%	High gain, CIC, and complexity.
83	High gain single-switch buck-boost with continuous input and output power.	89% - 92%	High complexity for simultaneous continuous input/output power in a high-gain QBB.
84	High-efficiency transformerless buck–boost DC–DC converter.	93% - 96%	Explicitly targets high efficiency.
85	Switched inductor-capacitor network: A Double D^2 gain converter.	88% - 91%	Extreme gain implies a very high component count and accumulated losses.
86	Transformerless high step-up based on conventional boost and voltage multiplier cells.	89% - 92%	Voltage Multiplier Cells (VMCs) add many diodes and capacitors, increasing losses.
87	New high step-up DC-DC converter.	90% - 93%	General high-gain design.
88	Extendable switched-inductor and capacitor-divider network based high-boost DC-DC converter.	89% - 92%	Modularity and high component count in extended versions.
89	Grid-connected PV based on HGNISS DC-DC converter.	91% - 94%	General high-gain, single-switch, non-isolated topology.
90	Efficient step-up boost converter with CLD cell.	92% - 95%	Focus on efficiency. Coupled-inductor (CLD) designs can be high efficiency if leakage is managed.
91	High gain switched-inductor switched-capacitor step-up Cuk converter.	88% - 91%	Extremely high component count from L+C cells.
92	High gain boost converter with reduced switching stress.	92% - 95%	Low-stress design targets high efficiency.
93	Transformerless ultra high gain DC–DC converter.	89% - 92%	Ultra-high gain implies high component count.
94	Transformer-less double quadratic boost converter.	89% - 92%	Extremely high gain and component count.
95	Novel extendable single-switch quadratic-based high step-up DC-DC converter.	90% - 93%	Modularity and complexity.
96	Switched-inductor-based large conversion ratio, low components count DC-DC regulators.	92% - 95%	Low component count for a given gain implies higher efficiency.
97	Integrated PV–BESS-Fed high gain converter.	90% - 93%	High gain and multi-source integration add complexity.
98	Modified multiplier SEPIC converter.	90% - 93%	High gain modification of SEPIC.
99	High step-up DC-DC converter using voltage lift techniques.	89% - 92%	Voltage lift techniques add many components in series, increasing accumulated losses.
100	High voltage gain DC-DC boost converter.	91% - 94%	General high-gain boost modification.
101	SEPIC-based single-switch buck–boost with continuous input current.	92% - 95%	Modified classical topology, medium complexity.

FIGURE 65. Second group efficiency comparison.

towards topologies where the diode count supports the voltage gain in a single-switch structure. The single lowest complexity is observed in reference [75] with $N_{all} = 7(1L, 3C, 1S, 2D)$, highlighting a specific design objective of extreme component minimization.

- Mid-to-High Complexity Architectures ($9 \leq N_{all} \leq 14$): This is the largest and most varied category, encompassing a wide range of component counts. These architectures are designed to offer enhanced performance, particularly high voltage gain, over the basic structures. Topologies: Key representatives of this range include [44], [45], [46], [47], [52], [53], [62], [63], [64], [65], [66], [67], [68], [70], [74], [76], [81], [82], [83], [84], [85], [86], [87], [88], [89], [90], [91], [92], [94], [95], [96], [98], [99], [101], [102], [109], [110], [113], [115], [116], [117], [119], [120], [123], [124], [125], [127], [131], [132], [133]. Component Characteristics: A critical observation is the strong propensity to maintain a low active switch count, with the vast majority utilizing $S = 1$(*e.g.*, [82]). The increase in N_{all} from 10 to 14 is predominantly driven by the proliferation of passive components (C and L) and diodes (D), which are used to integrate auxiliary gain enhancement structures like Voltage Multiplier Cells (VMCs) or switched capacitor networks. For example, theN_{all} topology [85] (2L, 4C, 1S, 5D) uses a higher count of diodes and capacitors to boost the voltage without increasing the complexity of the control stage. Two-Switch Topologies: A notable subset, such as [45] (3L, 3C, 2S, 2D) and [120] (2L, 4C, 2S, 4D), utilizes two active switches, often for increased flexibility, bi-directional operation, or enabling soft-switching transitions, accepting a slightly higher control complexity.
- Maximum-Complexity Architectures ($N_{all} \geq 15$): This tier comprises the most component-intensive topologies, engineered for the most demanding applications, such as ultra-high voltage conversion ratios and multi-level functionality. Topologies: This high-end group includes [93], [97], [100], [103], [104], [105], [107], [108], [111], [112], [114], [118], [121], [121], [126], [128], [129], [130], [134], [135], [136], [137], [138], [139], [140]. Component Characteristics: These converters exhibit the maximum utilization of passive components and diodes. The highest component counts are seen in [104] (3L, 7C, 1S, 7D) and [136] (5L, 3C, 1S, 9D), reaching $N_{all} = 18$. The overwhelming number of diodes and capacitors, such as the 9 diodes in [136], points toward advanced, high-order VMCs used to

Ref	Converter Title / Key Features	Expected Peak Efficiency Range (Approx.)	Rationale
102	High gain DC-DC converter for PV applications.	91% - 94%	General high-gain design.
103	Voltage hexa-lift and output triple stacked boost converter.	88% - 91%	Extremely high component count and complexity.
104	Ultra-step-up DC–DC converter with low-voltage stress on devices.	91% - 94%	High component count for ultra-gain, but low stress aims to keep it efficient.
105	Design of novel HG-SIQBC-fed multilevel inverter.	90% - 93%	High Gain Switched-Inductor QBC; high complexity.
106	Transformerless ultra high gain DC–DC converter.	89% - 92%	Ultra-high gain implies high component count.
108	Single-active switch high-voltage gain using a non-coupled inductor.	91% - 94%	Avoids coupled inductor loss, but still high complexity for high gain.
111	Switched LC network-based multistage ultra gain DC-DC converter.	88% - 91%	Very high component count and accumulated losses.
112	Switched-capacitor and switched-inductor network based high-gain DC-DC converter.	88% - 91%	Combination of L and C cells for extreme gain.
113	High gain boost converter with common ground for solar-PV and low ripple input current.	92% - 95%	Design focuses on practical features (common ground, low ripple) while maintaining high gain.
114	New quadratic CUK-based step-up DC/DC converter without right hand plane zero.	91% - 94%	Focus on improved control (no RHPZ), which is often secondary to efficiency. High component count.
115	New non-isolated high-gain DC-DC converter.	91% - 94%	General high-gain design.
116	High step-up DC/DC converter with low input current ripple and low voltage stress on semiconductors.	93% - 96%	Explicitly claims low stress/ripple, targeting high efficiency.
117	Switched capacitor DC-DC boost converter with high voltage gain.	89% - 92%	Switched capacitor circuits often have lower efficiency due to current spikes.
118	Single switch high gain DC-DC converter with reduced voltage stress.	92% - 95%	Low-stress design targets high efficiency.
119	High step-up single switch quadratic modified SEPIC converter.	90% - 93%	High complexity for Q-SEPIC.
120	Non-isolated high step-up based on switched-inductor switched-capacitor network.	88% - 91%	Very high component count.
121, 122	Modified LUO high gain DC-DC converter with minimal capacitor stress.	90% - 93%	High component count of Luo plus modification.
123	New transformerless semi-quadratic buck–boost based on Cuk and traditional buck–boost converters.	90% - 93%	High complexity of the hybrid topology.
124	Quasi Z-source (QZS) network-based quadratic boost converter.	89% - 92%	QZS adds many components (2L, 2C, 2D) to a Q-boost, heavily increasing losses.
125	Family of transformerless quadratic boost high gain DC-DC converters.	90% - 93%	High component count.
126	Ultra-high step-up based on boost, Luo, and voltage doubler structure.	88% - 91%	Extremely high component count.
127	Boost and Luo based non-isolated DC-DC converter.	89% - 92%	High complexity.
129	DC–DC boost converter with a wide input range and high voltage gain.	92% - 95%	High gain for wide input range, often optimizing components for high efficiency.
130	Non-isolated DC-DC converter with a high-voltage conversion ratio.	91% - 94%	General high-gain design.
131	Novel high quadratic gain boost converter for fuel cell electric vehicle applications.	91% - 94%	Quadratic gain and complexity.
132	Implementation and reliability analysis of a new non-isolated quadratic buck–boost converter.	90% - 93%	High complexity QBB.
133	Ultra-high step-up based on VMC, POSLLC, and boost converter.	91% (Reported)	Extremely high component count.
134	Novel non-isolated quad-switched inductor double-switch converter.	89% - 92%	Very high component count (4L, 2S).
135	Novel immense configurations of boost converter.	90% - 94%	General high-gain boost.
138	Non-isolated quadratic DC-DC converter improved by voltage-lift technique.	89% - 92%	Combining two complex techniques leads to high component count.
139	Modified boost with switched inductor different configurational structures.	91% - 94%	General high-gain boost.

FIGURE 66. Third group efficiency comparison.

Topologies	Switches	Diodes	Inductors	Capacitors	ALL	RCI (Relative Cost Index)	Topologies	Switches	Diodes	Inductors	Capacitors	ALL	RCI (Relative Cost Index)
[40]	2	2	2	2	8	26	[41]	2	2	2	2	8	26
[42]	2	2	2	2	8	26	[43]	2	2	2	2	8	26
[44]	1	5	3	3	12	33	[45]	2	2	3	3	10	32
[46]	1	3	3	3	10	29	[47]	1	3	3	3	10	29
[48]	2	2	2	2	8	26	[49]	2	2	2	2	8	26
[50]	2	2	2	2	8	26	[51]	2	2	2	2	8	26
[52]	2	2	3	3	10	32	[53]	2	2	3	3	10	32
[54]	2	2	2	2	8	26	[55]	2	2	2	2	8	26
[56]	2	2	2	2	8	26	[57]	2	2	2	2	8	26
[58]	2	2	2	2	8	26	[59]	1	3	2	2	8	23
[60]	1	3	2	2	8	23	[61]	1	3	2	2	8	23
[62]	2	3	2	3	10	29	[63]	1	4	2	3	10	26
[64]	2	3	2	3	10	29	[65]	2	3	2	3	10	29
[66]	2	3	2	3	10	29	[67]	2	3	3	4	12	35
[68]	2	3	3	4	12	35	[69]	1	3	1	3	8	19
[70]	1	3	2	4	10	25	[71]	1	2	2	3	8	22
[72]	1	3	1	3	8	19	[73]	1	3	1	3	8	19
[74]	1	2	3	4	10	28	[75]	1	2	1	3	7	17
[76]	1	3	2	4	10	25	[77]	1	3	2	2	8	23
[78]	1	3	2	2	8	23	[79]	1	4	2	1	8	24
[80]	1	3	2	2	8	23	[81]	1	4	2	3	10	26
[82]	1	2	3	4	10	28	[83]	1	4	2	3	10	26
[84]	1	2	3	4	10	28	[85]	1	5	2	4	12	29
[86]	1	5	2	4	12	29	[87]	1	4	3	4	12	32
[88]	1	5	2	4	12	29	[89]	1	5	2	4	12	29
[90]	1	4	3	4	12	32	[91]	1	5	3	3	12	33
[92]	1	6	2	3	12	30	[93]	1	6	2	6	15	33
[94]	1	5	3	3	12	33	[95]	1	5	3	3	12	33
[96]	1	7	3	1	12	35	[97]	1	8	3	2	14	38
[98]	1	5	2	4	12	29	[99]	1	4	2	5	12	28
[100]	1	5	2	6	14	31	[101]	1	3	3	5	12	31
[102]	1	3	4	6	14	37	[103]	1	7	2	6	16	35
[104]	1	7	3	7	18	41	[105]	1	8	2	4	16	40
[106]	1	7	2	6	16	35	[107]	1	7	3	5	16	39
[108]	1	5	3	7	16	37	[109]	1	3	3	5	12	31
[110]	1	3	4	6	14	37	[111]	1	7	4	4	16	43
[112]	1	9	3	3	16	41	[113]	1	5	2	5	13	30
[114]	1	7	4	6	18	45	[115]	1	5	2	4	12	29
[116]	1	5	2	4	12	29	[117]	2	4	2	4	12	32
[118]	1	7	2	5	15	34	[119]	1	4	3	4	12	32
[120]	2	4	2	4	12	32	[121]	2	5	2	5	14	35
[122]	2	4	3	5	14	38	[123]	2	3	3	4	12	35
[124]	2	3	3	4	12	35	[125]	1	5	2	4	12	29
[126]	1	6	3	5	15	37	[127]	1	5	3	5	14	35
[128]	2	5	2	5	14	35	[129]	2	5	2	5	14	35
[130]	1	5	4	6	16	41	[131]	1	5	2	5	13	30
[132]	2	4	3	3	12	36	[133]	1	6	3	4	14	36
[134]	2	9	4	1	16	49	[135]	1	7	4	4	16	43
[136]	1	9	5	3	18	51	[137]	1	7	5	5	18	49
[138]	2	6	4	4	16	46	[139]	1	9	4	2	16	45
[140]	1	9	5	3	18	51							

FIGURE 67. Cost comparison.

step up the voltage significantly while minimizing the voltage stress on the single main switch. The complexity here underscores the performance trade-off: superior electrical characteristics are achieved at the cost of a larger physical footprint, increased component power losses, and heightened vulnerability to component failure. In conclusion, the component enumeration offers an effective hierarchical categorization, revealing a clear trend across the spectrum: increasing performance capability is primarily realized by selectively augmenting the complexity of the passive and diode-based gain stages—a strategy that preserves the fundamental simplicity of the active switch control.

Also, the cost comparison is done in Fig. 67. The cost comparison is done accordin to the RCI (Relative Cost Index). For the purpose of this comparative review, a ''Relative Cost Index'' (RCI) was developed. The objective of this index is not to predict the exact Bill of Materials (BOM) cost in dollars, which is impossible without knowing the precise operating specifications (like output voltage) and component ratings. Instead, the RCI serves as a robust metric for quantifying topological complexity and its strong correlation with total system cost. The RCI is calculated for each converter using the following weighted formula:

$$RCI = (5 \times N_{switch}) + (5 \times N_{inductor}) + (2 \times N_{diode}) + (1 \times N_{capacitor}) \quad (85)$$

where:

- N_{switch} = Total number of active switches (e.g., MOSFETs, IGBTs)
- $N_{inductor}$ = Total number of magnetic components (inductors and transformers)
- N_{diode} = Total number of diodes (rectifiers, Schottky diodes, etc.)
- $N_{capacitor}$ = Total number of capacitor functions (input, output, resonant, etc.)

The weights (5, 5, 2, 1) are not arbitrary. They are assigned based on the component's relative impact on the total system cost for a high-power (200W) application.

IV. SUITABLE APPLICATIONS FOR THE DISCUSSED DC–DC CONVERTERS

DC-DC converters are integral to numerous industrial sectors, including green hydrogen production ([141]), electric vehicles ([142], [143], [144], [145], [146]), photovoltaic (PV) panels ([147], [148], [149], [150], [151]), vehicle-integrated PV panels ([152], [153], [154], [155], [156], [157]), and thermal-to-electrical generators ([158]). Figure 68 symbolically illustrates the application of DC-DC converters in these diverse contexts. The deployment of modern distributed energy resources and advanced power systems necessitates the use of high-performance power conditioning stages. Non-isolated DC-DC converters are frequently selected as the core power interface due to their intrinsic high efficiency, reduced component count, and structural simplicity compared to their isolated counterparts. However, the operational constraints imposed by various energy sources and loads dictate specific, application-dependent requirements for the chosen topology. The following analysis details the essential features required

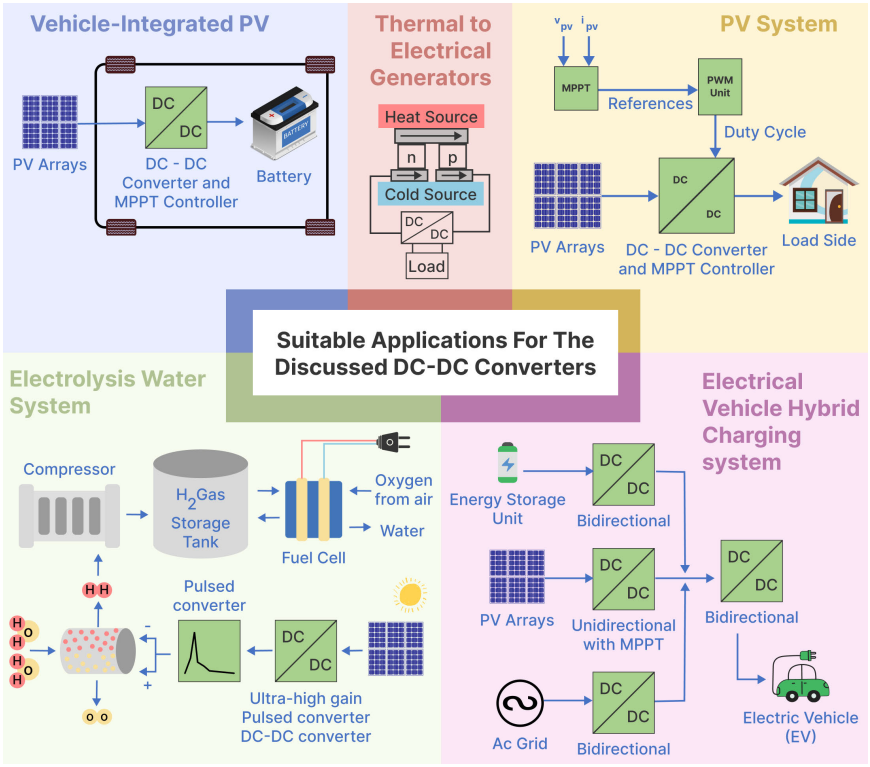

FIGURE 68. Suitable application of the discussed converters.

of non-isolated DC-DC converters across key emerging applications, as illustrated in the preceding figure.

- Vehicle-Integrated Photovoltaics (VIPV): In VIPV systems, the DC-DC converter manages the power flow between the rooftop PV array and the onboard battery. This application is fundamentally defined by the highly variable nature of the PV source and the strict constraints of the automotive environment. The primary requirement is the implementation of Maximum Power Point Tracking (MPPT) capability, achieved by actively controlling the converter's duty cycle to maintain the PV array's operation at its peak power output despite changing irradiance and temperature. Crucially, the converter must accommodate a Wide Input Voltage Range stemming from the PV source and deliver power to the comparatively fixed-voltage battery. Furthermore, a Continuous Input Current is essential to prevent pulsed loading of the PV array, which could diminish efficiency and reduce panel lifespan. Advanced VIPV may also require a Bidirectional Power Flow to facilitate functions such as regenerative braking energy recovery or Vehicle-to-Grid (V2G) applications. Finally, stringent High Power Density is a mandatory constraint due to the limited space and weight budget within a vehicle.
- Thermal to Electrical Generators (TEG): Thermoelectric Generators (TEGs) present one of the most challenging environments for DC-DC power conversion. TEGs produce electrical energy based on the Seebeck effect, typically generating a very Low Input Voltage (often less than 1 Volt) at a high current. Consequently, the single most critical feature for the DC-DC converter in this system is an Ultra-High Voltage Gain. The converter must step up the sub-volt input to a usable load voltage (e.g., 5V, 12V, or higher), often demanding boost ratios exceeding 10:1. This necessity drives the selection of highly specialized, non-isolated topologies, such as those employing quadratic boost stages or multi-stage inductor-based Voltage Multiplier Cells (VMCs). Given the typically low power output of TEGs, the converter must also exhibit High Efficiency at Low Power Levels, making minimized switching and conduction losses imperative to maximize the usable energy harvest. Similar to PV, an integrated MPPT control is necessary to optimize power extraction based on the temperature gradient.
- General Photovoltaic (PV) Systems: In residential or grid-tied PV systems, the non-isolated DC-DC converter functions as the primary power stage connecting the PV array to a high-voltage DC link (often 400 V or higher). The core demands here include achieving a High Voltage Gain to bridge the significant gap between the array voltage (e.g., 40V–100V) and the DC-link voltage. Paramount to system robustness and stability is the requirement for Purely Continuous Input Current across the entire operating range. A continuous input current ensures effective MPPT operation, reduces stress on the PV panels, and minimizes conducted electromagnetic

interference (EMI). Given the high gain requirement, the chosen topology must also feature Voltage Clamp/Stress Reduction mechanisms to limit the voltage spike across the main power switch, which would otherwise be excessive in conventional boost circuits operating at high duty cycles.

- Electrolysis Water System: Electrolysis systems, particularly those powered by renewable sources like Fuel Cells (FCs) or PV arrays, require DC-DC converters to manage power flow and achieve the high voltages needed for the electrolysis cell stack or an intermediate high-voltage bus. The conversion stage must deliver an Ultra-High Voltage Gain (e.g., 10:1 or more) to step up the low-voltage source to the required operational voltage of the system. While the primary converter delivers high voltage and must maintain Continuous Input Current (if connected to an FC or PV source), the ultimate application may benefit from a specialized, fast-acting, high-power Pulsed Converter to optimize the kinetics and efficiency of the electrochemical reaction within the cell itself. Furthermore, these systems often operate at substantial power levels, mandating non-isolated topologies capable of High Power Handling and robust thermal management.
- Electrical Vehicle Hybrid Charging System: The EV Hybrid Charging System represents the most complex application in terms of power management, integrating the AC grid, PV arrays, and an Energy Storage Unit (ESU) with the Electric Vehicle (EV) battery. The defining functional requirement across all converters connected to the ESU and the EV is Mandatory Bidirectional Power Flow. These converters must facilitate seamless power transfer both into (charging) and out of (discharging/V2G) the respective energy storage units. Given the nature of modern charging protocols, these converters must be designed for High Power Handling (fast charging) and must maintain High Efficiency during both forward and reverse power flows. The system demands that the non-isolated converters possess a Fast Dynamic Response to manage rapid mode switching between charging, discharging, and grid support functions, thus requiring highly controllable and robust bridge-based or bidirectional buck-boost non-isolated topologies.

In summary, the necessary features of non-isolated DC-DC converters are intrinsically linked to the operational demands of the application. The trend favors high-gain, single-switch topologies with continuous input current for renewable energy harvesting (PV, TEG), while bidirectional and high-power-density converters are essential for energy storage and mobility applications (VIPV, EV Charging). The component-intensive high-complexity converters identified in preceding analysis are directly leveraged in applications demanding Ultra-High Voltage Gain (TEG, Electrolysis).

V. CONCLUSION

This paper successfully delivered a focused, structural-based, and comprehensive review of over 100 high step-up DC-DC converter topologies that do not employ coupled inductors. The goal was to overcome the limitations of prior reviews by providing a deep, comparative analysis rooted in fundamental topological characteristics. The initial analysis of classic converters (Boost, Buck-Boost, Ćuk, SEPIC, and Zeta) confirmed that while they are structurally simple, their applicability for high-gain scenarios is fundamentally limited by high voltage stress on semiconductor devices (equal to or greater than the output voltage for most) and the severe efficiency degradation associated with high duty-cycle operation. The main body of work introduced a systematic framework to classify and compare the advanced topologies into 23 distinct groups, revealing the complex trade-offs between a converter's structural complexity and its overall performance. Key conclusions drawn from the quantitative comparisons include: Semiconductor Voltage Stress, Input/Output Current Characteristics, and Topological Complexity. In summary, the structural-based categorization and detailed comparative data provided in this review serve as an invaluable tool for power electronics engineers. It enables the quick identification and optimal selection of a non-isolated, high step-up DC-DC converter that meets specific application requirements—such as those demanding ultra-high voltage gain for electrolyzers or continuous input current for fuel cells, or bidirectional power flow for Electrical Vehicle Hybrid Charging Systems—by clearly linking performance metrics to intrinsic topological features.

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