

A Sub-GHz UWB Correlation Receiver for Wireless Biomedical Communication

Menno Vastenholt

A Thesis Submitted to
The Faculty of Electrical Engineering, Mathematics and Computer Science in Partial
Fulfilment of the Requirements for the Degree of
MASTER OF SCIENCE
in Electrical Engineering

Supervisor: Dr. ir. Wouter A. Serdijn

Thesis committee

Dr. ir. Wouter A. Serdijn
Dr. ir. Gerard J.M. Janssen
Dr. Reza Lotfi
ir. Mark Stoopman

Delft University of Technology

September 2014

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Section Bioelectronics

Faculty of Electrical Engineering, Mathematics and Computer Science

Delft University of Technology

Abstract

The advantages of microelectronics can be found in the biomedical industry, where the technology is used in neuroscience, surgical procedures etc. An example of these advantages is wireless communication for biomedical purposes. Wireless communication offers the possibility to enhance the functionality of the implantable device. Examples of this added functionality are monitoring and diagnosis.

In previous work done in the Department of Microelectronics, Section Bioelectronics in Delft, sub-GHz Ultra-Wideband biomedical communication was researched. This research resulted in the design of a transmitter architecture. Unfortunately, insufficient time was spent on the receiver end of the communication link. This thesis continues with the research in wireless biomedical communication in the sub-GHz Ultra-Wideband spectrum, with the primary goal of designing a suitable receiver architecture, thereby completing the communication link.

A system level design of a sub-GHz correlation receiver is presented in the first part of this thesis. This architecture makes use of the pulse generator that was previously specifically build for the transmitter, as a reference. A major advantage of the correlation receiver is its simple design; having a small number of components, thereby making it suitable for implantable devices. Research is performed on the correlation concept, of which specifications are derived in order to achieve optimum correlation (such as the maximum allowed timing deviation between the received pulse and the locally generated pulse). A test environment is built in order to test the designed receiver and compare its performance with other receiver architectures. Research on negative influences on the communication link is done, and this research is used for building the test environment. These negative influences are narrowband, noise and multipath interference. Simulations performed with said test environment show that the correlation receiver is robust against the mentioned negative influences, while also having a better performance compared to other receiver architectures (such as an energy detector and a quadrature autocorrelation receiver).

In the last part of the thesis, a MOS-only, four-quadrant, low power, 1 GHz multiplier circuit is designed, using AustriaMicroSystems 0.18 μm High-Voltage CMOS technology. Circuit simulations show that the multiplier circuit is robust over process variations, device mismatch, temperature and supply voltage variations. The circuit was designed to operate for a 1.2 V supply, and has an average power consumption of 153.2 μW . The multiplier circuit is then embedded into the system design of the correlation receiver, in the aforementioned test environment. The designed multiplier was compared here with the performance of an ideal multiplier. It is shown that the designed multiplier is suitable for the correlation receiver.

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List of Abbreviations

ADC	Analog-to-Digital Converter
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase-Shift Keying
DHTR	Delay-Hopped Transmitted Reference
IC	Integrated Circuit
LNA	Low Noise Amplifier
NRZ	Non-Return-to-Zero
OOK	On-Off Keying
PRF	Pulse Repetition Frequency
PSD	Power Spectral Density
QDAcR	Quadrature Downconversion Autocorrelation Receiver
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
UWB	Ultra-Wideband

1 Introduction

For the past decades, microelectronics has grown (or rather “shrunk”) to the point where it is almost impossible to imagine our everyday lives without its influence. Whether it’s in mobile communication, the automotive industry or the defense industry, microelectronics has greatly improved these markets. The advantages of microelectronics are also found in the biomedical industry, where the technology is used in neuroscience, surgical procedures etc. An example of these advantages is wireless communication for biomedical purposes. In this field, there is still much research to be done. This thesis focuses on wireless biomedical communication.

1.1 Wireless Biomedical Communication

Since the beginning of the field of biomedical engineering, its primary goal has been to close the gap between engineering and medicine. This means combining the design and problem solving skills of engineering with medical and biological sciences to advance healthcare treatment, including diagnosis, monitoring, treatment and therapy. An example of the engineering and medical science combination is the implantable device such as the artificial cardiac pacemaker. This device, first introduced in 1958, is used as a treatment for patients with heart rhythm disorders. The original pacemaker only covered the treatment application of medical science, where diagnosis and monitoring still had to be done externally by a physician. Now, the goal is to also be able to use the implantable device in all of the applications within healthcare treatment.

Wireless communication offers the possibility to enhance the functionality of the implantable device. Previously, once the device was implanted inside a patient the physician could no longer influence the device without surgery, an uncomfortable procedure for the patient. Influencing the implantable device via percutaneous access (i.e. access via needle puncture through the skin) and the use of wires is a solution but also very uncomfortable for the patient. Percutaneous connection increases the risk of infection. A non-invasive solution is preferred. This is where wireless communication is used as an outcome, since it doesn’t affect the comfort of the patient.

The implantable device can also be used for monitoring as well as diagnosis, where it monitors the health of the patient and then transmits the collected data to the outside of the body on demand. All of this is done without reducing the comfort of the patient. Therefore, wireless biomedical communication is a crucial part in improving the efficacy in healthcare treatment, as well as the quality of life for the patient.

1.1.1 Previously done research

In the Department of Microelectronics, Section Bioelectronics, in Delft, Wireless Biomedical Communication has previously been researched by Mark Stoopman for his MSc. thesis [1]. A suitable communication channel was identified (sub-GHz Ultra-Wideband, which will be discussed later), the electrical characteristics of human tissue were investigated and various antennas were tested within muscle simulating liquid and raw pork meat to represent the human body. Based on this research a

transmitter architecture for use in implantable devices was designed. Because of the duration of the project little time had been spent on the design of the receiver end to complete the communication link.

This thesis continues with the research in wireless biomedical communication in the sub-GHz Ultra-Wideband spectrum. The primary goal is to design a suitable receiver architecture, thereby completing the communication link.

1.2 Ultra-Wideband Communication

Ultra-Wideband Communication (UWB) is a radio technology for short to medium range (indoor) communications. It is based on the concept that by increasing the bandwidth of the signal the channel capacity also increases/improves. This concept is seen in Shannon-Hartley's formula for channel capacity [2]:

$$C = B \log_2 \left(1 + \frac{S}{N} \right) \quad (1.1)$$

where C is the channel capacity in bits per second, B is the bandwidth of the channel in hertz, S is the average received signal power over the bandwidth measured in watts and N is the Average White Gaussian Noise (AWGN) over the bandwidth measured in watts. Furthermore, S/N is defined as the signal-to-noise ratio (SNR). Note that the channel capacity is directly proportional to the bandwidth, whereas the SNR is only logarithmically proportional to the channel capacity. In other words, the usage of UWB signals directly translates into higher channel capacity, whereas increasing only the SNR will have much less improvement on the channel capacity.

1.2.1 UWB regulations

Due to the wideband nature of UWB emissions, it could potentially interfere with other licensed bands in the frequency domain if left unregulated. For this reason the Federal Communications Commission (FCC) issued UWB regulations in 2002 [3]. According to the FCC, UWB is defined as any wireless transmission scheme that occupies a bandwidth of more than 20% of its center frequency, or more than 500 MHz. This definition holds only for the United States, since there are no worldwide regulations for UWB communication. Asia (the Japan's Ministry of Internal Affairs and Communications, or MIC) and Europe (the European Telecommunications Standards Institute, or ETSI) have devised their own regulations, although these are still in discussion. This thesis will primarily follow the FCC regulations, since most recent designs use the FCC mask as emission limit.

Figure 1.1, on the next page, shows the general FCC emission limits for indoor and outdoor UWB communication in the United States.

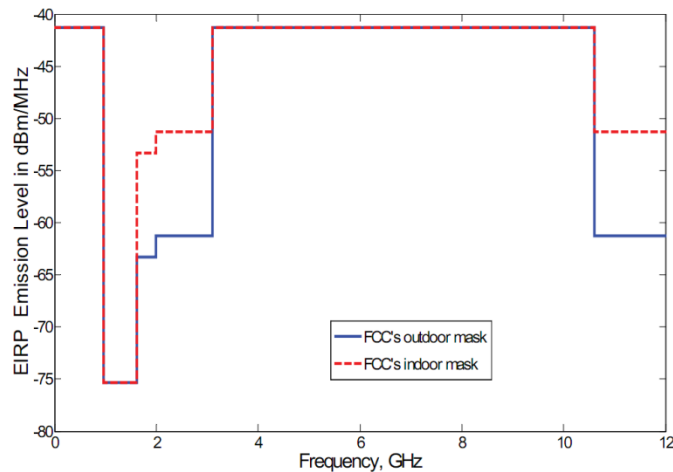


Figure 1.1: FCC indoor and outdoor UWB emission masks

As shown in Figure 1.1 the band allocated for UWB use is most prominently from 3.1 GHz to 10.6 GHz. The maximum allowed power emission level is at -41.3 dBm/MHz, which confines UWB to indoor, short range communications. There is also room left in the sub-GHz region (0 Hz to 960 MHz) for UWB purposes.

The FCC has made the 402-405 MHz band available for wireless biomedical communication, since this band satisfies the requirements with respect to EM wave penetration, antenna size, performance and receiver design. This band only specifies *narrowband* biomedical communications, as there are no specific regulations for UWB biomedical communications yet.

1.2.2 UWB in Biomedical applications

UWB shows promising qualities in the use of wireless biomedical communication, as it operates at low power (which is an important requirement for implantable devices, as will be discussed later) and at low-data rate. UWB is also robust to narrowband and multi-user interference, which is an advantage when the patient is in a hospital, surrounded by electronically radiating equipment. Furthermore, UWB signal penetration into a medium is low-loss, which is an advantage when the signal has to travel through the human body.

Its short to medium range characteristic is no issue for biomedical technology, since there are no developments in biomedical communications that require long range applications.

1.3 System Requirements

This section discusses the system requirements that have to be taken into account when designing the receiver. These requirements are:

- Compatibility
- Sizing
- Power Consumption
- Reliable Communication Link

Each of the listed system requirements are discussed in more detail below.

Compatibility

As the transmitter end of the communication system has already been fully designed, it is desirable to build a receiver structure that is compatible with the transmitter. For instance, the transmitter operates with the Binary Phase-Shift Keying (BPSK) scheme, so the receiver should be able to detect the two different phases of the incoming signal. Furthermore, any necessary adjustments to the transmitter as a result of the receiver design should be avoided.

Note that, when the transmitter was designed, it was assumed that only the transmitter would be implanted in the human body, and that the receiver end would operate outside of the human body [1]. This restricts the communication link to being unidirectional only. As discussed previously, a bidirectional communication link is preferred. Therefore, like the transmitter, the receiver architecture should also be designed for implantable devices.

Sizing

The receiver has to be implanted in the human body, so an as small-as-possible approach has to be maintained. This is because the area in implantable devices is extremely limited. A simplistic design with a small amount of components is preferred. Also, when designing the integrated circuit of the receiver, the use of bulky components should be avoided.

Power Consumption

Implantable devices operate on battery power. This puts restrictions on the operation of the device since batteries have a fixed energy density and limited lifetime. Changing an empty battery of the implantable device would require surgery, which should be avoided. Therefore, an ultra-low approach is preferred in order to extend the lifetime of the battery.

Reliable Communication Link

Reliability in the communication link is perhaps the most important requirement as well as the biggest challenge. There are a number of factors that can negatively influence the communication link between transmitter and receiver, such as noise, electromagnetic interference, multipath interference and signal distortion caused by the human body.

1.4 Research Objectives

This work focuses on the receiving end of the biomedical communication system. Most notably the issue of negative influences on the communication link have to be investigated. Also, since the transmitter end of the communication link has been established, a suitable receiver architecture that is compatible with this transmitter is designed.

The following research tasks that are discussed in this thesis are:

- Determine negative influences (in terms of signal processing) on communication link.

- Investigate different types of receiver architectures.
- System level design and analysis of the receiver.
- Circuit level design of a low-power multiplier for correlation purposes.

1.5 Thesis Outline

This thesis is organised as follows. The system level design is discussed in Chapter 2. The signal characteristics, derived from the already designed transmitter, are discussed and used for finding a suitable receiver architecture. Once a receiver architecture is chosen, a simulation program (Matlab) is used to test the functionality of the receiver and whether the receiver contributes to the reliability of the communication link. Several negative influences in signal processing on the wireless transfer are taken into account, such as noise, electromagnetic interference etc. The simulation results are discussed and compared with other receiver architectures in the last part of the chapter.

Chapter 3 focuses on the circuit design of a low-power, analog multiplier for use in the receiver architecture. Various multiplier topologies are discussed of which a suitable architecture is further developed.

Chapter 4 tests the designed multiplier from Chapter 3 on its functionality. The multiplier is also tested on its robustness by varying process corners, device mismatch, supply voltage and temperature. Finally, Chapter 4 combines the previous two chapters by implementing the designed multiplier from Chapter 3 in the overall system design of the developed receiver in Chapter 2. The overall system design is again tested and simulated to check its overall robustness.

The thesis ends with the fifth and last chapter on conclusions, scientific contributions and recommendations.

2 System Design

This chapter discusses the system design of an UWB receiver. First, characteristics of the signal to be received are discussed. Next, all negative influences that can affect the wireless communication link have to be examined. Once the signal characteristics and the negative influences in signal processing are known, the receiver topology can be designed. Several receiver topologies are examined for their compatibility with the communication link. The system requirements discussed in the first chapter are also taken into account. A suitable receiver topology is then chosen and further developed in the simulation program MATLAB. Finally, simulation results from the designed receiver are shown and compared with other receiver architectures at the end of this chapter.

2.1 Signal Characteristics

Previously, during his Msc. thesis work, Mark Stoopman proposed a suitable communication channel for wireless biomedical communication [1]. The specifications of this communication channel, which have to be taken into account when designing the UWB receiver, are directly taken from his work and briefly summed up in this section. Further information of how the channel was designed can be found in his thesis work.

Signal Parameters

The main signal parameters that are of significance for this thesis are summed up in Table 2.1. Further comments on these signal parameters are discussed below.

Table 2.1: Signal Parameters

Term	Data	Unit	Comment
R_b	1	Mb/s	Bit Rate
d	5	m	Distance (Range)
T_{Pulse}	6	ns	Pulse width
DC	0.6	%	Duty Cycle ($DC = T_{\text{Pulse}} \cdot R_b$)
PRF	1	MHz	Pulse Repetition Frequency
f_{BW}	500	MHz	-10 dB Bandwidth
f_{H}	1	GHz	-10 dB Upper Frequency
f_{L}	500	MHz	-10 dB Lower Frequency
f_{C}	750	MHz	Center Frequency

The bitrate R_b was established as a trade-off between bitrate and power consumption. The amount of data in the case of biomedical communication seldom exceeds 1 Mb/s, therefore a low bitrate of 1 Mb/s was established.

The distance d between the transmitting and receiving antennas is set at a short 5 meters (UWB is only beneficial for short distances). An average sized room (15-20 m²), such as a hospital room where the patient resides, has been assumed.

The pulse width T_{Pulse} and the Pulse Repetition Frequency PRF define the pulse shape. In this case, the UWB signal is a Gaussian pulse train. The PRF defines the repetition of this pulse train, T_{Pulse} defines the width of every individual Gaussian pulse.

The frequency terms f_{BW} , f_H , f_L and f_c define the bandwidth of the signal. Signals in UWB technology are defined, according to the FCC, to have a fractional bandwidth greater than 0.20 or occupy 500 MHz or more of the spectrum. Mathematically, this fractional bandwidth (B_{frac}) is expressed as:

$$B_{frac} = 2 \cdot \frac{f_H - f_L}{f_H + f_L} \quad (2.1)$$

where f_H is the upper frequency and f_L is the lower frequency of the -10dB emission point. The center frequency f_c of the transmission is defined as the average of the upper and lower -10dB points:

$$f_c = \frac{f_H + f_L}{2} \quad (2.2)$$

From Equation (2.1) it is concluded that the fractional bandwidth of the signal is $B_{frac} = 0.67$, which complies with the FCC definition of an UWB signal, since the fractional bandwidth is greater than 0.2.

The duty cycle DC defines the operation per cycle that a single pulse is transmitted, and is calculated by the pulse width multiplied with the bitrate. The fact that the duty cycle is so low (0.6%) shows the advantage of UWB in terms of low power consumption.

In terms of power, the transmitter drives the antenna with an average pulse power of 54.95 μW . Its peak pulse current is 5.5 mA. With this data the Power Spectral Density (PSD) of the emitted signal, as well as the E-field at a certain distance from the transmitting antenna can be calculated. This emission analysis was performed using CST Microwave Studio. Figure 2.1 shows the simulated E-field at a distance of 5 meters from the emitting antenna [1].

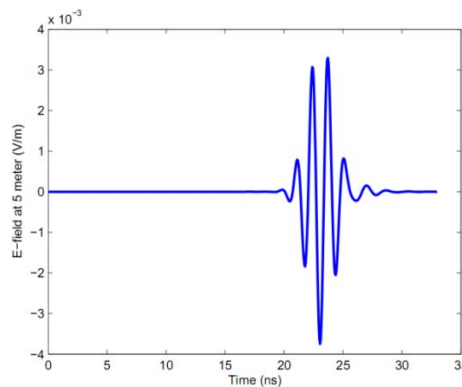


Figure 2.1: Simulated E-field at 5 meters [1]

Despite signal amplitude loss and modifications in the shape, it is also visible from Figure 2.1 that the Gaussian shape is still clearly present. This may help with the reliability of the communication link, which will be discussed further later on.

The pulse shape with the properties described above is shown in Figure 2.2a. Note that this graph displays the current that is driving the antenna on the transmitter side. The pulse train of the signal, with its PRF of 1 MHz, is shown in Figure 2.2b. The Power Spectral Density of the signal, along with the FCC emission mask, is shown in Figure 2.2c.

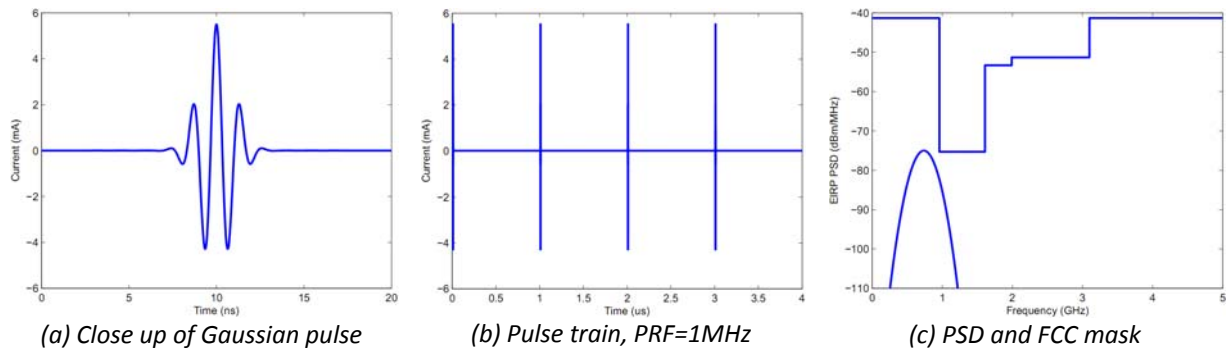


Figure 2.2: Gaussian Pulse Train [1]

Modulation scheme

The transmitter is designed so that it is able to change the polarity of the pulse. This means that the transmitter is suitable for either Binary Phase-Shift Keying (BPSK) or On-Off Keying (OOK).

In terms of low power consumption, OOK would be the most suitable choice. The binary information is encoded in the presence or absence of the symbol waveform. This scheme reduces the power consumption of the transmitter, since it doesn't transmit the '0' bits in the binary code. However, OOK has some issues in its robustness. For instance no reception can be considered as a logic '0'. It is also prone to amplitude related interference: overall noise can be mistaken for binary information.

In case a higher SNR is required, BPSK would be a better choice. Here the binary information ('0' or '1') is directly translated into the polarity. This does however increase the power consumption on the transmitter side.

2.2 Negative influences on communication link

This section discusses the different factors in the communication band that have a negative influence (i.e. distortion) on the signal to be measured. These influences are narrowband interference, multipath interference and noise. They are discussed here since they have to be simulated later on in Matlab in order to test the designed receiver architecture.

2.2.1 Narrowband Interference

Narrowband communication is a widely used system for wireless communication. Since UWB systems transmit signals over a wide frequency range, they're bound to overlap with existing narrowband systems. Below is a summary of several narrowband systems currently in use.

IEEE 802.11, Wireless LAN

The IEEE 802.11 is a set of physical layer standards for implementing wireless local area network (LAN) computer communication. It was first established in 1997, at 2.4 GHz, and has subsequent amendments throughout the years. These standards provide the basis for wireless network products using the Wi-Fi brand.

Currently wireless LAN communication is implemented in 2.4, 3.6, 5 and 60 GHz frequency bands. The 2.4 and 5 GHz bands are the more regulated bands.

GPS Frequency Bands

The frequency band from 0.96 to 1.61 GHz is reserved for GPS. Its strong presence in the spectrum is visible when observing Figure 1.1. More specifically, satellites broadcast information at 1227.6 and 1575.42 MHz (for civilian and military use). According to the FCC, jamming or interfering these frequencies is against the law.

GSM Frequency Bands

GSM frequency bands are the cellular frequencies designated by the ITU (International Telecommunication Union) for the operation of GSM mobile phones. The ones used in most parts of the world (Europe, Middle East, Africa, Australia, most of Asia and some countries in South and Central America) are *GSM-900*, *GSM-1800* and *EGSM/EGSM-900*. *GSM-850* and *GSM-1900* are used in the United States, Canada and other countries in the Americas. The *2,100 MHz* band is also in use in Brazil for 3G services.

Note that, from the number of narrowband signals that have been investigated, only the 900 MHz GSM band overlaps with the proposed biomedical UWB signal. This may help reduce the strain on the robustness of the receiver architecture. All the narrowband signals outside the proposed UWB signal can be removed by a proper band pass filter.

2.2.2 Multipath Interference

Multipath Interference is the distortion of a signal caused by that same signal taking different paths to reach the receiving antenna. This causes phase and polarisation shifts, thus interfering with the “original signal” (the one that takes the path of least distance). While it is mostly a problem in narrowband technology (for instance in the GSM industry), it also affects UWB transmissions.

There are two factors that influence multipath interference. One is the environment where the transceiver is placed. A small sized room will have more effect on multipath than an outdoor environment with less obstacles. Since the transceiver is being designed for biomedical purposes, it is assumed that it will be placed in an indoor hospital environment, albeit with concrete walls and floors. There are known studies where the multipath effect on UWB has been tested in different environments [4]. The other factor for multipath interference is the distance between the transmitting and receiving antennas. As this distance decreases, the number of paths should also decrease (causing less distortion on the original signal).

2.2.3 Noise

White noise is the most common occurrence in signal processing. Its random signal contains equal power within any frequency band with a fixed width. It is especially a factor in UWB communication since the UWB signal amplitude often resides below the noise floor. This causes decrease in SNR, and bursts of error can occur in the information transport.

A basic and generally accepted model for noise in communication channels is Additive White Gaussian Noise (AWGN). This model has a flat Power Spectral Density, a Gaussian distribution and the noise is additive to the transmitted signal. The use of this model to test a receiver design (in Matlab) will be discussed later in this chapter.

2.3 Receiver topologies

In this section, several receiver topologies are discussed, along with their advantages and disadvantages. Compatibility with the already designed transmitter topology, and its corresponding data output, is taken into account.

2.3.1 Rake receiver

A Rake receiver is an UWB receiver specifically designed to counter the effects of multipath fading. It consists of several sub-receivers (also known as fingers), each assigned to a different multipath component [5]. An increase in the number of sub-receivers that a Rake receiver consists of translates to an increase in performance of the overall receiver.

An example of a Rake receiver with an N-number of parallel fingers [6] is shown in Figure 2.3.

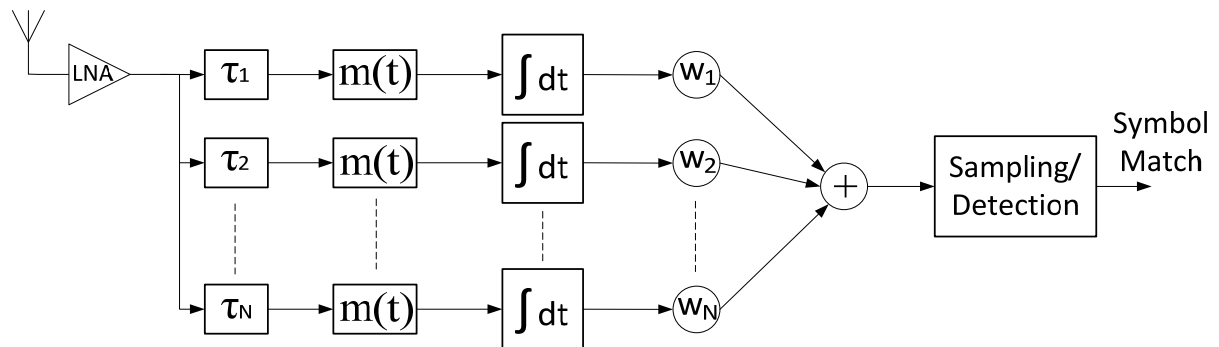


Figure 2.3: A Rake receiver with N parallel fingers [6]

As shown in Figure 2.3, each sub-receiver consists of a time delay element τ (which function is to align the multipath component in time), a correlator mask $m(t)$, an integrator and finally a weighting function w . The result of each sub-receiver is then combined for sampling/detection. The relation in which each result is combined is determined by the weighting function. Different types of weighting schemes can be utilised, such as Maximum Ratio Combining (MRC), Selection Diversity (SD), Equal Gain Combining (EGC) etc. The choice of a weighting scheme depends on the type of receiver and the desired structure complexity.

The main disadvantage of the Rake receiver is that its number of multipath components is directly proportional to its hardware complexity [7]. In some cases, several hundreds of fingers may be required for detection. This translates to increase in size of the hardware, power consumption and fabrication cost. There has been research in designing low-power, low-complexity rake receiver architectures [8], but since size and power are important requirements for wireless biomedical communication it is decided other receiver architectures may be more suitable.

2.3.2 Energy detection

Energy detection is a non-coherent approach for UWB signal reception, where low complexity receivers can be achieved. It detects the presence of a signal by measuring its energy and comparing the measured energy with a predetermined threshold [9].

As opposed to the Rake receiver, estimation of individual pulse shapes, path amplitudes and delays at each multipath component are not necessary for energy detectors. Energy detectors are also less sensitive against synchronization errors and are capable of collecting the energy from all the multipath components.

A block diagram of an energy detection UWB receiver is shown in Figure 2.4 [10].

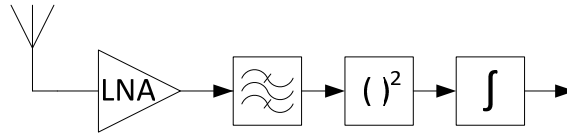


Figure 2.4: Energy Detector [10]

As shown in Figure 2.4, the received signal is first amplified and filtered by the Low Noise Amplifier and Band Pass Filter. Next, the squarer and integrator detect the energy of the received pulse. The major advantage of the energy detector above other receivers is its quick and simplistic design, consisting of only a few blocks. All blocks are easily designable on circuit level. For instance, the squaring function can be designed by several techniques, such as a Gilbert cell mixer or MOS transistors operating in saturation, triode or sub-threshold region [10].

Unfortunately, the energy detector underperforms in the case of high noise levels. Once the noise exceeds the signal amplitude the SNR decreases to the point where valid information can no longer be received. This phenomenon is noticeable when observing the detection process mathematically:

$$g(t) = A(t) \cos(\omega_c t) + n(t) \quad (2.3)$$

In Equation (2.3), an UWB signal $g(t)$ is defined with amplitude $A(t)$, carrier frequency ω_c and additive noise $n(t)$. This signal is processed by the squarer function, as shown in Equation (2.4).

$$[g(t)]^2 = [A(t) \cos(\omega_c t) + n(t)]^2 \quad (2.4)$$

$$[g(t)]^2 = A(t)^2 \cos^2(\omega_c t) + 2A(t) \cos(\omega_c t) \cdot n(t) + n(t)^2 \quad (2.5)$$

In Equation (2.5) it is clear that both the UWB signal as well as the noise are squared. Also, the noise is correlated with the UWB signal. Even though this part can be removed by a filter, the squared noise part still remains. If $n(t) > A(t)$ then the noise will be the dominant factor in the end result.

There are ways to improve the performance of the energy detector [11], which usually involves adding complexity to its design. This however beats the overall advantage of the simplicity of the energy detector over other receivers. For this reason the use of the energy detector is discarded.

2.3.3 Subsampling

Subsampling receivers are usually found in narrowband communication systems [12], however research has shown that this type of receiver is also suitable for wideband [13] and UWB [14] communication. Here an incoming signal is sampled at a frequency lower than the incoming signal frequency. The sampled signal is then further processed in the digital domain via an Analog-to-Digital conversion. The subsampling receiver has the advantage of operating in low power because of its low frequency sampling, making it a suitable choice for wireless biomedical communication. The addition of a digital signal processor makes for a smaller number of necessary (analog) components than with the RAKE receiver.

Figure 2.5 shows an example of a subsampling receiver for UWB communication, in this case a Direct-Conversion architecture [15].

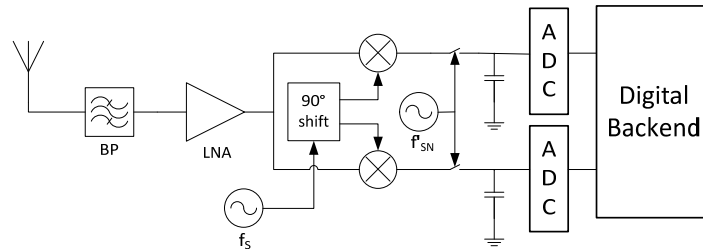


Figure 2.5: Direct-Conversion Subsampling architecture [15]

As shown in Figure 2.5, this receiver architecture consists of two separate subsampling stages. The first subsampling stage down converts the incoming RF signal by a sampling frequency f_s to lower intermediate frequencies (between 0 and $f_s/2$ Hz). The second subsampling stage down converts the signal further to baseband, with sampling frequency f'_{SN} , for the Analog-to-Digital Converters (ADC). The ADC's then transfer the sampled signal to a digital backend for further processing. The reason for having two subsampling stages in the example shown in Figure 2.5 is the difficulty in choosing a suitable sampling frequency if there is only one stage in the receiver architecture. A high sampling frequency is required to prevent jitter and thermal noise, however this requires faster operation from the ADC's and thus causes excessive power dissipation.

Unfortunately the subsampling receiver has some drawbacks when operating in UWB communication. The subsampling receiver has a low resistance against narrowband interference, as it collects all information/energy in the RF band (including interferers) and adds this information at

baseband. Since narrowband signals have a higher amplitude than UWB signals, they will be more present in the output result than the required UWB information. Also, this type of receiver has a high sensitivity to timing offsets, which can be introduced by frequency and phase mismatch between the transmitter and receiver oscillators. The addition of digital components to the design is also a reason why this receiver is neglected. The addition of digital components may add flexibility, but also introduces more complexity to the signal processing. A receiver that already collects the incoming information in the analog domain is preferred.

2.3.4 Autocorrelation

The autocorrelation receiver makes use of a delay-hopped transmitted reference system (DHTR), which was first proposed by Hoor and Tomlinson [16]. The basic transmitted reference communications system is defined as such that two versions of a wideband carrier are transmitted, one modulated by data and the other unmodulated. The modulated and unmodulated versions are typically separated from one another either in time or in frequency. In the case of DHTR, the two waveforms are separated in time. The carriers used may be either RF pulses or continuous, wideband (pseudo-) noise.

The core part of the transmitted reference scheme receiver, also known as the autocorrelation receiver, is shown in Figure 2.6 [17].

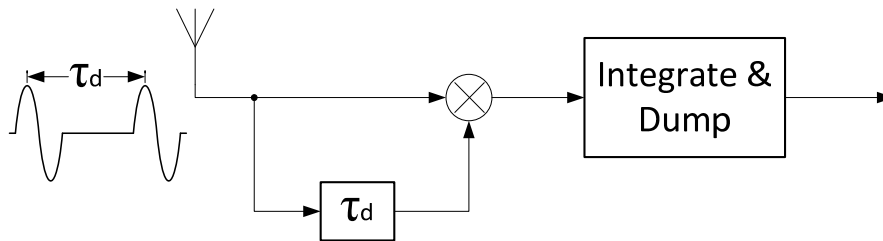


Figure 2.6: Autocorrelation receiver with example waveform

In the autocorrelation receiver, two pulses per symbol are sent with a chosen delay τ_d between them. The first pulse acts as the reference and the second pulse is the modulated one. The receiver delays the first pulse (by the delay function τ_d), multiplies it with the second pulse and integrates the result over one delay length, which correlates the two pulses. This type of receiver is useful for modulation schemes such as BPSK or Non-Return-to-Zero (NRZ). For a logical zero the modulated/second pulse is polarity reversed compared to the reference/first pulse, whereas for a logical one both the reference and the modulated pulse have the same polarity. The absolute value of the output after integration is the energy of the pulse while the polarity of the output contains the digital data. Thus, the information is in the relative polarity of the two pulses and the delay between them acts as a synchronisation mechanism. An important factor in this type of receiver is that as long as the two consecutive pulses have corresponding waveforms, except for their polarity, the autocorrelation receiver can detect them properly.

An example of a receiver architecture that makes use of the autocorrelation receiver concept is the Quadrature Downconversion Autocorrelation Receiver (QDAcR) [17], as shown in Figure 2.7.

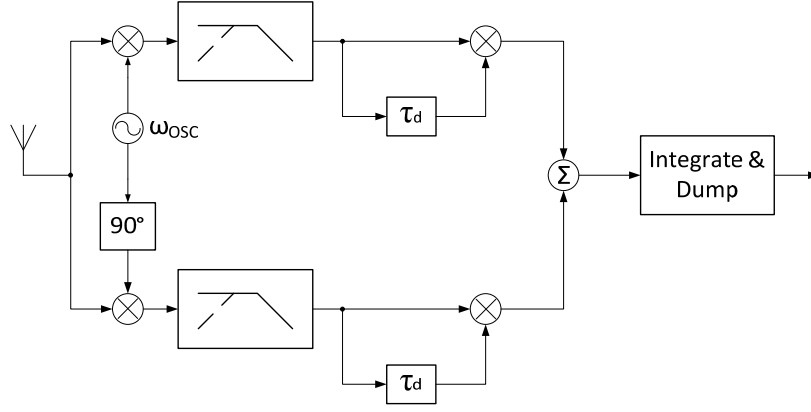


Figure 2.7: Quadrature Downconversion Autocorrelation Receiver

The QDAcR employs frequency conversion, as shown by the local oscillator ω_{osc} in Figure 2.7. Its frequency is chosen such that the spectrum of the incoming signal wraps around baseband. The advantage of this technique is that further processing is now done at lower frequencies, which reduces power consumption and on-chip circuit area. This technique is also useful for interference rejection, since narrowband interferers can be either down- or upconverted and subsequently filtered out. Also note that the incoming signal is fed into two pathways, the difference between the pathways being that the upper pathway is mixed with ω_{osc} , and the lower pathway is mixed with a 90° out-of-phase version of ω_{osc} . When both pathways are added up before integration, the frequency conversion parts cancel each other (since $\sin(\omega_{osc}t)^2 + \cos(\omega_{osc}t)^2 = 1$).

Time Domain Analysis

Using time domain analysis, the processing of the QDAcR looks as follows. The received signal can be written as:

$$g(t) = A(t) \cos(\omega_c t) \quad (2.6)$$

Where $A(t)$ is the amplitude of the envelope and ω_c the carrier frequency. The phase $\varphi(t)$ of the signal is not included for ease of calculation. Note that Equation (2.6) only defines the first (reference) pulse. The second (carrier) pulse, which is delayed by τ_d , is written as:

$$g(t - \tau_d) = A(t - \tau_d) \cos(\omega_c \cdot (t - \tau_d)) \quad (2.7)$$

Both pulses are frequency converted and then the higher frequency parts are removed because of the low pass filter. Equations (2.6) and (2.7) subsequently become:

$$\frac{1}{2} A(t) \cos((\omega_c - \omega_{osc})t) \quad (2.8)$$

$$\frac{1}{2} A(t - \tau_d) \cos((\omega_c - \omega_{osc})(t - \tau_d)) \quad (2.9)$$

$$\frac{1}{2} A(t) \sin((\omega_{osc} - \omega_c)t) \quad (2.10)$$

$$\frac{1}{2} A(t - \tau_d) \sin((\omega_{osc} - \omega_c)(t - \tau_d)) \quad (2.11)$$

(2.8) and (2.9) describe the pulses in the lower pathway, (2.10) and (2.11) describe the pulses in the upper pathway. In the autocorrelation part, (2.8) and (2.9) are multiplied with each other and (2.10) and (2.11) are multiplied with each other. Both results are then added up before integration. This results in:

$$\frac{1}{4}A(t - \tau_d)^2 \cos(\omega_{osc}\tau_d) \quad (2.12)$$

As shown in Equation (2.12), the end result is now dependent on $\omega_{osc}\tau_d$, which has to be $2\pi n$ (with n being a natural number). Otherwise the output performance of the QDAcR will degrade. In worst case, i.e. $\omega_{osc}\tau_d = \frac{1}{2}\pi$, the output will be zero, regardless of the transmitted data and detection.

Drawbacks

The QDAcR does have some drawbacks, mainly in the delay function block. The accuracy in the timing delay, at both the transmitter and the receiver ends, is important in acquiring nominal information. Any timing deviations will result in performance degradation. Also, the delay block itself is difficult to fabricate from a circuit design point of view. Different types of circuits have been designed for this specific function ([18],[19],[20]), and most (if not all) of these designs are either complex, are difficult to control, exhibit distortion in waveform or have high power consumption. For these reasons the QDAcR is yet to be successfully used in real applications.

2.3.5 Correlation

As discussed previously in Subsection 2.3.4, the autocorrelation receiver shows improved results in terms of SNR compared to other UWB receiver models [17],[21]. However, because of implementation difficulties (specifically the delay function) the QDAcR is yet to be used in real applications. Still, the concept of multiplying the UWB carrier signal with a reference signal proves to be useful. For this reason, the concept of the correlation receiver is looked into. The correlation receiver is an old receiver concept. with publications dating back to 1960 ([22], page 375). The use of the correlation receiver was to detect weak signals. Figure 2.8 shows a basic design of this type of concept.

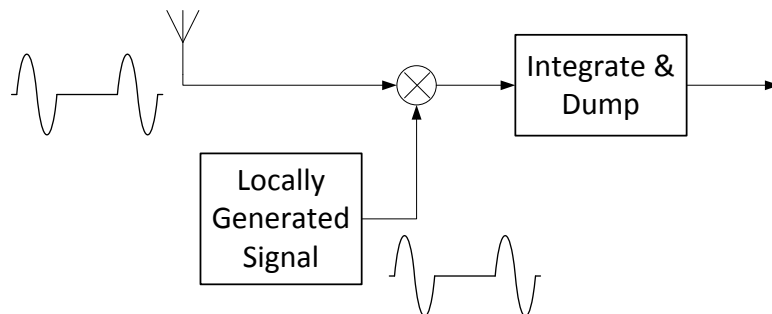


Figure 2.8: Basic concept of the correlation receiver

As shown in Figure 2.8, the correlation receiver makes use of a locally stored replica of the transmitted signal, and multiplies this with the incoming signal. The result after multiplication is then integrated, which completes the correlation process. The advantage of using a locally generated

replica over the transmitted reference scheme with the QDAcR is that the locally generated signal is not influenced by noise or interference that occur during wireless transmission, which should improve the overall SNR after correlation. This theory can be tested mathematically by time domain analysis, as shown below.

Time Domain Analysis

In time domain analysis, the processing within the correlation receiver looks as follows:

$$g(t) = A(t) \cos(\omega_c t) \quad (2.13)$$

$$f(t) = A(t) \cos(\omega_c t) \quad (2.14)$$

The transmitted signal is defined as $g(t)$, the reference signal at the receiver end is defined as $f(t)$. These definitions for an UWB pulse are the same as used in Subsection 2.3.4. Since the circuit that generates these signals are the same in the transmitter and the receiver, both signals are equal. Note that for simplicity noise and narrowband interference for $g(t)$ are, for now, not taken into account.

Both signals are multiplied with each other:

$$g(t) \times f(t) = A(t) \cos(\omega_c t) \times A(t) \cos(\omega_c t) \quad (2.15)$$

Equation (2.15) is rewritten using $\cos(a) \cos(b) = \frac{1}{2} [\cos(a + b) + \cos(a - b)]$:

$$g(t) \times f(t) = \frac{1}{2} A(t)^2 [\cos(2\omega_c t) + 1] \quad (2.16)$$

Finally an ideal low pass filter is used to remove the higher frequencies:

$$\frac{1}{2} A(t)^2 \quad (2.17)$$

When comparing the result from (2.19) with (2.12), the end result of the QDAcR, it is shown that, mathematically speaking, the correlation receiver can derive at least twice as much energy from the incoming signal.

The concept can also be tested mathematically with noise. The noise is additive to the incoming signal $g(t)$:

$$g(t) = A(t) \cos(\omega_c t) + n(t) \quad (2.18)$$

The incoming signal is then multiplied with the locally generated signal:

$$g(t) \times f(t) = A(t)^2 \cos(\omega_c t)^2 + A(t) \cos(\omega_c t) \cdot n(t) \quad (2.19)$$

From (2.19) it can be observed that the noise part on the right is now situated around the carrier frequency, while the information part on the left is down converted to lower frequencies. This means that, mathematically speaking, by using a low pass filter after multiplication, the noise can be

removed. This shows improved noise performance compared to the Energy Detection receiver, discussed in Subsection 2.3.2.

Conclusion

An advantage of the correlation receiver over the other receivers discussed in this chapter is the simplicity in its design. As shown in Figure 2.8, the core of its design only requires a block that generates the replica signal, a multiplier and an integrator. It does not require additional components for downconversion (such as with, for instance, the QDAcR) since this is already done by the multiplication component. The circuit that is needed to generate the replica signal is already available, as it has been designed by Mark Stoopman [1]. Furthermore the multiplier and integrator can also be realised in circuit design.

Unfortunately the concept of the correlation receiver has never been popular in (UWB) wireless communication since it suffers from multipath components, timing acquisition and synchronisation related issues. However, since technology in wireless communication has greatly improved over the years, known issues with the correlation receiver could be easier solved nowadays than 50 years earlier. For this reason it is decided that the correlation receiver is the most optimal choice for biomedical UWB communication.

2.4 Correlation Receiver Analysis & Design

In Section 2.3 the correlation receiver was chosen as the most suitable receiver architecture for use in biomedical UWB communication. There are however some issues that need to be examined, such as the importance of received signal and generated replica being identical, and properly synchronising both pulses. The importance of these issues are discussed in Subsection 2.4.1. In Subsection 2.4.2 a Correlation Receiver Architecture is introduced and explained. Finally, Subsection 2.4.3 discusses additional details concerning pulse synchronisation that need to be considered.

2.4.1 Analysis of correlation concept

In this section the concept of correlation (i.e. multiplication of a signal with an exact replica, and integration of the result) is analysed. Important factors that need to be observed is the influence of signal modification and deviation on the outcome after integration. To do this, calculation/simulation programs such as Maple or Matlab can be used (Maple 13 was used for the calculations in this section).

The following equation for implementing the Gaussian pulse was used, which is the general function for this specific type of pulse (as defined by Carl Friedrich Gauss):

$$f(t) = a \cdot e^{-\frac{(t-b)^2}{2 \cdot c^2}} \quad (2.20)$$

This formula defines the Gaussian pulse as a symmetric “bell curve” shape that quickly falls off towards plus/minus infinity. The parameter a is the height of the curve’s peak, b is the position of the center of the peak, and c controls the width of the “bell”. In this thesis, the transmitted pulse is

defined to have a width of 6 ns, so $c = 6 \times 10^{-9}$. The pulse amplitude is set at 1 ($a = 1$) and for now the pulse is centered at $t = 0$ ($b = 0$). This particular Gaussian pulse is shown in Figure 2.9a. Figure 2.9b shows this same pulse differentiated eight times to replicate the pulse shape as shown in Figure 2.2a.

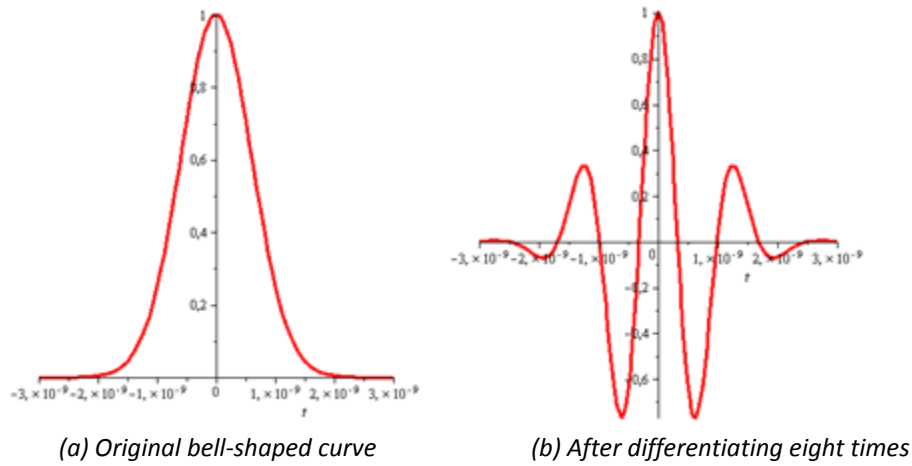


Figure 2.9: Gaussian pulse defined in Maple 13

First the ideal case (with no signal modification or deviation) is being observed. The Gaussian pulse from Figure 2.9b is multiplied with itself. The result is shown in Figure 2.10. Obviously the result is simply a square function, where all negative values become positive. When integrating this signal, maximum energy is derived for further procession.

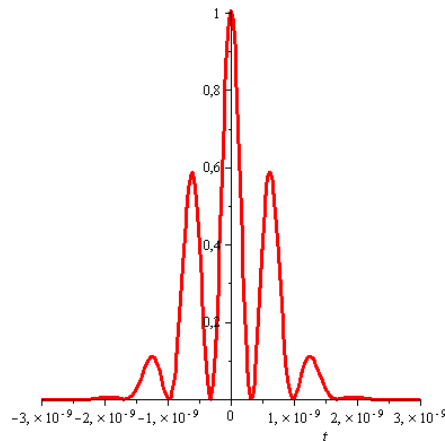
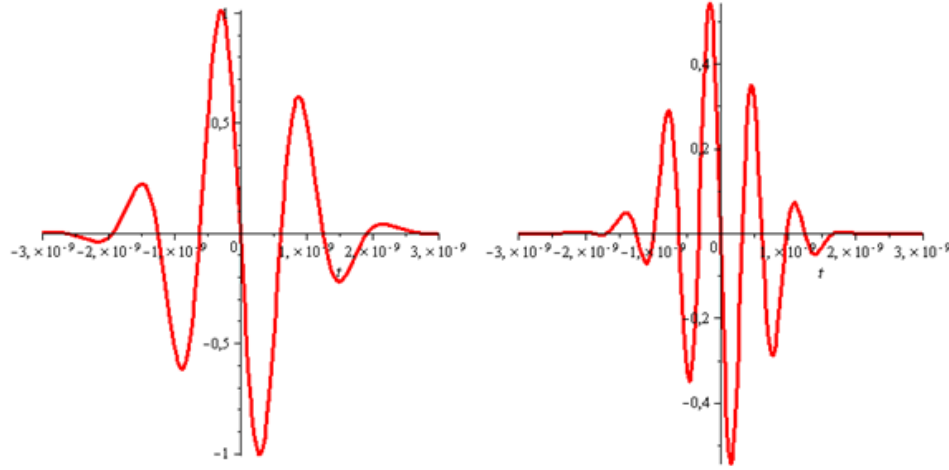


Figure 2.10: Gaussian pulse from Figure 2.9b multiplied with itself

In signal processing there is often the case of the signal being modified (i.e. differentiation or integration) because of, for example, antenna read-out and filtering (occurrences which will be discussed later). This causes the shape of the pulse to be changed dramatically. For example, Figure 2.11a shows the original pulse from Figure 2.9b differentiated once more. Figure 2.11b shows the result when the original pulse is multiplied with the differentiated one.



(a) The original Gaussian pulse differentiated

(b) Differentiated pulse multiplied with the original one

Figure 2.11: The result of differentiation in our Gaussian pulse

Two observations can be made from Figure 2.11b. First of all, the maximum amplitude of the multiplied signal has now lowered to at least half of the original one, which implies that information/energy has been lost. A second observation is that the signal is now odd symmetric around the origin. Integrating an odd symmetric function results in minimal (or 0 in the ideal case) information extraction. From this an important specification is derived when designing the correlation receiver:

All signal modifications, i.e. differentiation/integration, that are caused within the transceiver must be taken into account to ensure maximum information/energy extraction.

Finally, any time shift of the signal also needs to be taken into account. Pulse synchronisation is a common obstacle for wireless receivers, and this is no exception for the correlation receiver concept. It is therefore important to know how much the effect of time shifting will influence correlation. To simulate this effect in Maple, a parameter ' D ' (for shifting over time) is introduced in the calculations:

$$f(t) \cdot f(t + D) \quad (2.21)$$

In Equation (2.21), ' D ' is added in the timing of a Gaussian pulse (from Equation (2.20)), and then multiplied with a pulse ideally centered at $t = 0$. Integrating this multiplication from $t = -3$ ns to $t = 3$ ns, the expression becomes the correlation result as a function of the shifting over time:

$$h(D) = \int_{-3 \times 10^{-9}}^{3 \times 10^{-9}} f(t) \cdot f(t + D) dt \quad (2.22)$$

Equation (2.22) is then plotted as a function of ' D ', which is shown in Figure 2.12a.

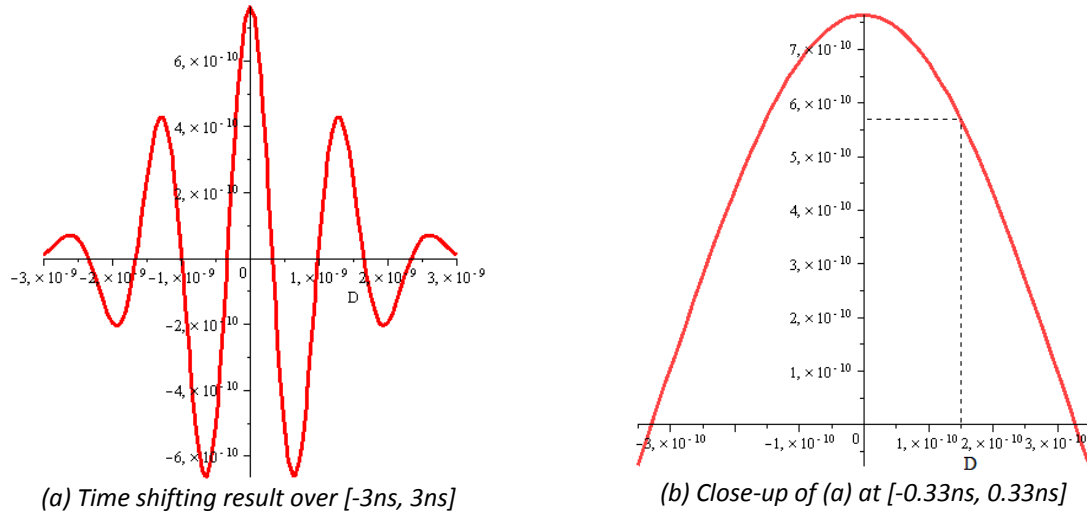


Figure 2.12: Correlation result when time shifting (D) occurs

Figure 2.12a demonstrates the effects of time shifting on to correlation. The more the signal shifts in time before multiplication, the greater the signal loss after correlation. Figure 2.12a also shows that a certain amount of time shifting (greater than $\pm 0.33ns$) causes change in the phase of the output result, i.e. a '1' is received as a '0' and vice versa. This is demonstrated by the negative peaks in the graph. From this observation, it is concluded that only the positive middle peak (around $t = 0$) is valid for signal extraction.

Figure 2.12b is a close-up of the peak centered around 0 in Figure 2.12a. From this graph an important specification is derived when designing the correlation receiver: the maximum allowed deviation over time. A threshold value of at least 75% from the maximum attainable peak is chosen to attain the correct information from the incoming pulse. This 75% is marked by the dotted line in Figure 2.12b, and shows that this corresponds to a deviation of $\pm 0.15 ns$ (or consequently 5% of the total pulse width). This timing specification needs to be taken into account for pulse synchronisation.

2.4.2 Correlation Receiver Architecture

The proposed UWB receiver is depicted in Figure 2.13. This architecture will also be simulated in Matlab in the next section, Section 2.5. The receiver consists of a low noise amplifier, band pass filter, multiplier, a replica-signal generator, a low pass filter and an integrator. Further specifications concerning these blocks will be discussed below.

Note that a synchronisation scheme is not included in the receiver architecture. At the time of writing this thesis, it was decided that there are techniques available for proper synchronisation. Therefore, more time was spend on designing the correlation receiver itself. However, since some information needs to be known concerning pulse synchronisation, this issue is discussed further in Subsection 2.4.3.

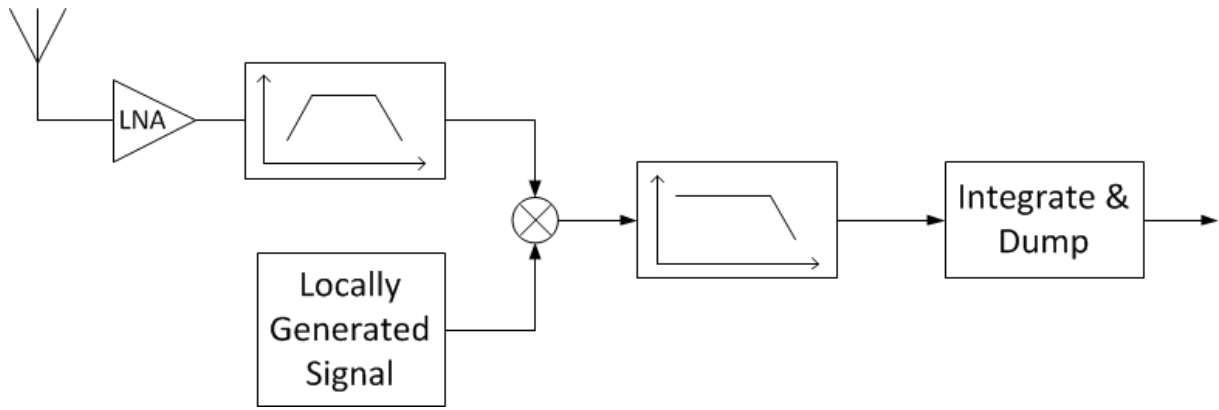


Figure 2.13: Proposed UWB receiver architecture

Band Pass Filter

As discussed in Section 2.1, the frequency band of the signal is between 500 MHz and 1 GHz. The band pass filter has to be designed to these frequencies.

Locally Generated Signal

The block that generates the replica signal should be the same system as the pulse generator at the transmitter side. This pulse generator has already been designed by Mark Stoopman [1] and can therefore simply be implemented at the receiver end. It can also be noted that, should a transmitter and receiver be implemented on a single chip, they can both be driven by one single pulse generator, thus saving area on the integrated circuit.

Multiplier

The multiplier is the most important part in the correlation scheme. It should be noted that this is not to be confused with a (frequency) mixer. A mixer is primarily meant for shifting a signal from one frequency to another, and is therefore not always designed to produce a linear multiplication of its inputs (having one of its inputs act only as a reference). For the correlation receiver, the multiplier is expected to produce a linear and instantaneous product of its two inputs.

Low Pass Filter

The low pass filter is used after the signal is down converted to lower frequencies by the multiplier. It should operate from 0 to 500 MHz. This frequency is calculated by utilising $f_L - f_H$ and $-f_L + f_H$.

Integrate and Dump

Integration of the signal is the final step in the correlation scheme. This checks the energy of the pulse over a specified time. The time step of the integrator is based on the pulse width of the received signal with added compensation for errors in pulse interval. The pulse width of the original pulse is 6ns, therefore a time step of 10ns is chosen. Once the pulse is integrated over time, the end result is checked by a threshold detector. A minimum of 75% of the original pulse amplitude is taken as a reference for checking whether the received pulse is valid information.

2.4.3 Pulse Synchronisation

At the time of writing this thesis, the synchronisation concept that is needed for the correlation receiver was not designed. However, since it is an important aspect for the correlation receiver, as previously discussed in Subsection 2.4.1, this paragraph will briefly discuss some aspects of pulse synchronisation for future work.

Pulse synchronisation is a difficult process, and in fact perfect synchronisation cannot be accomplished. Still, there are ways to reduce the synchronisation error as much as possible, and since a timing specification is known for proper correlation (maximum timing deviation of ± 0.15 ns), this process should be realisable. Several proposals for improving time synchronisation have been researched [23][24][25]. These proposals make use of an acquisition and tracking strategy, or maximum likelihood approach, which consists of successive detection tests on consecutive received signal pulses. The process stops when a likelihood measure of the presence of the expected preamble exceeds a predefined threshold.

Influenced by the designs mentioned in the proposals, they can be translated to this work by two types of pulse synchronisation concepts. Both these options are displayed in Figure 2.14. The main difference between them is one solves pulse synchronisation before correlation takes place (Figure 2.14a) while the other checks the synchronisation accuracy after correlation and subsequently improves it via feedback (Figure 2.14b).

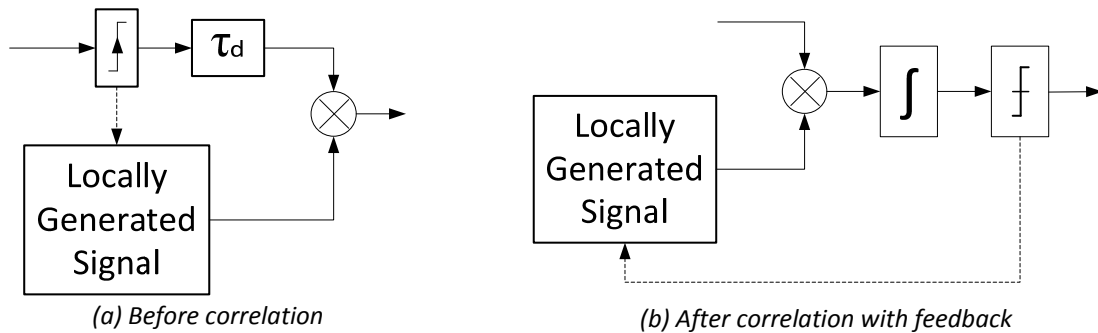


Figure 2.14: Synchronisation concepts for the proposed correlation receiver

As shown in Figure 2.14a, synchronisation is achieved by activating the local replica signal once an incoming pulse is detected by, for instance, a threshold detecting comparator. Since it takes time for the replica signal to be generated, the incoming signal has to be delayed by τ_d , corresponding to the activation time of the replica signal. This type of concept is very difficult to achieve because of a number of reasons. First, the threshold detector may have issues with high noise and interference on the incoming signal, which can make the signal difficult to detect. Second, this concept requires a delay block which, as previously discussed in Subsection 2.3.4, is difficult to implement and may distort the waveform of the signal. Third, the timing delay τ_d may be difficult to estimate.

The concept shown in Figure 2.14b has a feedback loop from the threshold detector to the replica generator. Synchronisation is achieved by shifting the replica pulse in time and subsequently checking the change in amplitude of the correlation result by the threshold detector. When the incoming and replica pulses are synchronised, its maximum amplitude is determined by the threshold

detector. This concept requires a number of incoming pulses to estimate the synchronisation timing. A high amount of incoming pulses should increase the accuracy of pulse synchronisation, however also results in higher power consumption for the transmitter. A nominal number of required pulses has to be estimated.

The difficulty in choosing a useful design from the mentioned proposals is that they prove their functionality by means of BER simulations. These BER simulations are a function of the amount of added noise to the communication channel; time shifting of the received pulse, as was examined in subsection 2.4.1, is not taken into account. Therefore, the BER results from the proposals cannot be compared with the timing specification derived in this work. So in order to fully determine the functionality of the synchronisation schemes for this work, further testing has to be done.

2.5 Matlab Implementation

In order to test the functionality of the Correlation receiver, a simulation model is set up in Matlab/Simulink. This section discusses the complete build-up of this model. Note that only the global structure is discussed here. Figures and variables of the complete model can be found in Appendix B. The subsequent simulation results derived from that model are displayed and further discussed in Section 2.6.

A basic block diagram of the total simulation model is shown in Figure 2.15. The contents of each of these blocks are further discussed below.

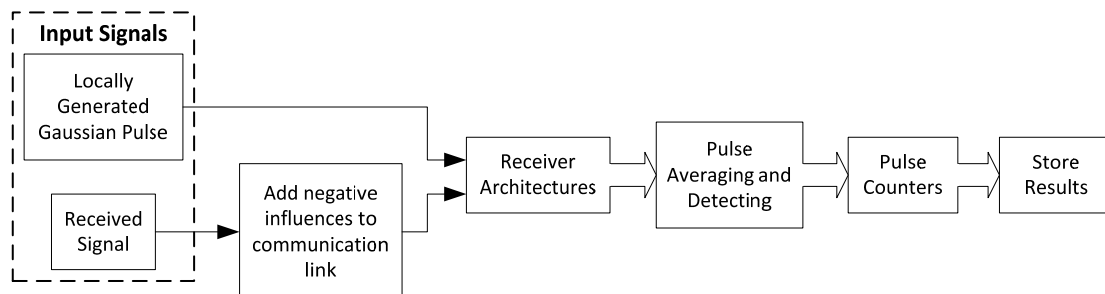


Figure 2.15: Block diagram of Simulation Model

Input Signals

The first important step in simulating the receiver is utilising the correct input signals. There are two distinctive signals used in the simulations. One is the locally generated Gaussian pulse (Figure 2.2a), the other the received signal from the antenna (Figure 2.1). The necessary (digital) information to generate these signals in Matlab was taken from [1].

Note that concerning the signal specifications, the PRF is changed in the simulations. As previously noted in Section 2.1, the specification for the PRF is 1 MHz (=1 μ s spacing between every pulse). While this is possible to implement in the simulation model, it makes for very long simulation time especially when running a high number of pulses. Therefore the time spacing between pulses is kept to lower values. All the other signal specifications are left unchanged.

Negative Influence Blocks

All three negative influences on the communication link that are discussed in the previous sections, i.e. noise, narrowband and multipath interference, are built up and generated separately in Matlab.

AWG Noise

An *AWGN channel* block is used to simulate white noise. The amount of noise on the received signal can easily be adjusted with this block. Its root mean square (RMS) value is also measured and used as a unit of measurement for the simulation results.

Narrowband interference

To simulate narrowband interference, a *Band-Limited White Noise* block is used. The required narrowband frequencies are then taken out of this noise by means of band pass filters. A gain block is used to control the amplitude of the interference. These interference signals are then added to the received signal. For ease of simulation, all narrowband signals have the same gain setting. The narrowband signals that are used in the simulations are 900 MHz, 1.8 GHz, 2.4 GHz and 5 GHz.

The root mean square value of the narrowband interference is used as a unit of measurement for the simulation results (like with the AWGN).

Multipath Interference

As opposed to the noise and narrowband interference systems, a suitable block for adding multipath interference to the proposed signal is not readily available. The *Multipath Rayleigh Fading Channel* block is not compatible (in terms of frame and sample based signals) with the simulation model that is designed here. For this reason a custom Multipath Interference model is built into the simulation model. This model is based on the mathematical equation for multipath propagation, which is shown here:

$$y(t) = h(t) = \sum_{n=0}^{N-1} \rho_n e^{j\varphi_n} \delta(t - \tau_n) \quad (2.23)$$

In Equation (2.23), $\delta(t)$ is the original transmitted signal. Due to the presence of multiple signal paths, more than one pulse will be received. This is expressed in the summation, with N being the number of received impulses (equivalent to the number of electromagnetic paths). The time delay of a received pulse is expressed with τ_n , and $\rho_n e^{j\varphi_n}$ represents the complex amplitude (i.e., magnitude and phase) of the generic received pulse. This equation is implemented as a continuous loop model as shown in Figure 2.16.

The variables from Equation (2.23) are present in the model shown in Figure 2.16, with input signal $\delta(t)$, time delays τ_1 to τ_n and gain blocks ρ_1 to ρ_n ; n is the number of loops implemented in the model. Both τ and ρ are adjustable parameters for the simulations. Note that the summation of all gain blocks $\rho_1 + \rho_2 + \dots + \rho_n$ must be smaller than '1' in order to prevent $y(t)$ from going to infinity.

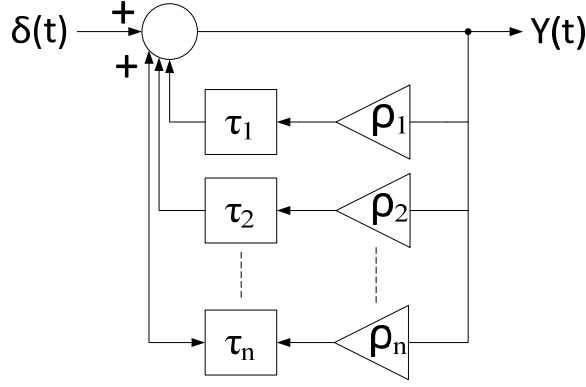


Figure 2.16: Loop model for Multipath Propagation

A decreasing value for τ is equivalent to decreasing travelling time of the multipath signals. It is assumed the transceiver will be used in small to medium-sized (hospital) rooms, where the signal will not travel more than a few meters. Assuming the signal travels at the speed of light, the traveling time will be in the nanoseconds. Note that by trial-and-error it is observed that τ cannot become lower than 50 picoseconds. This has to do with the sampling time to generate the received signal (which is also 50 picoseconds).

The complex amplitude $e^{j\varphi_n}$, phase, is left out. This is done because the error in phase on the signal has already been analysed in Subsection 2.4.1.

Receiver Architectures

The correlation receiver needs to be compared with other receiver architectures. Since a specific type of simulation model is generated in Simulink, it is decided to also build other receiver architectures within the same model for comparison. This choice of operation is deemed more accurate than comparing simulation results of the correlation receiver with other publications, that may not have been tested within a similar simulation model.

From the list of topologies discussed in Section 2.3, the Energy Detection and QDAc receivers are used. The reasons for using these two topologies are, in the case of Energy Detection, successful use in real applications and, in the case of the QDAcR, proven results at a system level. Also, both of these topologies are the easiest to implement compared to the RAKE and subsampling receivers. The RAKE receiver would require a high number of fingers and the subsampling receiver requires digital processing.

In the case of the QDAc Receiver the $\omega_{osc}\tau_d = 2\pi n$ rule for the oscillator and delay blocks is taken into account, as was previously discussed in Subsection 2.3.4. For example, the spacing between every pulse is 50ns (so $\tau_d = 50$ ns). Since the preferred oscillator frequency has to be around 750 MHz (for proper downconversion) the result gives $n = 37$ or 38 , and $f_{osc} = 740$ MHz or 760 MHz.

Also, to test whether only having a correlation receiver is sufficient enough, two extra receivers are included which are a combination of correlation and autocorrelation (transmitted reference) (Figure 2.17a) and correlation and the energy detection scheme (Figure 2.17b).

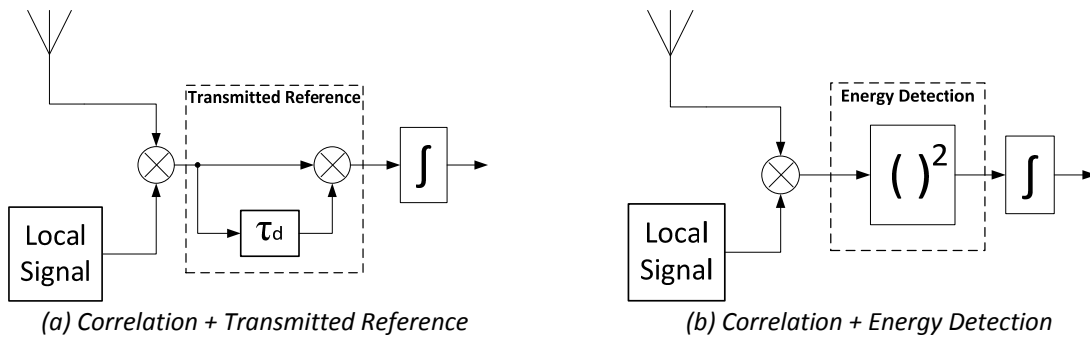


Figure 2.17: Combination of Correlation with (a) Trans. Ref. or (b) Energy Detection

Both architectures shown in Figure 2.17 are implemented in the simulation to test if additional signal processing beside correlation helps improve the overall performance of the receiver.

Filters

Here are some notes on the choice of filters in the design. Standard (ideal) transfer functions are used for these filters. Further research on the influence of non-ideal characteristics in filters on the overall system performance is neglected. This is because most fabricated filters today behave close to the desired ideal transfer function described here.

All filters used in the design are fourth order transfer systems. With these filters the unwanted frequencies are attenuated more steeply than when using lower ordered transfer systems. Also, the filters used in the simulations are critically damped (the damping ratio is '1') since over damped filters cause information loss (in amplitude and frequency) and under damped filters show unstable behaviour. Simulations with filters with a damping ratio of '0.7' were also performed, as common filter designs (such as Butterworth) have this damping ratio. However, since these filters displayed more unstable response in the simulations, a damping ratio of '1' was chosen as more suitable.

Pulse Averaging and Detecting

This block has two functions, of which one is influenced by the other. One functions checks the result of every receiver with a certain threshold value. The other functions generates that threshold value by means of averaging. This is because of the constant change in amplitude of the signal after every function block. It is difficult to maintain fixed amplitudes, especially when it changes constantly for every simulation (with different noise values).

Averaging is done by doing a simulation run, adding up the amplitudes of all the received pulses and dividing them by the total number of pulses of that simulation run. This value is then used as the threshold value for the next simulation run, that tests for valid pulses. Therefore, what the simulation model tests for is consistency of every receiver. Note that, since the threshold changes whenever the interference is set at a different amplitude, this averaging has to be done constantly for every simulation run.

Pulse Counter

This block consists of an up-counter that checks for rising edges: every received pulse gives a rising edge. Note that the counter does not make the distinction between correctly received pulses from the transmitter, and invalid pulses that are caused a receiver mistakenly perceiving high noise as

information. This behaviour will be made more clear in the simulation results, shown in the next section.

Finally, at the end of a simulation run, the total number of received pulses for each receiver is stored.

2.6 Simulation results

Where the previous section (Section 2.5) explains how the simulation model is built up in Matlab/Simulink, this section presents and discusses the simulation results derived from the simulation model. To explain once more, the goals of these simulations is to:

- Test the Correlation receiver on its robustness against negative influences in the communication link (Section 2.2).
- Check if only multiplication between the received signal and a locally generated template is sufficient, or additional signal modification (energy detection or transmitted reference) is necessary for better performance.
- Compare the performance of the Correlation Receiver with the Energy Detector and QDAcR.

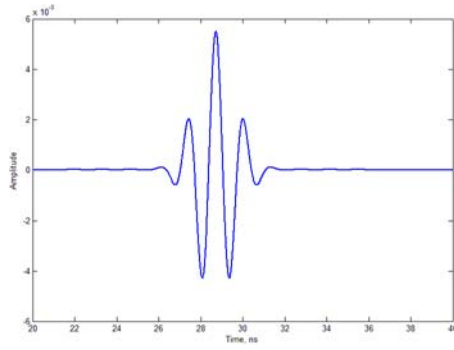
Furthermore, this section also discusses and simulates whether the Gaussian pulse generator and (analog) multiplier can be replaced by a ternary pulse generator (that contains the information of the original pulse) and a switching multiplier.

Input signals

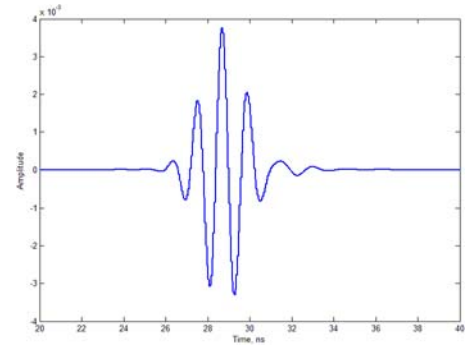
The waveforms of the input signals (*without* interference) are displayed in Figure 2.18; individually (Figure 2.18a and b) as well as in their continuous pulse trains (Figure 2.18c and d). The PRF chosen for these simulations is 20 MHz (= 50 ns per pulse). The fact that both signals are synchronised to each other is noticeable when comparing the timing of the graphs with each other.

Examples of the waveforms of the received signal from the antenna *with* interference are shown in Figure 2.19. The original signal without interference is included in black in the graphs for comparison; the signal with interference is shown in blue. Since the locally generated signal is assumed to be ideal (i.e. no noise), no interference is added to this signal (this also excludes noise that is present in electronic circuits).

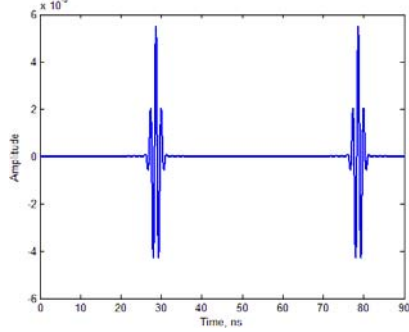
In the examples shown in Figure 2.19, the narrowband amplitude is set to $\text{RMS } 5 \times 10^{-4}$, noise amplitude to $\text{RMS } 3 \times 10^{-4}$ and the multipath model consists of two loops in parallel, one with gain 0.9 with a 2 ns time delay and the other with gain -0.1 and a 4 ns time delay.



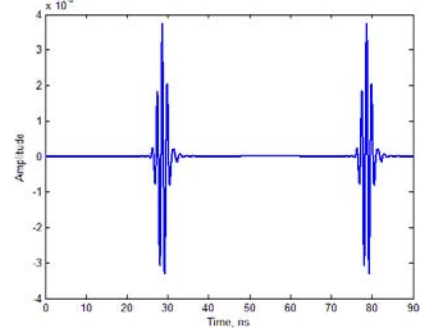
(a) Locally Generated Signal



(b) Received Signal from Antenna

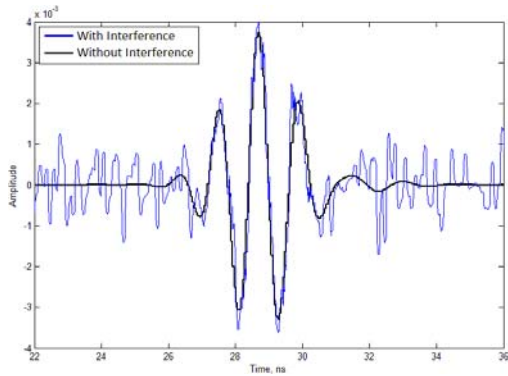


(c) Local Pulse Train, PRF = 20 MHz

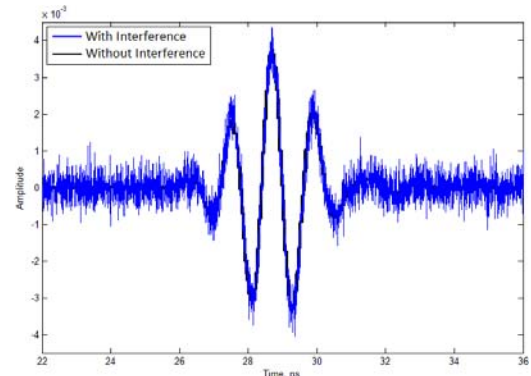


(d) Received Pulse Train, PRF = 20 MHz

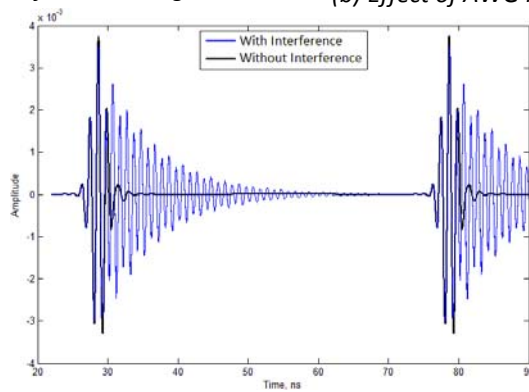
Figure 2.18: Simulation Input Signals



(a) Effect of Narrowband Interference on signal



(b) Effect of AWG Noise Interference on signal



(c) Effect of Multipath Interference on signal

Figure 2.19: Received Signal with added Interference

Simulation results for narrowband and noise

In these simulations a total of 1000 pulses are “transmitted” through the communication link. The number of correctly received pulses at the end indicates the performance of each receiver. Although the Correlation and QDAc receivers can operate as BPSK receivers, these simulations focus on positive polarity of the pulses only. This is because of the addition of the Energy Detector in the simulations (which can only operate in On-Off Keying operation).

The graphs are plotted as a function of the ratio of the root mean square value of the added interference over the root mean square value of the received signal without the interference (i.e. the signal is “clean”). This ratio is shown in Equation (2.24). The root mean square value of the received signal without interference is measured at $RMS\ 5.1 \times 10^{-4}$.

$$ratio = \frac{RMS(Interference)}{RMS(Clean_Signal)} \quad (2.24)$$

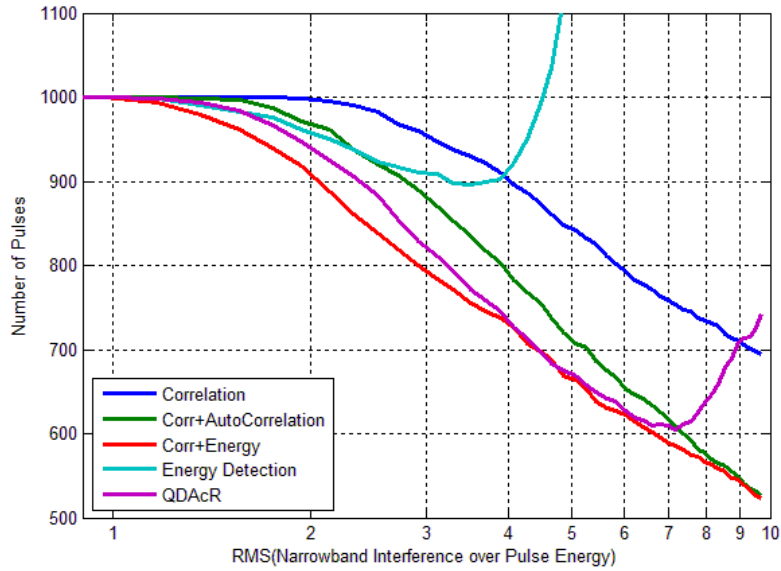


Figure 2.20: Narrowband Interference Simulation

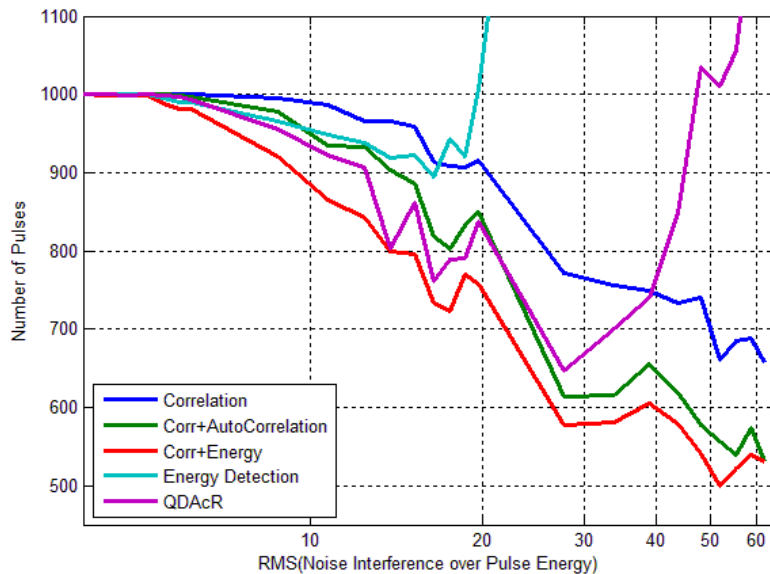


Figure 2.21: Noise Interference Simulation

The most notable observation in these results is the behaviour of both the Energy Detection and QDAcR. At a certain noise/narrowband amplitude these receivers seem to receive more pulses than the amount that is transmitted. This is because of their low(er) robustness against noise/narrowband, which is especially noticeable in the Energy Detection receiver (a problem that was previously described in Subsection 2.3.2). The QDAcR has this same issue, but at higher noise/narrowband levels. Also note that, unlike the Correlation receiver, both the Energy Detection and QDAcR are not as critical in the location of each pulse over time. They receive continuously over time, which increases the risk of receiving invalid pulses.

The results from the noise simulations are more chaotic when compared to the narrowband simulations. This is because of the characteristics of the AWGN Channel Block, which has more random behaviour than the Narrowband model. Several noise simulations were performed to test for consistency. While the shape of the lines are not always exactly identical, the overall results are the same.

Overall these results demonstrate the advantage of the Correlation scheme over the other receivers. The combination of correlation and transmitted reference or energy detection is also tested, but these architectures show reduced results compared to the Correlation receiver. From this the conclusion is made that any additional manipulation on the signal after multiplication does not improve the performance (although the Correlation + Transmitted Reference structure does show better performance than the QDAcR).

Removing the received signal

Finally, in order to prove that the Correlation Receiver does not simply measure the locally generated signal a noise simulation is performed where the antenna signal is removed. The result is therefore the locally generated signal correlated with noise. This information is also useful when the Correlation Receiver is used as an OOK receiver. The simulation results are shown in Figure 2.22.

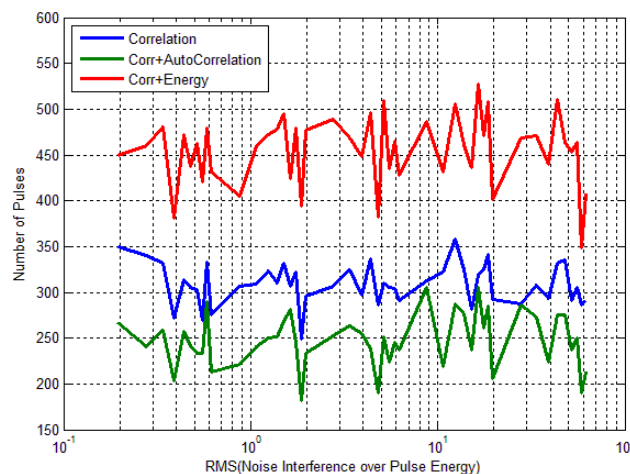


Figure 2.22: No Locally Generated Signal present, Noise Interference

As shown in Figure 2.22, there is a probability that the receivers will perceive noise as valid pulses. Fortunately this probability is lower than the number of invalid pulses that are discarded. It is also noticeable that this probability does not change as a function of the noise level, which indicates the consistency of the Correlation receiver.

Simulation results for multipath propagation

The simulations that were done for multipath interference are discussed separately from the noise/narrowband simulations. These simulations did not show similar figures as displayed previously where the number of received pulses gradually decreases with increasing interference. Instead a rapid increase of received pulses with increasing multipath interference is noticeable, only for some receiver architectures. To explain this behaviour, the waveforms of the signals in the model are examined.

First the effect of multipath interference in the Correlation scheme is examined in Figure 2.23.

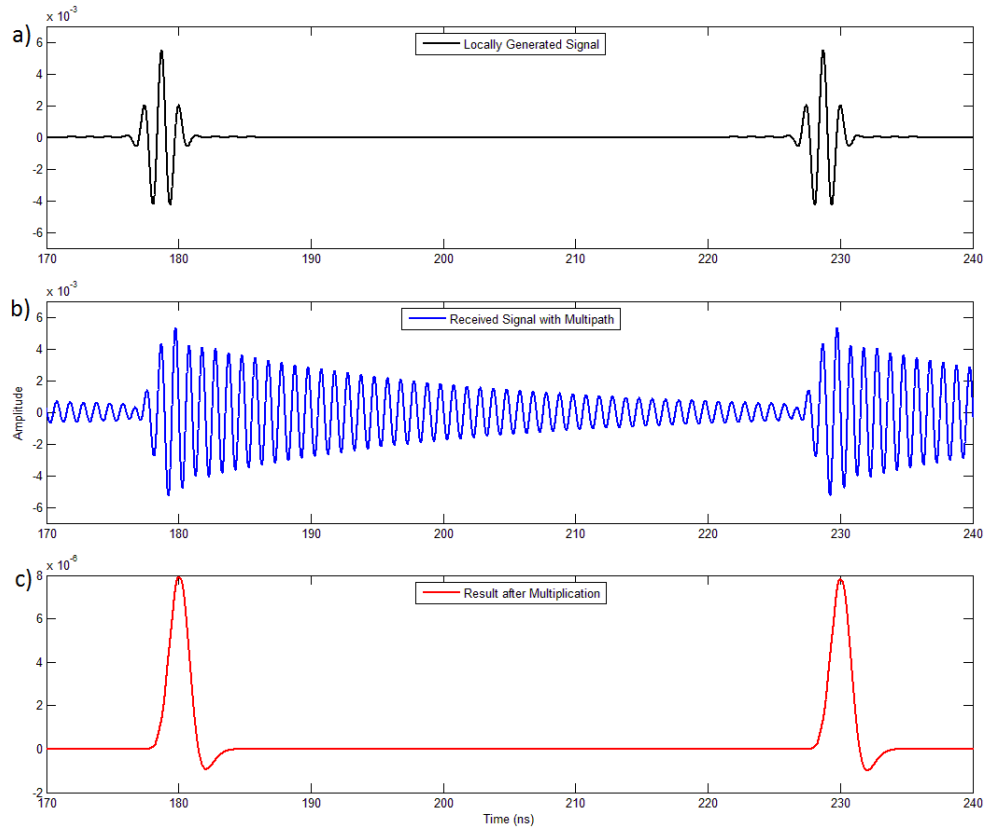


Figure 2.23: Effect of Multipath Interference in Correlation Receiver: (a) locally generated signal, (b) received signal with multipath interference and (c) result after multiplying (a) and (b) and subsequent low pass filter

In Figure 2.23, the top graph displays the local pulse, the middle graph (in blue) the received pulse with multipath interference and the bottom graph (in red) the result after multiplication and low pass filtering. Note that for this example the multipath gain ρ is set at an unrealistic 0.99.

From Figure 2.23 it can be seen that the influence of multipath interference is completely removed by the multiplier, leaving only the required information intact. Because of this the Correlation Receiver has no difficulties with multipath interference. The requirement here is that both local and received pulse have to be synchronised. Since it is assumed that the multipath signals have a lower amplitude than the directly transmitted signal this should be an advantage for the receiver to properly locate the original signal.

The QDAcR also didn't have difficulties with multipath interference. The amplitude of the multipath signals is significantly removed during downconversion and low pass filtering. The transmitted reference scheme further removes the multipath interference, leaving only the original information intact.

The Energy Detector, however, does have difficulties with multipath interference, as demonstrated in Figure 2.24.

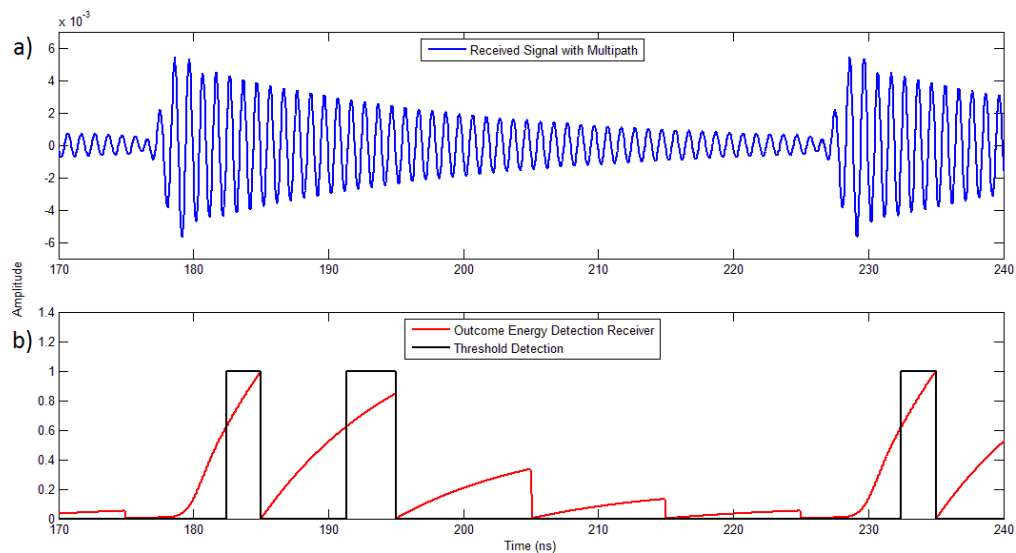


Figure 2.24: Effect of Multipath Interference in Energy Detection: (a) received signal with multipath interference and (b) result of Energy Detection

In Figure 2.24 the received signal (with multipath interference) is displayed in blue, the receiver result after quadrating and integrating the signal is shown in red and the threshold detection of this result is shown in black. The graphs show that once the amplitude of the multipath interference exceeds the threshold of the detector, the receiver perceives this as valid information. In these simulations the Energy Detector would receive over twice as many pulses as originally transmitted, since the receiver does not critically check for the location of each pulse over time. From this the conclusion is made that the Energy Detector is not robust against (high) multipath interference.

Analog multiplier vs. Switching multiplier

The defining characteristic of the Correlation Receiver is its fully analog behaviour: the signal generator gives an *analog* signal which is then multiplied with the received signal via an *analog* multiplier. Most receiver models utilise an oscillator with a switching multiplier circuit (or oscillator mixer) to down convert the received signal to baseband frequencies. This same technique can be used for the Correlation receiver while still using the locally generated signal as a reference.

The concept here is to convert the generated analog signal to a ternary signal (which only consists of the states '-1', '0' and '1'), which can be generated by an oscillator. The locally generated signal would then look as shown in Figure 2.25.

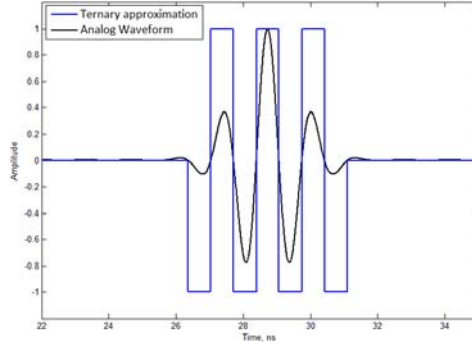


Figure 2.25: Locally Generated Signal, as an analog waveform and ternary signal

As shown in Figure 2.25, the locally generated signal (the analog waveform in black) is sent through a sign-function, which results in the ternary approximation shown in blue. Only the frequency of the original signal is still present. Note that only the large peaks in the 6 ns time-frame are converted, and the smaller peaks (below 10% of the maximum peak amplitude) are neglected. This type of signal can (more) easily be generated by an oscillator and only requires the PRF and frequency of the signal. Also, this implementation can be used with a switching multiplier circuit instead of a fully analog multiplier circuit. The question is whether this implementation would produce better results than the analog approach.

The same interference simulations are performed again, now comparing the analog receiver models with the switching receiver models. Note that any simulations for multipath propagation are left out, since it was shown previously that this interference does not affect the correlation receiver. The results are shown in Figure 2.26.

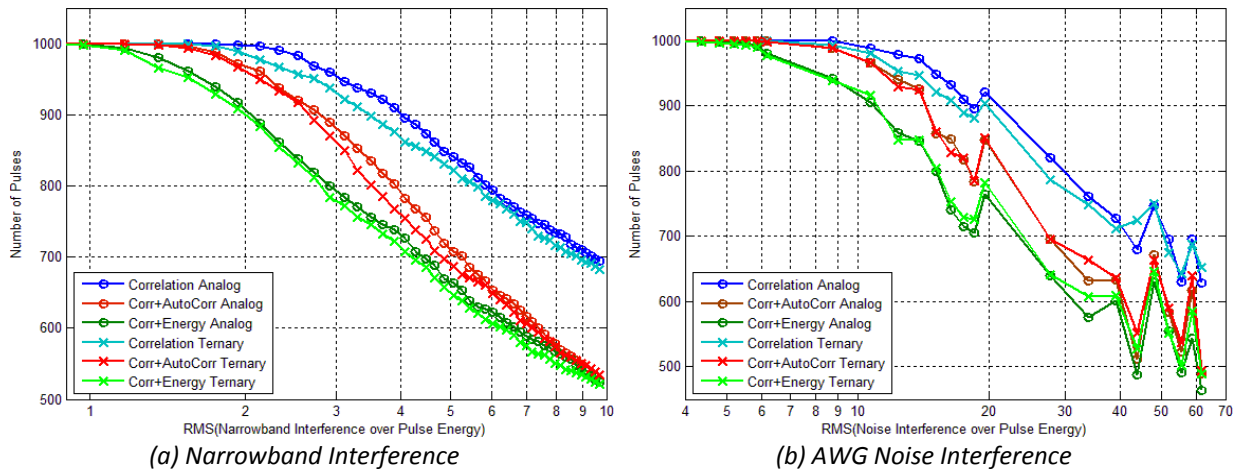


Figure 2.26: Comparing results of analog waveform with analog multiplier vs. ternary waveform and switching multiplier

Both simulation results show that, although both approaches are slightly similar, the analog approach still gives better results. An explanation for this is because of the loss in waveform-information in the ternary signal.

This concludes that using the analog signal generator and an analog multiplier circuit is the best approach for the correlation receiver.

2.7 Summary

In this chapter the system level of a sub-GHz UWB receiver for wireless biomedical communication purposes has been designed, evaluated and simulated.

The communication link that was previously designed by Mark Stoopman for this Master Thesis is researched. A list of specifications necessary for the receiver end was given.

In order to fully test the receiver architecture, negative influences on the communication link were researched. These influences are narrowband interference, noise and multipath propagation. Defining these specific influences proves useful in testing existing and new receiver architectures for their robustness. Specifications are given to define these negative influences. For instance, a list of narrowband signals found over the frequency band is specified, which will later be used for the simulation models.

The Correlation scheme is chosen from a list of UWB receiver topologies. This type of receiver consists of a local template generator that is multiplied with the received signal. Its primary advantage is its simplistic design, which proves useful for implantable devices that require circuits with small area. Furthermore, since the Correlation scheme requires the same pulse/template generator that is used by the transmitter, both receiver and transmitter can share the same generator when implementing them on a single chip.

During the designing process of the Correlation Receiver, signal modification and synchronisation is analysed. Signal modification describes changes in the waveform of the signal because of differentiation/integration during transmission (usually caused by the antenna). These modifications on the received signal have negative results on the outcome of the receiver, so modifications on the local template may be necessary to accommodate for this effect. Therefore, information on these effects is researched and included in Appendix A.

Synchronisation focuses on whether the local and received pulses are correctly synchronised before multiplication. When describing the correlation result as a function of timing deviation, a specification of ± 0.15 ns is derived. This specification describes the maximum amount of timing deviation that is allowed in order to maintain 75% or better performance of the receiver. This specification is useful when designing a synchronisation method.

A simulation model is designed in Matlab/Simulink to test the functionality of the Correlation receiver and compare its performance with other receivers. Other receivers such as the Energy Detector and QDAcR are included in the simulation model for the comparison.

Finally, the results derived from the simulation model show that the Correlation Receiver is robust against noise, narrowband and multipath. It also shows better results than the other receivers that it is compared with in the simulation model. With these conclusions the Correlation Receiver is further developed.

3 Circuit Design

This chapter discusses the circuit design of the UWB correlation receiver that is proposed in the previous chapter. A brief discussion is given on which specific parts of the receiver will be treated in this thesis. From this section the (analog) multiplier is regarded as an important part of the receiver and will be designed for an integrated circuit realization. General design considerations that need to be taken into account, such as choice of Integrated Circuit (IC) technology, operating temperature range, power supply and process variations are then discussed in the section that follows. A suitable multiplier topology is then chosen, while regarding some of the system requirements that were discussed in section 1.3. Once a suitable multiplier topology is chosen, it is further analysed and designed at circuit level to be implemented for the UWB receiver.

3.1 Introduction

The block diagram of the UWB correlation receiver that was proposed in Subsection 2.4.2 is shown here once more for reference in Figure 3.1.

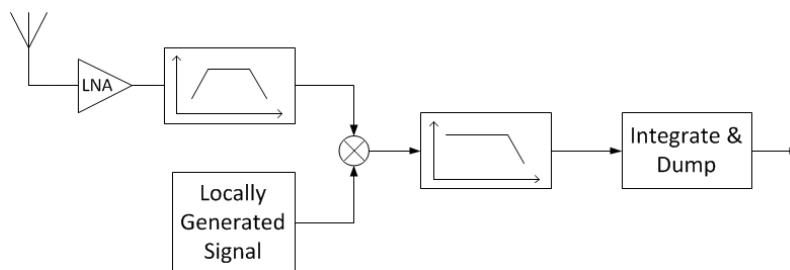


Figure 3.1: Proposed UWB correlation receiver architecture

The total receiver architecture consists of a low noise amplifier (LNA), band pass filter, local signal generator, multiplier, low pass filter and an integrator.

Many examples of LNA's, band-pass and low-pass filters and integrators with small size and low power specifications are available (although they are usually designed for narrowband communications) and can be used for the correlation receiver proposed in this work. Therefore the decision is made that it is not necessary to design these blocks in this thesis.

The two most important and distinct blocks of the correlation receiver are the signal generator (*Locally Generated Signal* in Figure 3.1) and the analog multiplier. The circuit that locally generates the UWB pulse is the pulse generator circuit from the transmitter, which was already designed by Mark Stoopman for his MSc. thesis [1]. Therefore this circuit is already available and doesn't need to be (re-)designed for this work.

The analog multiplier is an important part of the correlation receiver as it converts the received signal to baseband and improves the overall signal-to-noise ratio of every received pulse. Therefore this chapter focuses on designing a suitable multiplier circuit.

3.2 Circuit Design Considerations

This section discusses some of the general considerations that need to be taken into account when designing the multiplier circuit. These considerations are the IC technology of choice, the available power supply, the temperature range that the circuit operates in and process variations that occur during the fabrication process.

Choice of technology

The choice of IC technology for this design is the 0.18 μm High-Voltage CMOS technology from AustriaMicroSystems (AMS). This technology was chosen by the Section Bioelectronics of Delft University as a suitable technology for fully implantable systems. This technology has some the following highlights, as stated on the AMS website [26]:

- Proprietary scalable architecture with operating voltages from 1.8V, 5.0V, 20V to 50V
- Operating frequency up to 4 GHz
- Low leakage option for power sensitive applications
- Low on resistance HV devices for improved performance and small chip sizes
- Fully characterized passives including various capacitors and high res. poly

The main advantage of this technology for the Section Bioelectronics is the ability to integrate all of the subsystems of a fully implantable system on one single chip. Some of these subsystems, for example the neural stimulator and the power management system, require high voltage devices that can handle voltages of 15V or higher. Other subsystems, such as the wireless communication system, require low voltage devices for low power consumption that can operate at high speed. This all has to be done with small sized devices. The 0.18 μm CMOS technology from AMS provides both the low and high voltage devices and is suitable for analog and digital design.

Operating Temperature Range

The UWB receiver in this thesis is meant for a bidirectional biomedical communication link, as previously mentioned in Section 1.3. This requires the receiver to operate as part of an implantable system inside the human body, and also as part of an UWB transceiver outside the human body. When discussing temperature specifications, the implantable system needs to function within a small range, around 37 °C, which is the regulated temperature of the human body. The temperature range for the environment outside the human body is much larger and needs to be taken into account. An operating temperature range from -10°C to 70°C is chosen and considered for the circuit design.

Power Supply

The implantable system is powered by a battery. A power management system is implemented to provide a stable power supply. During the circuit design process, it is assumed this management system is able to deliver the required power.

Process Variations

The reliability of the integrated circuit design is determined by its robustness against parameter variations that can occur during the fabrication process. Therefore, worst case process corner and device mismatch simulations will be performed on the designed circuit in order to test its reliability.

3.3 Multiplier Circuit Topologies

Multipliers are categorized as single-quadrant (where the inputs x and y are unipolar), two-quadrant (where either x or y is bipolar) and four-quadrant (where both x and y are bipolar). The received signal from the antenna and the signal from the local pulse generator are both bipolar, so a four-quadrant multiplier is required for the correlation receiver.

IC multipliers are realizable by using transconductance devices, i.e. MOS transistors in CMOS IC Technology [27]. The MOS transistor is essentially a non-linear device, so instead of only generating the desired multiplication component $x \cdot y$, other undesired components are also generated. These undesired components are high-order polynomial functions, and will be discussed in more detail later in this section. In order to remove these undesired components, the IC multiplier consists of a cancellation configuration. The way of operation of the cancellation method is based on the operation region of the MOS transistor. There are several operation regions that the MOS transistor functions in, each with its own advantages and disadvantages. The first step in designing the IC multiplier is choosing the most suitable operation region for the MOS transistor.

Weak Inversion (Subthreshold) vs. Strong Inversion

The two operation regions, weak and strong inversion, are determined by the Gate-to-Source voltage V_{GS} , and its relation to the threshold voltage V_{th} of the MOS transistor. When $V_{GS} < V_{th}$, the MOS transistor obeys an exponential voltage-to-current relationship, much like the bipolar transistor. This exponential relation is shown in Equation (3.1), where V_T is the thermal voltage, n the subthreshold slope factor and I_{D0} is the drain current when $V_{GS} = V_{th}$.

$$I_D = I_{D0} e^{\frac{V_{GS} - V_{th}}{nV_T}} \quad (3.1)$$

An example of a CMOS multiplier with transistors operating in weak inversion is the Gilbert cell [28]. The original design of the Gilbert cell consists of bipolar transistors, which were later replaced by MOS transistors operating in weak inversion when CMOS technology became popular. The major advantage of transistors operating in weak inversion is that they consume very little power. This makes it a tempting candidate for biomedical applications.

Unfortunately, the weak-inversion transistor is limited to low signal frequencies, because at low current densities the transition frequency f_T of the MOS transistor becomes very small. The IC multiplier for the Correlation Receiver proposed in this work is required to operate at frequencies up to 1 GHz. In order to reach the higher frequencies, the MOS transistor has to be operated in strong inversion, where $V_{GS} > V_{th}$.

Linear/Triode vs. Saturation/Active

With the MOS transistor operating in strong inversion, a decision has to be made whether the transistors should operate in the linear or saturation region. This is determined by the Drain-to-Source voltage V_{DS} for which, in the linear region, it holds $V_{DS} < V_{GS} - V_{th}$, and in the saturation region it holds: $V_{DS} > V_{GS} - V_T$. These operation regions are illustrated in Figure 3.2, taken from [29], where the drain current I_D is plotted as a function of V_{DS} , for different values of V_{GS} . Note that

in Figure 3.2 the linear region is represented as the triode region, and the saturation region as the active region.

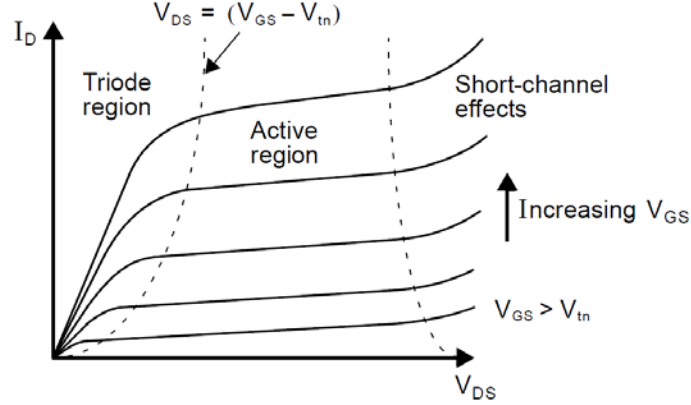


Figure 3.2: Drain Current I_D versus Drain-to-Source Voltage V_{DS} , which shows the operation regions of the MOS transistor. Image taken from [29]

The different voltage to current relations shown in Figure 3.2 can be expressed by Equations (3.2) and (3.3) shown below. For the linear/triode region:

$$I_D = \frac{W\mu_n C_{ox}}{L} \left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (3.2)$$

Drain current I_D has a linear relation with V_{GS} and V_{DS} (as shown by $V_{GS} \cdot V_{DS}$), while also having a quadratic relation with V_{DS} (as shown by V_{DS}^2). Multiplier architectures can be build based on either of these relations, where the other relation is then cancelled out.

The voltage to current relation in the saturation/active region is shown in Equation (3.3).

$$I_D = \frac{W\mu_n C_{ox}}{2L} (V_{GS} - V_{th})^2 (1 + \lambda(V_{DS} - V_{DSsat})) \quad (3.3)$$

Note that in Equation (3.3), the additional factor involving λ is the channel-length modulation parameter, which models the current dependence on the drain voltage. This effect is also visible in Figure 3.2, where the current I_D slightly increases with V_{DS} in the active region. For simplicity during further analysis, the parameter λ is assumed to be zero, meaning that there presumably is no channel length modulation, and I_D is not dependent on V_{DS} . In this case, Equation (3.3) demonstrates a quadratic relation between I_D and V_{GS} .

While both operation regions give the opportunity to design a four-quadrant multiplier [27], one of these has to be chosen as the most suitable for the correlation receiver. The differences between the operation regions is in their performance, mainly speed and transconductance. While the MOS transistor consumes less power in the linear region, its transition frequency f_T is also lower compared to its value in the saturation region. As the operation frequency is an important factor in this thesis work, it is decided to operate in the saturation region.

Multiplier architecture, based on square devices

With the transistor operating in strong inversion saturation region, it now operates as a squaring device. A multiplier architecture that makes use of squaring devices has to be designed. The working principle of a basic multiplier architecture consisting of square devices is shown in Figure 3.3. Unwanted components, such as higher-order (x^2 and y^2) and common-mode (X and Y), are cancelled out because of the differential structure and the addition of adders/subtractors in the architecture.

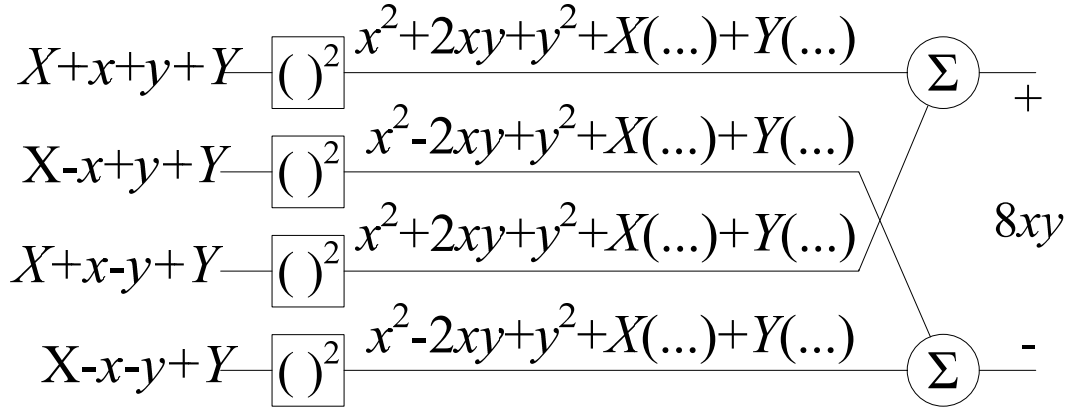


Figure 3.3: Basic four-quadrant multiplier architecture, using square devices. Common mode components X and Y are excluded. Image taken from [27]

The output signal of the structure of Figure 3.3 is written as Equation (3.4), shown below.

$$\begin{aligned} & \left[((X+x) + (Y+y))^2 + ((X-x) + (Y-y))^2 \right] \\ & - \left[((X-x) + (Y+y))^2 + ((X+x) + (Y-y))^2 \right] = 8xy \end{aligned} \quad (3.4)$$

Choice of multiplier circuit

Several published CMOS multipliers are examined and compared in terms of their specifications (supply voltage, bandwidth, power consumption, etc.). These publications are listed in Table 3.1, on the next page. This gives a good overview of the different methods that can be utilised in order to achieve the desired specifications.

Note that all of the multiplier designs in the table are done in 0.18 μm technology, with the exception of [32],[33] which has its multiplier designed in 0.35 μm technology. The working principle of each multiplier is specified on the right side of the table, corresponding to the principles that are discussed in [27], i.e. whether the multiplier is operating in the linear or saturation region. Even though the operation region for the multiplier in this work was already decided upon in the previous subsections, it is still interesting to examine multiplier design that operate in the linear region for comparison.

A number of the publications are specifically focused on wideband CMOS multipliers for UWB transceivers [30], [31], [34], [35]. They are distinguishable from the other publications in Table 3.1 because of their high bandwidth specifications (up to 10 GHz). Although the multiplier circuit for this thesis work requires a bandwidth of up to 1 GHz, it is useful to investigate the techniques utilised in

these publications to achieve high bandwidth. There is also the possibility to decrease the bandwidth of the designs and thereby lower the power consumption as well.

Table 3.1: A list of published CMOS multiplier designs, with corresponding supply voltage, maximum bandwidth, input voltage or current swing and power consumption

Paper	Supply	Bandwidth	Input Swing	Consumption	-Working Principle -Comments
[34]	1.8 V	10 GHz	100 μ A p.p.	16.56 mW	-Linear region -Bipolar, translinear type circuit in CMOS
[31]	1.8 V	9.2 GHz	0.3V p.p	10.8 mW	-Saturation region -Contains bandwidth enhancing Inductors
[30]	1.8 V	10 GHz (unloaded) 7 GHz (loaded)	0.3V p.p	3.6 mW	-Linear region -Contains bandwidth enhancing Inductors
[36]	203 μ A	900 MHz	$V_{in} = 0.3V$ p.p $I_{in} = 40$ μ A p.p	365 μ W	-Saturation region - $I_{in} \times V_{in} = I_{out}$ type multiplier
[32],[33]	1.2 V	110 MHz	0.8V p.p	290 μ W	-Saturation region -0.35 μ m Technology
[35]	0.9 V	10.6 GHz	0.6V p.p	261 μ W	-Linear Region -Based on “programmable transconductor” scheme

[30] and [31] achieve high bandwidths because of their use of shunt connected inductors at the output. The addition of inductors at the output causes a high frequency zero in the transfer function of the multiplier. The use of inductors in the multiplier design negatively influences the fabrication of the IC, as on-chip inductors require a large area. For this reason, the designs in [30] and [31] are discarded.

The CMOS multiplier design in [34] is based on a bipolar translinear circuit, i.e. the Gilbert Cell. The bipolar transistor is emulated by a bipolar cell, which consists of MOS transistors and a diode. The result is a linear multiplier with high gain and high bandwidth. The drawbacks of this design are its large number of CMOS components (every bipolar transistor is replaced by 3 MOS transistors and a diode) and its high power consumption.

The design in [35] stands out as having the lowest power consumption, requiring no bandwidth boosting inductors and still acquiring high bandwidth. The design is based on the programmable linear transconductor [27], where one transistor acts as a source follower and another transistor modulates the transconductance of the source follower. This structure is then implemented in a differential architecture to enable multiplication. The problem with the design from [35] is that its structure is rearranged so that the source followers now have a very low transconductance. Having source followers with a low transconductance translates to a very low output gain (which explains the result of having high bandwidth). The publication solves the low transconductance issue by increasing the W/L ratio of the source followers, which results in very large transistors. The linearity of the multiplier is also very poor.

Publication [36] is unique from the other publications in Table 3.1 in that it multiplies a voltage signal with a current signal, whereas the inputs of the other multiplier designs are identical. This multiplier design is meant for sensing current-mode signals, as it has very low-impedance input nodes. Its structure consists of a Flipped Voltage Follower Current Sink (FVFC), which creates a relation between the input voltage and current. Publication [36] stands out in consuming low power, having a relatively large bandwidth of 900 MHz (almost reaching the required 1 GHz), requiring a low supply current and having good linearity. Unfortunately, the $I \times V$ characteristic does give issues in the circuit design process of the correlation receiver, in that the other components have to be adapted to the multiplier. The local signal generator from Mark Stoopman's work [1] has a voltage output, therefore requiring the band pass filter (see Figure 3.1) to have a current output. There may be the possibility in adding a voltage-to-current or current-to-voltage converter in the design, but this would add unwanted complexity to the receiver design, and may influence the performance of the multiplier negatively. The $I \times V$ multiplier also consists of a large number of MOS transistors (compared to the other publications).

Finally, the design presented in [32] and [33] stands out by representing a low power multiplier with high linearity¹. It utilises a simplistic design and requires a low number of components (12 CMOS transistors, and two resistors). Its drawback is that this publication has a bandwidth of only 110 MHz. It is however noticeable that this publication was done in 0.35 μm technology, and all transistor sizes are kept as small as possible (also having a low W/L ratio). By implementing the design in a smaller technology (0.18 μm) and increasing the W/L ratio of the transistors the bandwidth of the design can be increased, while still maintaining low power consumption. For this reason it is decided to implement the multiplier circuit design from [32] and [33].

3.4 Low Power Multiplier Circuit Design

Now that a suitable, low power, multiplier circuit topology is chosen (Section 3.3), this section focusses on the analysis, design and implementation of that multiplier circuit. In Subsection 3.4.1 the circuit from [32] and [33] is discussed and analysed in order to understand the workings of the circuit. The objectives here are to locate the main influences (in terms of component parameters) on bandwidth and supply voltage. Next, in subsection 3.4.2 the multiplier circuit is designed and implemented according to the requirements derived in this thesis (Sections 1.3 and 3.2).

3.4.1 Circuit Analysis

The CMOS Four-Quadrant Analog multiplier from [32] is shown in Figure 3.4, on the next page.

In Figure 3.4, the two differential input voltages are defined as $V_{id1} = V_1 - V_2$ and $V_{id2} = V_3 - V_4$. The differential output voltage is defined as $V_O = V_{O1} - V_{O2}$. The total multiplier circuit from Figure 3.4 consists of two sub-circuits: a combiner (Figure 3.5a) and a subtractor (Figure 3.5b). Each of these

¹ Note that [32] and [33], both contributed by the same author, present essentially the same multiplier circuit topology with the exception of the circuit in Publication [33] containing two current sources for improving the linear range. Despite this difference, the circuits from both publications are discussed as being identical in this thesis.

sub-circuits are first discussed individually, then combined in order to find the relation from inputs to output.

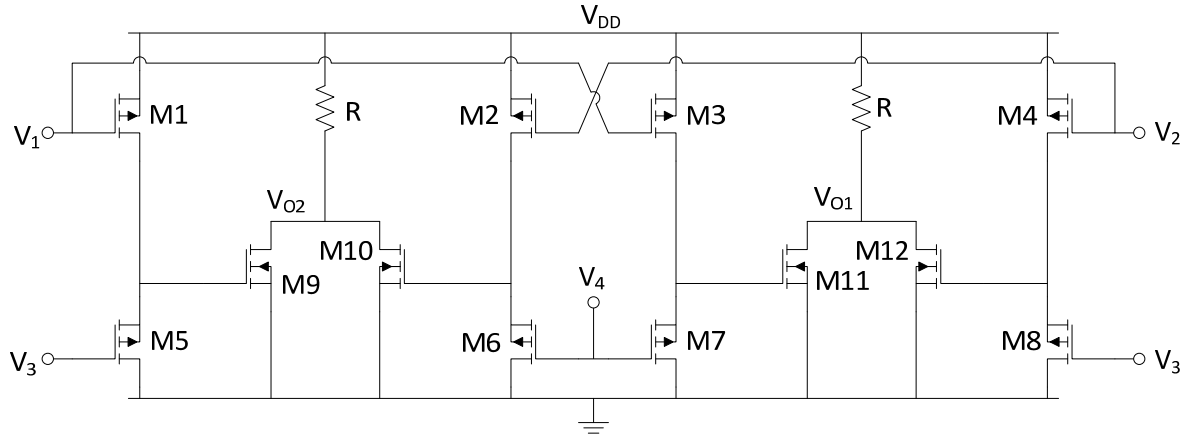


Figure 3.4: Low voltage, low power, high linearity CMOS multiplier [32]

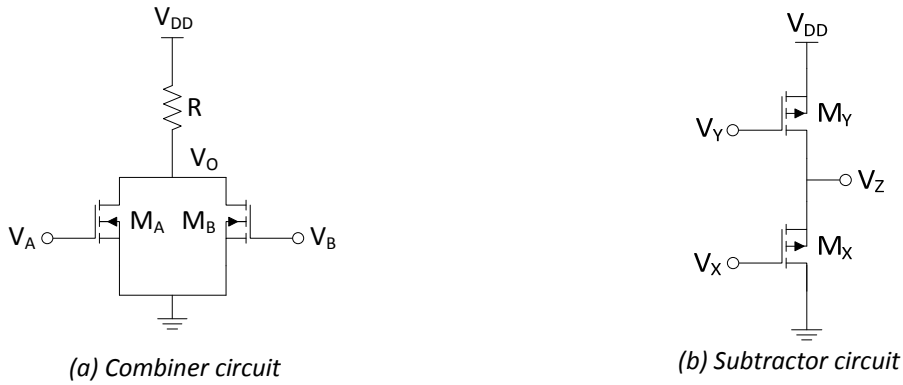


Figure 3.5: Sub-circuits of the low power CMOS multiplier shown in Figure 3.4

Combiner Circuit

In Figure 3.5a, the input voltages V_A and V_B control the drain currents of their respective NMOS transistors. These drain currents are summed, or combined, in load resistor R . The summation is read out as voltage V_O . The relation between V_O and the drain currents of transistors M_A and M_B is expressed as:

$$V_O = V_{DD} - V_R = V_{DD} - R \cdot I_R = V_{DD} - R \cdot (I_{DS,A} + I_{DS,B}) \quad (3.5)$$

The expression $(I_{DS,A} + I_{DS,B})$ is taken separately, and written as a function of the input voltages V_A and V_B .

$$(I_{DS,A} + I_{DS,B}) = k_{n,A}(V_A - V_{tn,A})^2 + k_{n,B}(V_B - V_{tn,B})^2 \quad (3.6)$$

Equation (3.6) is the summation of two drain currents when both transistors are in the strong-inversion saturation region, as taken from Equation (3.3). Note that from Equation (3.3) the channel length modulation (parameter λ) is neglected, and the term $\frac{1}{2} \frac{W}{L} \mu_n C_{ox}$ (the transistor's width W , length L , carrier mobility μ_n and oxide capacitance C_{ox}) is expressed as k_n in Equation (3.6).

Equations (3.5) and (3.6) are combined to show the relation between the output V_O and the inputs V_A and V_B . It is for simplicity assumed that M_A and M_B are identical devices, so $k_{n,A} = k_{n,B} = k_n$ and $V_{tn,A} = V_{tn,B} = V_{tn}$ and thus:

$$V_O = V_{DD} - Rk_n[(V_A - V_{tn})^2 + (V_B - V_{tn})^2] \quad (3.7)$$

Subtractor Circuit

The subtractor circuit in Figure 3.5b consists of two PMOS transistors, which are controlled by the input voltages V_X and V_Y respectively. The relation between output voltage V_Z and the inputs will be briefly analysed here. From Figure 3.5b, it can be seen that V_Z is dependent of the voltages between the drain-to-gate (V_X) and gate-to-source of PMOS transistor M_X .

$$V_Z = V_X + V_{SG,X} \quad (3.8)$$

In Equation (3.8), $V_{SG,X}$ can be rewritten by using the drain current equation when the transistor is in strong-inversion saturation. This results in:

$$V_Z = V_X + V_{tp,X} + \sqrt{\frac{I_{DX}}{k_{p,X}}} \quad (3.9)$$

Note that in Equation (3.9) k_p is expressed as $k_p = \frac{1}{2} \frac{W}{L} \mu_p C_{ox}$. The PMOS transistors are connected in series, therefore $I_{DX} = I_{DY}$.

$$\begin{aligned} V_Z &= V_X + V_{tp,X} + \sqrt{\frac{k_{p,Y}(V_{DD} - V_Y - V_{tp,Y})^2}{k_{p,X}}} \\ &= V_X + V_{tp,X} + \sqrt{\frac{k_{p,Y}}{k_{p,X}}} (V_{DD} - V_Y - V_{tp,Y}) \end{aligned} \quad (3.10)$$

For simplicity, it is assumed that M_X and M_Y are identical devices (the same approach as with the combiner circuit), so $k_{p,Y} = k_{p,X}$ and $V_{tp,X} = V_{tp,Y}$ and thus:

$$V_Z = V_X - V_Y + V_{DD} \quad (3.11)$$

Equation (3.11) shows that V_Z is determined by a subtracting relation between inputs V_X and V_Y .

Complete Multiplier Equation

Now that the inputs-to-output relations of the two subcircuits of Figure 3.5 are known, they are combined according to the multiplier architecture of Figure 3.4. This will generate the total multiplier equation. First, the differential voltage outputs V_{O1} and V_{O2} are expressed separately. Equations (3.7) and (3.11) are used here. Note that it is assumed that the resistors from both combiner circuits in Figure 3.4 are identical.

$$V_{O1} = V_{DD} - Rk_n[(V_4 - V_1 + V_{DD} - V_{tn})^2 + (V_3 - V_2 + V_{DD} - V_{tn})^2] \quad (3.12)$$

$$V_{O2} = V_{DD} - Rk_n[(V_3 - V_1 + V_{DD} - V_{tn})^2 + (V_4 - V_2 + V_{DD} - V_{tn})^2] \quad (3.13)$$

By rewriting Equations (3.12) and (3.13), and using the definition of the differential output $V_O = V_{O1} - V_{O2}$ (that was stated previously), the V_{DD} and V_{tn} terms are removed. The result is Equation (3.14), as shown below, where the definitions of the differential inputs $V_{id1} = V_1 - V_2$ and $V_{id2} = V_3 - V_4$ are also utilised.

$$V_O = Rk_n(2V_1V_4 + 2V_2V_3 - 2V_1V_3 - 2V_2V_4) = \boxed{-2Rk_nV_{id1}V_{id2}} \quad (3.14)$$

From Equation (3.14) it can be concluded that V_O is not only dependent on V_{id1} and V_{id2} , but also on the resistor R and the parameter k_n of the NMOS transistors M_{9-12} . The “ Rk_n ” component in Equation (3.14) represents the output voltage gain of the multiplier, and shows that its amount is determined only in the second/final stage (the combiner circuit) and not in the first stage (the subtractor circuit).

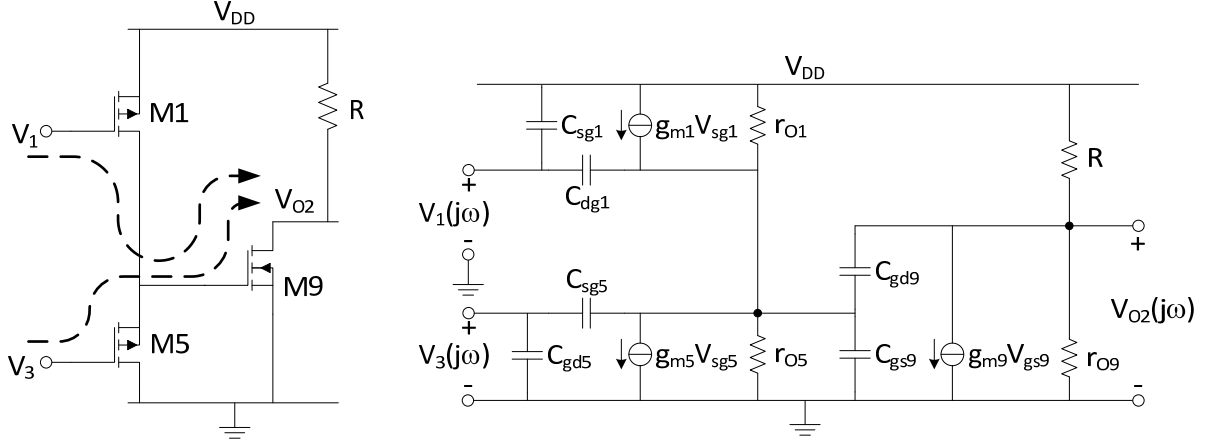
AC analysis

As discussed previously the required bandwidth of the multiplier (1 GHz) is an important specification. The multiplier architecture published in [32] and [33] is designed with a bandwidth of only 110 MHz, as the designer was focusing mainly on low power operation and high linearity. Design steps have to be taken to achieve a bandwidth of 1 GHz while still consuming little power. Linearity is not an important requirement; during the system design process of the correlation receiver in Sections 2.4 to 2.6, it was concluded that after multiplication only the polarity of the output signal is of real importance, not its waveform.

An AC analysis of the multiplier architecture is performed in order to understand which parameters are of influence to the bandwidth. Having two differential inputs (V_{id1} and V_{id2}), both leading to one differential output (V_O), the AC analysis is performed as such that each input is examined separately (where one is controlled with an AC signal and the other with a DC signal, and vice versa). This is because both signal paths are not identical, so their respective frequency responses may also not be identical. It is interesting to note that most of the publications that were discussed on page 40, with the exception of [31] and [35], have published the frequency response of their multiplier via only one of the two inputs. This thesis will present the frequency response of both inputs, considering the importance of the frequency requirement of the multiplier.

Knowing that the multiplier architecture is symmetrical, and transistors M_{1-4} , M_{5-8} , M_{9-12} and both resistors R are identical, it is sufficient enough to do an AC analysis on only a part of the structure. This structure is shown in Figure 3.6a, on the next page.

As shown in Figure 3.6a, the two AC paths that will be examined are from V_1 to V_{O2} (with V_3 set at a constant value) and from V_3 to V_{O2} (with V_1 set at a constant value). It is assumed that the results for these paths are identical for all the other input-to-output paths in the architecture. Small-signal models of the NMOS and PMOS transistors are used, as shown in Figure 3.6b.



(a) Two paths for AC analysis, from V_1 to V_{O2} and from V_3 to V_{O2}

(b) Small signal model of structure shown in Figure 3.6a

Figure 3.6: Structure used for AC analysis of the total multiplier architecture

Fully calculating the AC transfer functions $V_{O2}(j\omega)/V_1(j\omega)$ and $V_{O2}(j\omega)/V_3(j\omega)$ proves to be difficult, given the complexity of the (two-stage) small-signal structure of Figure 3.6b. By examining the structure it is clear that it contains several feedback networks caused by the capacitances C_{gd9} , C_{sg5} and C_{dg1} . This causes the operation of all three transistors to be dependent on each other. Instead of calculating the whole network in Figure 3.6b, it is decided to make certain simplifications and/or approximations and then verify these with simulations performed in Cadence. This will help in finding the information necessary in order to achieve the bandwidth specification.

Starting with the output stage, M_9 , the output resistance at V_{O2} consists of resistors R and r_{O9} connected in parallel. It is assumed that $R \ll r_{O9}$, therefore the output resistance of M_9 is roughly equal to R . C_{gd9} can be transformed to the input and output of transistor M_9 using the Miller approximation [37], which helps to simplify the circuit. The newly formed capacitors C_{in9} and C_{out9} are now written as:

$$C_{in9} = C_{gd9}(1 + g_{m9}R) \quad (3.15)$$

$$C_{out9} = C_{gd9} \left(1 + \frac{1}{g_{m9}R} \right) \approx C_{gd9} \quad (3.16)$$

In Equations (3.15) and (3.16) the term $-g_{m9}R$ is the voltage gain from input to output (of transistor M_9). Due to the Miller approximation, two poles are specified in the left half plane: for the output its $p_{C_{out9}} = -C_{gd9}R$, and for the input its $p_{C_{in9}} = -C_{in9}/g_{m5}$ (not taking into account the parasitic elements of transistors M_1 and M_5). Note that C_{gd9} also introduces a zero in the right half plane: $z_{C_{gd9}} = +g_{m9}/C_{gd9}$. However, this zero is ignored, as it is assumed to be outside of the operating bandwidth of the multiplier.

Second, the AC transfer from input V_3 to the output V_{O2} is analysed. Input V_1 is set to DC, thereby removing the influences of the capacitor C_{sg1} and subsequently the current source $g_{m1}V_{sg1}$ (as $V_{sg1} = 0$). Looking into the drain terminal of PMOS transistor M_1 , its impedance is roughly based on r_{O1} and C_{dg1} connected in parallel. The influence of the resistive load r_{O1} is neglected because of its parallel connection with the transconductance component g_{m5} ($r_{O1} // \frac{1}{g_{m5}} \approx \frac{1}{g_{m5}}$).

PMOS transistor M_5 is connected as a source follower, which implies a direct voltage transfer from input terminal V_3 to the input of transistor M_9 . Assuming that capacitors C_{gd5} and C_{sg5} have little influence on the direct voltage transfer, they are therefore neglected. The current source $g_{m5}V_{sg5}$ is still present in the network. Load resistor r_{O5} is also removed because, like r_{O1} , it has little influence when it is connected in parallel with transconductance component g_{m5} . With these approximations, it is assumed there is a pole present in the left half plane written as:

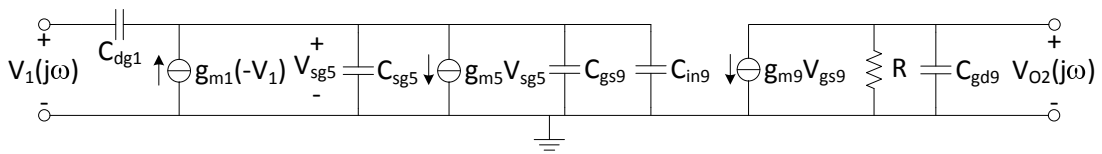
$$p_{V_3} = -\frac{1}{g_{m5}} \cdot (C_{dg1} // C_{in9} // C_{gs9}) \quad (3.17)$$

Note that in Equation (3.17) the parallel connections of the capacitors are defined by the symbol “//”.

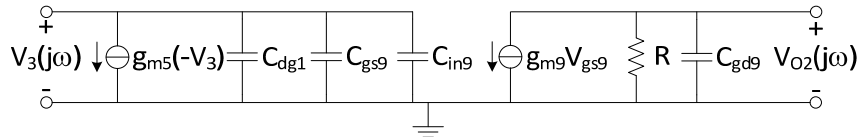
Third and finally, the AC transfer from input V_1 to the output V_{O2} is analysed. Transistor M_1 acts as a current source. Ideally, the transconductance component g_{m1} is not frequency dependent so this component is removed. Capacitor C_{sg1} is also removed, considering it is driven by an ideal voltage source. Input V_3 is set to DC, thereby removing the influence of the capacitor C_{dg5} . Note that the current source $g_{m5}V_{sg5}$ is still influential in the network and the parasitic capacitor C_{sg5} is also present. Resistors r_{O1} and r_{O5} are removed because they are connected in parallel with $1/g_{m5}$. Finally, with these approximations, a pole is assumed to be present in the left half plane and is written as:

$$p_{V_1} = -\frac{1}{g_{m5}} \cdot (2C_{dg1} // C_{in9} // C_{gs9} // C_{sg5}) \quad (3.18)$$

To help the reader in understanding the simplified AC networks that were described, their respective illustrations are shown below in Figure 3.7.



(a) AC network for transfer V_1 to V_{O2}



(b) AC network for transfer V_3 to V_{O2}

Figure 3.7: Simplified networks of Figure 3.6, for both AC signal paths

By examining the extracted poles from the network in Figure 3.6, it can be concluded that the g_m of each transistor and the output impedance R are defining factors in influencing the location of the poles (and thereby influencing the bandwidth of the network). Adjusting R is easier than adjusting g_m , but this also directly affects the area of the circuit. It is therefore preferred to influence the g_m

of the transistors. One way of increasing the g_m is by increasing the width, W , of the transistor, or the overall W/L ratio. Unfortunately, the parasitic capacitances (C_{gs} and C_{gd}) will then also increase. This subsequent influence on the frequency response can be better understood by using for example the principles discussed in [38], on page 55. The f_T of a MOS transistor is expressed in [38] by the following equation:

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gb} + C_{gd}} \quad (3.19)$$

The parameters g_m and C_{gs} are expressed in [38] as:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (3.20)$$

$$C_{gs} = \frac{2}{3} W L C_{ox} \quad (3.21)$$

Note that these equations hold for when the MOS transistor operates in strong inversion saturation. Also, in [38], C_{gs} is assumed to be much greater than $(C_{gb} + C_{gd})$, as the intrinsic values for C_{gb} and C_{gd} approach zero due to channel pinch-off when in strong inversion saturation². Rewriting Equation (3.19) by using (3.3), (3.20) and (3.21) gives:

$$f_T = 1.5 \frac{\mu_n}{2\pi L^2} (V_{GS} - V_t) \quad (3.22)$$

Equation (3.22) shows that changing W has no effect on f_T . The two parameters that do have a significant influence on f_T are L and V_{GS} . Knowing that L is preferably kept at the minimum value of 180 nm, only V_{GS} remains as the main parameter to influence f_T .

Taking the conclusion derived from Equation (3.22) and implementing it in the network shown in Figure 3.6a implies that its performance is dependent on the DC voltages at the input terminals V_1 and V_3 . This will directly modify the g_m of transistors M_1 and M_5 , without influencing their parasitic capacitances. The difficulty here is that the DC operating voltage at the input of transistor M_9 can only be modified via the input terminals V_1 and V_3 . Knowing that the overall performance of the multiplier is most dominant in its output stage, nominal values for the biasing voltages at the input have to be determined. This is done by doing an AC analysis on the network in Figure 3.6a in Cadence. Two AC simulations are performed, one via V_1 and the other via V_3 . In both simulations the DC voltages on the input terminals are modified separately. A bode plot of the output node V_{O2} is generated for each simulation.

Starting with an AC signal (amplitude = 200 mV) on input terminal V_1 , with V_3 fixed to a DC value (0 V in this case), the DC voltage on V_1 is swept from 300 mV to 700 mV. Note that the biasing voltage on

² While in [38] the influences of C_{gb} and C_{gd} are neglected when the transistor operates in strong inversion saturation, it is interesting to note that these parasitic capacitances, like C_{gs} , also increase with increasing W and L . In most small signal transistor models, C_{gb} is influential in the cut-off region and equals $W L C_{ox}$, while C_{gd} is influential in the linear region and equals $\frac{1}{2} W L C_{ox}$.

transistor M_1 is defined as $V_{sg} = V_{DD} - V_{1,DC}$ (with $V_{DD} = 1.2$ V), so an increase of $V_{1,DC}$ will decrease the region of operation of the PMOS transistor. The result of this simulation is shown in Figure 3.8.

The first observation in Figure 3.8 is a decline in gain beyond 1 GHz. Fortunately the f_{-3dB} crossing is beyond this frequency so the network still operates within the specifications. Maximum gain is achieved at $V_{1,DC} = 400$ mV, whereas at DC voltages of 300 and 350 mV the gain declines at slightly higher frequencies (as shown in the phase diagram). As expected, the gain and bandwidth of the network rapidly decrease as $V_{1,DC}$ increases beyond 500 mV. Furthermore, a zero is noticeable in the bode plot beyond 100 GHz, which is assumed to be $z_{C_{gd9}}$, as was previously discussed. Fortunately this zero is far beyond the operating bandwidth of the multiplier and should therefore not cause any problems.

Figure 3.9, on the next page, shows the bode plot for modifying the DC voltage on input terminal V_3 ($V_{1,DC} = 500$ mV in this example). Note that the bandwidth of the network is not affected by modifying $V_{3,DC}$. This can be explained by examining pole p_{V_1} , and assuming this is the dominant pole that causes the roll-off. The pole p_{V_1} contains no components that are directly affected by $V_{3,DC}$ (g_{m5} does not change according to $V_{3,DC}$). Maximum gain is achieved at $V_{3,DC} = 200$ mV.

Next, the same two simulations are performed but now with an AC signal (amplitude = 250 mV) on input terminal V_3 . The results are shown in Figure 3.10 and Figure 3.11, on Pages 49 and 50 respectively. Comparing the AC_{V_1} and AC_{V_3} simulations with each other indicates slightly similar results in the magnitude diagrams. A noticeable difference is the difference in phase (180 deg) in the simulations. This can be explained by examining the two transfer paths: the path from V_1 to V_{O2} has two inverting stages (caused by M_1 and M_9), the path from V_3 to V_{O2} has only one inverting stage (caused by M_9). Maximum gain is achieved at $V_{1,DC} = 350$ mV and $V_{3,DC} = 200$ mV.

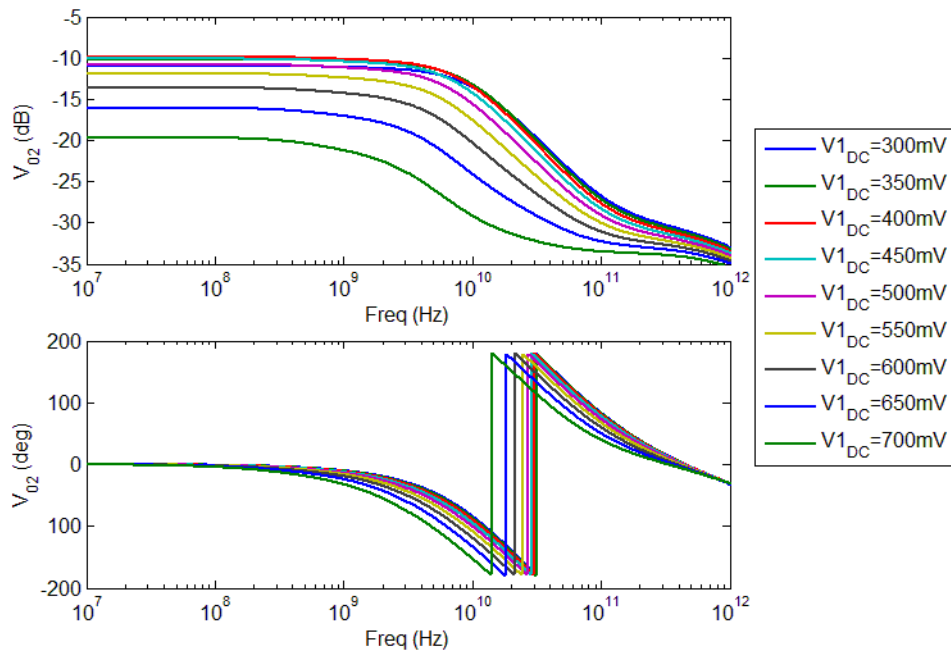


Figure 3.8: Bode plots following from an AC simulation on the circuit shown in Figure 3.6a, with an AC signal via input terminal V_1 . The DC voltage on input V_1 is swept from 300 mV to 700 mV, with steps of 50 mV. $V_{1,AC} = 250$ mV

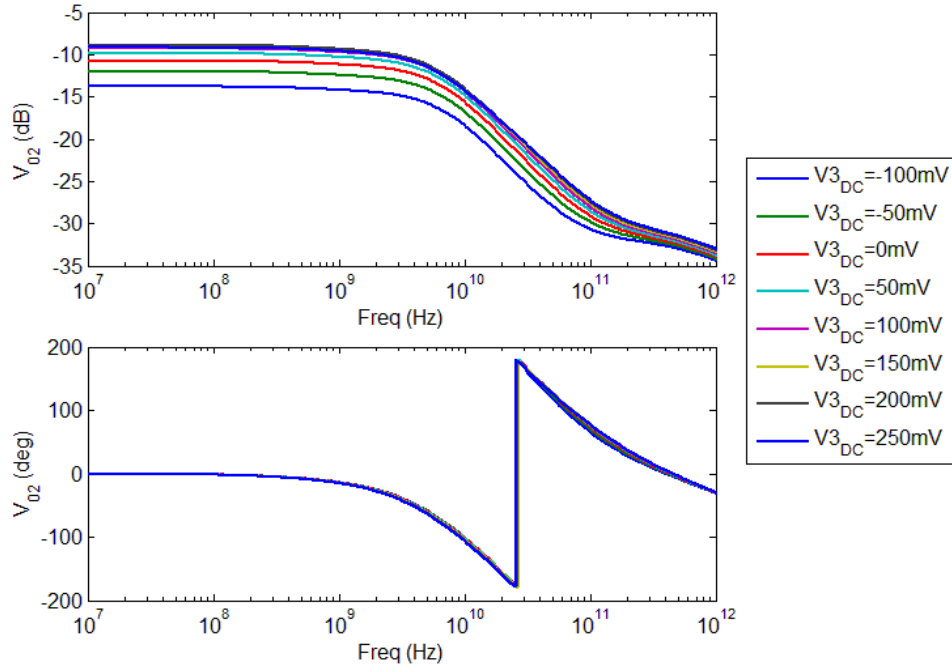


Figure 3.9: Bode plots following from an AC simulation on the circuit shown in Figure 3.6a, with an AC signal via input terminal V_1 . The DC voltage on input V_3 is swept from -100 mV to 250 mV, with steps of 50 mV.
 $V_{1,AC} = 250$ mV

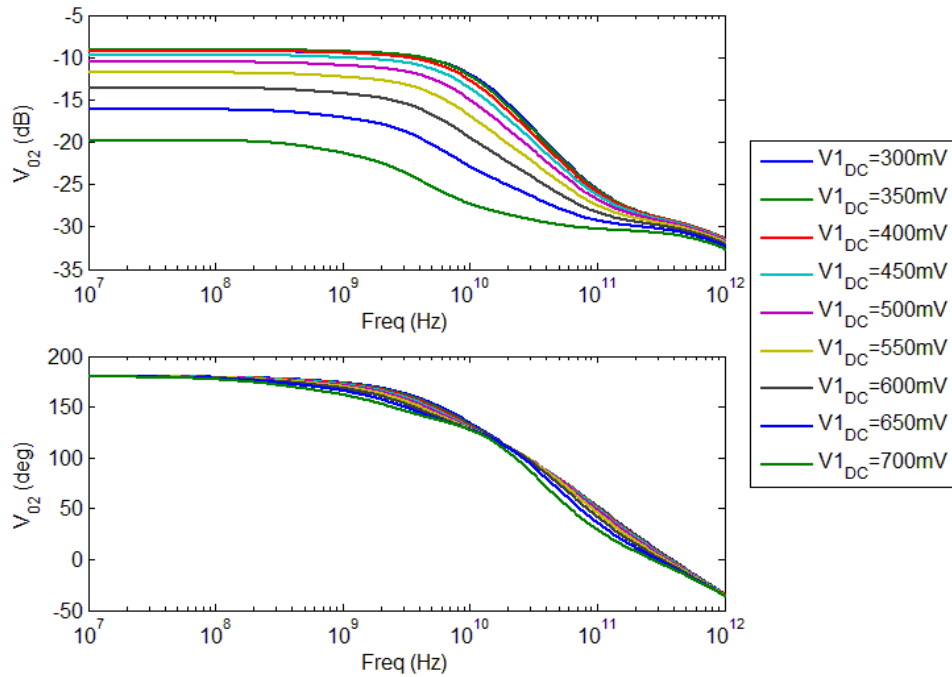


Figure 3.10: Bode plots following from an AC simulation on the circuit shown in Figure 3.6a, with an AC signal via input terminal V_3 . The DC voltage on input V_1 is swept from 300 mV to 700 mV, with steps of 50 mV.
 $V_{3,AC} = 250$ mV

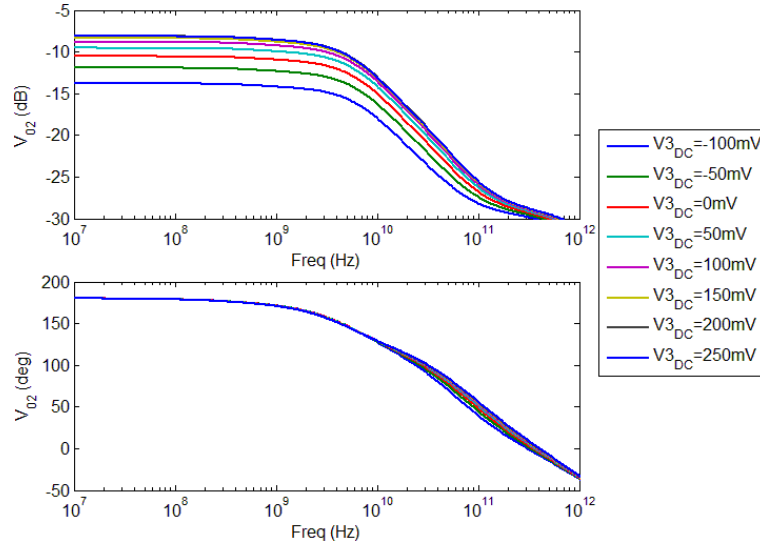


Figure 3.11: Bode plots following from an AC simulation on the circuit shown in Figure 3.6a, with an AC signal via input terminal V_3 . The DC voltage on input V_3 is swept from -100 mV to 250 mV, with steps of 50 mV. $V_{3,AC} = 250$ mV

Finally, AC simulations are performed on the total multiplier circuit of Figure 3.4. This is to check for any changes in the transfer paths now that the circuit is driven differentially. The multiplier circuit is simulated via both differential input signals (V_{id1} and V_{id2}) separately, the results of which are shown in Figure 3.12. For input V_{id1} , the differential input voltage $V_1 - V_2$ is driven with an AC signal with an amplitude of +250 mV and -250 mV respectively, and both terminals are biased at a DC voltage of 550 mV. The differential input voltage $V_3 - V_4$ is fixed at DC voltages 450 mV and -50 mV respectively. The simulation result is shown in Figure 3.12 in blue. For input V_{id2} , the differential input voltage $V_3 - V_4$ is driven with an AC signal with an amplitude of +250 mV and -250 mV respectively, and both terminals are biased at a DC voltage of 200 mV. The differential input voltage $V_1 - V_2$ is fixed at DC voltages 800 mV and 300 mV respectively. The simulation result is shown in Figure 3.12 in green.

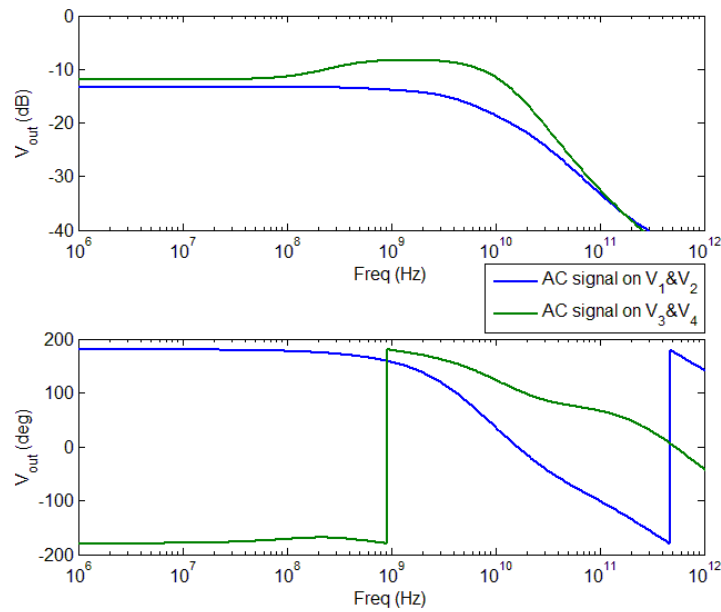


Figure 3.12: Frequency response of the multiplier circuit from Figure 3.4. Note the increase in gain in the magnitude diagram of inputs V_3 & V_4 , before the -20dB/decade roll-off

While in Figure 3.12 the blue line (representing AC path V_{id1}) corresponds with the earlier simulations shown in Figure 3.8 and Figure 3.9, the green line (representing AC path V_{id3}) presents an unexpected behaviour. An increase in gain occurs at 200 MHz, before the -20dB/decade roll-off, as shown in the magnitude diagram. This is assumed to be caused by a pole-zero doublet [39] [40]. Doublets in a transfer function can arise, for example, by feed-forward paths. The behaviour shown in Figure 3.12 may be caused by the capacitors that were previously removed due to the Miller approximation (on Page 45). While the Miller approximation was used for simplifying the AC analysis, the simulation in Figure 3.12 shows that these capacitances cannot be neglected, as they cause a closed loop in the system. A pole and zero in this transfer path are located close to each other, resulting in a pole-zero doublet³.

The advantage here is that the bandwidth of this transfer path has increased (compared to the results in Figure 3.10 and Figure 3.11), with the f_{-3dB} threshold now exceeding 10 GHz. This however does not help in increasing the overall bandwidth of the multiplier, as it is limited by input path V_{id1} . Also, this doublet in the frequency response reduces the linearity and degrades the settling time of the multiplier. While linearity is not a high specification for the receiver design, the negative influence on settling time should be prevented. Known techniques for dealing with doublet behaviour in transfer functions (such as operational amplifiers in [40]) are adding passive components to the circuit to reduce the doublets influence⁴. Adding extra passive components to the multiplier circuit is preferably prevented, as this will add extra complexity to its structure. Rather, reducing the influence of the pole-zero doublet can also be achieved by adjusting the biasing voltages of all input terminals, as it was previously discussed that all poles and zero's in the system are influenced by the biasing of the transistors. The end result is shown in Figure 3.13, on the next page.

In Figure 3.13 the previous doublet in the magnitude diagram of Figure 3.12 has been reduced, while still maintaining a high bandwidth for this particular transfer path. For the differential input V_3 & V_4 the f_{-3dB} threshold is measured at approximately 8.3 GHz. For the differential input V_1 & V_2 the f_{-3dB} threshold is measured at approximately 4.4 GHz. Unfortunately its roll-off starts before $f = 1$ GHz, measuring a 0.6 dB reduction from the maximum DC gain (-3.06 dB) at 1 GHz. This slight decrease in gain is deemed acceptable in achieving the bandwidth specification. However, the bandwidth needs to be thoroughly verified when the multiplier is tested for process corner and temperature variations, as the bandwidth is now at a critical value.

Further details regarding the simulation of Figure 3.13 are: inputs V_1 & V_2 are set at DC 550 mV, with transistors M_{1-4} biased at $1.2 - 0.55 = 650$ mV. Inputs V_3 & V_4 are set at DC 0 V; the DC voltages on the source terminals of transistors M_{5-8} are measured at 644.5 mV, therefore these transistors are biased at 644.5 mV. Transistors M_{9-12} are also biased at 644.5 mV.

³ Note that the main uncertainty here is that the doublet is not present (or observable) in Figure 3.10 and Figure 3.11, where only a part of the multiplier circuit is analysed. This would imply that the doublet is caused specifically because of the differential structure of the total multiplier circuit.

⁴ Note that these techniques can also be used to introduce doublets in a transfer function, which is meant to achieve large stable bandwidth and slew rate.

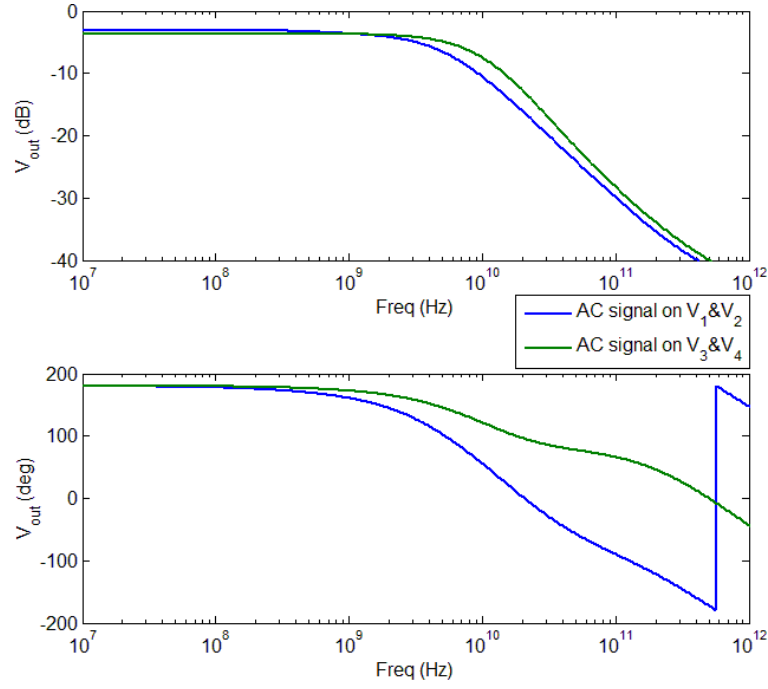


Figure 3.13: Frequency response of multiplier circuit, with AC signal performed on both differential inputs (V_1 & V_2 and V_3 & V_4) separately

Input Operating Range

The operating ranges of both differential inputs of the multiplier are influenced by the available/required supply voltage. No exact specifications for the available supply voltage or the required input operating ranges were made during the writing of this thesis. What is known however, is that the pulse generator that supplies the locally generated signal [1] has a 1 V peak-to-peak output swing. It is likely the output of the pulse generator will be connected to the multiplier via a buffer. This buffer can be designed to decrease the peak-to-peak voltage swing of the signal in order to lower the requirements on the multiplier.

Because no exact specifications on the required input range of the multiplier or the available supply voltage are known, it is useful to find the relation between these two quantities. That way the multiplier can later be modified according to this relation once any specifications are given.

From Figure 3.4 on Page 42, the overdrive voltages (otherwise known as effective voltages) for PMOS transistors M_{1-4} are defined as:

$$V_{OV,1-4} = (V_{SG,1-4} - |V_{tp}|) = \sqrt{\frac{I_{D,1-4}}{k_{p,1-4}}} \quad (3.23)$$

The maximum differential input voltage of $V_{id1} = V_1 - V_2$ can be defined as a function of the overdrive voltage of transistors M_{1-4} :

$$|V_{id1}|_{max} = 2V_{OV,1-4} \quad (3.24)$$

Forcing transistor pairs M_{1-2} and M_{3-4} into the triode region should be avoided. This brings the following condition for the differential input V_{id1} :

$$V_{1,2} < V_{DD} - |V_{tp}| - V_{OV,1\&2,3\&4} \quad (3.25)$$

where $V_{OV,1\&2,3\&4}$ is the overdrive voltage of the transistors in either pair $M_{1\&2}$ or $M_{3\&4}$. Combining Equations (3.24) and (3.25) creates the following boundaries for input signals V_1 and V_2 :

$$V_{DD} - |V_{tp}| - V_{OV,1\&2,3\&4} - 2V_{OV,1-4} < V_{1,2} < V_{DD} - |V_{tp}| - V_{OV,1\&2,3\&4} \quad (3.26)$$

Note that in Equation (3.26), the left side of the equation is defined as $V_{1,2(min)}$ (the minimum value of input signals V_1 and V_2). The input signals V_3 and V_4 can be written as a function of $V_{1,2(min)}$ and the relation between transistors M_{1-4} and M_{5-8} . Again, like with V_{id1} , the condition for differential input signal $V_{id2} = V_3 - V_4$ is that transistors M_{1-4} and M_{5-8} are not forced into the triode or subthreshold region:

$$V_{3,4} < V_{1,2(min)} - 2 \sqrt{\frac{k_{p,1-4}}{k_{p,5-8}}} V_{OV,1-4} \quad (3.27)$$

Finally, the minimal value for inputs V_3 and V_4 is determined by the threshold voltages of PMOS transistors M_{5-8} and NMOS transistors M_{9-12} :

$$V_{3,4} > V_{tn(9-12)} - |V_{tp(5-8)}| \quad (3.28)$$

Combining Equations (3.27) and (3.28) presents the following boundaries for inputs V_3 and V_4 :

$$V_{tn(9-12)} - |V_{tp(5-8)}| < V_{3,4} < V_{DD} - |V_{tp}| - V_{OV,1\&2,3\&4} - 2 \sqrt{\frac{k_{p,1-4}}{k_{p,5-8}}} V_{OV,1-4} \quad (3.29)$$

The equations derived here can be graphically shown in Figure 3.14.

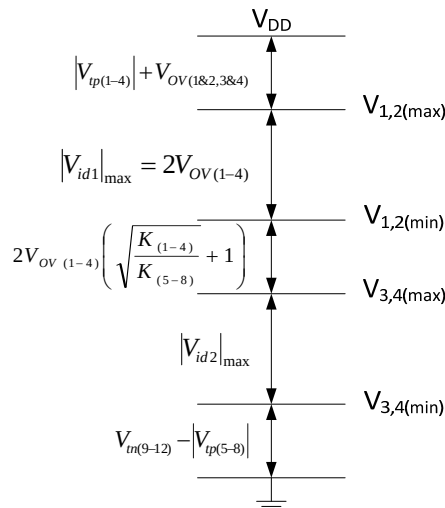


Figure 3.14: Input operating range of the multiplier circuit of Figure 3.4

Equations (3.26) and (3.29) show that, aside from a relation in size between transistors M_{1-4} and M_{5-8} , the input operating ranges are dependent only on the supply voltage and the threshold voltages of all the transistors in the circuit. Also, equations (3.26) and (3.29) can be used to calculate the common-mode points of $V_{1,2}$ and $V_{3,4}$ to allow for maximum voltage swing, if necessary.

Power Consumption

Having a low power consumption is an important requirement for biomedical electronics (Section 1.3). It is useful to derive an equation for finding the (quiescent) power consumption of the multiplier, in order to achieve minimal power consumption. The power consumption of the circuit (P_{total}) is the supply voltage (V_{DD}) multiplied by the total current consumption of the circuit (I_{total}). Considering the circuit in Figure 3.4, I_{total} is a combination of the currents going through the resistors R and transistors M_{1-8} . This gives the following relation:

$$P_{total} = V_{DD}I_{total} = V_{DD}(4 \cdot I_{1-4} + 2 \cdot I_R) \quad (3.30)$$

In Equation (3.30), parameter I_{1-4} is the current going through transistors M_{1-4} . As discussed previously on page 43, $I_{1-4} = I_{5-8}$. Taken from Equation (3.10), this current is defined as:

$$I_{1-4} = k_{p(1-8)}(V_{DD} - V_{1,2} - |V_{tp}|)^2 \quad (3.31)$$

Note that Equation (3.31) holds for when $k_{p(1-4)} = k_{p(5-8)} = k_{p(1-8)}$.

The current through resistors R was defined previously in Equations (3.5) and (3.6) on page 42. Rewriting these equations as a function of the transistor parameters and voltages in Figure 3.4 gives:

$$I_R = 2 \cdot k_{n(9-12)}(V_{GS(9-12)} - V_{tn})^2 \quad (3.32)$$

$V_{GS(9-12)}$ is defined as the voltage on the gate of transistors M_{9-12} . This voltage was previously defined by Equation (3.11) on page 43, and is rewritten here as a function of input voltages V_{1-4} :

$$V_{GS(9-12)} = V_{3,4} - V_{1,2} + V_{DD} \quad (3.33)$$

Finally, combining Equations (3.30) through (3.33) gives the following result for the total quiescent current consumption of the multiplier circuit:

$$I_{total} = 4 \left[k_{p(1-8)}(V_{DD} - V_{1,2} - |V_{tp}|)^2 + k_{n(9-12)}(V_{3,4} - V_{1,2} + V_{DD} - V_{tn})^2 \right] \quad (3.34)$$

Note that these equations only determine the quiescent power consumption (at DC operation), as time-dependent parameters (such as $V_{id1}(t)$ and $V_{id2}(t)$) are neglected. Still, these equations show what parameters directly influence the power consumption of the circuit. In Chapter 4 the average power consumption over time will be measured during transient simulations.

3.4.2 Circuit Design

In this subsection the multiplier circuit is implemented according to the requirements for the correlation receiver, using the equations and information derived in the previous subsection. Some adjustments are made to the circuit for improvement, in terms of power consumption and area. At the end of this subsection the complete circuit design with corresponding parameter values is presented.

Replacing output resistors R with transistors

During the circuit designing procedure, the decision was made to replace the two passive resistors R with MOS transistors. This is mostly done to reduce the area on a chip, as resistors generally occupy more chip area than transistors. Using transistors may also improve the circuit's robustness over process variations, as passive resistors' values can have a large spread over process variation. Process variation on the circuit is further discussed in the next chapter on simulations.

PMOS transistors are implemented instead of NMOS transistors because of the body effect, which is less evident in PMOS transistors. The gates of the transistors are connected to ground, thus operating them in strong inversion triode region. While the use of diode connected transistors are more common, transistors operating in saturation regions are preferred as this increases the gain and bandwidth of the circuit.

The main disadvantage of using transistors instead of passive resistors is that the multiplier is now less linear. This is because the voltage at the drain terminals changes according to the input voltages V_{id1} and V_{id2} , which changes the operating conditions of the transistors. Since chip area is a higher requirement than linearity, this disadvantage is discarded.

Note that the resistors' primary function is to act as a load and convert the output current into a voltage. If the next stage after the multiplier requires a current signal, a current mirror is used to generate a current output. Such a (differential) current output would be designed as shown in Figure 3.15.

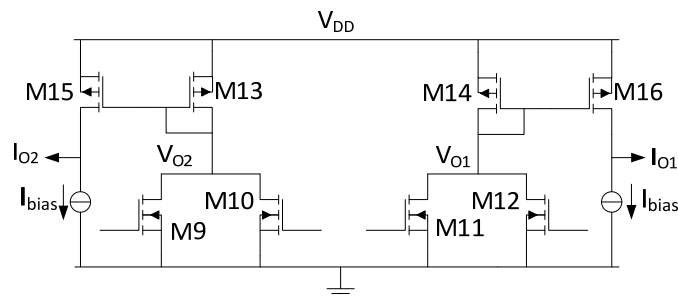


Figure 3.15: Output stage of multiplier with current output implementation, by means of current mirrors $M_{13}&M_{15}$ and $M_{14}&M_{16}$

The output transistors that were previously discussed in this subsection are modified to operate as current mirrors. The mentioned current mirrors are transistors $M_{13}&M_{15}$ and $M_{14}&M_{16}$. Two current sources (I_{bias}) are also added, to compensate for (unwanted) common mode voltages at the output. Note that the other components in the multiplier remain unmodified.

This thesis will focus only on the multiplier with a differential voltage output, as a current output is not specifically required for the simulations performed in the next chapter.

Final Circuit Implementation

The final circuit implementation of the multiplier is shown in Figure 3.16 below. The MOSFET transistor dimensions are specified in Table 3.2, and the parameters for supply voltage, transistor biasing and maximum input voltage swings are specified in Table 3.3. The common mode voltages measured at each output voltage node is also specified in Table 3.3.

Table 3.2: MOSFET dimensions

Transistor	W (μm)	L (μm)
PM1-4	1.25	0.18
PM5-8	1.25	0.18
NM9-12	0.5	0.18
PM13-14	1.25	0.18

Table 3.3: Supply, transistor biasing and voltage swing parameters

Parameter	Voltage (V)
V_{DD}	1.2
Biasing NM1-4	0.55
Biasing NM5-8	0
Voltage swing V_{1-4}	0.5
DC Voltage at output nodes V_{O1} and V_{O2}	1.113

As shown in Table 3.2, all MOSFET dimensions are designed as small as possible in order to reduce chip area and power consumption. The transistor lengths are kept at the minimal length that the CMOS technology has to offer, 0.18 μm . Having such small transistor dimensions might cause issues when the circuit is tested for process corner variations. Also, having small channel lengths increases the influence of channel length modulation. Whether or not these influences are an issue to the operation of the multiplier will be further examined in the next chapter. Also note that the PMOS transistors have a 2.5 times larger W/L ratio compared to the NMOS transistors, because the hole mobility in PMOS is a factor 2.5 times less than the electron mobility in NMOS.

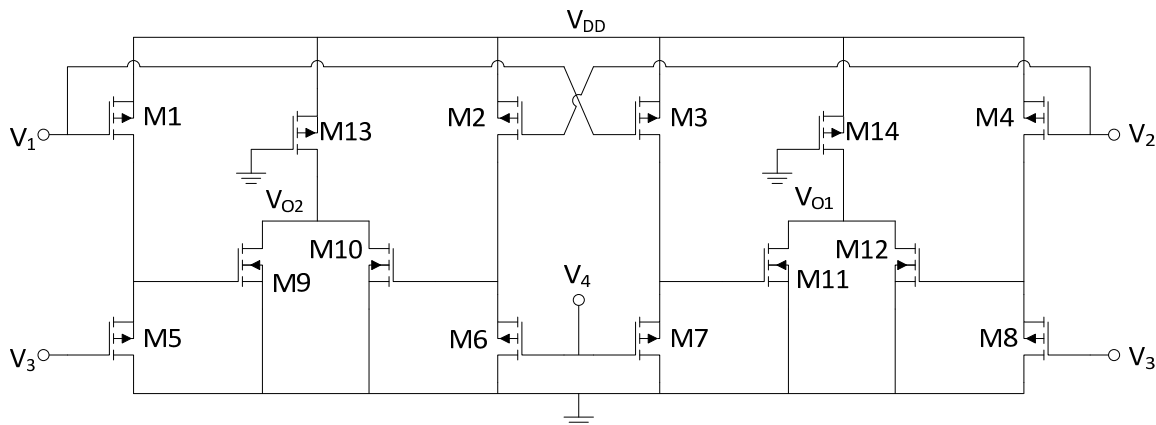


Figure 3.16: Low power, four-quadrant, 1 GHz multiplier

3.5 Summary

In this chapter a low-power, MOS-only, four-quadrant multiplier circuit with 1 GHz bandwidth is designed for the correlation receiver from Chapter 2. The 0.18 μm High-Voltage CMOS technology from AustriaMicroSystems (AMS) is used for designing the circuit.

While examining the system design for the correlation receiver, it is decided that the multiplier block is an important part of the receiver architecture. The other blocks in the system design, while also having significant importance for the operation of the receiver, are either already designed or have examples available that can be used.

The designing process is performed as follows. A suitable operating region of the transistor is chosen in order to achieve a bandwidth of 1 GHz. It was decided to operate in the strong inversion saturation region. This decision leads to a multiplier architecture based on squaring devices. Next, several known (published) multiplier circuits are examined and discussed. From this list a compact, low-voltage, low-power, highly-linear CMOS four-quadrant analog multiplier circuit is chosen as a suitable circuit for the correlation receiver. Its only drawback is that the published multiplier has a low bandwidth (100 MHz), so design steps have to be taken in order to achieve a bandwidth of 1 GHz.

The chosen multiplier circuit is analysed. Its transient operation, frequency response, (quiescent) power consumption and input operating range are discussed. During the analysis and design process, the linearity of the multiplier is sacrificed for low-power operation, small chip area and high bandwidth. This is because the correlation receiver does not require a multiplier with high linearity.

Finally, the total multiplier circuit consists of only MOS transistors, thereby making it easier to be integrated on chip. The MOS dimensions are kept as small as possible in order to save chip area.

4 Simulation Results

In this chapter the designed circuit from Chapter 3 is verified with circuit simulations. First the functionality of the circuit is verified. Then the robustness of the circuit is tested by varying process corners, device mismatch (MonteCarlo), varying the supply voltage and the temperate. These simulations are performed in Cadence RF Spectre. Finally, the results obtained from multiplier circuit design from Cadence is incorporated into the system design (Matlab) from Chapter 2. This way the entire system design is fully tested with the functionality of the designed multiplier.

4.1 Circuit Design Verification

This section tests the functionality of the multiplier circuit design presented on Page 56. Note that for all simulations the biasing and supply conditions for the multiplier are, unless specified otherwise, taken from Table 3.3 on Page 56.

For each simulation the two differential inputs V_{id1} and V_{id2} are simulated separately (as previously discussed on Page 45, on AC analysis). This is to check for differences between the signal paths.

Figure 4.1 shows the frequency response of the proposed multiplier circuit, with an AC signal performed on V_{id1} and a DC value on V_{id2} (Figure 4.1a) and vice versa (Figure 4.1b). Various gains are shown by stepping the AC input signal's amplitude from 0.1 to 0.5V.

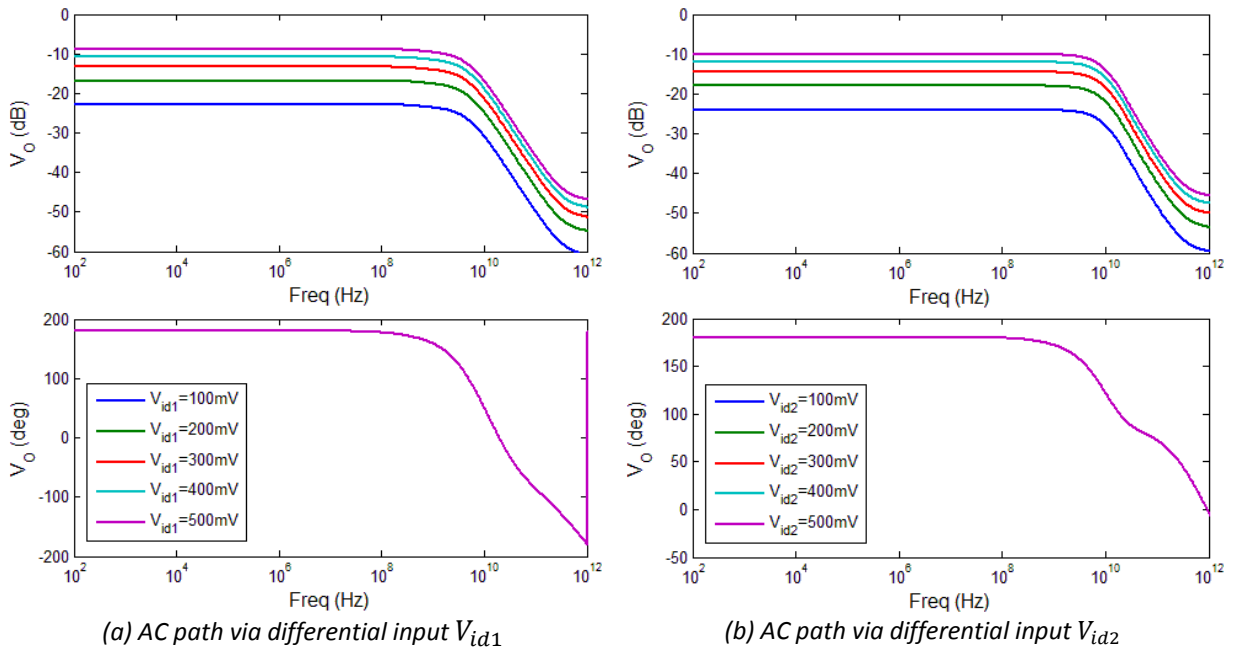


Figure 4.1: Frequency response of the proposed multiplier circuit

From Figure 4.1a, it can be seen that via signal path V_{id1} the f_{-3dB} frequency is at 3.98 GHz. Note that there is a decrease of 0.79 dB at 1 GHz. From Figure 4.1b, it can be seen that signal path V_{id2} has a larger bandwidth, having the -3 dB threshold at 8.51 GHz. Finally, by comparing the two images it is also noticeable that the signal path V_{id2} has a lower gain of 1.2 dB. This lower gain is because the

PMOS transistors M_{5-8} driven by V_{id2} are connected as source followers, therefore not generating any gain (as opposed to the PMOS transistors M_{1-4} driven by V_{id1}). While this can be corrected by adjusting the ratio between transistors M_{1-4} and M_{5-8} , it is decided not to: the transistors are deliberately kept as small as possible. It is expected this difference in gain will not be an issue for the correlation receiver.

Figure 4.2 shows the DC transfer characteristics of the multiplier. In Figure 4.2a, V_{id1} is continuously swept from -0.5 to 0.5V, while V_{id2} varies in the similar range but with a 0.1 V step size. This is done vice versa in Figure 4.2b.

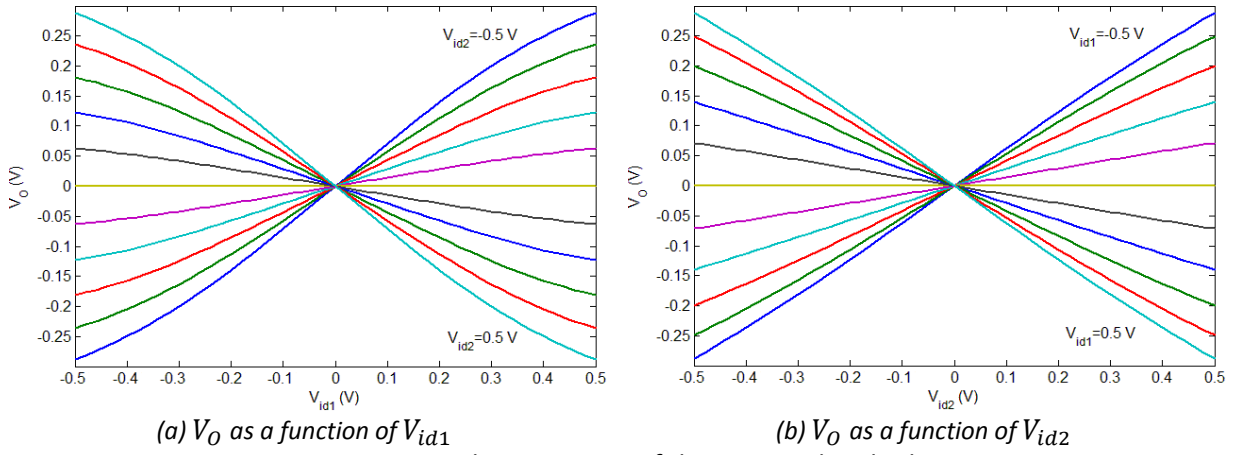


Figure 4.2: DC characteristics of the proposed multiplier

It can be observed in Figure 4.2b that the path from V_{id2} to output V_O provides good linearity. However, the path from V_{id1} to output V_O shows poorer linearity, as shown in Figure 4.2a.

Figure 4.3 shows the performance of the multiplier configured as a balanced modulator where a 0.5V, 40MHz sinusoidal V_{id1} modulating signal is multiplied by a 0.5V, 1GHz sinusoidal V_{id2} carrier signal (displayed by the blue line) and vice versa (displayed by the green line).

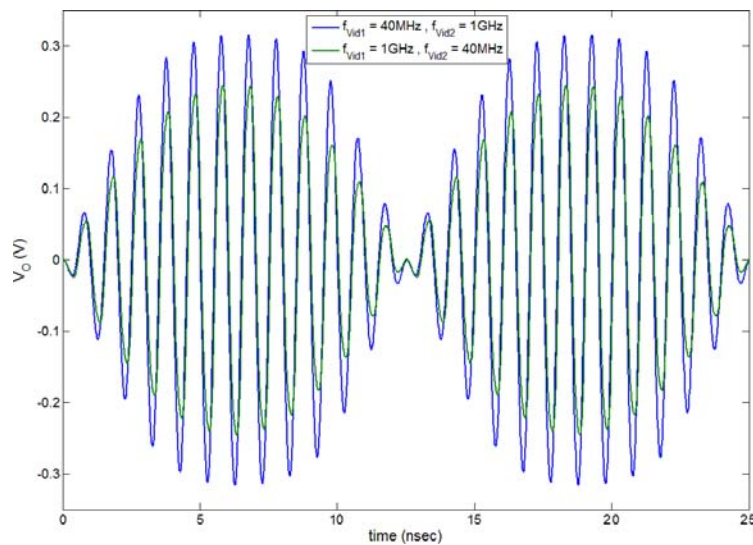


Figure 4.3: Transient response of the proposed multiplier

Figure 4.3 shows some characteristics of the multiplier design that are also visible in Figure 4.1 and Figure 4.2. For instance the blue line has a higher output amplitude swing than the green line, and upon closer inspection the green line contains slewing. This is because for the blue line the 1GHz carrier signal is done via input terminal V_{id2} , which as previously shown in Figure 4.1 has a higher bandwidth than input path V_{id1} . Also, the poor linearity of the multiplier, visible in Figure 4.2a, is displayed by the blue line. Despite this, the waveforms of the carrier and modulating signals are still visible in the graph.

The average power consumption over time is also measured during the transient response of Figure 4.3, using the following equation:

$$P_{avg} = \frac{1}{t} \int_T^{T+t} V_{DD} \times I_{supply} dt \quad (4.1)$$

Where t is the time during which the power consumption is measured and T a specific period in a transient simulation. For the blue line in Figure 4.3, an average power consumption of 144.3 μ W is measured; for the green line it's 153.2 μ W. The power consumption is also measured when no input signals are applied, which is 97.06 μ W, indicating that the multiplier still consumes a large amount of power when it is not being used. This is because the transistors are always on (biased in the strong-inversion saturation region) and thereby always having a current pass through. While this thesis will not focus on a solution to this issue, it may be suggested that the power consumption can be reduced by turning the transistors off when the multiplier is not being used. This process of turning the transistors ON and OFF can be regulated by controlling the bias voltages of the transistors.

The noise contribution of the multiplier circuit is also measured. The noise plot of the circuit, from input to output, is shown in Figure 4.4.

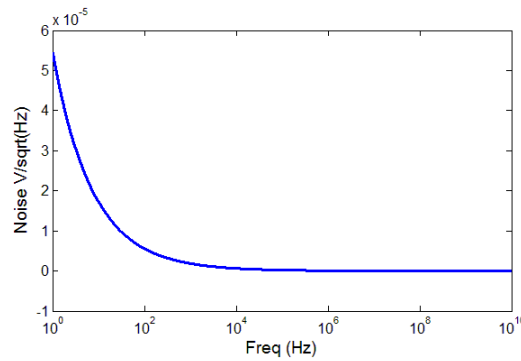


Figure 4.4: Contributed noise of the proposed multiplier

As shown in Figure 4.4, pink noise (or $1/f$ noise) is the most dominant noise contributor in the circuit. Luckily this noise has little influence at higher frequencies (as its contribution is very small from 1 kHz). At 1 GHz, the total summarized noise is $1.8 \times 10^{-8} V/\sqrt{Hz}$. It is found that the output transistors M13 and M14 (of Figure 3.16) contribute the most noise (16.54% each). The other transistors contribute 6% or less noise. Integrating the noise figure shown in Figure 4.4 from 1 Hz to 1 GHz gives a noise contribution of 0.67 mV. Considering the small amount of noise (compared to the signal magnitude) that the circuit contributes, and the assumption that for the correlation receiver

only the energy of the output signal is of importance, no extra precautions on noise reduction are performed.

4.2 Circuit Robustness tests

This section tests the robustness of the multiplier circuit, by varying several parameters which may vary in practice. These parameters are device mismatch, process corners, temperature and the supply voltage.

4.2.1 Device Mismatch

The influence of device mismatch (between MOS transistors) on the multiplier's performance is checked with a Monte Carlo simulation. The frequency response of the multiplier, from Figure 4.1, is simulated with 200 Monte Carlo runs. The result of these 200 Monte Carlo runs is shown in Figure 4.5.

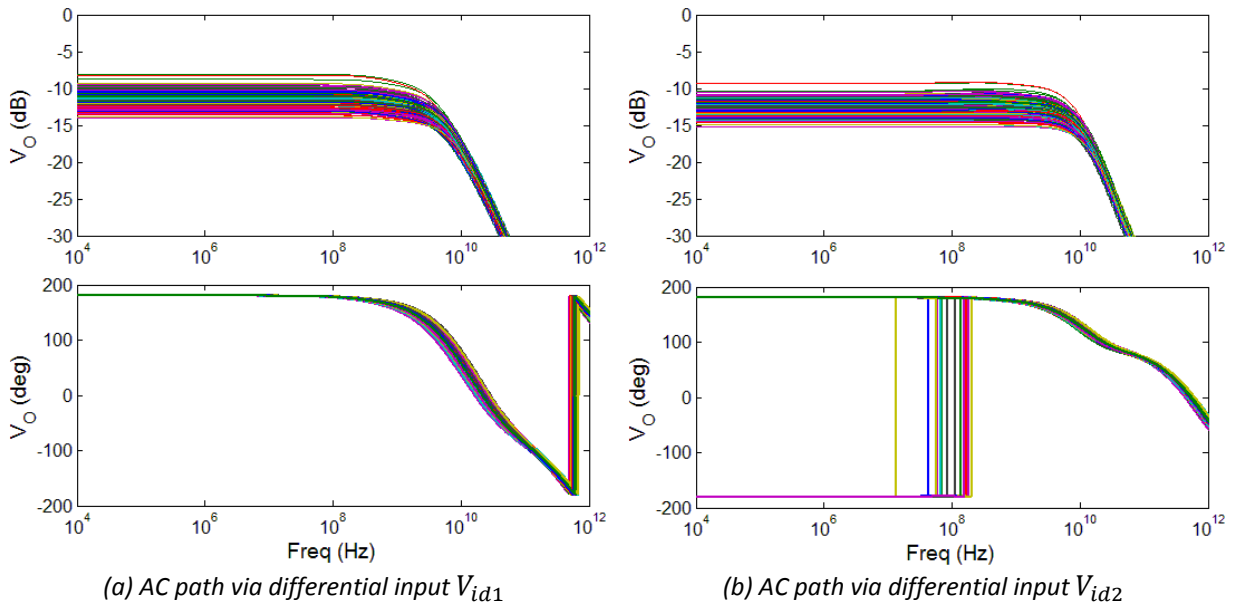


Figure 4.5: Effect of Monte Carlo simulations (200 runs) on the frequency response of the multiplier

As shown in Figure 4.5, the bandwidth of the multiplier (via both AC paths) is not affected: the f_{-3dB} threshold remains above 1 GHz. However, the DC gain of the multiplier varies over each Monte Carlo run. For Figure 4.5a, a maximum DC gain deviation of 60% is measured. For Figure 4.5b, the maximum DC gain deviation is 52%.

The transient response of the multiplier, from Figure 4.3, is also performed with 200 Monte Carlo runs, and is shown in Figure 4.6.

As shown in Figure 4.6, the waveform of the signal is unaffected, which indicates that the linearity of the multiplier has not been reduced/improved much. However, the maximum voltage output swing varies over each Monte Carlo run. This deviation in maximum output swing corresponds with the Monte Carlo results from Figure 4.5.

Finally, a statistical device mismatch analysis is conducted by measuring the average power consumption (from Equation (4.1)) of 180 Monte Carlo runs. The results are shown in Figure 4.7, where the number of Monte Carlo distributions are plotted as a function of the deviation from the nominal power consumption.

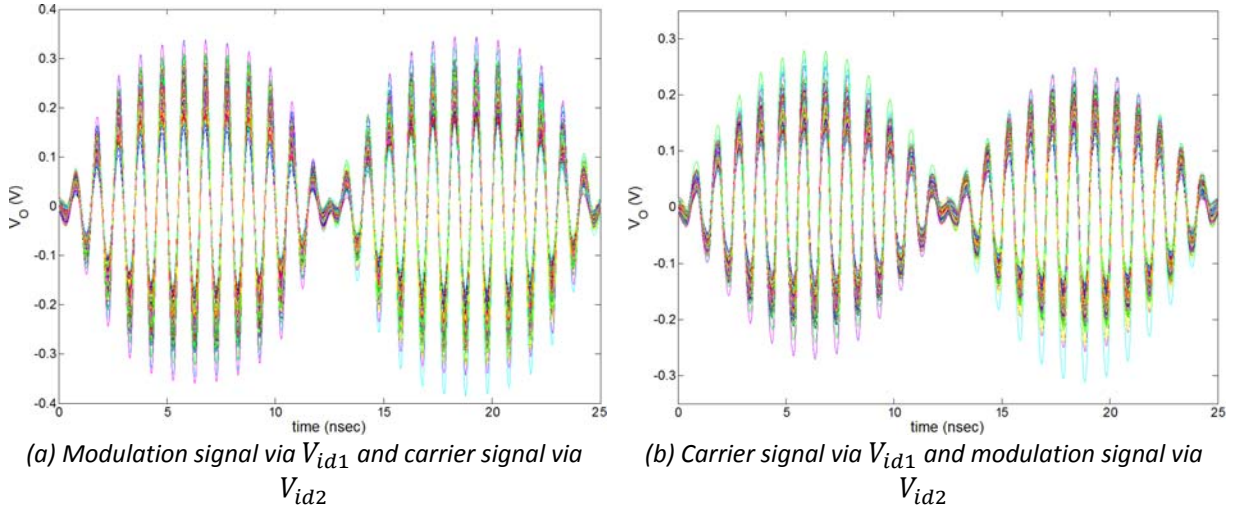


Figure 4.6: Effect of Monte Carlo simulation (200 runs) on the transient response of the multiplier

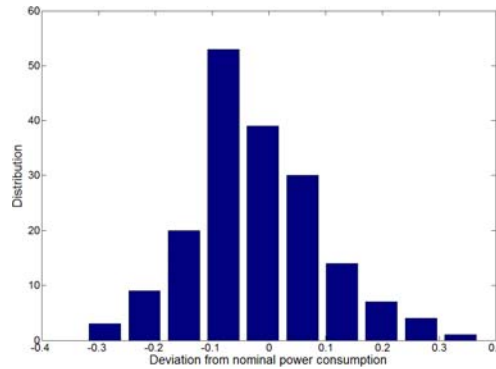


Figure 4.7: Monte Carlo distribution results for nominal power consumption (180 runs)

The Monte Carlo distribution in Figure 4.7 has a bell-shaped curve, with the maximum peak close to little or no deviation from the nominal power consumption. This indicates a minimal deviation from the expected results of the multiplier.

In conclusion, the most important specification of the multiplier, bandwidth, is unaffected by device mismatch. The change in output gain should not be an issue for the correlation receiver, as long as the stage after the multiplier can still measure the signal.

4.2.2 Process Corners

When an integrated circuit is mapped on a semiconductor wafer, variations in fabrication parameters occur due to aspects such as variations in temperature and humidity of the environment during the manufacturing. Process corners represent the extremes of these parameter variations, and thereby help verify the robustness of the integrated circuit design. Since the multiplier circuit only consists of

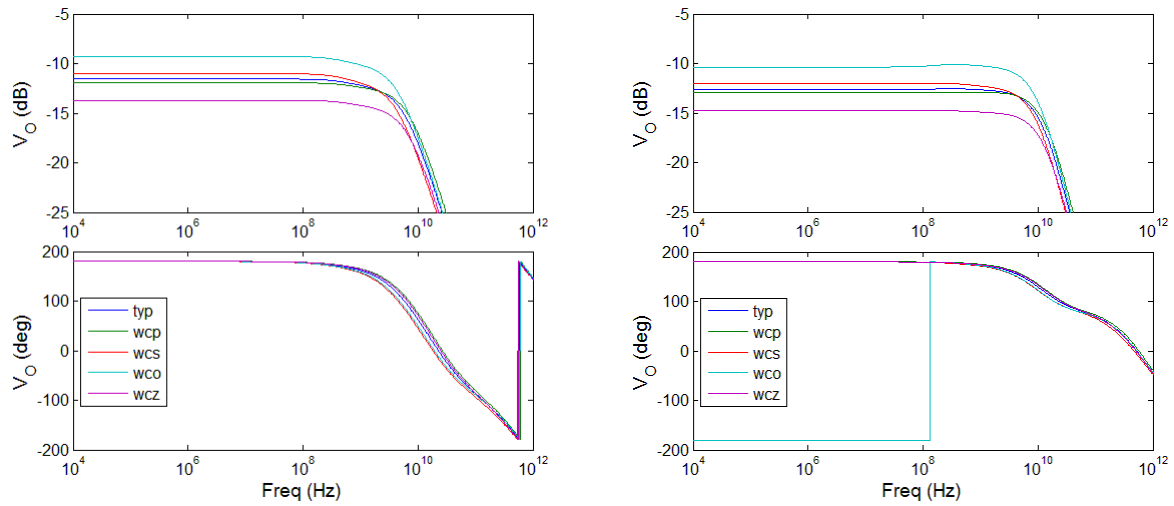
MOS transistors, the process corners for these specific components will be used. The five different MOS corners specified for the 0.18 μm Technology are shown in Table 4.1.

Table 4.1: Process corners

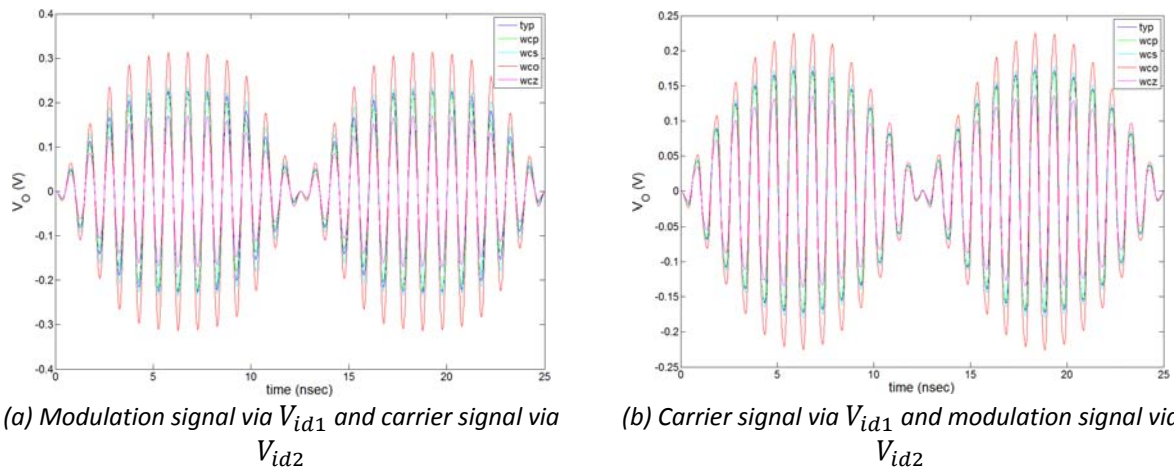
Corner type	3σ corner
Typical	typ
Slow N, Slow P	wcs
Fast N, Slow P	wco
Slow N, Fast P	wcz
Fast N, Fast P	wcp

The corners shown in Table 4.1 are: worst case power (wcp), worst case speed (wcs), worst case zero (wcz) and worst case one (wco). The effect on the N and P dopants corresponding to each corner is also shown in Table 4.1. The “typical” corner type is when no variations are performed on the fabrication parameters.

The simulations from Figure 4.1 and Figure 4.3, previously performed in Section 4.1 are simulated again with the process corners. The results are shown in Figure 4.8 and Figure 4.9.



(a) AC path via differential input V_{id1}
(b) AC path via differential input V_{id2}
Figure 4.8: Effect of process corner simulation on the frequency response of the multiplier



(a) Modulation signal via V_{id1} and carrier signal via V_{id2}
(b) Carrier signal via V_{id1} and modulation signal via V_{id2}
Figure 4.9: Effect of process corner simulation on the transient response of the multiplier

As shown in Figure 4.8 and Figure 4.9, the output gain of the multiplier circuit varies over each corner (similar to the device mismatch simulations performed in the previous subsection). Fortunately, the bandwidth of the multiplier is still greater than the specified 1 GHz, and no significant changes in the waveform of the output signal (Figure 4.9) are noticeable. This concludes that the multiplier circuit is sufficiently robust over all process corners.

4.2.3 Temperature

The specifications for the temperature range were previously discussed in Section 3.2. The operating temperature range is specified from -10 to 70 °C. Redoing the simulations from Section 4.1, now adding temperature as a parameter, shows a change in output signal amplitude or gain of at most 7%, which is considered negligible. No significant change in signal waveform or bandwidth is noticeable. This concludes that the multiplier circuit is robust over temperature variations.

4.2.4 Supply Voltage

It was assumed in Section 3.2 that the circuit design would be supplied with a stable power supply, provided by a power management system. Still, the robustness of the multiplier circuit against variations in the supply voltage needs to be tested. The frequency simulations from Figure 4.1 are performed, now with varying V_{DD} .

Note that the biasing voltages on transistors M_{1-4} also vary according to V_{DD} in order to keep $V_{SG,1-4}$ at 650 mV. This is because otherwise the simulation results will only show the multiplier's performance change due to the transistors being differently biased. Transistors M_{1-4} are especially sensitive to this effect since they are connected directly to V_{DD} .

The frequency responses of inputs V_{id1} and V_{id2} are again performed separately. For both responses the bandwidth of the multiplier is still (greater than) 1 GHz even with a reduction of 30% in the supply voltage. For input V_{id1} the bandwidth rapidly decreases once V_{DD} decreases further than 30%. The input V_{id2} is more robust against decreasing V_{DD} , however the pole-zero doublet, previously discussed on Page 51, becomes more prominent in the frequency response. An increase in V_{DD} does not decrease the bandwidth of the circuit.

The gain of the frequency response of both inputs varies with varying V_{DD} . For both inputs the gain decreases for increasing V_{DD} and increases for decreasing V_{DD} . For V_{id1} , a reduction of 30% in V_{DD} results in a decrease of 29% in gain, an increase of 30% results in a decrease of 35%. For V_{id2} , a reduction of 30% in V_{DD} results in a decrease of 11.68% in gain, an increase of 30% results in a decrease of 22%.

These simulations show that the multiplier circuit is robust against varying supply voltage. It should however be noted that this conclusion holds as long as the biasing voltages of the transistors are modified accordingly. The robustness of the circuit was also tested when the biasing voltages on transistors M_{1-4} are not modified, which resulted in the multiplier failing the bandwidth specification.

at a 13.3% decrease in V_{DD} . Modifying the biasing voltages according to varying V_{DD} can be done with a (tuneable) biasing control circuit, however no such circuit has been designed during the writing of this thesis.

4.3 System (Matlab) Implementation

In this section, the multiplier circuit design from Chapter 3 is combined with the correlation receiver design from Chapter 2. More specifically, the methods and simulations described in Sections 2.5 and 2.6 are performed here again, only this time the ideal multiplier block in the Matlab/Simulink environment is replaced by the multiplier circuit design from Chapter 3.

The simulations of interest are the ones shown in Figure 2.20 and Figure 2.21 (on Page 29), where 1000 pulses are sent through several receivers while the added interference to the received signal gradually increases over each simulation. The intention in this section is to run simulations for the correlation receiver with the ideal multiplier block, and the correlation receiver with the proposed multiplier circuit design; the results derived from these simulations are then compared with each other.

It should be noted that the number of transmitted pulses is reduced to 200 due to the size and complexity of the simulations. It was found that running 1000 pulses, while trying to maintain high resolution, resulted in large amounts of data that takes Cadence and Matlab a long time to process. Therefore, a trade-off between the number of transmitted pulses and the resolution of the signal had to be made. It was deemed 200 pulses would still give a good indication of the performance of the receivers.

Instead of directly taking the data from Figure 2.20 and Figure 2.21 to use for comparison, the simulations for the correlation receiver with the ideal multiplier were performed again. This is especially important for the noise interference simulations because of its random, unpredictable behaviour (as previously noted on Page 30). The QDaC and energy detector receivers are left out: the proposed multiplier is not designed specifically for these receivers, so their performance results are not necessary in this section. The simulation results are shown in Figure 4.10 and Figure 4.11 on Page 66.

As shown in Figure 4.10 and Figure 4.11, the receivers with the designed circuit multiplier (from Cadence) have an identical slope as the receivers with the ideal multipliers (from Matlab). Unfortunately, according to the figures the receivers with the designed multiplier are less robust than the ones with the ideal multiplier. An average difference of 20 pulses is observed. Upon closer inspection, it was discovered that the main issue is in the performance of Cadence and Matlab, rather than the simulation setup itself. Because of the required size of the simulations, the programs automatically compress data in order to save space (thereby throwing away information). This is unfortunate for the simulation setup, as the simulations focus specifically on the waveform of the measured signals.

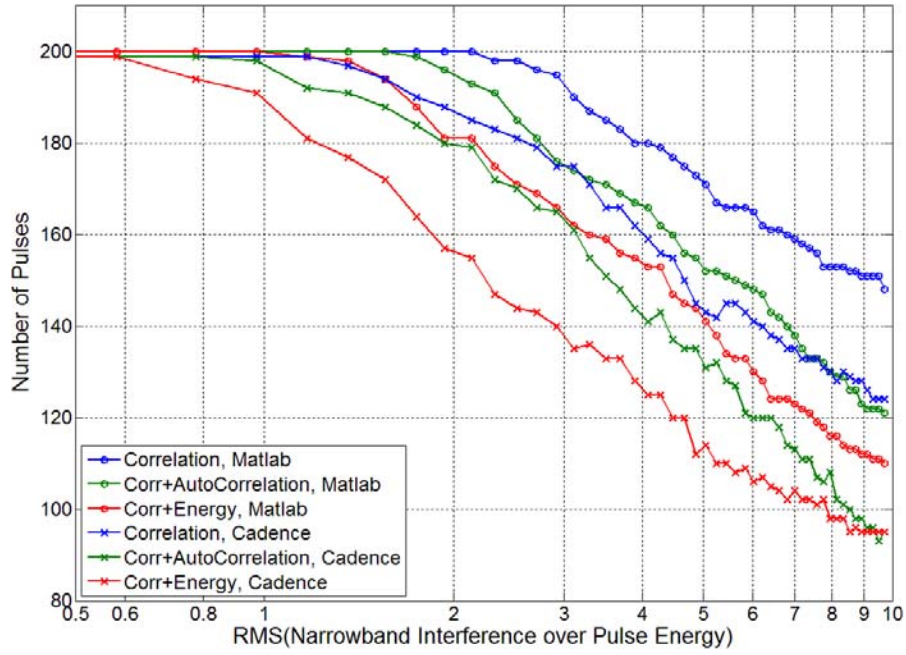


Figure 4.10: Narrowband Interference Simulation

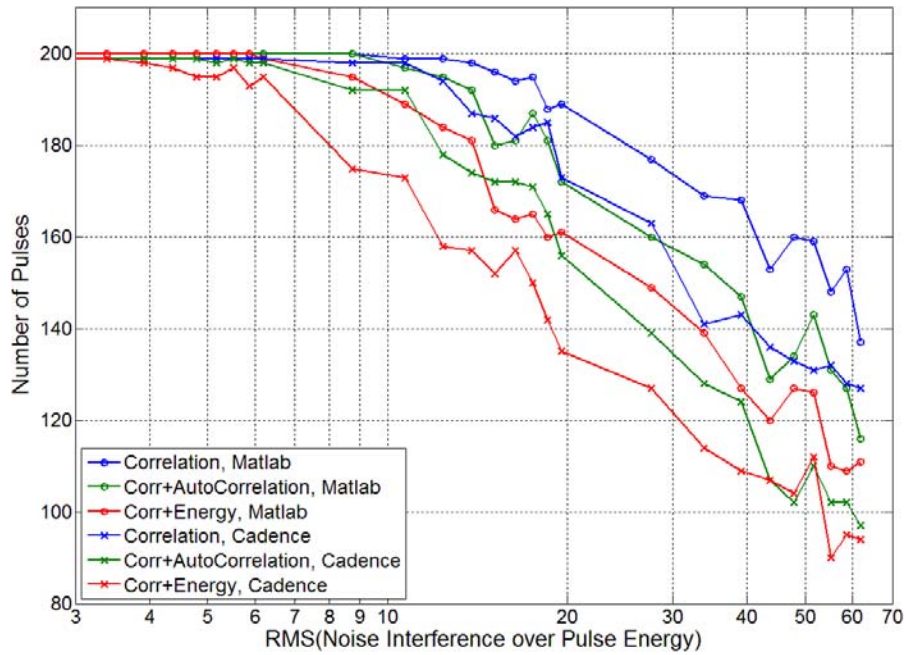


Figure 4.11: Noise Interference Simulation

The issue performance shown in Figure 4.10 and Figure 4.11 is solved by configuring the simulation programs to utilise a high resolution of at most 2 psec per step. This configuration resulted in such heavy simulation data that it is difficult for the programs to operate without having memory issues. It was decided to redo only a few of the simulations, enough to have a sufficient comparison between the ideal and the designed multiplier. The results are shown in Figure 4.12 and Figure 4.13 on Page 67.

While the results shown in Figure 4.12 and Figure 4.13 do not show the receivers' behaviour over the same amount of interference levels (although the acquired range is identical), the figures do show

that the receivers with the designed multiplier are as robust against interference as the receivers with the ideal multiplier.

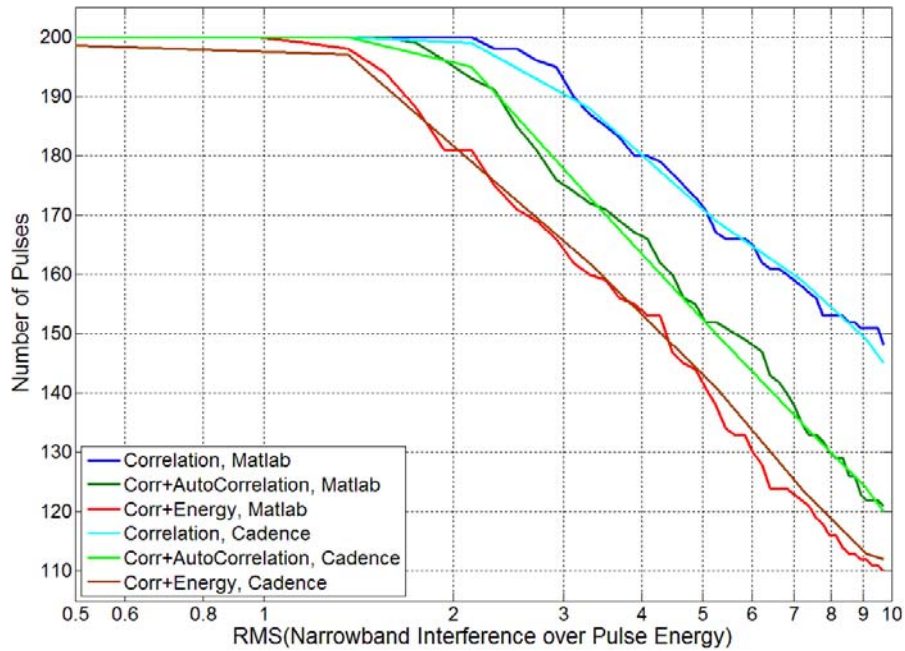


Figure 4.12: Narrowband Interference Simulation, after improving data resolution

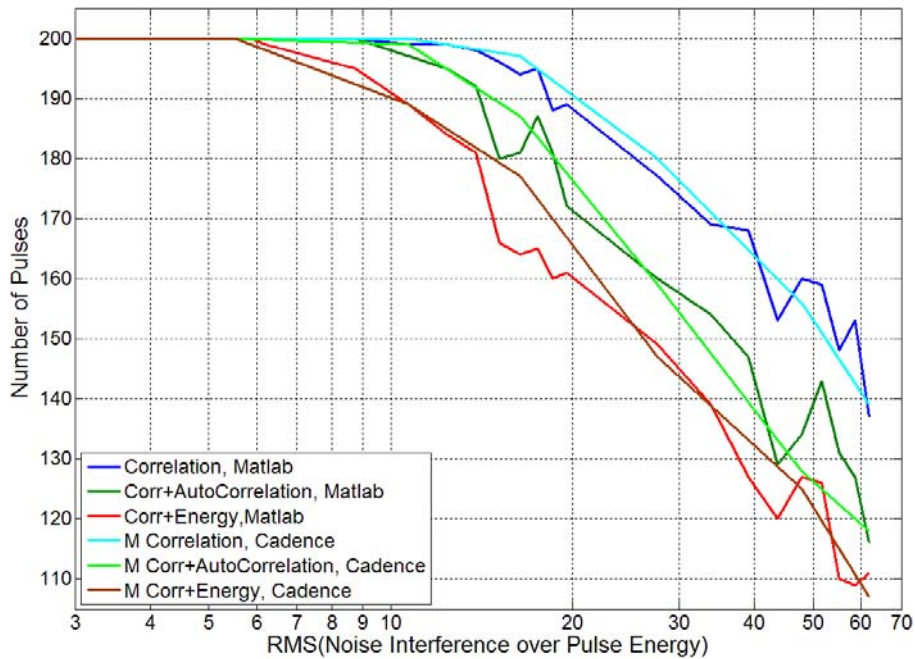
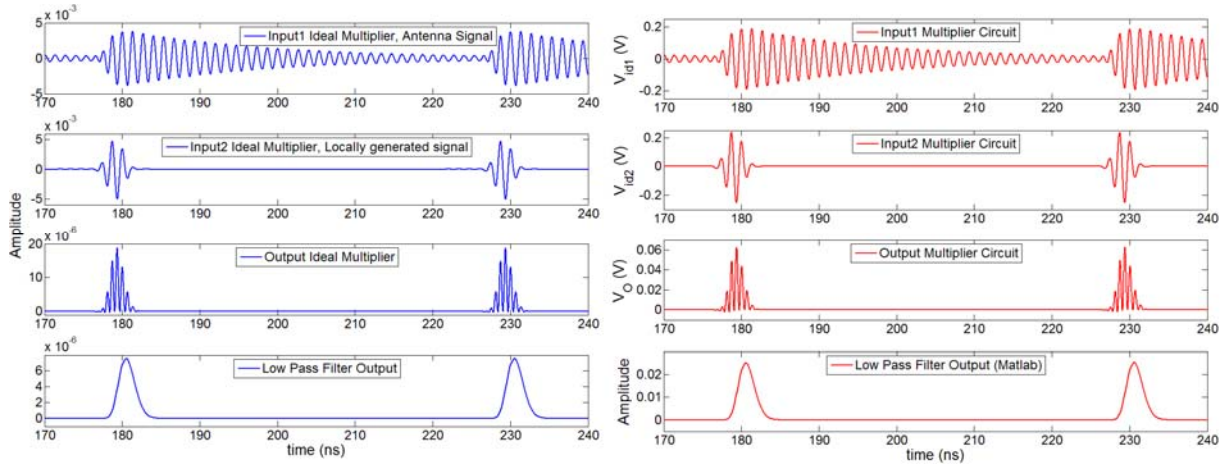


Figure 4.13: Noise Interference Simulation, after improving data resolution

Finally, the multiplier is also tested for its response to multipath interference. The response of the correlation receiver on multipath interference was previously shown in Figure 2.23 on Page 31. The multipath simulation is again performed here on the proposed multiplier circuit design, while expecting similar results to the previous multipath simulation of Figure 2.23. The result with the designed multiplier is shown in Figure 4.14 on Page 68. Note that the result of Figure 2.23 is again displayed here for comparison.



(a) Multipath simulation on correlation receiver with ideal multiplier. Results are taken from Figure 2.23 on Page 31

(b) Multipath simulation on correlation receiver with proposed multiplier circuit design

Figure 4.14: Comparing the correlation receivers' response to multipath interference with (a) an ideal multiplier and (b) the proposed multiplier circuit. Shown signals from top two bottom (for both figures) are: antenna signal with interference (V_{id1}), locally generated signal (V_{id2}), multiplier output (V_O) and the output of the subsequent Low Pass filter.

Figure 4.14a (with the blue graphs) is the multipath, transient simulation result from Figure 2.23. From top to bottom, the shown signals are: the received signal from the antenna with multipath interference⁵, the locally generated signal, the ideal multipliers' output and the output of a Low Pass Filter. Figure 4.14b (with the red graphs) has the same layout, but now the proposed multiplier circuit is utilised. Displayed here are the multiplier input signals V_{id1} and V_{id2} , and output signal V_O from Cadence. The subsequent Low Pass Filters' result is generated in the Matlab environment. Comparing the results of both figures with each other shows that the correlation receiver's performance against multipath interference with either the ideal or the proposed multiplier are similar: the effects of the added multipath interference are removed⁶. Therefore, the designed multiplier is also robust against multipath interference.

This section concludes that the designed multiplier from Chapter 3 has passed the required test in that it reproduces the performance of the ideal multiplier in the correlation receiver.

4.4 Summary

In this chapter the performance of the low power, 1 GHz multiplier (from Chapter 3) is tested with Cadence RF Spectre simulations. The designs functionality is verified by performing DC, frequency and transient simulations. From these simulations it is concluded that the bandwidth of the multiplier is 1 GHz but has poor linearity (compared to its original design proposed in [32]). The average power consumption (over time) is 153.2 μ W (from a 1.2 V supply), thereby indicating that the multiplier consumes little power. The measured noise contribution of the multiplier is low

⁵ The configuration of the multipath interference on this signal is taken from Page 31, where the multipath gain factor ρ is set at a(n) (unrealistic) value of 0.99.

⁶ It should be noted that, having a very low Pulse Repetition Frequency of 1 MHz, the effects of multipath interference on the receiver are very low. The PRF of the (tested) signal shown in Figure 4.14 is higher: 20 MHz.

(compared to the signal amplitude): the integrated noise from 1 Hz to 1 GHz was calculated at 0.67 mV.

The multiplier is robust over all process corners and device mismatch runs (i.e. the circuits bandwidth and signal waveform are not affected), indicating that the majority of the fabricated circuits will fall within the performance specifications. The circuit is also robust over wide temperature range. The multiplier is robust against supply voltage variations, as long as the biasing of the transistors in the circuit are modified accordingly. To achieve this, a tuneable biasing control circuit should be added to the design.

Finally, the designed multiplier (from the Cadence environment) is implemented into the system design of the correlation receiver (the Matlab environment), in order to compare its performance with an ideal multiplier. Like in Chapter 2, the receivers are tested for their robustness against narrowband, noise and multipath interference. It was eventually shown that the simulated results of the designed multiplier are identical to an ideal multiplier. It should however be noted that the simulation set-up is sensitive to compression in the data files, caused by Cadence and Matlab (in order to save hard drive space). A high data resolution is required in order to achieve accurate simulation results.

5 Conclusions, Contributions and Recommendations

In this chapter the work presented in this thesis is summarized. The first section sums up the conclusions from the previous chapters. Next, an overview of the scientific contributions made in this thesis is presented. Finally, a list of recommendations for future work is provided.

5.1 Conclusions

Wireless communication offers the possibility to enhance the functionality of biomedical implantable devices. In previous work conducted by Mark Stoopman, sub-GHz UWB biomedical communication was proposed and investigated [1]. From this research a wireless transceiver system was established and a transmitter consisting of a UWB pulse generator was designed. Unfortunately the design of a receiver was not completed due to time constraints. For this reason a suitable receiver is to be designed in order to complete the transceiver system. While in [1] it was assumed only the transmitter would be implemented in an implantable device, focus was also put on the concept of having the complete transceiver system in implantable devices. Therefore, the requirements that come with implantable devices (low power, small size) needed to be taken into account for the receiver end.

Specifications of the communication link under consideration were researched. The transmitted signal consists of Gaussian shaped pulses, 6 ns wide, that have a pulse repetition frequency of 1 MHz (1 pulse every 1 μ s). The signal covers the frequency band from 500 MHz to 1 GHz. It was also established in [1] that the pulse shape of the transmitted signal can be predicted when it reaches the antenna on the receiver end. This advantage could be taken into account when choosing a suitable receiver architecture.

Several negative influences on the communication link were established. These influences are noise, narrowband and multipath interference. Investigating these interferences is useful in designing a robust receiver. Models that replicate these interferences have been defined and created in order to test the designed receiver during the simulation process. A list of existing narrowband signals over the frequency band was specified, and research was performed on the aspects of multipath propagation in order to create a suitable model.

A number of UWB receiver topologies were researched and compared with each other (in terms of performances): the rake receiver, energy detector and the autocorrelation receiver. Finally the correlation receiver was chosen as the most suitable receiver for wireless biomedical communication. It offers a simple design (in structure), and given the advantage of having a good prediction on the pulse shape of the transmitted signal, the aforementioned UWB pulse generator can also be used for the receiver.

The correlation scheme was thoroughly analysed, and from this specifications on signal modification and synchronisation were established. For instance, differentiation/integration on the signal waveform (caused by the antennas) will have negative results on the performance of the receiver. Extra information is given in Appendix A on the behaviour of antennas on signals. For pulse

synchronisation, it was concluded that a maximum timing deviation between pulses of ± 0.15 ns is allowed for the correlation receiver to maintain 75% or better in terms of performance. The latter specification is particularly important when a pulse synchronisation scheme is designed.

A system level design of a correlation receiver was presented. Its main operating blocks are a multiplier and an integrator. The inputs of the multiplier are the received signal from the antenna (which is amplified by a low noise amplifier and passes through a 500 MHz to 1 GHz band pass filter), and the locally generated signal (which is the UWB pulse generator).

A test environment in Matlab was presented in order to test the correlation receiver, and compare its performance with other receivers. The test environment includes the aforementioned interference models, which are to test the receivers for their robustness against these negative influences. The correlation receiver structure is implemented in the test environment, along with an energy detector and a quadrature downconversion autocorrelation receiver. The latter two receivers are added for comparison. Also, two receivers that combine the correlation scheme with the transmitted reference or the energy detector scheme are introduced and implemented in the test environment. These are to test if extra signal processing besides correlation is necessary in order to improve performance.

Finally, the simulations from the test environment concluded that the correlation receiver is more robust against the three interference models than the other receiver architectures. It was also observed that no extra signal processing besides correlation is necessary. It was also tested whether an analog multiplier is necessary, or a mixer (using a ternary signal, which mimics the frequency of the original transmitted signal, as reference) is suitable. Simulations results showed that an analog multiplier gives better performance than a mixer.

A low-power, MOS-only, four quadrant multiplier with a bandwidth of 1 GHz was designed using the 0.18 μm High-Voltage CMOS technology from AustriaMicroSystems (AMS). Its structure is based on the transistor operating in the strong inversion saturation region, as transistors can achieve higher bandwidths when operating in this region. The structure was chosen from a number of multiplier designs for its low power operation and small number of components. Adjustments were made to the design in order to achieve 1 GHz bandwidth, and all passive components were replaced with MOS transistors to save chip area.

The multiplier circuit's performance was tested using Cadence RF Spectre simulations. These simulations showed that the multiplier operates over a bandwidth of 1 GHz, consumes little power (the average power consumption is 153.2 μW from a 1.2 V supply) and contributes little noise (0.67 mV) compared to the signal amplitude. The multiplier performs poorly in terms of linearity, but it was established that linearity is not a major requirement for the correlation receiver. Simulations also showed that the multiplier circuit is robust over process corners and device mismatch runs, temperature variations and supply voltage variations. It should however be noted that its robustness against supply voltage variations is dependent on the biasing of the transistors. A tuneable biasing control circuit which can respond to these supply voltage variations is recommended in order to increase the robustness of the multiplier against said supply variations.

Finally, the multiplier circuit from the Cadence environment was embedded into the test environment from Matlab. This way the correlation receiver is tested with the multiplier circuit against an ideal multiplier. Simulations showed that the results from the multiplier circuit are identical to the results from an ideal multiplier, which concludes that the designed multiplier is suitable for the correlation receiver.

5.2 Contributions

Below is a list of the scientific contributions in this thesis, along with a short summary:

- *Fundamental research on negative influences (in terms of signal processing) on a wireless communication link*

Several negative influences that may occur on a wireless communication link were researched and subsequently specified. These influences are:

- Narrowband interference, caused by other wireless devices that make use of narrowband communication
- Noise interference, also known as “white noise”
- Multipath interference, which is the distortion of a signal caused by that same signal taking different paths to reach the receiving antenna

After defining these specific influences, simulation models that replicate them were created in order to test receiver architectures on their robustness against these negative influences. These models are used in a test environment in Matlab (further discussed below).

- *The design of a correlation receiver suitable for UWB, sub-GHz biomedical communication purposes*

An UWB receiver based on the correlation scheme was designed on system level. Several (UWB) receiver architectures were examined, of which the correlation receiver was deemed the most suitable for UWB, sub-GHz biomedical communication. During the design process of the receiver, attention was given to not having to perform adjustments on the (already designed) UWB transmitter [1]. The receiver is suitable for either Binary Phase-Shift Keying or On-Off Keying and consists of a low number of system blocks. After several simulations performed in a test environment in Matlab (further discussed below), the correlation receiver displayed good performance compared to other receiver architectures. Also, a clear specification on pulse synchronisation was established (Subsection 2.4.1 on Page 17) in order for the correlation receiver to operate as optimal as possible.

- *The build-up of a testing environment for (UWB) receivers in Matlab*

A test environment in Matlab was created in order to fully test the designed correlation receiver and compare its performance with other receiver architectures. The test environment consists of input signal generators, the aforementioned negative influence (or interference) models, several receiver architectures and a subsequent pulse detecting and counting scheme. The advantage of such a test environment is that all implemented receivers are tested on an equal level for accurate and unbiased comparison. It should be noted that the test environment relies on high signal waveform resolution.

- *The design of a robust, low power, MOS-only, four-quadrant, 1 GHz multiplier circuit*

A four-quadrant multiplier based on [32] was designed for the correlation receiver. This type of multiplier architecture was chosen from a list of designs (Table 3.1 on Page 40) for its low power performance and for having a comparatively low number of components. The design was adjusted in order for the multiplier to fulfill the 1 GHz bandwidth requirement while still consuming little power (average power consumption is 153.2 μ W, with a 1.2 V supply). Its drawback is its poor linearity, however, this is not an important specification for the correlation receiver. Also, the passive components of the original design were replaced with MOS transistors in order to save area on a single chip. After several simulations, the multiplier proved to be suitable for the correlation receiver, while also being robust over process variations, device mismatch and temperature. It is also robust over supply voltage variations, under the condition that the biasing of the transistors remains stable.

5.3 Recommendations

Since some topics have been left open in this work, below is a list of some recommendations for future work.

- *Pulse Synchronisation Scheme*

During the design process of the correlation receiver, it was assumed that the received signal from the antenna and the locally generated signal are fully synchronised before the correlation process. However in this work, specifically Section 2.4, it was discussed that pulse synchronisation is an important part of the correlation receiver and therefore should also be designed and implemented. In Subsection 2.4.1 the correlation scheme was researched and from this the maximum allowed deviation over time (between pulses) was specified (± 0.15 ns, or consequently 5% of the total pulse width). Two possible pulse synchronisation schemes are briefly discussed in Subsection 2.4.3, and may be useful for the receiver but this has not yet been determined.

- *Further implementation of the correlation receiver at a circuit level*

So far only the multiplier block of the correlation receiver (displayed in Figure 2.13 on Page 21) has been realised at a circuit level. The following blocks of the receiver still need to be designed on circuit level: a low noise amplifier, a 500 MHz to 1 GHz band pass filter, a low pass filter with its f_{-3dB} frequency at 500 MHz and an integrator. The local signal/pulse generator was already designed [1]. Several specifications that were taken into account when the multiplier was designed (such as low power operation, low complexity and small size on chip) also need to be taken into account when designing the other system blocks of the receiver.

- *Circuit Design of accommodating subsystems*

Besides the system blocks of the correlation receiver, other circuit subsystems are required for the correlation receiver. The need for these subsystems were established during the circuit design process of the multiplier. These subsystems are:

-Turn off/on circuit: the multiplier circuit is now designed such that it continuously consumes power, even when there is no definite signal on its inputs. Considering the transmitter sends a 6 ns wide pulse every 1 μ s, the multiplier unnecessarily consumes power every 994 ns. The power consumption of the multiplier circuit can be reduced by introducing a subsystem that switches the multiplier off during the 994 ns when there is no signal present. This type of subsystem should also be compatible with the other system blocks of the correlation receiver.

-Biasing circuit: as previously discussed in Subsection 4.2.4 on Page 64, the multiplier circuit is robust over supply voltage variations as long as its MOS transistors remain properly biased over these variations. A subsystem that controls the necessary biasing voltages needs to be designed. It is required that this biasing circuit is able to respond to supply voltage variations and subsequently varies the biasing voltages if necessary.

A Antennas

This appendix discusses the research that was done on antennas. Influences that the antenna has on the shape of a transmitted and/or received pulse are discussed. This research is mainly used for designing a UWB receiver on a system level.

A known principle in antenna theory is the influence of the antennas used on the communication channel. The term “influence” means changes in the signal/pulse shape when it is transmitted and/or received by an antenna. This phenomenon is an issue in communication technology though most transceivers can operate despite this behaviour: even though the shape of the signal changes, the signal itself (i.e. the information) is still present. However, for the Correlation receiver described in this thesis the pulse shape is a critical factor in its operation. As has been concluded in Section 2.4.1, signal modifications caused by differentiation and/or integration can cause a minimal or zero result at the output. Better understanding of antenna theory helps in the estimation of the received signal.

The antenna effect on signal pulse shapes has been published both theoretically as well as experimentally. Both approaches are discussed here.

Note that there are several types of antennas suitable for UWB communication, each with different characteristics. In this case, the *electrically small antenna* will be used as a primary example since these are suitable for medical implants. Electrically small antennas are characterized by being much smaller than the wavelength of the signal. They also exhibit very low directivity⁷, low input resistance and high input reactance. Examples are the short dipole and small loop.

Figure A.1, shows a diagram of a pair of two identical antennas [41]. In this example the antennas are aligned so that there are no polarization losses and that the transfer gain is maximum.

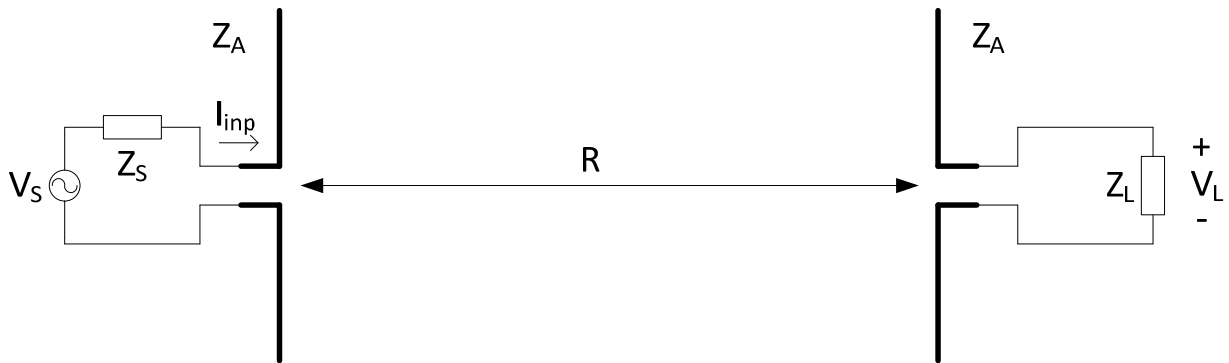


Figure A.1: Diagram of a pair of antennas aligned according to the maximum transmit direction and minimum polarization losses.

⁷ Directivity describes the ratio of the radiation intensity in a given direction from the antenna to the radiation intensity averaged over all directions. Isotropic antennas do not exist in practice; therefore it radiates and receives more effectively in some directions than in others.

In Figure A.1, V_S is the antenna input voltage with source impedance Z_S , I_{inp} is the current through the antenna input terminals, R is the radial distance between the sending and receiving antennas, Z_L is the load impedance connected to the receiving antenna and V_L is the measured voltage over this impedance. Z_A is the impedance of the antenna and is modelled as $Z_A = R_A + jX_A$. Note that this impedance is equal irrespective of whether the antenna is in receiving or transmitting mode, as stated by the reciprocity theorem [42]. This impedance is dependent on frequency, antenna shape and surrounding environment. The sign of the input reactance depends on the near field predominance of the field type: electric (capacitive) or magnetic (inductive). As previously mentioned for the input resistance and reactance for electrically small antennas it holds: $R_A < X_A$.

Assuming the antennas from Figure A.1 are infinitesimal dipoles, the link voltage transfer function, $H(\omega)$, is given by:

$$H(\omega) = \frac{V_L(\omega)}{V_S(\omega)} = -j \cdot Z_0 \cdot \frac{\omega}{c} \cdot \frac{e^{-j\beta \cdot R}}{4 \cdot \pi \cdot R} \cdot \left(\frac{l}{2}\right)^2 \cdot \frac{Z_L}{(Z_A + Z_S) \cdot (Z_A + Z_L)} \quad (\text{A.1})$$

where Z_0 is the free space impedance, $\beta = \omega/c$ is the wave number and l is the length of the antenna. Assuming that the source and load impedances are purely resistive, equal to R_S and larger than the antenna resistance, and Z_A is capacitive (C_A), the transfer function has three zeros and two poles:

$$z_{1,2,3} = 0; p_{1,2} = \frac{-1}{C_A \cdot R_S} \quad (\text{A.2})$$

Having poles in the transfer function causes phase shifting. According to [41] this has the following implications onto the shape of the received pulse: if the signal power is mainly located at frequencies well below $p_{1,2}/2\pi$, the received signal shape would be (close to) the third derivative of the transmitted pulse. These three derivatives can also be explained when observing the energy transfer from the source to the load in Figure A.1:

- The transmitting antenna current is the first derivative of the input voltage because the antenna impedance is essentially capacitive.
- The radiated electrical field is the derivative of the antenna current.
- The voltage across the load impedance is the derivative of the receiving antenna open circuit voltage, because the antenna impedance is essentially capacitive.

While the above example explains the antenna effect mainly from a theoretical approach, the following example is derived from an article that presents the antenna effect both theoretically and experimentally [43]. In this case several types of antennas are used in both transmission and reception, where the change in pulse shape is measured and documented. These results are shown in Table A.1 on the next page, where the antenna effect (differentiation, integration or no effect) is displayed. The corresponding legend is written below the table.

Table A.1: Relationship between input and received pulse for various antennas

Transmitting Antennas	Receiving Antennas				
	RDH	VVD	TEM	DSC	BCN
RDH	Diff.	Diff.	Diff.	Diff.	Same
VVD	Diff.	Diff.	Diff.	Diff.	Same
TEM	Diff.	Diff.	Diff.	Diff.	Same
DSC	Diff.	Diff.	Diff.	Diff.	Same
BCN	Same	Same	Same	Same	Int.

Legend

RDH = Ridged-Horn Antenna Diff. = Received Signal is the differentiation of input signal
VVD = Vivaldi Antenna Same = Received Signal is the same as input signal
TEM = TEM-Horn Antenna Int. = Received Signal is the integration of input signal
DSC = Disc-Cone Antenna
BCN = Biconical Antenna

A notable difference between the first (theoretical) and second (experimental) article is that the first article concludes three derivatives on the received signal, while the second article only presents one derivative on the signal. A possible explanation is that the second article does not include electrically small antennas in its analysis. Unlike the small antennas, the antennas used in the article do not have an input reactance greater than its input resistance. The first article concludes that this reactance is the cause for the derivation of the signal, hence the different results in the second article. Also, the second article compares the pulse shapes by observation. Since it is difficult to distinguish first and third derivatives (with other interferences added to the measured signal), the possibility of the third derivative could be overlooked. Still, despite this the article does show clear examples of change in UWB pulse shapes in real experiments.

B Matlab/Simulink designs

This appendix displays the complete simulation model as it is designed in Matlab/Simulink. All details of the model are added to give the reader the opportunity to fully replicate it. This appendix starts with the top system level and gradually discusses all individual subsystems. All figures shown here are directly copied from the Simulink models. Comments on some systems, as well as implemented values and parameters are also listed here.

The top system level of the total simulation model is shown in Figure B.1.

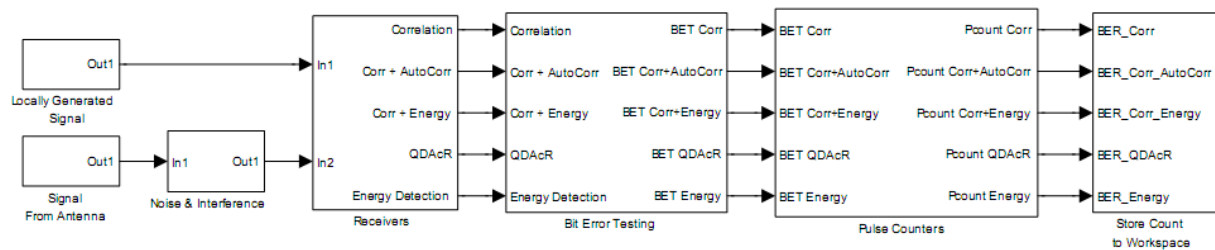


Figure B.1: Top system level of total Simulation model

The subsystems, or blocks, that the simulation model consists of are:

- The two input signals: the *locally generated signal* and the *received signal from the antenna*
- The *Noise & Interference* block
- The *Receivers* block
- The *Bit Error Testing* block
- The *Pulse Counters* block
- The block that stores all incoming data to a file, *Store Count to Workspace*

All these subsystems are discussed in the following sections.

B.1 Input Signals

The models that generate the two different input signals are shown in Figure B.2, on the next page. Figure B.2a shows the model that generates the Gaussian pulse, from the designed pulse generator [1]. This particular signal was previously shown in Figure 2.2a and Figure 2.18a. The model shown in Figure B.2b generates the received signal from the antenna, previously shown in Figure 2.1 and Figure 2.18b. These signals are generated from tables that contain their data. Below is a list of the values that are implemented in each block.

Locally Generated Signal

Pulse Generator: 9.995002499 psec, with a 18.73 ns delay

Pulse Generator2: 50 nsec, 39.99% pulse width and a 18.73 ns delay

“Current” = table of 2001 values for antenna current

Received Signal From Antenna

Pulse Generator3: 50 psec, with a 20 psec delay

Pulse Generator4: 50 nsec, with 29.9% pulse width and a 22.77 ns delay

“GaussianSignal2” = table of 299 values for received signal

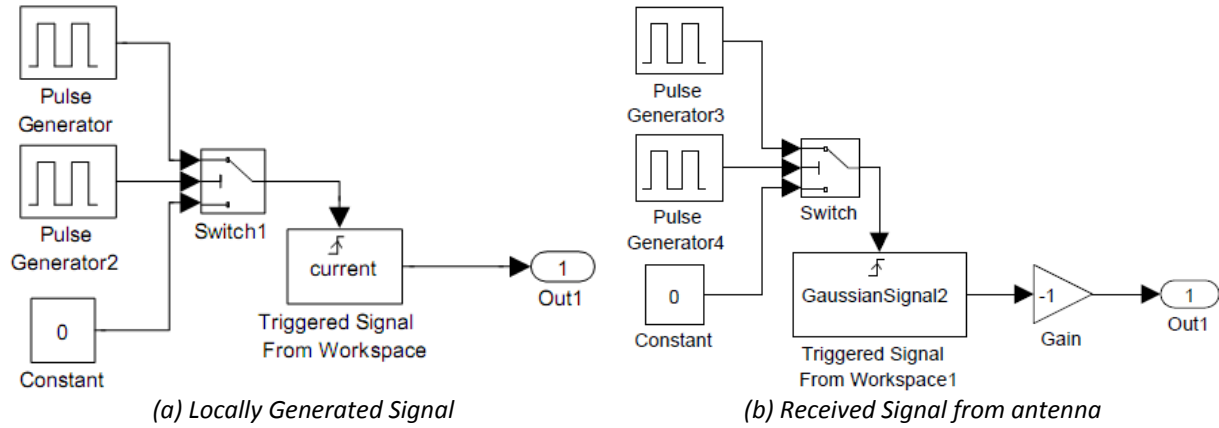


Figure B.2: Input signal generators for the receiver blocks

B.2 Noise & Interference

The contents of the *Noise & Interference* subsystem are shown in Figure B.3.

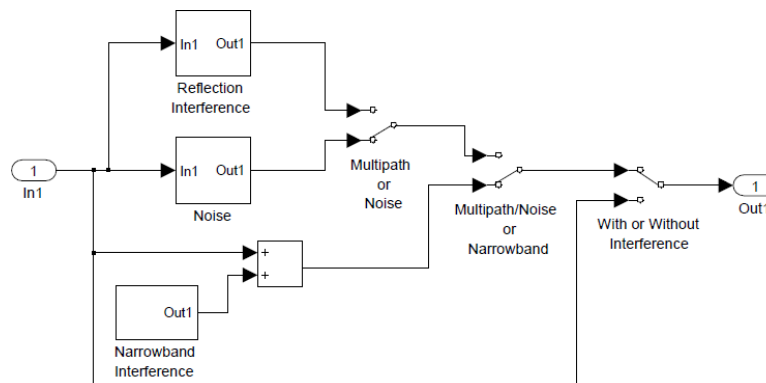


Figure B.3: Contents of Noise & Interference subsystem

The system shown in Figure B.3 consists of three different subsystems, which are the three negative influences on a communication link previously discussed in Section 2.2. These subsystems are noise, narrowband interference and reflection (multipath) interference. Several switches are added to turn on/off any of these subsystems. Each subsystem is explained in the following subsections.

B.2.1 Noise

The noise model is shown in Figure B.4 on the next page. The *AWGN Channel* block adds noise to the communication channel. The *Continuous RMS* block measures the added noise and, once the simulation is completed, writes this value to a file.

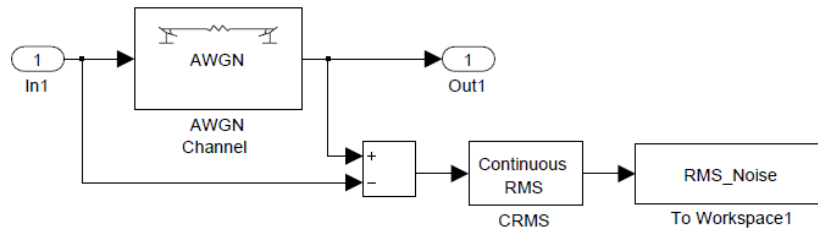


Figure B.4: Noise model

B.2.2 Narrowband Interference

The narrowband interference model is shown in Figure B.5.

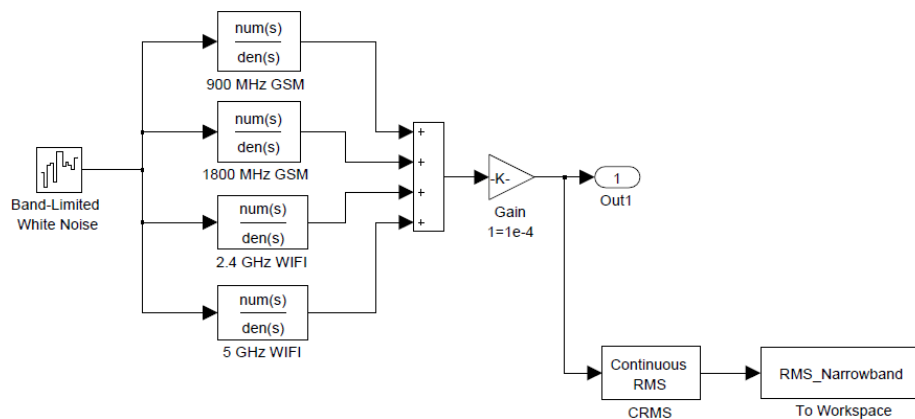


Figure B.5: Narrowband interference model

In Figure B.5, the *Band-Limited White Noise* block generates random noise over the frequency spectrum (which can be specified by the used). The subsequent Band-Pass Filters take out specific frequencies corresponding to narrowband signals, which are then added up. The *Gain* block adjusts the amount of narrowband interference. The *Continuous RMS* block measures the generated narrowband interference and, once the simulation is completed, writes this value to a file.

Band-Limited White Noise: 100 psec sample time

Band Pass Filters displayed are set to 900 MHz, 1800 MHz, 2.4 GHz and 5 GHz.

B.2.3 Reflection/Multipath Interference

The model for, a one loop, reflection interference (previously discussed on page 24) is shown in Figure B.6. The values implemented in the *Delay* and *Gain* blocks are dependent on the number of loops of the model, which is explained in detail on page 24 and examples given on page 31.

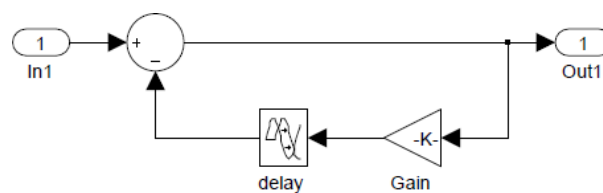


Figure B.6: One loop example of reflection/multipath interference model

B.3 Receivers

The contents of the *Receivers* subsystem from Figure B.1 is shown below in Figure B.7.

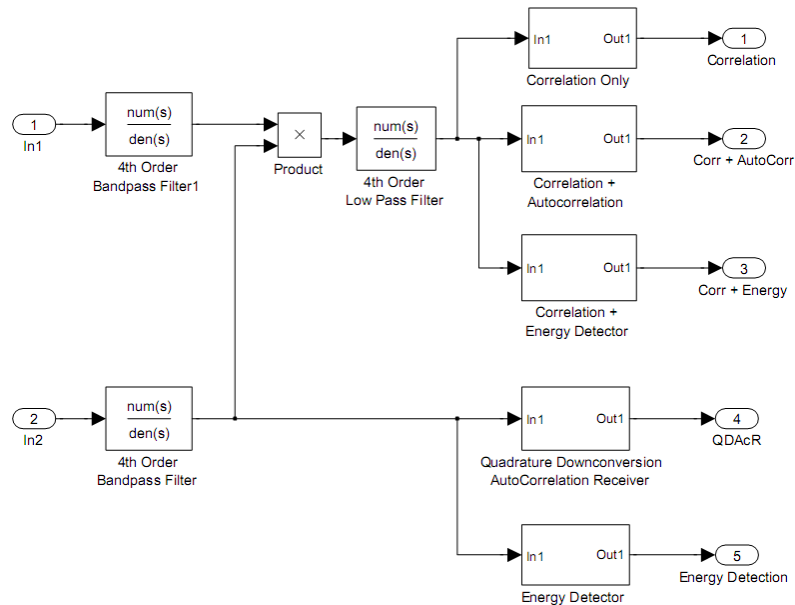


Figure B.7: Contents of Receivers subsystem. Note the five subsystems to the right of each receiver

The incoming signals, from Section B.1, are first filtered by Band Pass Filters. The multiplier (*Product* block) is part of the correlation receiver, as it multiplies both incoming signals with each other. This only happens for three of the five receiver subsystems, as the QDAcR and Energy Detector don't operate with this multiplication. The five subsystems are further discussed in the following subsections.

4th Order Band Pass Filters: 750 MHz center frequency

4th Order Low Pass Filter: 500 MHz

B.3.1 Correlation Only

The subsystem of the correlation receiver is shown in Figure B.8. It only contains an integrator, as multiplication is already performed outside the subsystem.

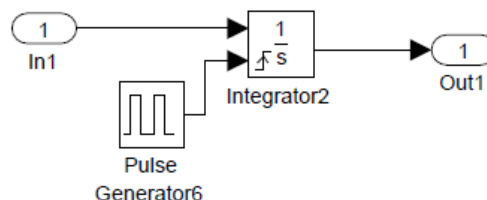


Figure B.8: Subsystem of correlation receiver

Pulse Generator6: 10 nsec, with 5 nsec delay

B.3.2 Correlation + AutoCorrelation

Figure B.9 shows the subsystem of the autocorrelation (transmitted reference) receiver after correlation.

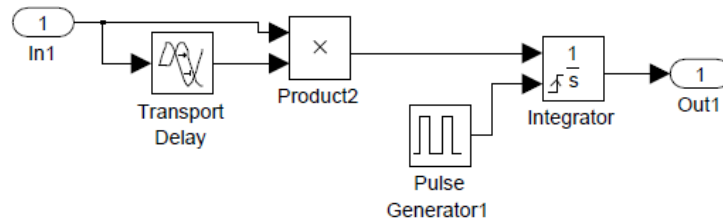


Figure B.9: Subsystem of autocorrelation (transmitted reference) receiver after correlation

Transport Delay: 50 nsec

Pulse Generator1: 10 nsec, with 5 nsec delay

B.3.3 Correlation + Energy Detection

Figure B.10 shows the subsystem of the energy detector after correlation.

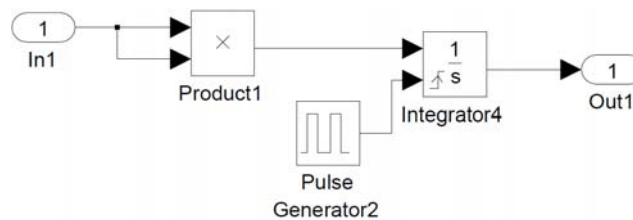


Figure B.10: Subsystem of energy detector after correlation

Pulse Generator2: 10 nsec, with 5 nsec delay

B.3.4 Energy Detector

Figure B.11 shows the subsystem of the energy detector.

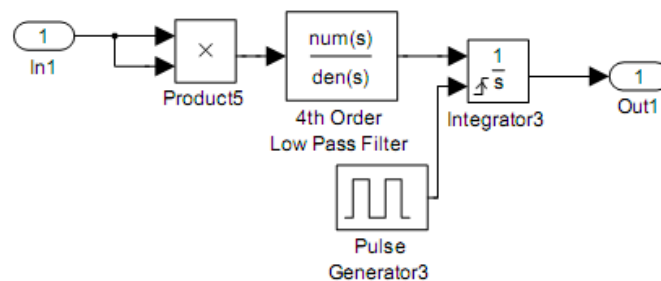


Figure B.11: Subsystem of energy detector

Pulse Generator3: period of 10 nsec, with 5 nsec delay

4th Order low pass filter: 500 MHz

B.3.5 Quadrature Downconversion AutoCorrelation Detector

Figure B.12 shows the subsystem of the QDAcR.

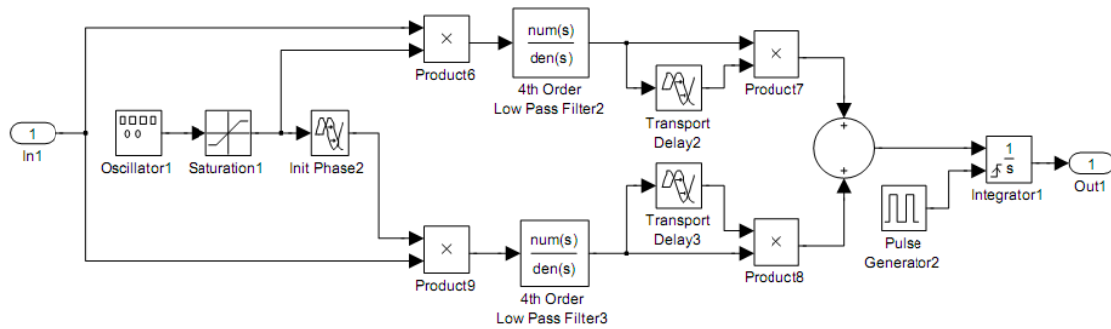


Figure B.12: Subsystem of QDAcR

Pulse Generator2: 10 nsec, with 7.5 nsec delay

Oscillator1: frequency 20 MHz x 37 (=740 MHz)

Init Phase2: quarter of timing of the frequency set in Oscillator1 (1/740 MHz)

4th Order Low Pass Filters: 200 MHz

Transport Delays: 50 nsec

B.4 Bit Error Testing

The contents of the *Bit Error Testing* subsystem of Figure B.1 are shown in Figure B.13. The blocks shown here are subsystems, each containing a model that tests the incoming bits (pulses) of the receivers. Each of these models is essentially the same, so the next subsection only shows one example of this model (of the *correlation only* subsystem).

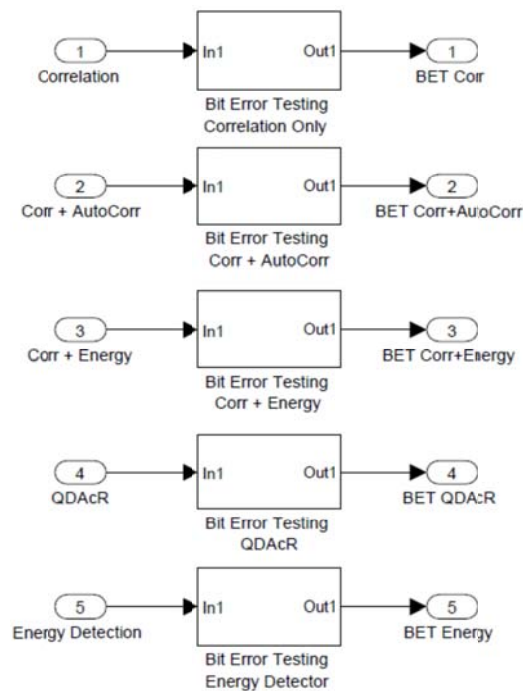


Figure B.13: Contents of Bit Error Testing subsystem

B.4.1 Bit Error Testing model, for the correlation receiver

An example of the Bit Error Testing model is shown in Figure B.14, which is the model used for the correlation receiver. Note that this model is used for all five receiver models.

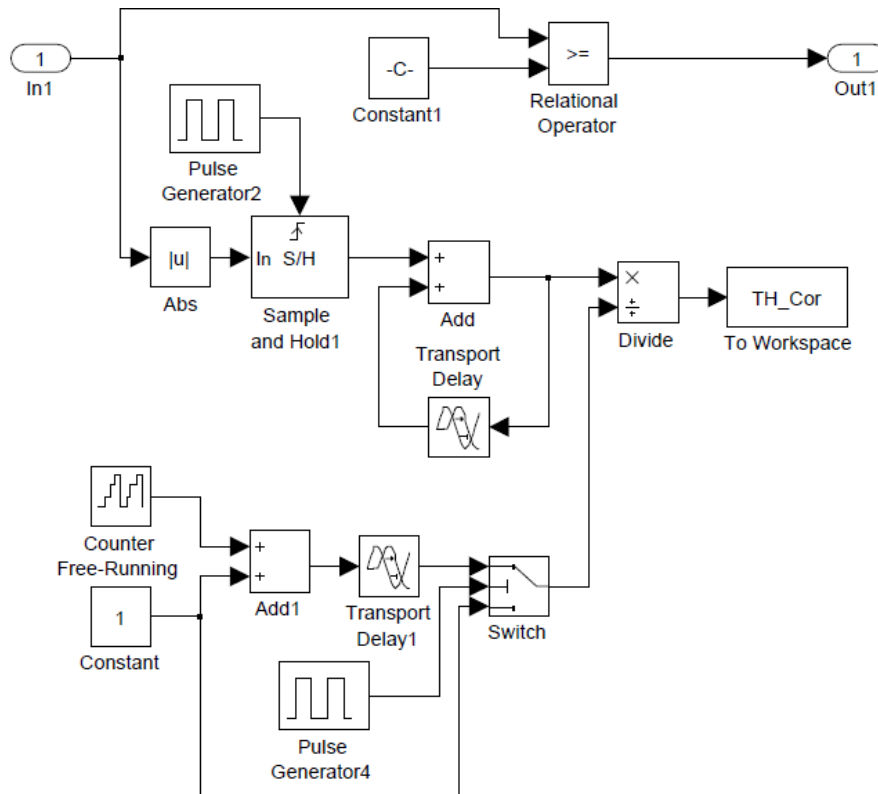


Figure B.14: Bit Error Testing model for the correlation (only) receiver

The incoming pulses (bits) are tested by a specified threshold (given by the *Constant1* block) before being sent to the next subsystem (the Pulse Counter). This specific threshold is determined by the previous simulation, where the amplitudes of all pulses are gradually added up (by the *Sample and Hold1* and *Add* blocks) and then divided by the total number of pulses that have elapsed (this total number is given by the *Free-Running Counter* block). This gives a value for the average amplitude of each pulse, which is then stored to a data file (*TH_Cor* in this case) and used for the next simulation in the *Constant1* block. This explains why for every adjustment to the *Noise & Interference* subsystem, the total system has to be run twice where the first simulation run acts as a reference for the second one. The results of the second simulation run are documented.

Pulse Generator2: 50 nsec, with a phase delay of 34 ns

Constant1: $TH_Cor.signals.values * Threshold$

$Threshold = 0.75$

Transport Delay: 50 nsec

Counter Free-Running: sample time is 50 nsec

Transport Delay1: 30 nsec

Pulse Generator4: period of 1 sec with 99% pulse width and 35 nsec delay

B.5 Pulse Counters

The contents of the *Pulse Counters* subsystem of Figure B.1 are shown in Figure B.15. As shown below, each receiver has its own pulse counter. Also, all pulse counters are essentially identical, with the exception of the pulse counter for the QDAcR, which has its own *Integrator Clk* block.

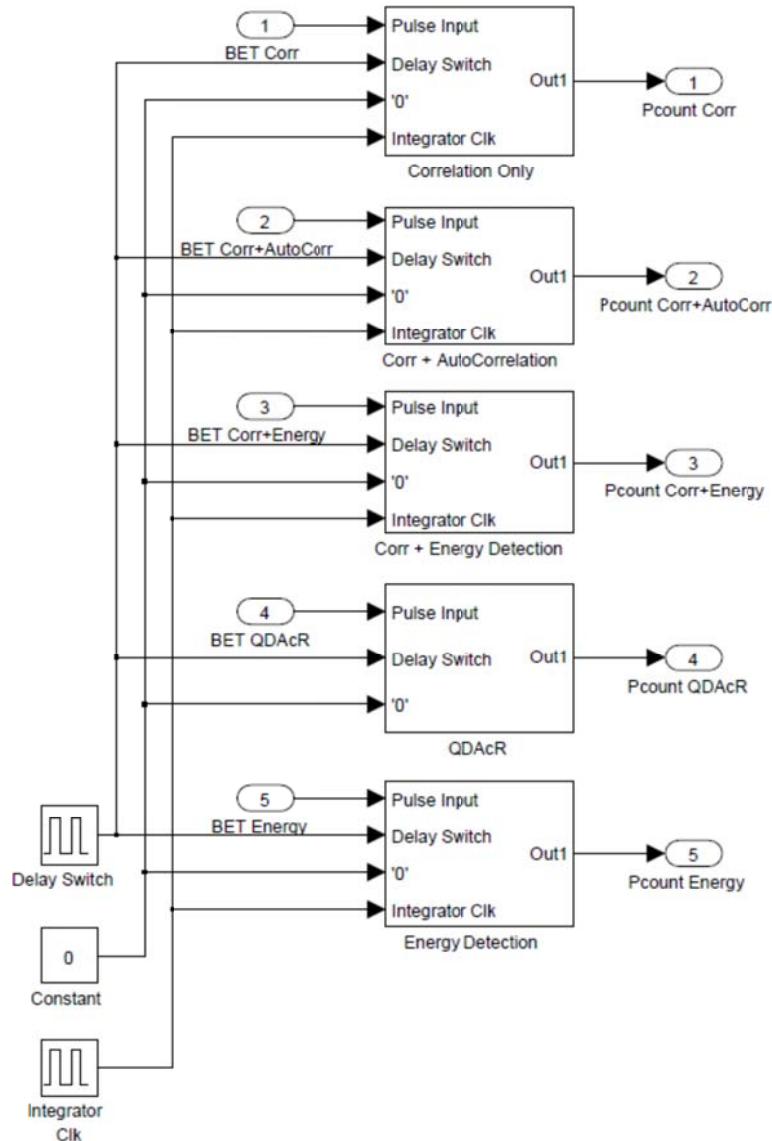


Figure B.15: Contents of Pulse Counting subsystem

As all of these models are essentially the same, the next subsection only shows one example of this model (of the *correlation only* subsystem).

Delay Switch: 10 sec, with a pulse width of 99.9% and a phase delay of 50 nsec

Integrator Clk: 10 nsec, with a delay of 5 nsec

For the QDAcR, the *Integrator Clk* (not shown in Figure B.15) has a 10 nsec period, with a 7.5 nsec delay

B.5.1 Example Pulse Counter, for correlation receiver

An example of the Pulse Counting model is shown in Figure B.16, which is the model used for the correlation receiver. Note that this type of model is used for all five receiver models.

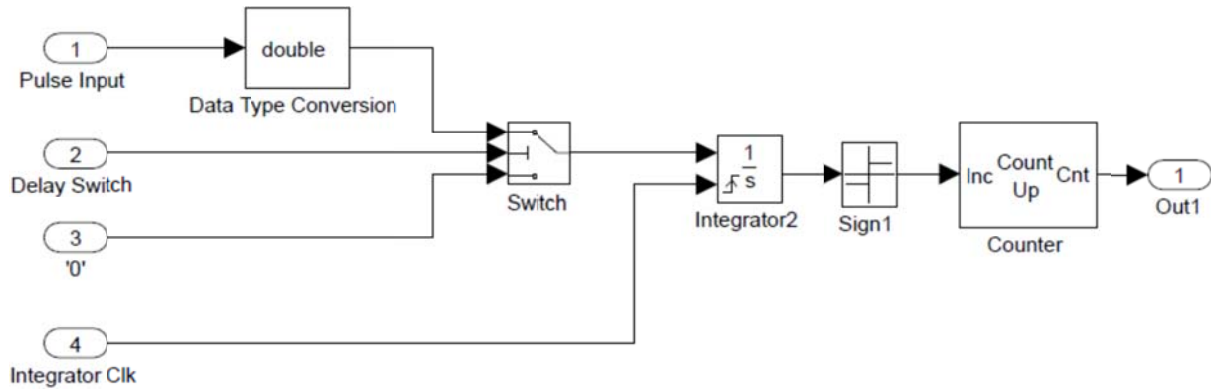


Figure B.16: Pulse Counting model for the correlation (only) receiver

In Figure B.16, the pulses that passed the previous (*Bit Error Testing*) subsystem are once again verified by an integrator. The output of the integrator is an analog signal, so the *Sign1* modifies it to a bipolar signal. This bipolar signal acts as a trigger for the up-counter.

B.6 Store to Workspace

The contents of the *Store Count to Workspace* block in Figure B.1 is shown in Figure B.17. Each block stores the total number of counted pulses to a data file once a simulation is completed.

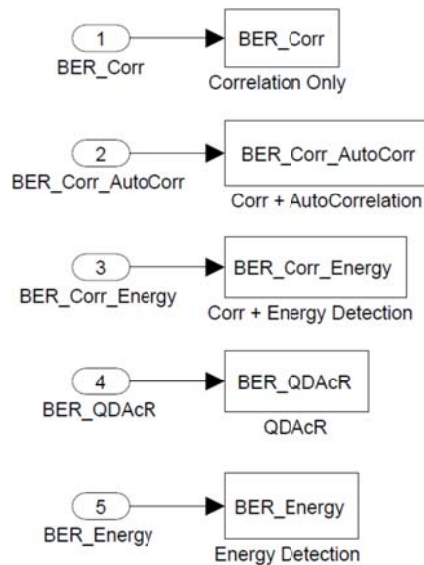


Figure B.17: Function blocks that store the total number of counted pulses after each simulation

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