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Letters

# Carrier-Based Generalized Discontinuous PWM Strategy for Single-Phase Three-Legs Active Power Decoupling Converters

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***Abstract*—Three-legs active power decoupling (APD) converters are widely studied in the single-phase grid-connected systems to enhance the circuit lifetime by creating an alternative path for the typical existing dc-side power pulsating ripple. Therefore, this reduces the requirement of smoothing dc capacitors allowing compact designs even with the implementation of long life metalized film technology. In this article, to allow enhancement of the system power density by improving power conversion efficiency and thus reducing the requirement of thermal management of the semiconductors, a carrier-based generalized discontinuous PWM strategy is proposed. This method detects the converter ac currents and ac reference voltages to determine the optimum clamped duration in each one of the three bridge-legs, which will minimize the converter overall switching losses. The proposed modulation method is analyzed and validated on a PLECS simulation and a 2 kVA single-phase three-legs APD converter.**

***Index Terms*—Active power decoupling (APD), discontinuous pulsewidth modulation (DPWM), single-phase.**

## I. Introduction

THE inherent ripple power in the conventional full-bridge based single-phase ac–dc converter results in an undesirable low-frequency voltage ripple on the dc-link, which can degrade the system performance in terms of ac current distortion, and reliability [1]. To address this significant issue, a single-phase three-legs converter operated with an intrinsic active power decoupling (APD) circuit (c.f. Fig. 1) was proposed in [1]–[4]. This comprises the conventional full-bridge ac–dc converter and an auxiliary bridge-leg offering an alternative path for the dc ripple power to flow through additional energy storage components at the ac side. This enables a considerable reduction on the requirement of smoothing electrolytic capacitors on the dc-link [5]–[8]. This particular concept has attracted considerable attention in recent years because when compared to other APD circuits it has reduced components count, lower semiconductor losses, and less current and voltage stresses on the added storage capacitor $C_{ac}$[7], [8]. However, as for all other APD circuits, the additional auxiliary power decoupling functionality incorporates extra power losses to the ac–dc converter, which will lower the power conversion efficiency when compared to the conventional full-bridge converter.

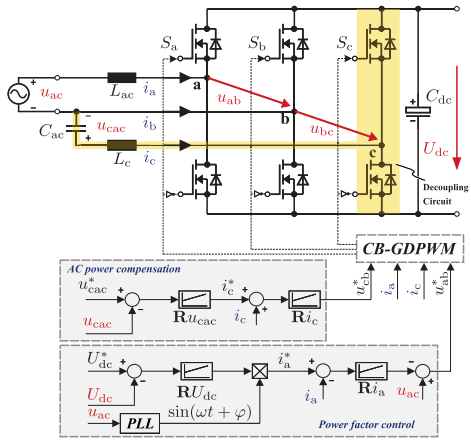


Fig. 1. Three-legs APD converter circuit.

To relieve this problem, this work proposes a carrier-based generalized discontinuous pulsewidth modulation (CB-GDPWM) strategy for the single-phase three-legs APD converter. The topology circuit and its corresponding control scheme [5]–[8] are shown in Fig. 1. The proposed algorithm is able to adjust the clamping interval in which the switches of the bridge-legs stop switching based on the instantaneous value of the phase currents and reference voltages. With such

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a characteristic, the proposed strategy can realize the minimum switching losses action at any instant, thus improving the power efficiency and power density of the system, e.g., by reducing the semiconductor thermal management requirements. It is noted that in the literature available today the modulation strategies studied in the three-legs APD converters are based on the continuous PWM methods, e.g., space-vector PWM (SVPWM) and sinusoidal PWM (SPWM) [5]–[7]. To the best of the authors' knowledge, no literature work has applied discontinuous PWM (DPWM) methods into the single-phase ac–dc converter with APD functionality. Different from the existing DPWM strategies [9]–[12], which are widely studied in balanced and symmetric three-phase three-wire applications, such as in motor drives and grid-tied converters, herein, in a three-legs single-phase ac–dc implementation, the reference voltages seen by each bridge-leg of the system are naturally unbalanced and asymmetrical, and the peak value of the ac current is particularly difficult to predict.

In this article, the proposed CB-GDPWM strategy is studied and compared with the SVPWM [5] and the classical DPWM method, i.e., DPWM1, which is initially proposed for the three-phase balanced system in [9]. The benchmarking is carried out considering power conversion efficiency, dc rms current value, and ac current total harmonic distortion (THD), using both PLECS-based simulation and experiments in a 2 kVA single-phase three-legs APD converter. Herein, to verify the practicability of the proposed method the circuit is operated as a rectifier, processing active and reactive power, and solely processing reactive power in STATCOM mode.

## II. Working Principle of the Proposed Method

The proposed CB-GDPWM is based on the general control structure with power factor control and ac power compensation [5], [6], where the magnitude and phase of of the voltage across the added capacitor $C_{\rm ac}$ ($u^*_{\rm cac}$), as $U_{\rm cac}$ and $\theta_{\rm cac}$, are determined by (1)–(4) [5], so the APD circuit is able to absorb the double-frequency ripple across the dc-bus

$$U_{\rm cac} = \sqrt{P_{\rm ab\_2\omega}\left(\frac{1}{\omega C_{\rm ac}} - \omega L_c\right)} \tag{1}$$

$$\theta_{\rm cac} = 0.5\varphi_{\rm ab} \tag{2}$$

$$P_{\rm ab\_2\omega} = \sqrt{(U_{\rm ac}I_{\rm a})^2 + (\omega L_{\rm ac}I_{\rm a}^2)^2 + 2\omega L_{\rm ac}U_{\rm ac}I_{\rm a}^3\sin\varphi} \tag{3}$$

$$\varphi_{\rm ab} = \arctan\frac{-U_{\rm ac}I_{\rm a}\cos\varphi - \omega L_{\rm ac}I_{\rm a}^2\sin(2\varphi)}{U_{\rm ac}I_{\rm a}\sin\varphi - \omega L_{\rm ac}I_{\rm a}^2\cos(2\varphi)} \tag{4}$$

herein, $U_{\rm ac}$ and $I_{\rm a}$ are the peak value of the grid voltage and current, respectively; $\omega$ is the grid angular frequency; $C_{\rm ac}$ is the ac capacitor used as part of the auxiliary energy storage of the power converter; $L_{\rm ac}$ and $L_c$ are the inductors, which are connected to the phase leg $a$ and $c$; $\varphi$ is the phase angle between $u_{\rm ac}$ and $i_{\rm a}$.

The proposed CB-GDPWM modulator depends not only on the converter reference line-to-line voltages ($u^*_{ab}$ and $u^*_{cb}$), but also on the phase currents passing through the converter ($i_{\rm a}$, $i_{\rm c}$, and $i_{\rm b} = -i_{\rm a} - i_{\rm c}$). First, the converter reference voltages ($u^*_{\rm a}$, $u^*_{\rm b}$, and $u^*_{\rm c}$) can be determined by

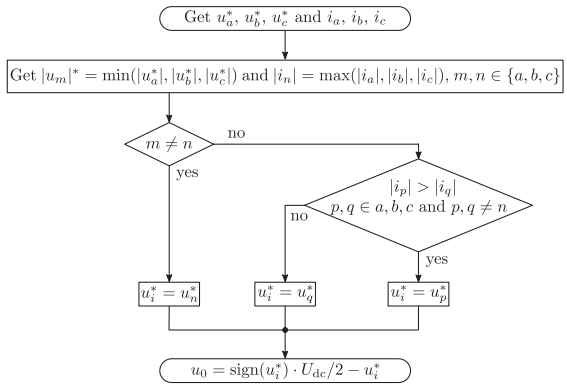


Fig. 2. Flowchart of the proposed CB-GDPWM to decide the zero-sequence signal of the modulation waveform.

$$\begin{cases} u^*_{\rm a} = u^+_{\rm a} + u^-_{\rm a} = \frac{2u^*_{ab} - u^*_{cb}}{3} \\ u^*_{\rm b} = u^+_{\rm b} + u^-_{\rm b} = \frac{-u^*_{ab} - u^*_{cb}}{3} \\ u^*_{\rm c} = u^+_{\rm c} + u^-_{\rm c} = \frac{-u^*_{ab} + 2u^*_{cb}}{3} \end{cases} \tag{5}$$

$$u^*_{\rm a} + u^*_{\rm b} + u^*_{\rm c} = 0 \tag{6}$$

where, $u^+_x$ and $u^-_x$ ($x \in \{a, b, c\}$) are the positive and negative sequence components of each converter reference voltage, respectively. Due to the three-phase three-wire system without zero-sequence component, the relation in (6) is still valid. Thereafter, the zero-sequence signal of the modulation waveform can be determined by

$$u_0 = \text{sign}(u^*_i) \cdot U_{\rm dc}/2 - u^*_i \qquad i \in \{a, b, c\} \tag{7}$$

where, $u^*_i$ is the selected reference voltage to be clamped. The principle of $u^*_i$ selection is illustrated in Fig. 2. If the magnitude of the phase reference voltage with maximum phase current is not lower than the other two phases, this reference voltage is selected as $u^*_i$. Otherwise, one of the other phase reference voltages with larger current magnitude is used. Finally, the modulation waveforms $u^{**}_{\rm a}$, $u^{**}_{\rm b}$, and $u^{**}_{\rm c}$ of the CB-GDPWM method are obtained to be compared with the PWM triangular carriers:

$$u^{**}_x = u^*_x + u_0 \qquad x \in \{a, b, c\}. \tag{8}$$

Fig. 3 shows the simplified illustration of the proposed PWM method in the APD converter operating with different $\varphi$ in rectifier mode. If the instantaneous value of current is lower when the switching device is acting, the switching loss will also be lower [9]. It is indicated that not only the reference voltages, but also the measured converter currents are important to determine the optimal clamped intervals in the CB-GDPWM strategy. If only the voltage references are used to choose the clamping region as the method proposed in [9], i.e., without the information of the converter current, the obtained DPWM strategy can not achieve the performance of minimum switching losses, because the clamped switches are not always matched with the phase-leg with the maximum current [10]. By using only the measured currents, the phase reference with minimum

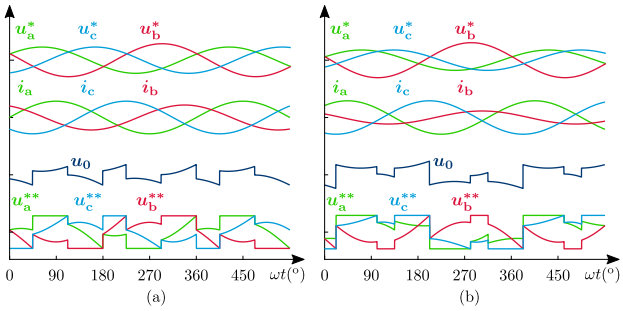


Fig. 3. Simplified illustration of the proposed CB-GDPWM: rectifier mode at (a) $\varphi = 0°$, and (b) $\varphi = 45°$.

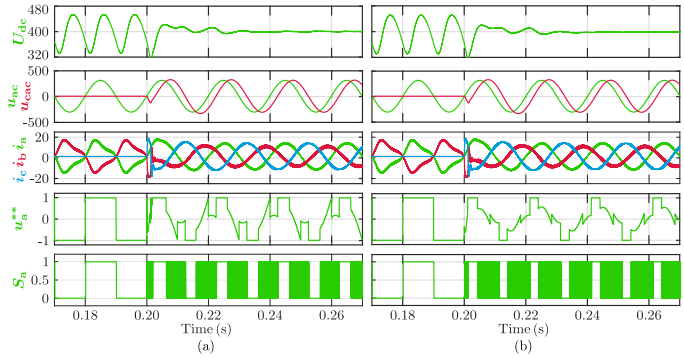


Fig. 4. Simulation results of the transient responses when enabling the APD at $t = 0.2$ s with: (a) CB-GDPWM (b) DPWM1.

voltage magnitude and maximum phase current magnitude can be selected, which will cause the problem of overmodulation in another phase and affect the waveform quality.

Therefore, the clamped interval of the proposed method for each phase can be placed around the highest value of the converter current whose corresponding reference voltage is allowed to be clamped. This will lead to an optimal reduction of the semiconductor switching losses.

## III. Simulation and Experimental Results

To verify the effectiveness of the proposed CB-GDPWM, a PLECS based circuit simulation and a 2 kVA single-phase three-legs power conversion system controlled by the Texas Instruments TMS320F28379D based on the Fig. 1 control diagram is designed. In both simulation and experiments, the rms value of the input grid voltage is 220 $V_{rms}$/50 Hz (purely sinusoidal without distortion); the output dc voltage is 400 V; the switching frequency $f_s$ is set as 40 kHz; SiC MOSFETs from Wolfspeed C3M0120090J [13] are used; the grid side inductance is $L_{ac} = 1.44$ mH and that for the ac capacitor side is $L_c = 1.15$ mH; the dc capacitance is 135 $\mu$F; the ac capacitance is designed to be 130 $\mu$F based on (9), where $U_{cac(max)} = U_{ac} = 220$ V, and $S_{max} = 2$ kVA is the maximum apparent power that the converter is designed to process. Traditional SVPWM and DPWM1 methods are benchmarked in this section, whose zero-sequence signal generation can be found in [5], [8], and [9].

$$C_{ac} = \frac{S_{max}}{\omega U^2_{cac(max)}}. \tag{9}$$

### A. Simulation Results

Fig. 4 shows the simulation results of the transient responses when the APD controller is enabled at $t = 0.2$ s with CB-GDPWM and DPWM1 operating at $\varphi = 0°$. A resistive load of 80 $\Omega$ is connected on the dc side, and the total output power at this moment is 2 kW. It can be seen that the traditional DPWM methods can also be applied into the three-legs APD converter with proper zero-sequence signal injection. However, the position and length of the clamped time of $S_a$ for DPWM1 in Fig. 4(b) are different from that for the CB-GDPWM in Fig. 4(a), because the clamped phase of DPWM1 is only decided by the reference signal with the largest voltage magnitude.

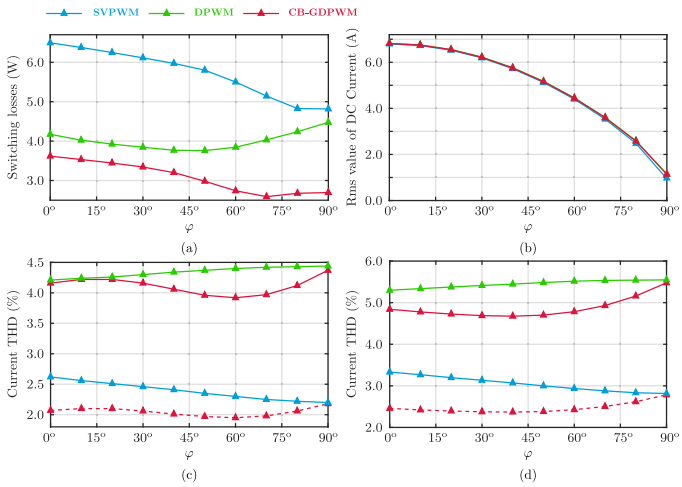


Fig. 5. Performance comparison of (a) switching losses, (b) dc current, (c) current THD for $i_a$, (d) current THD for $i_c$.

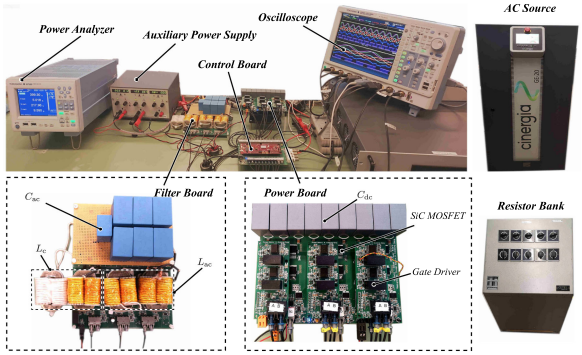


Fig. 6. Experimental setup.

Fig. 5 presents the performance comparison in terms of switching losses, dc current, and ac current THD obtained in the circuit simulation. The apparent power is kept constant by current control loop with the setting up of the grid current rms reference value $i_a$ as 9.09 $A_{rms}$. In Fig. 5(a), the switching energies for turn-ON ($E_{on}$), turn-OFF($E_{off}$) and diode

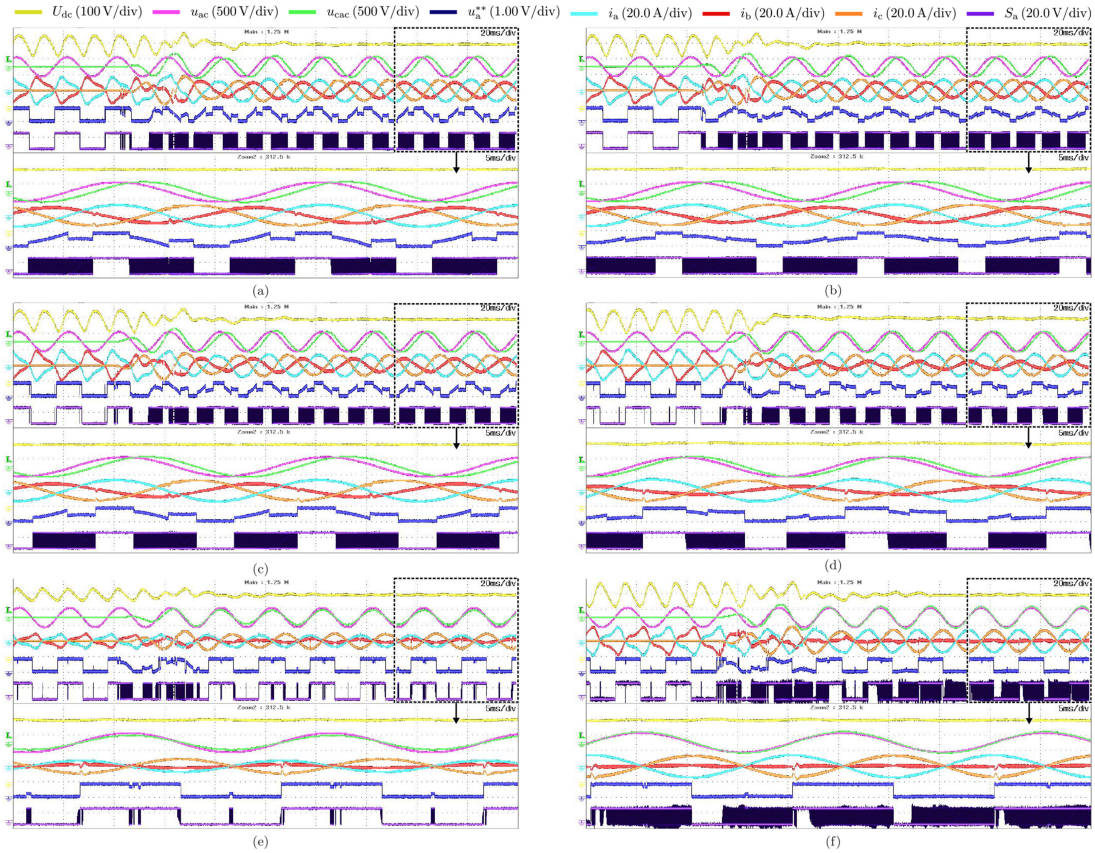


Fig. 7. Experimental results of the APD converter, rectifier mode at $S_o \approx 2\,\mathrm{kVA}$ with (a) CB-GDPWM, $\varphi = 0°$, (b) DPWM1, $\varphi = 0°$, (c) CB-GDPWM, $\varphi = 15°$, (d) CB-GDPWM, $\varphi = 45°$, and STATCOM mode with (e) CB-GDPWM, $I_a = 5\mathrm{A_{rms}}$, (f) CB-GDPWM, $I_a = 10\mathrm{A_{rms}}$. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

reverse-recovery ($E_{rr}$) from the data-sheet [13] are built into the loss model of the switches in the simulation. As expected, the switching losses for CB-GDPWM is lower than that for SVPWM and DPWM1 over all $\varphi$ range. Fig. 5(b) shows the influence of different PWM methods on the dc rms current. It can be seen that the obtained values are almost the same, because DPWM methods do not use another active vectors to replace the zero vectors, hence it results in a low impact on the dc side current ripple [12]. Fig. 5(c) and (d) compares the current THD of $i_a$ and $i_c$, respectively. SVPWM has the lowest current THD value among all PWM methods, while DPWM1 is relatively larger than that for the CB-GDPWM. However, as seen in Fig. 5(a), the CB-GDPWM method is able to reduce nearly 50% of the switching losses in comparison with the SVPWM, which means the $f_s$ of CB-GDPWM can be doubled under equivalent total system switching losses. As a result, the current THD of the circuit implementing the CB-GDPWM with doubled $f_s$ [dotted line in Fig. 5(c) and (d)] becomes lower than that for SVPWM.

## B. Experimental Results

The experimental setup is shown in Fig. 6. The average dc voltage in all experimental cases is controlled at 400 V. Fig. 7 shows the experimental results of the converter with the proposed CB-GDPWM working as rectifier and STATCOM cases with the waveforms before and after the APD circuit is enabled to work with an apparent power of $S_o \approx 2\,\mathrm{kVA}$. Fig. 7(a) and 7(b) are the experimental results for CB-GDPWM and DPWM1 at $\varphi = 0°$ with the restive load of 80 Ω. Fig. 7(c) and (d) are the experimental results for the CB-GDPWM at $\varphi = 15°$ and $\varphi = 45°$, where the resistance of the load is changed to 83 Ω and 113 Ω, respectively, to keep $S_o \approx 2\,\mathrm{kVA}$. Fig. 7(e) and (f) is the experimental results for STATCOM mode with CB-GDPWM, where $\varphi$ is fixed at 90° with two different settings of output currents, $5\,\mathrm{A_{rms}}$ and $10\,\mathrm{A_{rms}}$.

The results in Fig. 7 demonstrate that the average dc voltage in all cases is stable at 400 V. It can be seen that without the APD circuit, the voltage ripple at the dc-link is particularly high with the implemented 135 $\mu$F dc capacitor, which comprises a relatively low value of smoothing dc capacitance. This dc voltage ripple deteriorates the performance of the current control loop and the ac side current becomes distorted. By enabling the APD circuit with the ac power compensation components, the ripple in the dc voltage reduces remarkably and the ac current waveform shape improves as well. Note that the proposed CB-GDPWM method can adapt well to the changes of the set phase angle $\varphi$, and the switching signal $S_a$ is clamped along different intervals with different duration depending on the currents. The APD converter can also work well in the experiment with DPWM1. As predicted in the simulation, the clamped duration time of $S_a$ for DPWM1 in Fig. 7(a) is shorter than that for the proposed CB-GDPWM method, and is not around the peek current of

TABLE I
COMPARISON OF THE MEASURED EXPERIMENTAL RESULTS

| Mode | $\varphi$ | PWM | THD | $\Delta P$ | Efficiency |
|---|---|---|---|---|---|
| Rectifier | 0° | SVPWM | 2.19 % | 62.9 W | 96.9 % |
| | | DPWM1 | 2.92 % | 52.8 W | 97.4 % |
| | | GDPWM | **2.74 %** | **49.7 W** | **97.6 %** |
| | 15° | SVPWM | 2.05 % | 57.2 W | 97.0 % |
| | | DPWM1 | 3.12 % | 48.7 W | 97.5 % |
| | | GDPWM | **2.96 %** | **46.3 W** | **97.6 %** |
| | 45° | SVPWM | 1.95 % | 55.9 W | 96.2 % |
| | | DPWM1 | 3.38 % | 46.1 W | 96.8 % |
| | | GDPWM | **2.52 %** | **44.5 W** | **97.0 %** |
| STATCOM @5 A | 90° | SVPWM | 2.58 % | 32.6 W | - |
| | | DPWM1 | 4.07 % | 27.3 W | - |
| | | GDPWM | **3.94 %** | **25.1 W** | - |
| STATCOM @10 A | 90° | SVPWM | 1.26 % | 57.3 W | - |
| | | DPWM1 | 3.31 % | 53.3 W | - |
| | | GDPWM | **2.96 %** | **45.6 W** | - |

$i_a$. It is noted that with both studied DPWM methods, it exists a small distortion on $i_c$ and $i_b$, because these methods generate low-frequency harmonic components in $u_{cb}$, which can be close to the resonance frequency of the ac storage components, i.e., $L_c$ and $C_{ac}$. This is also found in balanced three-phase three-wire ac–dc converters as shown in [14] and [15]. However, the current distortion in the studied single-phase circuit is confined within the APD circuit and the bridge-leg $b$, as seen in $i_c$ and $i_b$. Therefore, there is no noticeable distortion to the grid side current $i_a$ in all experimental cases, as seen in Fig. 7. All experiments verify the feasibility of the proposed CB-GDPWM working with the APD converter and it proves the adaptive character of the proposed modulator.

Table I shows the power losses and the efficiency of the APD converter working with SVPWM, DPWM1, and the proposed CB-GDPWM for both rectifier and STATCOM modes. The total power losses $\Delta P = P_{in} - P_{out}$, current THD, and the power efficiency are measured by the power analyzer YOKOGAWA WT500. The difference between the real power flowing into the converter and that out of the converter can be regarded as an estimation of the total losses in the converter, including the switching devices and filters. For STATCOM mode, the output active power is zero, thus the measured input active power represents the circuit loss. As shown in Table I, with DPWM methods, the power efficiency of the converter can be improved remarkably compared to the commonly employed SVPWM method, and the proposed CB-GDPWM is able to further reduce the losses and increase the power efficiency in comparison with DPWM1. Moreover, with the implementation of DPWM methods, the current THD will be increased for all cases. Since only the harmonics components below the 50th order are considered in the power analyzer, the measured current THD results are lower than the one obtained from the simulation results in Fig. 5. It can be seen that the current THD for the CB-GDPWM method is generally better than DPWM1, and the difference between CB-GDPWM and SVPWM is relatively small in the experiments. All experimental cases show the reduced power losses with CB-GDPWM based APD converter, which confirms the validity and superiority of the proposed modulation method.

## IV. CONCLUSION

This work was proposed a CB-GDPWM for a single-phase three-legs APD converter. The proposed method was based on the detection of the current position relative to the reference ac voltage. This modulator adaptively clamps the switching device that conducts the largest current whose reference voltage can be clamped at any instant, which leads to the optimum clamped duration to obtain a minimum switching losses. The experimental results not only verified the effectiveness of the proposed method, but also showed its superior performance over the conventional SVPWM and DPWM1 studied in the existing literature.

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