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An Open-Source graphical tool for class E PA design exploration and optimization

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ABSTRACT

This paper presents a novel platform for the efficient analysis, design, and optimization of ideal single-ended Class-E power amplifiers (PAs). It employs a comprehensive time-domain analytical model, which extends the conventional design space by incorporating variable duty cycles, variable voltage switching (VVS), and variable derivative voltage switching (VDS), enabling precise evaluation of key performance parameters such as harmonic efficiency, maximum output power capability, maximum operating frequency, and device stress. To facilitate practical design verification, an open-source, GUI-based CAD tool has been developed, providing researchers with an accessible and interactive environment for analysis and validation. In addition, a Python-based global optimization algorithm is integrated into the framework to automate component selection and enhance design robustness, particularly in scenarios involving finite DC-feed inductance. The accuracy and applicability of the proposed methodology are validated through nonlinear harmonic balance (HB) simulations. The results confirm the model's ability to predict system behavior with high fidelity, making it a valuable resource for both academic and industrial design applications.

1. Introduction

The evolution of power amplifiers (PA) has been driven by continuous innovation aimed at improving efficiency, given their critical role in a wide range of scientific and technological applications. Despite their significance, PAs are characterized by substantial power consumption and inherent non-linearities, leading to increased power dissipation and signal distortion. These challenges have significant implications for energy efficiency, especially in an era increasingly dominated by the Internet of Things (IoT) and the global push for green and sustainable technological solutions [1,2].

Class-E PAs have historically emerged as a promising framework in this context due to their inherent non-overlapping condition between voltage and current waveforms, resulting in 100 % theoretical efficiency [3,4]. Conventional class-E PAs are characterized by two additional conditions: zero voltage switching (ZVS), given by Equation (1), and zero voltage derivative switching, given by Eqs. (2) [5].

$$V(\theta)|_{t=2\pi} = 0 \tag{1}$$

$$\left.\frac{dV(\theta)}{d(\theta)}\right|_{\theta=2\pi} = 0 \tag{2}$$

Early methodologies for Class-E PA synthesis relied primarily on numerical and iterative approaches; since then, however, the design process was considerably streamlined by the introduction of experimentally-validated [6] analytical solutions. These were first reported in 2007 by Acar et al. [7] and were corrected later by Gogoi et al. [8].

Subsequent research has introduced practical considerations, such as variable voltage switching [9], variable derivative switching [10], finite on resistance [11], and load mismatch factors [12]. Mixed approaches combining analytical equations with iterative tuning have also emerged, providing a balance between theoretical rigor and practical applicability [13–15]. Tools such as Maple™ have further facilitated the derivation of circuit parameters under constraints like finite quality factors and voltage limits in VLSI processes [16,17]. Additionally, the rapid use of nonlinear harmonic balance (HB) simulations has been employed to account for practical effects and provide optimized results based on values calculated from the analytical expressions [18]. These simulations offer a powerful means to validate analytical models and refine circuit designs, ensuring alignment with real-world performance requirements.

Despite significant advancements in Class-E PAs design methodologies, a unified analytical framework that seamlessly integrates finite

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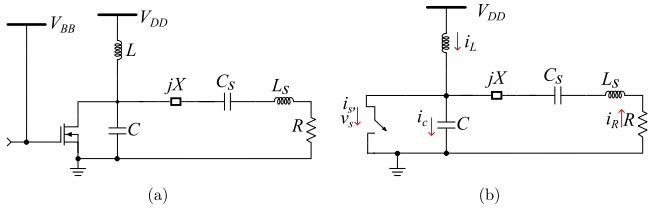


Fig. 1. Class-E PA (a) schematic and, (b) its equivalent circuit.

DC-feed inductance, variable duty cycles, and generalized boundary conditions-while addressing practical trade-offs in harmonic analysis and performance metrics-remains absent in the current literature, to the best of the authors' knowledge. Furthermore, existing studies lack the development of an open-source tool that consolidates all critical design considerations into a single optimization framework, thereby hindering the efficient development of Class-E PA designs.

Most prior works rely on iterative processes and complex curve-fitting functions to assist designers [19]; however, these approaches often struggle to ensure rapid convergence or provide a comprehensive solution. In contrast, this study presents an extended analytical formulation integrated with a GUI-based design tool to support researchers. Additionally, a global optimization technique is employed to determine optimal design parameters based on device stress requirements directly, eliminating the need for tedious iterative processes and enabling a more efficient and systematic design methodology. Furthermore, the analytical values have also been verified through HB simulations, further validating the analytical model and its effectiveness for practical applications.

The rest of the article is organized as follows: Section 2 presents the extended analytical modeling of the proposed Class-E PAs design framework. Section 3 discusses the performance metrics used to evaluate the design, followed by the results and validation of the proposed methodology in Section 4. Finally, the article concludes with a summary of key findings, contributions, and future research directions in Section 5.

2. Analytical modeling of class e PA

The schematic of a Class-E-tuned switched-mode power amplifier with a finite DC feed is shown in Fig. 1(a). The load network consists of a feed inductance L, which supplies current to the transistor. It encompasses a parallel capacitance ($C = C_{dev} + C_{ext}$), that represents the device's inherent capacitance C_{dev}, along with any external capacitance C_{ext}, which ensures the current in and out of the switch-capacitor combination. For simplification, C_{dev} is neglected in this work. The series reactance jX is connected to a series resonant circuit ($L_s - C_s$) with high Q_s that is tuned to the design angular frequency ω_o. This configuration is then connected to the optimal load resistance R. The load current, i_R is given by Eq. (3),

$$i_R(\omega t) = I_R \sin(\omega t + \phi) \tag{3}$$

where ϕ is the initial phase shift and I_R is peak amplitude of the current. A switching duty cycle of d and zero on-resistance of the transistor the generalized boundary conditions are given by Eqs. (4) and (5), with the relation $\omega t = \theta$.

$$\frac{1}{V_{DD}} v_s(\theta)\Big|_{\theta=2\pi} = K \tag{4}$$

$$\frac{1}{V_{DD}} \frac{dv_s(\theta)}{d\theta}\Big|_{\theta=2\pi} = s \tag{5}$$

2.1. Circuit analysis

For the time interval, $0 \le \theta < d\pi$, the switch is closed and the current flowing through the switch can be given by Eq. (6).

$$i_s(t) = i_L(t) + i_R(t) \tag{6}$$

Using the continuity condition, the initial current at the inductor is given by Eq. (7)

$$i_L(0) = -I_R \sin(\phi) + C\omega s \tag{7}$$

The current flowing through the switch can be given by Eq. (8).

$$i_s(\theta) = \begin{cases} \frac{V_{DD}}{\omega L}\theta + I_R[\sin(\theta+\phi) - \sin(\phi)] + C\omega s & 0 \le \theta \le d\pi \\ 0 & d\pi < \theta \le 2\pi \end{cases} \tag{8}$$

When the switch is opened in the interval $d\pi < \theta \le 2\pi$, the current through the switch becomes zero and the current in the capacitor, C can be given by Eq. (9)

$$\begin{aligned} i_C(t) &= i_L(t) + i_R(t) \\ &= \frac{1}{\omega L}\int_{d\pi}^{\theta} \left[V_{DD} - v_s(t)\right] d\theta + i_L(d\pi) + I_R \sin(\theta+\phi). \end{aligned} \tag{9}$$

Using $i_C(t) = C\, dv_s(t)/dt$, Eq. (9) can be transformed into a second-order linear differential equation given by Eq. (10)

$$LC\frac{d^2 v_s(t)}{dt^2} + v_s(t) - V_{DD} - I_R \omega L \cos(\theta+\phi) = 0 \tag{10}$$

The switch voltage can be found by solving the differential equation which has a form given by Eq. (11).

$$v_s(\theta) = \begin{cases} 0 & 0 \le \theta \le d\pi \\ V_{DD}[1 + C_1\cos(q\theta) + C_2\sin(q\theta) - \frac{q^2 p}{1-q^2}\cos(\theta+\phi)] & d\pi < \theta \le 2\pi \end{cases} \tag{11}$$

Here, C_1 and C_2 are arbitrary constants. Without loss of generality, the parameters q and p are defined by Eqs. (12) and (13), respectively. The variable q represents the ratio between the resonance frequency of the parallel $L-C$ network and the operating frequency of the circuit where the series resonator $L_s - C_s$ is tuned. On the other hand, p denotes the ratio of the inductive reactance at the operating frequency to the equivalent resistance seen by the supply voltage V_{DD} and the fundamental current I_R [19].

$$q = \frac{1}{\omega\sqrt{LC}} \tag{12}$$

$$p = \frac{\omega L}{V_{DD}} I_R \tag{13}$$

Using the boundary conditions, given by Eqs. (4) and (5) the constant C_1 and C_2 can be given by Eqs. (14) and (15) ,

$$\begin{aligned} C_1 = V_{DD}\Bigg[&\frac{q^2}{1-q^2} p\cos(\phi)\cos(2\pi q) + \frac{q}{1-q^2} p\sin(\phi)\sin(2\pi q) - \cos(2\pi q)\Bigg] \\ &- \frac{s}{q}\sin(2\pi q) + K\cos(2\pi q), \end{aligned} \tag{14}$$

$$\begin{aligned} C_2 = V_{DD}\Bigg[&\frac{q^2}{1-q^2} p\cos(\phi)\sin(2\pi q) - \frac{q}{1-q^2} p\sin(\phi)\cos(2\pi q) - \sin(2\pi q)\Bigg] \\ &+ \frac{s}{q}\cos(2\pi q) + K\sin(2\pi q). \end{aligned} \tag{15}$$

In this case, p and ϕ are unknown, therefor using the initial condition, The continuity of the capacitor voltage at $\theta = d\pi$, $v_s(d\pi) = 0$, in Eq. (11) gives, Eq. (16)

$$C_1\cos(qd\pi) + C_2\sin(qd\pi) + V_{DD} - \frac{q^2}{1-q^2} pV_{DD}\cos(d\pi+\phi) = 0. \tag{16}$$

Similarly, using the initial condition of shunt inductor current at $\theta = d\pi$

$$\begin{aligned} i_L(d\pi) &= \frac{1}{\omega L}\int_0^{d\pi}\left[V_{DD} - v_S(t)\right]d\theta - I_R\sin(\varphi) + C\omega s \\ &= \frac{V_{DD}d\pi}{\omega L} - \frac{1}{\omega L}\int_0^{d\pi} v_S(t)d\theta - I_R\sin(\varphi) + C\omega s. \end{aligned} \tag{17}$$

Using Eq. (17) in Eq. (9), with $i_C(t) = C\,dv_s(t)/dt$, gives Eq. (18)

$$\begin{aligned} &- C_1 q\sin(qd\pi) + C_2 q\cos(qd\pi) + \frac{q^2}{1-q^2}pV_{DD}\sin(d\pi+\varphi) \\ &- V_{DD}d\pi q^2 + q^2\int_0^{d\pi} v_S(t)d\theta + pV_{DD}q^2[\sin(\varphi) - \sin(d\pi+\varphi)] \\ &- s = 0. \end{aligned} \tag{18}$$

With the given design parameters (q, d, k, s), Eqs. (16) and (18) can be solved numerically, yielding solutions for (p, ϕ). In contrast to previously cited works [16,19], which rely on purely analytical methods, this approach avoids excessive algebraic complexity and reduces the likelihood of mathematical errors.

2.2. Design set

The general design of Class-E PAs involves solving for the circuit parameters under ideal switching conditions. The flexibility in the DC-feed inductor and switch duty cycle, along with the generalized boundary conditions, contributes to the existence of infinitely many solutions. These parameters influence the operation of the amplifier by incorporating variable voltage switching and derivative conditions. Given the values of p and ϕ, the design parameters can be expressed as:

- K_L: The coefficient associated with the DC-feed inductor, L.
- K_C: The coefficient associated with the capacitance C in the circuit.
- K_P: The coefficient related to the power level.
- K_X: A parameter that accounts for the excessive impedance.

These parameters referred as K-Design set that connects the prescribed operating angular frequency ω_o, the desired output power P_{out} and the supply voltage V_{DD} to the values of the circuit components as shown in Fig. 1 The average supply current is given by Eq. (19).

$$\begin{aligned} I_0 &= \frac{1}{2\pi}\int_0^{2\pi} i_S\,d\theta \\ &= I_R\left[\frac{(d\pi)^2}{4\pi p} - \frac{d}{2}\sin(\varphi) - \frac{\cos(d\pi+\varphi)}{2\pi} + \frac{\cos(\varphi)}{2\pi} \right. \\ &\quad \left. + \frac{sd}{2pq^2V_{DD}}\right] \end{aligned} \tag{19}$$

Assuming 100 % efficiency due to the ideal switch, results in Eq. (20)

$$R\frac{I_R^2}{2} = V_{DD}I_0 \tag{20}$$

Using Eq. (19) in Eq. (20), the expression for K_L is given by Eq. (21)

$$K_L = \frac{p}{\left(\frac{d^2\pi}{2p} - d\sin(\varphi) - \frac{1}{\pi}\cos(d\pi+\varphi) + \frac{1}{\pi}\cos(\varphi) + \frac{sd}{q^2pV_{DD}}\right)} \tag{21}$$

The expression for K_C and K_P are then given by Eq. (22) and (23)

$$K_C = \frac{1}{q^2K_L} \tag{22}$$

$$K_P = \frac{p^2}{2K_L^2} \tag{23}$$

Finally, since the values of p and φ are known, the numerical integration of Eqs. (24) and (25) can be performed to find K_X, as given by Eq. (26).

$$V_R = \frac{1}{\pi}\int_0^{\frac{2\pi}{\omega}} v_s(t)\sin(\omega t+\varphi)\,dt \tag{24}$$

$$V_X = \frac{1}{\pi}\int_0^{\frac{2\pi}{\omega}} v_s(t)\cos(\omega t+\varphi)\,dt \tag{25}$$

$$K_X(q,d) = \frac{V_X}{V_R} \tag{26}$$

These coefficients, in turn, determine the circuit parameters R, L, and C, as well as the excessive impedance, as shown in Figure 1

3. Performance metrics for class-E PA

In the design of Class-E PAs, evaluating performance is critical to ensuring device reliability, efficiency, and optimal operation. This section discusses key performance metrics, including harmonic efficiency, η derived from harmonic analysis; device stress ($V_{peak,n}$, $I_{peak,n}$); output power capability, c_p; and normalized maximum operating frequency, f_n. These parameters provide valuable insights into the effectiveness of the design and play a crucial role in assessing trade-offs in practical PAs implementations and making informed decisions.

3.1. Harmonic analysis

The harmonic content of the system is also significant, as it impacts the overall performance and power distribution across different frequency components. The voltage and current waveforms through the switch are expanded into their Fourier series coefficients. The voltage waveform across the switch, $v_{\mathrm{ds}}(\theta)$, can be expressed as:

$$v_{\mathrm{ds}}(\theta) = a_0 + \sum_{n=1}^{m} a_n\cos(n\theta) + \sum_{n=1}^{m} c_n\sin(n\theta) \tag{27}$$

where a_n and c_n are the Fourier coefficients for the cosine and sine terms, respectively, and θ represents the angular position or phase of the switch cycle. Similarly, the current waveform is given by:

$$i_{\mathrm{ds}}(\theta) = b_0 + \sum_{n=1}^{m} b_n\cos(n\theta) + \sum_{n=1}^{m} d_n\sin(n\theta) \tag{28}$$

where b_n and d_n represent the Fourier coefficients for the current harmonics.

Using the complex representations of voltage and current, the output power at each harmonic can be calculated. The voltage and current components at each harmonic are given by:

$$V_n = a_n - jc_n, \quad I_n = b_n - jd_n \tag{29}$$

where j is the imaginary unit. The power at each harmonic is then computed as:

$$P_n = \frac{1}{2}\mathrm{Re}\left[-V_n \cdot I_n^*\right] \tag{30}$$

where I_n^* denotes the complex conjugate of I_n, and P_n is the power at the n-th harmonic [20].

The overall efficiency quantifies an amplifier's ability to concentrate energy at the fundamental frequency while minimizing power dissipation in harmonics. Mathematically, it is defined as the ratio of the fundamental output power, P_1, to the total power, which includes the P_{diss} dissipated power and the sum of powers at all harmonic frequencies, as expressed in Eq. (31) [21].

$$\eta = \frac{P_1}{P_1 + P_{diss} + \sum_{n=2}^{m} P_n} \tag{31}$$

3.2. Device stress and maximum output power

Device stress is a critical parameter that is typically normalized relative to the supply voltage. This normalization serves as an important metric for evaluating the reliability of the device. In particular, the peak voltage ($V_{\text{peak,n}}$) and peak current ($I_{\text{peak,n}}$) across the device may exceed the supply voltage and current, respectively. In this study, the device under consideration is a transistor. If the breakdown voltage of the transistor is lower than the peak voltage, the device may not be suitable for constructing a Class-E PAs.

The maximum output power capability, c_p, is defined as the ratio of the output power P_{out} to the product of the peak voltage, ($V_{\text{peak,n}}$) and current ($I_{\text{peak,n}}$), as given by Eq. (32):

$$c_p = \frac{P_{\text{out}}}{V_{\text{peak,n}} \cdot I_{\text{peak,n}}} \tag{32}$$

where P_{out} is the output power of the system. This provides a means to assess the power output in relation to the stress on the device.

3.3. Maximum operating frequency

In this analysis, the output transistor parasitic capacitance denoted as C_{out}, is assumed to behave linearly for simplicity. Then the shunt capacitance, C, can be replaced by the output parasitic capacitance, C_{out} · The maximum operating frequency $f_{\max}$ of the Class-E PA is an important performance metric and is given by Eq. (33) [22].

$$f_{\max} = \frac{K_C}{2\pi C_{\text{out}} R} \tag{33}$$

where K_C is given by Eq. (22), C_{out} is the output parasitic capacitance, and R is the load resistance.

To compare the frequency $f_{\max}$ under different operating conditions, a frequency ratio f_n is defined by Eq. (34),

$$f_n = \frac{f_{\max}}{f_{\max}(K=0, s=0)} \tag{34}$$

where $f_{\max}(K=0, s=0)$ refers to the maximum frequency when the parameters K and s are set to zero, effectively representing the reference frequency of the system under ideal conditions.

This frequency ratio f_n provides insight into how the inherent frequency of a Class-E PA varies as a function of the parasitic capacitance C_{out}, the load resistance R, and other design parameters. The ability to adjust the frequency ratio optimizes the PA's performance, especially in scenarios where the output power, DC supply voltage, and parasitic capacitance are pre-specified.

4. Results and discussion

In this section, the theoretical model is validated by employing HB analysis, and the performance of the proposed design is evaluated based on the metrics introduced in the previous section. Furthermore, an optimization methodology is described and benchmarked against the same criteria.

4.1. GUI Based design tool

To facilitate researchers in navigating the numerous design variables, an open-source Python-based GUI has been developed. By entering values for s, K, d, and q, users can obtain analytically derived solutions, perform harmonic analysis, and assess key performance metrics. This tool enables rapid design evaluation and verification, streamlining the research process. The algorithm used to develop this tool is presented in Algorithm 1, while Fig. 2 provides a screenshot of the implemented interface.

Algorithm 1 GUI for Generalized Class E Design.

1: **Input:** Given constants $V_{DD}, s, q, d, k, f, P_{out}$, harmonic
2: Compute $\omega = 2\pi f$
3: Define functions $C_1(p,\phi)$ and $C_2(p,\phi)$as given by Eq. 14and15.
4: Define system of equations $f_1(p,\phi)$ and $f_2(p,\phi)$:
5: Initialize guess for (p,ϕ)
6: Solve the system of equations using a numerical solver
7: Select first solution, update p and ϕ
8: Value of K_L K_p K_C are calculated by Eq. (21) (23) and (22)
9: Value of Kx is calculated using numerical integration of Eq. 26
10: Define voltage and current function and normalize them:

$$v_s(\theta) = C_1(p,\phi)\cos(q\theta) + C_2(p,\phi)\sin(q\theta) + V_{DD} - \frac{q^2}{1-q^2} pV_{DD}\cos(\theta+\phi)$$

$$I_s(\theta) = \frac{V_{DD}\theta}{\omega L} + \frac{pV_{DD}}{\omega L}(\sin(\theta+\phi) - \sin\phi) + s\frac{K_C P_{\text{out}}}{K_P V_{DD}^2}$$

11: Calculate the fourier coefficients and use them to reconstruct the voltage and current

$$I \approx \sum_{n=0}^{k}\left(a_{In}\cos(\frac{2\pi nt}{T}) + b_{In}\sin(\frac{2\pi nt}{T})\right),$$

$$V \approx \sum_{n=0}^{k}\left(a_{Vn}\cos(\frac{2\pi nt}{T}) + b_{Vn}\sin(\frac{2\pi nt}{T})\right)$$

12: Calculate η c_p, and f_n given by Eq. (31), (32) (34)
13: Generate the current and voltage plots obtained by the analytical method and reconstruction and display the above-given metrics

4.2. Circuit verification

The HB simulations are conducted using the commercially available Keysight Advanced Design System (ADS) tool [23]. HB simulations are widely recognized for their efficiency and accuracy in analyzing nonlinear circuits under periodic steady-state conditions [24]. By combining frequency-domain analysis with iterative techniques, HB simulations allow for a precise evaluation of harmonic interactions in high-frequency circuits, such as Class-E power amplifiers. The circuit values for the simulations were calculated using the design Eqs. (35) (36) and (37),

$$R = K_P \frac{V_{\text{DD}}^2}{P_{\text{out}}} \tag{35}$$

$$L = K_L \frac{R}{\omega_o} \tag{36}$$

$$C = K_C \frac{1}{\omega_o R} \tag{37}$$

Where, R: Load resistance; L: Inductance of the circuit; C: Capacitance of the circuit; K_P, K_L, K_C: Design coefficients; V_{DD}: DC supply voltage; P_{out}: Output power; and ω_o: Operating angular frequency

If the parameter K_X is positive, the excess impedance of the circuit is inductive. In this case, the additional inductance L_X is given by Eq. (38)

$$L_X = K_X \frac{R}{\omega_o} \tag{38}$$

Conversely, if K_X is negative, the excess impedance is capacitive, and the additional capacitance C_X is calculated as Eq. (39)

$$C_X = \frac{1}{\omega_o R|K_X|} \tag{39}$$

And if $K_X = 0$, we get the standard case known as the parallel case, where the series resonator is connected to the load network directly to

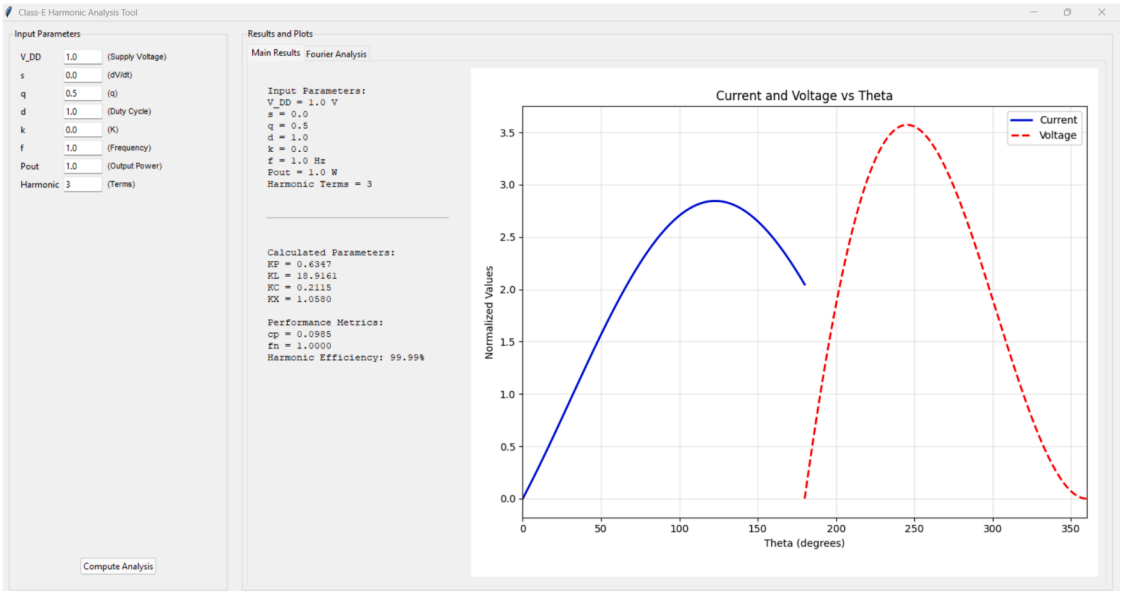


Fig. 2. Developed GUI for Class E design..

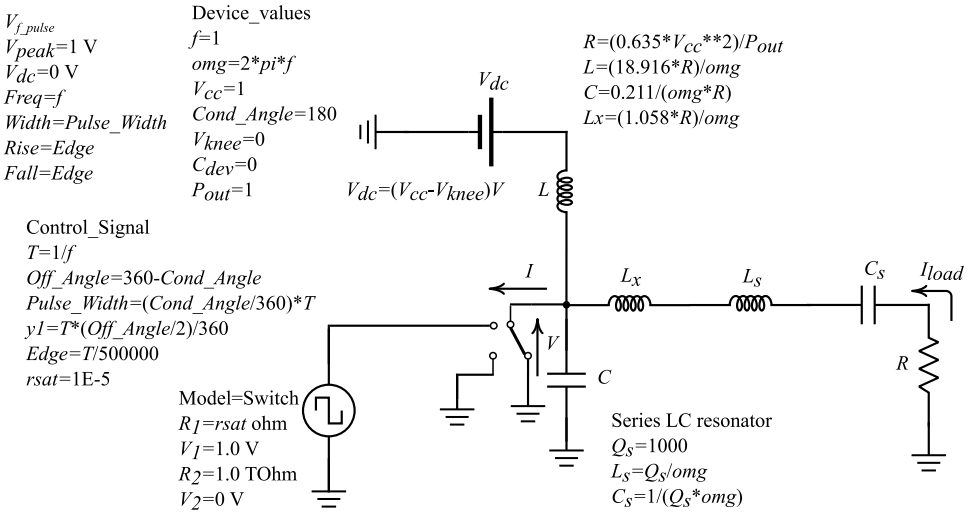


Fig. 3. ADS simulation setup for the idealized topology of Class-E PA for $q = 0.5$, $d = 1$, $K = 0$ and, $s = 0$.

the load resistance R without the need for any additional impedance [25] .

The simulation setup in ADS is depicted in Fig. 3. For comparative analysis, the input parameters are normalized to $f = 1$, $V_{cc} = 1$, and $P_{out} = 1$. In this setup, an input source $V_{f\_pulse} = 1$ is used, representing a voltage source with a Fourier series expansion of a periodic rectangular wave, characterized by varying pulse widths and duty cycles, within the HB simulation environment. All other essential parameters required for running the simulation are shown in Fig. 3.

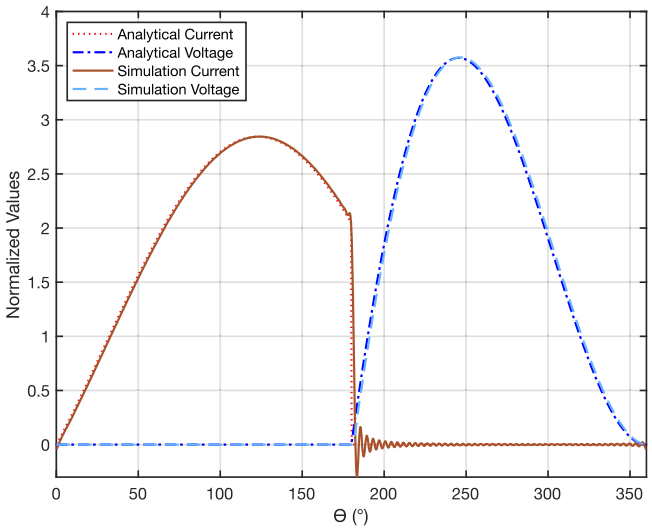
The voltage and current waveforms obtained from the analytical expressions are validated against HB simulation results using the ADS tool for the standard case of $q = 0.5$, $s = 0$ and $K = 0$, as illustrated in Fig. 4a. The close agreement between the analytical predictions and circuit simulations demonstrates the accuracy of the proposed model. Furthermore, the key performance metrics are benchmarked against existing literature to ensure consistency. Since practical implementations account for only a finite number of harmonics [26], the reconstructed waveform is also presented in Fig. 4b, providing a comprehensive comparison of the model's effectiveness and its practical applicability.

This comparative analysis confirms that the design equations yield comparative results, further validating the proposed design methodology. However, as the HB simulations employ nonlinear modeling, the solutions obtained from the circuit simulations are approximate and prone to oscillations, which must be carefully considered during analysis [24]. The role of selecting the quality factor of the series resonator must also be addressed during the design process. This aspect has been extensively explained in [18].

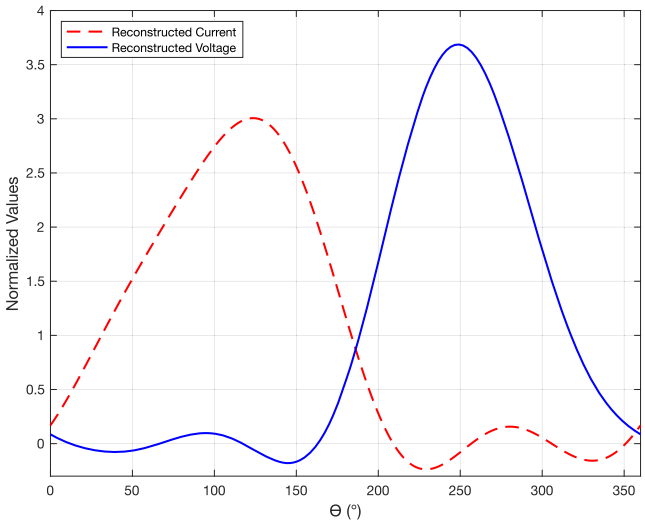
4.3. Performance analysis

The three important performance metrics harmonic effciency, η, maximum output power capability, c_p and normalized maximum operation frequency, f_n as defined in the Section by 3 are plotted against the design parameter $q = [0.5, 2]$ for $s = -1, 0, 1$ and $K = 0, 1$ with $d = 1$ to compare the results.

As observed in Fig. 5, the case of $K = 0$ with $s = 0$ gives the standard class E , but for $s = -1$ the operating frequency is enhanced as compared to standard case $s = 0$ however it comes at a cost of lower output power



(a)



(b)

Fig. 4. Voltage and current $d = 1$ $q = 0.5$ for $K = 0$ and $s = 0$ (a) analytical vs simulated and, (b) reconstructed waveform up to the 3rd harmonic.

capability and efficiency due to the power lost in the harmonics. Similarly, as observed in Fig. 6, with $K = 1$ and $s = 0$ exhibits higher output power capability, indicating reduced device stress. However, this comes at the cost of lower efficiency, presenting a trade-off scenario. Nevertheless, variations in the duty cycle introduce additional changes, leading to multiple trade-offs, as suggested by the graphical analysis. These design parameters, in turn, help the designers make an informed decision when selecting the components. In the case of a non-conventional Class E design, as presented, the analytical equations indicate a reduction in efficiency. Therefore, the design parameters must be carefully selected to maximize efficiency while satisfying the constraints imposed by the design equations.

4.4. Optimization

The solution to the analytical expressions yields an infinite set of possible solutions; however, many may not be valid when considering practical implementation constraints. Among these, device stress is the most critical parameter as it is a key input to determine the optimal design set. To address this, optimization can efficiently identify the best design parameters by directly incorporating device stress requirements, ensuring a practical and optimized solution without the need for exhaustive iterative processes or traditional curve-fitting techniques.

In this respect, the Simplicial Homology Global Optimization (SHGO) algorithm is a promising global optimization (GO) method [27], designed to solve general nonlinear programming (NLP) and black-box optimization problems, particularly in low-dimensional cases. This optimization category is also known as constrained derivative-free optimization. The general mathematical formulation of such problems is given by Eq. 40,

$$\min_{x} f(x), \quad x \in \mathbb{R}^n \tag{40}$$

subject to inequality and equality constraints given by Eq. 41 and 42

$$g_i(x) \geq 0, \quad \forall i = 1, \ldots, m \tag{41}$$

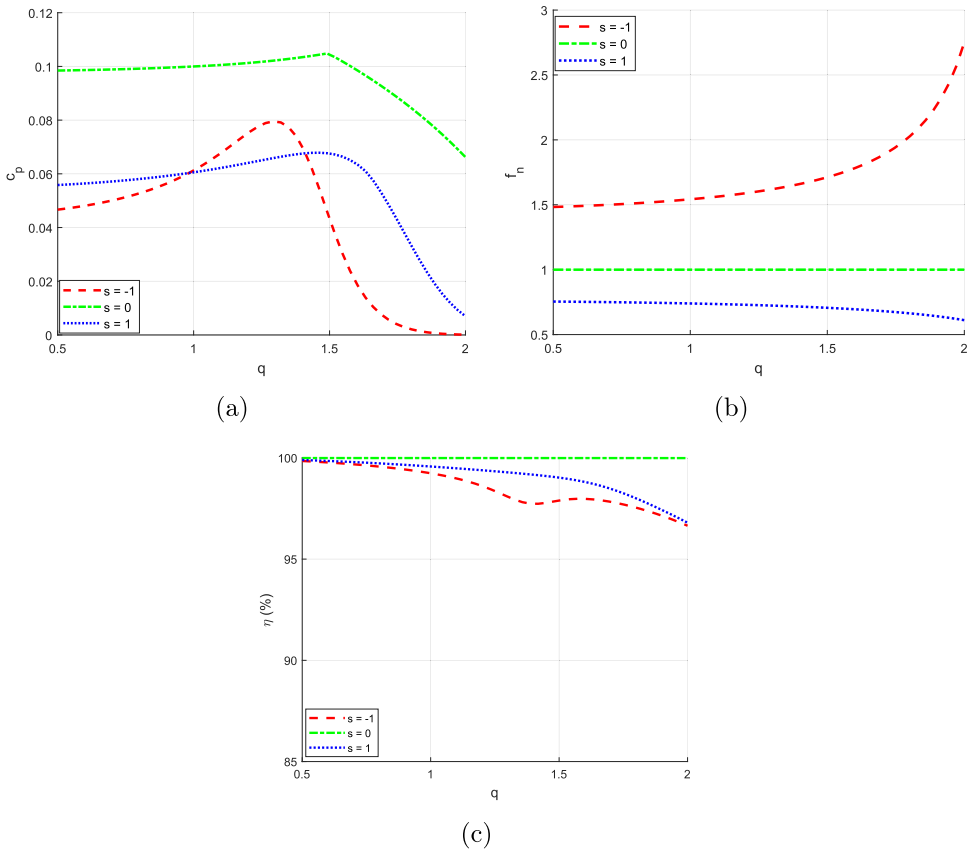


Fig. 5. Performance metrics of Class-E PA for $K = 0$, $d = 1$ for varying q with $s = -1, 0, 1$ (a) maximum output power capability, c_p, (b) normalized maximum operating frequency, f_n and, (c) harmonic efficiency, η.

Algorithm 2 Optimization of Generalized Class-E Parameters..

Input: Target values $I_{\max}^{(0)}, V_{\max}^{(0)}$, frequency f_0, weights w_1, w_2, w_3, w_4
Define parameter bounds:

$$s \in [-s_1, s_2], \quad q \in [q_1, q_2], \quad d \in [d_1, d_2], \quad k \in [-k_1, k_2]$$

function LossFunction(s, q, d, k)
  Compute: $K_P, K_L, K_C, K_X, I_{\max}, V_{\max}, \eta \leftarrow$ Calculate Class-E Params(s, q, d, k, f_0)
  $P_1 \leftarrow \max(0, I_{\max} - I_{\max}^{(0)})^2$ ▷ Current penalty
  $P_2 \leftarrow \max(0, V_{\max} - V_{\max}^{(0)})^2$ ▷ Voltage penalty
  $P_3 \leftarrow \begin{cases} 0, & 0.5 \le \eta \le 1.0 \\ (0.5 - \eta)^2, & \eta < 0.5 \end{cases}$ ▷ Efficiency penalty
  $P_4 \leftarrow \begin{cases} 0, & K_P \ge 0 \wedge K_L \ge 0 \wedge K_C \ge 0 \\ 1, & \text{otherwise} \end{cases}$ ▷ Penalty for invalid circuit components
  $L_1 \leftarrow w_1 \cdot P_1$
  $L_2 \leftarrow w_2 \cdot P_2$
  $L_3 \leftarrow w_3 \cdot P_3$
  $L_4 \leftarrow w_4 \cdot P_4$
  return $L_1 + L_2 + L_3 + L_4$
end function
procedure OptimizeParams
  Use SHGO to minimize LossFunction(s, q, d, k) over the defined bounds
  Return optimal (s^*, q^*, d^*, k^*), and the corresponding $(K_P, K_L, K_C, K_X, I_{\max}, V_{\max}, \eta, Metric)$
end procedure

Table 1
Comparison of target vs. achieved values along with the optimized design variables and the computed metric.

V_t	I_t	V_a	I_a	s	q	d	K	η	*Metric*
2	2	2.16	2.01	-0.602	1.174	1.851	0.078	96.8 %	0.0264
3	3	2.78	2.99	-0.665	2.231	1.004	1.693	96.9 %	0
4	4	3.82	2.39	1.439	2.213	1.106	1.342	95.17 %	0

$$h_j(x) = 0, \quad \forall j = 1, \ldots, p \tag{42}$$

where x is a vector of decision variables, $f(x)$ is the objective function $f : \mathbb{R}^n \to \mathbb{R}$, $g_i(x)$ represents the inequality constraints $g : \mathbb{R}^n \to \mathbb{R}^m$, and $h_j(x)$ represents the equality constraints $h : \mathbb{R}^n \to \mathbb{R}^p$. Additionally, optional lower and upper bounds can be imposed as shown in Eq. 43

$$x_l \le x \le x_u \tag{43}$$

Although most theoretical results on SHGO have been proven for cases where $f(x)$ is a Lipschitz-smooth function, the algorithm is also guaranteed to converge to a global optimum for non-continuous, non-convex, and non-smooth functions if the default sampling method is employed [28].

The optimization procedure, presented as pseudocode in Algorithm 2, aims to find the design parameters s, q, d, and k, such that the efficiency is maximized while the peak voltage and current are kept under the target values V_t and I_t. In practice, this algorithm is implemented using the open-source Python library SciPy [29].

Although efficiency is used as the primary metric in this work, other aspects can also be incorporated as needed, depending on the specific

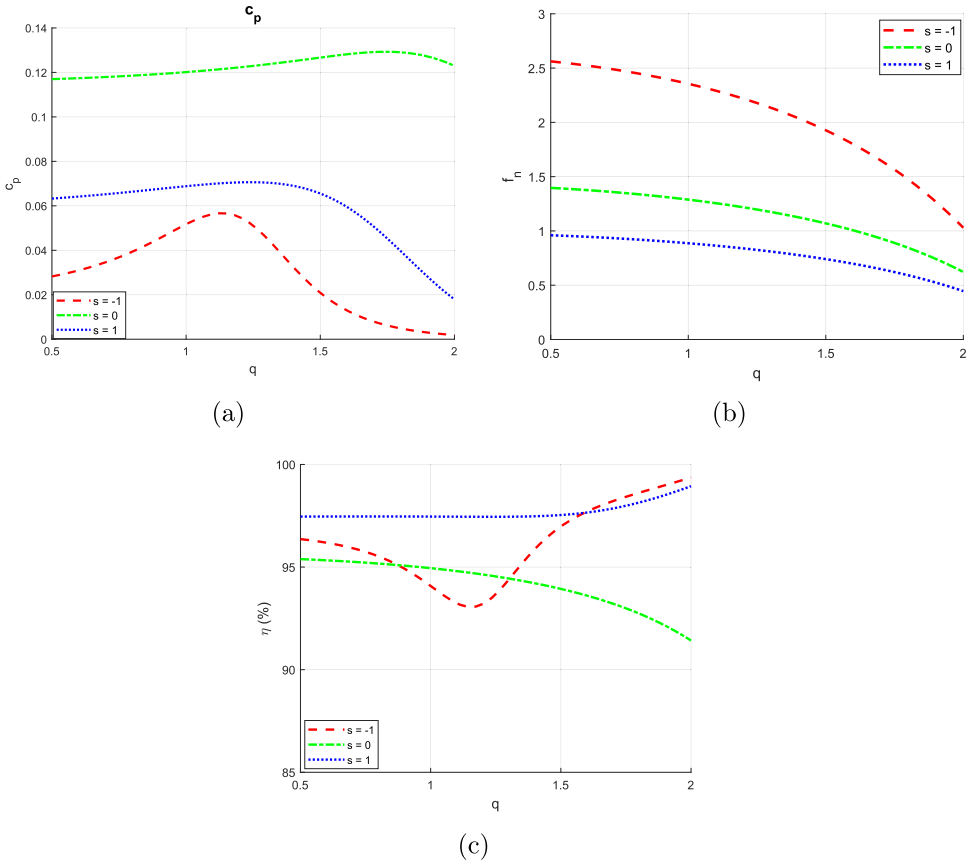


Fig. 6. Performance metrics of Class-E PA for $K = 1$, $d = 1$ for varying q with $s = -1, 0, 1$ (a) maximum output power capability, c_p, (b) normalized maximum operating frequency, f_n and, (c) harmonic efficiency, η .

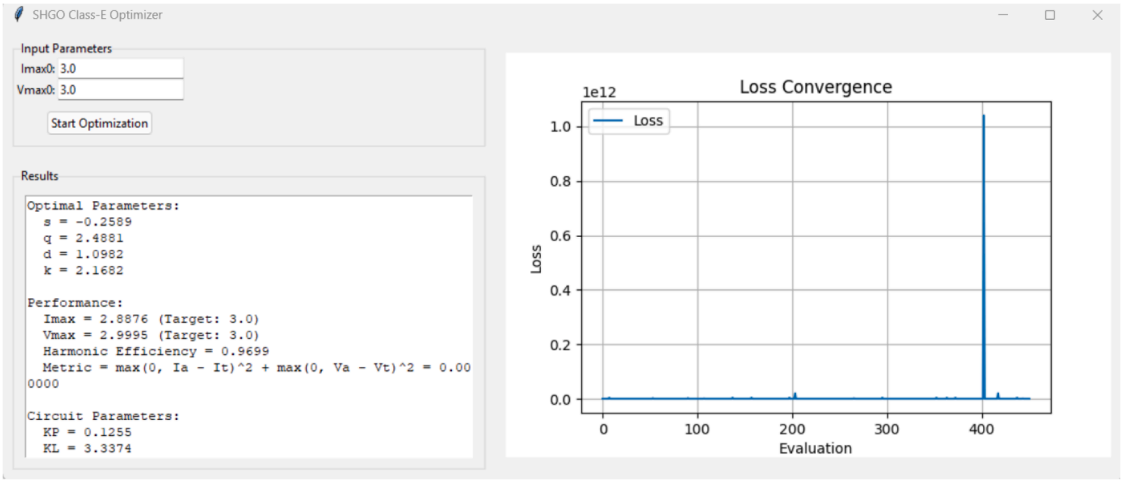


Fig. 7. GUI of the developed optimizer with integrated circuit design environment. .

requirements of the design process. For example, an additional metric quantifying how much the obtained waveform exceeds the maximum target values V_t and I_t can be obtained as shown in Eq. (44).

$$\text{Metric} = \max(0, I_a - I_t)^2 + \max(0, V_a - V_t)^2 \tag{44}$$

where I_a and V_a represent the maximum values of the optimized current and voltage waveforms, respectively, which is taken from the optimization algorithm directly.

Table 1 presents some optimization results for three target voltages and currents, and one can notice that in two cases the metric achieves the ideal value of 0, meaning that the resulting waveform perfectly satisfies the imposed condition. Compared to traditional optimization methods, which are usually based on heuristic algorithms or trial and error approaches, this framework deterministically finds the most suitable circuit elements according to a set of customizable constraints.

A screenshot for the developed GUI for optimization is shown in Fig. 7. The interface allows users to input design parameters, visualize optimization progress, and analyze resulting performance metrics in real time. Additionally, the program displays the design set K, which can be directly used to find out the practical circuit elements given by Eqs. 35, 36, 37, 38, 39.

5. Conclusion and future work

This paper presents a comprehensive analytical approach for the synthesis of Class-E power amplifiers, extending the conventional design space and enabling accurate optimization of key performance metrics. To enhance accessibility and promote broader adoption, an open-source GUI tool has been developed, allowing researchers to efficiently analyze and refine their designs. The proposed methodology has been validated through nonlinear harmonic balance simulations, demonstrating strong predictive capability, although experimental validation has not yet been conducted. Thus, future work will mainly focus on performing practical assessment of the model, while also making the theoretical framework more robust by incorporating empirically relevant effects such as non-ideal switching behavior, component imperfections and parasitic responses.

CRediT authorship contribution statement

Pallab Kr Gogoi: Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization; **Ştefan Ştefănescu:** Visualization, Software, Resources; **Jurgen Vanhamel:** Writing – review & editing, Supervision, Project administration; **Jérôme Loicq:** Writing - review & editing, Supervision, Project administration.

Data availability

Data will be made available on request.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The author is an Editorial Board Member/Editor-in-Chief/Associate Editor/Guest Editor for this journal and was not involved in the editorial review or the decision to publish this article.

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

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