# Revisiting the Partial Power Processing Concept

## Case Study of a 5-kW 99.11% Efficient Flyback Converter-Based Battery Charger

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# Revisiting the Partial Power Processing Concept: Case Study of a 5-kW 99.11% Efficient Flyback Converter-Based Battery Charger

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***Abstract*— This article proposes an analytical methodology to evaluate the performance of the main partial power processing (PPP) architectures in terms of the improvements in the system's conversion efficiency. This analysis considers the influence of the system's voltage gain, the auxiliary dc/dc converter's efficiency, and the possibility of bidirectional power flow. Herein, the key PPP architectures are, thus, modeled and benchmarked. The presented results attest to the series configuration as the most efficient PPP circuit solution, with no limits on the system voltage gain, contrary to the generalized results found in today's literature. To assess these results and the significance of the proposed analysis, a well-known, simple, and cost-effective flyback topology has been designed and tested for a series PPP circuit solution able to effectively interface a 5-kW battery energy storage system (BESS) to a 700-V dc grid. A relatively high power conversion efficiency and compact hardware are achieved due to the reduced size requirements on the input and output filtering stages. Above all, while explaining the PPP concept, this study shows that even converter circuits known for their low power efficiency can be used to derive highly efficient systems. A design approach is, thus, provided to facilitate the design of the presented PPP circuit, and measurements are, finally, carried out to compare the obtained results with the expected ones derived from the developed analytical models.**

***Index Terms*— Battery charger, battery energy storage system (BESS), dc-dc power conversion, flyback converter, partial power processing (PPP).**

## I. Introduction

SOCIETAL and environmental concerns have increased the interest in sustainable power sources and the rational use of the electric energy [1]. The ongoing electrification of loads and the consequent electrical power demand growth is forcing grids toward more complex architectures capable of interconnecting several decentralized energy sources [4]. The interest in the application of battery energy storage systems (BESSs) is increasing due to the efficiency improvements that they can provide on the energy usage [5], aided by the superior properties of the lithium-based technology, for industrial, transportation, and household applications, particularly for electric vehicles (EVs), the provision of an uninterruptible power supply (UPS) functionality, and for grid ancillary services provision as peak power shaving, congestion management, and/or frequency regulation in MV grids [6]. Besides, EVs still have several challenges, such as limited range, high cost, slow charging, and limited charging opportunities in cities [2]. Achieving higher EV battery charger efficiencies and decreasing their size can help to increase the charging rate and reduce costs, thus helping the societal transition to electric mobility [3].

Hence, remarkable research effort has been spent to improve the efficiency, size, and cost of power conversion stages for BESSs. Conventional circuit solutions are intended to process the full power flowing through the BESS. Therefore, these systems must be rated for the maximum power that the BESS is intended to process. This naturally limits the achievable improvements in terms of conversion efficiency, power density, and manufacturing costs, which are challenged by the circuit component technology, especially whenever wide voltage gain or high currents are involved [7]. Recently, the interest in solid-state power conversion stages processing only a partial part of the total flowing power, commonly addressed as partial power processing (PPP) circuits, differential power processing (DPP) circuits, or fractional power processing circuits, is growing due to the increasing number of applications, which might benefit from their advantages, for instance, PV [8], electrochemical energy storage [9], BESS [10], EV charging [11], [12], and power flow control for meshed dc grids [13]. Indeed, since only a part of the power is processed by the converter, a secondary path is provided for the power to flow directly to the load with close to unitary efficiency [14]. Accordingly, only the auxiliary converter's reduced processed power contributes to a significant loss of energy, achieving a higher overall system conversion efficiency compared to a full power processing (FPP) converter [19]. Moreover, due to the lower power processed by the auxiliary converter, partially rated circuit components can be used, which will

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lead to both a higher power density and a more cost-effective solution [15].

Nevertheless, conventional PPP circuits have also drawbacks, such as the lack of galvanic isolation, which might involve challenges for some applications. Indeed, the PPP circuit concept is not new, as its first application seems to be in spacecraft technology for the photovoltaic generation [16] where its advantages and limitations were well described.

Although the literature has already addressed several PPP circuit concepts and their operation principles, a research gap is found in the development of the system's analytical models in terms of its voltage gain limitations, power conversion efficiency, and the partial power, which is processed. In fact, not much attention has been paid to the sensitivity analysis of the PPP system performance as a function of the power flow direction, which is particularly important in applications dealing with bidirectional power flows, such as BESS. Indeed, today's literature mostly considers the usage of PPP circuits in unidirectional power flow applications, namely, PV, grid-to-vehicle (G2V) battery charging, and electrochemical processes. Particularly, in the household application, a bidirectional power converter enables the reversed EV vehicle-to-grid (V2G) functionality, where the EV's battery can operate as a UPS system and/or buffer the power locally generated to benefit economically the owner and help to stabilize the local distribution grid with congestion management [17].

This article addresses the described research gap by developing comprehensive analytical modeling of the conventional PPP circuits and on the experimental verification of the study. The main contributions of this article are given as follows.

1) A detailed analysis of series and parallel PPP architectures operating with the bidirectional power flow necessary for the battery charging application.
2) The proof that it is possible to derive very highly efficient (>99%) battery chargers using a traditional power electronics circuit, i.e., a flyback topology that is well received in many different applications, as it perceives a low cost, a low complexity, and has dedicated control ICs ready available on market. These features are important in today's battery charging applications, where many new players are joining this market, and low-cost power electronics solutions adding outstanding high power efficiency become of paramount importance for a competitive advantage.
3) The development of analytical models and experimental verification of a series PPP based on a bidirectional flyback converter.

The remainder of this article is organized as follows. In Section II, a theoretical benchmarking between the series and parallel PPP architectures is given while considering the system attained efficiencies and the partial power processed by the auxiliary dc/dc converter according to the power flow direction. Finally, a design approach for a dc grid-tied BESS is proposed in Section III by means of a PPP system conceptualized with a conventional flyback converter arranged in a series PPP configuration, assessing the tradeoff on the coupled inductor turn ratio and its influence on the system efficiency and maximum components' applied voltage stress. Experimental results are, thus, assessed on a 5-kW laboratory prototype in Section IV in order to verify the developed analytical modeling and the advantages of the presented PPP.

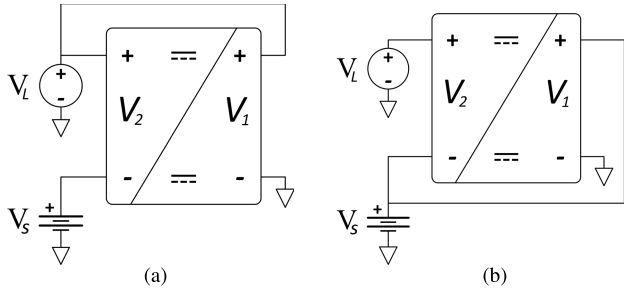



Fig. 1. PPP main architectures. (a) Parallel PPP. (b) Series PPP.

## II. Partial Power Processing Architectures

According to the literature, the series (input-parallel output-series) and parallel (input-series output-parallel) PPP architectures, as shown in Fig. 1, are addressed as the two main researched PPP architectures [18]. These PPP architectures require a dc/dc converter with nondirect internal ground connection due to the different voltage references on the negative input–output ports. This definition allows the use of nonisolated dc/dc topologies [19] and not only galvanic isolated ones, as claimed in [20]. However, due to the series connection of the battery voltage $V_S$ with the auxiliary dc/dc converter's output port $V_2$, a galvanic isolation between $V_S$ and the dc grid voltage $V_L$ is lost even if isolated dc/dc topologies are involved [16], [21]. Hence, additional stages or smart solutions are required if galvanic isolation is a requirement for the application. Besides, while, in both series and parallel architectures, the converter's output port $V_2$ requires to be rated only for the differential voltage $V_L - V_S$, the input port $V_1$ is subject to different voltage requirements according to whether it is connected to $V_L$ or $V_S$ in the parallel or series architecture, respectively [20].

In the remainder of this article, the dc grid voltage $V_L$ is assumed to be greater than the battery voltage $V_S$, i.e., $V_L > V_S$.

### A. PPP Architectures' Comparison

Despite some previous literature [9], [14], [18]–[22] have benchmarked the series and parallel PPP architectures, the analytical modeling of their efficiency is addressed in a simplified manner. Indeed, the limit on the input–output voltage gap in the parallel PPP architecture, beyond which the efficiency of the system goes lower than that of an FPP system, is not a limit anymore for a series PPP circuit. Moreover, the results presented in the following will demonstrate how the efficiency of different PPP architectures is strongly influenced by the power flow direction, e.g., power flowing from a dc-bus to a rechargeable battery load or vice versa.

According to Kanstad *et al.* [3] and Jørgensen [21], for the case of the parallel PPP configuration shown in Fig. 1(a), it is possible to express the partial power processed by the dc/dc converter as the ratio between the power flowing

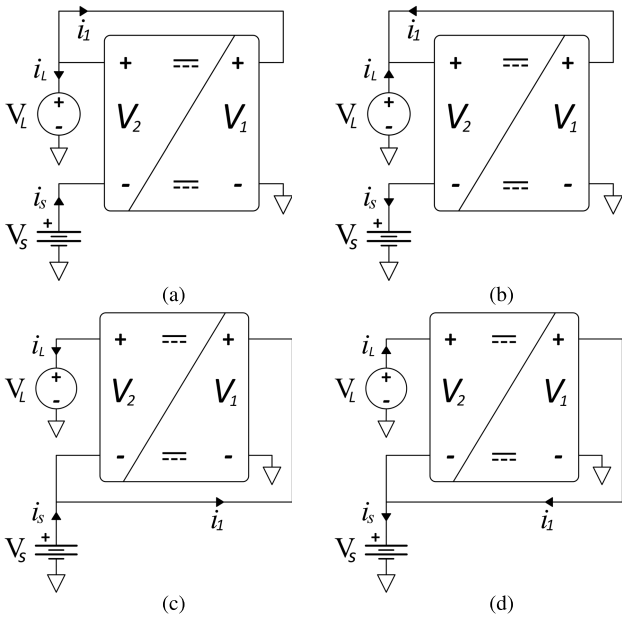



Fig. 2. PPP source-load architectures. (a) Parallel PPP-source. (b) Parallel PPP-load. (c) Series PPP-source. (d) Series PPP-load.

into this circuit, $P_{\text{converter}}$, and the power delivered to or from the battery, $P_S$, as

$$k_p = \frac{P_{\text{converter}}}{P_S} = \frac{V_2 \cdot I_S}{V_S \cdot I_S} \approx \frac{V_L - V_S}{V_S}. \tag{1}$$

The system conversion efficiencies of both series and parallel PPP architectures can then be expressed as functions of the converter efficiency $\eta_c$ and the ratio $k_p$ for both power flow directions, i.e., the charging or discharging of the battery load. Accordingly, results are compared with the efficiency of a conventional FPP architecture, $\eta_{\text{sys}} = \eta_c$.

*1) Parallel PPP Architecture—Source Power Flow:* The total system's efficiency $\eta_{\text{sys}}$ of the parallel PPP circuit is analyzed while processing a power flow direction from the battery to the dc grid or $V_S$ to $V_L$, i.e., as illustrated in Fig. 2(a). Herein, this power flow direction will be referred to as Source. It is possible to write the expression for the dc/dc converter current $i_1$ as

$$i_1 = \frac{i_S \cdot (V_L - V_S)}{\eta_c \cdot V_L}. \tag{2}$$

Therefore, the system's total efficiency is given by

$$\eta_{\text{sys}} = \frac{P_L}{P_S} = \frac{V_L \cdot (i_S - i_1)}{V_S \cdot i_S} = \frac{(1 + k_p) \cdot \eta_c - k_p}{\eta_c}. \tag{3}$$

The parallel PPP system efficiency, $\eta_{\text{sys}}$, is plotted in Fig. 3(a) as a function of the dc/dc converter efficiency $\eta_c$ and different values of $k_p$. Note that, for values of $k_p$ greater than 1, the PPP total system efficiency is always lower than what is obtained by a conventional dc/dc converter solution processing the full source power, i.e., an FPP system.

The partial power processed by the converter can be evaluated according to the converter input power $P_1 = V_1 \cdot i_1 = V_L \cdot i_1$. Therefore, it is possible to express the dc/dc converter input power $P_1$ as a function of the battery power $P_S = V_S \cdot i_S$ by using the relation $V_L = V_1 = V_S \cdot (1 + k_p)$ and (2)

$$P_1 = i_S \cdot \frac{V_S \cdot (1 + k_p) - V_S}{\eta_c} = P_S \cdot \frac{k_p}{\eta_c}. \tag{4}$$

Hence, the partial power processed by the converter is

$$P_{\text{PP}} = \frac{P_1}{P_S} = \frac{k_p}{\eta_c}. \tag{5}$$

The sensitivity of $P_{\text{PP}}$ with the variables $\eta_c$ and $k_p$ is shown in Fig. 3(c). It can be noticed that, as the converter efficiency decreases, naturally, more power needs to be processed by the dc/dc converter, and eventually, the PPP circuit solution will process more power than an FPP dc/dc converter.

*2) Parallel PPP Architecture—Load Power Flow:* The total system's efficiency $\eta_{\text{sys}}$ of the parallel PPP architecture is analyzed while processing a power flow direction from the dc grid to the load (battery) or $V_L$ to $V_S$, i.e., as illustrated in Fig. 2(b). Herein, this power flow direction will be referred to as load. It is possible to write the expression for the dc/dc converter current $i_i$ as

$$i_1 = \frac{\eta_c \cdot i_S \cdot (V_L - V_S)}{V_L} = i_S \cdot \frac{k_p \cdot \eta_c}{1 + k_p}. \tag{6}$$

Therefore, the total system's efficiency is given by

$$\eta_{\text{sys}} = \frac{i_S \cdot V_S}{V_L \cdot (i_S - i_1)} = \frac{1}{1 + k_p \cdot (1 - \eta_c)}. \tag{7}$$

The parallel PPP system efficiency, $\eta_{\text{sys}}$, is plotted in Fig. 3(b). As it can be observed, for values of $k_p$ greater than 1 and within a certain dc/dc converter efficiency range $\eta_c$, the analyzed $\eta_{\text{sys}}$ is found to be lower than the one obtained by an FPP system.

The partial power that is processed by the dc/dc converter can be evaluated according to its input power $P_2 = V_2 \cdot i_2 = (V_L - V_S) \cdot i_S$. It is possible to express the current $i_L$ as

$$i_L = i_S - i_1 = i_S \cdot \left(1 - \frac{k_p \cdot \eta_c}{1 + k_p}\right) \tag{8}$$

which gives

$$i_S = i_L \cdot \frac{1 + k_p}{1 + k_p - k_p \cdot \eta_c}. \tag{9}$$

Therefore, it is possible to express the dc/dc converter input power $P_2$ as a function of the dc grid delivered power $P_L = V_L \cdot i_L$ by using the relation $V_L = V_S \cdot (1 + k_p)$ and the equation (9) as

$$P_2 = (V_L - V_S) \cdot i_S = P_L \cdot \frac{k_p}{1 + k_p - k_p \cdot \eta_c}. \tag{10}$$

Hence, the partial power processed by the converter is

$$P_{\text{PP}} = \frac{P_2}{P_L} = \frac{k_p}{1 + k_p - k_p \cdot \eta_c}. \tag{11}$$

The sensitivity of $P_{\text{PP}}$ with the variables $\eta_c$ and $k_p$ is shown in Fig. 3(d). It can be noticed that, as the converter efficiency increases, more power is processed by the dc/dc converter, and eventually, the PPP circuit solution will process more power than an FPP dc/dc converter.

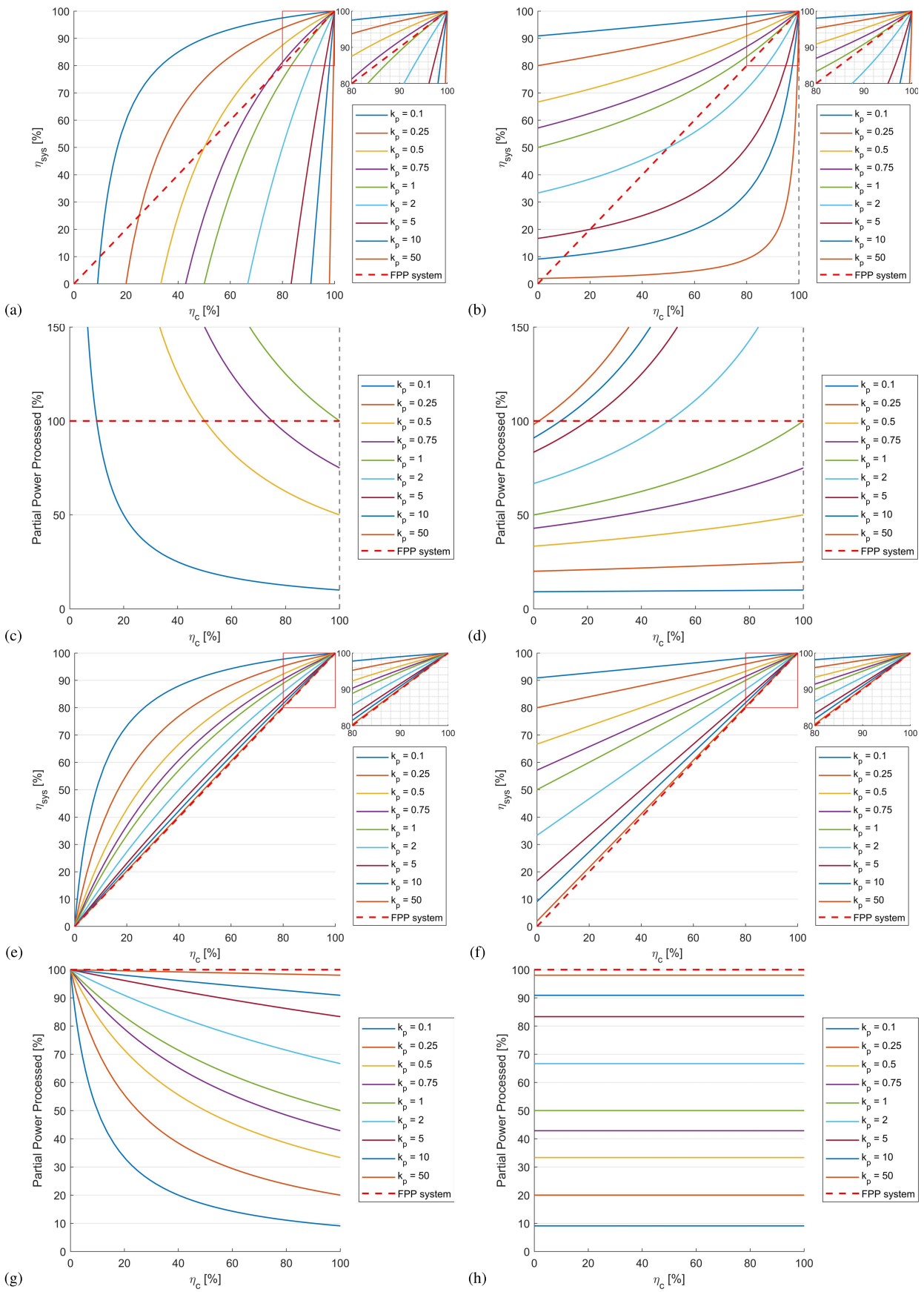



Fig. 3. Parallel PPP system conversion efficiency as (a) source and (b) load, and converter's partial power processed as (c) source and (d) load. Series PPP system conversion efficiency as (e) source and (f) load, and converter's partial power processed as (g) source and (h) load.

*3) Series PPP Architecture—Source Power Flow:* The total system's efficiency $\eta_{\text{sys}}$ of the series PPP architecture is analyzed while processing a power flow direction from the battery to the dc grid or $V_S$ to $V_L$, i.e., as illustrated in Fig. 2(c). It is possible to write the expression for the dc/dc converter current $i_1$ as

$$i_1 = \frac{i_L \cdot (V_L - V_S)}{\eta_c \cdot V_S} = i_L \cdot \frac{k_p}{\eta_c}. \tag{12}$$

Therefore, the total system's efficiency is given by

$$\eta_{\text{sys}} = \frac{i_L \cdot V_L}{V_S \cdot (i_L + i_1)} = \frac{\eta_c \cdot (1 + k_p)}{\eta_c + k_p}. \tag{13}$$

The series PPP system efficiency operating in the source power flow direction is plotted in Fig. 3(e) as a function of $\eta_c$ and $k_p$. It can be seen that there is no limit of $k_p$ above which the system's efficiency is lower than that of an FPP system. Nevertheless, as the power ratio $k_p$ increases, the gain in the improvements of the power efficiency of the series PPP system reduces compared to an FPP system.

The partial power that is processed by the converter can be evaluated according to the converter input power $P_1 = V_1 \cdot i_1 = V_S \cdot i_1$. It is possible to write the current $i_L$ as

$$i_L = \frac{\eta_{\text{sys}} \cdot V_S \cdot i_S}{V_L}. \tag{14}$$

Therefore, it is possible to express the converter input power $P_1$ as a function of the battery delivered power $P_S = V_S \cdot i_S$, by using the relation $V_L = V_S \cdot (1 + k_p)$, as

$$P_1 = V_S \cdot i_L \cdot \frac{k_p}{\eta_c} = P_S \cdot \frac{k_p \cdot \eta_{\text{sys}}}{\eta_c \cdot (1 + k_p)} \tag{15}$$

which, by combination with (13), leads to the partial power processed expression

$$P_{\text{PP}} = \frac{P_1}{P_S} = \frac{k_p}{k_p + \eta_c}. \tag{16}$$

The analysis of $P_{\text{PP}}$ as a function of $\eta_c$ and $k_p$ for the series PPP circuit in the source power flow direction is shown in Fig. 3(g). It can be noticed that, always, less power is processed by this PPP solution than that of an FPP system regardless of $k_p$.

*4) Series PPP Architecture—Load Power Flow:* The total system's efficiency of the series PPP architecture is analyzed while processing a power flow direction from the dc grid to the battery or $V_L$ to $V_S$, i.e., as illustrated in Fig. 2(d). It is possible to write the dc/dc converter current $i_1$ as

$$i_1 = \frac{\eta_c \cdot i_L \cdot (V_L - V_S)}{V_S} = \eta_c \cdot k_p \cdot i_L \tag{17}$$

and, since $i_S = i_L + i_1$, the total system's efficiency is given by

$$\eta_{\text{sys}} = \frac{V_S \cdot (i_L + i_1)}{V_L \cdot i_L} = \frac{1 + k_p \cdot \eta_c}{1 + k_p}. \tag{18}$$

The series PPP system efficiency for the load power flow direction is plotted in Fig. 3(f) as a function of $\eta_c$ and $k_p$. It can be seen that there is no limit of $k_p$ above which the system's efficiency is lower than an FPP system. Nevertheless, as for the series PPP operating in the source power flow direction, as the power ratio $k_p$ increases, the gain on the improvement of the system power efficiency reduces compared to an FPP system.

TABLE I
PPP CONFIGURATIONS' ANALYTICAL RESULTS

| PPP Configuration | $\eta_{sys}$ | $P_{PP}$ |
|---|---|---|
| Parallel Source | $\frac{(1+k_p)\cdot\eta_c - k_p}{\eta_c}$ | $\frac{k_p}{\eta_c}$ |
| Parallel Load | $\frac{1}{1+k_p\cdot(1-\eta_c)}$ | $\frac{k_p}{1+k_p-k_p\cdot\eta_c}$ |
| Series Source | $\frac{\eta_c\cdot(1+k_p)}{\eta_c+k_p}$ | $\frac{k_p}{k_p+\eta_c}$ |
| Series Load | $\frac{1+k_p\cdot\eta_c}{1+k_p}$ | $\frac{k_p}{k_p+1}$ |

The partial power that is processed by the dc/dc converter can be evaluated according to its input power $P_2 = V_2 \cdot i_2 = (V_L - V_S) \cdot i_L$. Therefore, it is possible to express $P_2$ as a function of the dc grid delivered power $P_L = V_L \cdot i_L$, by using the relation $V_L = V_S \cdot (1 + k_p)$ and $P_2 = (P_1/\eta_c)$, as

$$P_2 = \frac{\eta_c \cdot k_p \cdot i_L \cdot V_S}{\eta_c} = P_L \cdot \frac{k_p}{k_p + 1}. \tag{19}$$

Hence, the partial power processed by the converter is

$$P_{\text{PP}} = \frac{k_p}{k_p + 1}. \tag{20}$$

The analysis of $P_{\text{PP}}$ as a function of $\eta_c$ and $k_p$ for the series PPP system in the load power flow direction is shown in Fig. 3(h). It can be noticed that the power that is processed by the converter is always less than the one processed by an FPP converter, and in this case, it is also independent of the dc/dc converter's efficiency $\eta_c$ as it directly relies on the power ratio $k_p$ [cf. Fig. 3(f)].

Finally, the obtained results are, thus, summarized in Table I.

## III. DESIGN APPROACH FOR GRID-TIED BESS WITH PPP-BASED CONVERTER

In Section II, it has been shown how the power ratio is a common design tradeoff for PPP-based converters. For example, there is a critical voltage gain in the parallel PPP solution, above which this concept becomes less efficient than an FPP system. The series PPP architecture overcomes this limitation as this circuit always processes less power than an FPP system. However, the higher the voltage gain is, the higher is the power the auxiliary dc/dc converter has to process, reducing its advantages in relation to an FPP system. Nevertheless, despite that, the series PPP system's conversion efficiency is anyway higher than that of an FPP system. Moreover, according to results in Fig. 3, under the same load conditions, the auxiliary converter in a parallel PPP architecture would always process more power than in a series PPP architecture. Thus, the resulting auxiliary converter's volume would be larger in a parallel PPP architecture due to both higher active and passive components' sizing requirements. However, the achieved analytical results are valid for any auxiliary converter topology, which fulfills PPP architecture requirements.

In this article, to assess this result, special attention has been paid to the design of a series PPP circuit implementing as

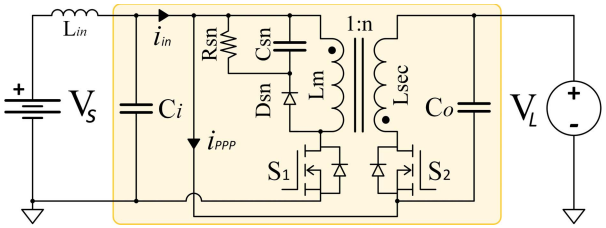



Fig. 4. Bidirectional series PPP flyback topology.

TABLE II
SWITCHES' VOLTAGE STRESS

| Configuration | $V_{DS_1}$ | $V_{DS_2}$ |
|---|---|---|
| FPP | $V_S + \frac{1}{n}V_L$ | $V_L + nV_S$ |
| Parallel PPP | $V_L + \frac{1}{n}(V_L - V_S)$ | $(1+n)V_L - V_S$ |
| Series PPP | $V_S + \frac{1}{n}(V_L - V_S)$ | $V_L + (n-1)V_S$ |

TABLE III
BESS SPECIFICATIONS

| Parameter | Value |
|---|---|
| Operating Range: | 430 − 550 V DC |
| Max. Recharge Current: | 10.7 A @ 467 V |
| Max. Discharge Current: | 11.7 A @ 427 V |
| Max. (Dis)charge Power: | 5 kW |

an auxiliary dc/dc converter a bidirectional flyback converter, as shown in Fig. 4. This dc/dc converter represents a well-received, low complexity, and cost-effective galvanic isolated circuit topology, which is capable of handling bidirectional power flow, as required in BESS applications with many dedicated control ICs available on market. Since a nondirect topology is a requirement for any PPP converter, as previously stated in Section II, any galvanic isolated topology fulfills this requirement with the added possibility, compared to nonisolated topologies, of achieving a reduced components' voltage stress due to the transformer turn ratio [20]. According to Fig. 1, the applied voltage stresses on the flyback switches are reported in Table II for both parallel and series PPP architectures.

According to results in Table II, the series PPP architecture shows the lowest applied voltage stress on both flyback switches under every load condition. Accordingly, the series architecture is, thus, chosen to interface a commercial household BESS ($V_S$), specifications of which are given in Table III, to a 700-V dc grid ($V_L$).

To model the converter, $V_S$ is initially taken as a source; the input filtering and the snubber circuits are neglected. However, those elements are taken into account for conversion losses only.

The two current conduction subintervals are $DT_S$ and $D'T_S$, as shown in Fig. 5(a) and (b), respectively, where $D$ is the driving duty cycle, $D' = 1 - D$, and $T_S$ is the switching period. Moreover, the converter is assumed to operate in the continuous conduction mode (CCM), and the coupled inductor of the flyback converter is considered to have a high coupling factor $K = 1$, where $M = K \cdot (Lm \cdot L_{\text{sec}})^{1/2}$, $Lm$ is the

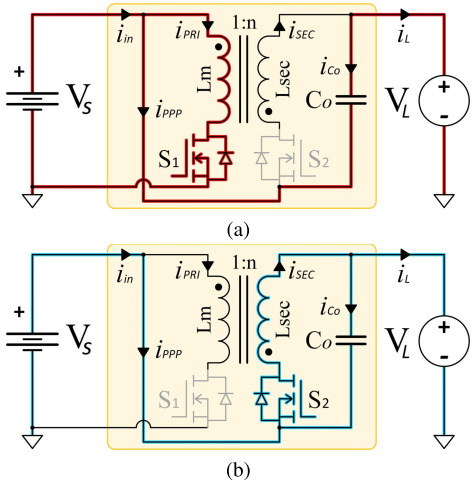



Fig. 5. Bidirectional series PPP flyback topology current conduction subintervals. (a) D subinterval. (b) D' subinterval.

magnetizing inductance referred to the primary side, and $L_{\text{sec}}$ is the secondary winding inductance.

It is, thus, possible to write the state equations for the $D$ subinterval

$$\frac{\partial i_{\text{pri}}(t)}{\partial t} = \frac{v_{Lm}(t)}{Lm} = \frac{v_S(t)}{Lm} \tag{21a}$$

$$\frac{\partial v_{Co}(t)}{\partial t} = \frac{i_{Co}(t)}{Co} = -\frac{i_L(t)}{Co} \tag{21b}$$

$$i_S(t) = i_{\text{pri}}(t) + i_L(t) \tag{21c}$$

while the state equations for the $D'$ subinterval are

$$\frac{\partial i_{\text{pri}}(t)}{\partial t} = \frac{v_{Lm}(t)}{Lm} = -\frac{v_L(t) - v_S(t)}{n \cdot Lm} \tag{22a}$$

$$\frac{\partial v_{Co}(t)}{\partial t} = \frac{i_{Co}(t)}{Co} = \frac{i_{\text{sec}}(t) - i_L(t)}{Co} \tag{22b}$$

$$i_S(t) = i_L(t). \tag{22c}$$

By considering the variables averaged values within the switching period $T_S$, denoted here as $I_{\text{pri}}$, $I_{\text{sec}}$, $I_{Co}$, $I_S$, $I_L$, $V_{Co}$, $V_S$, and $V_L$, it is possible to write the steady-state equations as

$$0 = \frac{V_S}{Lm}D - \frac{V_L - V_S}{n \cdot Lm}D' \tag{23a}$$

$$0 = -I_L D + (I_{\text{sec}} - I_L)D' \tag{23b}$$

$$I_S = (I_{\text{pri}} + I_L)D + I_L D'. \tag{23c}$$

By solving (23a)–(23c), the voltage and current conversion ratios, as well as the primary and secondary inductor currents, can be obtained

$$G_V = \frac{V_L}{V_S} = \frac{1 + (n-1)D}{1 - D} = G'_V + 1 \tag{24a}$$

$$G_I = \frac{I_L}{I_S} = \frac{D'}{nD + D'} \tag{24b}$$

$$I_{\text{pri}} = I_{\text{sec}} \cdot n = \frac{n}{D'}I_L \tag{24c}$$

$$I_{\text{sec}} = \frac{I_L}{D'} \tag{24d}$$

where $G'_V = n(D/D')$ is the voltage gain of a conventional FPP flyback.

The coupled inductor and input currents are shown in Fig. 6, where $i_{\text{pri}}$ is the current in the primary side of the coupled

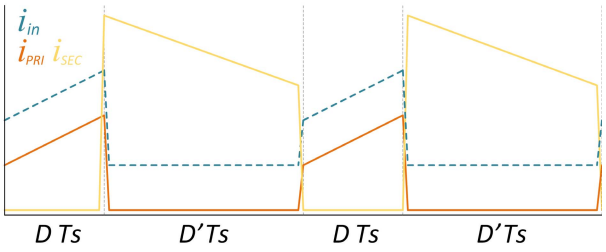



Fig. 6. Series PPP flyback topology currents.

inductor (or the current across the S1 switch), $i_{\text{sec}}$ is the current in the secondary side of the coupled inductor (or the current across the S2 switch), and $i_{in}$ is the input current.

It can be noticed that, while considering the power flow from the battery to the dc grid, the input current $i_{in}$ never becomes discontinuous (or goes to zero) due to the series connection, which provides a secondary path for the power to flow directly from the battery to the dc grid. If this result is compared to a conventional FPP flyback converter, assuming the same magnetizing inductance $Lm$ and the same power provided to the load, (24a) states that the duty cycle of the partial power converter is smaller due to the series connection of $V_S$ with the output port $V_2$ of the dc/dc converter. Therefore, the ripple and average currents, as of (21a) and (24c), on the primary winding of the coupled inductor are also lower in the PPP converter. Thus, since the same average current is sourced from the battery in both FPP and PPP power architectures, it can be stated that the maximum magnitude of the input current is lower in the PPP circuit solution. As a consequence, the input filtering size requirements are, thus, reduced, for instance, $C_i$ and $L_{in}$ in Fig. 4. Accordingly, as a result of the architectural series connection, the output capacitor is also subject to a lower applied voltage. Thus, the same output voltage or current ripple can be achieved with smaller capacitance values than those of the conventional FPP converter. However, as for a conventional FPP bidirectional flyback converter, a snubber circuit is required to limit the voltage overshoot on the S1 and S2 switches, according to the power flow direction due to the coupled inductor leakage inductance. The snubber circuit on the secondary switch was not required for this article's designed hardware, which will be discussed in the following, and it has been implemented only for the primary switch S1 according to Fig. 4.

By reversing the currents directions in Fig. 5, it is possible to obtain the converter's equations whenever the battery is operating as a load, e.g., whenever the battery is being recharged. These, according to the mathematical models, differ only for the current conversion ratio, which becomes

$$G_{I_{\text{LOAD}}} = \frac{I_L}{I_S} = \frac{D'}{1+(n-1)D}. \tag{25}$$

The efficiency of the system has, thus, been modeled as

$$\eta_{\text{sys}} = \frac{P_L}{P_S + P_{\text{losses}}} \quad \text{or} \quad \frac{P_S}{P_L + P_{\text{losses}}} \tag{26}$$

according to the power flow direction. $P_{\text{losses}} = P_{\text{Switch}} + P_{\text{Inductor}} + P_{\text{Snub}} + P_{\text{Cap}}$ takes into account the semiconductors switching and conduction losses, $P_{\text{Switch}}$, the coupled inductor's winding and core losses, $P_{\text{Inductor}}$, and the primary side snubber losses, $P_{\text{Snub}}$, as well as the capacitor losses, $P_{\text{Cap}}$, according to the specifications of the selected components for the design, which are listed in Table IV, and to (21), (22), and (24).

TABLE IV
PROTOTYPE SELECTED COMPONENTS

| Component | Value |
|---|---|
| S1 | G3R160MT17D |
| S2 | NVH4L020N120SC1 |
| $D_{sn}$ | STPSC10H12B2-TR |
| $L_{in}$ | 22 $\mu$H |
| $C_i$ | 12 $\mu$F, 630V |
| $C_o$ | 22 $\mu$F, 450V |
| $C_{sn}$ | 44 nF, 1700V |
| $R_{sn}$ | 14 k$\Omega$ |
| Gate Drivers | ISO5852S, 1.5A |
| Core | EPCOS B65713A0400A027 |
| Magnetizing Inductance | 1 mH |
| Turn Ratio 1:n | 1:0.5 |
| Primary leakage inductance | 17.85 $\mu$H |
| Switching frequency | 50 kHz |
| Grid voltage | 700 V |

The primary side of the coupled inductor measured, through an impedance analysis at 50 kHz, an equivalent series resistance (ESR) $\text{ESR}_{Lm}$ of 370 m$\Omega$, a secondary winding ESR $\text{ESR}_{L_{\text{sec}}}$ of 75 m$\Omega$, and a leakage inductance $L_{\text{leak}}$ of 17.85 $\mu$H. It is, thus, possible to express the coupled inductor losses as the sum of different related losses' contributions

$$P_{\text{Inductor}}^{\text{Primary}} = \text{ESR}_{L_m} \cdot \left( I_{\text{pri}}^2 + \frac{1}{12}\Delta_{I_{\text{pri}}}^2 \right) \tag{27a}$$

$$P_{\text{Inductor}}^{\text{Secondary}} = \text{ESR}_{L_{\text{sec}}} \cdot \left( I_{\text{sec}}^2 + \frac{1}{12}\Delta_{I_{\text{sec}}}^2 \right) \tag{27b}$$

$$P_{\text{Inductor}}^{\text{Snubber}} = \frac{1}{2 \cdot T_S} \cdot L_{\text{leak}} \cdot \left( I_{\text{pri}} + \frac{\Delta_{I_{\text{sec}}}}{2} \right)^2 \tag{27c}$$

$$P_{\text{Inductor}}^{\text{Core}} = V_{E_{\text{core}}} \cdot K_{\text{core}} \cdot f^{\alpha_{\text{core}}} \cdot \Delta B_{\text{core}}^{\beta_{\text{core}}} \tag{27d}$$

where $I_{\text{pri}}^{\text{rms}}$ and $I_{\text{sec}}^{\text{rms}}$ rms currents have been considered, and the relevant parameters can be expressed as

$$\Delta_{I_{\text{pri}}} = \frac{V_S \cdot D \cdot T_S}{L_m} \tag{28a}$$

$$\Delta_{I_{\text{sec}}} = \frac{(V_L - V_S) \cdot D' \cdot T_S}{L_{\text{sec}}} \tag{28b}$$

$$\Delta B_{\text{core}} = \sqrt{\frac{\Delta_{I_{\text{pri}}}^2 \cdot L_m}{A_{C_{\text{core}}}^2 \cdot R_{\text{core}}}} \tag{28c}$$

$$R_{\text{core}} = \frac{l_{\text{core}}}{\mu_e \cdot A_{C_{\text{core}}}} + \frac{l_{\text{gap}}}{\mu_0 \cdot A_{C_{\text{core}}}}. \tag{28d}$$

The core parameters, thus, are $A_{C_{\text{core}}} = 0.00091$ m$^2$, $V_{E_{\text{core}}} = 0.000133$ m$^3$, $l_{\text{core}} = 146$ mm, $l_{\text{gap}} = 3.5$ mm, $K_{\text{core}} = 71.305$, $\alpha_{\text{core}} = 1.1$, $\beta_{\text{core}} = 2.3$, and $\mu_e = 2000 \cdot \mu_0$.

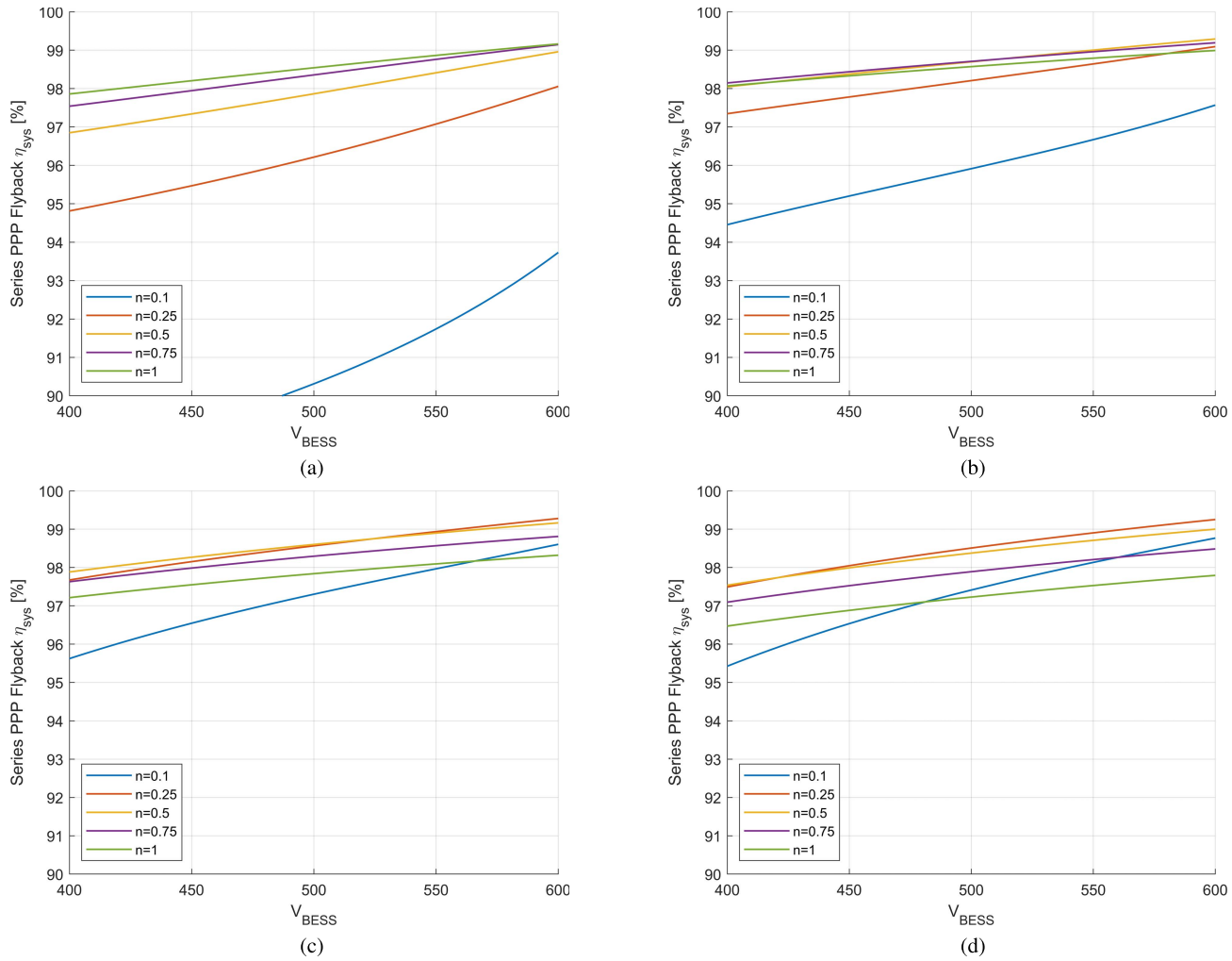



Fig. 7. Series PPP flyback analytical conversion efficiency with turn ratio comparison. (a) $I_{\text{BESS}} = 1$. (b) $I_{\text{BESS}} = 3$. (c) $I_{\text{BESS}} = 7$. (d) $I_{\text{BESS}} = 10$.

The output capacitor losses can be written as

$$P_{C_o} = I_{C_o}^{\text{rms}\,2} \cdot \text{ESR}_{C_o} = \left(\frac{1}{\sqrt{12}}\frac{I_L}{D'}\right)^2 \cdot \text{ESR}_{C_o} \tag{29}$$

where $\text{ESR}_{C_o} = 1.25\ \text{m}\Omega$ is obtained as a result of the parallel connection of 12 "TDK-CKG57NX7T2W225M500JJ" ceramic capacitors used in this design in order to fulfill dc bias, temperature, and frequency deratings.

The switches losses can be evaluated as sum of conduction $P_{\text{cond}}^{S_i}$, switching $P_{\text{sw}}^{S_i}$, and gate $P_{\text{gate}}^{S_i}$ losses contributions

$$P_{\text{cond}}^{Si} = R_{\text{DS}_{\text{ON}}}^{S_i} \cdot I_{\text{DS}_{\text{rms}}}^{S_i^2} \tag{30a}$$

$$P_{\text{sw}}^{Si} = \frac{V_{\text{DS}}^{S_i} \cdot I_{\text{DS}_{\text{peak}}}^{S_i} \cdot Q_{\text{ISS}}^{S_i}}{T_S \cdot I_G^{S_i}} \tag{30b}$$

$$P_{\text{gate}}^{Si} = \frac{V_{\text{GS}}^{S_i} \cdot Q_{G_{\text{TOT}}}^{S_i}}{T_S} \tag{30c}$$

where $Q_{\text{ISS}}^{S_i} = C_{\text{ISS}}^{S_i} \cdot V_{\text{GS}}^{S_i}$, and the design parameters are $V_{\text{GS}}^{S_i} = 15$ V, $I_G^{S_i} = 1.5$ A, $R_{\text{DS}_{\text{ON}}}^{S1} = 200\ \text{m}\Omega$, $R_{\text{DS}_{\text{ON}}}^{S2} = 30\ \text{m}\Omega$, $C_{\text{ISS}}^{S1} = 854$ pF, $C_{\text{ISS}}^{S2} = 2.943$ nF, $Q_{G_{\text{TOT}}}^{S1} = 29$ nC, and $Q_{G_{\text{TOT}}}^{S2} = 220$ nC. The switches rms and peak currents, as well the drain–source voltages, can be expressed as

$$I_{\text{DS}_{\text{rms}}}^{S1} = \sqrt{I_{\text{pri}}^2 + \frac{1}{12}\Delta_{I_{\text{pri}}}^2} \tag{31a}$$

$$I_{\text{DS}_{\text{rms}}}^{S2} = \sqrt{I_{\text{sec}}^2 + \frac{1}{12}\Delta_{I_{\text{sec}}}^2} \tag{31b}$$

$$I_{\text{DS}_{\text{peak}}}^{S1} = I_{\text{pri}} + \frac{\Delta_{I_{\text{pri}}}}{2} \tag{31c}$$

$$I_{\text{DS}_{\text{peak}}}^{S2} = I_{\text{sec}} + \frac{\Delta_{I_{\text{sec}}}}{2} \tag{31d}$$

$$V_{\text{DS}}^{S1} = V_S + \frac{V_L - V_S}{n} \tag{31e}$$

$$V_{\text{DS}}^{S2} = (n-1)V_S + V_L. \tag{31f}$$

According to what has already been thoroughly discussed, the definition of the turns ratio of the flyback coupled inductor involves different tradeoffs in the PPP converter design. Thus, different turn ratios have been compared, as shown in Fig. 7, for the system's efficiency evaluation. With lower turn ratios, e.g., $n = 0.1$, the efficiency is lower due to the higher currents in the primary and secondary transformer windings. On the other hand, higher turn ratios, e.g., $n = 1$, may offer higher conversion efficiency with lower currents, such as the case of $I_{\text{BESS}} = 1$. However, high turn ratios lead to high

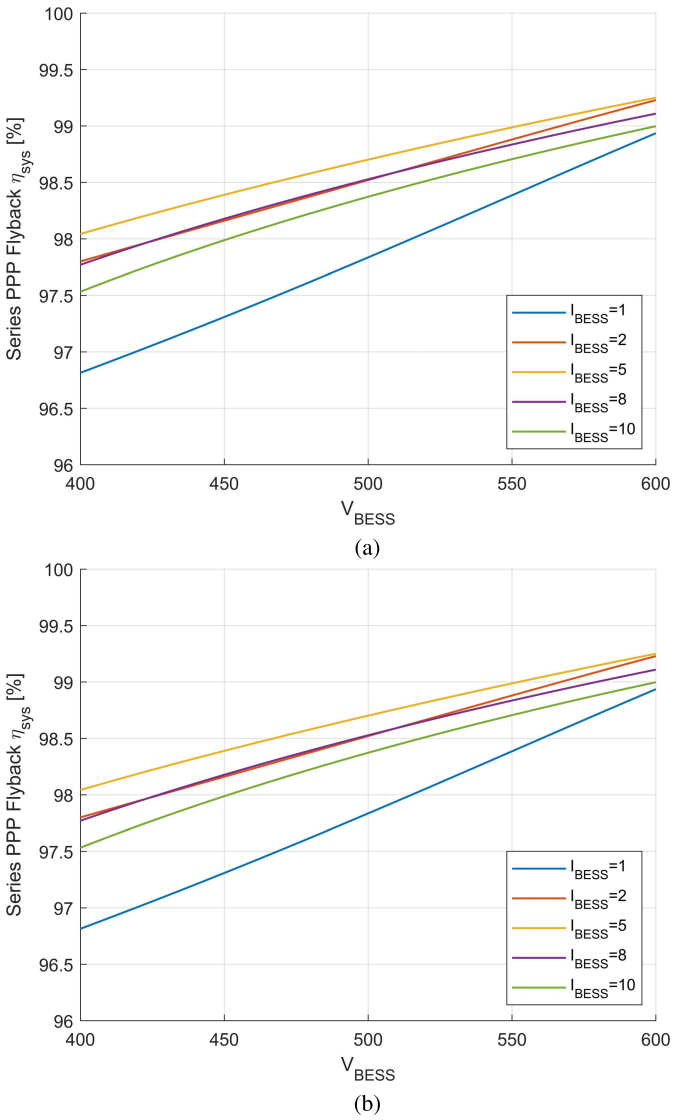



Fig. 8. Series PPP flyback analytical conversion efficiency with a turn ratio of $n = 0.5$. (a) Conversion Efficiency—BESS source. (b) Conversion efficiency—BESS load.

applied voltage stresses, reducing the advantages of the PPP circuit concept. Accordingly, the turn ratio $n = 0.5$ has been chosen, as it provides the best tradeoff between efficiency and components applied voltage stress within the required current loads and voltage range for the specified converter design.

The resulting system efficiencies, with the chosen turn ratio $n = 0.5$, are, thus, plotted for both power flow directions in Fig. 8.

## IV. Prototype Measurements

According to the design, a 5.5-kW (550 V/10 A) flyback converter in series PPP configuration has been implemented, as shown in Fig. 9.

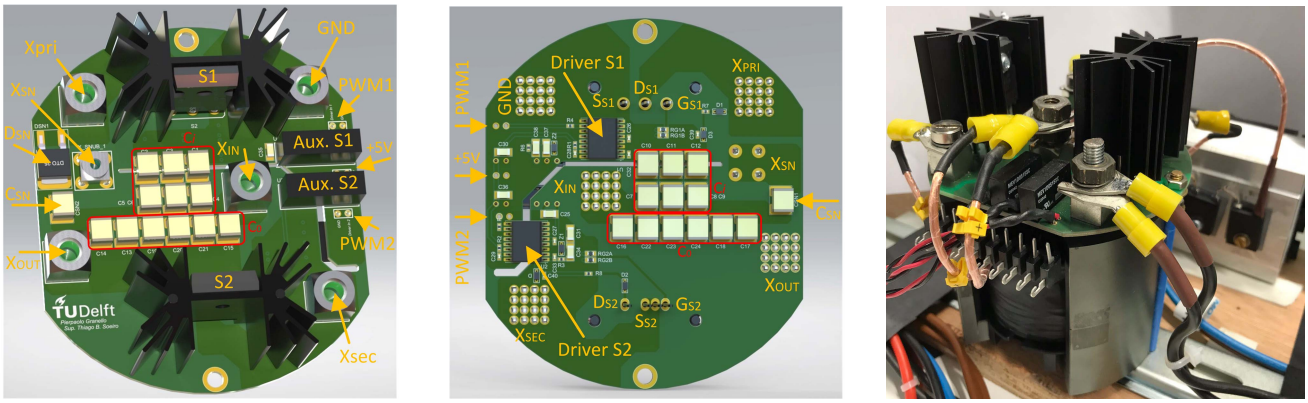
This circuit has been tested with a 50-kHz switching frequency to assess the system's conversion efficiency within the BESS voltage and power range specifications while interfacing a 700-V dc grid. This converter has been designed to be modular as part of a power electronics building block (PEBB) to be used in future research, and the snubber resistor is connected externally through screw points, while the snubber diode and capacitor are onboard. Murata MEV1D0515SC is used onboard, as shown in Fig. 9(a), to provide the auxiliary power supplies, +15 and −5 V, to correctly drive the SiC switches S1 and S2, from a common input of +5 V, which is provided from an external power supply. Input $C_i$ and output $C_o$ capacitors are distributed on both top and bottom layers. In particular, the input capacitors are doubled in series to fulfill the voltage requirements. A board cutout has been designed to provide isolation for the external driving signals and the +5-V supply voltage. Finally, the PCB is mounted on top of the coupled inductor to optimize the horizontal space, and the coupled inductor is connected through the provided onboard screw points.

Accordingly, the hardware setup and the connections diagram are shown in Fig. 10, where the current probe directions are shown. The dc grid voltage, $V_L$, the BESS voltage, $V_S$, and current measurements are carried out by the Yokogawa WT500 power analyzer to evaluate the system conversion efficiency, which has been accordingly set up based on the power flow direction. The switches drain to source voltages and currents are measured by a Yokogawa DLM 2034 oscilloscope.

Experimental measurements have been carried out in both power flow directions, assessing, thus, both the BESS charging and discharging conversion efficiencies. The power analyzer and the oscilloscope screens highlighting the maximum flowing power and the highest efficiency operating points are shown in Fig. 11. Note that the highest conversion efficiencies of 99.12% and 99.08% are found during the BESS charging and discharging phases, respectively, both with a battery voltage of 550 V and a current of 2 A.

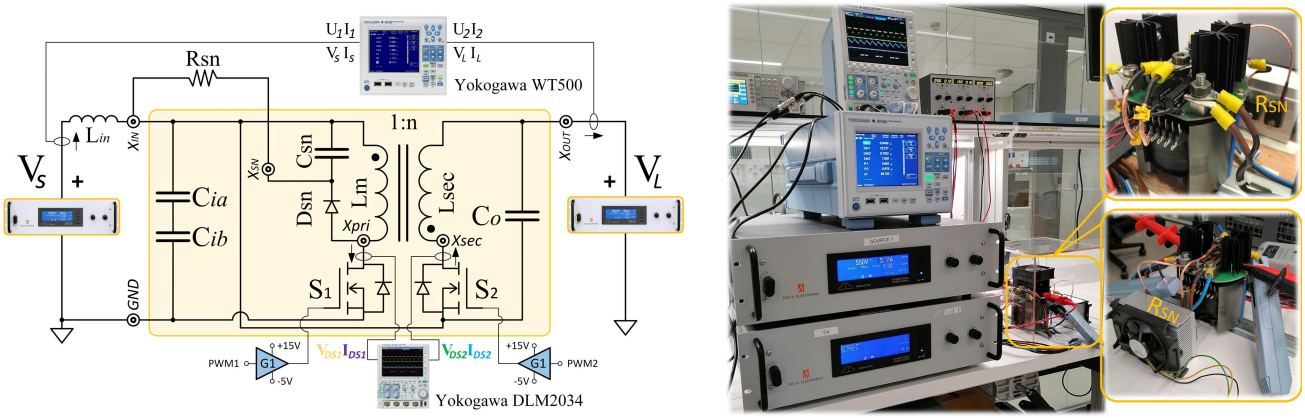
The measurements' results on the overall BESS voltage and current range have been processed and plotted in Fig. 12, and are comparable with the expected conversion efficiencies of Fig. 8.

It can be noted on the oscilloscope screens in Fig. 11, purple and blue waveforms, that the excursions of the coupled inductor currents are positive or negative basing on the BESS power flow direction, according to the measuring current probes directions as in Fig. 10(a). Indeed, according to Fig. 2 and to what has already been extensively discussed in Sections II and III, the current excursion on $Lm$ is positive (charging $Lm$) for a source-series PPP architecture [input current on the $V_1$ port as in Fig. 2 and $X_{\mathrm{IN}}$ side as in Fig. 10(a)], while it is negative (discharging $Lm$) for a load-series PPP architecture (output current on the $V_1$ port). Hence, the current on $L_{\mathrm{sec}}$ is positive (discharging $L_{\mathrm{sec}}$) for a source-series PPP architecture [output current on the $V_2$ port as in Fig. 2 and $X_{\mathrm{OUT}}$ side as in Fig. 10(a)], while it is negative (charging $L_{\mathrm{sec}}$) for a source-series PPP architecture (input current on the $V_2$ port). Finally, according to (16) and (20), as plotted in Fig. 3(g) and (h), respectively, it is possible to evaluate the partial power, which is processed by the converter. A comparison between the expected results and measured ones is plotted in Fig. 13 in both power flow directions. It can then be positively noted that the power handled by the converter is always less than the power flowing to or from the BESS, assessing the partial power handling and the analytical modeling of the architectures.



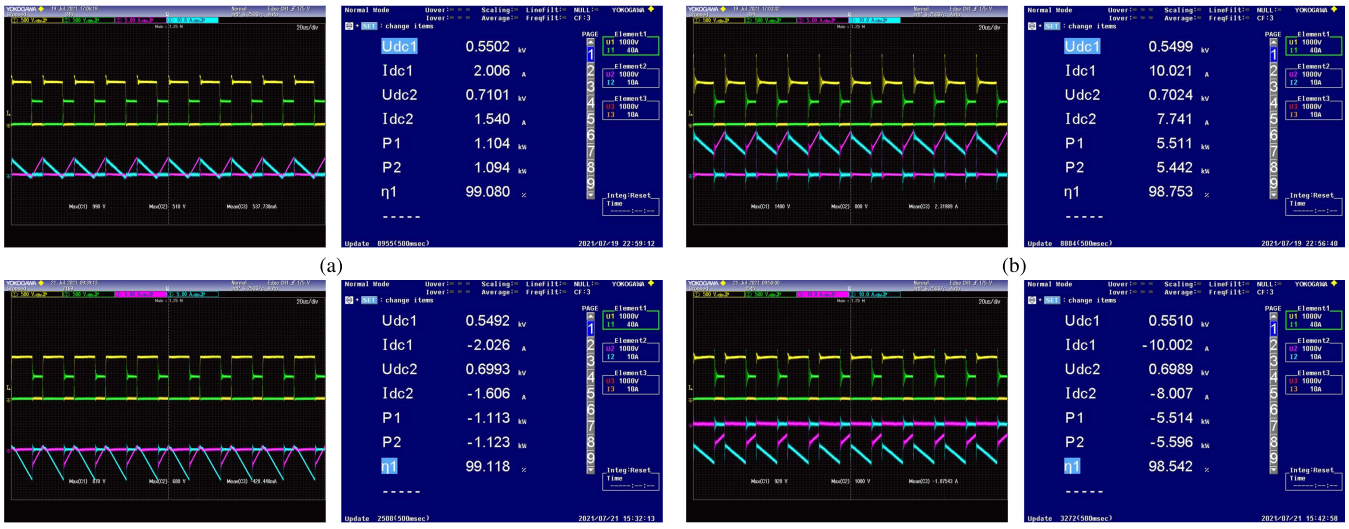

(a) (b) (c)

Fig. 9. Prototype designed PCB. (a) Top view. (b) Bottom view. (c) Prototype.




(a) (b)

Fig. 10. Measurements setup. (a) Setup drawing. (b) Setup picture.




(a) (b) (c) (d)

Fig. 11. Oscilloscope and power analyzer relevant measurements. (a) BESS source 2 A–550 V. (b) BESS source 10 A–550 V. (c) BESS load 10 A–550 V. (d) BESS load 10 A–550 V.

## V. Conclusion

This article proposed an analytical methodology to evaluate the system's conversion efficiency and the partial power processed by the dc/dc converter in the two main PPP architectures known in the literature: the series and parallel technologies. Results obtained with the derived analytical models are, thus, compared, assessing the series architecture as the most efficient partial power conversion solution with no limit on the system's voltage gain. A well-known, simple, and cost-effective flyback topology has, thus, been designed

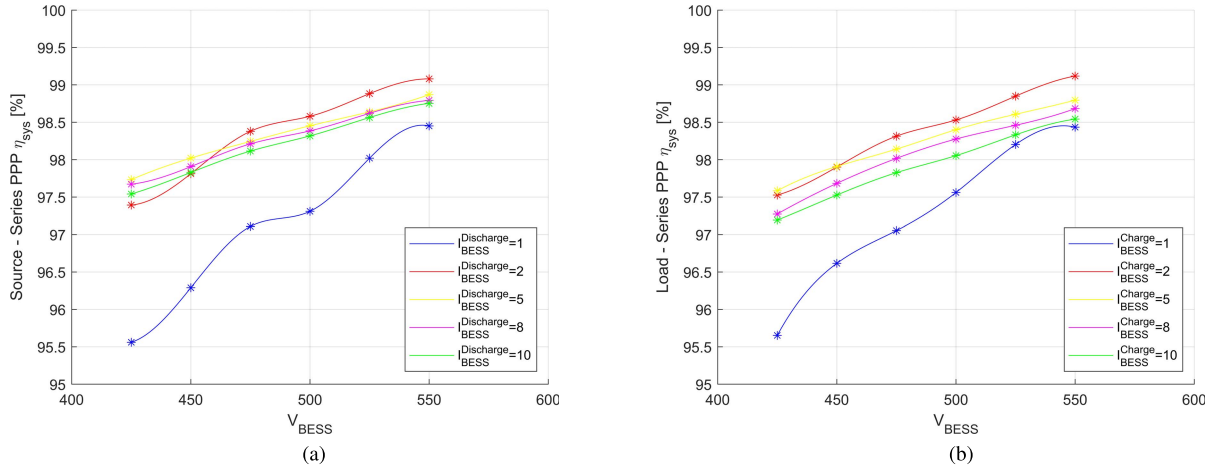



Fig. 12. Series PPP flyback conversion efficiency—fitting of the experimental measured results. (a) Series PPP flyback—BESS source. (b) Series PPP flyback—BESS load.

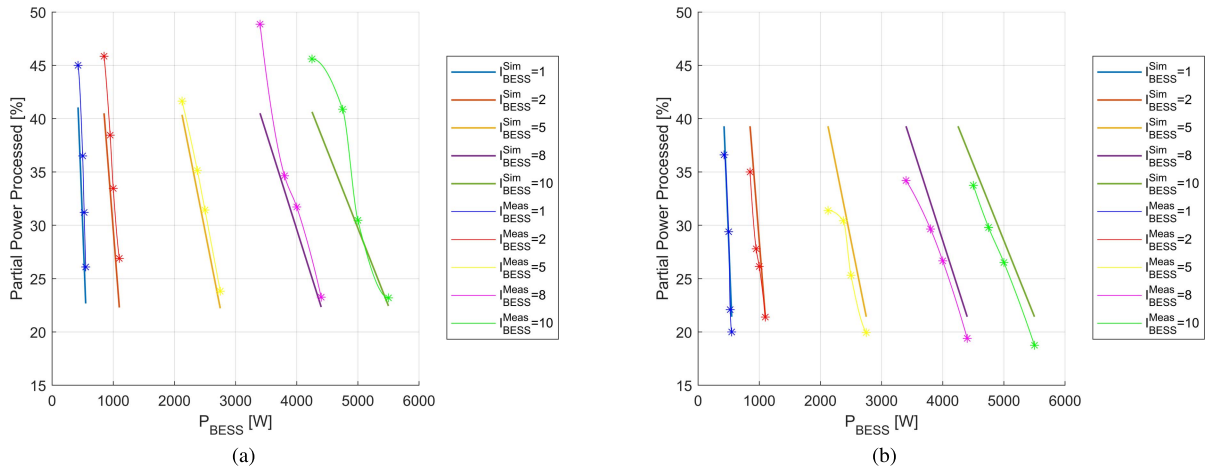



Fig. 13. Series PPP flyback partial power processed—comparison of analytical and experimental fit results. (a) Series PPP flyback—BESS source. (b) Series PPP flyback—BESS load.

and tested for verifying the developed study and configured as a series PPP architecture to interface a 5-kW BESS to a 700-V dc grid. The proposed design approach outlined the advantages of this PPP circuit concept, namely, the lower components' applied voltage stress due to the series connection and the lower requirement for the input and output filtering sizes, which further increases the power density of the system. Finally, the hardware setup measurements verified the accuracy of the developed analytical models in terms of system conversion efficiency as a function of the power flow direction and the partial power, which is processed by the converter.

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