Delft University of Technology

Design of a Zero voltage switching Flyback synchronous rectification controller for high voltage applications

Msc Final Project

Gaetano Nahar

Thesis committee:
prof.dr.eng. J. A. Ferreira
Dr.J.Popovic
Ir.F.Pansier
Dr.ing. J. L. Jose Rueda Torres
J.kloet

Abstract

The recent launch of high voltage switching devices of new semiconductor materials such as Silicon Carbide, have shown better performance. This makes it possible to use the single stage Flyback converter for low to moderate power, high input voltage applications, which is attractive due to its inherent advantages of low cost and simplicity. However, the losses in the Metal-Oxide-Semiconductor-Field-Effect Transistor (MOSFET) are aggravated due to the high input voltage, which decreases the efficiency. Additionally, the losses in the secondary diode can be considerable, thus deteriorating the efficiency further.

With the current trend towards high power density converters, the replacement of through hole component with surface mounted technology (SMT) components for the active devices is often the solution, under the condition that they require minimal thermal management i.e. using SMT components with minimal footprint without heat-sinks. In the light of thermal management it is important to reduce the losses in the active components, thereby effectively decreasing the generation of heat. Therefore, the objective of this thesis is to design a high power density 40W flyback converter by reducing the losses in the active components.

First the nature of the losses are identified theoretically and afterwards the results are verified experimentally. It was found that the switching losses in the primary MOSFET and the conduction losses in the secondary diode are the major loss contributors. To reduce both these losses a synchronous rectification controller was built which ensures zero voltage switching (ZVS) by making the converter bidirectional.

The experimental results show that for loads greater than 0.5 $I_{nominal,}$, the losses in the active components are reduced effectively to levels which allow the use of SMT component with minimal footprint. For light load conditions the converter showed erratic behavior due to the limited blanking time of the primary controller. To address this issue, a solution was proposed which has proven to work successfully for the voltage range of 400V-600V. Under a few special condition for voltages higher than 600V, the proposed solution has shown some erratic behavior, which is expected to be a result of the control loop stability.

Acknowledgements

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1 Contents

1 Introduction

Flyback converters are widely used as mains isolated converter for low to moderate power applications due to their inherent low cost, simplicity of design and intrinsic efficiency. Moreover, these converters provide isolation between the primary and the secondary side which makes them more attractive compared with other isolated topologies. This thesis deals with the design of a flyback which is intended to be used as auxiliary power supply . The auxiliary power supply is used to generate power for cooling fans, control logic and other equipment within the actual power supply. These converter are fed from the three phase mains after being rectified by a typical power factor front end rectifier. In such three phase applications, the high input voltage leads to some potential problems for the flyback converter. One of these problems is the limited availability of high blocking voltage switching devices which are able to provide sufficient margin in order to ensure reliability[31]. Moreover, these devices have high on-state resistance which deteriorates efficiency. Conventionally, two switch flyback converters were used to overcome these problem [1] at the expense of complexity among other problems. With the advent of high blocking voltage devices with low on-state resistance makes it possible to use single stage flyback converter which are far more attractive due to lower component cost and relative simple driving requirements. However, the high input voltage in the single switch topology can result in poor efficiency due to the following. Firstly, the high input can cause large peak voltage due to the leakage inductance of the transformer, voltage which in turn results in peak losses. This is not entirely correct, because the leakage inductance is not directly a consequence of the high input voltage, but more dependent on the transformer design. Secondly, the high input voltage translates into a high voltage stress of the primary switch which can cause considerable switching losses. The losses exhibited in the components leads to a temperature rise in the components as well as the printed circuit board (PCB) and therefore requires proper thermal management. This can be achieved by using heat-sinks and/or by increasing the PCB area at the expense of decreasing power density. The current trends towards high power density converters requires higher efficiency which enables cooling effort reduction [2]. In the Flyback converter the components responsible for producing heat are the primary switch , secondary diode and transformer. The primary switch and secondary diode are considered active components and usually demand the use of heatsink which reduces the power density. High power density can most often be achieved by using SMT components instead of conventional plated through hole components [3]. It is important to point out that SMT components only increase the power density when they do not require additional thermal management, that is they do not need require a larger cooling area than the (minimal) footprint they occupy. In other words, using SMT components should not divert the focus to thermal management. Recent developments in silicon technology have helped power Metal-Oxide-Semiconductor-Field-Effect Transistor(MOSFET)

manufacturers reduce the on state resistance to levels to the order of milliohms, which makes it attractive to use MOSFETs for rectification instead of diodes. Hence effectively reducing the conduction losses and improving efficiency and increasing power density. Besides, the use of MOSFET on the secondary side brings new possibilities for achieving zero voltage switching (ZVS) of the primary switch and thereby reducing switching losses. And the reason this is important is that it is pointless to put effort into finding devices with high blocking voltage capability with better performance, if the switching losses cannot be limited.

The main research question this thesis strives to answer: Is it possible to reduce the losses to the required level as to allow the use of SMT components for the active devices with minimal thermal management requirements, that is using SMT components with minimal footprint without heatsink.

A set of 2 sub question arose from the main question:

1. Which loss reduction techniques are best suitable for the converter at hand?
2. How does the transformer design affect the performance?

1.1 Design specifications

The specifications given below are established by Delta Elektronika , where the thesis project was conducted.

Design constraints:

- input voltage 400 - 800 V
  The power supply obtains its power from three phase mains which is first rectified by a frond end rectifier. The supply voltage ranges between 342VAC -562VAC which is rectified to 483.6V and 794.7V DC. Thus with the 400V-800V design, the whole input voltage range is covered.
- output voltage 13.5 V
  This power supply is intended to power different load which operate under different voltages. The idea is to make the output voltage of the power supply as to fulfill the requirement of the largest load . which is for this design the cooling Fan. The 13.5 volt is then further reduced by small commercial converters to provide the remaining loads which require less power.
- Maximum allowable voltage peak on the primary MOSFET is 1400V
  This maximum voltage is a design requirement given by Delta Elektronika in order to provide sufficient margin for the 1700V Silicon Carbide MOSFET .
- Output power 40W
  This reflect the power required to provide all the loads of the system.

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Design wishes:

- frequency 100 KHz but variable frequency allowed
- Maximum absolute hotspot temperature transformer 100˚C
  This temperature is chosen to allow sufficient margin under extreme operating and environmental conditions .

1.2 Objectives

The main goal of this thesis is to optimize a flyback converter to achieve high efficiency in terms of losses in the active components. The thesis particularly focuses on reducing the losses associated with the active devices in order to avoid the use of heat sinks. In this way it becomes possible to use active SMT components with minimal thermal management requirement.

1.3 Scope

Before proceeding further it is helpful to start off by defining the scope of this research. The scope of this research will be limited to the optimization of the losses in the active components. More specifically, the losses in the primary switch and secondary diode will be considered, whereas the optimization of the losses in the transformer is not part of this study.

1.4 Outline of thesis

Chapter 2 provides a brief introduction of the different operating modes of the flyback converter. Additionally a Flyback model for the discontinuous mode is presented , which is used in this thesis for converter analyses. The common faced challenges and solutions concerning the flyback transformer are discussed. To summarize, this chapter gives the required background for the understanding the design of a Flyback.

In chapter 3 the conventional design of the flyback including experimental results are presented. Various challenges were included and their solutions are discussed. Additionally, the theoretically expected losses are verified through in depth experiments. More importantly, from these results the major contributors of the losses are identified. In this respect, this chapter lays the fundament on which the rest of the thesis is built on.

Chapter 4 discusses the required strategy to reduce the losses which were identified in chapter 3. More specifically, the concept of synchronous rectification (SR) is introduced and discussed extensively. The theoretical expectations of the SR implementation are experimentally verified. Finally, an overview of the different zero voltage switching techniques is given.

In chapter 5 the design of the SR controller with the purpose of ZVS is presented. This chapter emphasizes on the operation of the controller on system level. Subsequently, the experimental verification of the design concept is shown .

In Chapter 6 the main conclusions of the research are presented and recommendations for future work are given.

2 Flyback State of the Art Techniques

The Flyback converter is one of the most widely used converters for low power application where isolation is required. The major advantage of this topology is that the inductor fulfills both the role of inductor and transformer, which reduces size and cost.

2.1 Operating modes

This paragraph discusses the various operating modes. The converter can be operated in different operating modes based on the requirements and application namely, continuous current mode, discontinuous current mode and boundary condition mode. These operating modes differ in both the manner that current flows and the instant the primary transistor is switched.

Continuous Conduction mode

In the Continuous conduction mode (CCM), the energy stored in the inductor is not completely transferred to the secondary. More specifically, during the secondary conduction cycle the current does not reach zero before the next switching cycle. The main characteristics of CCM are the relatively lower Peak current with correspondingly lower RMS currents. Due to the higher required inductance, more turns are required which in turn leads to higher resistance with corresponding higher losses. However, CCM requires a large inductor for this reason it is not suitable for the design at hand. Specifically, a large inductance comes at the expense of a large leakage inductance which combined with the high input voltage will cause severe voltage stress on the MOSFET. The consequences the leakage inductance has on the transistor peak voltage will be discussed in chapter 2.4.1. CCM also suffers from switching losses in the secondary diode due to the reverse recovery in the diode .

Discontinuous Mode

In Discontinuous mode (DCM) , the energy in the inductor is completely depleted before the next switch cycle. In this way, depending on the load requirements, the required energy is stored on a cycle to cycle basis. DCM has high peak currents which translate into higher RMS values but not more than a 15% increase compared to CCM [4]. Despite this relatively higher current , the winding losses in DCM are mostly lower due to the lower required number of turns[4]. Moreover, DCM operation has the advantages of zero reverse recovery of the secondary diode and a smaller transformer [5]. Partly due to the characteristics mentioned above, the DCM mode is preferred in the conventional design, which is also state of the art at Delta Elektronika.

Boundary Condition Mode

The boundary condition mode (BCM) is similar to DCM, in the sense that stored energy is depleted completely before the next switching cycle. Unlike in DCM, where the primary MOSFET is switched according to a fixed frequency, in the BCM the transistor is switched on as soon as the secondary current reaches zero. This in fact is the main difference compared to DCM where there is some "dead time" after the secondary current reaches zero. In BCM often some dead time is intentionally introduced by delaying the instant at which the transistor turns on in order to switch at it minimum voltage [5]. Obviously, the instant the transistor switches on varies with both the input voltage and load, thus variable switching frequency is necessary to keep switching at minimum input voltage. This operation mode offers the advantages of lower switching losses and lower electromagnetic interference (EMI) [5]. Drawbacks of BCM include those of DCM and poor efficiency at light load due to high switching frequency. It is worth mentioning that most integrated circuits(ICs) inherently have frequency clamping function built in. This function purposefully introduces (sufficient) dead time at light load condition. Consequently, the frequency is decreased which improves the efficiency.

DCM

At this point it is clear that CCM is not applicable for the application at hand. Therefore, the choice remains between DCM and BCM. DCM was chosen as a design starting point, because of its simplicity and the fact that it is state of the art at Delta Elektronika for auxiliary power supplies. In this respect, it makes sense to discuss this operating mode in depth. On the other hand the operation of DCM correlates close to that of BCM.

A simplified version of the Flyback converter is shown in figure 1. Note that the turns-ratio is not indicated in the figure. By looking at the operation of the Flyback under the assumption of ideal components, a better understanding can be obtained.

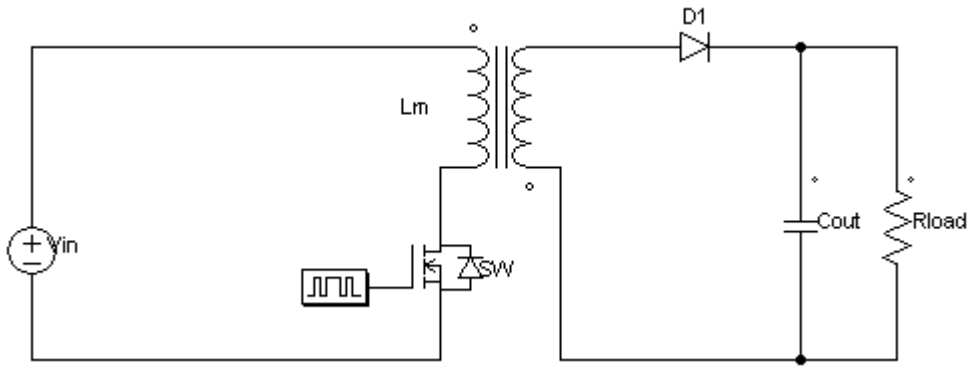


Figure 1 simple schematic of a Flyback converter .

During the on time of the MOSFET the current builds up in the primary and energy is stored in the inductance.

$$I_p(t) = \frac{V_{in}}{L}\ t \qquad 0\ \leq t \leq t_{on} \tag{1}$$

At the same time the diode on the secondary side prevents the inductor from discharging to the load. When the MOSFET is turned off, the inductance tries to resist the change of current by reversing the polarity of the voltage. As a result the diode in the secondary becomes forward biased and the stored energy is delivered to the load and output capacitor

$$I_p(t) = -\frac{V_{out}}{L}\ t \qquad t_{on} \leq t \leq t_{off} \tag{2}$$

The general equation for the stored energy in the inductor is given by:

$$E = \frac{1}{2} L_p \cdot {I_{peak}}^2 \tag{3}$$

Where :

$$V_{out} = the\ output\ voltage$$

$$t_{on} = the\ on - time\ of\ the\ MOSFET$$

$$t_{off} = the\ off - time\ of\ the\ MOSFET$$

$$I_{peak} = the\ peak\ current\ in\ the\ primary$$

$$L_p = the\ primary\ main\ inductance$$

This equation links the amount of power required by the load to the necessary peak current. The operation of DCM is thus based on storing the demanded energy required by the load in

packages on a cycle to cycle basis. In this sense a higher load demands a higher peak current which translates into a longer on-time for the primary switch.

Note that the previous equations are solely valid for discontinuous and boundary condition mode.

2.2 Flyback model

In figure 2, the Flyback converter including its non-ideal(parasitic) components is shown. The MOSFET is modeled as a switch with the parasitic capacitance across it. And the transformer is modeled with it its parasitic capacitance $C_{transomformer}$ and (parasitic) leakage inductance $L_{leakage}$.

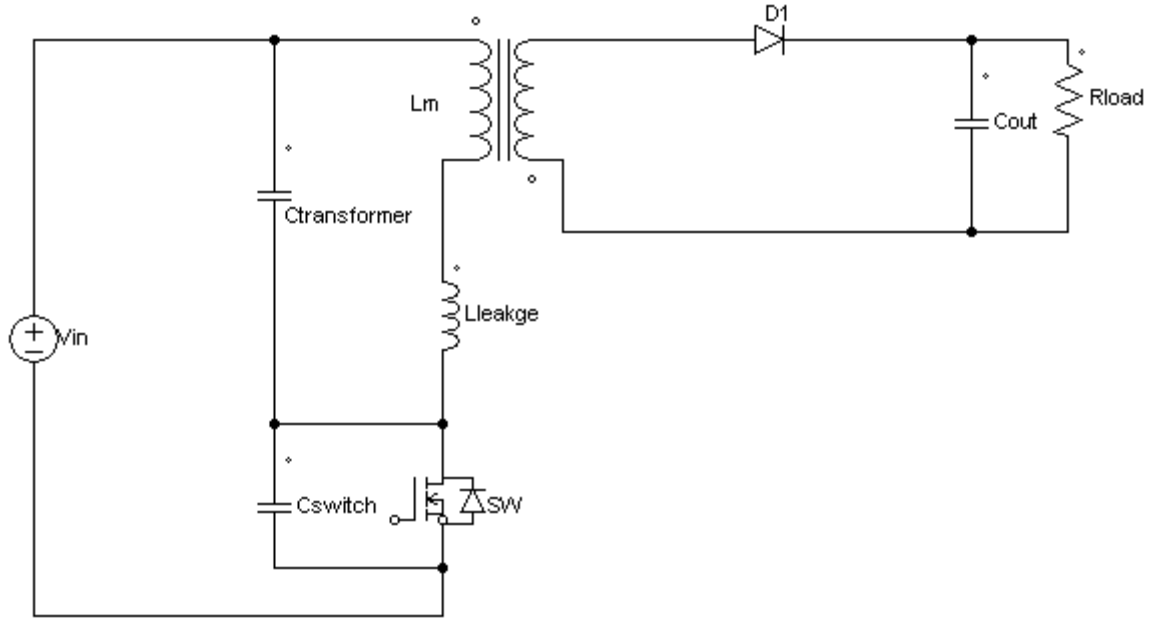


Figure 2 Flyback Model including parasitic elements

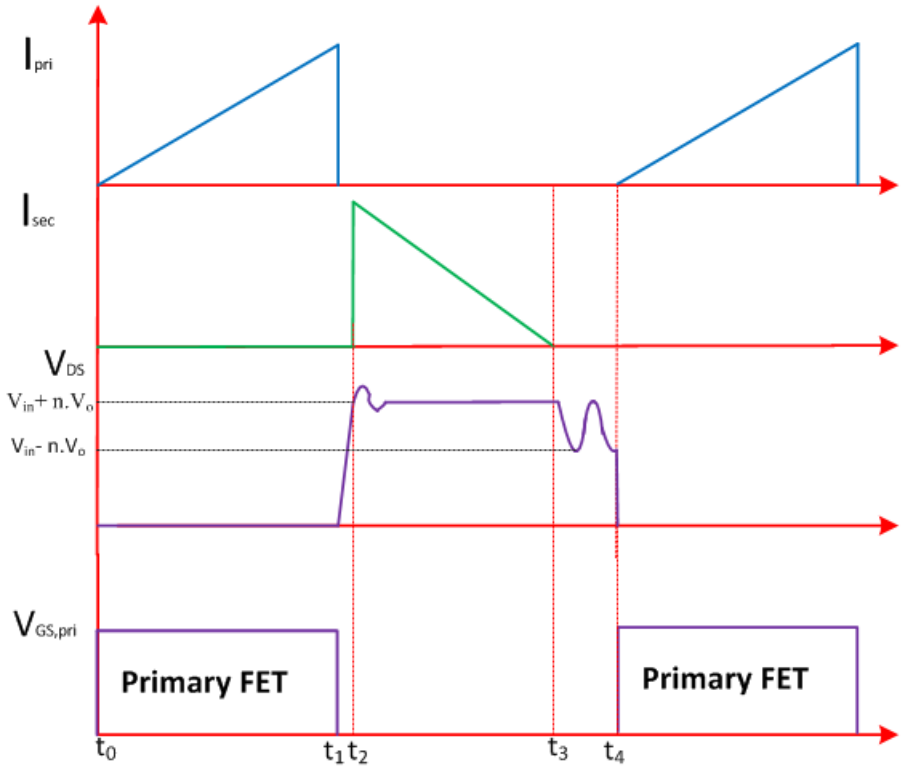


Figure 3 Shows the waveforms during steady state operation of Flyback in DCM

The steady-state operation is described as follows:

Mode 1: [t_0-t_1]

At t_0 the primary switch turns on and primary current increases linearly by equation 1.

This mode ends when the switch is turned off.

Mode 2: [t_1-t_2]

At t_1 the voltage across the switch V_{switch} increases linearly to $V_{in}+ n.V_o$ assuming the magnetizing inductance is large enough to ensure that the primary current is constant.

Mode 3: [t_2-t_3]

At t_2, the secondary diode starts to conduct .At this moment a resonance occurs between the leakage inductance and the equivalent capacitance C_{eq} seen by the switch. The equations describing the oscillations due to the resonance are given by [6]:

$$V_{c,eq}(t) = V_{in} - n \cdot V_o - \left(V_{in} + n \cdot V_o - V_{c,eq(0)}\right) cos\omega_0 (t - t_0) + Z_0 \cdot I_{L0} sin\omega_0 \, (t - t_0) \qquad (4)$$

Where: $C_{eq} = C_{switch} + C_{transformer}$

With the following initial values:

$$V_{c,eq}(0) = V_{in} + n \cdot V_0$$

$$I_{L0} = I_{peak}$$

$$\omega_{leak} = 2\pi f_0 = \frac{1}{\sqrt{L_s \cdot C_{eq}}} \qquad (5)$$

$$Z_0 = \sqrt{\frac{L_s}{C_{eq}}} \qquad (6)$$

$$V_{c,eq}(t) = V_{in} + n \cdot V_o + Z_0 \cdot I_{L0} sin\omega_0 \, (t - t_0) \qquad (7)$$

Based on the equations above the oscillations during the various resonant periods would be un-damped and continuous. To elucidate, In equation 7 the first two terms represent a DC component whereas the third component represent oscillating component which does not decrease in amplitude. In reality however, the oscillations are damped by several resistances including the winding of the transformer, the diode and the ESR of the output capacitor. The losses in the core also have some influence on the damping.

During this mode the current decreases from its peak value to zero according to equation 2. The current is composed of damped oscillating component superimposed on a linearly decreasing component. Note that oscillating term of the current is not shown in figure 3.

Mode 4: [t_3-t_4]

At t_3, the current in the secondary drops to zero as all of the energy is used. Subsequently, a resonance occurs between the L_m and C_{eq} according to [6]:

$$V_{c,eq}(t) = V_{in} - \left(V_{in} - V_{c,eq(0)}\right) cos\omega_0(t - t_0) + Z_0 \cdot I_{L0} sin\omega_0 (t - t_0) \tag{8}$$

With:

$$I_{L0} = 0$$

$$V_{c,eq}(0) = V_{in} + n \cdot V_0$$

$$Z_0 = \sqrt{\frac{L_P}{C_{eq}}} \tag{9}$$

$$\omega_{main} = 2\pi f_0 = \frac{1}{\sqrt{L_P \cdot C_{eq}}} \tag{10}$$

The voltage over the switch becomes

$$V_{c,eq}(t) = V_{in} + n \cdot V_0 cos\omega_0(t - t_0)$$

During this mode the voltage oscillates between $V_{in} - n \cdot V_0$ and $V_{in} + n \cdot V_0$

After this mode the transistor is switched on and the cycle repeats.

2.3 The Flyback transformer

In the Flyback topology the transformer is constructed as a multi-turn inductor wound on a common core. This transformer has the task to store energy from the input during the on-time and provide it to the output during the off-time as well as to provide galvanic isolation. Since these two benefits are provided by only one magnetic component it generates a simple and low cost design. The optimization of a transformer depends on the requirements of the application. Many efforts have been made to address the optimization with respect to high frequency losses, effect of gaps and tradeoff between cost and loss [7]

As previously mentioned the design at stake deals with a high input voltage, combined with the leakage inductance results in severe stress on the switch. Therefore, in this study the transformer is designed focusing on the reduction of leakage inductance. If these measures are insufficient, clamping or snubber techniques are considered necessary. Because the converter is intended to serve as an auxiliary power supply, it is important to ensure reliable operation. In this respect the primary design goal is to limit the temperature rise of the transformer.

2.3.1 Transformer design

The transformer is one of the crucial components in the design of the Flyback converter. As mentioned earlier, the transformer design at hand will focus on the leakage and hotpot temperature rise , instead of focusing on the optimization of the size.

The thermal design requirement limits the temperature rise in the transformer to a maximum level of approximately 30°C above ambient. This temperature rise is justified by the following assumption : The transformer is considered to operate at a 50˚ C room temperature, with a 20 ˚ C temperature rise due to the warming of other components. Accordingly, the design wish is to limit the absolute operating temperature to 100˚C. It should be pointed out that in general transformers are may be allowed to operate at higher temperatures dependent on the material and the relative safety standard . For this reason the restriction in this design should be considered merely as a design wish. This may lead to a overdesigned transformer, nonetheless this not an optimization criteria for this study.

Limitation of the allowable temperature rise is necessary to ensure reliable operation. This allowable temperature rise reflects the maximum amount of losses that are allowed, which in turn puts a constraint on the flux density and the thickness of the windings. More specifically, based on the allowed temperature rise of 30˚C and the thermal resistance of the selected core, the maximum losses within the transformer are calculated with:

$$P_{loss,max} = \frac{\left(T_{hotspot,max} - T_{ambient}\right)}{R_{th}} \tag{11}$$

Where:

$P_{loss,max} = the\ maximum\ allowable\ loss$

$T_{hotspot,max} = the\ maximum\ allowed\ hotspot\ temperature$

$T_{ambient} = ambient\ temperature$

$R_{th} = The\ thermal\ resistance\ of\ the\ core\ material\ of\ the\ transformer$

Based on the allowable losses, the flux swing is limited so that the core losses are within reasonable limits to leave a sufficient margin for the winding losses. Detailed calculations can be found in Appendix A.

The second aspect to be considered is the leakage inductance in the transformer, which is highly dependent on the winding arrangement and as a consequence on the physical design of the transformer. This leakage, present in both the primary and secondary, is that part of the flux which is not linked or mutual to both primary and secondary [8]. Furthermore, the leakage in one winding affects both the voltage in the semiconductors in that particular winding as well as the voltages in the semiconductor of the other winding [9]. One of the common ways to mitigate this troublesome parasitic is by interleaving the windings. In its simplest form the primary winding is split into two parts and then the secondary is positioned in between. As a result the secondary is “sandwiched" between the primary, significantly increasing the coupling. This gives a theoretical reduction of leakage inductance for more than 50% [9].

The distance between primary and secondary is also a factor which affects the leakage inductance. As the distance between two adjacent windings increases, the coupling decreases which results in a greater leakage inductance. Ideally, two adjacent windings would be placed right on top of each other with the intention of keeping the distance minimal. This complies with safety standard since triple insulated wire is used. However in practice it is difficult to wind on a layer which is rough due to the gaps between the turns. For that particular reason a couple layers of tape are placed to obtain a smoother surface. Accordingly the distance between windings increases, which deteriorates the coupling. Although not of primary interest it should be noted that increasing the distance between the windings, decreases the parasitic capacitance of the transformer. Thus the parasitic capacitance and leakage are inversely related, that is increasing one causes a decrease of the other [10].

Against this backdrop the transformer is designed on the basis of the guidelines provided by [11]. The specifications are summarized and shown in table 1. A complete overview of design steps and calculations can be found in the appendix A.

Frequency	100 KHz
Inductance L_p	2 mH
Transformation ratio n	16
Maximum allowable temperature rise	30°C

Table 1 summary of the required transformer specifications

For the purpose of convenience, the basic equations are shown here:

$$L_p = \frac{V_{in.min} \cdot D_{max}}{2 \cdot F_{sw}} \tag{12}$$

$$N_p = \sqrt{\frac{l \cdot L_P}{\mu \cdot A}} \tag{13}$$

$$n = \frac{N_p}{N_s} \tag{14}$$

2.4 Snubber techniques

In the previous paragraph it was pointed out that the transistor voltage stress can be reduced by mitigating the leakage inductance. As the reduction of the leakage due to interleaving has reached a plateau, clamping and snubber techniques are the only tool left. In this technique the leakage energy is stored and afterwards dissipated , returned to the input or used to achieve zero voltage switching.

Basically three different snubber techniques exists:

- Passive dissipative snubber
- Passive non-dissipative snubber
- Active networks

2.4.1 Passive dissipative snubber

The RCD snubber is widely used in Flyback converters, to limit the voltage spikes on the drain of the MOSFET [5]. The RCD snubber circuit is shown in figure 4. As the name suggests, this circuits consist of a resistor, capacitor and diode. When the MOSFET turns off, the drain voltage rises to $V_{in} + n \cdot V_o$ where the rate of rise is limited by the snubber capacitor. During this period some part of the current flows into the capacitor and is stored as energy. As soon as the switch turns on the energy stored in the capacitor is dissipated in the resistor. This method is quite popular because of its simplicity and low cost [12]. The main disadvantage is that the energy stored in the capacitor is dissipated in the resistor, which deteriorates the efficiency [13]. It is important to mention that several techniques could be used to increase the efficiency such as the use of a slow recovery diode for the snubber [4]. These techniques all have their limitation and are only effective with the right optimization which can complicate the design.

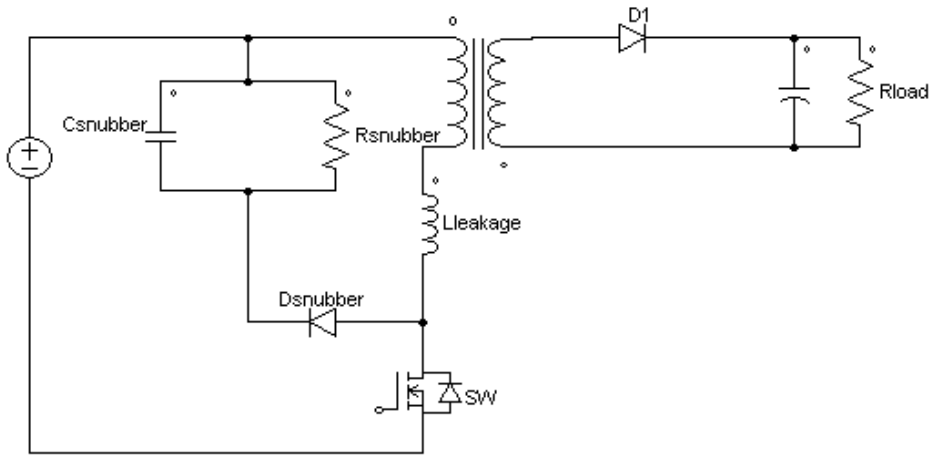


Figure 4 A typical scheme of a RCD Snubber in a Flyback converter

2.4.2 Passive non-dissipative snubber

To overcome the drawback of the RCD snubber, an LC snubber was proposed by [13], [14], [15]. The LC circuit is shown in figure 5. The operating principle can be explained as follows. The leakage energy is stored in the snubber capacitor during turn-off and recycled through the inductor to the input during turn-on [14]. In this way low voltage stress of the primary switch is achieved while remaining high efficiency.

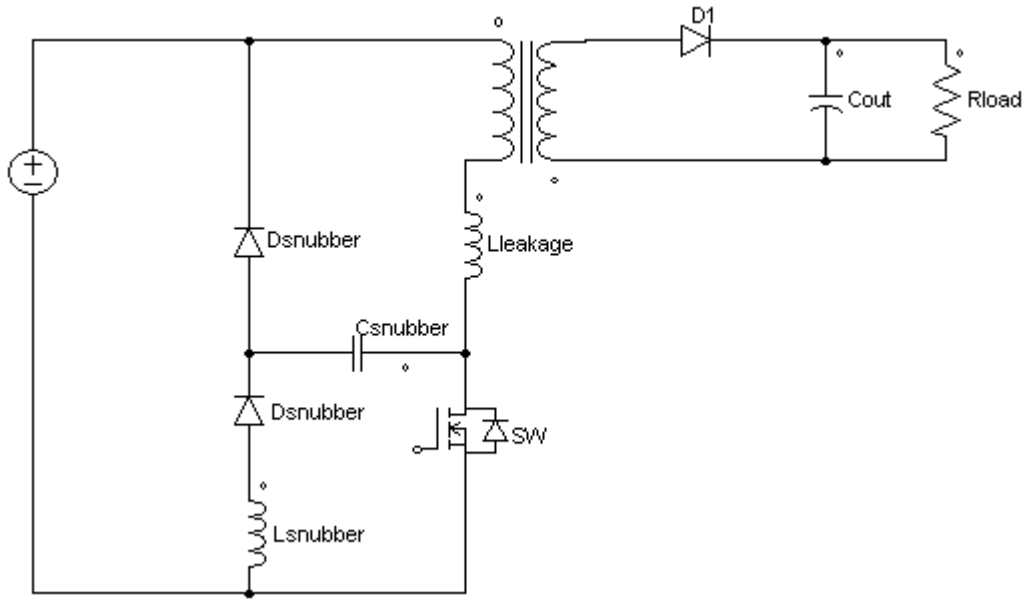


Figure 5 A typical scheme of LC snubber in a Flyback converter

2.4.3 Active clamp

The active clamp circuit is another method to eliminate the drawback of the RCD snubber. This scheme consists of an additional capacitor and switch. Similar to the lossless passive snubber, the leakage energy is stored and recycled to the input. Additionally, this scheme makes it possible to achieve soft switching. However, this technique requires auxiliary switching, drive and timing circuits and as a result increasing complexity and cost [13]

2.4.4 Summary

For the design, the non-dissipative passive snubber is chosen because of its simplicity and efficiency. A detailed analysis of the necessary design calculations can be found in [5].

2.5 Theoretical Loss estimation

The general idea of this work is to reduce the losses in the active devices in order to use SMT components. For this reason it is important to determine the breakdown of the losses. That is, it should be identified whether the losses in the active components are conduction- or switching losses or both. This determines which techniques should be applied to effectively reduce the losses.

Firstly, the losses in each component of the Flyback converter are calculated theoretically. These results are then compared with the experimental measurements in chapter 3. The following losses are considered:

- Conduction losses of transformer, MOSFET and diode
- Switching losses in the MOSFET
- core losses in the transformer

To estimate the worst possible losses, the converter is operated at its worst-case operating point. For the MOSFET this means the highest input voltage, while for the diode this corresponds to maximum load current. Due to the high input voltage, the input current is very small therefore it is expected that the conduction losses in the primary are negligible.

The switch on-voltage varies with load current therefore the operating point is chosen such that both maximum current and highest switch-on voltage are present. It should be noted that this operating point is not necessarily at the highest input voltage. From figure 24 and 25 in section 4.2 it can be observed that switch on voltage is dependent on the input voltage and the load current. The operating point is chosen in the following order: first the converter is set to operate at maximum load condition. Then the input voltage is varied near its maximum in such a way that the transistor switches on at maximum voltage. That is the voltage on the drain which, varies between $V_{in} + n \cdot V_o$ en $V_{in} - n \cdot V_o$ is consistently switched at $V_{in} + n \cdot V_o$.

2.5.1 Losses in the MOSFET

For the conduction losses in the MOSFET we need the root mean square (RMS) value of the current flowing through it. The conduction losses are then calculated as:

$$P_{switch,Conduction} = {I_{p,RMS}}^2 R_{ds,on} \tag{15}$$

$$P_{switch,Conduction} = 0.026\ W$$

Where $R_{ds(on)} = 1{,}5\Omega$ was taken from [16]. Since the on-state resistance increases with increasing temperature , the worst value is considered. That is the on-state resistance taken at 100˚C.

In every cycle energy is stored in the capacitance seen by the MOSFET, which has to be dumped and thus dissipated in the MOSFET at turn on. These losses correspond to the switching losses at the turn-on instant.

$$P_{switch,turn-on} = \frac{1}{2} C_{eq} V_{sw,turn-on,max}{}^{2} f_{sw} \qquad (16)$$

$$P_{switch,turn-on} = 2.32\ W$$

Where

$$C_{eq=} C_{transformer} + C_{switch} + C_{snubber}$$

$V_{sw,turn\ on}$	929.5V
$f_{sw=}$	100 Khz
C_{eq}	53.3 pF

Table 2 Operating condition of the measuring point

As put forward earlier, prior to turn-on, the voltage on the drain swings from $V_{in} - n \cdot V_o$ and $V_{in} + n \cdot V_o$. So, "minimum" switching losses can be achieved by turning the switch at $V_{in} - n \cdot V_o$. Because of this the losses in DCM vary greatly with the instant the transistor is switched on, which in turn is dependent on the input voltage and load condition.

By following the snubber circuit design procedure in [13] carefully, it was ensured that the snubber capacitor is completely discharged during the on-time of the FET. Consequently, at turn-off it can be assumed that all of the current flows through the snubber capacitor circuit resulting in zero turn-off losses for the primary switch.

2.5.2 The Diode losses

When the ideal is forward biased, the voltage across the diode is zero. However, we are dealing with a real diode which also has losses during the time it is forward biased. The losses in the diode are calculated as [17] :

$$P_{diode,losses} = \mathrm{V_f} \cdot \mathrm{I_{sec,av}} + R_d \cdot {I_{sec,rms}}^2 \quad (17)$$

With the following parameters :

$\mathrm{V_f}$	*0.51V*
$\mathrm{I_{sec,av}}$	*3A*
$I_{sec,rms}$	*4.3A*
R_d	*0.02*Ω

Table 3 Parameters for the diode loss calculation

$$P_{diode,losses} = 1.89\ W$$

3 Experimental design and results

The design phase starts with a calculation of the expected parameters in order to select components with proper ratings. Detailed calculations including the transformer design parameters can be found in the Appendix A .

3.1 Transformer measurement

Inductance measurement

After the physical construction of a transformer, the best way to verify the design is to take measurements. The leakage inductance can be measured by shorting the secondary winding and then measuring the inductance across the end of the primary winding. In this way, the coupled inductance is basically canceled out and the leakage (seen from the primary side) is measured [8]. As such the measurement generates the following results:

The primary inductance ($L_{m)}$	2,05 mH
The total leakage inductance ($L_{s)}$	60,3 µH

Table 4 Transformer inductance measurement

Capacitance measurement

The equivalent capacitance (seen by the primary MOSFET) is an important parameter because it is directly proportional to the switching losses. This capacitance can be obtained by measuring either the frequency of the ringing between the leakage inductance and capacitance or the ringing between the main inductance and capacitance [18]. Nevertheless, from a practical point of view, the ringing caused by leakage inductance is less complex to measure and for this reason employed in the following analysis.

From the measurements the equivalent capacitance is calculated with:

$$C_{eq} = \frac{1}{(2\pi \cdot f_{leakage})^2 \cdot L_{leakage}} = 53.3\ pF \tag{18}$$

Where:

$$L_{leakage} = 60\ \mu H$$

$$f_{leakage,osc} = 2.8\ MHz$$

3.1.1 Experimental result without interleaving

First, the transformer was built without interleaving from which drain voltage is shown in figure 6, where it can be observed that the peak voltage(blue) is around 1400V; hence the maximum voltage requirement is already *violated* at the lowest input voltage. It is also observed that the oscillations in the secondary current waveform are large in amplitude. As will be seen in chapter 4 these oscillations cause problems for SR implementation.

This can be verified theoretically by using equation (7):

$$V_{c,eq}(t) = V_{in} + n \cdot V_o + Z_0 \cdot I_{L0} sin\omega_0 \, (t - t_0)$$

With: $V_{in} = 400V$

$$I_{L0} = I_{peak} = 0.7A$$

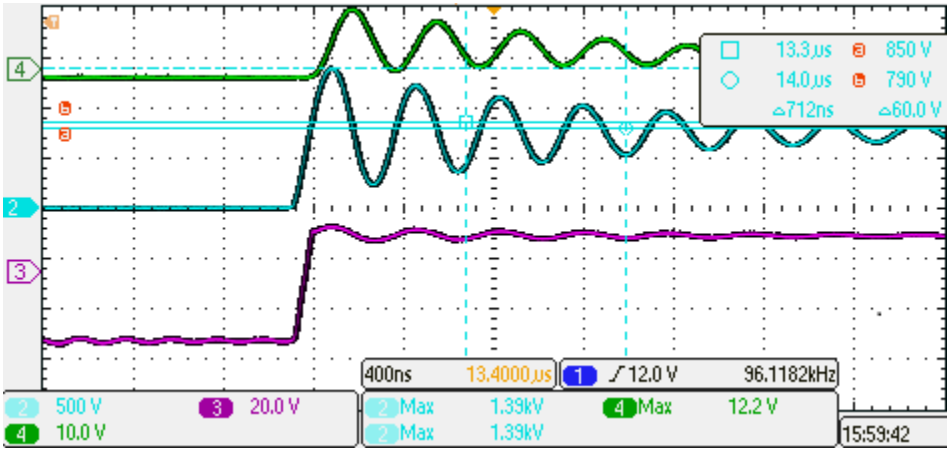


Figure 6 shows the voltage over the switch (blue), the secondary current (green) and voltage over the secondary winding (purple) without interleaving. Note how the peak voltage is almost 1400V with minimum input voltage

$$Z_0 = \sqrt{\frac{L_s}{C_{eq}}} = 1064\Omega$$

Taking into account the 0.5V forward voltage drop of the diode yield:

$$n \cdot V_o = 17 \cdot (13.5 + 0.5) = 238V$$

$$V_{c,eqmax}\left(t = \frac{1}{2}\pi\right) = 1382\ V$$

Thus, the theoretical voltage was found to be 1382V whereas the measured voltage was 1400V, therefore the experimental values closely match the theoretical values.

Peak current	0.7A
$V_{c,eqmax}$ theoretical	1382 V
$V_{c,eqmax}$ Experimental	1400 V

Table 5 comparison of result with normal transformer design

3.1.2 Experimental results with interleaving

From the experimental results in chapter 3.1.1 it is evident that the leakage inductance is problematic, therefore the transformer was interleaved. With interleaving a theoretical reduction of 50% was expected as mentioned earlier. However, only a reduction of 30% was obtained. This mismatch can be attributed to the following factors:

- The tape between the windings increases the leakage as mentioned in chapter 2.
- Since the secondary winding has only 8 turns it does not completely fill the bobbin. In order to minimize the leakage effects, the turns were spaced evenly across the layer. Nonetheless, air is still present between the windings, which creates a path for some leakage flux.

With the reduction of the leakage, a peak voltage of 1200 V was observed at 400V input voltage. In that respect the voltage was reduced by 200 V and the peak voltage design requirement is achieved but at *minimum input voltage.*

Theoretical verification similar to what was conducted in the 3.2.1 yields:

$$V_{c,eq}(t) = V_{in} + n \cdot V_o + Z_0 \cdot I_{L0} sin\omega_0 (t - t_0)$$

With: $V_{in} = 400V$

$$I_{L0} = I_{peak} = 0.7A$$

$$Z_0 = \sqrt{\frac{L_s}{C_{eq}}} = 868\Omega$$

$$n \cdot V_o = 17 \cdot (13.5 + 0.5) = 238V$$

$$V_{c,eq}\left(t = \frac{1}{2}\pi\right) = 1246\,V$$

Peak current	0.7A
$V_{c,eqmax}$ theoretical	1246 V
$V_{c,eqmax}$ Experimental	1200 V

Table 6 Peak voltage comparison with transformer interleaved

Hence, the observed voltage also matches the theoretical expectations.

Conclusion

The analysis shows that the theoretical expectations correspond to the expected values. Moreover, it is observed that the peak voltage can be reduced significantly by interleaving the windings of the transformer. It should be stressed that the peak voltage of 1200V after leakage reduction is observed only at minimum input voltage. Equation 7 indicates that the peak voltage increases as input voltage increases. Therefore, the peak voltage *at maximum input* (twice the input voltage) *would result in a high peak voltage* which would violate the design requirement.

3.1.3 Experimental result with passive non-dissipative snubber

In the previous section it was observed that the peak voltage at minimum input voltage was approximately 1246V. It should be emphasized that although this measured voltage is below the required 1300V, the condition is at 400V input voltage. Consequently, at 800V input voltage the peak voltage would exceed the required 1300V. As discussed in chapter 2.5 in such cases, clamping techniques are necessary. Specifically, the LC snubber discussed in 2.5.2 is used to decrease the peak voltage. For a matter of convenience the picture is repeated here

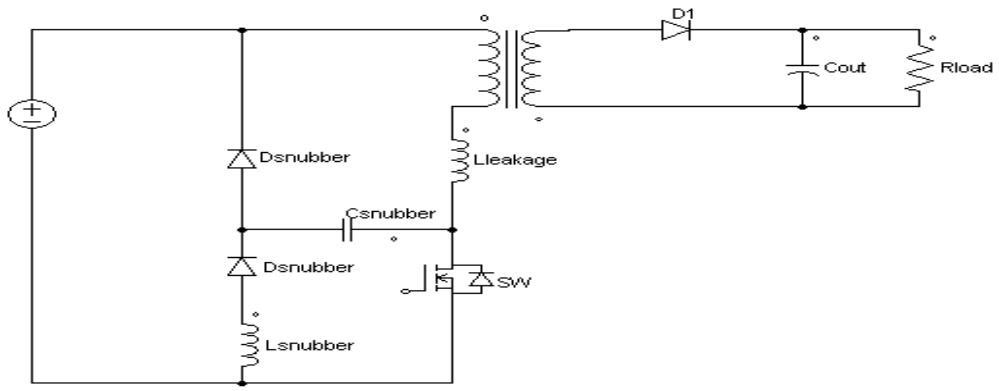


Figure 7 the passive non-dissipative snubber

Number of turns snubber($N_{snubber}$)	75
The snubber Capacitor ($C_{snubber}$)	1.5 nF

Table 7 Component specification of the snubber circuit

Minimum input voltage

The experimental results after implementation of the snubber circuit are shown in figure 8. It is observed that the peak voltage on the drain of the FET is approximately 800V at an input voltage of 400V. Hence the peak voltage requirements are satisfied at minimum input voltage.

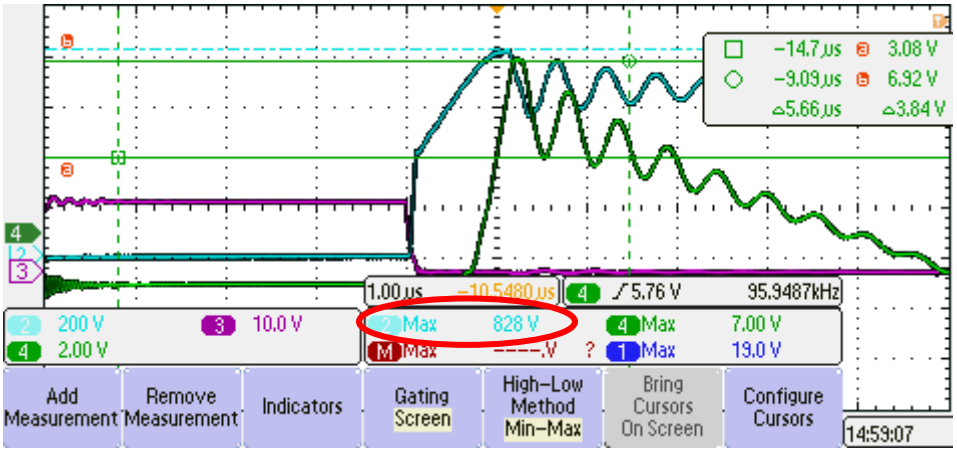


Figure 8 shows the voltage across the primary FET(blue), the secondary current (green) and the gate voltage (purple) with LC snubber implementation

Maximum input voltage

Figure 9 illustrates the waveforms at maximum input voltage, where it is observed that the maximum voltage on the drain is approximately 1300V. Hence the requirement of maximum allowable peak voltage on the primary switch is satisfied. The oscillations in the current of the secondary are also found to be significantly smaller, which is important for SR implementation as will be seen in chapter 4.

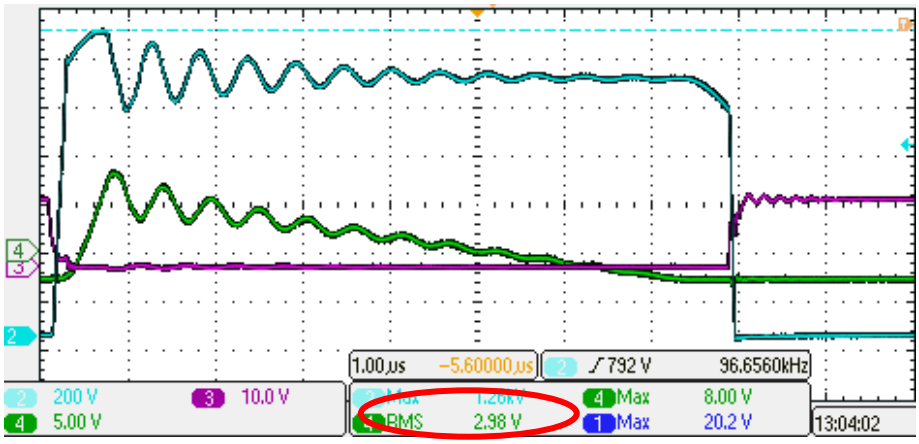


Figure 9 shows the voltage over the switch (blue), the secondary current (green) and the gate voltage winding (purple) with LC snubber

The results are summarized in table 8, where it can be seen that at both minimum and maximum input voltage the measured maximum voltage is below the maximum allowed voltage of 1300V, thus the peak voltage requirements are fulfilled.

Input voltage	$V_{c,eqmax,measured}$	$V_{c,eqmax,allowed}$
Minimum input Voltage	828V	**1300V**
Maximum input Voltage	1260V	**1300V**

Table 8 Peak voltage with LC at minimum and maximum input voltage

3.2 Loss estimation based on temperature measurements

When power components are operated they exhibit conduction and switching power losses. The heat generated as a result of these losses, needs to be conducted away from the chips into the environment by means of heat sinks. The heat generated at the chip causes a temperature drop from the chip towards the case. Infrared imaging methods take advantage of this temperature drop and provide flexibility to measure losses in power components. By using this method it is possible to accurately measure the hotspot temperature of components without physical contact. The basic limitation of infrared imaging makes it difficult to measure the temperature of reflecting metalized surfaces [19]. These surfaces reduce their infrared emission and "mix up" their field with stray emission from other reflective materials. Nonetheless, by taking measures such as covering reflective surfaces with tape or other material such as tipp-ex, reasonable measuring accuracy can be achieved.

By measuring the temperature at the case of the component equipped with the thermal resistance, the losses can be calculated by [6]:

$$P_{losses} = \frac{\left(T_{junction} - T_{ambient}\right)}{R_{total}} \tag{19}$$

It is important to note that this equation is valid for the static temperatures, that is the steady state temperature of the particular component. During the experimental measurements this is taken into account as follows by measuring the temperature constantly, until a steady state value is reached.

The thermal resistance of the individual layers affecting the thermal conduction, can be calculated with [6]:

$$R_{\theta paste} = \frac{d}{\lambda \mathrm{A_{eff}}} \tag{20}$$

Where:

$\mathrm{d} =$ is the length in meter

$\lambda = thermal\ conductivity$

$\mathrm{A_{eff}} = cross\ sectional\ area\ responsible\ for\ heat\ transfer$

3.2.1 Temperature loss estimation MOSFET

The steady state temperature measured at the case of the MOSFET was:

$T_{MOSFET=}$ 60° And $T_{ambient} = 22°$.

The MOSFET is mounted on an aluminium heat sink with an isolation pad and thermal paste in between. Figure 10 shows the different layers which affect the thermal conduction from MOSFET to heatsink. So the thermal resistances of the individual layers are calculated and then summed up, in order to calculate the thermal conduction.

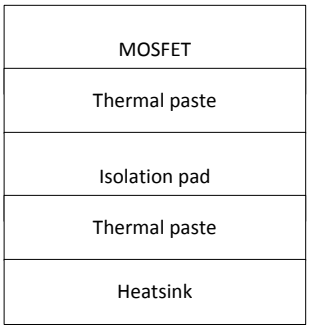


Figure 10 The thermal structure of the MOSFET mounted on the heatsink

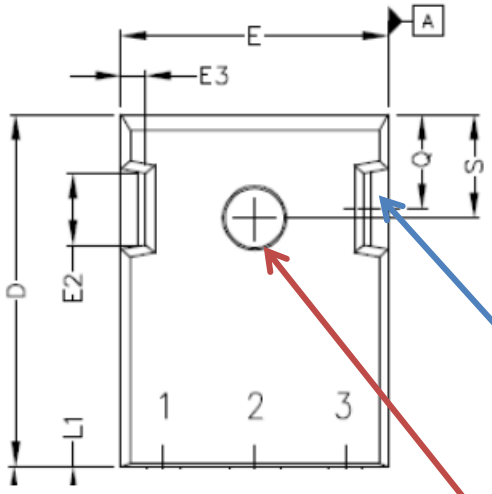


Figure 11 Package dimension of the MOSFET [23]

The effective area is the area enclosed by the paste isolation pad:

$$A_{effective} = Rectangular\ area - Circle - 2(small\ rectangles\ at\ the\ side)$$

The dimensions are obtained from [16].

$$A_{effective} = (20.8 \cdot 15.75) - (\pi \cdot (0.5 \cdot\ 3.51)^2)\ - 2(1 \cdot 3.68) = 310.5 \cdot 10^{-6}\ m^2$$

$$R_{\theta heatsink} = 18\ \text{C°/W}$$

$$R_{\theta paste} = \frac{d}{\lambda \mathrm{A_{eff}}} = \frac{20 \cdot 10^{-6}}{1 \cdot 310.5 \cdot 10^{-6}} = 0.06\ \text{C°/W}$$

$$R_{\theta isolation} = \frac{d}{\lambda \mathrm{A_{eff}}} = \frac{3 \cdot 10^{-3}}{3.5 \cdot 310.5 \cdot 10^{-6}} = 2.76\ \text{C°/}$$

$$R_{\theta Jc} = 1.7\ \text{C°/W}\ \ [16]$$

In fact these thermal resistances indicate the ability of the components to conduct heat .Since the heat flows from the MOSFET to heatsink, it has to pass al the thermal resistances. Thus, the total thermal resistance is found by taking the sum of the individual resistances :

$$R_{\theta total} = R_{\theta heatsink} + R_{\theta paste}\ + R_{\theta isolation}\ + R_{\theta paste}\ + R_{\theta Jc}$$

$$R_{\theta total} = 22.59\ \text{C°/W}$$

With equation(19) , the total losses are found as:

$$P_{mosfet,losses} = \frac{38}{22.59} = 1.68\ W$$

3.2.2 Temperature loss estimation diode

As seen in figure 12, the thermal structure of the diode is the same, so similar calculations can be done.

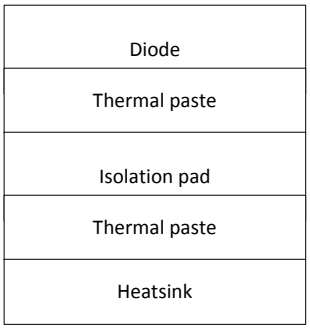


Figure 12 Thermal structure of the diode mounted on heatsink

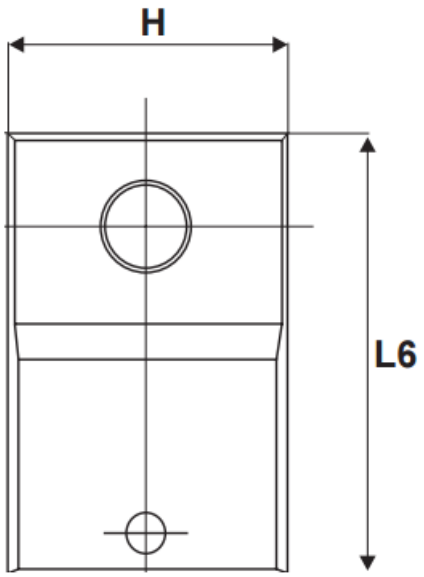


Figure 13 Package dimension of the diode [17]

The losses in the diode can be calculated in a similar manner. The effective area is the area enclosed by the paste and isolation pad :

$$A_{effective} = Rectangular\ area - Circle$$

$$A_{effective} = (15.9 \cdot 10.40) - (\pi \cdot 1.5^2) = 158 \cdot 10^{-6}\ m^2$$

Where dimensions are taken from [17]

$$R_{\theta paste} = \frac{d}{\lambda A_{\text{eff}}} = \frac{20 \cdot 10^{-6}}{1 \cdot 158 \cdot 10^{-6}} = 0.126\ \text{C°/W}$$

$$R_{\theta isolation} = \frac{d}{\lambda A_{\text{eff}}} = \frac{1 \cdot 10^{-3}}{3.5 \cdot 158 \cdot 10^{-6}} = 1.80\ \text{C°/W}$$

$$R_{\theta heatsink} = 27\ \text{C°/W}$$

$$R_{\theta Jc} = 1.3\ \text{C°/W}$$

$R_{\theta heatsink}$ and $R_{\theta Jc}$ are obtained from [20] and [17] respectively.

Similar, to the calculations in the previous paragraph we add the resistances :

$$R_{\theta total} = R_{\theta heatsink} + R_{\theta paste} + R_{\theta isolation} + R_{\theta paste} + R_{\theta Jc}$$

With equation (19) the losses in the diode can be found as:

$$P_{diode,losses} = \frac{40}{30.2} = 1.32\ W$$

3.2.3 Temperature loss estimation transformer

$$P_{transformer,losses} = \frac{\left(T_{junction} - T_{ambient}\right)}{R_{\theta th,core}} = \frac{46}{29} = 1.56\ W$$

Where : $R_{\theta th,core} = 29\ \text{C°/W}$ obtained from the application note EPCOS

The losses in the active components are summarized in table 8.

	Primary transistor	Diode	Total losses in the **active component**
Theoretical (electrically) measured losses	2.32 W	1.89 W	4.21 W
Experimental (thermally) measured losses	1.71 W	1.32 W	3.02 W

Table 9 Comparison of theoretical and experimental power losses in the active components

The total experimental losses have a deviation of 28% from the expected theoretical value. This discrepancy can be a result of various inaccuracies including :

- Inaccurate measurements due to measurement devices which are not calibrated
- Information from the datasheet is only accurate at the specified conditions of the manufacturer. This can differ from the conditions at which the above measurements are done.

3.3 Overview of the losses

From the analysis in 3.2 the following conclusions can be drawn;

- To approximate when it is suitable to use SMT components to achieve high power density the following conditions are defined:
    1. The ambient temperature is considered to be 50 °
    2. Minimal thermal management is required which means that the SMT component is able to remove its heat properly by using its minimal footprint.

    SMT components mounted using mounted with minimal footprint have a typical thermal resistance ranging between 50 and 100 C°/W [21]. By substituting these thermal resistance values and maximum allowable temperature rise of the active components to 50 degrees above ambient into equation 19, the maximum allowable losses in the active components are 0.5W. It should be noted that this 0.5W is not a definite condition but is only used as a guideline.

    From table 8 the losses in the active components which are 1.71 W and 1.31W in the FET and diode respectively, exceed the required level of 0.5W. Thus SMT components cannot be used without reducing the losses.

- Figure 14 provides a breakdown of the losses. It can be observed that the losses are more or less evenly distributed over the active components and transformer. Moreover, the losses in the active components on the secondary are solely *conduction losses* whereas in the primary transistor the *switching losses* dominate.

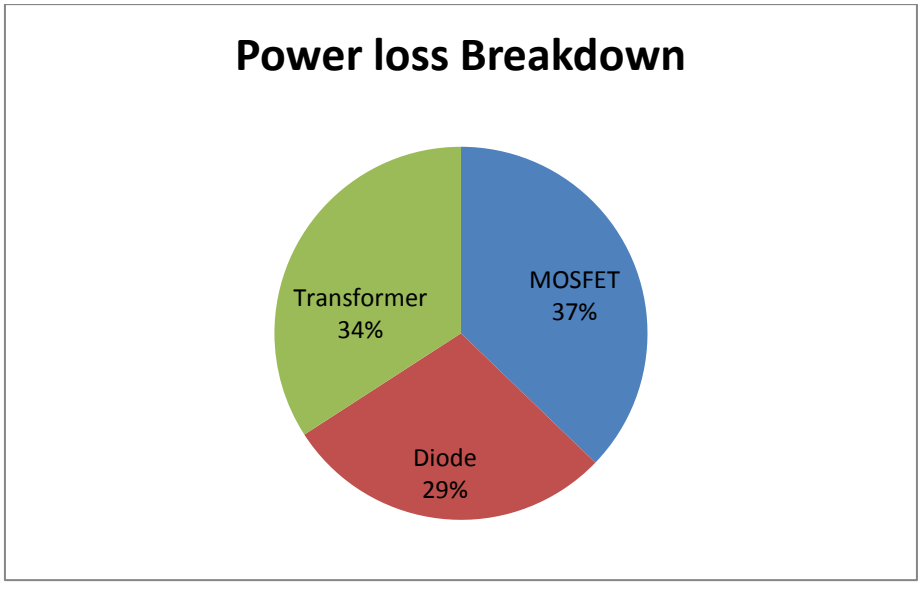


Figure 14 Power loss breakdown of the different components

4 Zero voltage switching and Synchronous rectification

4.1.1 Synchronous rectifier

In the previous chapter it became clear that a significant part of the total losses are the diode forward losses. Synchronous rectification is a technique to minimize these conduction losses, this technique implies the replacement of the diode by a MOSFET. The goal is to emulate the behaviour of the diode by properly driving the MOSFET. At low voltage rating MOSFETs are available with on-state resistance in the order of milliohms ,thereby reducing the conduction losses tremendously. In figure 15, the conduction losses in the diode and MOSFET are shown as a function of current. From the figure it is evident that the losses in the MOSFET are significantly lower before both graphs coincide, where they are equal. For the current range which is dealt with in this particular design, it can be assumed that the conduction losses in MOSFET are far lower than in the diode provided that the $R_{ds,on}$ is low enough(order of milliohms).

Although the previous arguments indicate that the SR rectification improves the efficiency , there is a "price" to be paid, that is increased complexity. Namely, the instant at which the controller turns on and off the MOSFET is important for both the efficiency and reliability. More specifically, turning the MOSFET on too late decreases the efficiency, meanwhile turning it on too early will cause cross-conduction. Therefore, the practical implementation of the SR concept certainly imposes challenges and requirements on the controller. These aspects are discussed in the next paragraph.

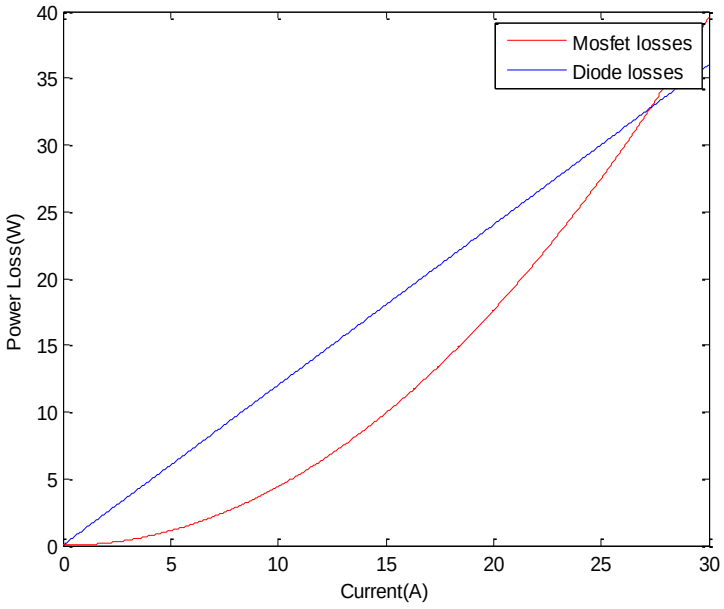


Figure 15 Comparison of the conduction losses in the SR FET and diode as a function of current

4.1.2 SR challenges and operation in Flyback circuit

The concept of SR is to use a MOSFET to mimic the operation of the diode. Figure 16 shows the power stage for the Flyback where the diode is replaced by SR MOSFET. Note that SR FET is positioned at the low side in order to use simple driving schemes. Although there are different gate drive control such as the use of current transformers etc., this study, focuses on the implementation of logic circuitry which drives the FET based on the drain-source voltage. Moreover, the operation of the SR technique differs depending on the operating mode. Logically, as the design deals with DCM/BCM operating modes, the challenges and principles of CCM are not discussed. For this reason it should be kept in mind that the analysis from here on is solely valid for the DCM/BCM operating mode.

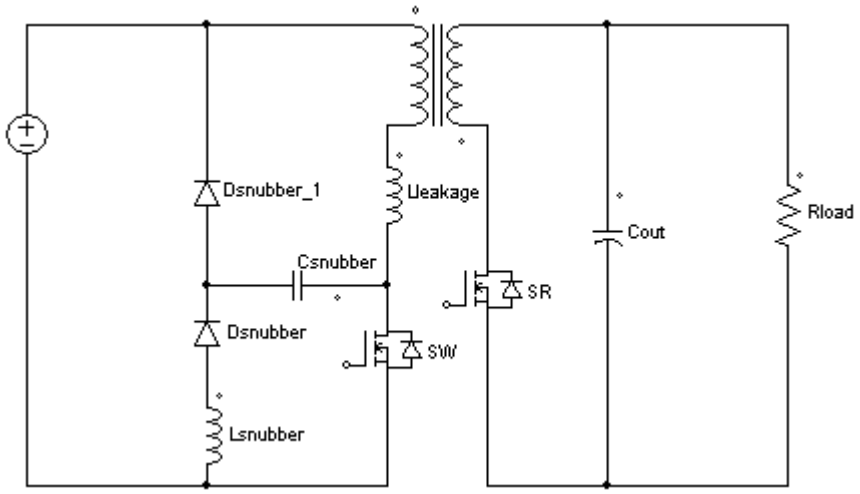


Figure 16 Flyback schematic with LC snubber with SR FET implementation

Challenges

Although, the concept of SR rectification is straightforward, driving the MOSFET properly is a challenging task for the controller. The main challenge is to drive the FET in such a way that it turns on immediately when the secondary current phase is initiated and immediately stops when the current is zero. In order to this the controller needs to be 'smart' enough to know when the gate should be driven high and low. As mentioned earlier, if the FET turns on too late the peak current will flow through the body diode for a non-negligible time, leading to poor efficiency. On the other hand, turning the FET too early causes cross-conduction leading to a short circuit with destructive consequences.

The same timing arguments apply for the turn off instant, but this is less critical as the current is already close to zero. If the FET is turned off too early, the body diode has to finish the current conducting cycle. On the other hand, turning the FET off too late will cause the current

to go negative. Under normal operation this is not desirable because the energy flow is then reversed which leads to an unnecessary increase in peak currents and corresponding losses.

Principle of operation

Proper operation of the SR is strongly dependent on the :

1. The turn-on phase
2. The turn-off phase

Turn-on

The key idea used in nearly all SR controllers is to sense the voltage across the drain and source. As the secondary conduction phase is started, current starts to flow through the body diode of the SR FET thereby causing a negative voltage. Since the voltage drop across the diode is relatively high compared voltage drop due to the on-state resistance $R_{ds,on}$ of the SR FET, the threshold V_{TH2} is triggered. Consequently, the controller turns on the SR FET by driving the gate high. As a result the current flows through the low resistance path which results in lower conduction losses and improved efficiency. It is important to note that the conduction time of the body diode, often referred to as dead time, should be minimized in order to maximize efficiency. Due to the parasitic elements significant ringing can occur at the turn on-instant(and a short period thereafter) which may possibly lead to unintentional turn-off. To overcome this effect, usually a minimum-on timer is built in, which ensures that the SR FET stays on for a pre-defined time. For this same reason it was mentioned in chapter 3, that the damping of the oscillations by snubber techniques is a requisite for correct SR operation.

Turn-off

As the current decreases , the voltage drop across the transistor reduces. As soon as the voltage becomes *greater* than V_{TH1} (in other words less negative), the driver output is pulled to ground. Consequently, the current flows through the body diode to finish the secondary conduction phase. Notice that when the FET is turned off, the voltage drop across the drain increases again due to the current flow through the forward biased body diode, which would trigger the V_{TH2} of the comparator and unintentionally turn on the transistor. To prevent this from happening, the controller usually has a minimum off-timer, thereby blanking any turn-on signals during a pre-defined time. Since the turn off threshold is a given parameter, the current at which it is triggered depends solely on the on-state resistance of the FET.

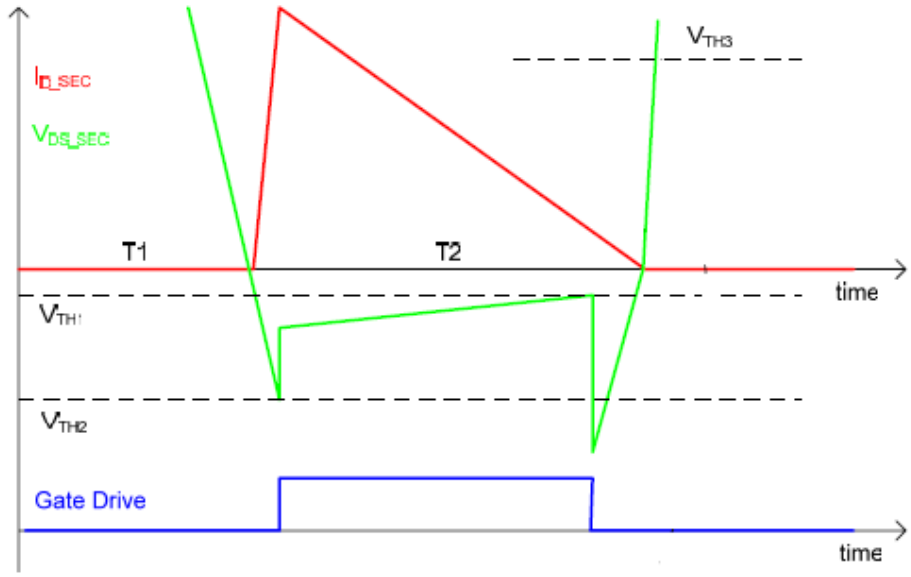


Figure 17 Simplified waveforms of the Flyback converter with SR [22]

4.1.3 Theoretical expectations and experimental results

By using synchronous rectification it is expected that the conduction losses will be decreased significantly. The initial conduction losses with the diode rectifier at full load are approximately 1.6W as calculated in 3.4.2.

For the implementation of SR rectification a MOSFET was chosen with a 14.5mΩ on state resistance at 100°C [23].

The on-state resistance is low enough to effectively reduce the losses, but high enough to provide a proper sensing voltage for the controller.

For the calculation it is assumed that the SR FET emulates the exact behaviour of a diode. In other words the dead time is zero, thus the current flows in SR FET for the entire conduction cycle.

With these considerations the theoretical expected losses are:

$$P_{SR\ Conduction,theoretical} = {I_{s,RMS}}^2 R_{ds,on} = 0.24\ \text{W}$$

Where :

$$I_{s,RMS} = 4.5A$$

$$R_{ds,on} = 14.5m\Omega$$

In the design the NXP TEA1792TS [24]SR controller was used because of its robust performance. Since this controller uses a novel technique which may have some effect on the efficiency, it makes sense to describe its operating principle.

Turn-on

The controller is triggered when a threshold of -220 mV has been exceeded. For the performance this means that the peak current flows for a non-negligible time through the high resistance path thereby causing losses.

Turn-off

As soon as the controller senses a voltage of -42 mV, the sensed voltage is maintained by decreasing the gate voltage to levels slightly above the threshold voltage. When the controller senses a voltage of -12mV the FET is turned-off almost instantly since the gate is already reduced. This novel concept to reduce the gate voltage, increases the on-state resistance of the FET. Although the current is already small during the period this takes place, the losses are not completely negligible.

Table 9, summarizes the experimental and theoretically expected losses.

Experimental losses diode	1.6 W
SR theoretical expected losses	0.24 W
Experimental losses SR	0.38 W

Table 10 Comparison of the losses in the different component with and without SR

From table 10, it is clear that the experimental losses are approximately 150% greater than the expected losses. This discrepancy can be attributed to the following reasons which are a consequence of the operating principle of the particular controller.

It is important to emphasize that although the losses are higher than expected theoretically, the efficiency is still greatly improved compared with the conventional diode implementation as seen in table 10 . More importantly, the losses are below the required 0.5W needed for SMT implementation as discussed in 3.3. Hence it may concluded that SR is a good solution to reduce the conduction losses.

4.2 Overview : ZVS strategies

Chapter 3 identified that the major part of the losses lie in the diode and the primary MOSFET, which are conduction and switching losses respectively . Section 4.1 has shown that with Synchronous rectification, the conduction losses in the secondary diode can be successfully reduced . However, The losses in the primary transistor are not resolved and therefore must still be dealt with. The switching losses are given by equation (16) which is repeated here for purposes of convenience:

$$P_{switch,turn-on} = \frac{1}{2} C_{eq} V_{sw,turn-on,max}{}^2 f_s$$

It can be observed that the losses are proportional to the parasitic capacitance, the frequency and the voltage squared. Partly because of this squared dependency it is most effective to decrease the losses by reducing the voltage. Also, generally speaking the frequency is difficult to reduce (optimize) since it is (to a certain degree) determined by other design considerations. Similarly, the capacitance is in general a given parameter. The capacitance however is dependent on the particular MOSFET. More specifically, the capacitance can be reduced by choosing a smaller device at the expense of higher $R_{ds,on}$. Thus a trade-off should be made between the conduction and switching losses. In the application at hand, this is not the case due to unique availability of a device with a 1700V rating. Consequently, the parasitic capacitance of the MOSFET can be considered a given parameter. The parasitic capacitance of the transformer also contributes to the total parasitic capacitance. Because the transformer is designed with the aim of minimization of the leakage inductance , the parasitic capacitance can be considered a given parameter for a particular design.

To decrease the switching voltage of the primary transistor basically two main methods can be distinguished [25]. An overview is given below .

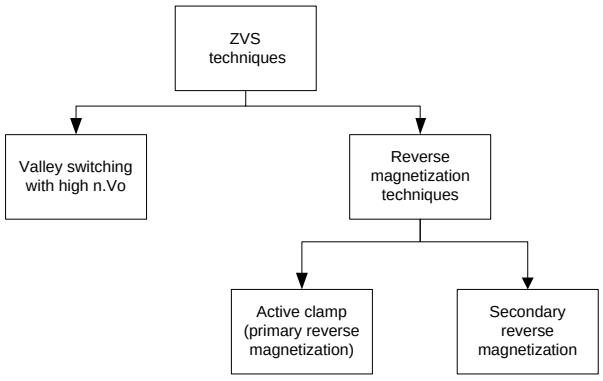


Table 11 general overview of the ZVS techniques

- Valley switching with high $n \cdot V_o$: Valley switching, is widely used in Flyback applications to reduce the switching losses and EMI. This technique is actually a variant of BCM where the transistor is controlled to switch on at the valley of the drain voltage. It is important to point out that the output voltage and the input voltage are given parameters, so the key is to "tweak" the turns ratio. Hence, a logical design strategy is to choose high turns-ratio as to ensure ZVS. At the same time however, the high turns-ratio also increases the voltage stress on primary transistor during turn off. This is demonstrated in the next illustrative example:

Assume the turns ratio is designed to achieve ZVS at maximum input voltage, thus:

$$n \cdot V_o = V_{in,max} = 800V$$

$$n = \frac{V_{in,max}}{V_o} \approx 60$$

This indicates that with a turns-ratio of 60 the valley of the drain voltage would automatically reach zero. The valley is then detected by the controller which switches the transistor on resulting in ZVS.

However, due to high turn-ratio and high input voltage the voltage at turn off becomes :

$$V_{sw,off} = V_{in} + n \cdot V_o = 800 + 13.5 \cdot 60$$

$$\boldsymbol{V_{sw,off} = 1610\,V}$$

It is critical to realize that the equation above neglected the overshoot caused by the leakage inductance , in this regard the calculated value should be considered as a very optimistic approximation.

From the analysis above it becomes clear that the turns-ratio is restricted by the maximum allowed voltage stress on the switch. For this reason in the design at hand, this strategy is not suitable due to the high input voltage. Accordingly, the maximum allowable voltage is exceeded which would provoke a negative impact on the design requirement.

- The second method to reduce the voltage, is based on the concept of magnetizing the transformer in the reverse direction. Two types of methods are known to reversely

magnetize the inductance [25]. In the first method, which is actually an active clamp technique the reverse magnetization is achieved by operations on the primary side. On the contrary, in the second method some mechanism on the secondary side causes the reverse magnetization.

- Active clamp ZVS technique : As mentioned in Chapter 2, in this technique the leakage energy is stored in the clamp capacitor. In the period of resonance between L_m and C_{eq} the auxiliary switch is turned on. During this time the voltage across the main and leakage inductance is negative . Hence, the transformer is then reversely magnetized. Since, the voltage across the primary transformer winding is negative the secondary diode is also forward biased. A substantial amount of research has been done at optimizing this strategy in order to achieve high efficiency.

Discussion: In the present application , Synchronous rectification is required to achieve low conduction losses. Accordingly, only active clamp methods which are compatible with synchronous rectifications are applicable. As a result, the active clamp methods such as [26], the diode is forward biased twice during one period, which would require complex control for SR. The background to this is quite simple, as the current flows the second time through the body-diode, the controller would be triggered to turn-on. However, the SR would not be triggered to turn-off prior to the turn on of primary FET with the corresponding destructive effects of cross-conduction. In [25]a variant of active clamp technique is documented that would possibly go hand in hand with SR. However, this technique gives rise to a number of problems including complex control [27]. Other techniques of active clamp techniques are based on CCM from which it is not clear if these are suitable for other operating condition such as the DCM/BCM in this design.

- SR reverse magnetization technique(SRMT): The secondary conduction time is extended by keeping the SR FET on for a longer time. More specifically, the SR FET is kept on after zero current crossing, thereby allowing the current to go negative. In other words, the current reverses direction, energy flow is reversed and therefore the transformer is reversely magnetized.

By analysing the simplified circuit given in figure 19 this technique can be explained further. In order to focus on the SRMT, the analysis is simplified by making the following assumptions :

1. The leakage inductance of the transformer and the snubber circuit are neglected, since they do not affect the SRMT.
2. It is assumed that the SR FET instantly turns on after the primary FET is turned off. In reality some delay is present which has no influence on the operating principle of SRMT.
3. The voltage over the switch increases instantly to $V_{in} + n \cdot V_o$,whereas in practice some time is needed to charge the parasitic capacitor.

The steady-state operation is described as follows and is depicted in figures 20-23 :

Mode 1 : [$t_0 - t_1$]

At t_0 the primary switch turns on and the primary current increases linearly by equation 1 just as in DCM. This is shown in figure 20.

This mode end when the switch is turned off.

Mode 2 : [$t_1 - t_2$]

The secondary diode start conducting instantly due to assumption 3, thus the current decreases linearly according to equation 2. This mode ends when the current reaches zero. The equivalent circuit is shown in figure 21.

Mode 3 : [$t_2 - t_3$]

Unlike in DCM/BCM , where the conduction of current stops at t_2, in the SRMT the SR is kept on until $\mathbf{t_3}$. During this time the energy flow is reversed and thus the transformer is reversely magnetized i.e. the flyback converter has become bidirectional. The amount of current required to achieve ZVS depends on the voltage, which is discussed in detail in chapter 5.2.

This mode ends when SR FET is turned off at the desired negative peak current. The equivalent circuit is shown in figure 22.

Mode 3 : [$t_3 - t_4$]

At the time instant t_3 the transformer is magnetized albeit in the negative direction. Since the SR FET is turned off and the inductor is charged, the current starts flowing on the primary side as shown in figure 23. In fact a resonance occurs between L_m and C_{eq}. However, the initial conditions are changed as will be discussed more thoroughly in 5.2, which results in a increasing amplitude. The key is to "dump" just enough energy back into the transformer in order to force the valley to reach zero, that is to increase amplitude of the resonance just

sufficient as to achieve ZVS. Dumping more energy back than necessary will needlessly increase the circulating current resulting in conduction losses.

Note that the primary FET is still off during this time , allowing the parasitic capacitance to be discharged . This mode ends when the capacitor is fully discharged, that is the voltage across the switch is zero. Then the primary FET is switched on and the cycle repeats.

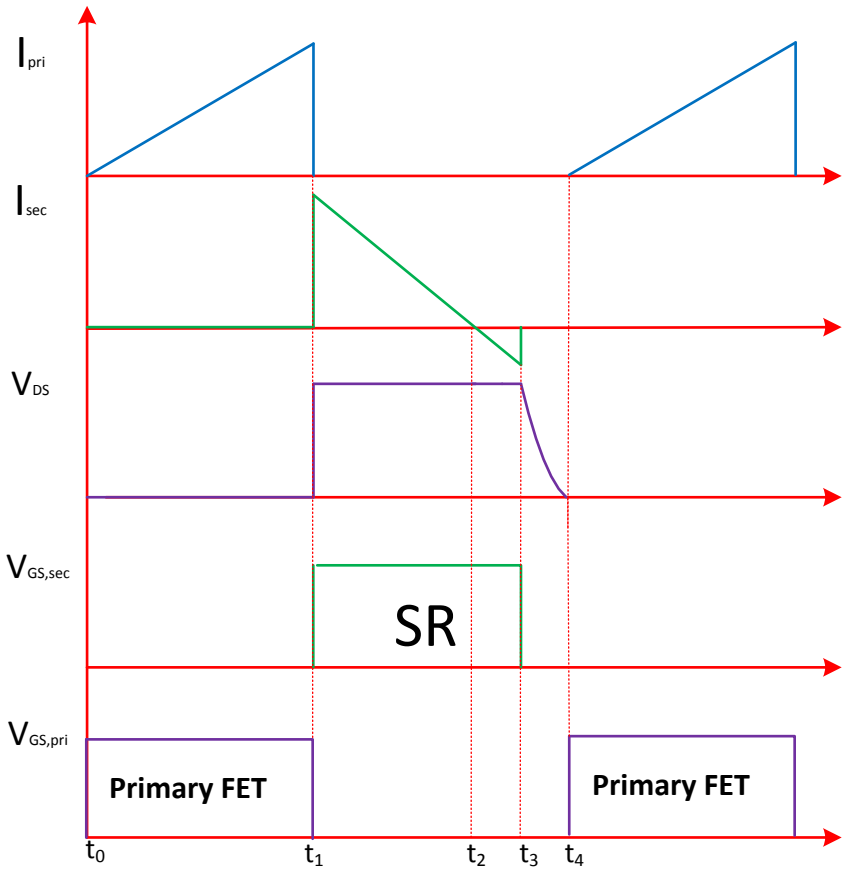


Figure 18 Shows the waveform during steady state operation of the Flyback with SRMT

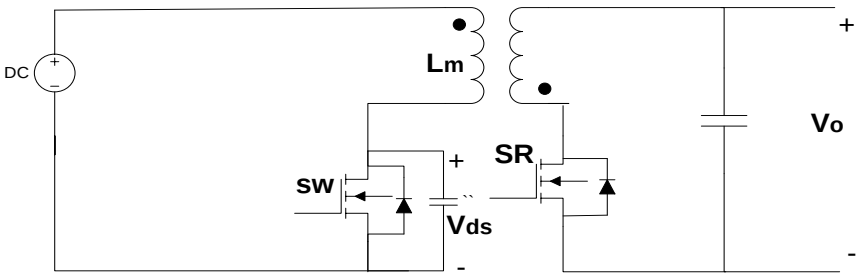


Figure 19 Simplified Flyback circuit with SR

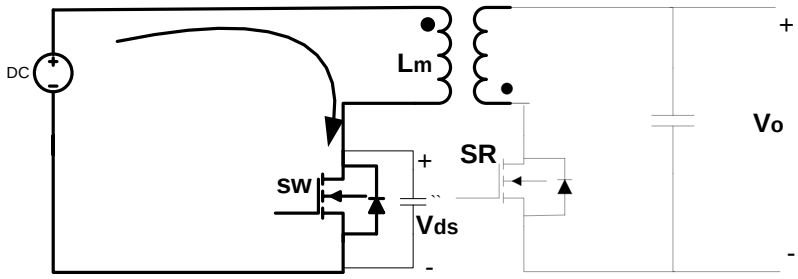


Figure 20 Equivalent circuit during mode 1

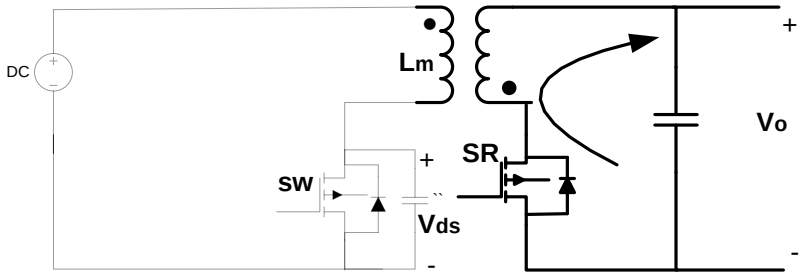


Figure 21 Equivalent circuit during mode 2

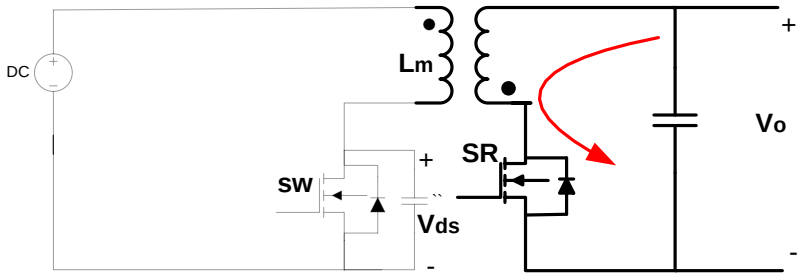


Figure 22 Equivalent circuit during mode 3

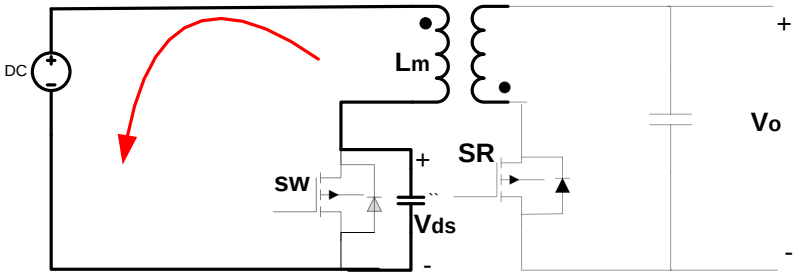


Figure 23 Equivalent circuit during mode 4

Prior art :the SR ZVS technique

The application of this technique is well documented in a number of papers and patents. In all of these documents, the concept is basically the same but they differ in control method. In [28], [29] a control method is proposed where the secondary gate signal is derived from the primary. By manipulating the primary gate signal with few logic circuit, a secondary gate signal is obtained. The disadvantages of this scheme are :

- The primary gate signal is delayed considerably to prevent cross conduction which gives a number of problems. Firstly, from a control engineering point of view, a large delay makes it hard to stabilize the loop.
- Secondly, the large delay will give poor dynamic response which makes it difficult for the converter to react to sudden load changes which in turn leads to instability. Lastly, the instant at which the SR MOSFET is switched on has a significant effect on the peak voltage stress which also affects the resonance loss [28]. Additionally, incorrect timing also results in a switching losses for the SR FET which deteriorates the efficiency. Conclusively, the instant the SR MOSFET is critical resulting in a complicated design.

The method used in [30] et al, use a discrete driver and a current transformer to achieve ZVS. This method needlessly increases component count, cost and complexity [24]

In [31]a method is proposed where the energy contained in the parasitic elements is used to discharge the parasitic capacitor. In this scheme the transformer windings are short circuited during the ringing time, that is the resonance between L_m and C_{eq} and subsequently this energy is used to discharge the parasitic capacitance. Because this energy is sparse, ZVS can only be successful in application with relatively low voltages. In relatively high input voltage applications such as the investigated design, the energy contained in the parasitic energy is not sufficient and should be combined with the method of reversing magnetization. Unlike other approaches, this concept has the advantage of good light load efficiency. The major drawback of this concept is that it requires an additional high-side FET which in turn requires complicated drive circuitry. Moreover, the described concept uses a digital control for the gate circuit. Although digital control brings many advantages, it needlessly complicates the design.

The importance of Variable frequency

In chapter 2 the variable frequency principle was briefly introduced. It should be noted that this varying switching frequency is a requisite for achieving ZVS under all operating conditions. Figure 24 and 25 show the waveforms with 700V input at light load and full load respectively. It can be observed that with constant input voltage, the frequency decreases as the load increases. Important to state is that the ringing period in the light load condition is longer and that is the reason why more oscillations can be observed. Furthermore, the instant at which the resonant(discontinuous mode) period starts changes, hence the resonant starting point is a varying parameter. This depends not only on the voltage but also on the load. In summary, in order to effectively achieve ZVS to at every operating condition, the switching frequency must be varied.

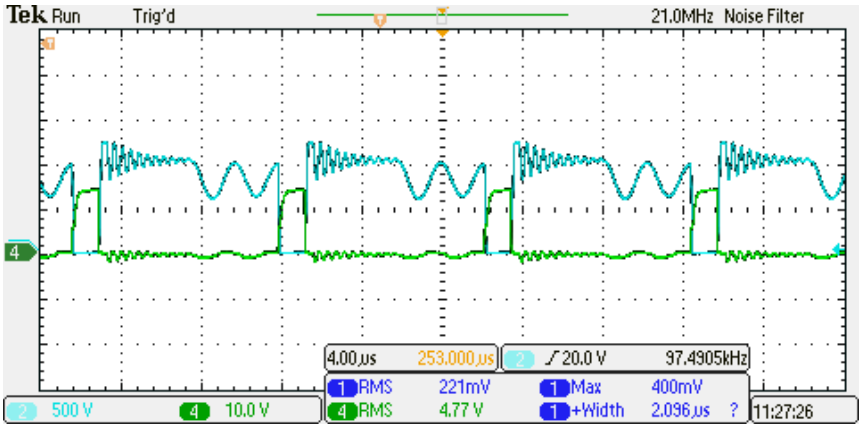


Figure 24 Typical waveforms of valley switching under light load condition where the voltage over the switch is shown in blue and the gate voltage of the primary FET is shown in green.

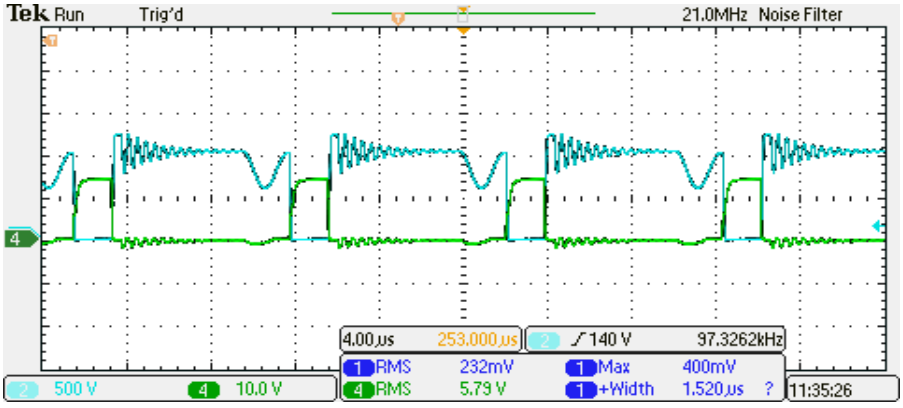


Figure 25 Typical waveforms of valley switching under moderate load condition where the voltage over the switch is shown in blue and the gate voltage of the primary FET is shown in green.

Conclusion: From the previous discussions it becomes clear that SR reverse technique is the most suitable for this design. Also, the methods found in literature all have their disadvantages and/or are difficult to implement. Finally, controllers with a ZVS feature built in are not commercially available. For this reason this thesis addresses the design of a ZVS SR controller by using simple analog logic circuitry. As mentioned earlier, the variable switching frequency is required , that is why a variable switching controller is used at the primary. Operating principle, schematics and design considerations are discussed in the next chapter.

5 Design and experimental results

Introduction

To reduce switching losses and simultaneously reduce the conduction losses a SR controller with current reverse technique has been developed. By modularly building every subsystem with logic circuitry a sophisticated controller was achieved. Every subsystem was first tested on its intended functionality in order to identify and resolve problems in an early design stage. Schematics of the essential circuit block, design considerations and experimental results are presented in this chapter. The complete schematics of the circuit including the required components can be found in Appendix B.

5.1 System level operation

To understand the operation of the controller design , the emphasis will be laid on the operation of the secondary side. The reason for this is that the primary controller works independently from the secondary controller. In this way the assumption is made that if the current is reversely magnetized causing the voltage to oscillate towards zero, the primary controller will sense the valley and hence switch on the transistor. As will be discussed later, this assumption is essentially valid with the exception of one special condition.

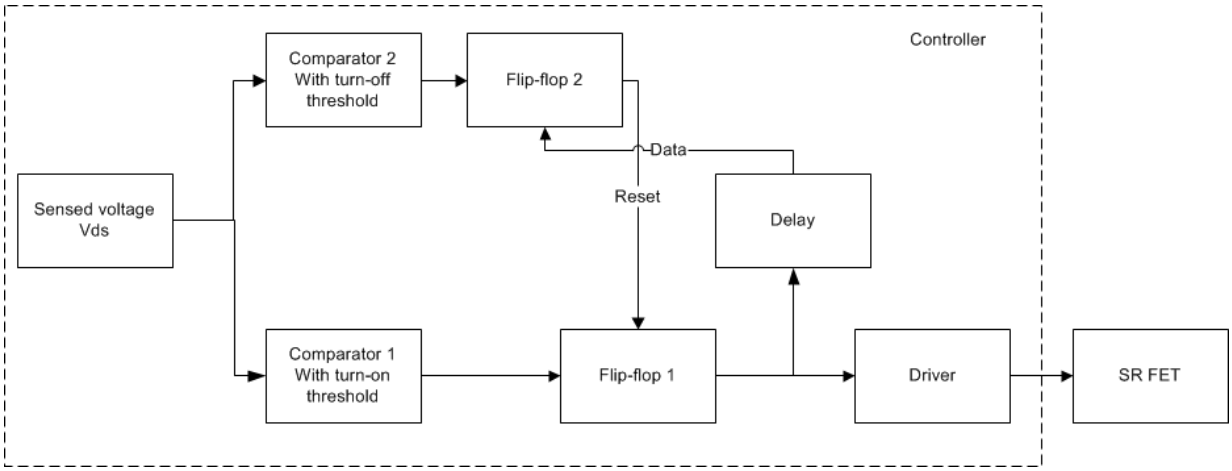


Figure 26 gives an overview of the functional description of the controller

Turn-on

Figure 26, shows the principal block diagram of the controller. The voltage across the drain (V_{DS}) is used to control the FET. As the current starts to flow through the body diode of the FET, comparator 1 is triggered and the gate is driven high. This is similar to the operation of the normal SR controller, where the FET is turned on at a typical

threshold voltage of -200 mV [24]. For the normal SR operation, that is without reversing current, this threshold is important due to the following : After the current decays towards zero, the MOSFET is turned off and the body diode finishes the conduction cycle. It was mentioned in 4.2 that this may lead to problems because the turn-on threshold is exceeded which would trigger the FET. As the turn-on threshold becomes higher, in other words less negative the sensitivity of this effect increases. Note also that the turn-on threshold increases the dead time decreases.

One of the main advantages of SR with reverse current is that this problem is avoided since the controller is switched off at a positive threshold. More specifically, the positive threshold implies that the current direction is reversed, thus the diode is automatically reverse biased during turn-off.

For that particular reason it is possible to optimize the turn on instant , hence reducing the dead time and significantly increasing the efficiency. Accordingly the controller design comparator 1 is triggered as soon as the voltage across the FET reverses , which would ideally mean the moment the current in the secondary starts to flow. This is practically impossible, because the different components each have their own delay.

Minimum turn on time

Although the implementation of two flip-flops may seem unnecessary this implementation is vital for correct operation due to the following two reasons:

- Comparator 2 which is responsible for turning off the FET has a reference voltage of approximately 11 mv. The origin of this particular value is explained in the next section. Bear in mind that during the primary conduction phase, the voltage across the secondary FET has a positive polarity. Since this voltage is larger than the threshold turn-off threshold, the comparator is triggered and resets Flip flop 1. As a result, flip flop 1 is disabled and in effect will not turn on . To, prevent this from happening, the second flip flop is enabled when the first flip flop goes high.
- Additionally, to overcome sudden turn-off due to ringing or other effects a delay is built in . To this end , comparator 2 is blanked for a predefined time (3us). Practically, this is achieved by using a simple RC circuit. By taking suitable values for the resistance and capacitor the time constant is set as to obtain the desired delay.

Turn off

After the current reverses, comparator 2 is triggered at a threshold that ensures ZVS at maximum input voltage. By calculating the required current for ZVS, the threshold voltage is set in accordance with the on-state resistance. Consequently, the positive threshold allows the transformer to reversely magnetize the transformer as to discharge the transistor parasitic capacitance. The analysis and calculations are presented in the next paragraph. In figure 27 and 28 , the waveforms with and without reversely magnetization are shown.

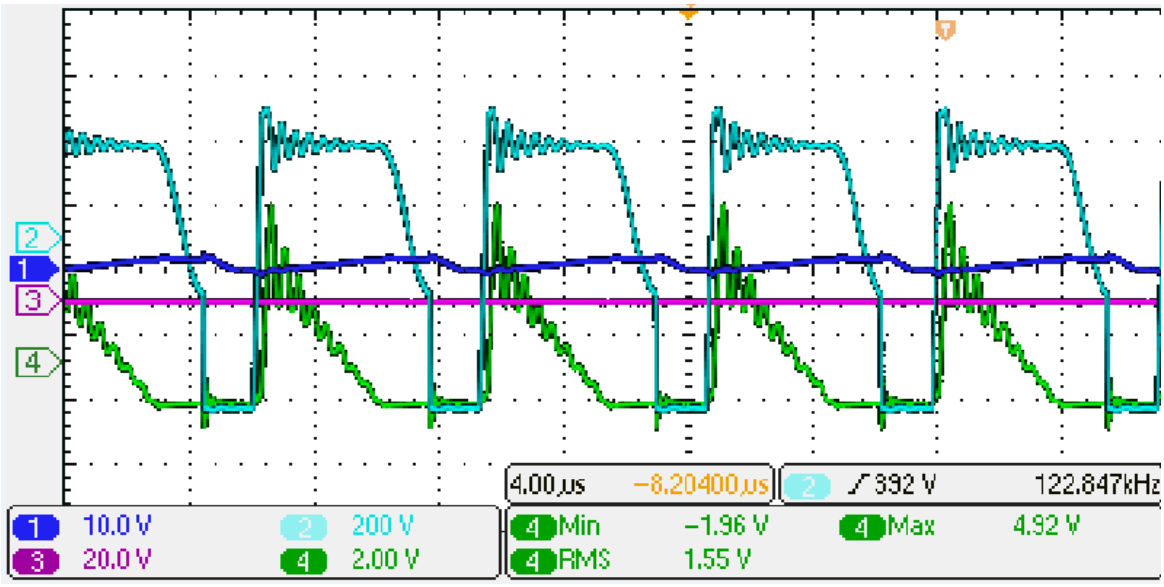


Figure 27 shows the waveforms of “normal” valley switching without reverse current

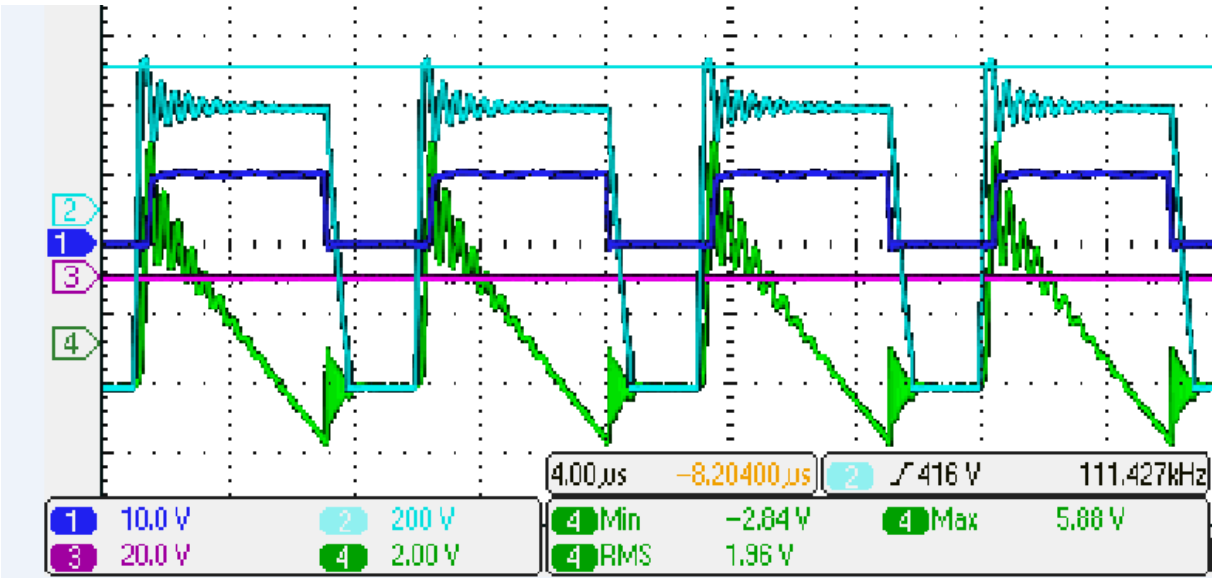


Figure 28 Shows the waveforms of ZVS by allowing the current to go negative

It should be stressed however that to ensure ZVS, the primary transistor should not be switched on immediately after the SR FET has been turned off. More specifically, it should allow the transformer to discharge the capacitor. Of equal importance is that the primary transistor is switched on at the instant when the voltage is zero. The reason for this comes from the fact that this corresponds to a resonant circuit where the resonant energy of the system is deliberately increased, thus the voltage would tend to increase to twice the initial value. If the voltage spikes up , the body diode of SR FET will be forward biased immediately when the primary FET voltage becomes equal to $V_{sw} = V_{in} + n \cdot V_o$. This would unintentionally turn-on the SR FET, although there is no " real energy " to be transferred to the load. In addition, and more importantly the control circuit is not able to distinguish this from the normal SR circuit and will stay on longer than required due to the classical minimum-on time function. Because of these reasons the correct operation of the primary transistor is vital in order for the system to function properly.

5.2 Determination of the required magnitude of the secondary negative current

As explained in 4.2 in mode 3: The secondary current has reached zero but the SR FET is kept on a bit longer which reverses the current direction and energy (taken from the output) is stored in the magnetizing inductance.

After the required negative current is obtained , the SR MOSFET is turned-off . This correspond to the end of mode 4.

At the this period a resonance occurs between L_m and the equivalent capacitance C_{eq} . So, again equation (8) applies which is repeated here for the purpose of convenience:

$$V_{c,eq}(t) = V_{in} - \left(V_{in} - V_{c,eq(0)}\right) cos\omega_0(t - t_0) + Z_0 \cdot I_{L0} sin\omega_0 (t - t_0)$$

$$I_{L,primaire,0} = I_{peak} = the\ required\ current\ that\ needs\ to\ be\ \acute{}fed\ back\acute{}$$

$$V_d = V_{in}$$

$$\omega_{zvs} = 2\pi \cdot f = \frac{1}{\sqrt{L_m \cdot C_{eqv}}}$$

$$Z_{zvs} = \sqrt{\frac{L_m}{C_{eqv}}}$$

$$V_{sw,t0} = V_{in} + n \cdot V_o$$

$$V_{sw}(t) = V_{in} - (V_{in} - (V_{in} + n \cdot V_o)) \cdot cos\omega_{zvs}(t - t_0) + Z_{zvs} \cdot I_{peak} \cdot sin\omega_{zvs}(t - t_0) \quad (21)$$

$$V_{sw}(t) = V_{in} + n \cdot V_o \cdot cos\omega_{zvs}(t - t_0) + Z_{zvs} \cdot I_{peak} \cdot sin\omega_{zvs}(t - t_0) \quad (22)$$

To describe what happens when the energy is reverse equation 22 is of interest. Note that this same equation is valid for DCM/BCM to describe the resonance between the main inductance L_m and the equivalent capacitance C_{eq} , as was explained in mode 4 in chapter 2.2. The main difference with DCM/BCM lies in the initial condition of the third term in equation 22 i.e. " $Z_{zvs} \cdot I_{peak} \cdot sin\omega_{zvs}(t - t_0)$" term.

In DCM/BCM mode the initial condition for the I_{peak} is zero. In the SRMT this current component is manipulated to achieve ZVS. In particular, the peak current I_{peak} is increased with negative polarity by keeping the SR FET on after zero current crossing.

Equation 22 represents an oscillation which is centered around the dc component V_{in} and therefore indicate that there is already energy is present in the system. From a conceptual point of view this makes sense, since in the normal DCM/BCM operation the voltage over the switch already oscillates between $V_{in} - n \cdot V_o$ and $V_{in} + n \cdot V_o$. This indicates that the Flyback converter inherently has energy contained in the LC circuit (L_m and C_{eq}). So , in order to achieve zero voltage switching we only need to inject the *remaining* energy needed to discharge the capacitor across the switch to zero. By considering the energy balance, the peak current can be can be calculated as follows :

$$energy\ required = energy\ to\ discharge\ from\ Vin\ - energy\ contained\ inherently\ in\ the\ LC\ circuit$$

$$\frac{1}{2} L \cdot {I_{peak,pr}}^2 = \frac{1}{2} C_{eq} \cdot {V_{in}}^2 - \frac{1}{2} C_{eq} \cdot (n \cdot V_o)^2 \quad (23)$$

$$\frac{1}{2} L \cdot {I_{peak,pr}}^2 = \frac{1}{2} C_{eq} \cdot {V_{in}}^2 - \frac{1}{2} C_{eq} \cdot (n \cdot V_o)^2$$

$$I_{peak,pr}{}^2 = \frac{C_{eq} \cdot (V_{in}{}^2 - (n \cdot V_o)^2)}{L_m}$$

$$I_{peak,pr} = \sqrt{\frac{C_{eq} \cdot (V_{in}{}^2 - (n \cdot V_o)^2)}{L_m}}$$

$$I_{peak,pr} = \frac{\sqrt{(V_{in}{}^2 - (n \cdot V_o)^2)}}{Z_{zvs}}$$

Now , with the turn ratio the secondary current becomes:

$$I_{sec,ZVS} = n \cdot I_{peak,pr} = \frac{n \cdot \sqrt{(V_{in}{}^2 - (n \cdot V_o)^2)}}{Z_{zvs}} \quad (24)$$

From equation (24) it can be observed that, the required current $I_{sec,ZVS}$ depends on the input voltage, output voltage, resonant impedance and turns-ratio. Note that the all the dependent parameters with the exception of the input voltage are constant. Therefore, as the input voltage increases the required current also increases and vice versa. For the implementation this means that the reference voltage V_{th2} needs to change with the input voltage. In practice this is not easy to implement, as the reference voltage is in the order of millivolts. To still be able to reach ZVS at every operating condition the reference voltage is designed for the highest input voltage, that is 800V. At lower input voltages ZVS will automatically be ensured at the *expense of more circulating current*. Due to the low on-state resistance of the SR FET the relative higher circulating current does not significantly increase the losses. Consequently, this tradeoff is justified.

By substituting the following parameters in equation (24), the required negative current is found to be :

V_{in}	800V
V_0	13.5V
Z_{zvs}	7924Ω
n	16

Table 12 Required parameters of the circuit for the negative peak current calculation

$$I_{sec,ZVS} = 1.55\ A$$

With this information and the on-state resistance of the transistor, the threshold voltage of comparator 2 can be defined as :

$$V_{th2} = \frac{I_{sec,ZVS}}{R_{ds,on}} \tag{25}$$

Bear in mind that the $R_{ds,on}$ depends on the temperature which in turn depends on the losses. Taking the $R_{ds,on}$ at 100 ˚C and $I_{sec,ZVS}$ =1.55A equation (25) becomes :

$$V_{th2} = 11mV$$

Because the exact value of the $R_{ds,on}$ is difficult to determine, this V_{th2} is used as first estimation. The final value of V_{th2} is a result of tuning process on the real board.

5.3 Experimental results Prototype

For verification of the concept, the controller was built on a typical protoboard . Although the parasitic effects on such a board are problematic, it brings the advantage to easily replace elements. To this end, the components of the converter were first established on the protoboard in order to verify whether the proposed control makes it possible to use SMT components for implementation. After verification the implementation the converter including the proposed control was built on a printed circuit board(PCB). The PCB design was done by identifying the major current loops and carefully adjusting the layout in order to minimize their interfering effects.

Theoretical loss expectations

By implementing the concept, the following results regarding the losses were expected :

- If ZVS is achieved, the losses in the primary transistor which are almost exclusively switching losses would reduce to zero, since $P_{switch,turn-on} \propto V^2$.

- The conduction losses in SR FET would be reduced to approximately 0.38W as was found in 4.1.2 . However, due to the current reversal for ZVS, relatively more current flows in the circuit which would slightly increase the conduction losses.

- Although it is not the focus of this research , it was expected that the losses in the transformer would be reduced due to the utilization of litz wire with lower effective resistance, thereby effectively reducing the winding losses.

5.3.1 Experimental results

In order to verify the theoretical expectations the Flyback converter with the proposed controller was built and tested. Figure 29 shows prototype design on a PCB board. Compared with the initial design of chapter 2 the following adjustment were made:

- The fixed-frequency controller was replaced by the NCP1207 variable frequency controller [[32]
- The diode was replaced by the BUK-7610 100 MOSFET [23]with the proposed controller
- The transformer was designed once again in order to take into account the variable frequency. The specification of this renewed design is summarized in table 12.

L_m	2.575 mH
L_s	40.7 µH
R_{dc}	1.9Ω
n	17

Table 13 Specification of the new transformer

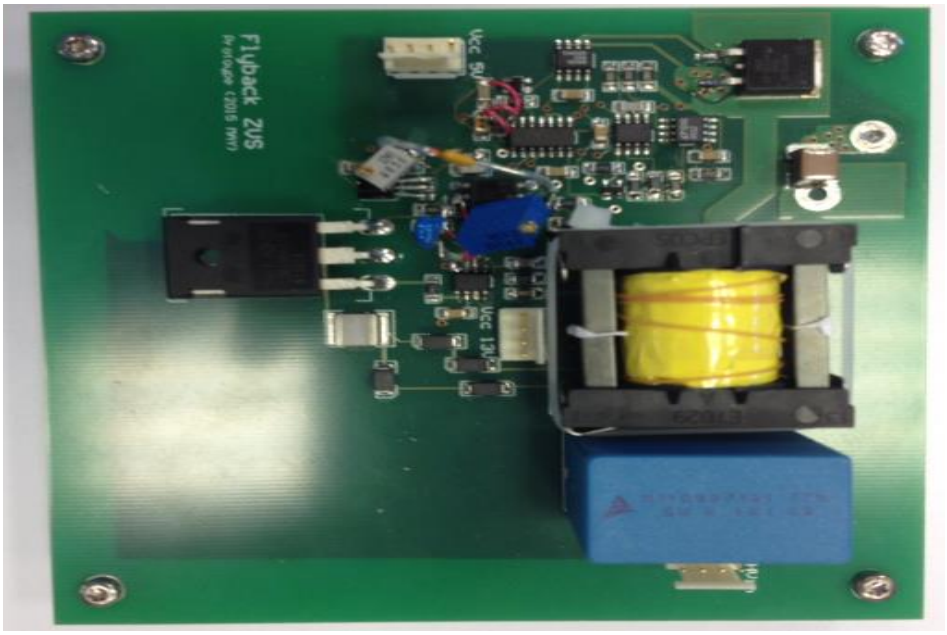


Figure 29 Shows the Flyback converter with the proposed controller implemented on PCB

The converter was tested at different operating conditions and the efficiency as well as the losses in the components were measured. The efficiency was evaluated by measuring the voltage and current at both the input and output. The results are shown in table 12.

input voltage (V)	$I_{output}/I_{nominal}$	Efficiency	Primairy FET Temp increase (˚C)	SR FET Temp Increase (˚C)	Losses primary FET (W)	Losses SR FET (W)
401	50%	90.60%	6	13	0.27	0.26
397.1	100%	90.70%	6.5	16.5	0.29	0.33
797	50%	90.06%	6.3	17	0.28	0.34
780	100%	89.09%	6.8	18.4	0.3	0.36

Table 14 Shows the experimental results at different input voltages and different load conditions

It can be observed that the converter operates with reasonable high efficiency in both full load and half load condition. It is important to emphasize that the efficiency of the total converter is not of primary interest. This study focuses on the reduction of the losses and thus the temperature in the active component to determine whether SMT components can be used with minimal footprint.

Note from table 14, that the temperature rise of the active components in the primary and secondary transistors are limited. Moreover, the last two columns show that the losses in these components are significantly reduced for both operating conditions. More specifically, the losses are below the required 0.5W which was the approximation made in chapter 3.3 for successful SMT implementation with minimal footprint.

These measurements are performed on the protoboard because it enables the use of infrared imaging methods. Infrared imaging measurements cannot be performed easily on a PCB, because the thermal characteristic of the PCB affects the thermal resistance of the individual components. Figure 30 shows the waveforms at minimum input voltage and full load of the converter with protoboard implementation. Whereas figure 31 and figure 32 show the results at full load with minimum and output voltage, respectively. Notice that the ringing of the voltage (light blue waveform) is significantly less in the PCB implementation due to the reduction of the parasitic elements.

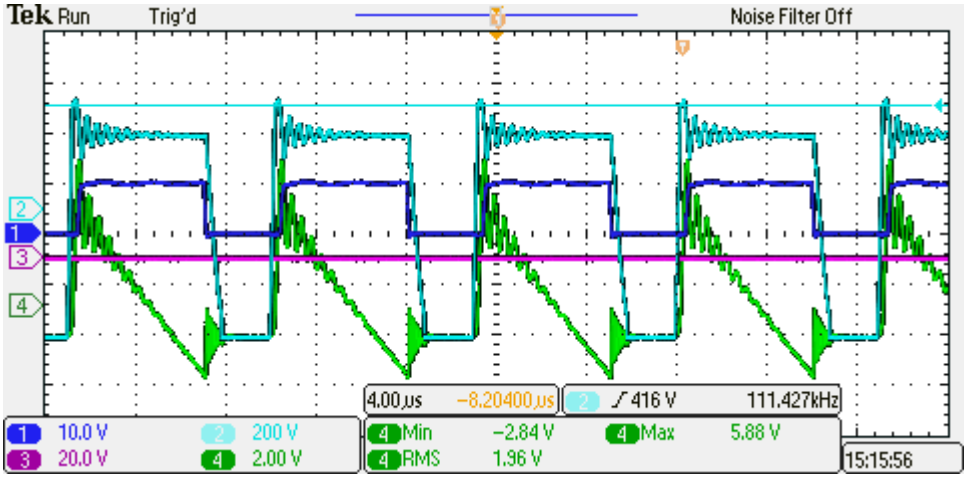


Figure 30 Shows the experimental results of the proposed ZVS scheme implemented on the protoboard where the voltage over the switch is shown in blue , the gate voltage of the SR FET is shown in blue and the current is shown in green

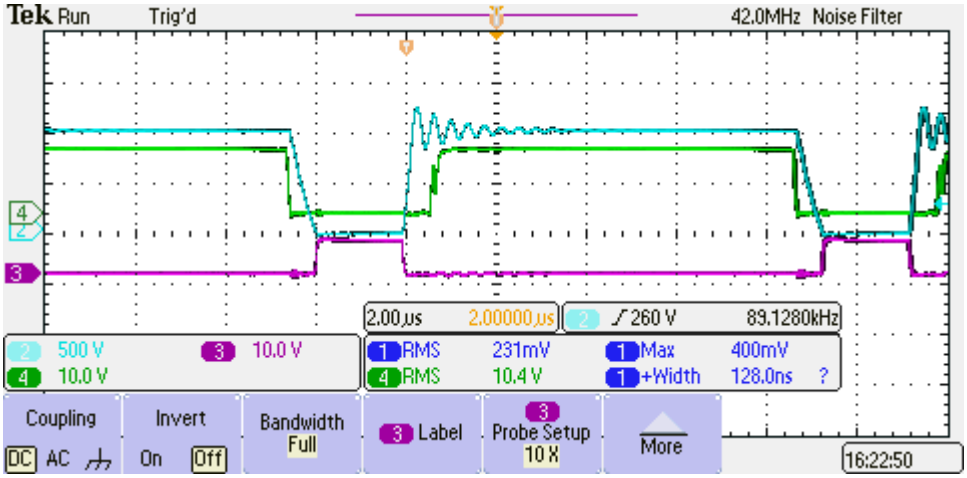


Figure 31 Shows the results of the proposed ZVS scheme at full load and 400 input voltage implemented on the PCB where the voltage over the switch is shown in blue, the gate voltage of the primary FET is shown in red and the gate voltage of the SR FET is shown in green.

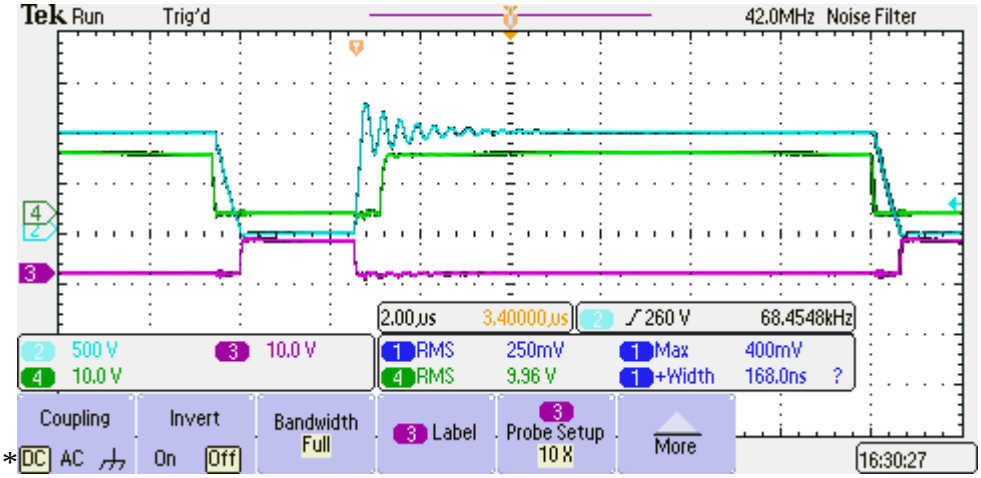


Figure 32 Shows the results of the proposed ZVS scheme at full load and 800V input voltage implemented on the PCB where the voltage over the switch is shown in blue, the gate voltage of the primary FET is shown in red and the gate voltage of the SR FET is shown in green.

Comparison of theoretical and experimental losses

To compare the experimental and theoretical losses, the experimental losses at full load and maximum input voltage are considered as they depict the worst operating condition.

- The losses in the SR FET were expected to be slightly higher than 0.38W as mentioned earlier. The experimental losses were found to be 0.36 W. This discrepancy can be owed to the following 2 factors:
    1. As was discussed in chapter 5.1, the operating principle of the designed controller turns the SR-FET much faster than the commercial available controllers, which significantly increases the efficiency .
    2. Measurement inaccuracies due to the use of measurement equipment which are not calibrated.

- The losses in the primary MOSFET were (theoretically) expected to be almost zero since :
    a) the switching losses are zero since the MOSFET is constantly switched on at zero voltage
    b) The conduction losses are negligible.

  The experimental losses were found to be 0.3W. The discrepancy can be due to the following factors:
    1. Measurement inaccuracies similar to the SR FET
    2. Inaccuracies in the estimation of the thermal resistances from the MOSFET case to ambient i.e. thermal paste, isolation Pad and Aluminum plate used as heatsink

Blanking time issue

From the results and analysis above it can be concluded that the designed controller significantly reduces the losses in and between the given operating points. During the experiments it was observed that at light load conditions the primary controller shows erratic behavior. In figure 33, the waveforms are shown at light load condition.

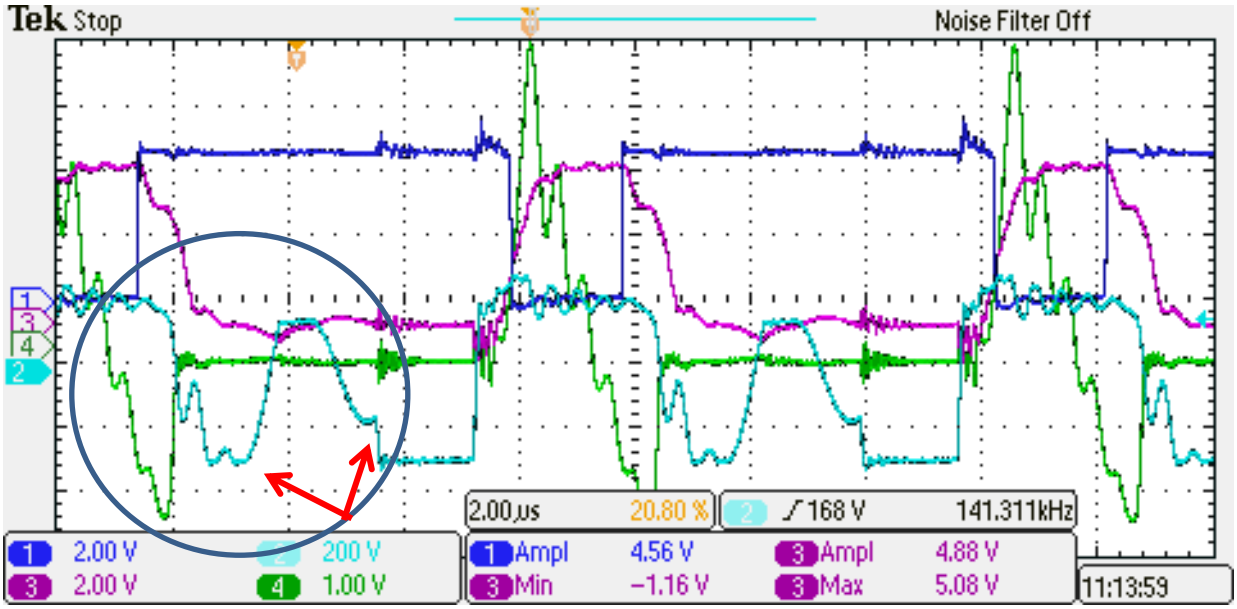


Figure 33 Shows the waveforms at a typical light load condition indicating the effect of the blanking time where the voltage over the switch is shown in blue and the secondary current is shown in green.

It can be seen that after the current is reversed and interrupted by switching off the transistor, the voltage oscillates towards zero. The primary controller however does not switch the transistor on and this results in a voltage which oscillates back up again. This is disadvantageous due to the following reasons:

- As the voltage swings up , it is possible that a scenario occurs where diode conducts again and unintentionally turns the FET with negative effect as was described in 5.1.
- Notice that the ZVS switching is lost , since the energy fed back to primary is again supplied to the secondary. While ZVS is not achieved, the circulating current is still increased which in turn deteriorates the efficiency.

The reason why the primary controller does not switch on the transistor is because of the internal blanking time. This blanking time is a feature built in virtually all quasi-resonant commercially available controllers. The idea of this blanking time is to limit the frequency to an acceptable value. Bear in mind that these controllers are made for valley switching operations. As the switching voltage is also proportional to the frequency, the valley switching technique loses its strength when the frequency increases considerably. To prevent, the efficiency from decreasing, the maximum frequency is clamped to a pre-defined value by the blanking time (typically 3µs). It is important to understand that in case *ZVS can be assured*, the frequency increase does *not affect the efficiency* as the switching losses are already zero. Thus, it can be concluded that the operating range of the current design is restricted by the commercial primary controller limitations. (restrict frequency due to gate losses and limitation of the driver, turn-on and turn-off time)

5.3.2 Primary controller

Based on the discussion above it became clear that the primary controller has some limitations. There are basically two solution for this problem:

1. Design of primary controller where the frequency is not limited. In doing so, the controller switches at the first valley independent of the load condition.
2. By using a technique where the DCM resonant period is delayed until the blanking time of the primary controller is expired. In this way the BCM is ensured at every operating condition.

Due to the limited time of this study, the first solution is not considered. The second solution is tested and discussed more thoroughly in the next section.

5.3.2.1 Proposed solution

Figure 34 shows the schematic of the proposed solution which is a variant of the circuit proposed by [31]. Although the schematic is the same, the control concept here is entirely different. The rising edge of the turn-on instant of the SR FET is used to generate a one shot pulse which is applied to the gate of the auxiliary transistor. The duty cycle of the one shot pulse is set to be slightly greater than the blanking time of the primary controller. In doing so, at light load when the secondary conduction phase is very short, the transformer windings are short circuited. Since the energy must be conserved, the resonance between L_m and C_{eq} is delayed until the one shot pulse is expired. In this way valley "seen" by the primary controller will always be after the blanking time, hence ZVS can be assured under all operating conditions.

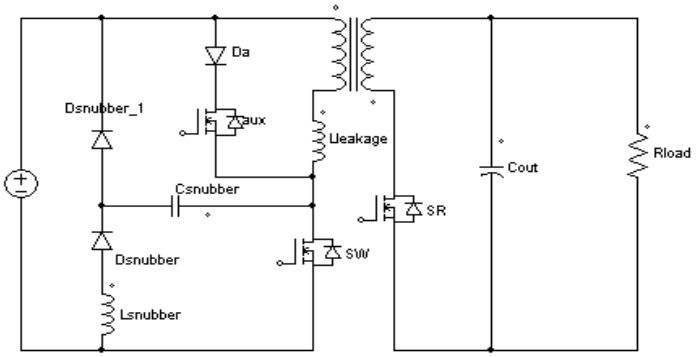


Figure 34 Proposed Flyback circuit with auxiliary circuit based on [25]

Experimental results

For the implementation of this solution, the following changes were made to the initial circuit :

- Power stage : For the power stage a diode in combination with additional (auxiliary) FET was added as shown in figure 34. Since this is a "high-side FET" with a differential voltage of approximately 600V, special driving requirement are necessary. To this end, the well-known bootstrap circuit was used.
- Control : The control circuit has been altered by adding the one-shot pulse. Since the auxiliary transistor is in the primary and the driving signal is retrieved from the secondary, an isolation driver was used to provide galvanic isolation between the two sides.

The functional diagram is shown in figure 35. Notice that the main difference regarding the control block, is the addition of a one shot pulse generator which is triggered at the rising edge of SR gate voltage.

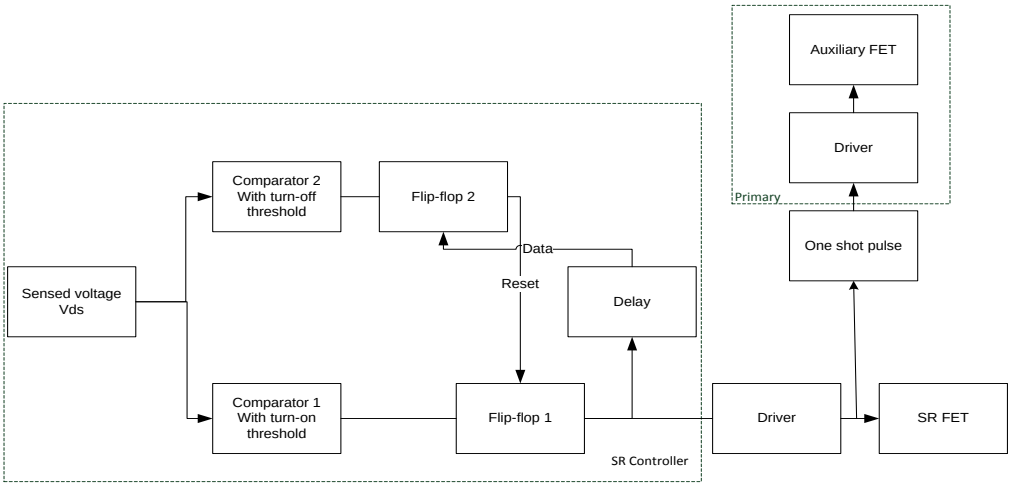


Figure 35 gives an overview of the functional description of the proposed controller with an auxiliary transistor

Light load

The experimental results are shown in figure 36 and 37. Figure 36 shows the situation at no load condition. Notice that the amount of positive current is almost the same as the amount of negative current. Hence, the average current is almost zero as would be expected in no load situation. In fact, the only current that flows in the circuit is the current required to achieve ZVS. In this specific situation the RMS value of the load current was measured to be approximately 1A which combined with the low on-state resistance of the SR FET results in negligible losses. Similarly, the losses in the primary are negligible due to ZVS. Accordingly, it was observed that the temperature rise in the active components were negligible, hence at light load condition high efficiency is achieved.

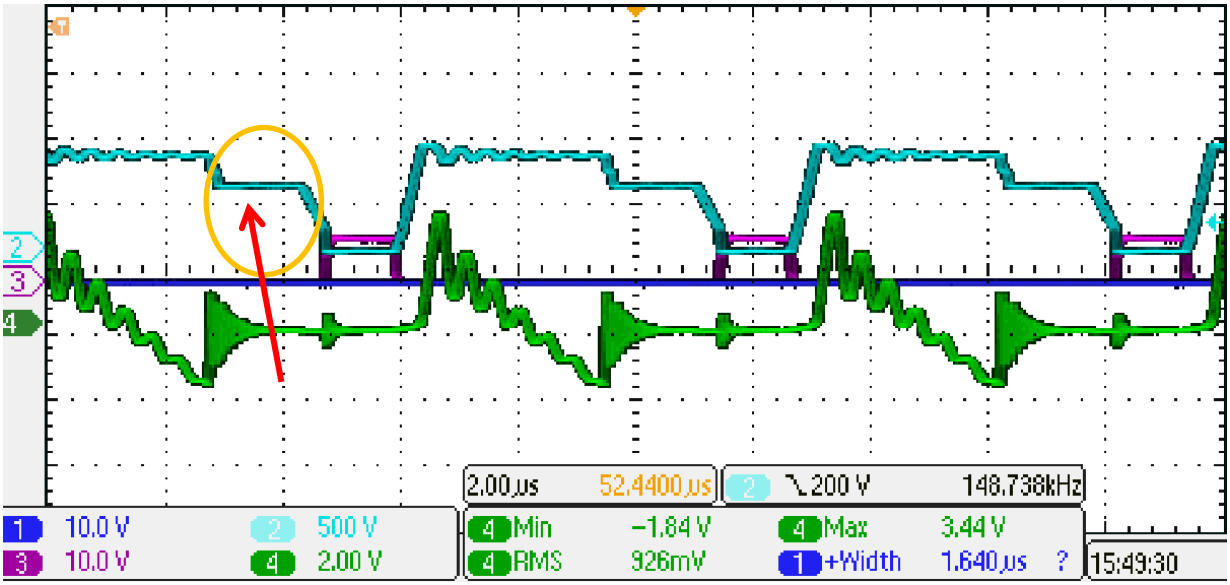


Figure 36 Shows the waveforms of proposed voltage clamping technique under light load condition where the voltage over the switch is shown in blue, the gate voltage of the primary FET is shown in red and the secondary current is shown in green.

Transition light to high load condition

Figure 37 shows the condition with the same voltage but increased load. Notice that the clamping time of the voltage is considerably reduced. In fact, the clamping effect decreases with increasing load and decreasing input voltage. Consequently, at high load the effect is lost, because the pulse width of the secondary gate voltage is wider than the one-shot pulse. In conclusion, this method does not affect the operation at high load conditions.

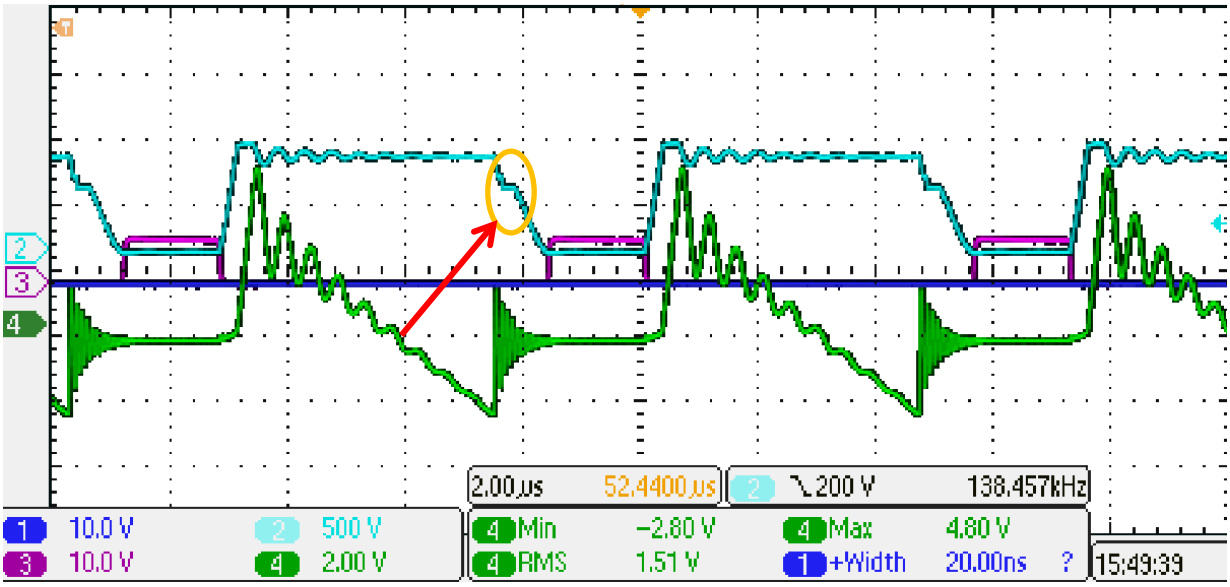


Figure 37 Shows the waveforms of proposed voltage clamping technique under moderate load condition where the voltage over the switch is shown in blue, the gate voltage of the primary FET is shown in red and the secondary current is shown in green.

Erratic behavior

Experimental results have shown that the proposed method works at every load condition from 400-600V. At higher voltages it was observed that the primary controller again shows erratic behavior. As shown in figure 38 by the red arrow in the circle, the primary controller does not switch on the primary controller even though the blanking time has passed. The erratic behavior the converter showed at these conditions were also observed when the control loop was not tuned correctly. Based on this observation it is believed that the erratic behavior of the primary controller is caused by problems regarding the control loop. In particular, we believe that the noise in the circuit on the protoboard disturbs the control loop as explained below.

Control loop and noise

From experimental observation the implementation on the protoboard has shown great difficult for the control stabilization. This is likely to be the result of noise disturbance due to the spacious design. In contrast, the same control loop on the PCB has shown great stability. It is important to state that the PCB design was done without auxiliary FET. Based on the stable behavior of the PCB, it is expected that the proposed scheme with auxiliary FET would be stable under all conditions. Due to limited time of this study, this was not investigated.

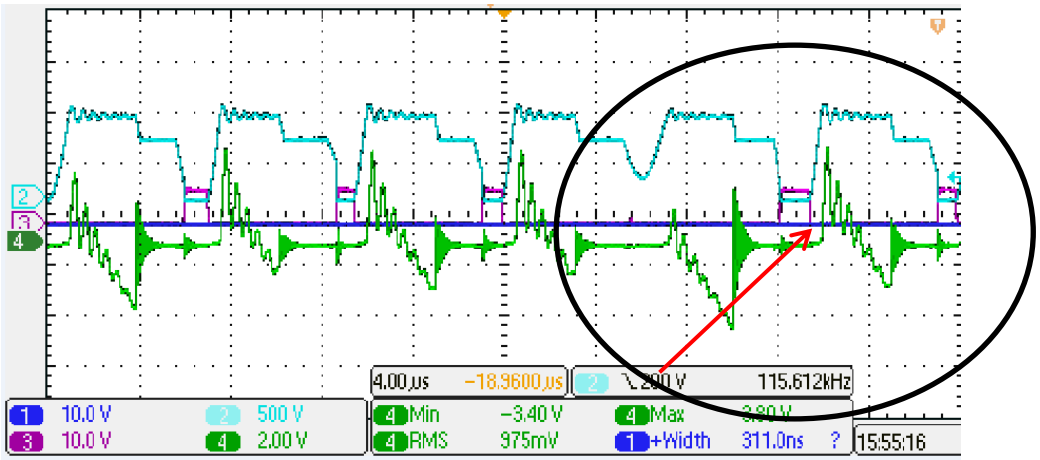


Figure 38 Shows the waveforms of proposed voltage clamping technique with erratic behavior where the voltage over the switch is shown in blue, the gate voltage of the primary FET is shown in red and the secondary current is shown in green.

6 Conclusions and Recommendations

In this chapter the conclusions of this study are presented and recommendations on further improvement of this study are made.

6.1 Conclusions

To reduce the losses a SR controller which enables ZVS has been successfully built and tested. From the experimental results the following conclusions can be drawn:

- At load conditions ≥ 1.5 A the proposed Flyback converter shows high efficiency, that is efficiency greater than 88%
- At these load conditions the highest losses in the active components are observed to be 0.3 W and 0.36W respectively. The temperature rise as result of these losses are within the specified limits as to use SMT components as was verified by the PCB design.
- At light load conditions that the limited blanking time of the controller leads to erratic behavior.
- To overcome light load conditions a solution was proposed. For the voltage 400-600V the proposed solution has proven to work under every load condition including no-load.
- At higher voltage the proposed solution has shown some erratic behavior which was expected to be a result of a control loop instability due to noise disturbance.
- The construction of the transformer has great influence on the peak voltage on the primary MOSFET. Although interleaving techniques reduce the peak voltage, the LC snubber technique was necessary to limit the voltage to meet the design requirement.

On the whole, it can be concluded that, even though the proposed converter showed some erratic behavior at some load conditions, the results in this thesis have shown that the losses in the active components can be significantly reduced to the level where SMT implementation with minimal footprint is possible.

6.2 Recommendations

Improving the operating range

1. The proposed solutions discusses in 5.3.2.1 has proven to work under load conditions with the input voltage range varying between 400-600V. Additional investigation is required as to determine if the proposed solution can be extended to work on the whole input voltage range . From the results it is expected that a stable control loop is the solution.
2. As mentioned, the commercially available primary controllers blanking time impose limitations for the operating range of the proposed SR scheme. The solution proposed in 5.3.2.1 requires an additional high voltage switch including driving requirements, which increases component cost. By using a controller without blanking time, it is expected that the proposed SR controller would be able to operate under all load conditions while keeping high efficiency. With this solution no additional components are required, thus it is recommended to investigate the design of a primary variable frequency controller without frequency clamping.

Transformer optimization

This study has focused on the reduction of the losses in the active components. In the future, the work can be extended for the optimization of the transformer.

Appendix A: Flyback DCM Design

As the optimization of the Flyback transformer is not the focus of this study, simple design guidelines provided by [11]are used.

The maximum reflected voltage is limited by the maximum allowable voltage on the drain of the FET, thus:

$$V_{R_{max}} = V_{sw,max} - V_{in,max} - 30\% \cdot V_{sw,max} = 1400 - 800 - 390 = 210\,V$$

With $V_o = 13.5\,V$:

$$n_{max} = \frac{V_{R_{max}}}{V_o} = 15.55$$

The amount of turn is chosen to be n= 16.

Now, the maximum duty cycle is calculated with:

$$D_{max} \approx \frac{V_R}{V_{in,min} + V_R} \approx \frac{210}{400 + 210} = 0.344$$

With $P_{in} = 45W$ assuming efficiency of 0.9 and $F_{sw} = 100\,kHz$, the inductance is calculated as:

$$L_p = \frac{V_{in.min} \cdot D_{max}}{I_{pri} \cdot F_{sw}} = 2\,mH$$

As the specifications are known, a suitable core can be chosen. To this end the application note of [33]is used, where the cores EI28, EER28, ETD29, EFD and EER35 are recommended for the power level of 40 W. Based on the available parts at, the ETD29 core is chosen.

To avoid saturation and to stabilize the magnetic circuit a small air gap will be introduced. The minimum air gap is chosen such that the reluctance of the air gap dominates over that of the core. For the first estimation: 4 sheets of A4 paper are used. One sheet of paper has a typical thickness of 0.1 mm.

With the simple magnetic formulas the required number of turns is calculated.

$$\mathcal{R} = \frac{l}{\mu A}$$

$\mathcal{R}_{total} = \mathcal{R}_{core} + \mathcal{R}_{airgap} \approx \mathcal{R}_{core}$ since $\mathcal{R}_{core} \gg \mathcal{R}_{airgap}$

$$A_{leg} \approx \frac{1}{2} A_{center}$$

$$\mathcal{R}_{leg} = \frac{l_{gap}}{\mu \frac{1}{2} A_{center}} = \frac{2 l_{gap}}{\mu A_{center}}$$

$$\mathcal{R}_{center} = \frac{l_{gap}}{\mu A_{center}}$$

The magnetic path start from the center of the core passes through one of the legs and end backs at the center. Therefore the total reluctance becomes:

$$\mathcal{R}_{total} = \mathcal{R}_{leg} = 2\mathcal{R}_{center}$$

$$L = \frac{N^2}{\mathcal{R}_{total}}$$

$$N_p = \sqrt{\frac{2 l_{gap} L}{\mu A_{center}}} = 129.34$$

Where :

$$l_{gap} = 4\ sheets\ of\ paper = 4 \cdot 0{,}1mm = 0.4mm$$

$$A_{center} = 76\ mm^3$$

$$B = \frac{N I_{peak}}{\mathcal{R}_{total} A_{center}} = \frac{N I_{peak} \mu}{2 l_{gap}} = 0.14\ T$$

Where:

$$\mu = \mu_{paper} \mu_o = \mu_{o=}\ 4\pi \cdot 10^{-7}$$

$$I_{peak} = 0.7A$$

The calculated flux density is low enough to limit the core losses. Therefore the specified air gap and the number of turns give a reasonable flux density.

The number of turns of secondary is then calculated by:

With n=16:

$$N_S = \frac{N_p}{n} \approx 8$$

The following step is to calculate the total allowed transformer losses. As the manufacture of the core specifies the thermal resistance, the allowable losses can easily be calculated with: --+

$$P_{tot} = \frac{\Delta T_{max}}{R_{th}} = 1.07W$$

Where:

$$\Delta T_{max} = 30\ ℃$$

$$R_{th} = 28\ {}^{℃}/_{W}$$

In order to take some safety margin, the flux swing is assumed to be 50% larger than the above calculated value.

$$B_{estimated} = 0.24\ T$$

The core losses are then obtained from the datasheet [34]:

$$P_{core} \approx 100\ {}^{kW}/_{m^3}$$

The volume of the core is found to be [35]:

$$V_e = 5350\ mm^3$$

Then:

$$P_{core} \approx 0.535\ W$$

The allowed copper losses are then calculated with:

$$P_{cu} = P_{tot} - P_{core} = 0.535W$$

From this the required resistance of the windings can be calculated. First the peak and RMS currents are calculated:

$$I_{pri,peak} = \frac{2 \cdot P_{in}}{D_{max} \cdot V_{in,min}} = 0.73\ A$$

$$I_{pri,rms} = I_{pri,peak} \cdot \sqrt{\frac{D_{max}}{3}} = 0.246\ A$$

$$I_{sec,peak} = I_{pri,peak} \cdot n = 11.68A$$

$$I_{sec,rms} = I_{sec,peak} \cdot \sqrt{\frac{(1 - D_{max})}{3}} = 5.46A$$

$$R_{pri} = \frac{P_{cu}}{2 \cdot {I_{p,rms}}^2} = 3.54\Omega$$

$$R_{sec} = \frac{P_{cu}}{2 \cdot {I_{s,rms}}^2} = 7.2m\Omega$$

The required primary and secondary copper is calculated by the considering the resistivity of copper at 100 ℃ and the average length-per-turn of the bobbin used for the ETD29 core:

$$Ap_{cu,min} = \frac{\rho_{100} \cdot N_p \cdot L_t}{R_p} = 2.75 \cdot 10^{-5}\ cm^2$$

$$As_{cu,min} = \frac{\rho_{100} \cdot N_s \cdot L_t}{R_s} = 0.21\ cm^2$$

With these specifications proper wires are selected and the transformer design is finalized.

The next step, the secondary rectifier is selected:

The voltage rating is set by the maximum reverse voltage it experiences including safety margin.

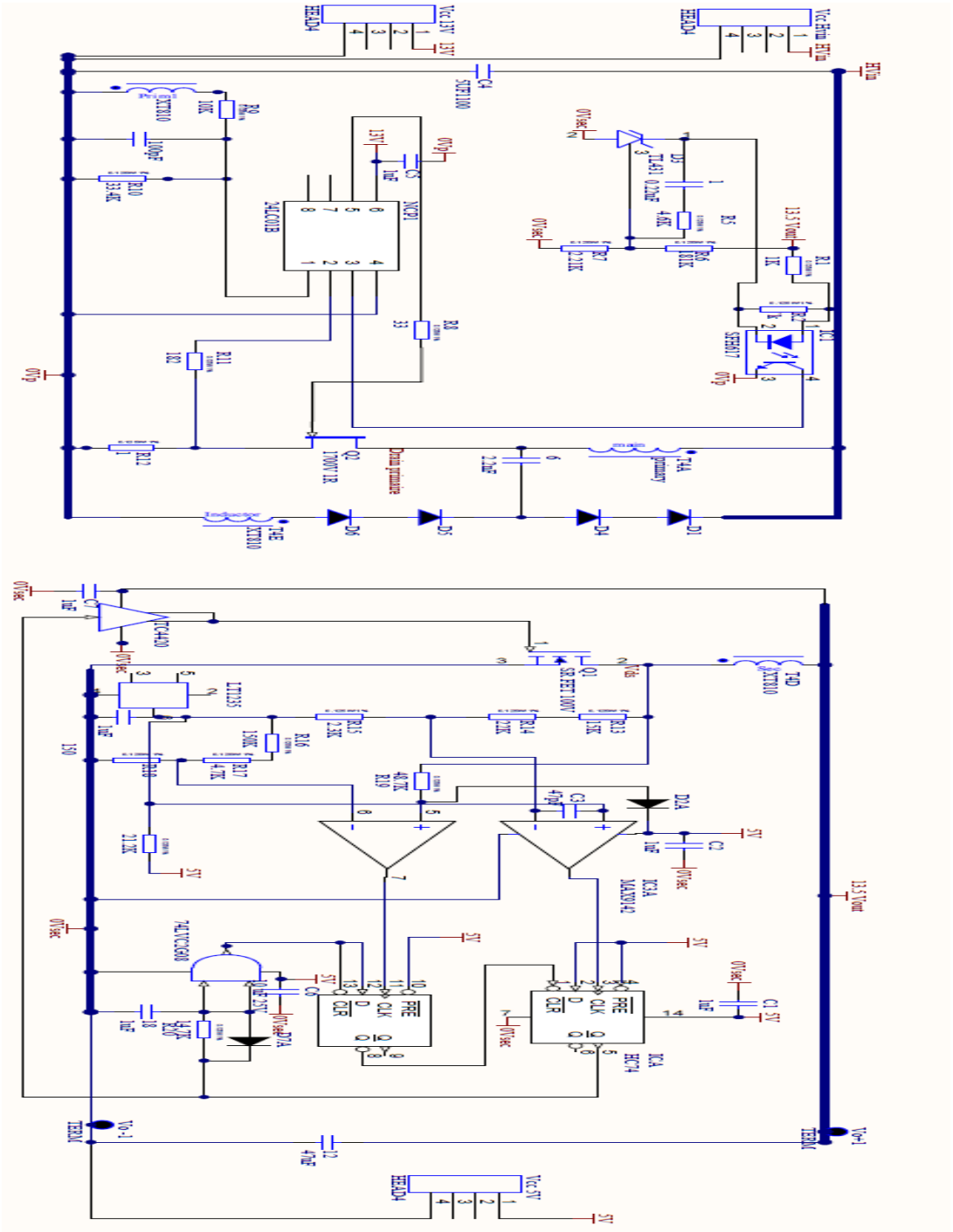
$$V_{ref} = V_{out} \cdot \left(1 + \frac{V_{in,max}}{V_r}\right) = 64.9V$$

Therefore, the diode STPS10H100CT [19] is selected which has a reverse breakdown voltage of 100V and 10A current handling capability.

For the output capacitor a 47µF 25V is chosen.

Appendix B : Schematic and PCB of the designed converter

The Altium schematic file and PCB file are included on the CD attached to the report.



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