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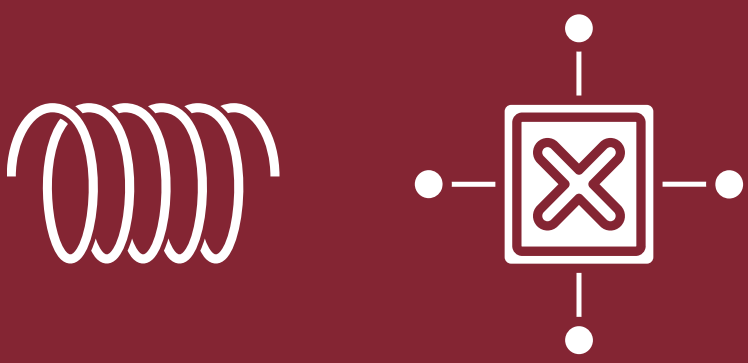

Amirhossein Jouyaeian

Hybrid Contactless Current Sensors in Standard CMOS

Hybrid Contactless Current Sensors in Standard CMOS

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
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CONTENTS

SUMMARY

This thesis presents the development of high-performance hybrid contactless current sensors in standard CMOS technology, aiming to simultaneously achieve wide bandwidth and high resolution.

Chapter 1 introduces the importance and applications of current sensors, particularly emphasizing the need for accurate, wide-bandwidth sensors in modern power electronics. It categorizes current sensors into shunt-based and contactless types and highlights the benefits of contactless sensors, especially in high-voltage applications. The chapter reviews key contactless sensing technologies—pick-up coils, Hall plates, fluxgate sensors, and magnetoresistive sensors—comparing their strengths and limitations. The motivation for using hybrid sensors, which combine coils and Hall plates to achieve a wide frequency range while maintaining accuracy, is established. The thesis objective is framed around enhancing the resolution, bandwidth, gain flatness over frequency, and thermal stability of hybrid contactless current sensors.

Chapter 2 discusses the key building blocks and design challenges involved in implementing hybrid contactless current sensors in standard CMOS technology. It begins with the design of the current rail, emphasizing the importance of differential sensing strategies to suppress stray magnetic fields. The chapter then focuses on the design and optimization of Hall plates, including a detailed explanation of a modified spinning-current technique that upmodulates the Hall voltage while keeping the offset at DC. Various readout techniques for Hall signals are compared, with a focus on achieving high resolution and low power consumption. The chapter also presents the electrical modeling of the pick-up coil used in this work, which is optimized for maximum signal-to-noise ratio (SNR). Parasitic components of the coil are analyzed, and two readout architectures—voltage mode and current mode—are evaluated, with current-mode readout demonstrating higher bandwidth by effectively bypassing parasitic capacitance.

Chapter 3 presents a 46A hybrid sensor that features a current-mode readout for the pick-up coil and a two-stage low-pass filter (LPF) with pole-zero compensation scheme to flatten the coil's differentiating response and suppress offset. In the Hall path, the spinning-current technique is combined with capacitively-coupled chopper amplifiers (CCAs) and a multiplexed ripple-reduction loop (RRL) to effectively cancel large DC offsets and suppress ripple. To block offset in the coil path, a large blocking capacitor is inserted between stages; however, this introduces a parasitic pole that degrades gain flatness unless the capacitor is sufficiently large. To address this, a compact on-chip solution was implemented by stacking MOS capacitors and MIM capacitors. Analog temperature compensation is applied in both sensing paths: the Hall plate is biased with a PTAT current source, while temperature coefficients in the coil path are balanced using TC-matched resistors. A one-time calibration scheme adjusts the Hall bias to match sensitivities between the two paths, achieving a flat gain response within ±1% accuracy and a resolution of 69 mA_{RMS} across a 5 MHz bandwidth.

Chapter 4 presents an improved hybrid sensor. A dual-differential DC servo loop (D3SL) replaces the blocking capacitor, introducing a parasitic pole well below the crossover frequency and minimizing its impact on gain flatness. This architectural modification allows the crossover frequency to be optimized for noise—lowered from 10 kHz to 2 kHz—leading to a resolution improvement from 69 mA_{RMS} to 43 mA_{RMS}. A sub-PTAT bias current is introduced for the Hall plate to reduce thermal sensitivity without risking Hall-plate saturation, and a temperature-dependent gain stage further stabilizes the response. The result is a hybrid sensor with a temperature-induced gain error of ±0.9% and ±2.7% in the coil and Hall paths, respectively, over −40 °C to 85 °C.

Chapter 5 concludes the thesis by summarizing the key findings and contributions in developing accurate hybrid contactless current sensors in CMOS technology. It highlights innovations such as the multiplexed RRL, the dual-differential DC servo loop (D3SL), and self-calibration for sensitivity matching. The chapter also outlines future research directions, including absolute sensitivity calibration, mechanical stress compensation, on-chip digitization, a three-path architecture, and using higher-order summing filters.

SAMENVATTING

Deze thesis beschrijft de ontwikkeling van hoogwaardige hybride contactloze stroomsensoren in standaard CMOS-technologie, met als doel om tegelijkertijd een brede bandbreedte en hoge resolutie te bereiken.

Hoofdstuk 1 introduceert het belang en de toepassingen van stroomsensoren, met bijzondere nadruk op de noodzaak van nauwkeurige sensoren met brede bandbreedte in moderne vermogenselektronica. Het maakt onderscheid tussen shunt-gebaseerde en contactloze sensoren, en belicht de voordelen van contactloze sensoren, vooral in hoogspanningsapplicaties. Het hoofdstuk bespreekt de belangrijkste contactloze meettechnologieën—opneemspoelen, Hall-platen, fluxgate-sensoren en magnetoresistieve sensoren—waarbij hun sterke en zwakke punten worden vergeleken. De motivatie voor het gebruik van hybride sensoren, die spoelen en Hall-platen combineren om een breed frequentiebereik te dekken met behoud van nauwkeurigheid, wordt uiteengezet. Het doel van deze thesis is het verbeteren van de resolutie, bandbreedte, versterkingsvlakheid over frequentie en thermische stabiliteit van hybride contactloze stroomsensoren.

Hoofdstuk 2 bespreekt de belangrijkste bouwstenen en ontwerpuitdagingen bij de implementatie van hybride contactloze stroomsensoren in standaard CMOS-technologie. Het begint met het ontwerp van de stroomrail, waarbij het belang van differentiële detectiestrategieën wordt benadrukt om storende magnetische velden te onderdrukken. Vervolgens richt het hoofdstuk zich op het ontwerp en de optimalisatie van Hall-platen, inclusief een gedetailleerde uitleg van een gemodificeerde spinning-current techniek, die de Hall-spanning opmoduleert terwijl de offset op DC-niveau blijft. Verschillende uitleestechnieken voor Hall-signalen worden vergeleken, met nadruk op hoge resolutie en laag energieverbruik. Ook wordt het elektrische model gepresenteerd van de opneemspoeldie in dit werk wordt gebruikt,

geoptimaliseerd voor een maximale signaal-ruisverhouding (SNR). Parasitische componenten van de spoel worden geanalyseerd en twee uitleesarchitecturen—spanningsmodus en stroommodus—worden geëvalueerd, waarbij de stroommodus superieure bandbreedte laat zien door parasitaire capaciteiten effectief te omzeilen.

Hoofdstuk 3 presenteert een 46 A hybride sensor met een stroommodus-uitlezing voor de opneemspoel en een twee-fase laagdoorlaatfilter (LPF) met een pool-nul-compensatieschema om het differentiërende gedrag van de spoel af te vlakken en offset te onderdrukken. In het Hall-pad wordt de spinning-current techniek gecombineerd met capacitief gekoppelde chopperversterkers (CCA's) en een gemultiplexte ripple-reductielus (RRL) om grote DC-offsets effectief te onderdrukken en rimpel te verminderen. Om offset in het spoelpad te blokkeren, wordt een grote blokkeringscondensator tussen de trappen geplaatst; deze introduceert echter een parasitaire pool die de versterkingsvlakheid aantast, tenzij de condensator groot genoeg is. Om dit aan te pakken, werd een compacte on-chip oplossing geïmplementeerd door MOS-condensatoren en MIM-condensatoren te stapelen. Analoge temperatuurcompensatie wordt toegepast in beide meetpaden: de Hall-plaat wordt aangestuurd met een PTAT-stroombron, terwijl temperatuurcoëfficiënten in het spoelpad worden gecompenseerd met TC-gematchte weerstanden. Een eenmalig kalibratieschema past de Hall-bias aan om de gevoeligheden tussen de twee paden op elkaar af te stemmen, wat resulteert in een vlakke versterkingsrespons binnen ±1% nauwkeurigheid en een resolutie van 69 mA_{RMS} over een bandbreedte van 5 MHz.

Hoofdstuk 4 presenteert een verbeterde hybride sensor. Een dubbel differentiële DC-servolus (D3SL) vervangt de blokkeringscondensator en introduceert een parasitaire pool ver onder de crossoverfrequentie, met minimale invloed op de versterkingsvlakheid. Deze architecturale wijziging maakt het mogelijk om de crossoverfrequentie te optimaliseren voor ruis—verlaagd van 10 kHz naar 2 kHz—wat leidt tot een verbeterde resolutie van 69 mA_{RMS} naar 43 mA_{RMS}. Een sub-PTAT biasstroom wordt geïntroduceerd voor de Hall-plaat om thermische gevoeligheid te verminderen zonder verzadiging te riskeren, en een temperatuurafhankelijke versterkingstrap stabiliseert de respons verder. Het resultaat is een hybride sensor met een temperatuuraangedreven

versterkingsfout van ±0.9% en ±2.7% in respectievelijk het spoel- en Hall-pad, over een temperatuurbereik van $-40\,^{\circ}\mathrm{C}$ tot $85\,^{\circ}\mathrm{C}$.

Hoofdstuk 5 sluit de thesis af met een samenvatting van de belangrijkste bevindingen en bijdragen aan de ontwikkeling van nauwkeurige hybride contactloze stroomsensoren in CMOS-technologie. Het benadrukt innovaties zoals de gemultiplexte RRL, de dubbel differentiële DC-servolus (D3SL) en zelfkalibratie voor het afstemmen van gevoeligheden. Het hoofdstuk schetst ook toekomstige onderzoekslijnen, waaronder absolute gevoeligheidskalibratie, compensatie voor mechanische stress, on-chip digitalisering, een driepadenarchitectuur en het gebruik van somfilters van hogere orde.

1

INTRODUCTION

Without data, you're just another person with an opinion.

W. Edwards Deming

Current sensors measure the flow of electric current in conductors and convert this information into signals that can be readily processed by other electrical systems. They enable the precise monitoring and control of electrical systems, ensuring that they function properly and can handle potentially hazardous conditions such as overloads and short circuits.

The market for current sensors is growing rapidly. In 2023, the global current sensor market was valued at around $2.8 billion and is forecast to increase to $4.7 billion by 2028, which corresponds to a compound annual growth rate (CAGR) of 10.4% [1]. This growth is mainly driven by the increasing demand for electric and hybrid vehicles, advancements in power management technologies, and the expanding adoption of smart grids.

1.1. PRINCIPLES OF CURRENT SENSING

Many physical phenomena can be used to implement current sensors. The most commonly used ones are discussed below:

- **Ohm's Law:** This states that the current (I) flowing through a conductor between two points is directly proportional to the voltage (V) between the two points and inversely proportional to

the resistance (R). Current can thus be determined by measuring the voltage drop across a known resistance.

- **Faraday's Law of Electromagnetic Induction:** This states that the induced electromotive force (EMF) in any closed circuit is equal to the negative rate of change of the magnetic flux through the circuit. Mathematically, it is expressed as:

$$\epsilon = -\frac{d\Phi_B}{dt} \tag{1.1}$$

  where ϵ and Φ_B are the induced EMF and the magnetic flux, respectively. In essence, Faraday's Law describes how a changing magnetic field can produce an electric current in a conductor. AC current can thus be sensed by measuring the induced voltage in a coil surrounding a current-carrying conductor. Note that DC current sensing is not possible.

- **Lorentz Force:** This is the total force experienced by a charged particle moving through an electromagnetic field. It is defined as:

$$\vec{F} = q\left(\vec{E} + \vec{v} \times \vec{B}\right) \tag{1.2}$$

  where $\vec{F}$ is the total force, q is the electric charge of the particle, $\vec{E}$ is the electric field vector, $\vec{v}$ is the velocity vector of the particle, and $\vec{B}$ is the magnetic field vector. The force ($\vec{F}$) consists of two components: a force in the direction of the electric field ($\vec{E}$) and a force perpendicular to both the magnetic field ($\vec{B}$) and the charge velocity ($\vec{v}$). The Hall effect arises from the Lorentz force acting on moving charges in a conductor in the presence of a magnetic field, which, in turn, creates a Hall voltage across the conductor.

To effectively compare the performance of different types of current sensors and judge their suitability for specific applications, some parameters are required to quantify their performance. Some key parameters are defined below:

- **Accuracy:** This indicates how well the output of a current sensor matches the actual current.

- **Sensitivity:** This is the ratio of the change in the output signal (e.g., voltage or current) to the corresponding change in the input current.

- **Input range:** This specifies the minimum and maximum currents that a current sensor can accurately detect.

- **Offset:** This is the output of a current sensor when there is no input current.

- **Bandwidth (BW):** This specifies the range of frequencies over which a sensor will respond to changes in current. It is closely related to the response time; a higher bandwidth enables a sensor to track rapid changes effectively.

- **Power Consumption:** This specifies the amount of power a sensor consumes during its operation.

- **Cost:** In the case of an integrated current sensor, this is directly related to the silicon area it occupies, as well as to the technology node and the complexity of the manufacturing process used. Also significant are the costs associated with calibration and testing.

The focus of this thesis is on the design of wide-bandwidth current sensors in CMOS technology. Such sensors are required to monitor and regulate the currents in modern power conversion systems, whose operating frequency is steadily increasing due to the rapid adoption of Silicon Carbide (SiC) and Gallium Nitride (GaN) switching devices. By switching faster, power converters can maintain similar performance levels with smaller energy-storage components. Switching frequencies of several hundred kHz are now common-place. Accurately monitoring and regulating such currents requires sensors with MHz bandwidths.

This thesis seeks to address the following question: *How can wide-bandwidth, accurate, and cost-effective current sensors be realized in CMOS technology?* To address this, we first need to understand the pros and cons of the various types of existing current sensors. This will be the focus of the next section.

1

1.2. TYPES OF CURRENT SENSORS

The first reliable current sensor was the galvanometer, invented by André-Marie Ampère in 1820. Early galvanometers were simple devices consisting of a wire coil suspended between the poles of a magnet. An electric current flowing through the coil created a magnetic field that interacted with the magnet's field, causing the coil to rotate.

The development of solid-state electronics led to the development of other types of current sensors. These can be divided into two categories: shunt-based current sensors and contactless current sensors. In a shunt-based current sensor, the sensing element is electrically connected to the current-carrying conductor. A contactless current sensor, however, senses the magnetic field around the conductor, and thus can be electrically isolated from it.

1.2.1. SHUNT-BASED CURRENT SENSORS

As shown in Figure 1.1, a simple way of sensing a current sensor is by measuring the voltage drop across a so-called shunt resistor [2–4]. According to Ohm's Law, this voltage drop is proportional to the flowing current, enabling accurate measurement.

Shunt-based current sensors are known for their high accuracy and resolution. Their accuracy is fundamentally limited by the accuracy of the shunt resistor, which should thus have a tight tolerance, as well as a low temperature-coefficient (TC). Metal-alloy shunts are available with tolerances down to 0.1% and with TCs as low as 100 ppm/°C

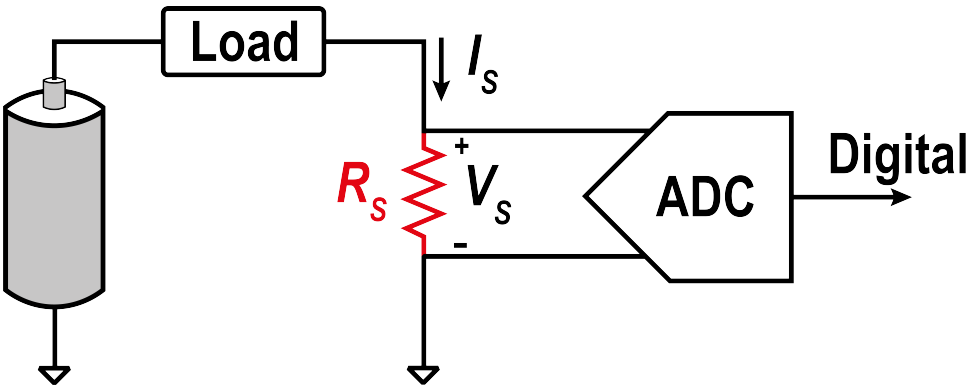

Figure 1.1: Shunt-based current sensing.

[5]. However, these are external components, which are much more expensive than on-chip resistors. Alternatively, low-cost metal shunts can be made from PCB traces, package lead frames and on-chip metal layers. However, these typically have large tolerances, as well as large TCs (0.4%/°C), and so, calibration and temperature-compensation schemes are needed, which increases system complexity [2–4, 6]. After a room-temperature calibration, gain errors of <0.25% across the industrial temperature range have been achieved [2].

Shunt-based current sensors can achieve bandwidths of up to a few hundred kilohertz. For example, [7] reports a bandwidth of 350 kHz using an integrated 400 $\mu\Omega$ shunt resistor. In another case, [8] achieves a bandwidth (BW) of 182 kHz with an external 12 mΩ resistor. However, at higher frequencies, their bandwidth is limited by the parasitic inductance of the shunt. Additionally, physical phenomena such as the skin effect and proximity effect also limit the bandwidth of shunt-based current sensors. Although compensation networks can be used, these also increase system complexity [9].

Despite their advantages, shunt-based current sensors also have several disadvantages. The voltage drop across the shunt resistor causes Joule heating, and thus a power loss that is proportional to the square of the current. Additionally, they lack galvanic isolation, making them unsuitable for applications where electrical isolation is critical. Furthermore, in low-side current sensing applications, the shunt resistor prevents a direct ground connection, while in high-side current sensing applications, the readout circuitry must handle a large input common-mode range (ICMR).

Shunt-based current sensors are used in applications such as power-grid current sensing, motor and solar inverters, power amplifiers, and smart-home energy management. They are also used in battery management units to monitor and control battery state-of-charge [10]. This is often done by Coulomb counting, which involves determining the net charge flowing into a battery by integrating its current over time.

1.2.2. CONTACTLESS CURRENT SENSORS

As shown in Figure 1.2, a contactless current sensor operates by sensing the magnetic field generated by the current flowing through a so-called current rail. Since there is no direct electrical connection between

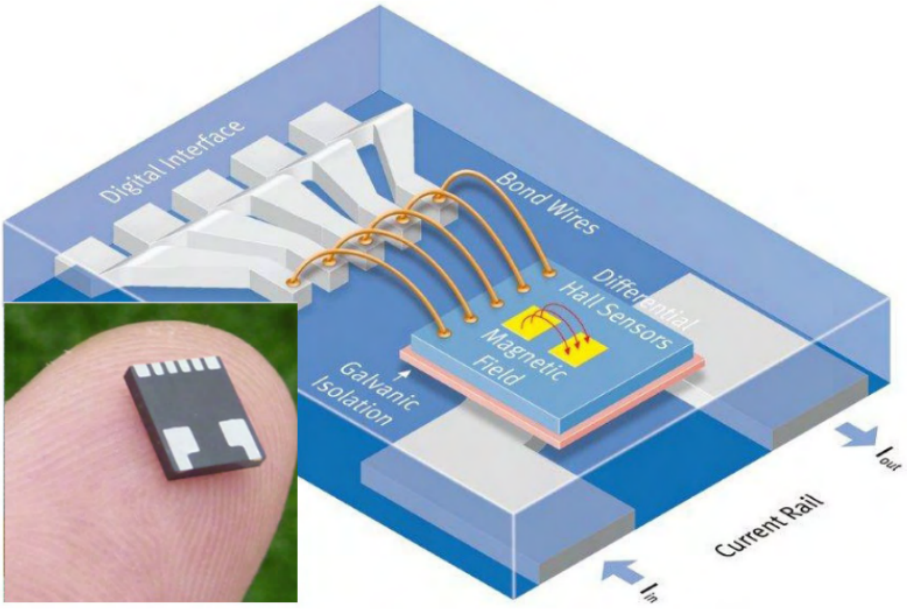

Figure 1.2: Magnetic current sensing principle.

the sensor and the current rail, contactless sensors provide galvanic isolation, which makes them suitable for high-voltage applications [11]. In addition, unlike shunt-based current sensors, there is less voltage drop and hence lower power loss.

Many aspects of the performance of a contactless current sensor are determined by the magnetic coupling between the sensing element and the current rail. Reducing the distance between them increases their coupling, thereby increasing the sensor's resolution. However, this usually comes at the expense of reduced isolation voltage.

Contactless current sensors can achieve bandwidths of tens of Megahertz. This is mainly determined by the bandwidth of the sensing element, but also by its magnetic coupling to the current rail, with the latter often being overlooked. At high frequencies, eddy currents in the current rail change the current distribution in the rail, which, in turn, changes the magnetic field at the sensing element [12].

Although contactless current sensors offer many benefits, they come with certain drawbacks. Compared to shunt-based current sensors, they typically have lower resolution, due to the indirect nature of

their operation. They are also susceptible to interference from stray magnetic fields, which reduces their accuracy in noisy environments. Furthermore, in core-based sensors, saturation or hysteresis can cause nonlinearities, thereby reducing accuracy.

An important application of contactless current sensors is in the battery management system (BMS) of electric vehicles (EVs). There, they are used to control battery charging rates, thus preventing overcharging and ensuring balanced charging across all cells. They are also used by the BMS to optimize power delivery to the motor and other systems, thus enhancing efficiency and performance. In addition, such sensors can detect abnormal currents that might indicate a potential short circuit or cell failure. In such cases, the BMS can take immediate action, such as shutting down the affected part of the battery, to prevent damage and ensure safety.

1.3. CONTACTLESS SENSING ELEMENTS

Various sensing elements can be employed in contactless current sensors, each utilizing different principles to detect magnetic fields and convert them into measurable electrical signals.

1.3.1. PICK-UP COILS

Pick-up coils operate based on Faraday's law of electromagnetic induction (see Figure 1.3). The magnitude of the induced voltage in the coil is proportional to the derivative of the magnetic field:

$$\varepsilon = -nA\frac{dB}{dt} \tag{1.3}$$

where n and A are the number of windings and the winding area, respectively. If the input magnetic field is a sine-wave with an amplitude of B_0 at frequency f, the magnitude of the induced voltage can be written as:

$$|\varepsilon| = 2\pi f \cdot n \cdot A \cdot B_0 \tag{1.4}$$

Since the main noise source of a pick-up coil is its resistance, its output noise power can be calculated as follows:

$$N^2 = 4kTR \cdot f_{BW} \tag{1.5}$$

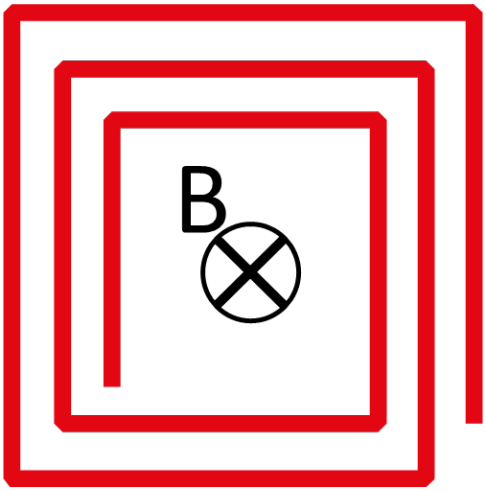

Figure 1.3: Pick-up coil.

in which R represents the coil resistance. The noise power is proportional to f_{BW}, while the signal power is proportional to f^2. Thus, the SNR at the output of a pick-up coil is proportional to the input frequency:

$$\mathrm{SNR} = \frac{P_{\mathrm{Signal}}}{P_{\mathrm{Noise}}} = \frac{\pi^2 n^2 A^2 B_0^2}{kTR} \cdot \frac{f^2}{f_{BW}} \tag{1.6}$$

As a result, pick-up coils are an attractive choice for measuring high-frequency magnetic fields. By the same token, however, they cannot sense DC signals and have poor SNR at low frequencies.

An example of a pick-up coil implementation is the Rogowski coil, an air-cored coil that is placed around a current-carrying conductor (see Figure 1.4). First introduced by Walter Rogowski more than 100 years ago [13], it has been applied in several fields, including 50 Hz grid current sensing. In the past 20 years, the basic concept has been adapted for implementation on PCBs, and bandwidths of 100 MHz [14] and 175 MHz [15] have been reported. The maximum achievable bandwidth is limited by the self-resonance of the coil. A reference design based on a PCB-based Rogowski coil achieved a bandwidth of 20 MHz and could measure currents up to 1000 A with a resolution of 12 bits [16].

An important feature of pick-up coils is that they are CMOS-compatible. Metal layers can be readily used to implement planar

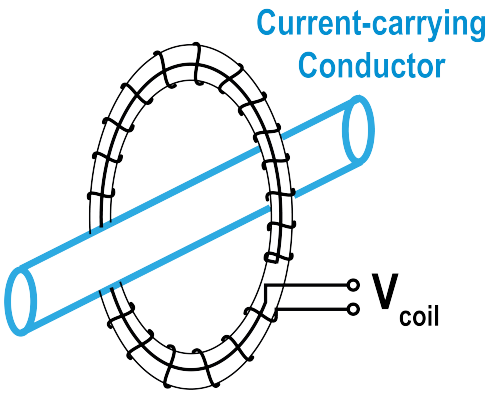

Figure 1.4: Rogowski coil.

coils. This enables the low-cost integration of pick-up coils with other on-chip readout circuits.

1.3.2. HALL PLATES

Hall plates are based on the Hall effect, which was discovered by Edwin Hall in 1879. As shown in Figure 1.5, In the presence of a normal magnetic field (B), a current flowing through two opposing terminals of a conductor produces a voltage across the other two terminals. The Hall effect is a consequence of the Lorentz force (F_L), which deflects the moving electrons in the conductor to one side of the conductor. The

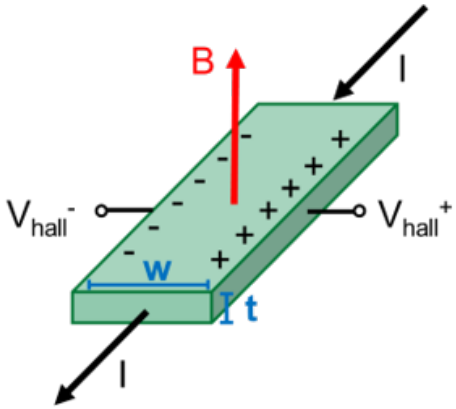

Figure 1.5: Hall plate.

Lorentz force (F_L) on the electrons can be expressed as:

$$F_L = -Bqv_d \tag{1.7}$$

where q is the magnitude of charge and v_d is the drift velocity. This force accumulates negative charges on one side and positive charges on the other side of the conductor. In equilibrium, the resulting electric force is equal to the negative of the Lorentz force:

$$qE = -Bqv_d \tag{1.8}$$

where E is the electrical field. The flowing current (I) is related to v_d:

$$I = nq \cdot w \cdot t \cdot v_d \tag{1.9}$$

in which n is the carrier concentration of the electrons, w and t are the width and thickness of the conductor, respectively. In addition, the voltage across the Hall-plate voltage (V_{Hall}) can be expressed as:

$$V_{\text{Hall}} = wE \tag{1.10}$$

Substituting eq. (1.9) and eq. (1.10) into eq. (1.8), we get:

$$V_{\text{Hall}} = \frac{IB}{nqt} = S_I IB \tag{1.11}$$

Therefore, the Hall voltage is proportional to the applied magnetic field and the flowing current and is independent of the input frequency. The constant S_I is known as the current-related sensitivity.

However, the derivation of eq. (1.11) involves some simplifying assumptions. First, it assumes that the Hall plate is infinitely long. Second, it neglects the geometry and size of the biasing and sensing contacts. These will affect V_{Hall} because they determine the current density and the electric field distribution in the plate [17]. Finally, it does not consider the effect of random deflection of charge carriers due to collisions with impurities or defects in the measured material [18]. By considering these effects, the current-related sensitivity can be rewritten as:

$$S_{I,\text{new}} = G \cdot \frac{r}{nqt} \tag{1.12}$$

where G is the Hall geometrical factor, and the scattering factor (r) is a parameter that characterizes the degree of scattering in the material. G depends on the shape of the Hall plate, the size and position of the contacts, and the strength of the magnetic field [19]. It can be evaluated by conformal mapping, boundary element methods, or finite element methods (FEMs) [18, 20–22].

Although any conducting material can be used as a Hall plate, semiconductors are superior to metals due to their lower carrier concentration (n), which leads to higher Hall sensitivity (S_{Hall}) [23]. Among semiconductors, Hall plates realized in GaN, GaAs, and InAs processes achieve the highest sensitivity [24, 25]. However, CMOS Hall plates are the most widely used because they can be co-integrated with their readout electronics. They typically consist of an n-well layer with four contacts and achieve sensitivities (S_I) between 50 to 500 V/(A·T) [18].

The sensitivity of silicon Hall plates is affected by mechanical stress. This is mainly due to changes in carrier mobility and the piezo-Hall effect. According to [26], the piezo-Hall effect varies significantly with different crystal orientations. Specifically, n-doped CMOS Hall plates oriented in {111} planes show the least sensitivity to mechanical stress, whereas those on {100} wafer planes are the most affected, being 15 times more sensitive to the stress induced by packaging.

Another source of error in Hall plates is their sensitivity drift due to temperature changes. This is primarily due to the temperature-dependent mobility of charge carriers. As temperature increases, the mobility of charge carriers decreases, leading to reduced sensitivity of the Hall plates [27].

The thermal noise of a Hall plate is produced by its equivalent Thevenin output resistance (R_{Hall}). So, it can be expressed as:

$$N^2 = 4kTR_{\text{Hall}}f_{BW} \tag{1.13}$$

Thus, the SNR of a Hall plate is inversely proportional to the input frequency:

$$\text{SNR} = \frac{P_{\text{Signal}}}{P_{\text{Noise}}} = \frac{(S_I IB)^2}{4kTR_{\text{Hall}}} \cdot \frac{1}{f_{BW}} \tag{1.14}$$

This means that the SNR of Hall plates decreases for wide bandwidths. This limits their use in wide-bandwidth applications, even though their

maximum BW is much higher (~ 1 GHz), being physically limited by the relaxation time of electrons and practically limited (~ 100 MHz) by the intrinsic capacitance of the n-well depletion layer [28–31]. For instance, [32] reports a resolution of 480 mA_{rms} with a BW of 1.7 MHz, while [33] achieves a resolution of 124 mA_{rms} with a BW of 400 kHz. Additionally, [31] achieves a BW of 1 MHz with a resolution of 70 mA_{rms}.

HALL-PLATE OFFSET

The offset of Hall plates is typically quite large (up to a few mV), and can be orders of magnitude larger than the desired signal [34]. This is mainly due to the combined effects of lithographic inaccuracy, process spread and mechanical stress [12, 19, 35].

As shown in Figure 1.6, a Hall plate under typical operating conditions can be modelled as an unbalanced Wheatstone bridge, in which one arm has a resistive deviation ΔR. The differential output voltage can then be calculated as follows:

$$V_{\text{Hall,OS}} = I_{\text{Bias}} \left(\frac{2R}{4R+\Delta R} \cdot (R+\Delta R) - \frac{2R+\Delta R}{4R+\Delta R} \cdot R \right) \tag{1.15}$$

This can be approximated as:

$$V_{\text{Hall,OS}} \approx \frac{\Delta R}{4} I_{\text{Bias}} = \frac{\Delta R}{4R} V_{\text{Bias}} \tag{1.16}$$

where V_{Bias} is the bias voltage across the Hall plate. If V_{Bias} is 1.2 V, then 1% resistor mismatch ($\frac{\Delta R}{R} = 1\%$) results in a 3 mV offset, which, with a

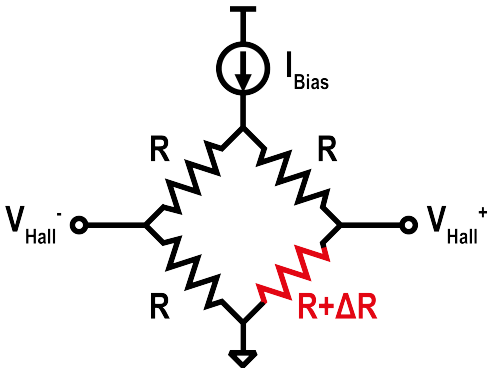

Figure 1.6: Hall sensors modeled as a Wheatstone bridge.

typical sensitivity of 60 mV/T, corresponds to a 50 mT equivalent input magnetic field. This is quite large and thus, in most applications, offset cancellation techniques must be used to prevent the desired magnetic signal from being completely overwhelmed.

A commonly used offset cancellation technique is orthogonal-pairing (see Figure 1.7) [36]. This involves connecting two nominally identical Hall plates in parallel, with the connections of one rotated by 90°. If the mismatch of the two Hall plates is equal, the resulting offsets will be zero. While this technique can eliminate systematic offsets due to, e.g., mechanical stress, the reduction of random offsets due to, e.g., manufacturing imperfections is limited to a factor of $\sqrt{2}$. In practice, this technique typically achieves an order-of-magnitude reduction in offset [17]. However, it doubles both area and power consumption.

In another bid to reduce offset, the so-called X-Hall sensor was proposed [28, 29, 37]. As shown in Figure 1.8, an X-Hall sensor comprises four small sense contacts and four large bias contacts. The bias current (I_{Bias}) is applied to two opposing bias contacts, while the other two are grounded. The two pairs of diagonally opposing sense contacts are shorted together. The sensor is thus simultaneously biased in four different directions in a symmetrical fashion. In [29], a residual offset of 560 μT is reported, which is lower than typical values of Hall

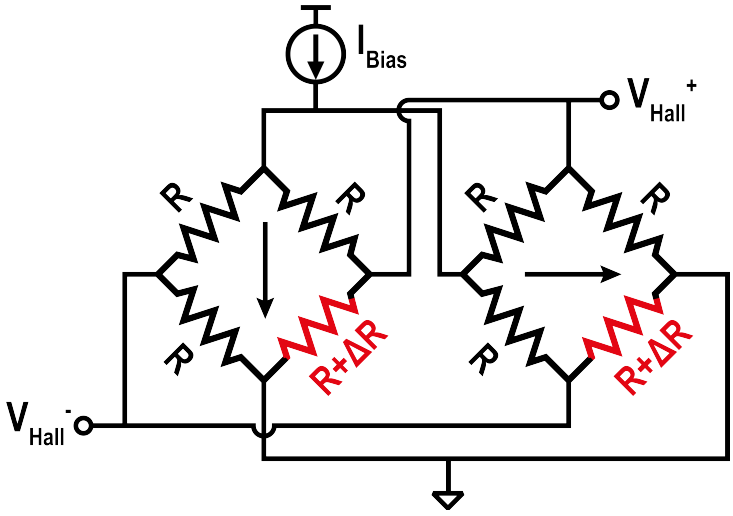

Figure 1.7: Orthogonal-pairing technique.

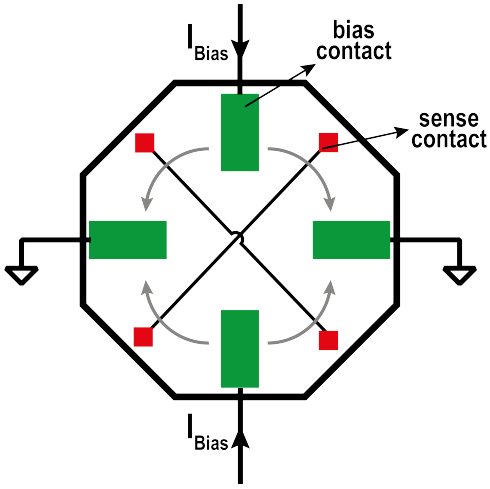

Figure 1.8: X-Hall sensor.

plate offset [18]. However, like the orthogonal-pairing technique, it does not compensate for the effects of random mismatch.

A much more effective way to reduce Hall plate offset is the spinning-current technique [35, 38, 39]. This involves periodically rotating the direction of the bias current. This causes the polarity of the offset to change, while the Hall voltage remains constant. A 2-phase spinning current scheme is shown in Figure 1.9. In phase 1, the output voltage is $V_{\text{Hall}} + V_{\text{Offset}}$, while in phase 2, the output voltage is $V_{\text{Hall}} - V_{\text{Offset}}$. Averaging the voltages from the two phases cancels the offset voltage, leaving only the Hall signal. Further details about this technique are discussed in chapter 2.

1.3.3. FLUXGATE SENSORS

Fluxgate sensors operate by leveraging the well-defined magnetic saturation of certain ferromagnetic materials. They typically consist of four coils: two excitation coils and two sensing coils, which, as shown in Figure 1.10, are wound around two parallel ferromagnetic bars. Short current pulses (I_{exc}, several nanoseconds) are then applied to the excitation coils to drive the bars into magnetic saturation. The excitation coils are configured to generate opposing excitation magnetic fields in the bars. In the absence of an external field, the voltages in

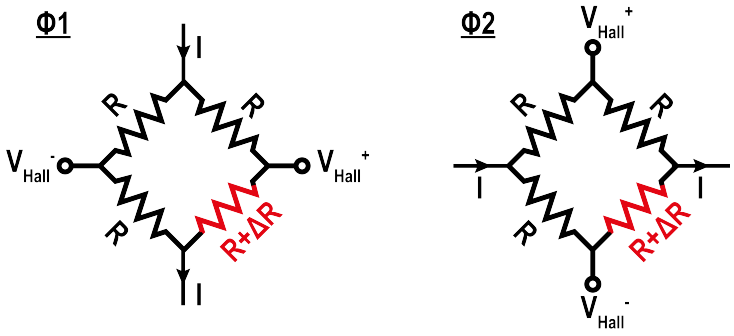

Figure 1.9: Operation of a 2-phase spinning current.

the sensing coils induced by the exciting fields cancel each other, and thus, the output voltage (V_{Sense}) is zero. In the presence of an external magnetic field, one of the bars will be saturated earlier than the other, resulting in spikes in the output V_{Sense}.

Compared to Hall plates, fluxgate sensors have superior sensitivity and can achieve resolutions as low as 500 nT with a BW of 125 kHz [40], and offsets as low as 900 nT [41]. However, they are usually more expensive, since additional manufacturing steps are required to realize their ferromagnetic cores. In addition, their linear input range is typically limited to less than 100 μT [42], as larger fields may saturate the

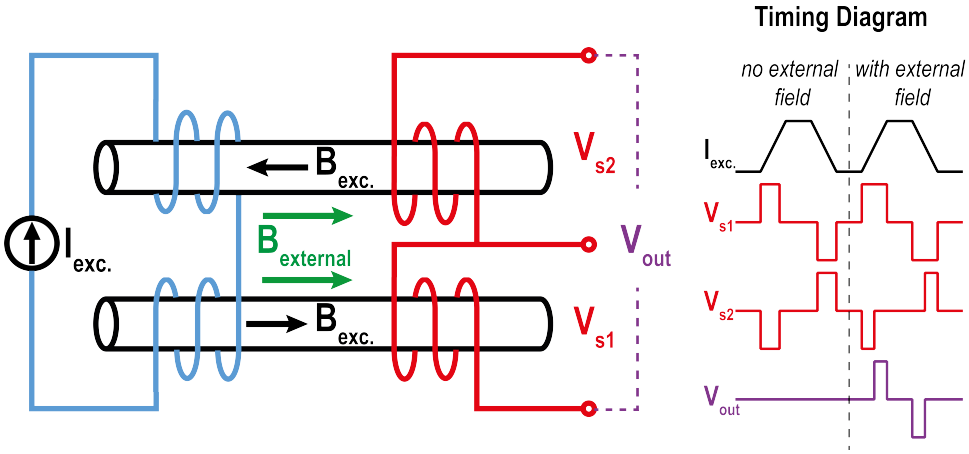

Figure 1.10: Fluxgate sensing.

core. To increase their input range, fluxgate sensors are often used in a closed-loop configuration. However, their bandwidth is then limited by stability requirements. For instance, an input range of ±2 mT with a bandwidth of 47 kHz is demonstrated in [43]. In another example, a bandwidth of 200 kHz is reported in [41].

1.3.4. MAGNETORESISTIVE SENSORS

Magneto resistors (MRs) are devices whose electrical resistance varies as a function of the strength and direction of an applied magnetic field. The most commonly used MR devices are based on the Anisotropic Magneto Resistance (AMR), Giant Magneto Resistance (GMR), and Tunnel Magneto Resistance (TMR) effects [44–46]. Their basic structure is shown in Figure 1.11. AMR sensors are the simplest, consisting of only one ferromagnetic layer (the free layer). Both GMR and TMR sensors consist of three layers: an intermediate layer is sandwiched between two ferromagnetic layers. They have two main differences. Firstly, the intermediate layer (the spacer layer) in a GMR sensor is a non-magnetic metal (Cu, etc.), while the intermediate layer (the barrier layer) in a TMR sensor is an insulator layer. Secondly, the flowing current is applied horizontally to the film surface in a GMR sensor. However, the current flows vertically to the film surface in a TMR sensor. A TMR sensor works based on the quantum-mechanical tunnelling effect, and its sensitivity is 20 and 6 times larger than that of AMR and GMR sensors, respectively [47]. Using TMR technology, [48] achieves a BW of 1 MHz with a resolution of 9.5 mA_{RMS} over a noise BW of 100 kHz. In another example, [49] reports a BW of 2 MHz with a resolution of 206 nT.

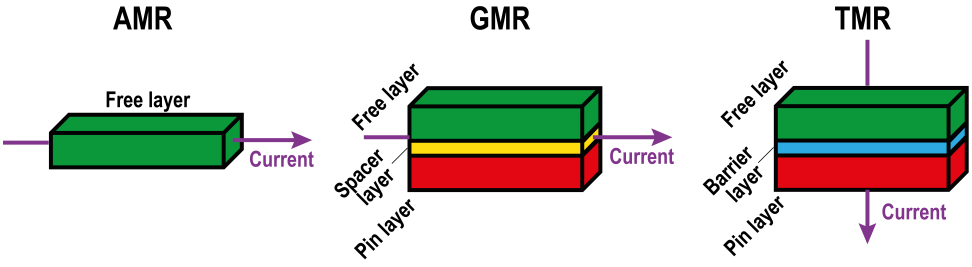

Figure 1.11: Different types of magneto-resistive (MR) sensors.

MR sensors, like Fluxgate sensors, suffer from similar drawbacks. They require additional fabrication processes, making them a costly option. Further drawbacks of MR sensors include nonlinearity and zero-point error.

1.3.5. HYBRID (COIL + HALL) CONTACTLESS CURRENT SENSORS

Both pick-up coils and Hall plates are CMOS compatible. However, they have quite different characteristics. Pick-up coils can provide high sensitivity and resolution at high frequencies, but they cannot sense DC signals. On the other hand, Hall plates can sense DC signals, but their resolution decreases as signal bandwidth increases. By using pick-up coils for high frequencies and Hall plates for low frequencies, as shown in Figure 1.12, their strengths can be combined. This enables the development of hybrid contactless current sensors with both high resolution and wide bandwidth [12, 38, 50–53].

While hybrid contactless current sensors effectively cover a wide frequency range without resolution degradation, they face several challenges. They inherit the issues associated with Hall plates, such

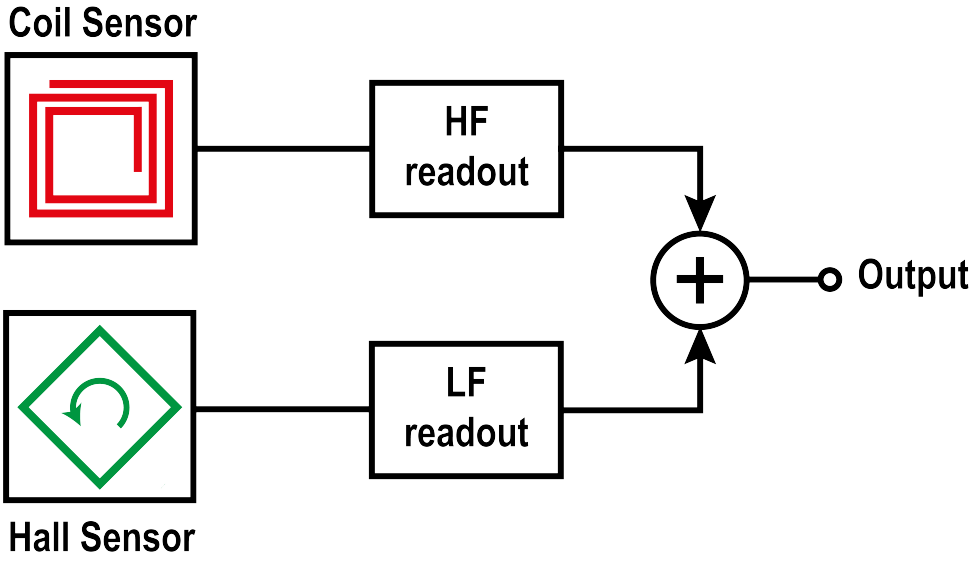

Figure 1.12: Hybrid magnetic current sensor.

as large raw offset and gain drift over temperature. Maintaining a flat frequency response is another major challenge. This is because the two sensors have different readout circuitry and so any mismatch between them can cause gain-flatness errors in their overall frequency response. For instance, [53] achieves a 5 MHz bandwidth, but its gain varies by more than ±6% across this range.

Although a number of hybrid sensors have been proposed to address these challenges, they have significant limitations. In [12], a planar pick-up coil is combined with a horizontal Hall plate. As shown in Figure 1.13, in the coil path, an open-loop integrator reads out the differentiated coil voltage. To prevent the integrator from saturating on its own offset, it employs a DC servo loop. To compensate for the extra pole introduced by the DC servo loop, while maintaining a flat frequency response, a bulky 10 μF off-chip capacitor is used. The sensor achieves a resolution of 480 mA_{rms} in a 3 MHz bandwidth.

Another hybrid current sensor is proposed in [50] (see Figure 1.14). It consists of a chip mounted on a current rail implemented as a PCB trace. A helix-shaped Rogowski coil and a vertical Hall plate measure the horizontal magnetic field generated by the rail current. In order to achieve a flat frequency response, a two-stage integrator

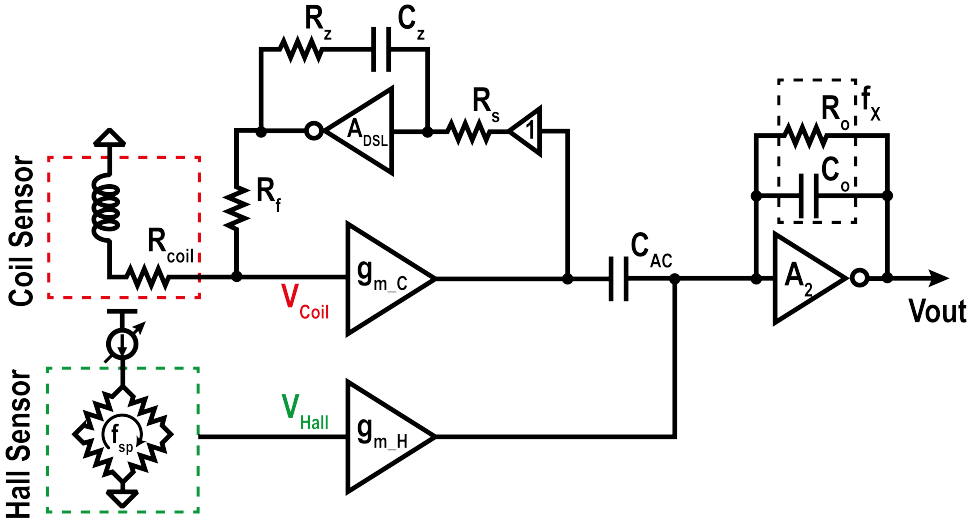

Figure 1.13: A hybrid current sensor with a 480mA resolution in a 3MHz BW [12].

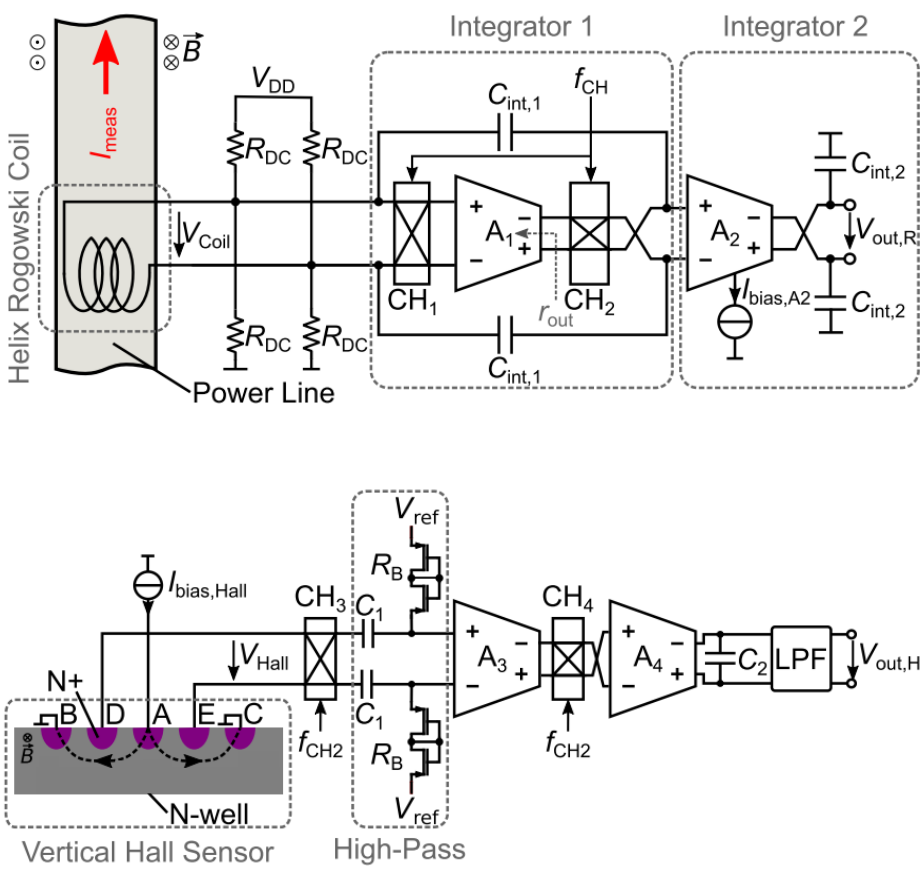

Figure 1.14: A hybrid current sensor with 15.3MHz BW and 710mA resolution (reprinted from [50].)

with an on-chip pole-zero cancellation scheme is used in the coil path. However, trimming is required to compensate for pole-zero mismatch, making it susceptible to sensitivity drift over temperature. Finally, an off-chip crossover network combines the outputs of the coil and Hall paths. This sensor reports a bandwidth of 15.3 MHz and a resolution of 710 mA_{rms} but its gain-flatness error is still quite high at ±3.7%.

Table 1.1: State-of-the-Art Integrated Wideband Contactless Current Sensors

Source	JSSC'19 [32]	JSSC'22 [40]	CT433 [48]	APEC'19 [50]	ACS37030 [53]
Sensor Type	Hall	IFG	TMR	Hybrid	Hybrid
Resolution (mA_{rms})	480	11[a]	13.5[c]	710	50
Input Range (A)	±300	±53[a]	±65	±60	±65
BW (MHz)	1.7	0.125	1	15.3	5
Power Consumption (mW)	13.2	100[b]+13	30	63.5	66
Gain Flatness	N/A	N/A	N/A	±3.7%	±6%
CMOS Compatibility	✓	✗	✗	✓	✓

[a]Conversion rate = 45μT/A
[b]Full-range power
[c]Noise BW = 100 kHz

1.4. THESIS OBJECTIVES

Contactless current sensors provide a superior solution for high-voltage applications since they provide galvanic isolation. Table 1.1 lists a number of integrated wideband current sensors that utilize contactless sensing elements. Fluxgate and TMR sensors can both achieve superb resolution ($< 20\,mA_{rms}$). However, the non-CMOS fabrication of fluxgate sensors adds complexity and increases cost, while TMR sensors suffer from inherent nonlinearity and zero-point error [40, 48]. In contrast, Hall-based current sensors are CMOS compatible. However, they face a fundamental trade-off between noise and bandwidth (BW): as BW increases, resolution reduces. Among various contactless current sensors, hybrid current sensors emerge as the most suitable option for applications requiring both wide bandwidth and high accuracy [50, 53]. These sensors consist of Hall plates and pick-up coils, which are the only CMOS-compatible solutions. So, they can be easily integrated with readout circuitry on a single chip, enabling low-cost current sensing. They can potentially break the noise-versus-BW trade-off, offering much better resolution compared to other types.

However, achieving high accuracy involves more than just achieving high resolution. An accurate current sensor must also exhibit low drift across PVT variation, as well as over frequency, which remains a key challenge for hybrid sensors. This aspect remains unresolved in existing solutions. For example, over frequency, [50] and [53] cannot achieve gain-flatness errors better than ±3.7% and ±6%, respectively.

This thesis aims to improve the accuracy of CMOS hybrid contactless

current sensors. This involves maximizing the resolution and minimizing the residual offset of the sensor. As mentioned earlier, the main challenge in the design of such sensors is achieving a flat frequency response. Therefore, the system must be carefully designed to deal with the gain mismatch between the two paths and the effect of parasitic poles/zeros in their readout transfer functions (TFs). Finally, since the sensitivity of both Hall plates and pick-up coils are temperature-dependent, the gain variation over the industrial temperature range (−40 °C to +85 °C) must be compensated.

1.5. THESIS ORGANIZATION

The rest of the dissertation is organized as follows. Chapter 2 provides an overview of the readout techniques for the sensing elements of hybrid current sensors. In particular, the spinning current technique, as an effective solution to reduce Hall-plate offset, is described. Additionally, various compensation techniques aimed at minimizing sensitivity drift due to temperature variations and mechanical stress are presented. Furthermore, the design and implementation of Hall plates, pick-up coils and current rails in CMOS processes are discussed.

Two prototypes of CMOS hybrid contactless current sensors and their measurement results are then presented. Chapter 3 describes the first hybrid current sensor that senses the coil current instead of its voltage. An analog temperature compensation scheme is proposed to reduce the gain drift in the coil path. The current spinning technique reduces the offset of the Hall plates, and a multiplexed ripple-reduction loop suppresses the resulting ripple.

Chapter 4 presents a hybrid current sensor with an area-efficient dual-differential DC servo loop. The dual-differential DC servo suppresses the coil-path offset while having a negligible effect on the gain flatness around the crossover frequency. In addition, the optimum crossover frequency to maximize the resolution is investigated in this chapter. Fabricated in a standard 0.18 μm CMOS process, the current sensor achieves a resolution of 43 mA in a 5 MHz bandwidth.

Finally, Chapter 5 concludes the thesis, summarizes its original contributions, and provides an outlook for future work.

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2

HYBRID CONTACTLESS CURRENT SENSORS

2.1. INTRODUCTION

In a contactless current sensor, the current flowing through a current rail generates a magnetic field, which is then detected by a nearby sensing element. As discussed in Chapter 1, hybrid sensors, which use a combination of Hall plates and pick-up coils as their sensing elements, are the most suitable option for realizing contactless current sensors in standard CMOS technology.

The design of a hybrid contactless current sensor is challenging. To enhance its resolution and stray field immunity, its current rail should be designed to provide a high coupling factor to the sensing elements. The latter should themselves be optimized to achieve the maximum SNR in the chosen CMOS technology. Hall plates should be designed for minimum offset, while pick-up coils need to achieve a wide bandwidth. The design of the associated readout circuitry is also challenging, because the output of Hall plates is typically at the millivolt-level, while that of pick-up coils is proportional to frequency and thus has a wide dynamic range.

In this chapter, we will explore the design considerations and challenges involved in developing hybrid contactless current sensors.

2.2. CURRENT RAIL

A major advantage of contactless current sensors is that they provide galvanic isolation between their current rails and their sensing elements. However, they are sensitive to interference from stray (external) magnetic fields since these are indistinguishable from the field generated by the current being measured. Such stray fields may originate from nearby electrical equipment, the earth's magnetic field, or other unintended sources.

2.2.1. DIFFERENTIAL SENSING

Differential sensing is an effective way to mitigate the impact of stray magnetic fields. It involves the use of two sensing elements to measure a field gradient. This cancels out homogenous stray fields, such as the Earth's magnetic field. Thus, common-mode fields can be suppressed by subtracting the outputs of the sensing elements.

Differential sensing can be realized in various ways. For example, in [1], two sets of Hall/coil and in [2], two Hall plates are placed on both sides of a current rail (see Figure 2.1(a)). As the sensing elements are both at the same distance from the current rail, they sense magnetic fields that are equal in magnitude but opposite in polarity.

Another differential sensing approach is shown in Figure 2.1(b). In this method, a hole is drilled in the middle of a current rail, and the sensing elements are placed inside the hole. Due to symmetry, the hole splits the rail current into two halves. This creates a horizontal magnetic field gradient across the hole. This method is often used in high-power applications in which the current rail is a relatively large bus bar (a solid metal bar that can carry large currents).

2.2.2. THE CURRENT RAIL USED IN THIS WORK

In this work, the current rail is made from the low-resistance (250μΩ) lead frame of a packaged chip, which was originally developed for use in a contactless current sensor based on Hall sensors [3]. As shown in Figure 2.2, it is S-shaped, which ensures that magnetic fields with opposite directions are generated above the slits in the lead frame. Consequently, differential sensing can be achieved by positioning sensing elements above these slits.

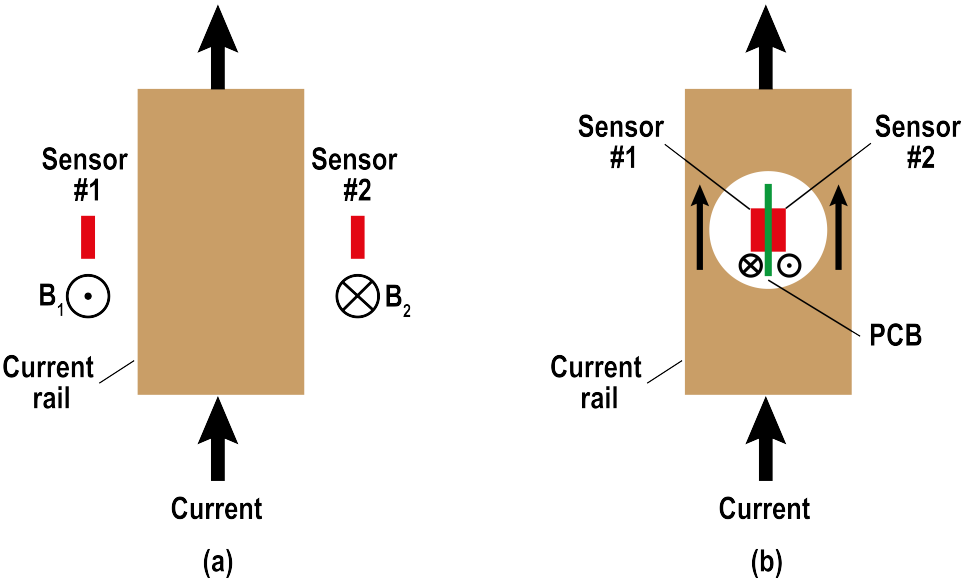

Figure 2.1: Differential sensing by placing two sensing elements (a) on both sides of a current rail (b) inside a hole in a current rail.

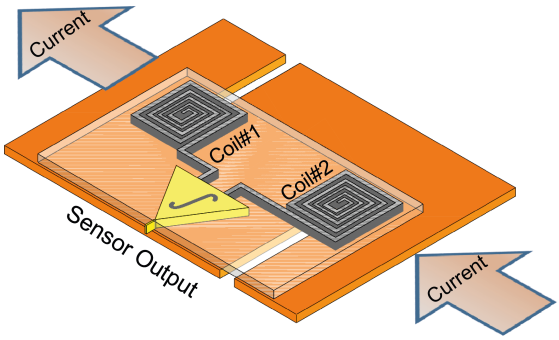

Figure 2.2: The S-shaped current rail used in this work

Another benefit of employing an S-shaped current rail is that it concentrates the magnetic field above its slits, thus effectively doubling the coupling factor ($\sim 2\times$) compared to that of a straight current rail (Figure 2.1(a)). Using the finite-element (FEM) method, the simulated magnetic field generated by the S-shaped current rail is shown in

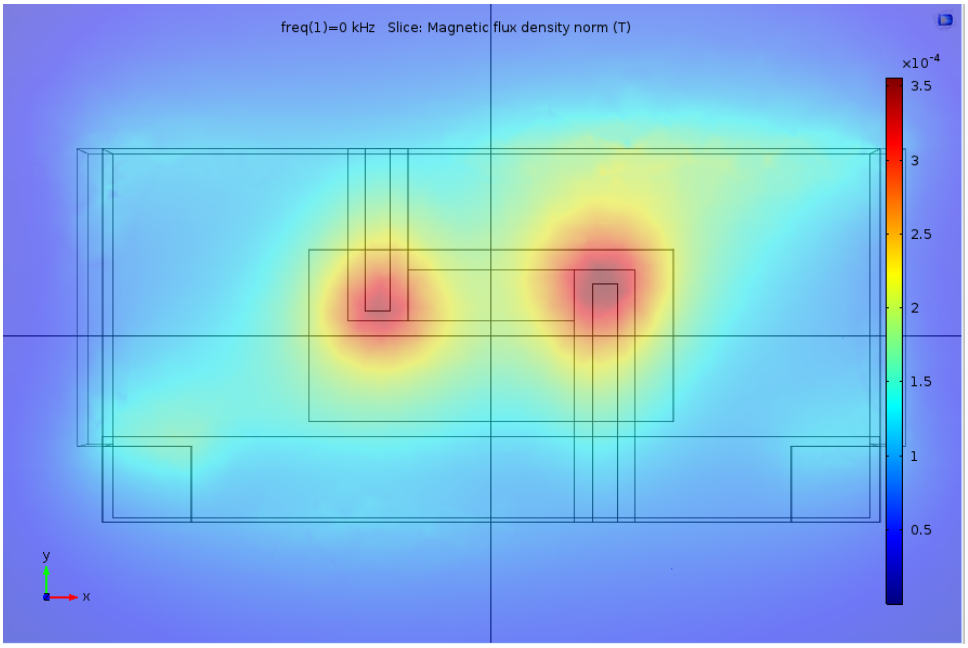

Figure 2.3: Simulated magnetic field distribution (with 1A DC current) on top of the current rail.

Figure 2.3. If the coils are 200µm above the rail, the resulting coupling factor, or current sensitivity, is about 283µT/A.

It is important to note that due to the presence of eddy currents in the current rail, the coupling factor is frequency-dependent. At low frequencies, the current in the rail is homogeneously distributed. At high frequencies, however, most of the current will flow via the edges of the lead frame. According to simulations, the coupling factor then decreases by approximately 6% at frequencies above 200kHz (see Figure 2.4). This reduction depends on several factors: (1) the geometry of the lead frame, particularly the slit shapes; (2) the height of the coils above the lead frame; (3) the dimensions of the coils; and (4) the assembly tolerances. Given the complexity of this topic, the optimal design of the rail warrants further discussion and investigation, but this is beyond the scope of this thesis.

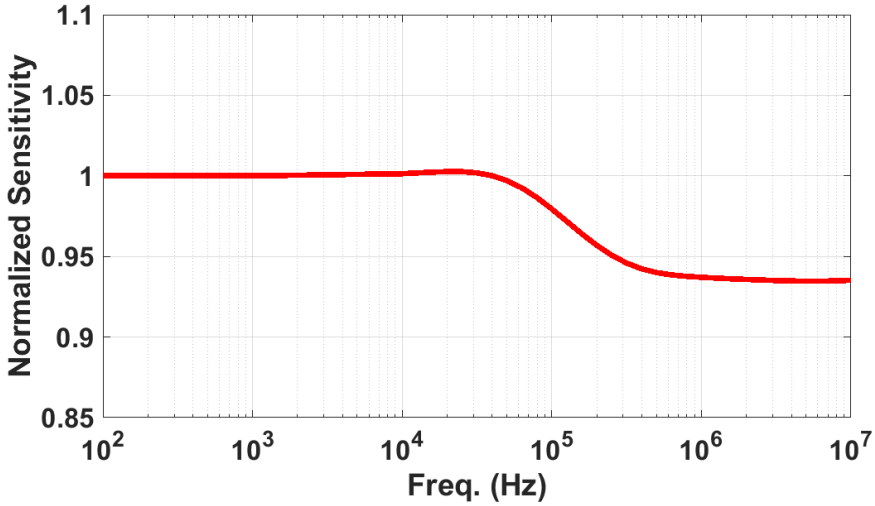

Figure 2.4: FEM-Simulation normalized sensitivity flatness vs. frequency.

2.3. HALL-PLATE DESIGN

This section describes the Hall plate used in the prototypes described in Chapters 3 and 4, as well as their key design considerations.

To enable differential sensing, two Hall plates are positioned above the slits of the current rail. Each Hall plate consists of four Hall devices organized in a 2×2 matrix (see Figure 2.5). The Hall devices are located close together to ensure that they match well and are at a uniform temperature. They are connected in parallel such that their bias currents flow in different directions during various spinning phases. To minimize the effect of the magnetic fields they generate, the wires carrying these currents are arranged diagonally and positioned above the center of the Hall devices. The resistance of the wires is minimized and well-matched to minimize potential bias-voltage fluctuations during the spinning phases, which could lead to increased offset and ripple.

Each Hall device is a square with quarter-circle contacts at its corners. Several vias connect the n-well diffusion to the metal interconnect, effectively reducing the contact resistance. Using quarter-circle contacts avoids high electric field concentrations near the contact edges. This, in turn, significantly reduces self-heating, ensures a uniform temperature

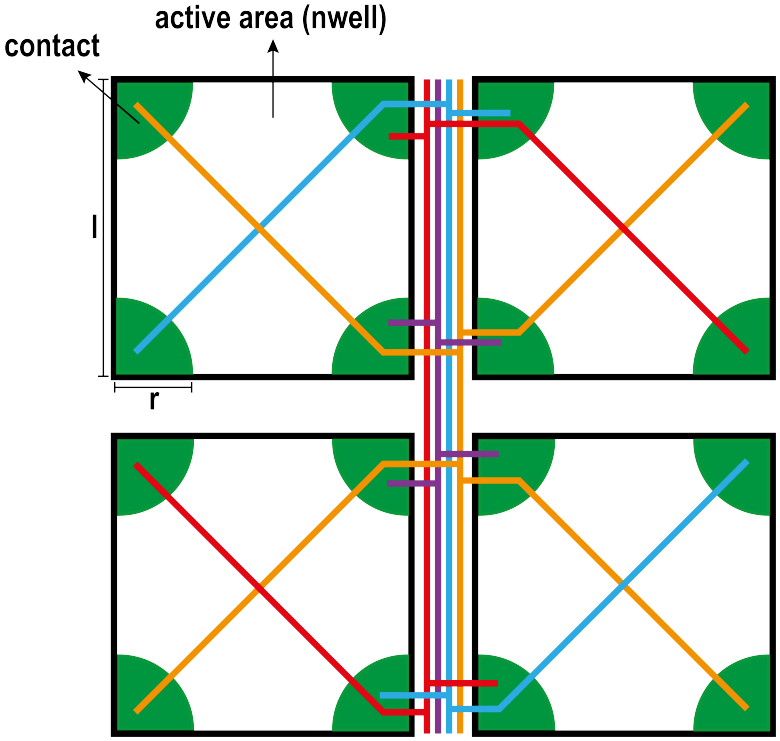

Figure 2.5: The Hall plate used in this work.

distribution, and minimizes thermo-offsets. Furthermore, this design is also simple and compact.

Each Hall device is characterized by two critical dimensions: the square's edge length (l) and the radius (r) of the contacts' quarter-circle. Another key parameter, denoted by λ, is the effective number of squares, defined as the ratio of the Hall device's input resistance (R_{in}) to the n-well sheet resistance (R_{sheet}). It is solely determined by the r/l ratio.

To maximize the signal-to-noise ratio (SNR) relative to the power dissipation in a Hall device, i.e., SNR/$\sqrt{P}$, the ratio G/λ must be maximized, where G represents the Hall geometrical factor [4]. For a square plate with large or medium-sized contacts, G can be approximated as [5]:

$$G \approx \frac{\lambda^2}{\sqrt{\lambda^4 + \lambda^2/2 + 4}} \tag{2.1}$$

As illustrated in Figure 2.6, the maximum value of G/λ occurs at approximately $\lambda \sim 1.4$. To achieve this, the radius of the quarter-circle contacts should be set to approximately 25% of the square's edge length, i.e., $r/l = 0.25$ (see Figure 2.7).

The voltage distribution of the designed Hall plate with a normalized

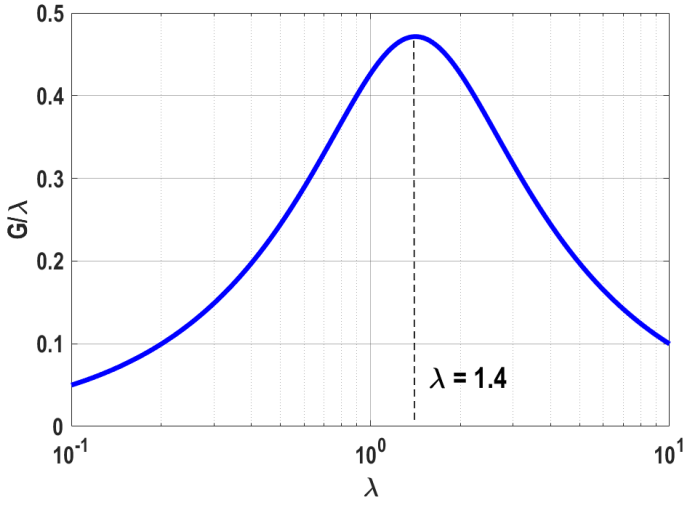

Figure 2.6: G/λ vs. λ.

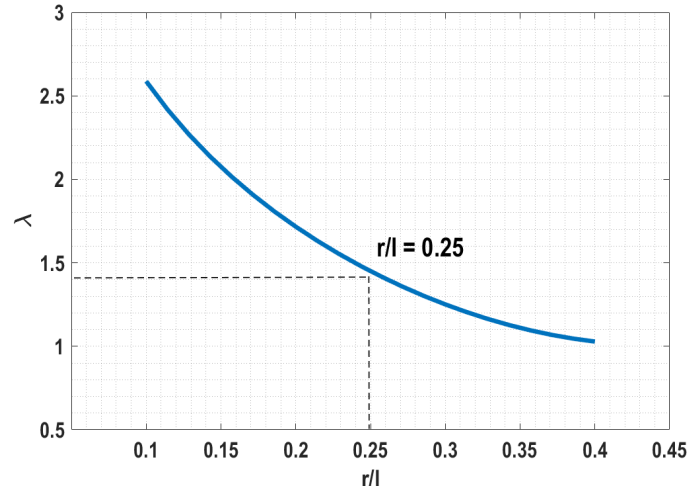

Figure 2.7: λ vs. r/l.

sheet resistance ($R_{\text{sheet}} = 1\,\Omega$) under a 1A bias current is depicted in Figure 2.8. In this configuration, current flows from the upper-left to the lower-right corner of the device. The simulation was performed in COMSOL.

Although smaller Hall devices can be made, they should be large enough to avoid velocity saturation, as this increases their nonlinearity and residual offset [6]. To prevent velocity saturation at n-type doping levels ranging from 10^{10} to $10^{18}\,\text{cm}^{-3}$, the electric field should stay below $10^5\,\text{V/m}$. Choosing an edge length (l) greater than $70\,\mu\text{m}$ ensures this for a 1.8V supply. The corresponding electric field profile for the Hall plate is shown in Figure 2.9.

2.4. READOUT OF HALL PLATES

The output of a Hall plate is a millivolt-level signal that is often accompanied by a large offset. Additionally, this signal is highly

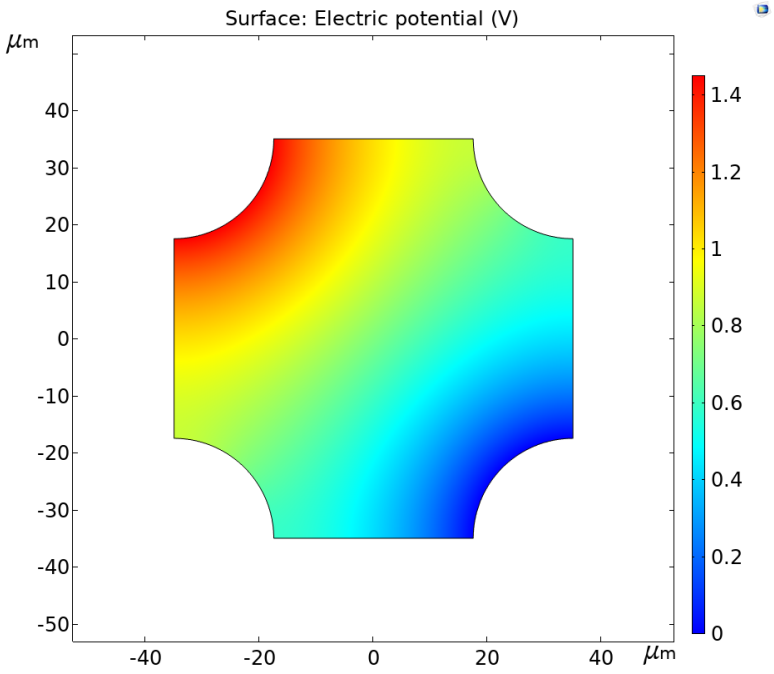

Figure 2.8: Simulated voltage distribution of the Hall plate at zero magnetic field ($R_{\text{sheet}} = 1\,\Omega$, bias current = 1A) .

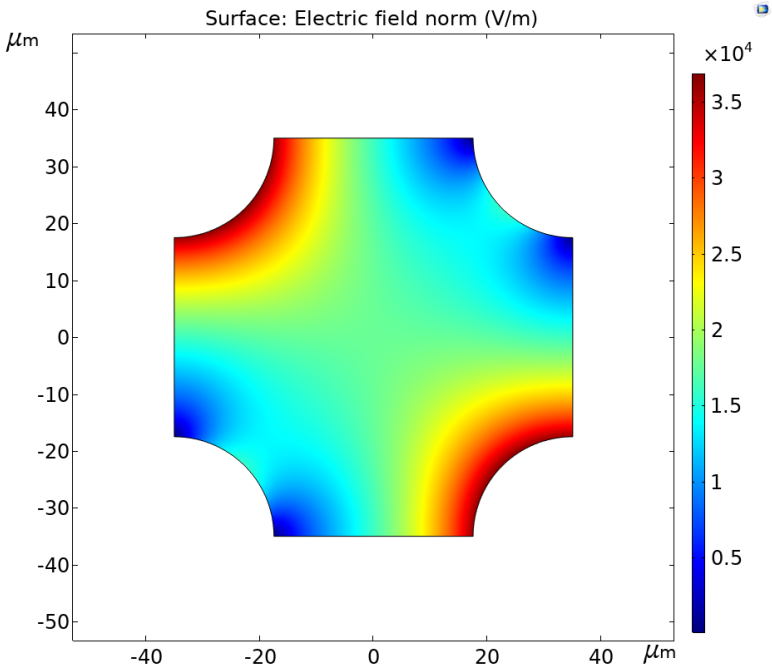

Figure 2.9: Simulated electric field distribution of the Hall plate (bias current = 1 A).

sensitive to variations in temperature and mechanical stress. Therefore, a precision readout circuit is required to separate the Hall signal from the unwanted offset, amplify it, and then stabilize it.

2.4.1. SPINNING-CURRENT TECHNIQUE

The spinning-current technique, first introduced in 1989 [7], is a dynamic offset cancellation method that can achieve residual offsets of a few (tens) of μT. It involves periodically changing the direction of the bias current in a Hall plate and then averaging the resulting output voltages. As discussed in section 1.3.2, this effectively cancels the offset while preserving the Hall signal.

Even with spinning, there will be some residual offset. This is mainly due to electrical nonlinearity, caused by the JFET effect and thermal variations across different phases [6], which produce slightly different Wheatstone bridge models in each phase. Consequently, the offset

cannot be completely eliminated.

One source of residual offset is the JFET effect. Ideally, the resistance of all the arms in the bridge model of a Hall plate (see Figure 2.10) are equal (R), i.e., $\beta = 1$. However, the biasing current flowing through the n-well modulates the width of the depletion region between it and the p-type substrate, and thus its resistance (see Figure 2.10). Since they are at a higher voltage, this depletion region is thicker in the arms that are connected to the bias-current source, and so the corresponding resistors are larger ($\beta > 1$). Due to the JFET effect, the Hall-plate offset voltage will be slightly different in each spinning phase and so cannot be fully cancelled after averaging.

To reduce the Hall-plate offset, the number of spinning phases can be increased. This improves the averaging effect and effectively reduces the residual offset. A 4-phase spinning current scheme is illustrated in Figure 2.11. It can be seen that the polarity of the offset flips during each phase while the Hall signal (V_{Hall}) remains unchanged. The offset (V_{Offset}) can then be cancelled by averaging the output (V_{out}). In [8], a residual offset of 50 μT was achieved with two spinning phases, which dropped to 10 μT in [2] using four-phase spinning. Finally, [9] achieves an offset of only 3.65 μT using an eight-phase spinning technique. It is important to note that to achieve such low offset levels, dynamic offset cancellation techniques must be used to reduce the offset of the readout

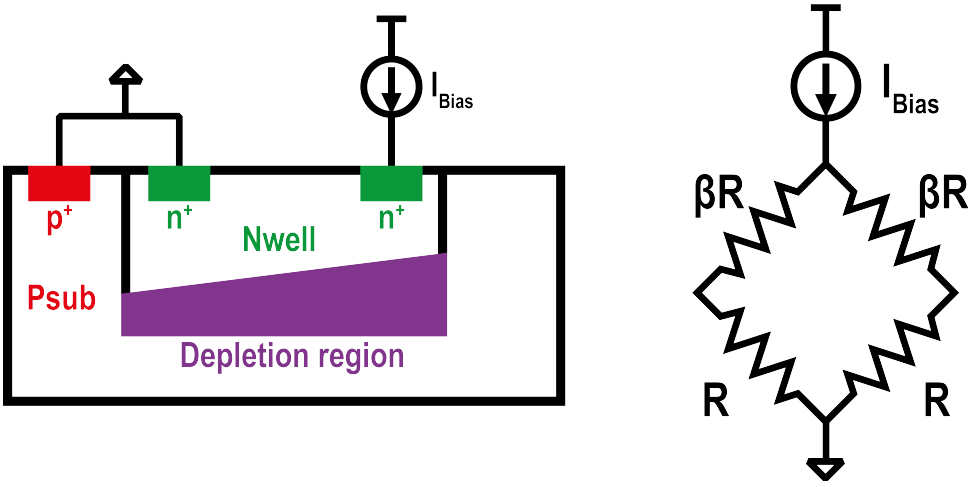

Figure 2.10: JFET effect in Hall plates.

circuitry. For example, in [9], nested-chopping and dead-banding are utilized to minimize the readout offset [10].

The spinning-current technique is quite similar to the well-known chopping technique, so it can be modelled in a similar manner (see Figure 2.12). Since the offset polarity changes in every phase, the offset voltage is modulated to twice the spinning frequency ($2f_{sp}$) in a 4-phase spinning scheme.

An amplifier is required to boost the millivolt-level Hall voltage (V_{Hall}). Unfortunately, it also suffers from offset (V_{OS}). Although trimming, chopping, or autozeroing can be employed to reduce amplifier offset [11–13], a simpler approach is to use the modified spinning-current technique [1, 14, 15].

The modified spinning-current technique and its equivalent circuit model are illustrated in Figure 2.13 and Figure 2.14. Compared to conventional spinning, the readout pins are also swapped during each phase. As a result, the offset remains at DC while the signal is upmodulated to twice the spinning frequency ($2f_{sp}$). This is

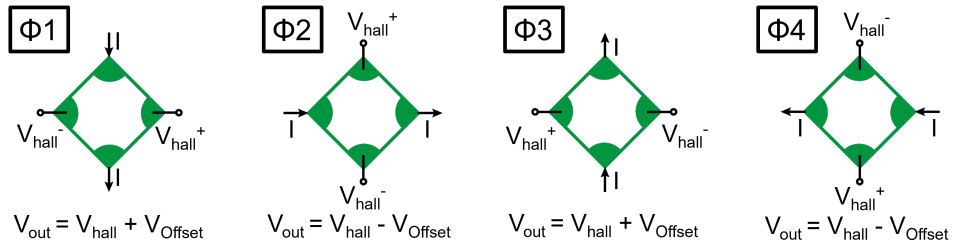

Figure 2.11: Operation of a 4-phase spinning current.

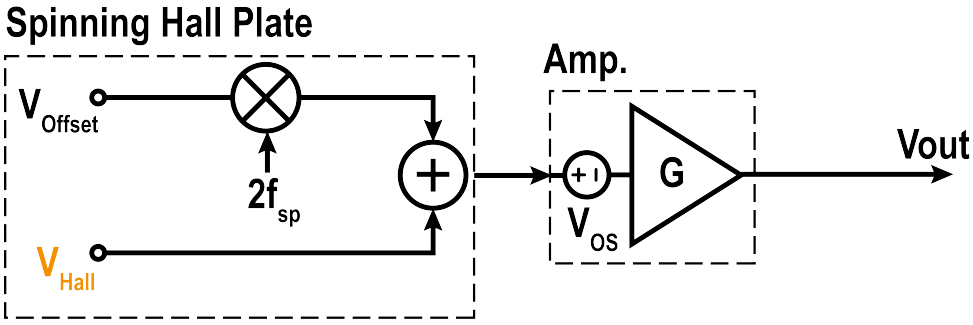

Figure 2.12: Spinning-current circuit model.

equivalent to chopping the Hall signal, but without the need for extra chopper switches and their associated charge injection. By applying this technique, the amplifier's offset (V_{OS}) is added to the Hall-plate offset (V_{Offset}). After amplification, a second chopper can be used to upmodulate the combined offset and convert the Hall signal back to DC. A key requirement is that the amplifier has enough gain at the effective chopping frequency ($2f_{sp}$), which may increase its power consumption somewhat.

2.4.2. RIPPLE-REDUCTION TECHNIQUES

As mentioned earlier, the spinning-current technique separates the Hall signal from the unwanted offset by upmodulating the offset and turning it into ripple. Although ripple is less harmful than offset, it must be suppressed, as it is also an error in the sensor's AC output.

One way to suppress spinning ripple is low-pass filtering. The ripple creates tones at the harmonics of the spinning frequency ($f_{sp}, 2f_{sp}, \ldots$),

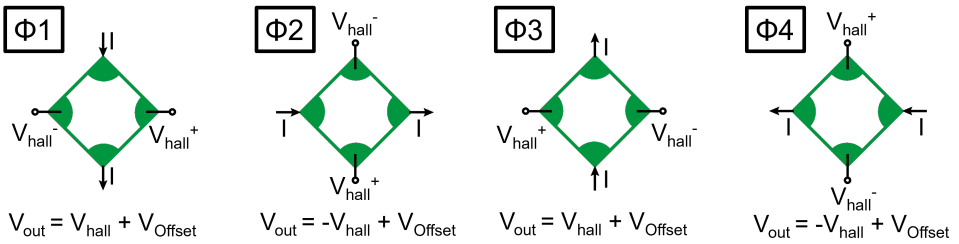

Figure 2.13: Operation of a modified 4-phase spinning current.

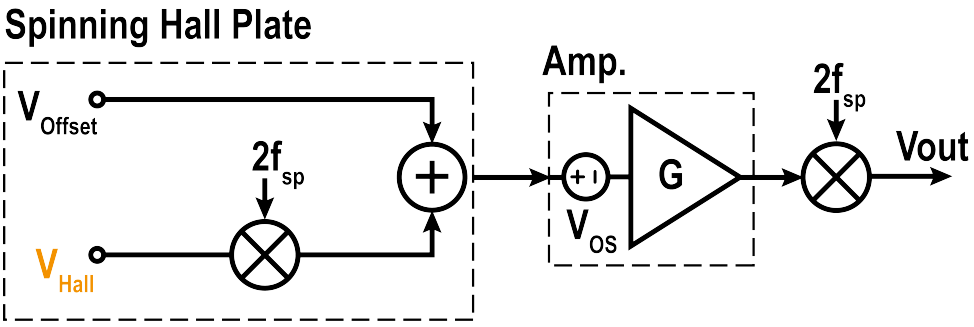

Figure 2.14: Modified spinning-current circuit model.

and so a low-pass filter (LPF) can be employed to suppress them. However, creating a filter with an ideal brick-wall response is impossible and so there will be some residual ripple. Using a practical first-order LPF with a gradual roll-off will dramatically reduce sensor BW. For instance, consider the use of a first-order LPF with a Hall sensor with 10 mT input-referred ripple (caused by the equivalent Hall-plate offset) at $2f_{sp} = 100$ kHz. To achieve 10 μT input-referred ripple, 60 dB attenuation is required, which means the LPF corner frequency must be 1000 times less than $2f_{sp}$, i.e., 100 Hz.

Increasing the spinning frequency (f_{sp}) to increase sensor BW is not an attractive solution since it increases the residual offset. This is mainly due to the spinning switches' charge injection and clock feedthrough [16]. Charge injection occurs when each of the spinning switches turns off, while clock feedthrough is a similar effect that occurs when the clock signals of the switches leak into the output signal. By increasing the spinning frequency, both of these effects get worse. Insufficient thermal settling of the Hall plate is another cause of residual offset, as it impacts the homogeneity of the n-well. At high spinning frequencies, the settling time decreases, worsening the issue of residual offset.

Another way to suppress Hall plate ripples is by using a ripple-reduction loop (RRL) [17]. As shown in Figure 2.15, a RRL consists of a ripple detector to extract the ripple at $2f_{sp}$, a chopper demodulator to convert the ripple back to DC, and an integrator. The integrator provides high DC gain in the RRL to enable Hall-plate offset cancellation.

Using a RRL does not limit sensor BW. However, it does cause a narrow notch at $2f_{sp}$, which deteriorates the gain flatness of the sensor. From another point of view, the sensor cannot sense any input current at twice the spinning frequency since it cannot be distinguished from the Hall-plate offset.

To address this issue, [1] proposes a multipath architecture, in which a spinning-current Hall sensor is used in a low frequency (LF) path, while a non-spinning Hall sensor is used in a high-frequency (HF) path. As shown in Figure 2.16, in the LF path the spinning-current technique is used to reduce the Hall-plate offset. The spinning ripple is then suppressed via a RRL. In the HF path, the spinning-current technique is not required since any offset in this path is rejected via the blocking

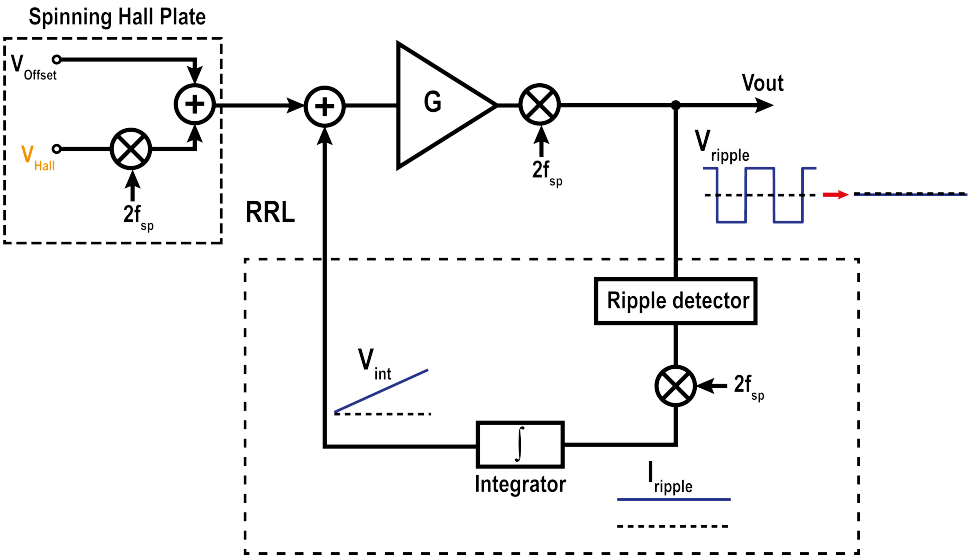

Figure 2.15: RRL for a spinning Hall plate.

capacitor C_1. Finally, the two paths are combined smoothly by the final stage, built around A_2. R_1, together with the RC network around A_2 (R_0 and C_0) form a first-order LPF with a corner frequency of $f_X = \frac{1}{2\pi R_0 C_0}$, while C_1 forms a first-order high-pass filter (HPF) with the same corner frequency. Thus, the gain of the HF path will fill the LF notch caused by the RRL.

It should also be noted that an alternative solution to address the RRL notch issue is to operate the RRL in spread-spectrum mode, combined with randomized spinning-current sequences, as proposed in [18]. This approach spreads the ripple energy over a wider frequency range, preserving the gain flatness of the sensor.

As mentioned in section 2.4.1, the actual offset of the 4-phase spinning Hall plate is a 4-level signal (see Figure 2.17). The dominant component is at DC, while the remaining ripple can be decomposed into three AC orthogonal components: two at f_{sp} and one at $2f_{sp}$. The component at $2f_{sp}$ cannot be distinguished from the main Hall signal and so cannot be canceled. It appears as a residual offset after the final chopper demodulator. The other components can be suppressed by using RRLs. Since the components are orthogonal, three RRLs can work in parallel to suppress each of the ripple components [1].

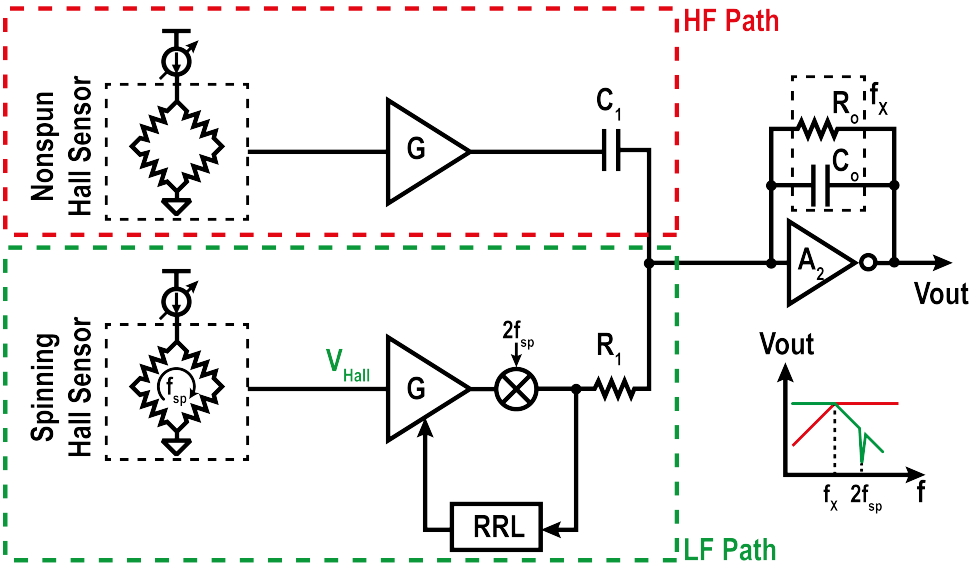

Figure 2.16: Combining a spinning Hall sensor and a non-spinning Hall sensor [1].

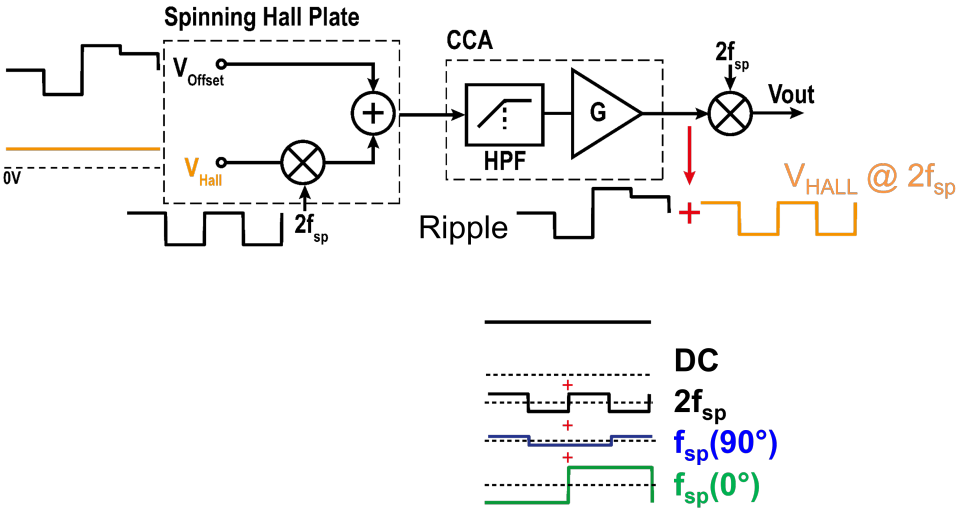

Figure 2.17: 4-phase spinning ripple and its decomposition.

2.4.3. AMPLIFICATION STAGE

Amplifiers are commonly used to boost the Hall signal. Below are some critical factors to consider when designing such amplifiers:

- **Gain:** Since the Hall signal is relatively small, an accurate and large gain, usually > 60 dB, is required to boost the Hall signal.
- **Input impedance:** This should be high input impedance to avoid loading the Hall plate, which will change its biasing current and alter its characteristics.
- **Noise:** The noise contribution of the amplifier should not exceed that of the Hall plate.
- **Offset:** As mentioned in 2.4.1, the spinning technique can reduce Hall-plate offset below 50 μT. In a proper design, the amplifier's offset should be less than that of the Hall plate.
- **Bandwidth:** The amplifier's bandwidth should be large enough to handle the upmodulated Hall signal. In 4-phase modified spinning, the Hall signal is upmodulated to twice the spinning frequency ($2f_{sp}$). So, the amplifier must have a flat frequency response of at least between $2f_{sp} - f_{in}$ and $2f_{sp} + f_{in}$.
- **Power consumption:** This should be minimized through the use of low-power topologies and optimized circuit design.

Based on the above requirements, a precision instrumentation amplifier (IA) is a promising solution for reading out a Hall plate. An IA is a type of differential amplifier with high input impedance, high common-mode rejection ratio (CMRR), and low offset voltage. Different architectures can be employed to realize an IA:

- **Two-opamp IA:** Such amplifiers have been used to read out Hall plates [17, 19]. As shown in Figure 2.18, this topology has high input impedance, since the input signal is connected to the non-inverting inputs of both opamps. Low-offset can be achieved by applying the chopping technique. The main drawback of this topology is that it requires the use of two opamps.

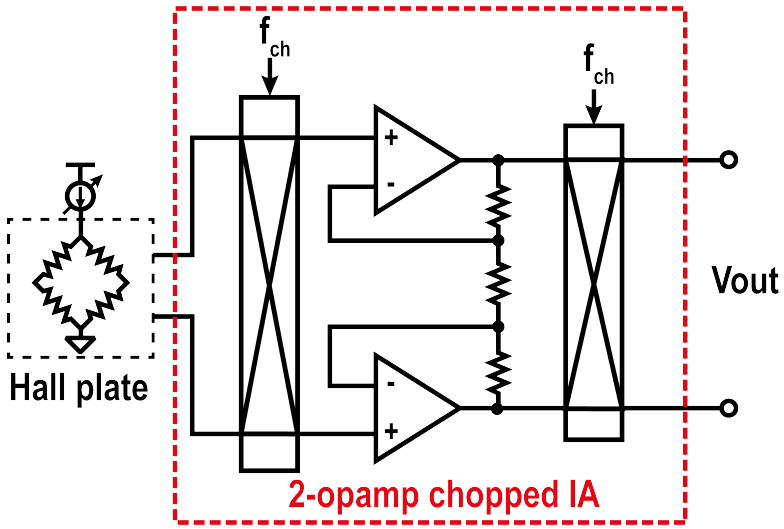

Figure 2.18: Two-opamp chopped IA.

- **Differential-Difference Amplifier (DDA):** In [20], a DDA is used to read out a Hall plate. As shown in Figure 2.19, it consists of two differential input stages with high input impedance and a shared output stage [21]. It requires less circuitry than the two-opamp IA, and the chopping technique can also be used to achieve low offset.

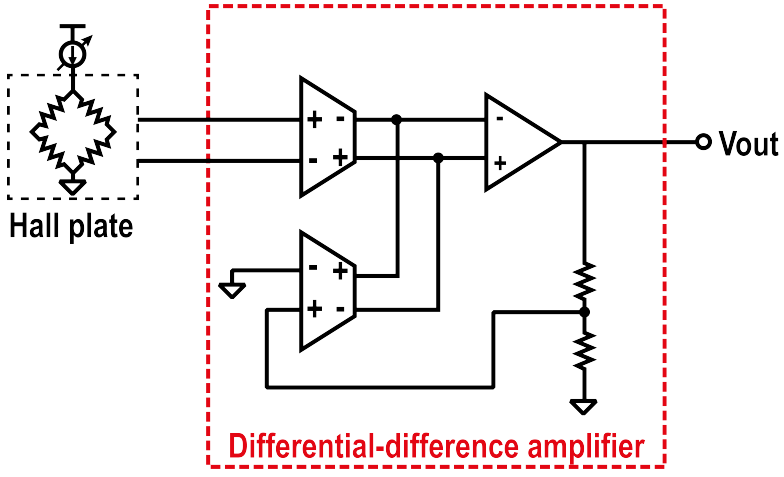

Figure 2.19: Differential-difference amplifier (DDA).

- **Capacitively-Coupled Chopper IA (CCIA):** As shown in Figure 2.20, the Hall plate is coupled to the amplifier via capacitors, which block the input common-mode voltage. Input choppers are used to enable the sensing of DC input signals. Although the chopper upmodulates the readout offset and flicker noise, it limits the input impedance of the readout [22]:

$$Z_{\text{in}} = \frac{1}{2\pi f_{\text{ch}} C_{\text{in}}} \tag{2.2}$$

  To reduce the loading effect of the readout circuit, the chopping frequency f_{ch} and the input capacitor C_{in} must be carefully chosen. To set the input common-mode (CM) of the amplifier, feedback resistors can be employed. These, along with feedback capacitors, define the high-pass corner frequency of the CCIA. To push this corner to lower frequencies, high-value resistors are required. These resistors (in the GΩ range) can be implemented using pseudo-resistors [23, 24] or switched resistors [25–27] in an area-efficient manner. Due to its low offset, low flicker noise, and high power efficiency, this topology is a promising solution for reading out Hall plates.

- **Transimpedance IA (TIA):** In the above topologies, the Hall voltage is read out, which requires high input impedance. Alternatively,

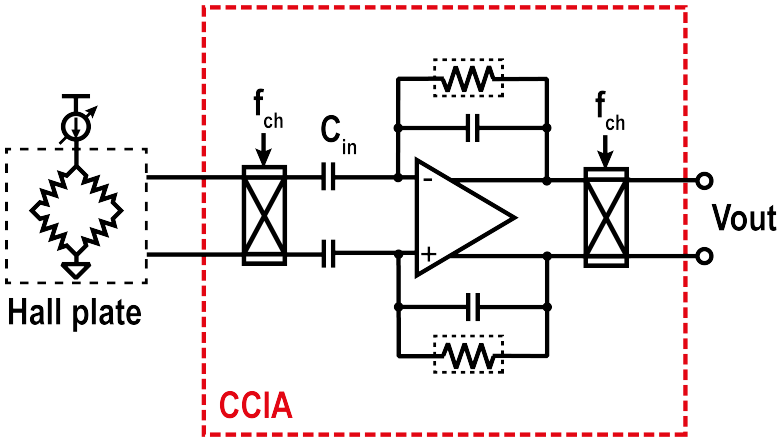

Figure 2.20: Capacitively-coupled chopper IA (CCIA).

the Hall current can be read out [8, 28, 29] using a transimpedance IA (TIA) with a very low input impedance (see Figure 2.21). Simplicity is the main advantage of this topology. However, due to the use of resistive feedback, the noise performance of a TIA is typically worse than that of a CCIA.

2.4.4. COMPENSATION TECHNIQUES FOR SENSITIVITY DRIFT

The sensitivity of CMOS Hall plates is susceptible to variations induced by mechanical stress and temperature variations. Such sensitivity drift is a significant challenge, as it can compromise the accuracy and reliability of these sensors in practical applications.

Sensitivity drift over temperature can be mitigated by calibration. This involves measuring the Hall plate's sensitivity at different temperatures, and then correcting for any drift by modifying the bias current. Such calibration is usually performed during manufacturing, with bias current settings for various temperatures established and stored. When the sensor is in operation, an integrated temperature sensor monitors ambient conditions, allowing the system to utilize the pre-stored calibration data to correct for sensitivity drift in real-time [30]. However, this method requires thorough characterization of both the Hall plate and the temperature sensor, which can be quite complex.

An alternative compensation method utilizes an on-chip AC magnetic field reference instead of a temperature sensor [31, 32]. This method consists of a feedback loop that adjusts the bias current to keep the

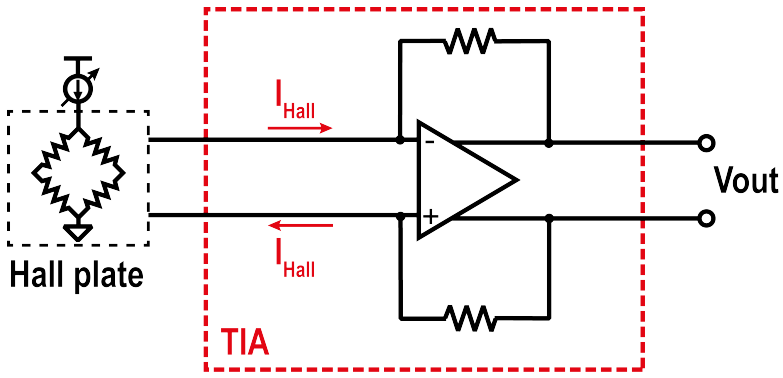

Figure 2.21: Transimpedance IA (TIA).

output of the Hall plate constant in the presence of the reference field. This not only helps reduce sensitivity drift over temperature, but it also addresses the effect of mechanical stress and aging. However, the calibration must be conducted as a periodic background process, which could lead to increased power consumption and chip area. Notably, the reference signal must not interfere with the main signal, necessitating orthogonality between them. In wide-band applications, achieving this orthogonality in the frequency domain is impractical. A promising solution in differential current sensors involves using a common-mode magnetic field as the reference, ensuring that the reference and main signals do not interfere [31].

To reduce the effect of mechanical stress, a symmetrical layout can help distribute stress more evenly across the device, reducing the piezoresistive effect. Another way to reduce the impact of stress is by using optimized packaging. Furthermore, making differential measurements and using calibration techniques, such as analog pre-compensation [7, 33, 34] and digital compensation [35, 36], can be utilized.

2.5. PICK-UP COIL DESIGN

To sense a vertical AC magnetic field, a planar pick-up coil can be employed (see Figure 2.22). Its design should consider factors such as the desired operating frequency, the number of turns, the coil's size, and the required sensitivity. In general, larger coils with more turns will have higher sensitivity but also higher parasitic capacitance, which can reduce their intrinsic BW.

As shown in Figure 2.23, the lumped-element model of a pick-up coil consists of a voltage source, its series parasitic inductance (L) and resistance (R), and a parasitic capacitor (C) connected in parallel. The voltage source is proportional to the derivative of the magnetic field, the coil area and its number of turns (N). The parasitic resistance can be calculated as:

$$R = \frac{D_{\text{in}} + D_{\text{out}}}{w} \times 2N \times R_{\text{sh}} \tag{2.3}$$

where D_{in} and D_{out} are the input and output diameters of the pick-up coil, respectively. R_{sh} is the sheet resistance of the metal layer used to

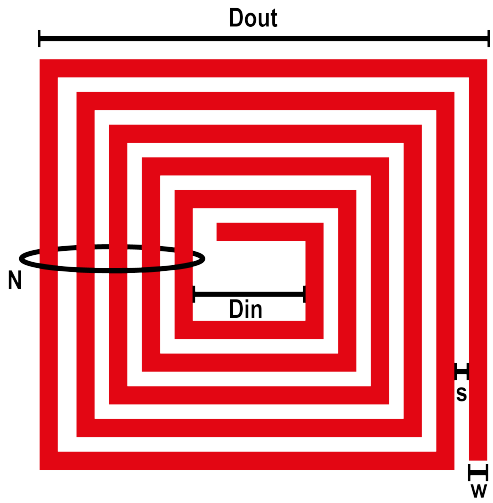

Figure 2.22: Coil layout and its parameters.

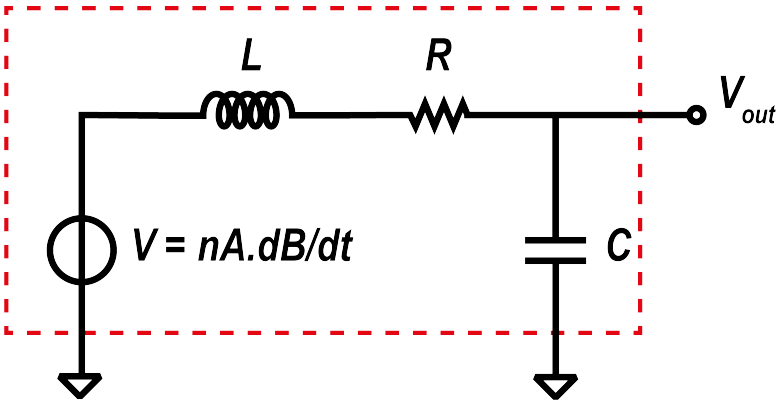

Figure 2.23: Lumped model of an unloaded pick-up coil.

implement the planar coil, w is the width of the coil conductor, and s is the spacing between adjacent turns. To obtain an expression for a planar coil inductance (L), the modified Wheeler formula can be used [37]. Using this, L can be expressed as:

$$L = K_1 \mu_0 \frac{N^2 D_{\text{avg}}}{1 + K_2 \rho} \tag{2.4}$$

in which K_1 and K_2 are layout-dependent coefficients. For a square planar coil, these coefficients are 2.34 and 2.75, respectively. In the

above formula, D_{avg} is the average of D_{in} and D_{out}, i.e., $D_{avg} = \frac{D_{in}+D_{out}}{2}$. Finally, ρ is the fill ratio, defined as:

$$\rho = \frac{D_{out} - D_{in}}{D_{in} + D_{out}} \tag{2.5}$$

The dominant part of the parasitic capacitance of a planar coil is its substrate capacitance. This capacitance can be calculated as:

$$C = \varepsilon_{OX} \frac{(D_{in} + D_{out}) \times 2N \times w}{t_{OX}} \tag{2.6}$$

where w and t_{OX} are the coil width and the thickness of the silicon oxide beneath the pick-up coil.

In this model, the series inductance (L) and parallel capacitor (C) form an LC tank circuit, with a resonance frequency ($= \frac{1}{2\pi\sqrt{LC}}$). The series resistor ($R$) sets the damping factor, which affects the sharpness of the resonance peak. The magnitude and phase of the magnetic-to-voltage transfer function of a pick-up coil are depicted in Figure 2.24. By increasing the value of the resistor, the resonance peak will be broader, resulting in a lower quality factor (Q).

In this work, two square pick-up coils are placed above the slits of the S-shaped current rail, directly above the Hall plates. The size of the current rail sets the outer diameter (D_{out}) of the pick-up coils to 500 μm. To minimize the parasitic capacitance, a minimum size width (1.5 μm) is used to implement the coil. In addition, to maximize the coil SNR, minimum-size spacing (1.5 μm) is chosen to maximize the number of turns. To set the inner diameter (D_{in}) and the number of windings, the normalized SNR with different numbers of turns is plotted in Figure 2.25. The optimized SNR is achieved with $N \sim 43$, which corresponds to $D_{in} \sim 250\,\mu$m. When the number of turns exceeds this threshold, the SNR fails to increase, and the parasitic capacitance also increases, thereby limiting the coil's bandwidth (BW). The degradation in SNR at higher values of N can be attributed to the small size of the added squares. Their contribution to the overall noise is greater than their contribution to the induced signal, leading to a reduction in SNR.

With the above critical dimensions and using eqs. (2.3), (2.4) and (2.6), the circuit model of the pick-up coil can be determined. Table 2.1 shows the values of the resulting key parameters of the implemented pick-up coil.

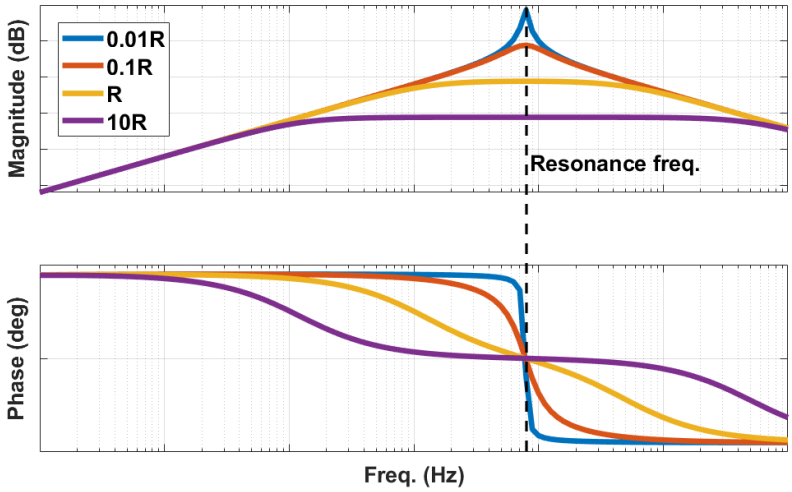

Figure 2.24: Magnitude and phase of the magnetic-to-voltage transfer function of a pick-up coil with different parasitic resistors.

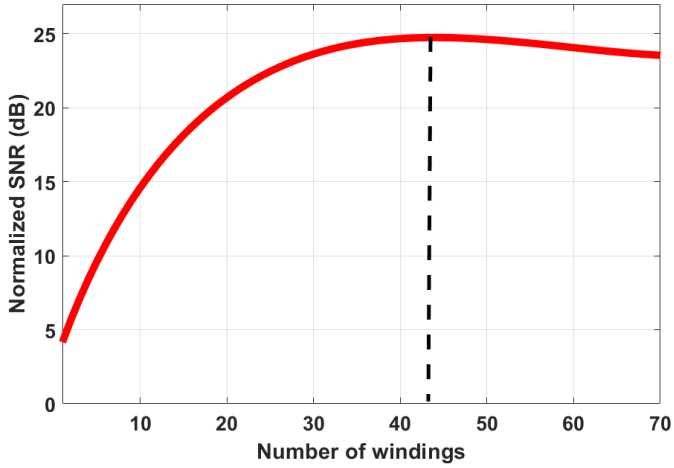

Figure 2.25: Normalized SNR vs. number of winding for the pick-up coil used in this work.

Figure 2.26 depicts the magnitude of the magnetic-to-voltage transfer function (TF) of the implemented pick-up coil. Three critical frequencies are specified in the plot: f_0, f_1, and f_2. The resonance frequency f_0 is

Table 2.1: The pick-up coil parameters

Parameter	Value
R	3300 Ω
L	1043 nH
C	3.95 pF
f_0	78 MHz
Q	0.16

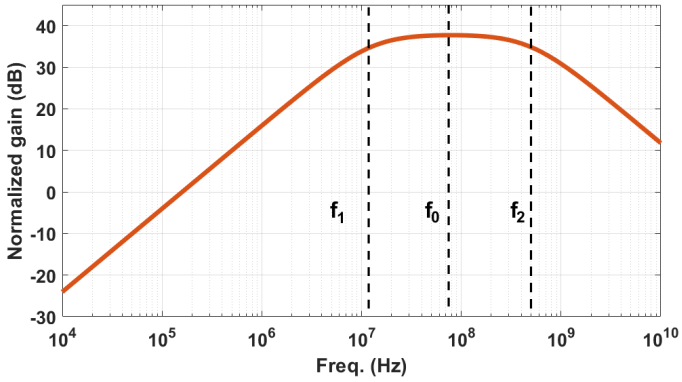

Figure 2.26: Magnitude of the magnetic-to-voltage transfer function of the implemented pick-up coil.

set by L and C, while the lower corner frequency f_1 is determined by R and C ($f_1 = \frac{1}{2\pi RC}$). Finally, the upper corner frequency f_2 is determined by R and L ($f_2 = \frac{R}{2\pi L}$). The usable bandwidth of the coil is limited by f_1, which arises from the parasitic capacitance of the pick-up coil.

2.6. READOUT OF PICK-UP COILS

As previously discussed in section 1.3.1, a pick-up coil has a differentiating characteristic, necessitating the use of an integrator to obtain a flat frequency response. This should be placed directly after the pick-up coil to limit its output at high frequencies. Without an integrator, the sensor's dynamic range (DR) will be significantly degraded.

2.6.1. INTEGRATOR IMPLEMENTATION

Common implementations of integrators include Gm-C integrators and active RC integrators (see Figure 2.27). A Gm-C integrator employs a transconductance (G_m) stage followed by an integrating capacitor (C). In contrast, an active RC integrator consists of an operational amplifier (op-amp), a resistor (R), and a capacitor (C).

The transfer function of the Gm-C integrator in the Laplace domain is:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{G_m}{sC} \tag{2.7}$$

Whereas the transfer function of the active RC integrator with infinite open-loop gain is:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1}{sRC} \tag{2.8}$$

A Gm-C integrator can typically achieve higher bandwidths than its closed-loop counterpart. However, the active RC integrator provides superior linearity due to the closed-loop configuration enabled by the op-amp. The choice between these implementations depends on the specific performance requirements of the application, such as bandwidth and linearity.

Another main difference between these configurations is their loading effect on the sensing element. The Gm-C integrator features a G_m stage

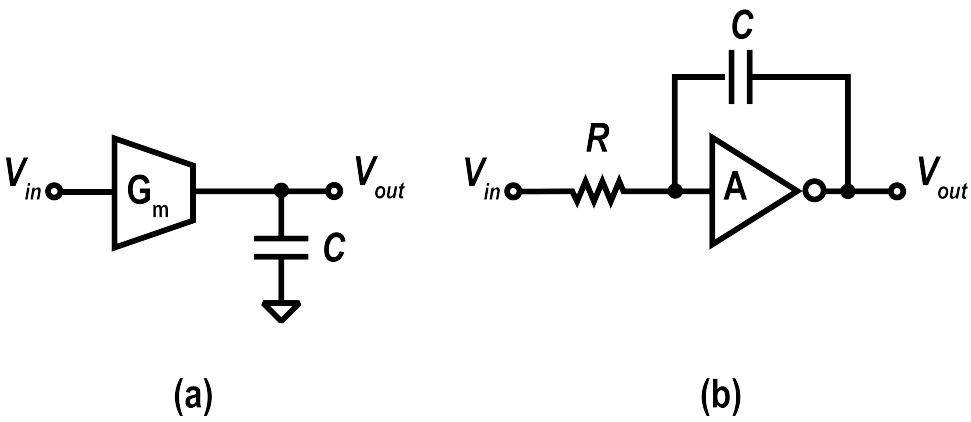

Figure 2.27: Integrator implementations: (a) Gm-C integrator (b) Active RC integrator.

with a high input impedance, which minimizes the loading effect on the pick-up coil when reading its voltage. In contrast, the active RC integrator typically has a lower input impedance due to the presence of resistors in the circuit. If the resistor values are not sufficiently high, they can load the sensing element, resulting in a voltage drop. As a result, the Gm-C integrator is generally the preferred choice for reading the coil voltage due to its high input impedance.

2.6.2. INTEGRATOR NONIDEALITIES

Regardless of how an integrator is implemented, it inevitably suffers from certain nonidealities. Two important ones are:

- **Finite DC gain:** In an ideal integrator, the Laplace transfer function has a pole at $s = 0$. When an ideal integrator is placed in front of a pick-up coil, which exhibits a differentiating characteristic, the resulting output of the integrator provides a flat frequency response from DC to high frequencies. However, in real-world implementations, no G_m stage has infinite output resistance, and no op-amp possesses infinite open-loop gain.

  For a Gm-C integrator, the transfer function is modified as follows:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{G_m R_{\text{out}}}{sR_{\text{out}}C + 1} \tag{2.9}$$

  where R_{out} is the output impedance of the G_m stage.

  Similarly, for an active RC integrator, the transfer function becomes:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-A_0}{sRCA_0 + 1} \tag{2.10}$$

  where A_0 is the open-loop gain of the op-amp.

  These modified transfer functions indicate that, due to finite DC gain, the pole is no longer at $s = 0$, but shifted to the right instead. As a result, the integrator behaves as a low-pass filter with a corner frequency determined by the finite gain. When the integrator is placed in front of the pick-up coil, the output no longer has a flat frequency response below this corner frequency.

In hybrid current sensors, the pick-up coil path is responsible for sensing high-frequency content above a certain crossover frequency. Therefore, a flat response around DC is not strictly necessary in the coil path. However, the finite DC gain still impacts the overall system, particularly the flatness of the combined response after merging the pick-up coil and Hall plate outputs.

- **Offset:** Both the G_m stage and op-amp introduce input offset. In an integrator, this offset is amplified by the DC gain of the integrator, which is $G_m R_{\text{out}}$ for Gm-C integrators and A_0 for active RC integrators.

  In hybrid current sensors, the amplified offset in the coil path is typically blocked and does not propagate to the final output. However, if the amplified offset becomes too large, it can saturate the output of the integrator itself, disrupting the normal operation of the integrator stage.

  It is important to note that reducing the DC gain of the integrator stage is not a good solution to this problem. Less DC gain makes the integrator behave more like a low-pass filter, which is not the desired transfer function for sensing a pick-up coil signal.

2.6.3. VOLTAGE READOUT VS. CURRENT READOUT

Up to this point, we have assumed that the readout system measures the coil's voltage, which requires a very high input impedance to prevent voltage attenuation and minimize the loading effect. However, an alternative approach is to measure the coil's current instead. The choice between measuring the voltage or current of a pick-up coil depends on the specific application and the characteristics of the pick-up coil, such as its type and size.

To compare the frequency response of current versus voltage readout, an ideal TIA is placed at the output of the lumped model of the pick-up coil (see Figure 2.28). For voltage readout, the coil's output voltage is measured without any loading, while for current readout, the output voltage of the TIA is measured.

Figure 2.29 demonstrates the frequency responses of these two methods. As expected, the bandwidth (BW) of the voltage readout

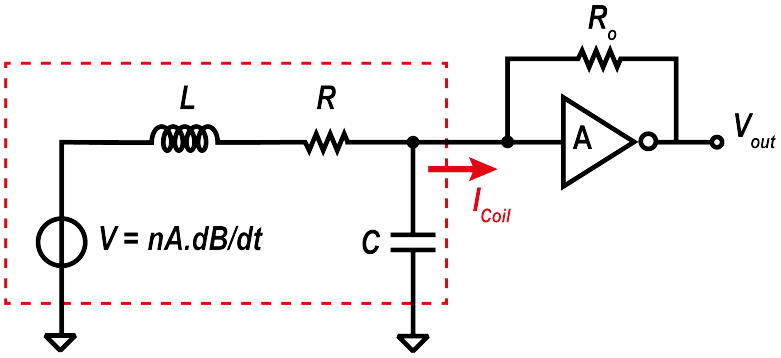

Figure 2.28: Coil-current readout.

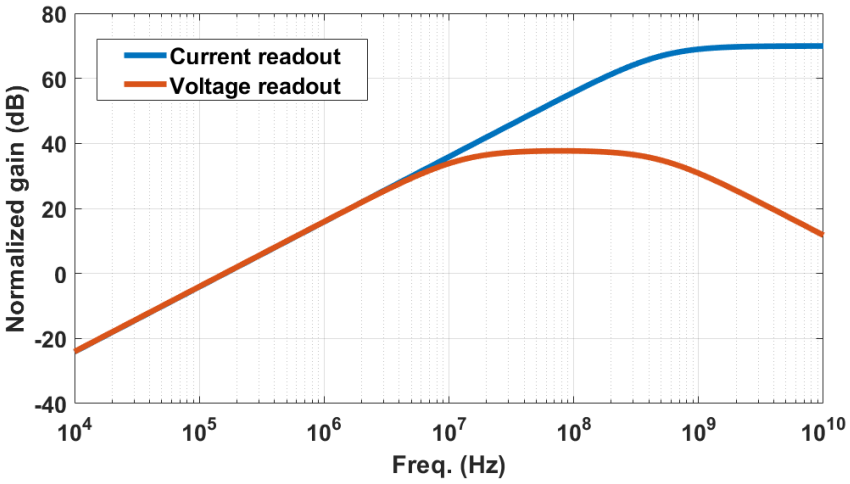

Figure 2.29: Coil-current vs. coil-voltage frequency response (lumped model).

is limited to ~10 MHz, caused by the parasitic capacitance of the coil. However, the usable BW of the current-readout mode extends to ~600 MHz, and is mainly limited by the parasitic inductance. Indeed, when using the current-readout mode, the parasitic capacitance is effectively shorted out, since the coil's output is connected to a virtual ground caused by the TIA. As a result, the lower corner frequency caused by this capacitor is removed.

Since the lumped model of the coil is valid only up to the resonance frequency of the coil [38], a distributed parameter model can be used

to validate the idea of improving the usable BW of the pick-up coil by reading out the current rather than the voltage (see Figure 2.30). For the simulation, the coil was divided into ten segments. As depicted in Figure 2.31, the usable BW is increased from ~20 MHz to more than 100 MHz by reading out the coil current. This demonstrates that even when using a distributed model, a significant amount of capacitance is bypassed, resulting in an extended BW.

Another drawback of voltage readout is limited dynamic range (DR) at high frequencies. Since the coil voltage is proportional to the input frequency, it can become very large at high frequencies. For instance, with a 40 A, 10 MHz current flowing through the rail, the implemented coil will output ~4 V. This obviously limits the maximum linear input range of the sensor at high frequencies. In contrast, current readout

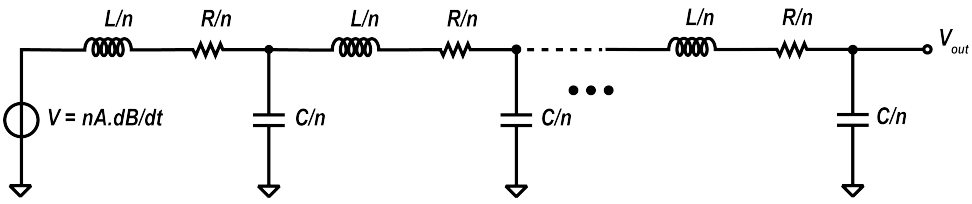

Figure 2.30: Distributed model of the pick-up coil.

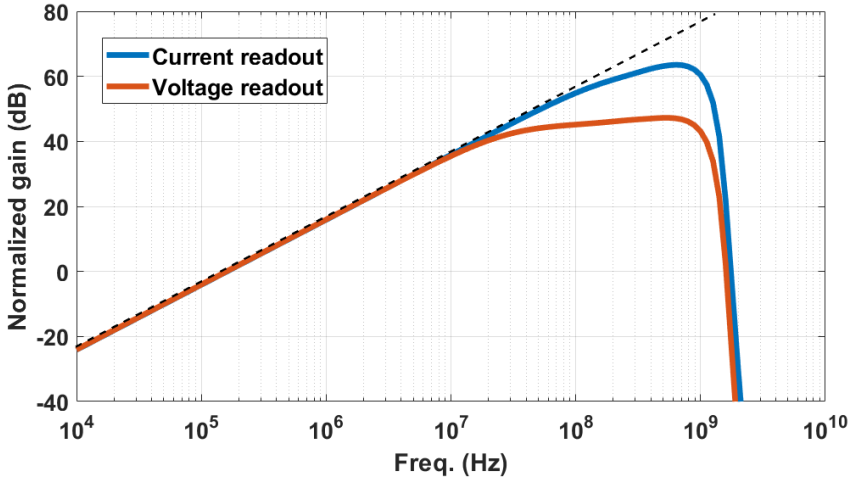

Figure 2.31: Coil-current vs. coil-voltage frequency response (distributed model).

circumvents this problem by effectively shorting the coil to a virtual ground. A low-pass filter can then be applied in the feedback of the TIA to limit the TIA's output voltage.

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3

IMPLEMENTATION 1: A HYBRID CURRENT SENSOR WITH A MRRL

3.1. INTRODUCTION

In the previous chapter, we introduced the concept of CMOS-compatible hybrid sensors, which combine Hall plates and coils to achieve both wide bandwidth (BW) and high resolution [1–5]. The hybrid current sensors utilize pick-up coils to detect high-frequency signals and Hall plates for low-frequency signals. To readout the signals from both the coils and Hall plates, two different gain paths are necessary. Additionally, a shared low-pass filter (LPF) is employed to both flatten the proportional-to-frequency coil signal and to restrict the bandwidth of the Hall-plate signal.

Based on this foundation, the current chapter describes the design of a prototype hybrid sensor. This sensor integrates differential (gradiometric) coils and Hall plates to detect the magnetic field generated by an S-shaped current-carrying lead frame.

The rest of the chapter is divided into three more sections. section 3.2 describes the proposed system. It covers the system architecture,

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outlines the method for temperature compensation in both the coil and Hall paths, presents the Multiplexed Ripple-Reduction Loop (MRRL) design, and introduces a self-calibration scheme. Following this, section 3.3 examines and interprets the measurement results. In the final section, the chapter concludes with a summary of the key findings.

3.2. PROPOSED HYBRID CURRENT SENSOR

3.2.1. SYSTEM ARCHITECTURE

Figure 3.1 shows a block diagram of the proposed current sensor. It consists of a CMOS chip mounted on a low resistance (250µΩ) S-shaped current rail, which concentrates the magnetic field seen by two coil/Hall plate pairs [2]. It also facilitates the use of a differential sensing scheme that rejects homogeneous interference, e.g., the earth's magnetic field [1]. Each n-well Hall plate consists of four sub-plates connected in parallel, whose bias currents flow in four different directions to reduce their combined offset and sensitivity to mechanical stress [6]. In contrast to [2], the Hall plates are not stacked, which leads to higher sensitivity and lower offset, and enables operation from a single 1.8V supply. Since the induced coil current is proportional to frequency, the coil path is designed to have an integrating characteristic, which is realized by a two-stage pole-zero cancellation scheme [2–4]. The first stage is a low-pass filter (LPF) with a pole at f_{p1}, and the second stage introduces another pole at f_X together with a zero at f_{z2}. This zero cancels the pole of the first stage (f_{p1}), thus turning the coil path into a first-order LPF with a pole f_{p2} (= f_X) that defines the cross-over frequency from the Hall to the coil paths. To suppress the offset of the first and second stages of the coil path, these stages are connected by an AC-coupling capacitor, which creates a parasitic pole at f_{p3}.

The output of the Hall plate is simply amplified and then added to the input of the coil path's second stage. In order to achieve a flat frequency response, the sensitivity of the Hall path must be adjusted to match the sensitivity of the coil path at f_X. As in [2], this is done by trimming the bias current of the Hall plates. The sensitivity of the coil and Hall path can be accurately determined by injecting known input currents I_{HP} (at $f_{HP}>f_X$) and I_{LP} (at $f_{LP}<f_X$) into two calibration coils located around the coil and Hall plates (Figure 3.1).

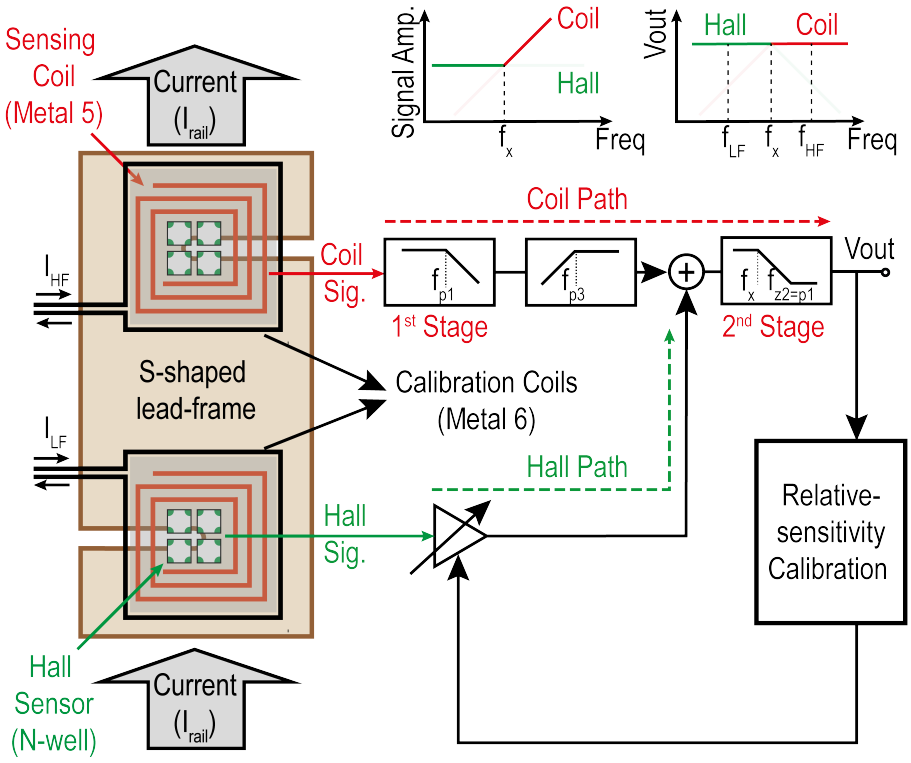

Figure 3.1: Simplified system block diagram including the off-chip relative-sensitivity calibration scheme.

A simplified schematic of the two sensor paths is shown in Figure 3.2. As in [2], the coil path consists of two stages. The input stage reads out the coil current and implements a pole $f_{p1} = 200\,\text{kHz}\left(\frac{1}{2\pi R_1 C_1}\right)$, thus limiting its output swing at higher frequencies. Compared to reading out the coil voltage, this approach greatly relaxes the design of the input stage.

As mentioned earlier, the 1st stage contributes a pole f_{p1}, while the 2nd stage contributes a pole f_{p2} $(\frac{1}{2\pi R_4 C_3})$ = 10 kHz and a zero f_{z2} $(\frac{1}{2\pi R_3 C_3})$ = f_{p1} = 200 kHz. This results in a coil path that behaves like a 1st order LPF with a pole at 10 kHz (= f_X). To ensure robust pole-zero cancellation, R_1C_1 and R_3C_3 are realized by the same type of components.

Although a 1st order LPF could be implemented with a single stage, R_1

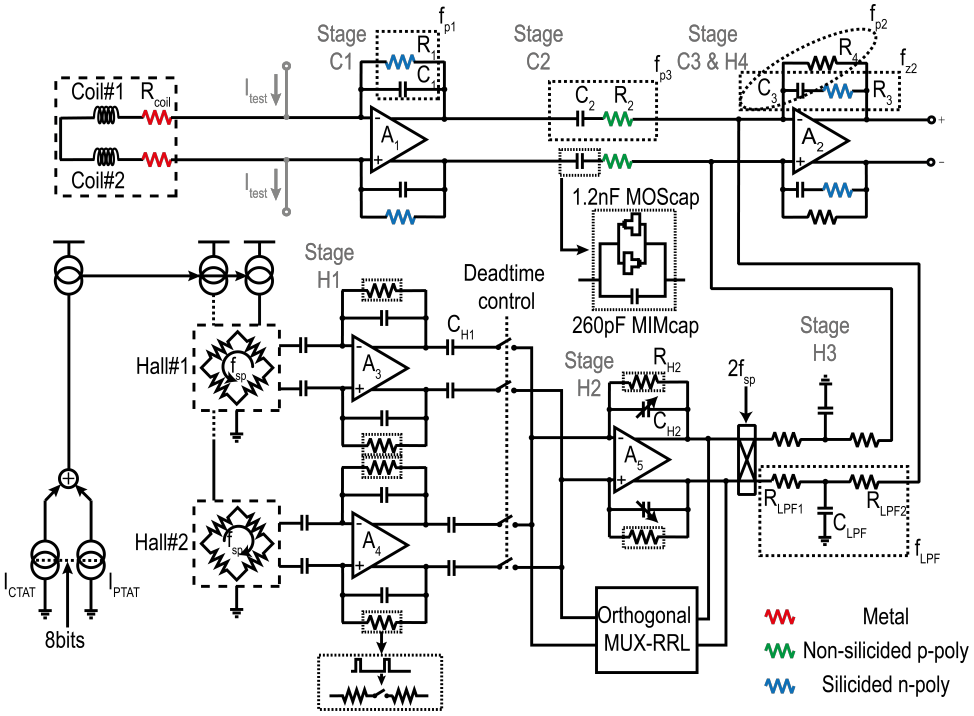

Figure 3.2: Full system block diagram.

would then be very large (6 MΩ, for $C_1 = 25$ pF). Since the coil resistance is small (~ 3 kΩ), the resulting DC gain would be quite large, causing the 1st stage to clip on its own millivolt-level offset. The two-stage architecture allows R_1 to be 20 times smaller ($f_{p1} = 20 f_X$), thus ensuring that the input stage does not clip. Furthermore, its output offset will be blocked by C_2.

Together with R_2, however, the presence of C_2 introduces a parasitic pole f_{p3}, which causes a dip in the overall transfer function (TF) around f_X. For a given coil path sensitivity, large capacitors are then needed to make f_{p3} as low as possible. In [2], these were realized by MIM capacitors, which occupied about 10% of the chip area. In this work, 6x larger capacitors (1.5 nF) are realized in the same area by placing MOS capacitors under the MIM capacitors. The MOS capacitors are split into two halves, which are connected in an antiparallel fashion to reduce (by 9x) their voltage-dependent non-linearity. Over process corners, the resulting 230 Hz parasitic pole causes a 2.3% dip (worst-case) in the

sensor's TF.

Since the outputs of the Hall plates are quite small, they are first amplified by local capacitively-coupled amplifiers (CCAs) with a gain of 50 ($A_{3,4}$), as shown in Figure 3.2. Their outputs are summed by another CCA (A_5) with a gain of 12 and converted back to DC by a chopper demodulator. The offset caused by spinning-induced transients is reduced by deadband switches [2]. The amplified Hall signal is then applied to the output stage via a passive RC low-pass filter with a pole at f_X, which, when combined with the TF of the coil path, results in a flat TF from DC to 8 MHz (the BW of the output stage), with an in-band gain variation of less than ±2.1% (verified by Monte Carlo simulations). The Bode plots of the different stages of the coil and Hall paths are shown in Figure 3.3.

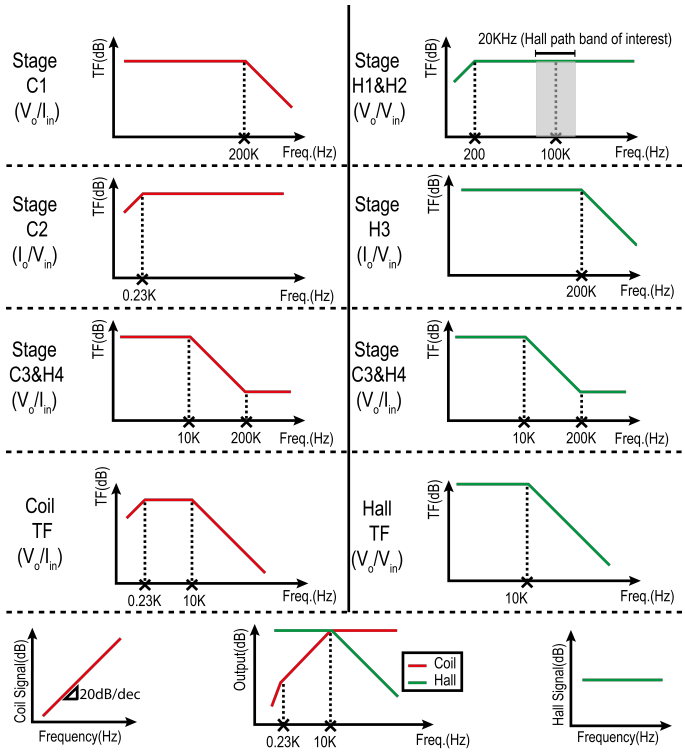

Figure 3.3: Transfer functions of different stages in the coil path (left) and Hall path (right).

3.2.2. TEMPERATURE COMPENSATION

One drawback of Hall plates is their significant gain drift versus temperature (> 20% from −70°C to 170°C [7]). In [7], this is compensated with the help of an on-chip temperature sensor. However, this requires (at least) a costly 2-point trim. In [5], which employs a differential sensing scheme, on-chip calibration coils generate a common-mode magnetic field, with which the gain of the Hall plates can be continuously calibrated. An off-chip control loop then stabilizes their gain drift by adjusting their biasing current. This approach requires a separate readout for sensing the common-mode magnetic field, and so consumes more power and chip area.

In this work, the TC of the Hall plates is approximately compensated by using a PTAT bias current (~ 2.5 mA at room temperature). This current is implemented by forcing a PTAT voltage ΔV_{GS} (the difference in gate-source voltage between a pair of PMOS transistors biased at a fixed current ratio in their sub-threshold region) across a p-poly resistor.

The sensitivity of the coil path G_E can be expressed as:

$$G_E = \begin{cases} \frac{R_1}{2\pi f R_{\text{coil}} R_2 C_3}, & \text{if } 10\,\text{kHz} < f < 200\,\text{kHz}, \\ \frac{R_3}{2\pi f R_{\text{coil}} R_2 C_1}, & \text{if } f > 200\,\text{kHz}. \end{cases} \tag{3.1}$$

The sensing coil R_{coil} is made of metal with a large temperature coefficient (TC = 0.34%/K). By realizing $R_{1,3}$ with silicided n-poly resistors (TC = 0.29%/K) and R_2 with non-silicided p-poly resistors (TC = -0.02%/K), the coil path overall TC is reduced significantly, to about -0.03%/K.

3.2.3. MULTIPLEXED RIPPLE-REDUCTION LOOP

Although Hall plates can be easily realized in CMOS, they usually suffer from a large offset, typically about 10 mT [8].

This can be significantly reduced by the spinning-current technique, which involves changing the direction of the sensor's bias current periodically and thus converting offset into AC ripple [7], which can be suppressed by low-pass filters or by ripple-reduction loops [1]. The residual offset, which is mainly due to n-well nonlinearity, can then be reduced to a few micro-Tesla [9].

In this work, the modified spinning-current technique proposed in [10] is used to keep the Hall offset at DC, while the desired Hall voltage is upmodulated to twice the spinning frequency ($2f_{sp} = 200\,\text{kHz}$). This ensures that most of the offset is blocked by the CCAs, leaving only some components at f_{sp} and $2f_{sp}$, which are again mainly due to n-well inhomogeneity. By ensuring that f_{sp} is much higher than f_X, this ripple will be significantly attenuated by the Hall-low-pass characteristic of the Hall path. However, the residual ripple is still quite significant and may limit sensor resolution [2].

To suppress the residual ripple further, ripple-reduction loops can be used. As shown in Figure 3.4, the residual ripple is a four-phase signal. This can be decomposed into three components, which are suppressed by three ripple reduction loops (RRLs) [1]. In this work, however, we note that the spinning ripple can be decomposed into four different components: a DC offset, a square wave at $2f_{sp}$, and two quadrature square waves at f_{sp}. The amplitude of these signals can be expressed as:

$$V_{DC} = \frac{1}{4}(V_{os1} + V_{os2} + V_{os3} + V_{os4}) \tag{3.2}$$

$$V_{2f_{sp}} = \frac{1}{4}(V_{os1} - V_{os2} + V_{os3} - V_{os4}) \tag{3.3}$$

$$V_{f_{sp}(0°)} = \frac{1}{4}(-V_{os1} - V_{os2} + V_{os3} + V_{os4}) \tag{3.4}$$

$$V_{f_{sp}(90°)} = \frac{1}{4}(V_{os1} - V_{os2} - V_{os3} + V_{os4}) \tag{3.5}$$

The DC offset will be blocked by the CCA, while the ripple at $2f_{sp}$ cannot be distinguished from the desired Hall voltage. The other two AC components can then be suppressed by just two RRLs.

Since spinning ripple is a quasi-static error, the two RRLs can be efficiently realized by a single multiplexed RRL (MRRL) (Figure 3.5). This is built around an opamp A_{int} and has four operating phases during which it: 1) auto-zeroes the offset of A_{int}, which would otherwise set the residual ripple amplitude; 2) sequentially suppresses each of the two quadrature components; and 3) suppresses the offset of A_5 with a DC servo loop (DSL), which would otherwise be converted into extra ripple by the output chopper. Each quadrature component is detected by a chopper demodulator, integrated on an integration capacitor $C_{f_{sp}}$

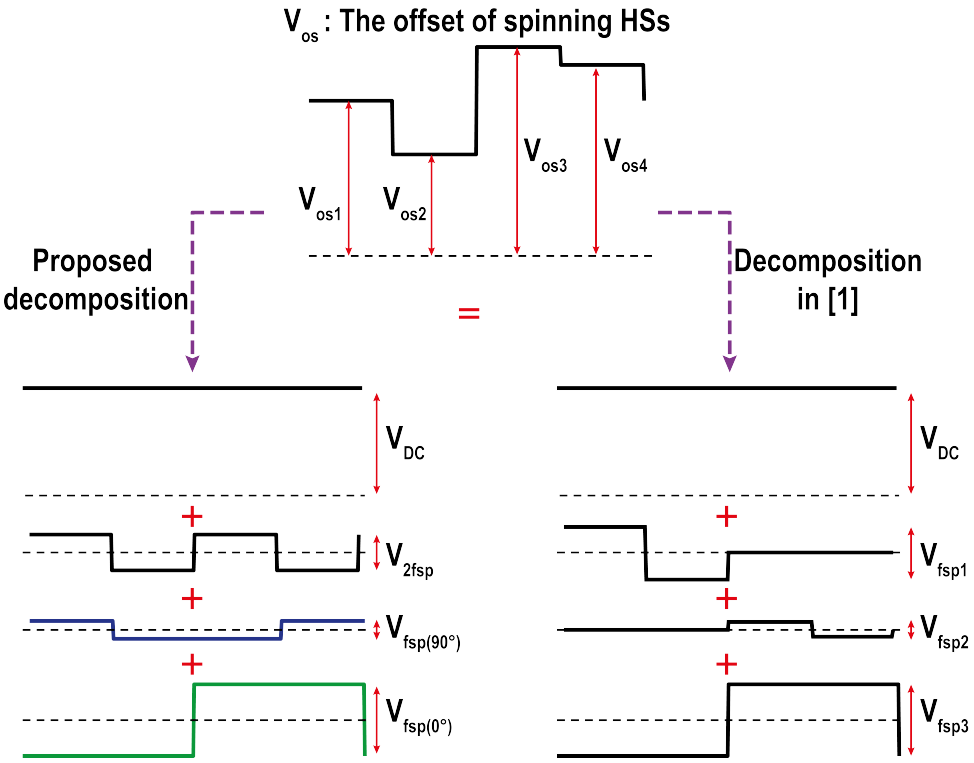

Figure 3.4: Decomposition of a 4-level Hall sensor offset into 3 orthogonal signals.

to generate a correction signal, which is then upmodulated and fed back to A_5 via an auxiliary input stage. The offset of A_5 is detected in a similar manner, but with the chopper disabled. The switched-resistor technique is used to realize a large sensing resistor ($R_{\text{sense}} > 100\,\text{M}\Omega$), resulting in narrow RRL notches ($< 1\,\text{kHz}$) that do not impact gain flatness.

By applying KCL at the output node of A_5 (V_o) and the virtual ground of A_5, the DSL transfer function $\left(\frac{V_o}{V_{\text{in}}}\right)$ can be expressed as:

$$\frac{V_o}{V_{\text{in}}} = \frac{g_1}{\frac{(sC_{H1}+g_1)(sC_{H2}R_{H2}+1)}{s(C_{H2}+C_{H1})R_{H2}+1} + \frac{1}{R_o \| R_s} + \frac{g_2}{\frac{1}{A_{\text{int}}}+sR_sC_{\text{DSL}}}} \tag{3.6}$$

where g_1 is the transconductance of A_5, g_2 is the DSL parallel input pair transconductance, and R_o is the load resistor of A_5. By assuming

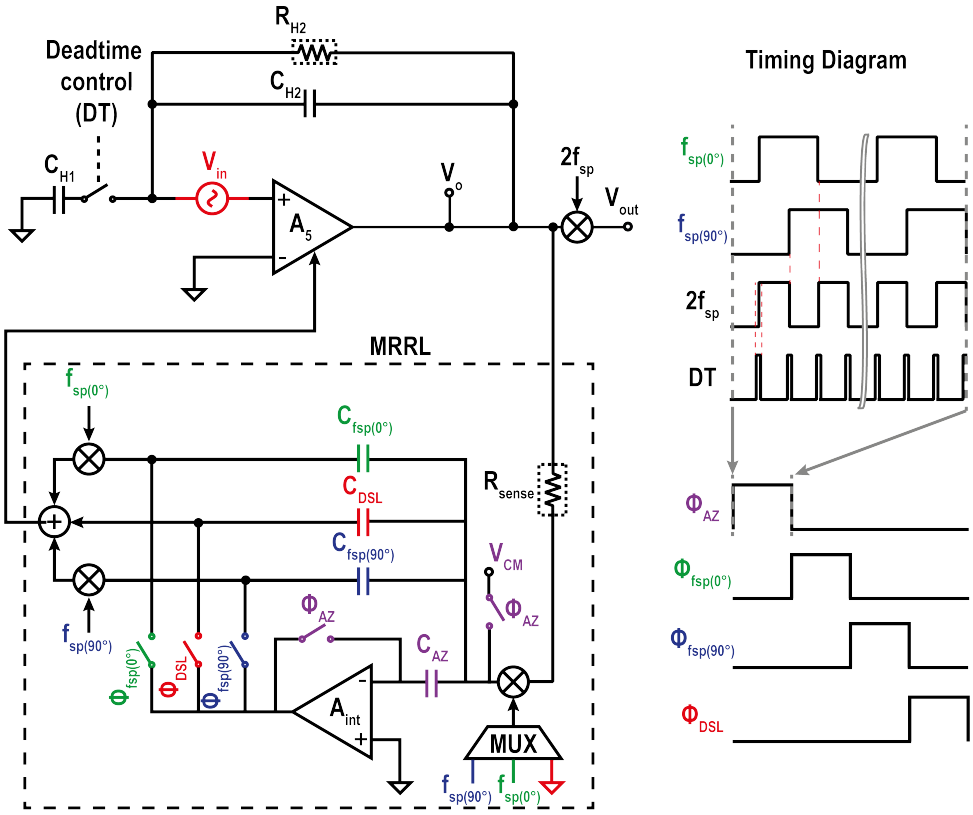

Figure 3.5: The simplified single-ended multiplexing ripple reduction loop (MRRL) and the timing diagram.

R_{H2} is large enough, the high-pass corner frequency of the DSL can be approximated as:

$$f_{\text{DSL}} = \frac{1}{2\pi R_s C_{\text{DSL}}} \cdot \frac{g_2}{g_1} \cdot \frac{C_{H1} + C_{H2}}{C_{H2}} \tag{3.7}$$

And the DSL attenuation is:

$$\text{Att.} = A_{\text{int}} \cdot \frac{g_2}{g_1} \tag{3.8}$$

In this design, $g_2 = 0.1 g_1$, $C_{\text{DSL}} = 5\,\text{pF}$, $A_{\text{int}} = 60\,\text{dB}$, $R_s = 100\,\text{M}\Omega$, and $C_{H2} = 12 C_{H1}$, which leads to a DSL corner frequency $f_{\text{DSL}} = 400\,\text{Hz}$ and a 40 dB attenuation.

By enabling the choppers before and after A_{int}, the DSL and its high-pass characteristic are converted to an RRL and a band-stop characteristic, respectively.

3.2.4. AMPLIFIERS IMPLEMENTATION

A_1 and A_2 are 2-stage amplifiers with a folded-cascode input stage and a class-AB output stage (Figure 3.6). In A_2, the output stage is required to drive an external 20 pF load capacitance, while in A_1, it is required to handle the large coil input currents at high frequencies. The equivalent input-referred noise of A_1 is equal to the thermal noise resistance of R_{coil} (3.3 kΩ).

A_3 and A_4 are current reuse telescopic amplifiers (Figure 3.7) designed to match their noise contribution to the noise of the Hall plate resistance R_{Hall} (350 Ω) with maximum noise efficiency.

3.2.5. FOREGROUND CALIBRATION SCHEME

To obtain a flat frequency response, the gain of the Hall plates can be trimmed to match the coil path. This is achieved by adjusting the Hall

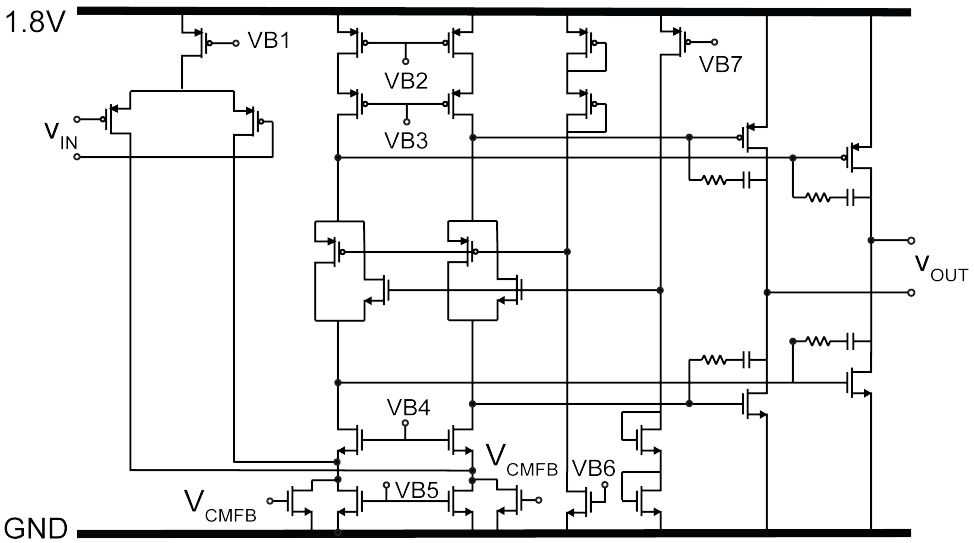

Figure 3.6: Schematic of A1 and A2.

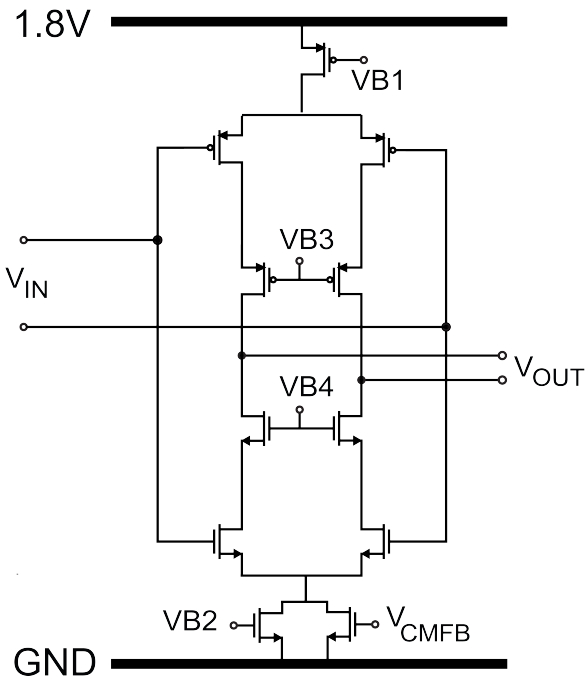

Figure 3.7: Schematic of A3 and A4.

plate's biasing currents with the help of an 8-bit PTAT current DAC, which can be used to trim the sensitivity of the Hall plates in steps of 1% (see Figure 3.8).

To realize the calibration scheme, two square-wave fixed currents ($8\,mA_{pp}$) at high (140 kHz) and low (200 Hz) frequencies are applied to the on-chip calibration coils. Since they are close to the sensors, these coils obviate the need to deliver large currents (~ a few amps) through the current rail for calibration. The magnetic fields generated by the calibration currents are detected by the sensing coils and Hall plates, respectively. The corresponding outputs are separated at the output of the final stage with two lock-in amplifiers. The outputs of the lock-in amplifiers are compared, and then their difference is integrated to control the 8-bit current DAC. The large calibration-loop gain ensures the difference is zero, and so the gain of the Hall and coil paths are matched. A 10 Hz measurement bandwidth (BW) was used to achieve $< 1\%$ trimming error.

A G factor (1.73) is considered at the output of the low-frequency

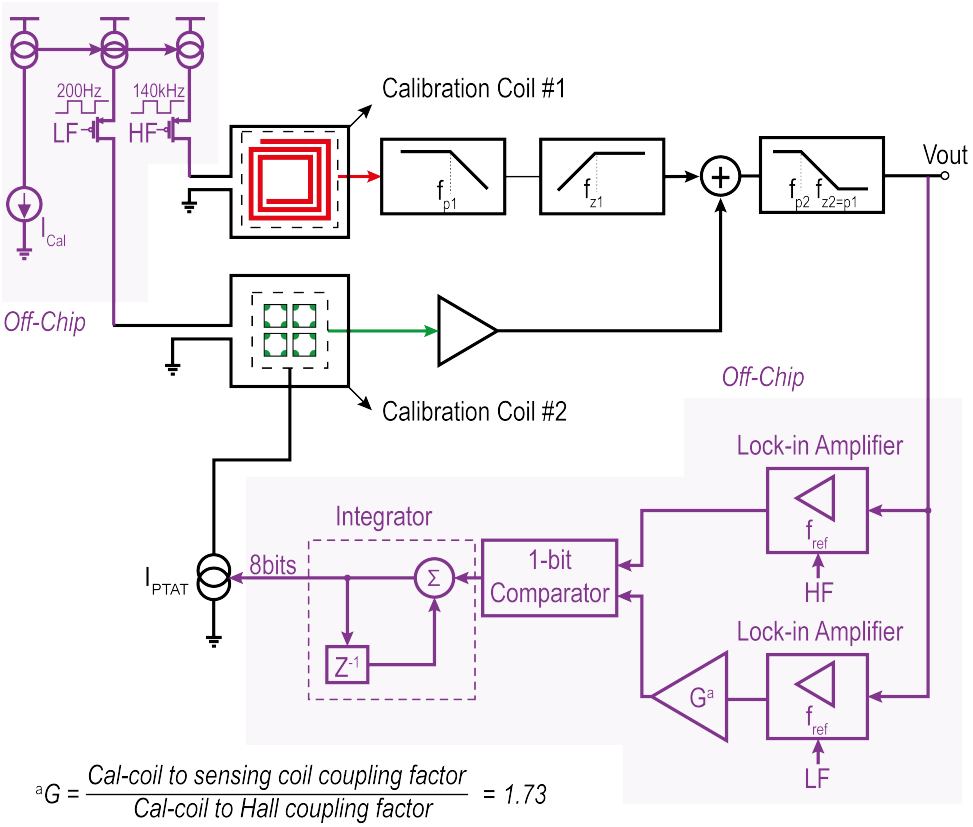

Figure 3.8: Self-calibration scheme.

lock-in amplifier to compensate for the different coupling factors between the calibration coil (metal 6) with the sensing coil (metal 5) and the Hall plate (substrate).

It should be mentioned that applying temperature compensation in both paths makes the overall transfer function robust to temperature drift, and so it only requires room-temperature calibration. To save area, only the critical calibration coils were implemented on the chip, while the rest of the system was implemented off-chip.

3.3. MEASUREMENT RESULTS

The hybrid current sensor is fabricated in a standard 0.18 μm CMOS process (Figure 3.9, bottom) and occupies 4.6 mm^2, which is mainly

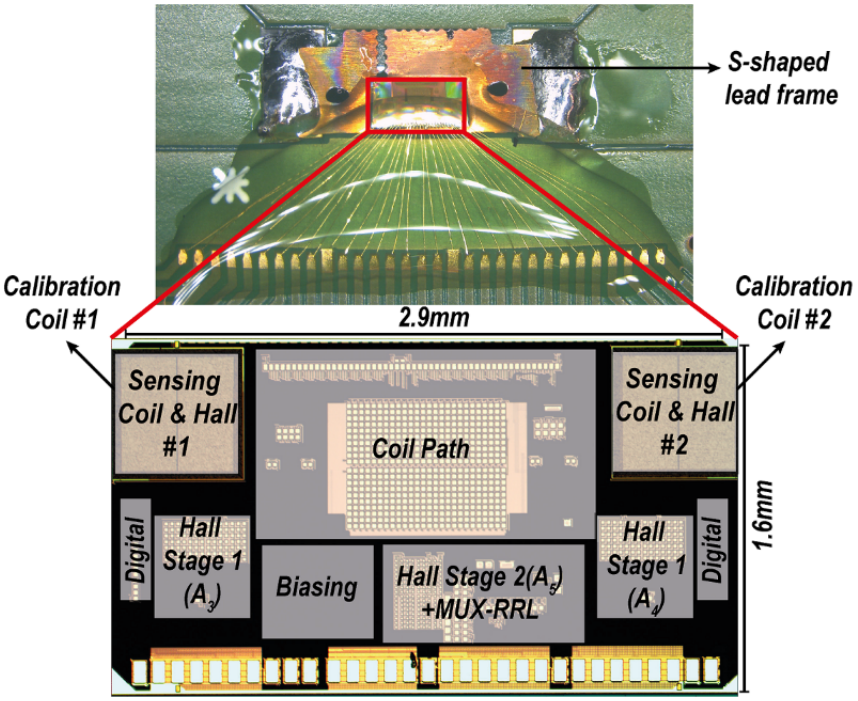

Figure 3.9: Sensor die on a copper lead-frame (Top) Die micrograph (Bottom).

determined by the need to position the Hall/coil sensors above the slots of the S-shaped current rail. The die is isolated from the leadframe by non-conductive glue (Figure 3.9, top). The chip is powered by an analog V_{DD} (1.8V) and a digital V_{DD} (1.8V). All other bias currents/voltages are implemented on-chip. The sensor draws 7.8mA, of which 5mA is used to bias the Hall plates. To mitigate high-frequency crosstalk, two grounded on-chip shields are employed: one above the metal coil in metal 6, while the other is placed between the coil sensor and the Hall plate.

As shown in Figure 3.10, a daughterboard printed-circuit board (PCB) is mounted over a motherboard PCB to measure the sensor sensitivity. The daughterboard PCB includes the S-shaped leadframe and the chip, while the motherboard consists of voltage regulators, differential-to-single-ended amplifiers, and an external clock reference. The calibration setup is also provided off-chip on the motherboard.

A network analyzer that sweeps over the frequency is connected to a waveform amplifier with high current capability. The output of the waveform amplifier delivers the current to the current rail. The sensor sensitivity can be determined at different frequencies by measuring the ratio between the sensor output voltage and the waveform amplifier current monitor output.

The sensitivities of the Hall and coil paths over temperature are shown in Figure 3.11. The PTAT bias current effectively compensates for the linear component of the Hall plate's temperature dependency, resulting in a 9% gain drift in the Hall path. The 2.7% gain drift in the coil path is due to the expected residual temperature coefficient (TC) of using different resistors.

After trimming at room temperature, the measured transfer function (TF) of the sensor is shown in Figure 3.12. Its 3 dB bandwidth is limited to 5 MHz by eddy currents induced in the current rail. Around f_X

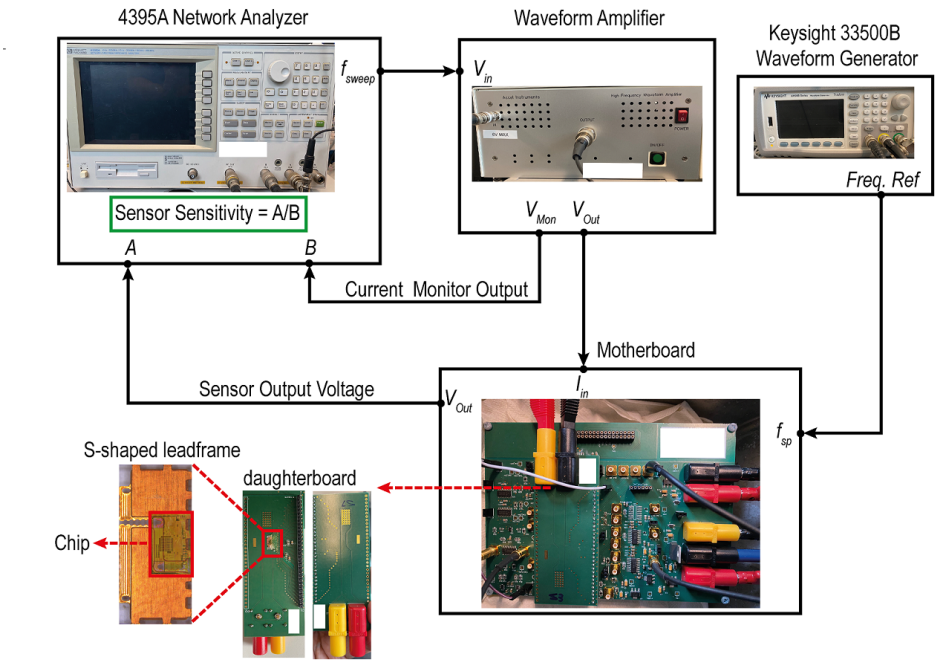

Figure 3.10: Measurement setup.

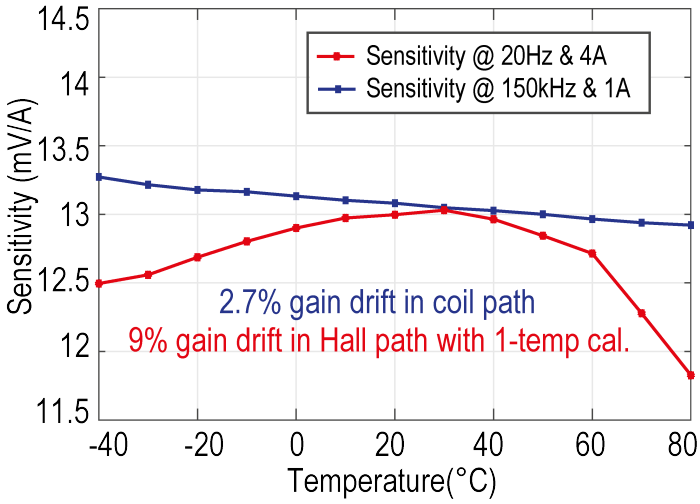

Figure 3.11: Sensitivity vs. temperature.

(DC-100 kHz), the measured gain variation is less than ±1.5% (±0.12 dB), which is about 6× less than that reported in [2]. The spread above 200 kHz is caused by the manual alignment of the chips with the slots in the current rail.

The dynamic range of the sensor was determined experimentally. At DC, the self-heating of the current rail limits the maximum input current to ~33 A. As the input frequency is increased above f_X, the induced coil voltage increases, causing the input stage of the coil path to eventually clip. By injecting a test current into the coil path, it was found to have a bandwidth (BW) of ~8 MHz, with the onset of clipping (THD = 3%) corresponding to 33 A_{rms} (46 A_p) at 300 kHz in the current rail. As shown in Figure 3.13, the use of deadbanding makes the Hall plate offset relatively independent of f_{sp}. For a good tradeoff between offset and the filtering of residual spinning ripple, f_{sp} = 99 kHz was chosen. This results in the worst-case offset of 57 μT (4 samples), which corresponds to 130 mA in the current rail. The sensor's response to small (1 A) and large (33 A) steps is shown in Figure 3.14 and Figure 3.15, respectively. In the case of the large step, the slow fall time is mainly due to the limitations of the 33 A current supply.

Figure 3.16 shows the noise spectral density together with the

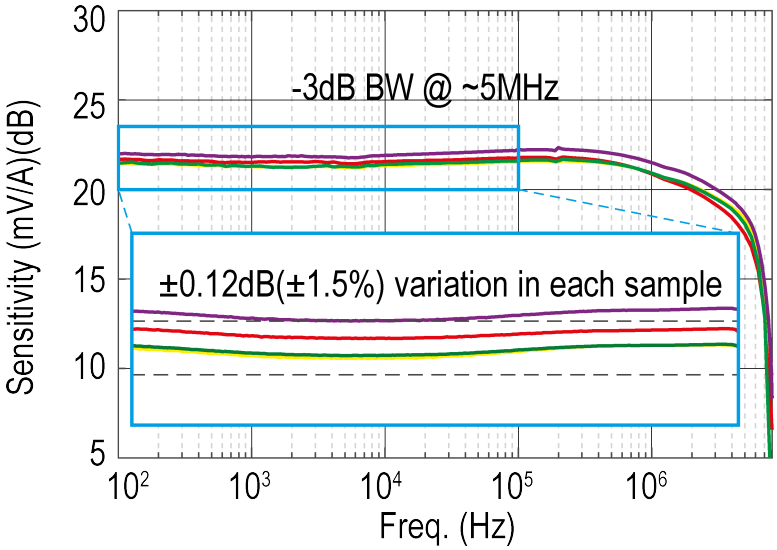

Figure 3.12: Sensitivity vs. frequency magnitude.

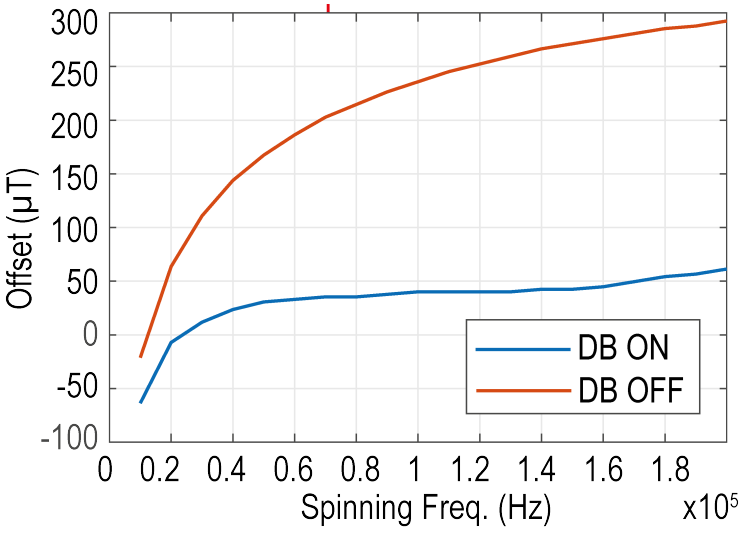

Figure 3.13: Uncalibrated offset vs. fsp w/ deadbanding on/off.

accumulation noise. The MRRL suppresses the main spinning ripple (at f_{sp} and $3f_{sp}$) by more than 20 dB. The total input-referred ripple corresponds to 16 mA_{rms} (5 μT_{rms}), which is about 20% less than that

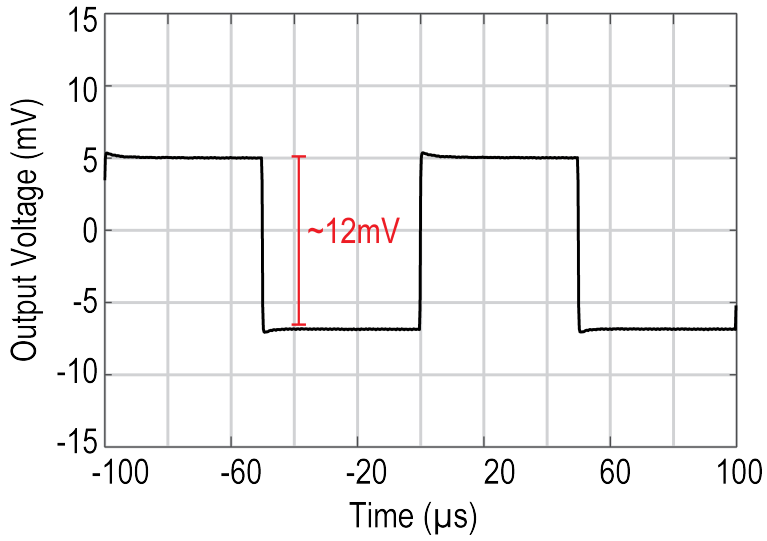

Figure 3.14: Transient response for a $1\,A_{p\text{-}p}$ square-wave @ 10 kHz (after 1024× averaging) .

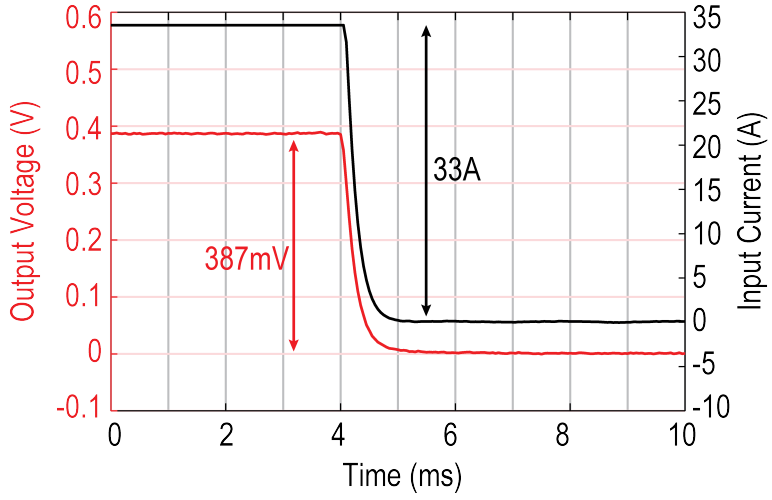

Figure 3.15: 33A step response.

reported in [1]. In a 5 MHz bandwidth, the sensor's accumulated noise corresponds to $69\,mA_{rms}$ ($20\,\mu T_{rms}$).

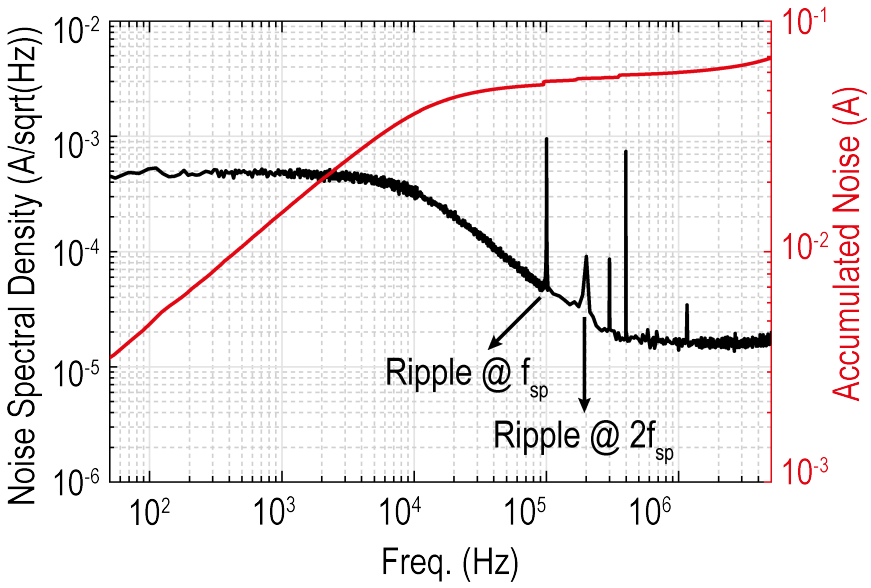

Figure 3.16: Noise spectral density and accumulated noise referred to current rail.

It should be mentioned that the current resolution depends on the proximity of the current rail to the on-chip sensors. Designs with on-chip current rails may have higher current resolution at the expense of increased manufacturing cost and reduced galvanic isolation. Finally, the residual ripple at f_{sp} only causes a 2 mA step in the total accumulated noise. The residual ripple is mainly due to the limited bandwidth (BW) of the CCAs. As a result, the ripple components are not perfect square waves and are not completely canceled by the RRLs. Switching transients also contribute to the residual ripple.

Table 3.1 summarizes the performance of the proposed hybrid current sensor and compares it with state-of-the-art magnetic current sensors. Compared to [2], the gain flatness and input-referred ripple are improved by 6× and 16×, respectively. This design also achieves the highest energy efficiency FoM (×3) and the lowest power consumption (×1.4) of all hybrid sensors.

Table 3.1: Performance Summary and Comparison

Source	**This Work**	ISSCC'21 [2]	JSSC'17 [1]	JSSC'19 [11]	JSSC'22 [12]	APEC'19 [3]
Sensor Type	**Coil + Hall**	Coil + Hall	Coil + Hall	Hall	IFG	Coil + Hall
Technology (μm)	**0.18**	0.18	0.18	0.35	0.25	0.18
Supply (V)	**1.8**	1.8/3.3	5	3.3	1.8/5	1.8
Area (mm^2)	**4.6**	4.6	8.75	N/A	4+3.6	2.74
Resolution (mA$_{rms}$)	**69**	64	480	480	11[c]	710
Input Range (A)	**±46**[a]	±25	±18[a]	±300	±53[c]	±60
Dynamic Range (dB)	**54**	52	17	56	74	39
BW (MHz)	**5**	1.8	3	1.7	0.125	15.3
Power Consumption (mW)	**14**	19.5	38.5	13.2	100[d]+13	63.5
Gain Flatness	**±1.5%**	±12%	N/A	N/A	N/A	±3.7%
Residual Ripple @ f_{sp} (μT)	**6**	74	8	N/A	N/A	N/A
Residual Offset (μT)	**57**	75	40	262	N/A	N/A
FoM[b] (fW/Hz)	**1.6**	17.7	2281	5	8.5	145
DR + 10log(BW/Power)	**139**	131	96	137	135	122

[a]Extrapolated

[b]FoM = Power/(BW x (Range/Resolution)^2)

[c]Conversion rate = 45 μT/A

[d]Full-range power

3.4. CONCLUSION

In this chapter, a hybrid magnetic current sensor with wide bandwidth (BW) of 5 MHz is proposed. A multiplexed ripple-reduction loop (RRL) is employed to effectively deal with the Hall plate offset in different spinning phases. With this approach, the residual ripple at the spinning frequency is 4× below the total integrated noise. The offset of the coil path is blocked by large on-chip capacitors (1.5 nF each), which are implemented in an area-efficient manner by placing MOS capacitors below MIM capacitors. The drift in the sensitivity of the coil path over temperature is compensated with the help of silicided poly resistors, which have nearly the same temperature coefficient (TC) as the metal coils, while the drift of the Hall path is compensated by biasing them with a PTAT current. The resulting temperature drift is limited to 9% from −40 to 80 °C, mainly due to the residual drift of the Hall path. A one-time room-temperature calibration scheme with on-chip calibration coils is utilized to equalize the sensitivity of the Hall and coil paths. The overall sensor achieves state-of-the-art energy efficiency with a figure of merit (FoM) of 1.6 fW/Hz.

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4

IMPLEMENTATION 2: A HYBRID CURRENT SENSOR WITH A D3SL

4.1. INTRODUCTION

In previous chapters, hybrid sensors have been presented as a promising solution for isolated current sensing, offering wide bandwidth and high resolution [1–5]. One of the main challenges in designing hybrid current sensors is achieving a flat response over the frequency range. A current sensor with a flat frequency response ensures compatibility with frequency-dependent systems, enabling accurate current monitoring and control over a wide frequency range. As shown in Figure 4.1, a 1^{st}-order low-pass filter (LPF) can smoothly combine the differentiating characteristic of coils and the all-pass characteristic of Hall plates. The corner frequency of the LPF defines the crossover frequency f_X, which also defines the sensor's noise bandwidth. For maximum resolution, f_X should be chosen so that the Hall and coil paths contribute the same amount of noise. In practice, a high-pass filter (HPF) is required to block the offset of the coil path, which may often be significantly larger than the mV-level output of the Hall plates. However, the HPF creates a parasitic pole at f_{Par} in the coil path, which, in turn, causes a

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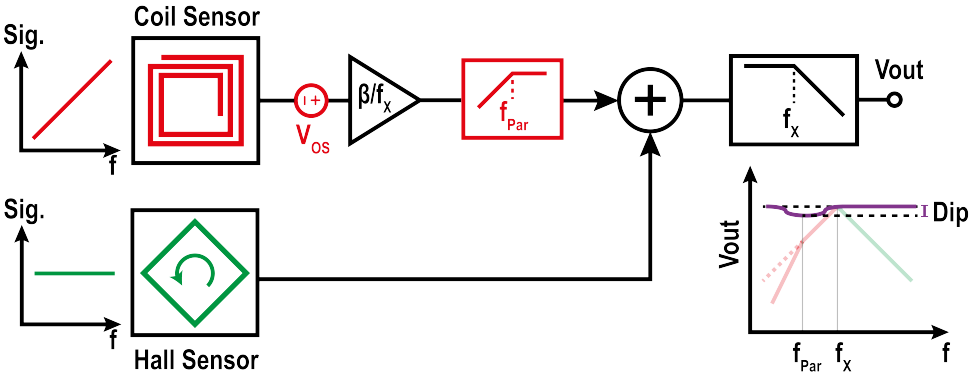

Figure 4.1: The effect of parasitic pole on the gain flatness.

dip around f_X in the combined response of the two signal paths. To minimize this dip, f_{Par} must be set much lower than f_X, which is quite challenging since f_X is typically in the order of a few kHz.

In the previous chapter, a hybrid current sensor was proposed to achieve high dynamic range (DR) by reading out the coil current instead of the coil voltage. To eliminate the need for external components, its coil path employed a two-stage low-pass filter. The coil-path offset was then blocked by a large on-chip capacitor (1.2 nF) placed between the two stages. However, the resulting parasitic pole caused a 3% dip in the sensor's frequency response around $f_X = 10$ kHz. This chapter presents the design of a hybrid magnetic current sensor with an optimized crossover frequency. As in [1, 5], a two-stage coil path is used. However, to simultaneously suppress the coil-path offset and achieve good gain flatness, the large blocking capacitor in [1, 5] is replaced by an area-efficient dual-differential DC servo loop (D3SL). The gain drift over the temperature of the Hall plates is partially compensated by a near-PTAT bias current. Their remaining gain drift is removed by designing the amplifiers in the Hall path to have a temperature-dependent gain. A similar approach is used to compensate for the gain drift of the coil path.

The rest of this chapter is organized as follows: the proposed system, including the crossover frequency optimization for noise, the design of the D3SL, and the temperature compensation in both the coil path and Hall path, are presented in section 4.2. section 4.3 shows and discusses

the measurement results. Finally, conclusions are drawn in section 4.4.

4.2. PROPOSED HYBRID CURRENT SENSOR

4.2.1. SYSTEM ARCHITECTURE

A system block diagram of the proposed hybrid current sensor is shown in Figure 4.2. A low-pass filter (LPF) with a corner frequency f_X is used to flatten the coil's differentiating characteristic and to limit the noise bandwidth of the Hall path. To achieve a flat response, the output of the coil path at f_X must be equal to that of the Hall path. As a result, the gain of the coil path can be expressed as β/f_X, where β is a constant. Taking into account the equivalent noise bandwidth of a 1st-order filter, the total output noise power of the Hall path is proportional to f_X and can be expressed as:

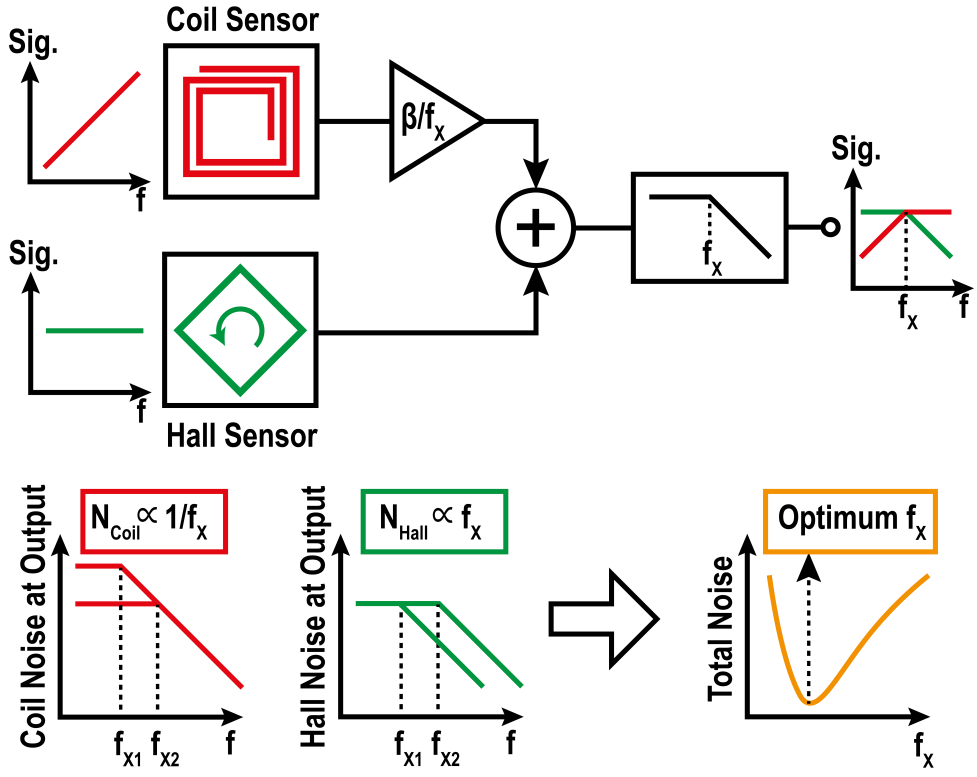

Figure 4.2: System block diagram and optimum crossover frequency.

$$N_{\text{Hall}} = 2kTR_H \times \pi f_X \tag{4.1}$$

where R_H is the output resistance of the Hall plate. In contrast, the output noise power of the coil path is inversely proportional to f_X and can be expressed as:

$$N_{\text{Coil}} = 2kTR_C \times \beta^2 \times \frac{\pi}{f_X} \tag{4.2}$$

where R_C is the resistance of the coil. The sensor's total noise power is the sum of the contributions of the coil path and the Hall path. As shown in Figure 4.2, if the crossover frequency is set too low, the noise of the coil path will be dominant, while if it is set too high, the noise of the Hall path will become dominant. At the optimum crossover frequency, the noise contribution of both paths is equal, resulting in the minimum total output noise. This optimized crossover frequency can be calculated as:

$$f_{X,\text{opt}} = \sqrt{\frac{R_C}{R_H}} \times \beta \tag{4.3}$$

In this design, $f_{X,\text{opt}}$ is 2 kHz. Simulations show that even large (20%) variations in f_X only increase the total noise slightly ($< 4\%$). Therefore, no trimming is required.

A simplified single-ended schematic of the proposed hybrid current sensor is shown in Figure 4.3, while the actual implementation is fully differential. As in [1, 5], the coil path employs a two-stage low-pass filter (LPF) based on a pole-zero cancellation scheme for reading out the coil current. The first stage sets a pole $f_{p1} = 140\,\text{kHz} = \frac{1}{2\pi R_1 C_1}$ to limit the first-stage output swing at high frequencies, while the second stage cancels the pole f_{p1} with a zero $f_{z2} = \frac{1}{2\pi R_3 C_3}$ and introduces a new pole $f_X = 2\,\text{kHz} = \frac{1}{2\pi R_4 C_3}$. The pole f_X sets the crossover frequency and is chosen for maximum resolution. To ensure the robustness of the pole-zero cancellation scheme, the same type of components are used to realize f_{p1} and f_{z2}.

In the Hall path, the up-modulated outputs of the spinning Hall plates are first amplified by two capacitively coupled amplifiers (CCAs). The amplified Hall signal is then demodulated back to DC and injected into the second stage of the coil path via a low-pass filter (LPF) with a

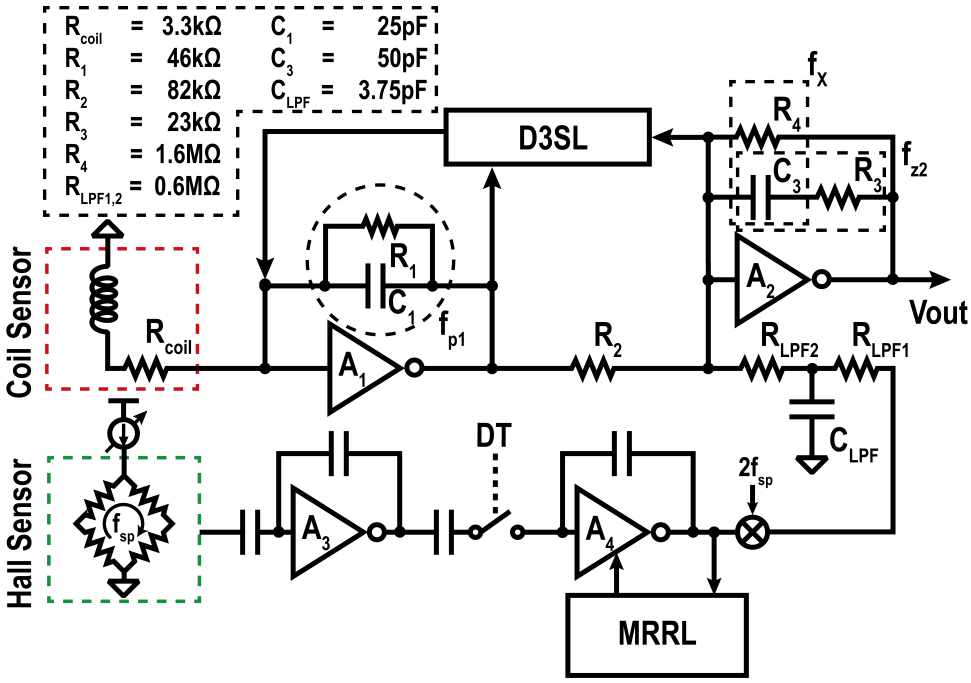

Figure 4.3: Simplified single-ended schematic of the hybrid sensor.

pole at f_{z2}. The combination of this LPF and the transfer function of the coil path's second stage results in a first-order LPF with a pole at f_X.

As in [5], a multiplexed ripple-reduction loop (MRRL) is used to suppress spinning-induced ripple (Figure 4.4), which is caused by the offset of the Hall plates [6]. The ripple can be decomposed into four orthogonal components: two square waves in quadrature at f_{sp}, a square wave at $2f_{\mathrm{sp}}$ that results in a residual offset in the final output, and a DC component that is blocked by the first CCA. The MRRL operates in four phases to consecutively suppress the quadrature component at f_{sp}, the offset of A_4, and the offset of A_5. In the first two phases, the MRRL is configured as a ripple-reduction loop (RRL), which senses the ripple via a sensing resistor $R_{s3} = 10\,\mathrm{M\Omega}$ and a chopper demodulator. The resulting DC signal is then integrated on a capacitor $C_{\mathrm{fsp}} = 5\,\mathrm{pF}$ to generate a correction signal, which is then up-modulated and fed back to the amplifier A_4 via an auxiliary input stage. In the second phase, the choppers are disabled, and the MRRL functions as a DC servo loop (DSL) to attenuate the offset of A_4. In the last phase, the

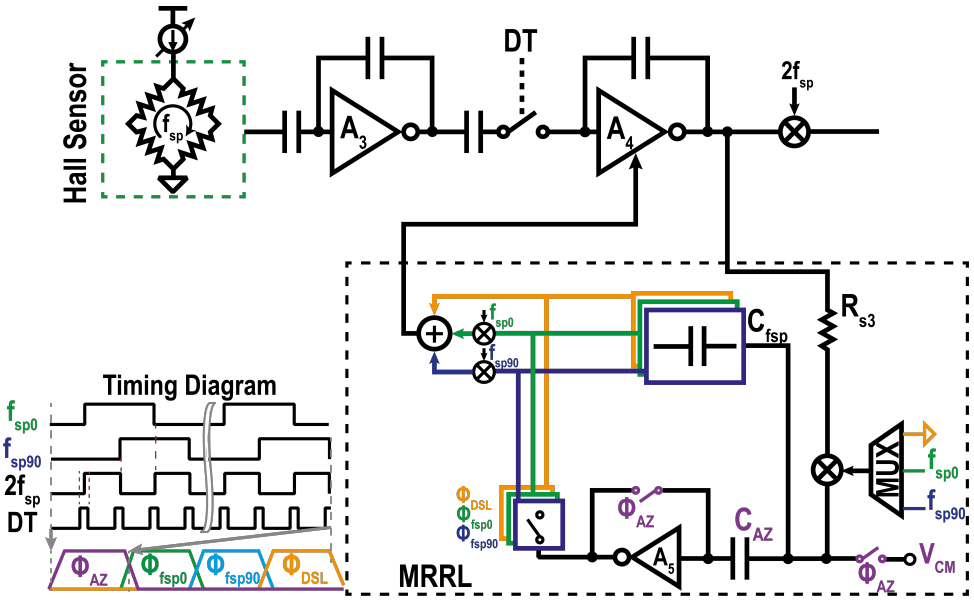

Figure 4.4: Multiplexed RRL.

offset of A_5 is auto-zeroed to reduce the residual ripple it causes.

4.2.2. DUAL DIFFERENTIAL DC SERVO LOOP (D3SL)

To achieve accurate sensing of DC signals using the Hall path, it is essential to eliminate the offset contribution of the coil path. Without an offset cancellation technique, the offsets of A_1 and A_2 would be amplified, resulting in an output-referred offset in the coil path (Figure 4.5):

$$V_{\mathrm{OS,Out}} = -\left(1+\frac{R_1}{R_{\mathrm{Coil}}}\right)\frac{R_4}{R_2}V_{\mathrm{OS1}} + \left(1+\frac{R_4}{R_2}\right)V_{\mathrm{OS2}} \tag{4.4}$$

where V_{OS1} and V_{OS2} are the input-referred offsets of A_1 and A_2, respectively. In [1, 5], a blocking capacitor is used between the coil-path stages to attenuate the coil-path offset. Due to its high impedance at DC, the blocking capacitor rejects V_{OS1} and ensures that V_{OS2} appears at the output with a gain of 1. However, the blocking capacitor C_B and the series resistor R_2 create a parasitic pole $f_{\mathrm{Par}} = 230\,\mathrm{Hz}$, which causes a dip in the sensor's transfer function. In [5], $C_B = 1.2\,\mathrm{nF}$ occupies more

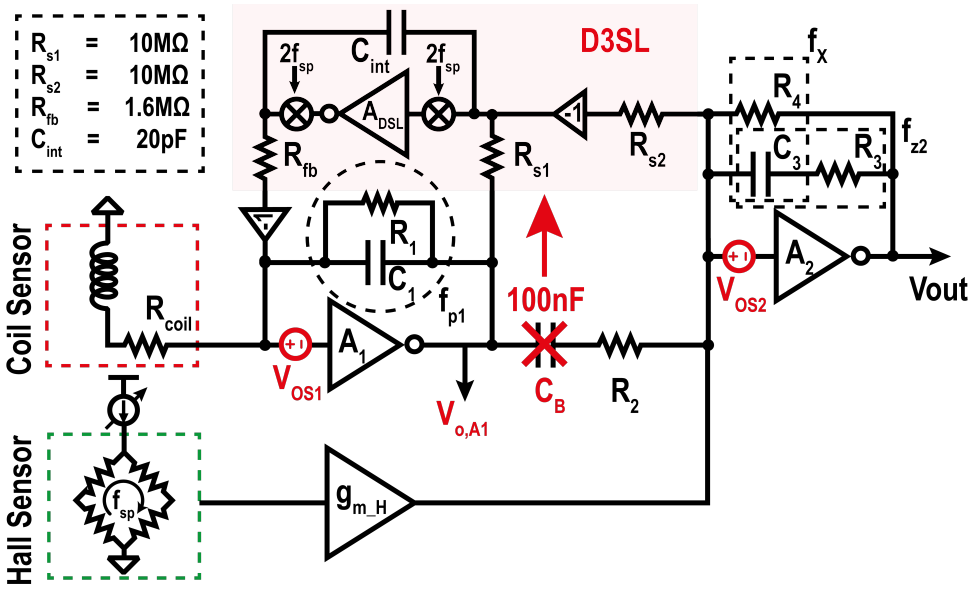

Figure 4.5: Dual differential DC servo loop (D3SL).

than 10% of the chip area, and $R_2 = 500\,\text{k}\Omega$ contributes 25% of the noise in the coil path. Therefore, it is not possible to further increase the size of these components to decrease f_{Par}. Instead, a higher than optimal crossover frequency (10 kHz rather than 2 kHz) was chosen in [5] to achieve less than 3% dip around f_X. To achieve the optimum crossover frequency (2 kHz), reduce the noise contribution of R_2 to less than 5%, and achieve a gain flatness of ±1%, a 100× larger blocking capacitor would be required, which is not practical.

Therefore, the blocking capacitor is replaced by a dual-differential DC servo loop (D3SL) in this work (see Figure 4.5). It senses the DC voltage across R_2 and drives it to zero by regulating the output of A1. Like a blocking capacitor, this ensures that the DC current flowing through R_2 is zero by driving the output-referred offset of A_1 to V_{OS2}.

In the proposed scheme, the voltage across R_2 is sensed via two sensing resistors $R_{s1,2} = 10\,\text{M}\Omega$, and then integrated on a capacitor $C_{\text{int}} = 20\,\text{pF}$ built around the amplifier A_{DSL}. The resulting voltage is fed back to the input of A_1 via a feedback resistor $R_{\text{fb}} = 1.6\,\text{M}\Omega$ to close the feedback loop and regulate the output of A_1. By applying feedback

theory, f_{Par} caused by the D3SL can be calculated as:

$$f_{\text{Par}} = \frac{1}{2\pi R_{s1,2} C_{\text{int}} \frac{R_{\text{fb}}}{R_1}} \tag{4.5}$$

In this design, $R_{s1,2} = 10\,\text{M}\Omega$, $R_{\text{fb}} = 1.6\,\text{M}\Omega$, $R_1 = 46\,\text{k}\Omega$, and $C_{\text{int}} = 20\,\text{pF}$, which leads to a D3SL corner frequency of $f_{\text{Par}} = 15\,\text{Hz}$.

As shown in Figure 4.6, to reduce the offset of A_1 to less than $1\,\mu\text{V}$, a two-stage amplifier A_{DSL} with a high DC gain of 120 dB is employed. The first stage of A_{DSL} is a current-reuse telescopic stage designed to maximize noise efficiency, while the second stage is a conventional common-source stage with a rail-to-rail output driver. To achieve a 60° phase margin, a Miller compensation capacitor with a nulling resistor is used. To mitigate the offset of A_{DSL}, the first-stage PMOS and NMOS input pairs are chopped. Otherwise, the offset of A_{DSL} would appear at the output of A_1 and then be amplified to the final output. The choppers modulate the A_{DSL} offset, and the resulting ripple is then

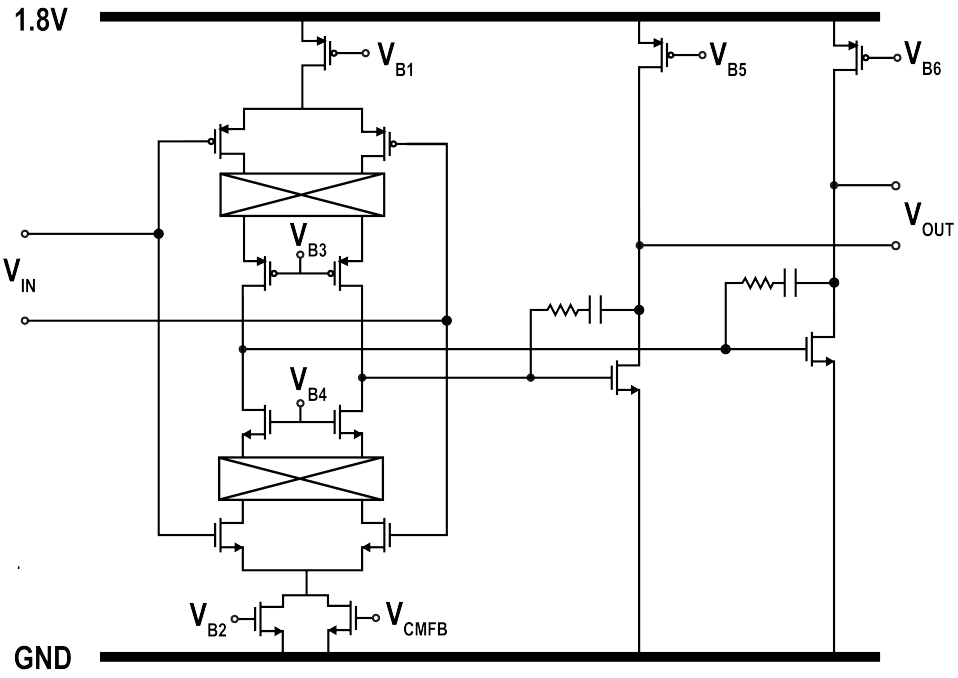

Figure 4.6: Schematic of A_{DSL}.

attenuated by the D3SL low-pass characteristic. Since $R_{s1,2}$ is much larger than R_2, and R_{fb} is much larger than R_{coil}, the noise contribution of the D3SL is negligible. From simulations, it only increases the output integrated noise by 5%.

4.2.3. TEMPERATURE COMPENSATION

As Hall-plate sensitivity is strongly temperature-dependent, a temperature compensation scheme is required. Otherwise, the Hall plates would exhibit a significant gain drift over temperature (> 20% from −70°C to 170°C [7]). The sensitivity of the Hall path can be expressed as (see Figure 4.7):

$$S_{\text{Hall-Path}} \propto I_{\text{Bias}} \times S_{\text{Hall}} \times \left(\frac{R_4}{2R_{\text{LPF}}}\right) \tag{4.6}$$

where I_{Bias} is the Hall-plate bias current and S_{Hall} is the current-related sensitivity of the Hall plate. It is worth noting that the gains of the CCAs (A_3 & A_4) used in the Hall path are temperature-independent, since they are set by capacitance ratios.

In [1, 5], a PTAT bias current with a large positive TC_{PTAT} is employed

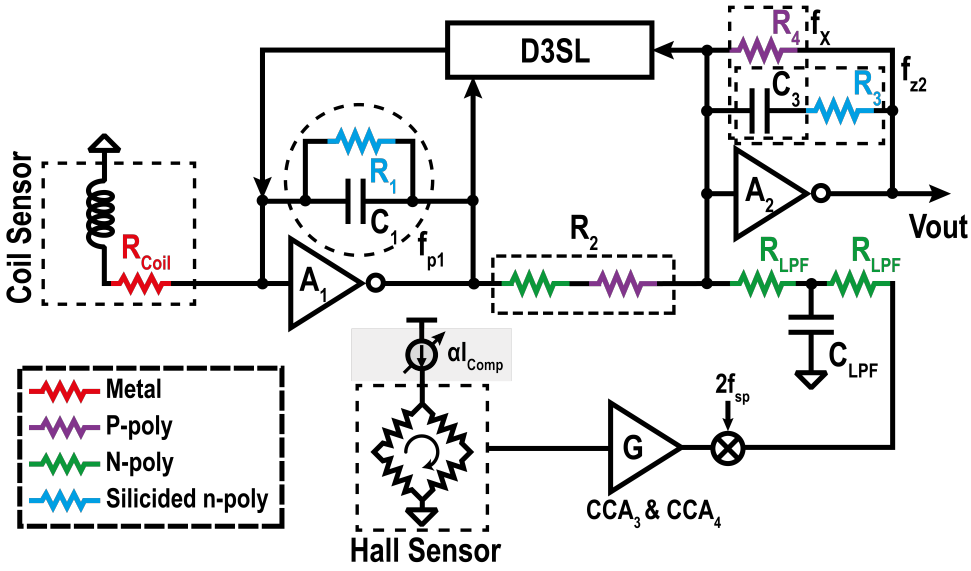

Figure 4.7: Temperature compensation scheme.

to partially compensate for the large negative TC (about −0.4%/K) of Hall plates. As the Hall plates are realized in an n-well layer with a large positive TC ($TC_{Nwell} = 0.37\%/K$), the supply voltage of the Hall plate has a very large TC of $TC_{PTAT} + TC_{Nwell} \approx 0.77\%/K$. This limits the maximum bias current at room temperature for a given supply voltage.

In this work, to simultaneously compensate for the Hall-plate gain drift and increase the maximum bias current, two different types of resistors are used as R_4 and R_{LPF} (Figure 4.7). R_{LPF} and R_4 are non-silicided n-poly (−0.15%/K) and non-silicided p-poly (−0.02%/K) resistors, respectively. Thus, the DC gain of the output stage has a positive TC of 0.13%/K.

The remaining Hall-plate sensitivity drift is compensated by using a tunable sub-PTAT bias current. As shown in Figure 4.8, the sub-PTAT bias current is generated by forcing a PTAT voltage ΔV_{GS} across two parallel resistors: a fixed non-silicided n-poly $R_{C1} = 5.7\,k\Omega$ and a tunable silicided n-poly $R_{C2} = 7.5\text{–}17.2\,k\Omega$. This tunability provides a ±9% tuning

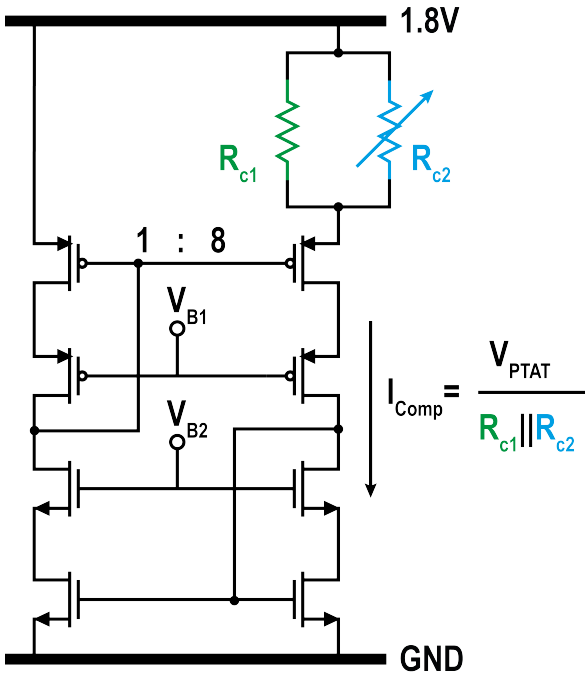

Figure 4.8: Tunable sub-PTAT bias generator.

range with a resolution of 0.3%.

As the coil path reads out the coil current and the coil is made of metal with a large temperature coefficient (TC) of 0.34%/K, a temperature compensation scheme is required to minimize the gain drift over the temperature in the coil path. The coil-path output is proportional to the ratio of resistors:

$$V_{\text{out,Coil}} \propto \begin{cases} \frac{R_1}{R_{\text{Coil}} \times R_2}, & f_X < f < f_{\text{p1,z2}} \\ \frac{R_3}{R_{\text{Coil}} \times R_2}, & f > f_{\text{p1,z2}} \end{cases} \tag{4.7}$$

In [1, 5], the temperature coefficient (TC) of the coil resistance R_{Coil} is compensated by using silicided n-poly (TC = 0.29%/K) and non-silicided p-poly resistors (TC = −0.02%/K) as $R_{1,3}$, and R_2, respectively. However, the residual TC causes a 2.7% gain drift over the temperature range. In this work, this residual TC is canceled by combining two types of resistors as R_2: 75% non-silicided p-poly (TC = −0.02%/K) and 25% n-poly (TC = −0.15%/K) resistors. This combination achieves the desired TC to cancel the residual TC.

4.3. MEASUREMENT RESULTS

The integrated hybrid current sensor was implemented in a standard 0.18-μm CMOS process and occupied 3.9 mm^2 (see Figure 4.9). Similar to [1, 5], it is mounted on a low-resistance (250 $\mu\Omega$) S-shaped current rail (Figure 4.9, bottom). The current flows through the current rail, generating a perpendicular magnetic field over the rail slots. The resulting magnetic field is then sensed via two coils and Hall plates positioned above the slots. The S-shaped geometry provides differential sensing and higher sensitivity ($\sim 2\times$) compared to a straight current rail. A non-conductive glue is used to isolate the chip from the current rail. The die thickness is 200 μm. This results in a current-to-magnetic coupling of about 283 μT/A. The sensor draws about 7.1 mA from a 1.8-V supply at room temperature. 60% of this current (4.4 mA) is used to bias the Hall plates. Each Hall plate consists of four Hall devices connected in parallel to reduce the initial offset. The current-related sensitivity of each Hall device is 45 V/A·T. Based on the geometry of the current rail, the coils consist of 43 minimum-width turns of top

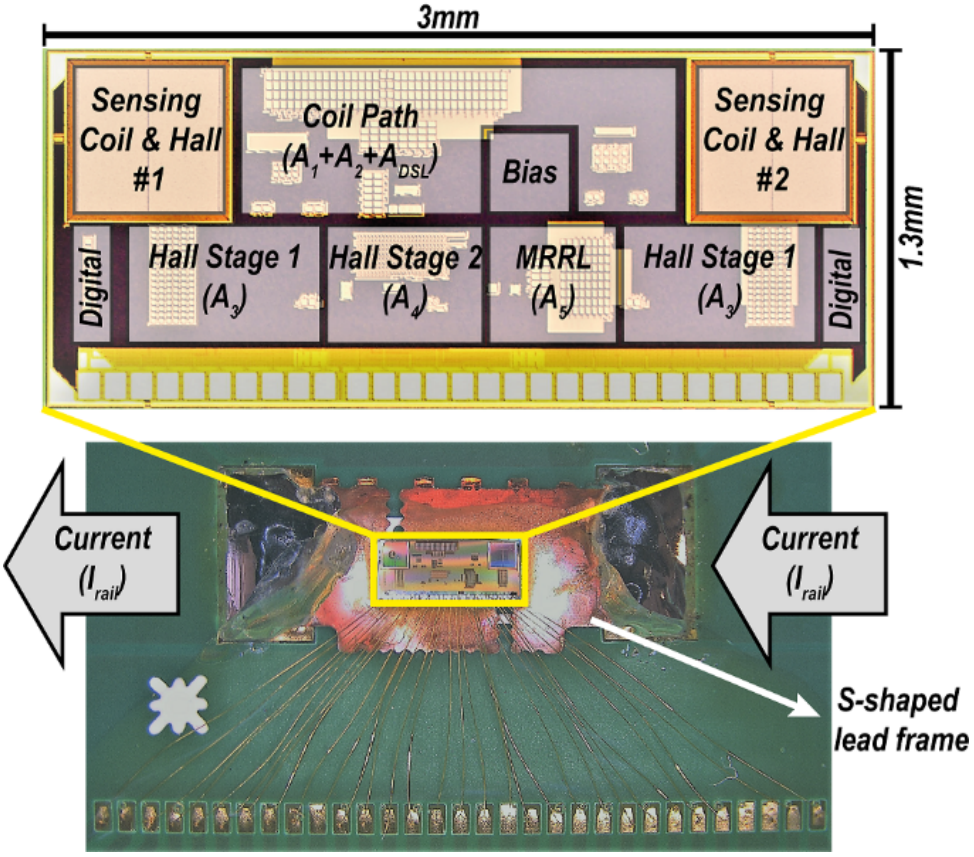

Figure 4.9: Sensor die on a copper lead-frame (Bottom) Die micrograph (Top).

metal with an outer width of 500 μm. Each coil can be modeled as a series inductance (1043 nH) with a resistance (3.3 kΩ), in parallel with a parasitic capacitor (3.95 pF). Simulations show that the coil current flowing into the virtual ground of A_1 has a differentiating characteristic up to ~ 100 MHz.

In this design, a spinning frequency (f_{sp}) of 25 kHz is selected to achieve a good tradeoff between offset and the filtered residual ripple.

Figure 4.10 shows the magnitude and phase of the sensor's overall frequency response with a 1-A input current through the current rail. Four samples have been measured. To achieve a flat frequency response, the Hall-plates biasing current is trimmed via an 8-bit current

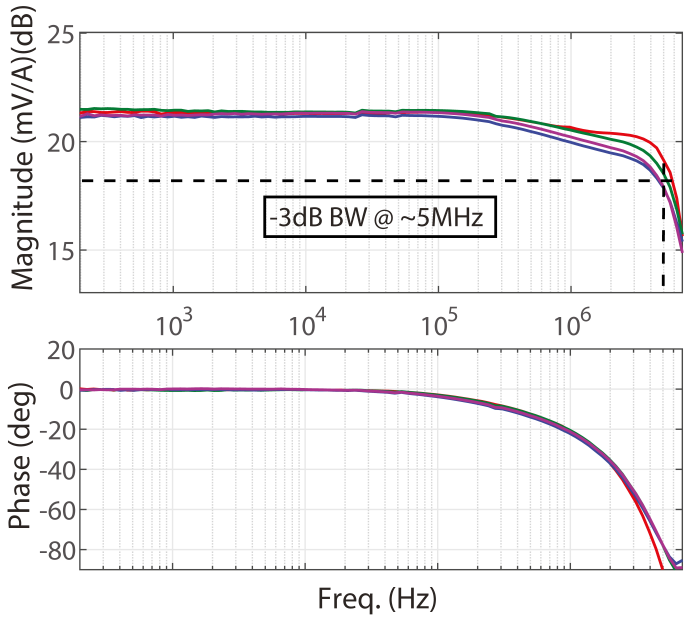

Figure 4.10: Sensitivity vs frequency (4 samples).

DAC. The −3 dB bandwidth (BW) of the sensor is approximately 5 MHz. At frequencies above 200 kHz, the gain decreases slightly due to eddy currents induced in the current rail [8]. This was confirmed by finite element method (FEM) simulations in ANSYS. These simulations show that eddy-current effects cause the flux through the coils to roll off at frequencies above 150 kHz, which agrees well with the measured data. Since each of the prototypes was assembled by hand, we attribute the observed spread in the roll-off to variations in the vertical distance between the coils and the lead-frame, as well as in the alignment of the coil centers with the slits. The sensor's frequency response around f_X is shown in Figure 4.11. The parasitic pole caused by the D3SL results in less than a 1% dip in the transfer function. The MRRL notches at f_{sp} and $2f_{\text{sp}}$ limit the gain variation to around ±1.1%.

The output spectrum at zero input current is shown in Figure 4.12. Enabling the MRRL reduces the spinning tones at f_{sp} and $3f_{\text{sp}}$ by more than 24 dB. Measurements on five samples show that the achieved reduction spreads from 22 dB to 26 dB.

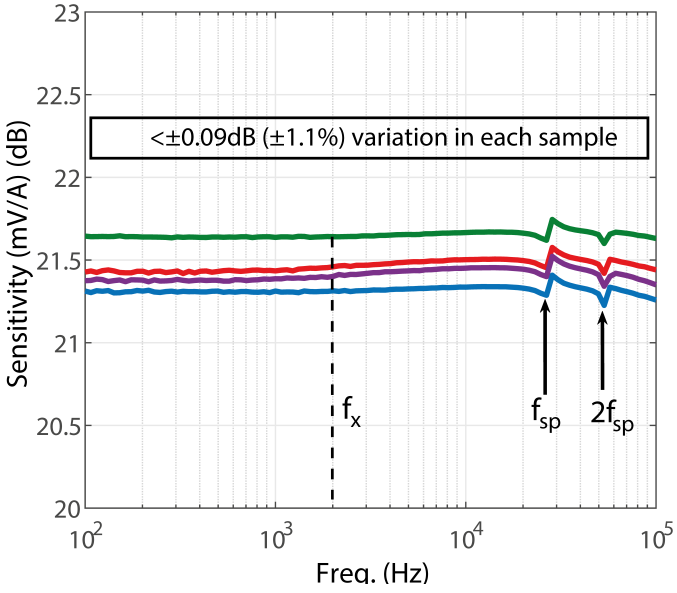

Figure 4.11: Zoomed in sensitivity vs frequency around f_X (4 samples).

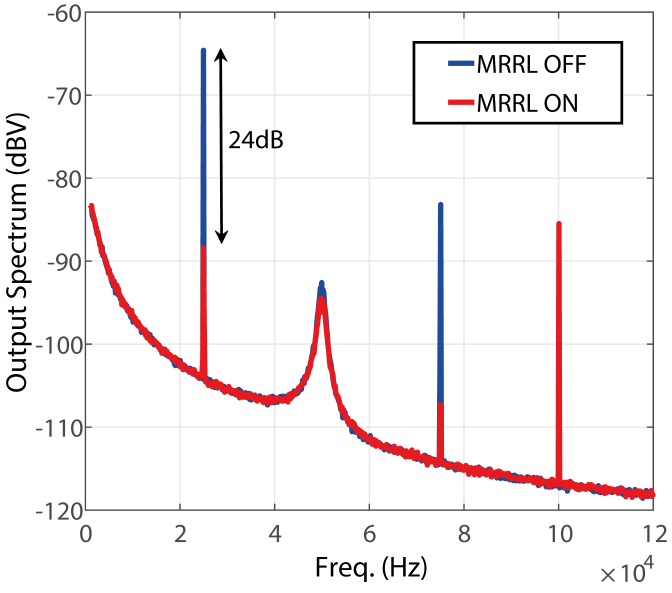

Figure 4.12: Output spectrum w/ MRRL on/off.

The noise spectral density and the accumulated noise are shown in Figure 4.13. The noise spectral density exhibits a 1st-order low-pass characteristic with a corner frequency of f_X (~ 2 kHz). At this frequency, the noise contributions of the coil path and the Hall path are equal. The integrated input-referred noise is 43 mA_{rms} in a 5 MHz bandwidth (BW). The total input-referred ripple is 5 mA_{rms}, which is more than 8× smaller than the integrated noise. In addition, the residual ripple at f_{sp} only causes a 0.3 mA step in the accumulated noise plot, demonstrating that the MRRL suppression is sufficient.

To verify the effectiveness of the proposed D3SL, the sensor offset (Hall + coil) of five samples has been measured (Figure 4.14). By enabling the D3SL, the offset is reduced from 600 μT (1σ) to 73 μT (1σ). Of this, about 60 μT (1σ) is due to the output-referred offset of A_2 and could be further reduced by, e.g., trimming.

The gain drift of the sensor is characterized in an oven from −40 °C to 85 °C. A 1-A input current is generated outside the oven and applied at 200 Hz and 80 kHz to measure the gain drift of the Hall and coil paths, respectively. The normalized sensitivities are shown in Figure 4.15.

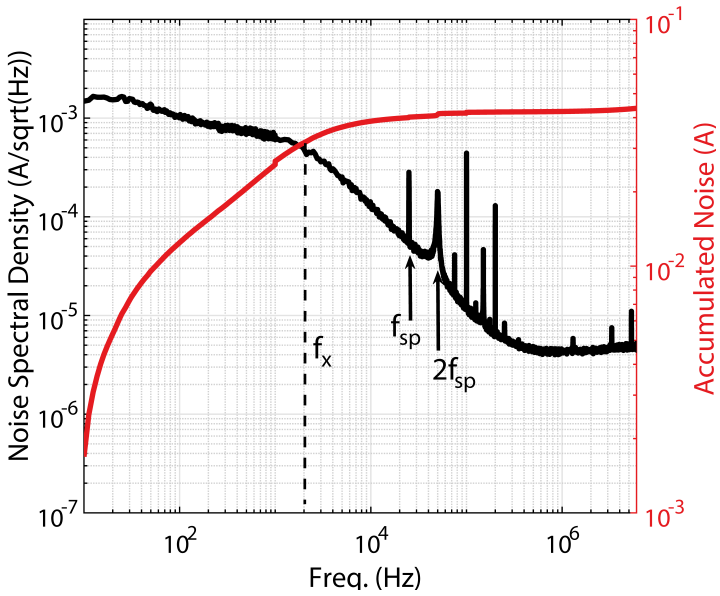

Figure 4.13: Noise spectral density and accumulated noise.

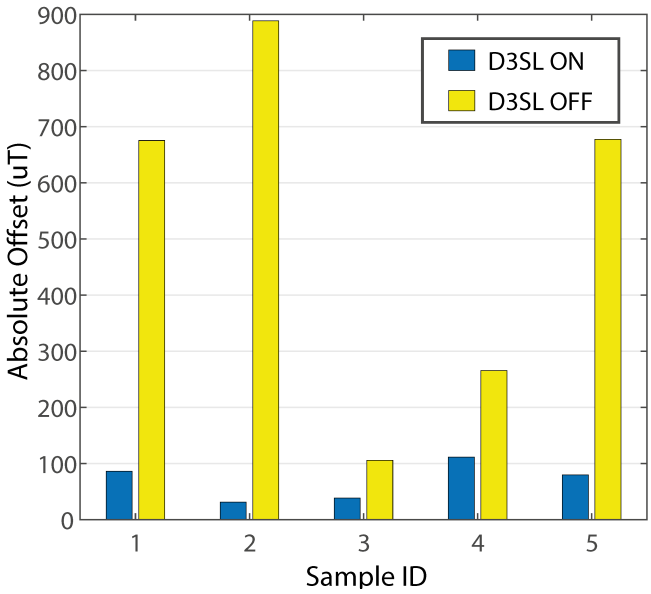

Figure 4.14: Sensor absolute offset (Hall) referred to current rail w/ D3SL on/off.

After fixing the TC trim setting, four samples have been characterized. With a fixed TC trim setting, the coil path and Hall path gain drifts are below ±0.9% and ±2.7%, respectively. The lack of temperature flatness is attributed to an insufficient trimming range, caused by a larger-than-expected component spread.

To evaluate the linearity of the Hall path, a DC current is applied to the current rail. As shown in Figure 4.16, the −1 dB compression point of the input current is 55 A, limited by the self-heating of the current rail. Due to the complexity of supplying large currents (tens of amps) at high frequencies, the input range of the coil path is determined by injecting a test current into the coil path (bypassing the coil sensors). This results in an equivalent input range of $72\,A_p$ ($51\,A_{rms}$).

The sensor's response to a $1\,A_{p\text{-}p}$ square wave and a $2\,A_{p\text{-}p}$ sine wave are illustrated in Figure 4.17 and Figure 4.18, respectively. The slight lack of amplitude flatness in the square-wave response is due to the residual gain mismatch between the Hall and coil paths.

Table 4.1 summarizes the performance of the proposed hybrid sensor

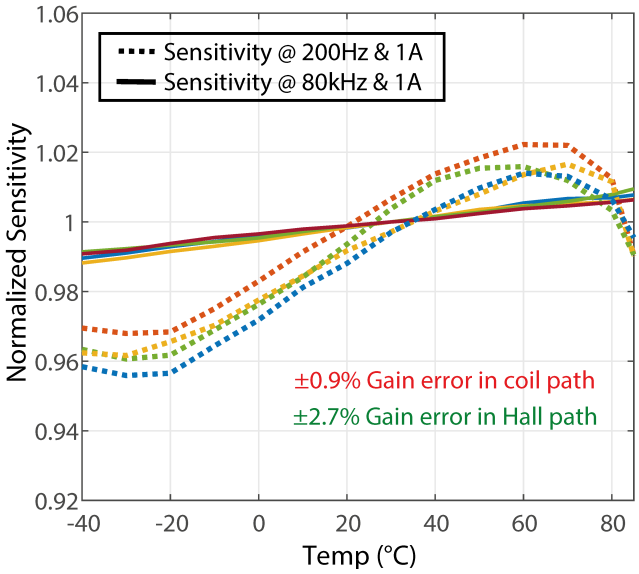

Figure 4.15: Sensitivity vs temperature (4 samples).

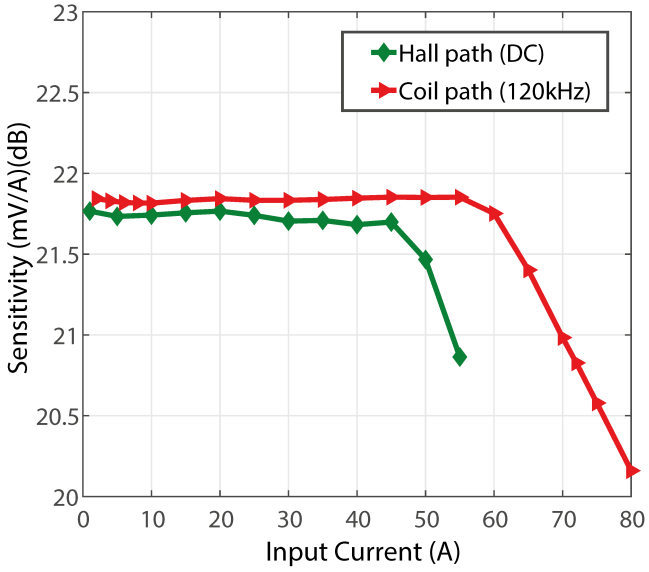

Figure 4.16: Sensitivity vs input range for DC and extrapolated AC(rms) currents.

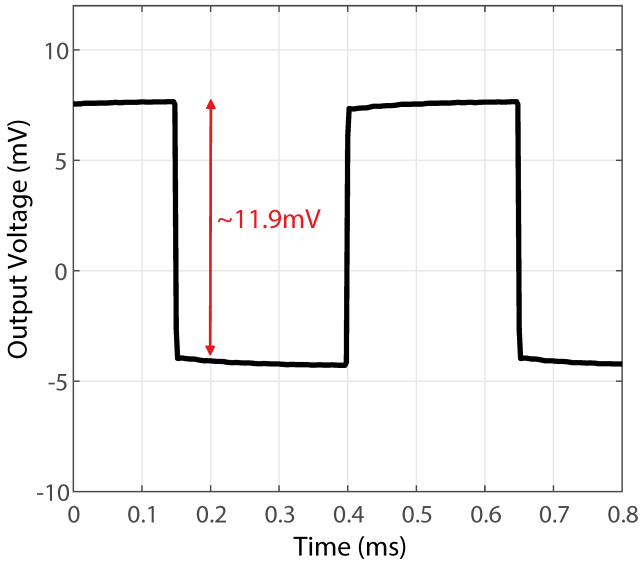

Figure 4.17: Transient response for a $1\,A_{p\text{-}p}$ square wave at $f_X = 2\,kHz$ (1024× averaging).

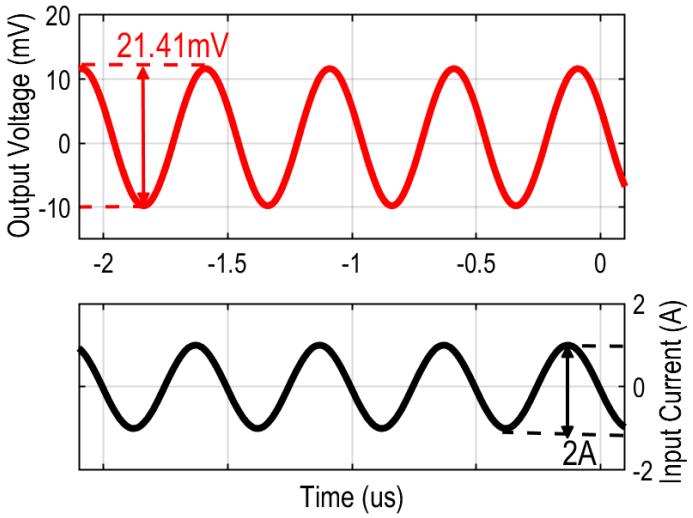

Figure 4.18: Transient response for a $2\,A_{p\text{-}p}$ sine wave at 1 MHz (1024× averaging).

Table 4.1: Performance Summary and Comparison

Source	**This Work**	JSSC'23 [5]	JSSC'17 [2]	JSSC'19 [9]	JSSC'22 [10]	APEC'19 [4]
Sensor Type	**Coil + Hall**	Coil + Hall	Coil + Hall	Hall	IFG	Coil + Hall
Technology (μm)	**0.18**	0.18	0.18	0.35	0.25	0.18
Supply (V)	**1.8**	1.8	5	3.3	1.8/5	1.8
Area (mm^2)	**3.9**	4.6	8.75	N/A	4+3.6	2.74
Resolution (mA$_{rms}$)	**43**	69	480	480	11[c]	710
Input Range (A)	DC: ±55[a] AC: ±51[a]	±46[a]	±18[a]	±300	±53[c]	±60
Dynamic Range (dB)	**61.5**	54	17	56	74	39
BW (MHz)	**5**	5	3	1.7	0.125	15.3
Power Consumption (mW)	**12.8**	14	38.5	13.2	100[d]+13	63.5
Gain Flatness	**±1.1%**	±1.5%	N/A	N/A	N/A	±3.7%
Residual Ripple @ f_{sp} (μT)	**1.5**	6	8	N/A	N/A	N/A
Residual Offset (μT)	**73**	57	40	262	N/A	N/A
FoM[b] (fW/Hz)	**0.45**	1.6	2281	5	8.5	145

[a]Extrapolated

[b]FoM = Power/(BW x (Range/Resolution)^2)

[c]Conversion rate = 45 μT/A

[d]Full-range power

in comparison to other state-of-the-art magnetic current sensors. Compared to prior hybrid sensors, the resolution (1.5×), dynamic range (+9.5 dB), and gain error (1.6×) have significantly improved. Furthermore, it achieves the highest energy-efficiency FoM (3×) among other magnetic current sensors.

4.4. CONCLUSION

This chapter presents a hybrid magnetic current sensor consisting of coil sensors and Hall plates for high and low frequencies, respectively. A 2-stage low-pass filter (LPF) reads out the coil current, while two capacitively coupled amplifiers (CCAs) amplify the upmodulated Hall voltage. By optimizing the crossover frequency f_X (2 kHz) for noise, the coil and Hall paths are combined. A dual differential DC servo loop (D3SL) reduces the coil-path offset from 600 μT to 73 μT. The D3SL acts similarly to a blocking capacitor between the coil-path stages in an area-efficient manner. With this approach, the D3SL introduces a parasitic pole at 15 Hz, which is more than 100× smaller than f_X and thus has a negligible effect (±1% dip) on the gain flatness. To achieve the same flatness and parasitic pole, a 100 nF blocking capacitor would have been required, occupying approximately 100× more chip area. The

gain drift over temperature in both paths is reduced by using different types of resistors. In addition, in the Hall path, a sub-PTAT bias generator is employed to cancel the residual temperature coefficient (TC) of the Hall path. This results in a gain error of ±0.9% and ±2.7% (from −40 to 85 °C) in the coil and Hall paths, respectively. Overall, the presented sensor is the most energy-efficient magnetic sensor reported so far, achieving a figure of merit (FoM) of 0.45 fW/Hz.

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5

MAIN FINDINGS AND FUTURE WORK

In this thesis, a number of CMOS hybrid magnetic current sensors have been described. This chapter will draw conclusions based on our findings and experimental results. In addition, we will propose some suggestions for further research and development in this field.

5.1. MAIN FINDINGS

The main findings of this work are listed below:

- By using coils to sense high frequencies, hybrid current sensors can break the bandwidth (BW) and resolution trade-off that limits the performance of Hall sensors.
- The resolution of a hybrid current sensor can be improved by optimizing its crossover frequency such that the noise contributed by its coil and Hall paths are balanced (see chapter 4).
- To achieve a flat frequency response, the sensitivities of the coil and Hall paths of a hybrid current sensor must be well matched over PVT. A practical way of achieving this is by using a self-calibration scheme (see chapter 3).
- To achieve a flat frequency response, the Hall path of a hybrid current sensor should have a 1^{st} order low-pass response, while the coil path should have a 1^{st} order high-pass response. Any

parasitic poles and zeros may then lead to gain-flatness errors. Mitigating these requires careful design (see chapter 3).

- Since the Hall path is responsible for DC sensing, the offset of the coil path should be blocked. Although this can be done with a blocking capacitor, this must be quite large to achieve good gain flatness. A dual-differential DC servo loop (D3SL) offers a more area-efficient alternative for implementing the blocking function (see chapter 4).
- The dynamic range of the coil path can be increased by reading out the current, rather than the voltage, induced in a coil by an external magnetic field. This also results in higher bandwidth, since this approach shorts out some of the coil's parasitic capacitance (see chapter 2).
- While the induced coil voltage is insensitive to temperature, the induced coil current is not. Since this is due to the coil's temperature-dependent resistance, it can be effectively compensated by using resistors with the appropriate temperature dependencies to define the gain of the coil path (see chapter 3).
- Employing the spinning technique significantly mitigates the offset of Hall sensors. Utilizing 4-phase spinning transforms the initial offset into a 4-level ripple, which can then be decomposed into three orthogonal signals. These signals can then be effectively attenuated using an area-efficient multiplexed ripple-reduction loop (see chapter 3).

Figure 5.1 illustrates the relationship between the bandwidth and resolution of CMOS magnetic sensors reported in IEEE publications from 2000 to 2025 (the full citations are listed in the appendix A). It shows a certain trade-off between bandwidth and resolution, which is broken by hybrid current sensors.

By taking power consumption and input range into consideration, a figure of merit (FoM) analogous to the energy efficiency FoM used in ADCs can be defined:

$$\mathrm{FoM} = \frac{\mathrm{Power}}{\mathrm{BW} \times \left(\frac{\mathrm{Range}}{\mathrm{Resolution}}\right)^2} \tag{5.1}$$

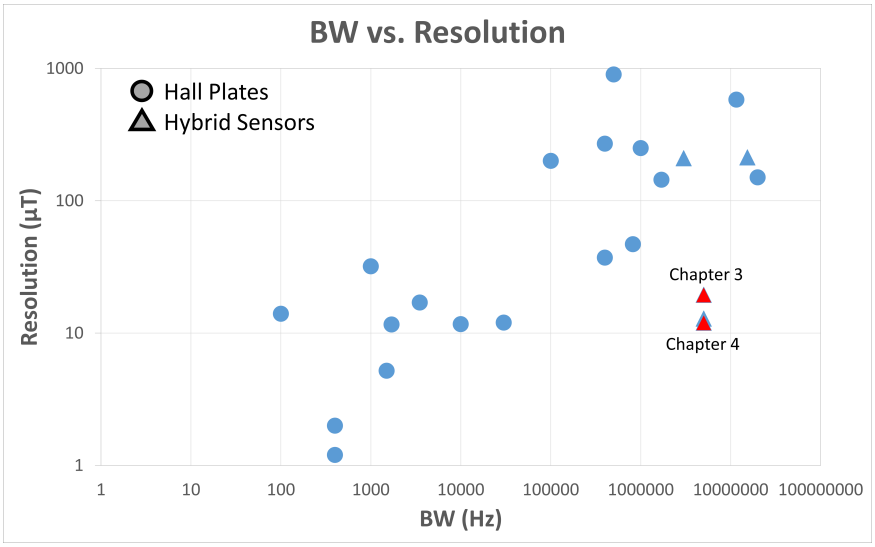

Figure 5.1: CMOS high-speed magnetic current sensors servo plot (as of May 2025) of resolution versus bandwidth.

Using this metric, the sensor introduced in chapter 4 emerges as the most energy-efficient magnetic sensor reported to date (see Figure 5.2).

5.2. FUTURE WORK

While the work described in this thesis represents a significant step in improving the performance of hybrid contactless current sensors, it is by no means the final chapter. The following are several areas where further improvements can be pursued.

5.2.1. ABSOLUTE SENSITIVITY CALIBRATION

The primary focus of this thesis was on the implementation of high-resolution and wide-bandwidth hybrid magnetic current sensors. A significant challenge in these sensors is maintaining gain flatness across frequencies. To address this, a self-calibration scheme was introduced, designed to automatically equalize the sensitivities of the two sensor paths. This scheme performs relative sensitivity calibration, enabling the Hall path sensitivity to be adjusted according to the coil path sensitivity by adjusting the Hall-bias current. However, the system still

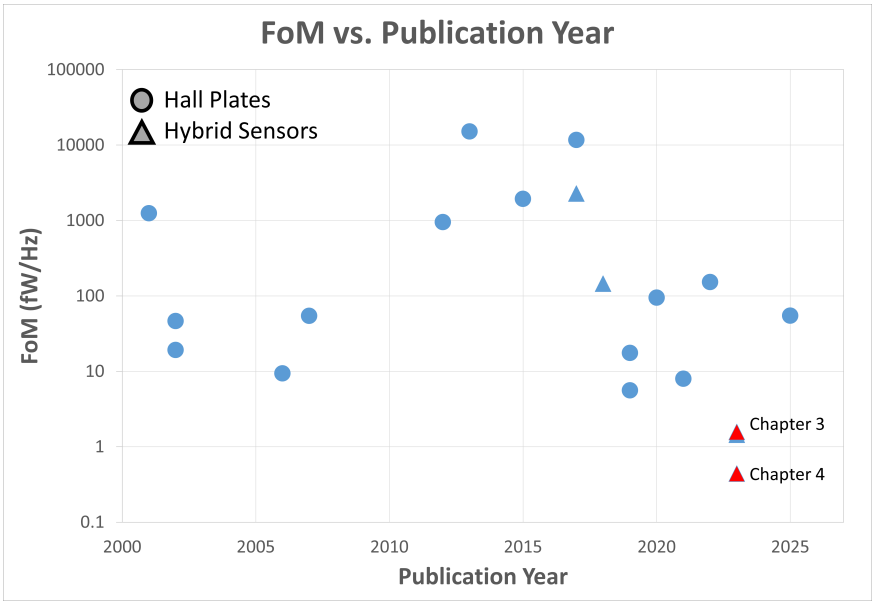

Figure 5.2: CMOS high-speed magnetic current sensors servo plot (as of May 2025) of FoM versus publication year.

requires absolute sensitivity calibration to compensate for tolerances in the distance between the sensor and the current rail. Furthermore, as discussed in section 3.2.2, since the sensor's output beyond the crossover frequency (f_X) is inversely proportional to on-chip RC time constants, calibration is required to compensate for process spread. This calibration can be achieved by applying a known reference current to the current rail and adjusting the sensor sensitivity to match a target value. Fine-tuning the sensitivity can be implemented by incorporating a programmable gain amplifier (PGA) after the summing amplifier.

5.2.2. Stress Compensation

Another point to consider is that the sensitivity of Hall sensors is influenced by packaging stress. To mitigate this, a stress-compensation scheme could be integrated into the system [1–4]. This would maintain the sensor's accuracy in the presence of stress variations, thereby enhancing its robustness and reliability over lifetime.

5.2.3. DIGITAL OUTPUT

Another potential enhancement to the hybrid current sensors described in this thesis is the inclusion of an ADC to provide a digital output. This would also improve the precision and versatility of the sensor by enabling direct interfacing with digital signal processing systems and microcontrollers. An additional enhancement could be to digitize the outputs of the Hall and coil paths individually and combine them in the digital domain.

5.2.4. 3-PATH ARCHITECTURE

An additional future direction could be to extend the hybrid architecture to include three sensing paths: a spinning Hall plate for low frequencies, a non-spinning Hall plate for mid frequencies, and a pickup coil for high frequencies (see Figure 5.3). This configuration would offer greater flexibility by enabling independent control over two crossover frequencies, f_{X1} and f_{X2}. Specifically, f_{X1} can be tuned to improve ripple suppression caused by the spinning technique, while f_{X2} can be optimized for better noise performance. Additionally, it enables a lower spinning frequency, thereby improving offset performance. It should be noted that selecting f_{X1} significantly smaller than f_{X2} can substantially reduce the residual gain flatness error introduced by the RRL notches.

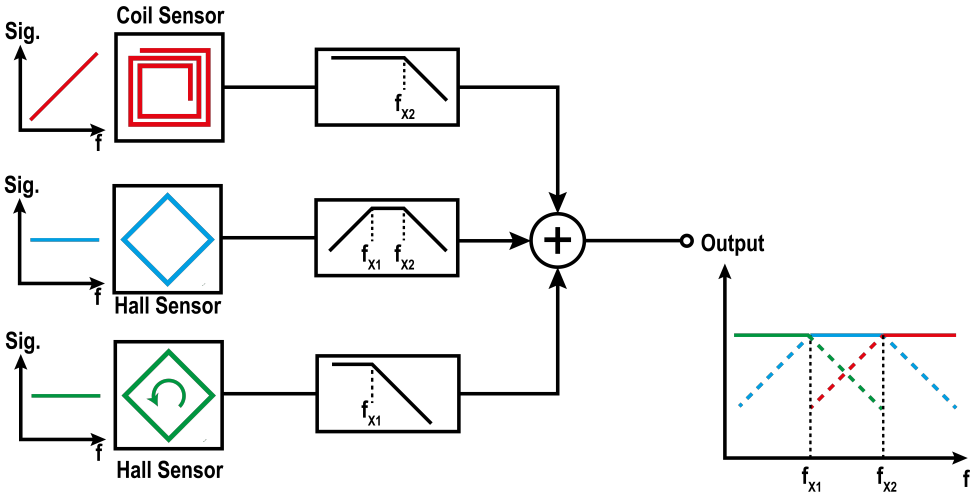

Figure 5.3: Conceptual diagram of the proposed 3-path architecture.

5.2.5. HIGHER-ORDER SUMMING FILTER

Another possible improvement involves replacing the first-order low-pass filter (LPF) with a higher-order summing filter to achieve improved ripple suppression.

For example, Figure 5.4 illustrates a hybrid current sensor architecture that employs a second-order passive LPF. In this configuration, the coil signal is first flattened via an integrator, after which a second-order passive filter combines the coil and Hall paths. The filter comprises two resistors and two capacitors. The transfer function (TF) from the Hall-plate signal to the output corresponds to a second-order LPF, exhibiting two poles. Meanwhile, the TF from the integrator output to the final output forms a second-order high-pass filter (HPF) with two poles and two zeros. Together, these complementary paths result in a flat overall frequency response from DC to high frequencies.

Compared to a first-order implementation, the second-order LPF provides a steeper roll-off of 40 dB/decade instead of 20 dB/decade, thus enhancing ripple rejection. Furthermore, this concept can be extended to even higher-order crossover networks for greater ripple suppression.

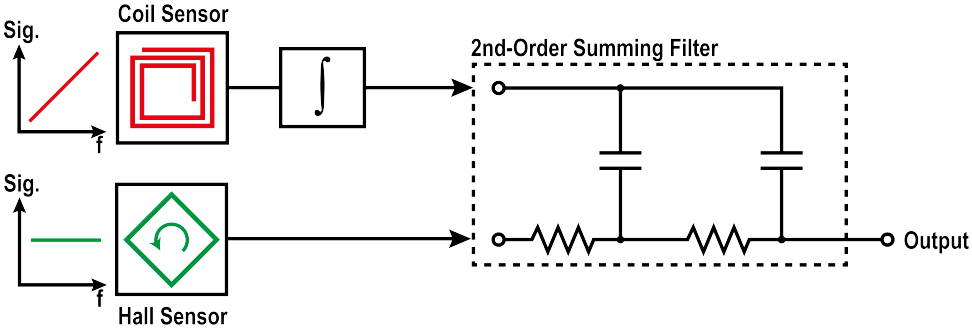

Figure 5.4: A hybrid current sensor with a second-order summing filter.

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APPENDIX

In this doctoral dissertation, one survey chart is utilized for reference and comparison, drawing upon existing literature in the field. The selection of publications for this survey was narrowed down to ensure relevance to the core topics of this research. The criteria for inclusion were as follows:

- Focus on CMOS-based design approaches.
- Availability of bandwidth and noise measurements, or the possibility of deriving these metrics.
- For current sensors that do not report the current-to-magnetic coupling factor, a value of 300 μT/A is assumed, corresponding to the coupling factor of the S-shaped leadframe used in this work.
- Publications originally issued from January 2000 to May 2025 in key conferences and journals, including:
  - **Conferences:**
    - IEEE International Solid-State Circuits Conference (ISSCC)
    - IEEE Symposium on VLSI Circuits (VLSI)
    - IEEE European Solid-State Circuits Conference (ESSCIRC)
    - IEEE Asian Solid-State Circuits Conference (A-SSCC)
    - IEEE Custom Integrated Circuits Conference (CICC)

- IEEE Sensors
- IEEE International Conference on Electronics Circuits and Systems (ICECS)
- International Conference on Environment and Electrical Engineering (EEEIC)

– **Journals:**

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE Sensors Journal

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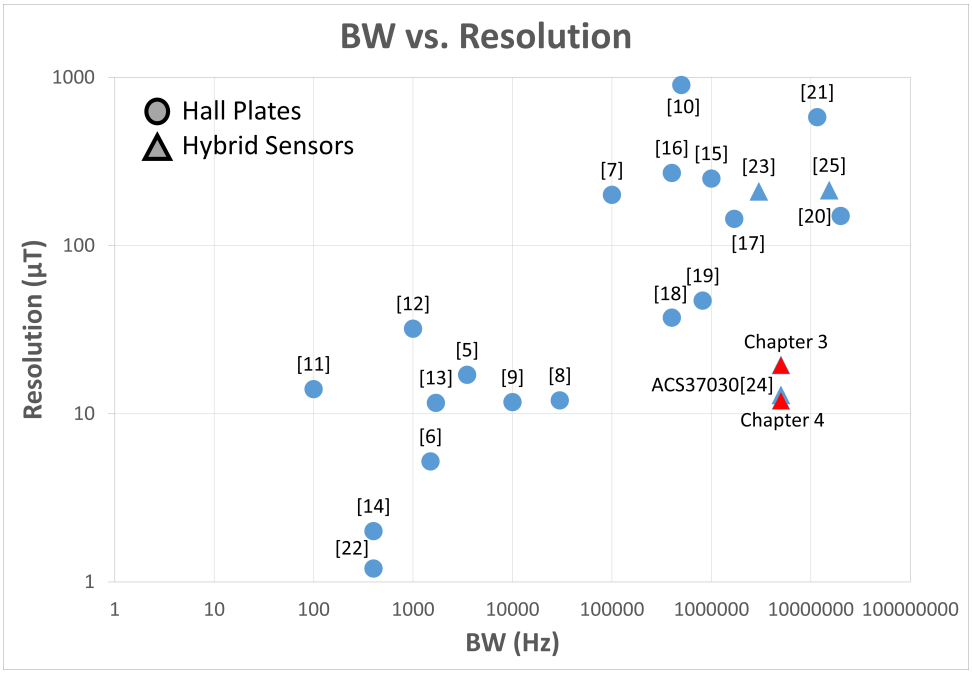
BW vs. Resolution
Hall Plates
Hybrid Sensors
Resolution (µT)
BW (Hz)
1000
100
10
1
1
10
100
1000
10000
100000
1000000
10000000
100000000
[10]
[21]
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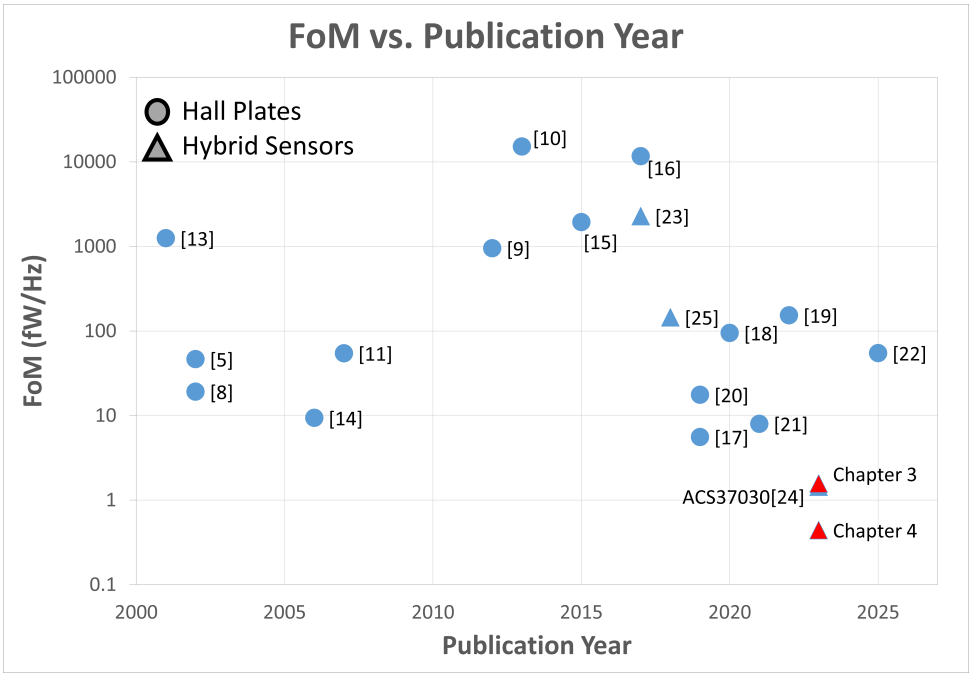
FoM vs. Publication Year
Hall Plates
Hybrid Sensors
FoM (fW/Hz)
Publication Year
100000
10000
1000
100
10
1
0.1
2000
2005
2010
2015
2020
2025
[10]
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List of Publications

Journal Papers

- **A. Jouyaeian**, Q. Fan, R. Zamparette, U. Ausserlechner, M. Motz and K. A. A. Makinwa, "A Hybrid Magnetic Current Sensor With a Multiplexed Ripple-Reduction Loop," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 10, pp. 2874–2882, Oct. 2023.

- **A. Jouyaeian**, Q. Fan, U. Ausserlechner, M. Motz and K. A. A. Makinwa, "A Hybrid Magnetic Current Sensor With a Dual Differential DC Servo Loop," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 12, pp. 3442–3449, Dec. 2023.

Conference Papers

- **A. Jouyaeian**, Q. Fan, M. Motz, U. Ausserlechner and K. A. A. Makinwa, "5.6 A 25A Hybrid Magnetic Current Sensor with 64mA Resolution, 1.8MHz Bandwidth, and a Gain Drift Compensation Scheme," *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021, pp. 82–84.

- **A. Jouyaeian**, Q. Fan, M. Motz, U. Ausserlechner and K. A. A. Makinwa, "23.3 A 51A Hybrid Magnetic Current Sensor with a Dual Differential DC Servo Loop and 43mArms Resolution in a 5MHz Bandwidth," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 22–24.

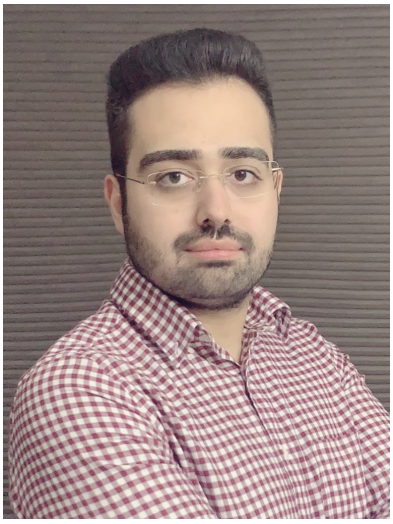
- E. Aydin, **A. Jouyaeian**, Z. Tang and K. A. A. Makinwa, "A Direct Conversion Transceiver for Portable Microfluidic NMR Flowmeters," *2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*, Bruges, Belgium, 2024, pp. 536–539.

PATENTS

- M. Motz, Q. Fan, **A. Jouyaeian**, K. A. A. Makinwa, "Apparatuses and methods for electrical current sensing," Patent, US11668767B2, Jan. 2022. Assignee: Infineon Technologies AG.

- M. Motz, **A. Jouyaeian**, K. A. A. Makinwa, "Hybrid high-bandwidth magnetic field sensor," Patent, US11828625B2, April 2022. Assignee: Infineon Technologies AG.

About the Author



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