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Scalable multi-chip quantum architectures enabled by cryogenic hybrid wireless/quantum-coherent network-in-package

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Abstract—The grand challenge of scaling up quantum computers requires a full-stack architectural standpoint. In this position paper, we will present the vision of a new generation of scalable quantum computing architectures featuring distributed quantum cores (Qcores) interconnected via quantum-coherent qubit state transfer links and orchestrated via an integrated wireless interconnect.

Index Terms—Scalability quantum computing systems, full-stack architecture design.

I. PROPOSED VISION

Today's tremendous interdisciplinary efforts towards building a quantum computer is aimed at a machine capable of tackling problems beyond the reach of any classical computer. The so-called quantum advantage, a term referring to a quantum computer performing a specific computation that is intractable for a classical computer, has been recently claimed with state-of-the-art Noisy Intermediate-Scale Quantum (NISQ) computers consisting of several tens of quantum bits (qubits) [1]. Nevertheless, it is widely recognized that addressing any real-world problem will require upscaling to thousands or even millions of qubits [2]. Scaling quantum computers to such a large number of qubits is a major challenge due to, among others, the confluence of (i) technology factors confining the qubits to low fidelity, (ii) the need for cryogenic temperatures to reach practical coherence times, (iii) the dense integration of digital/RF control circuits, which are needed on a per-qubit basis [3], and (iv) the manifold architectural and algorithmic implications of managing noisy and short-lived qubits. The scaling-up race is fiercely complex and mostly revolves around the qubit technological aspects, but the bottleneck will very soon shift to the architectural problems stemming from the need to densely pack together the qubits and their classical electronics interfaces.

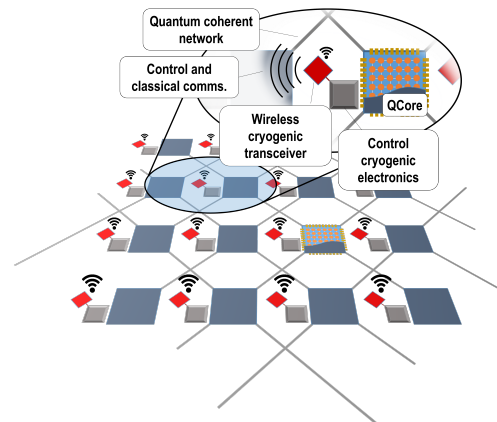


Fig. 1: The multi-Qcore architectural vision.

In analogy to early von Neumann computers, the first approach to the scaling of quantum computers has been to monolithically and densely integrate qubits within a single large array on the same silicon substrate, next to their classical control electronics. However, such a solution would impose an impractically high density of interconnects wiring the electronics at the array boundary to every single qubit or, in case of sharing of control lines, impractical requirements on qubit uniformity, increased noise (crosstalk) and limited yield. A viable architectural alternative proposed by leading quantum computing experts is to split the quantum processor into smaller cores (named here as Qcores) to be sparsely placed [4]–[6]. This approach is by no means trivial, though, as it implies the development of (i) appropriate architectural means to seamlessly manage multiple quantum cores, i.e. a multi-Qcore architecture, (ii) an interconnect that supports

the quantum and digital communication needs of such architecture, and (iii) a compact integrated quantum-coherent shared medium (i.e. preserving quantum state coherence) to realize the quantum side of the interconnect. These key aspects are crucially missing and require a leap beyond the current technology to be realized.

In this context, this position paper envisions creating post-NISQ massive quantum processors through the development of scalable architectures with multiple Qcores interconnected via quantum links within the cryogenic package (see Figure 1). This is only possible by providing a quantum-coherent alternative to the rigid, static and wire-dense interconnects that are nowadays commonplace in quantum computers. Specifically, an ideal multi-Qcore interconnect fabric should not only support many simultaneous quantum state transfers across the Qcores, but also include a complementary control fabric capable of orchestrating such quantum state exchanges. If realized, this would unleash the architectural scalability potential of quantum computers by virtue of a balanced adaptive trade-off between communication and computation functions.

To realize this vision, this paper proposes an all-RF solution to the problem of building an integrated, scalable, and agile network spanning both quantum state and classical data transfers. This solution takes the form of multi-chip quantum cavity links compactly co-existing with wireless communication networks at cryogenic temperatures, both built on the solid grounds of cryogenic RF technology already developed for qubit interfacing. This approach encompasses solid experimental foundations of this interconnect fabric, but also demonstrating its paradigm-shifting architectural implications with a cross-cutting approach. In Section II, this vision is further articulated, and in the subsequent sections the related multidisciplinary fields are discussed, with a final Section VII devoted to a proposed design space exploration methodology across layers to assess the feasibility of this vision.

II. MULTI-CORE QUANTUM COMPUTING ARCHITECTURES ENABLED BY A HYBRID INTERCONNECTION NETWORK

One of the main challenges for scaling up quantum computers is the wiring between the quantum processor and control electronics [7]. Existing quantum computers physically span several temperature levels, with the qubits typically operating at sub-1-K temperatures to ensure their coherence, while the classical control electronics are operating at room temperature. While this thermal gap can be readily bridged by a few wires for the small quantum processors available today (<100 qubits), it would be impractical to wire thousands or millions of qubits in future quantum computers due to wiring size and reliability issues. Recent advances are closing this vertical gap by pushing the qubits to operate at temperatures near 4K [8], where cryogenic refrigerators can dissipate the heat generated by the classical control electronics, and by developing cryogenic analog/RF control circuits that can be potentially co-integrated with the qubits at the same temperature level [7]. Additionally, recent research advocates for also moving digital

circuits to cryogenic temperatures [9], an approach that further alleviates the wiring bottleneck.

Although the full-cryogenic computer resulting from closing the vertical gap would be more compact than today's prototypes, scaling issues remain in the horizontal dimension. Specifically, scaling this integrated scheme to a very large number of qubits as a single array (Qcore) is deemed unfeasible due to the practical bottleneck in the wiring between the qubits and their interface electronics [4]. Moreover, other issues arise when integrating a high amount of qubits on a single chip, such as crosstalk, limited yield and qubit addressability. Instead, the multi-Qcore vision proposed here assumes N_c quantum chips, with each chip hosting a Qcore composed of a moderately sized array of N_q qubits. Thus, the Qcores can be spaced to fit the local electronics next to each core, thereby improving qubit addressability and reliability. Connecting the Qcores via quantum links allows the ensemble to remain coherent, thus maintaining the computational power of $N_c \times N_q$ entangled qubits, i.e. $O(2^{N_c N_q})$, rather than the incoherent addition of the Qcores, $O(N_c 2^{N_q})$. The realization and integration of such quantum links at the chip scale is a fundamental challenge that has not been addressed yet.

The first key element to enable the vision is an expansive quantum channel as enabler of the quantum interconnect fabric. The other key element in the vision (in hybrid co-existence) is a multi-chip interconnection network that, with the exchange of classical data, coordinates the emitter and receiver of the quantum state transfer, and enables the sharing of control signals and data across the Qcores. Without such an interconnection network, all data would have to go through the vertical connections to the host computer and back, which quickly becomes a roadblock. One could implement the inter-Qcore network through wired interconnects, yet this approach has drawbacks such as the difficulty of routing physical wires through the already densely wired system, or the high latency of system-wide transfers, which are critical for control. In this position paper, instead, we propose to realize the classical side of communications by means of a compact, high-bandwidth, highly reconfigurable wireless in-package network. The main idea is to integrate on-chip cryogenic antennas with RF cryogenic transceivers (developed with the same technology and techniques already employed in existing high-frequency qubit control circuits) so as to implement a wireless network within the quantum computing package. The resulting network is naturally system-wide and broadcast, allowing for agile reconfiguration of the underlying architecture. Moreover, although designing integrated circuits beyond their originally intended temperature operating range presents several challenges, the cryogenic environment is expected to opportunistically boost the antenna efficiency, reduce the thermal noise, and improve the transistor speed [7], [10].

III. QUANTUM-COHERENT HIGH-Q PLANAR CAVITY LINKS

Seamless micro-integration of cryogenic quantum communication links with quantum computational functions is the key enabler for the scaling and pervasive use of quantum

information technology platforms [11]. Optical photons have widely been used for high-fidelity remote entanglement and quantum state transfer [12]. However, optical quantum state transfer is highly probabilistic due to inefficiencies in photon coupling and transfer [13], placing fundamental limits on its use for inter-Qcore communication rates. In contrast, microwave cavities and circuits can combine low loss with strong coupling and are therefore well suited for on-demand high-rate quantum transfer, and thus to scale-up quantum computational architectures in a modular fashion. To date, a limited amount of microwave quantum communication solutions has been demonstrated, concentrating mainly in quantum register coupling [14]. Switchable quantum cavity channels to directly and resonantly entangle qubits from different Qcores are proposed to be implemented in the microwave and mm-wave frequency bands, and their CMOS-compatible heterogeneous integration into multi-Qcore solutions will be modeled, technological integration route developed, experimental demonstrator built-up and performance and limitations quantified.

The qubits will be strongly coupled to a substrate dielectric waveguide [15], allowing direct, fast and tightly coupled transfer of quantum information from qubits to microwave photons and vice versa. Depending on the quality factor of the quantum cavity channel, the substrate material will be a hollow waveguide or sapphire which can provide low loss ($\tan \delta \sim 5 \cdot 10^{-7}$) and quality factors exceeding $Q > 10^6$. These features are essential for the efficient transmission and storage of microwave photons in the cavity. However, the high Q of the cavity leads to an extremely narrow-bandwidth frequency response, which requires tuning to and of the qubits' resonance frequencies. This will be achieved by using a tunable coupler realized as a resonator with a tunable center frequency and tuning the qubit frequencies in resonance with the cavity waveguide. The planned dielectric waveguide can accommodate multiple modes, which can be used to selectively couple or decouple specific qubits in a multi-Qcore array, enabling frequency-multiplex quantum architectures. In this direction, two fundamental state-of-the-art challenges are addressed: (i) nanoscopic integration via plasmonic cavity approaches [16] in order to provide a robust and monolithic integration technology with potential for tightly integrated wireless multi-Qcore communications, and (ii) low-loss, high quality-factor, low-noise coupling between neighboring Qcores providing inter-Qcore entanglement for massive quantum computation scalability. Microwave (~ 12 GHz) and mm-wave technologies are addressed to explore the advantages and limitations of alternative channel configurations.

IV. CRYO-CMOS RF TRANSCEIVERS

Nanometer-scale CMOS electronics operating at cryogenic temperatures (cryo-CMOS) is widely accepted as the preferred IC technology for quantum-processor interfaces, thanks to its capability to operate down to (at least) 30 mK, its unmatched very large scale of integration (VLSI), and the mature design automation infrastructure, all necessary to handle millions of qubits [10], [17]. Several cryo-CMOS individual circuit blocks

have been demonstrated, as required for qubit control and co-integration. A broad range of cryo-CMOS interface circuits for the control and readout of qubits has been recently shown, including complex microwave transmitters operating at 4 K providing <100 MHz data bandwidth/qubit for <-16 dBm output power at a carrier frequency <20 GHz [7], [18], RF receivers [19] and high-speed baseband data converters [20]. Nevertheless, the lowest reported operating temperature for a wireless transceiver is 170 K [21], and no deep-cryogenic transceiver has been demonstrated.

In this work, it is proposed to implement the first-ever deep-cryogenic wireless transceiver, operating down to 4 K. To miniaturize the on-chip antenna, the operating frequency is expected to increase $> 3\times$ beyond the state-of-the-art for cryo-CMOS, while the data bandwidth and the transmitter's output power will both be extended by $> 20\times$ beyond the state of the art to realize a robust communication between the qubit tiles. We will explore using the waveguide proposed in section II for classical data transmission at 60 GHz by exciting the waveguide with an on-chip antenna and by minimizing the crosstalk to the quantum channels.

V. COMMUNICATION INTRANET WITHIN A QUANTUM COMPUTER

For an appropriate architectural integration of all-RF interconnects, the quantum photon and RF propagation within a quantum package needs to be characterized, and adequate communication protocols must be developed. On the one hand, existing works in channel modeling are mostly simulation-based studies for conventional computing chips at room temperature, at the mm-wave band and in the frequency domain only [22]. In contrast, for quantum computers at cryogenic temperatures, this field is at its infancy and the only relevant work is at microwave frequencies and not oriented to communications [23]. Hence, there are no models capable of capturing the particularities of the channels within quantum computer packages and cavities, which differ substantially from those in conventional computers, and at cryogenic temperature. We propose to explore this uncharted territory and provide a complete channel model in the time and frequency domains.

Since it appears to be the first time that multi-chip wireless/quantum interconnects are proposed for quantum computers, adequate protocols are missing. Protocols for quantum communications are currently limited to large-scale Quantum Internet proposals, which are grounded on the distribution of entangled pairs with repeaters at kilometer distances [24]. These assumptions do not apply to the proposed vision scenario, which is based on cavity-enabled quantum coupling at chip-scale distance and shows tight interplay with computation and high latency criticality. On the wireless transmission of classical data at the chip scale, the existing research has focused on theoretical wireless on-chip networks for conventional processors with tens of transmitters. MAC protocols are generally variants of token passing, seeking simplicity and performance [25]; whereas, at the network layer, wireless links are generally considered fixed unicast

connections between distant cores [26]. None of these works has therefore considered the unique problem addressed in this position paper, namely the need for protocols to manage the access to potentially hundreds of latency-critical, computing-driven quantum links at cryogenic temperatures, with the implications that this has on the design of protocols for the non-quantum wireless links. We propose to develop a protocol stack covering both the quantum and non-quantum planes and capable of systematically leveraging architectural information to maximize the system performance.

VI. ARCHITECTING SCALABLE AND RECONFIGURABLE QUANTUM PROCESSORS

NISQ devices are publicly accessible (e.g., IBM Q experience, Qinspire) and users can already run small instances of quantum algorithms. However, these quantum processors suffer from several constraints, such as limited connectivity among the qubits. This requires the quantum compiler to modify the quantum algorithm, described as a quantum circuit, to realize it on a given quantum chip. This transformation process is known as mapping and might compromise the successful execution of the algorithm [27].

Exact approaches for small-size quantum circuits and approximate mapping solutions using heuristics for larger quantum circuits have been developed for specific single-core NISQ devices [28], [29]. Recently, the first compiler techniques for mapping and scheduling quantum algorithms onto connectivity-simplified multi-core quantum architectures have been proposed [30], [31] as distributed or modular architectural approaches are becoming more prominent for scaling-up quantum hardware [4]–[6], [32]. These mapping solutions all focus on multi-Qcore architectures that assume all-to-all intra- and inter-core connectivity with unlimited and ideal communication resources and a fixed and invariant interconnection network. In this work it is proposed to build on top of these quantum hardware advances and define scalable multi-Qcore architectures, including the communication perspective and the required compilation techniques, connecting today's experiments with future practical implementations. We will also perform on-line dynamic optimizations of the Qcores transfers for an efficient execution of the algorithms leveraging the reconfigurability provided by the wireless control plane.

VII. DESIGN SPACE EXPLORATION FOR ARCHITECTURE/NETWORK/CIRCUIT/LINK CO-DESIGN

Although quantum computers already exist in the form of intermediate-scale quantum processors, there is no consensus in the quantum computing community on what benchmarks and metrics to use to compare them and to assess their performance. As a first attempt, IBM proposed Quantum Volume (QV) and Circuit Layer Operations Per Second (CLOPS) as metrics to measure three key quantum computing performance attributes: quality, speed and scale [33]. Also, different sets of quantum benchmarks for assessing their overall performance have been introduced [34], [35]. In addition, the higher layers of full-stack systems, consisting of both quantum software

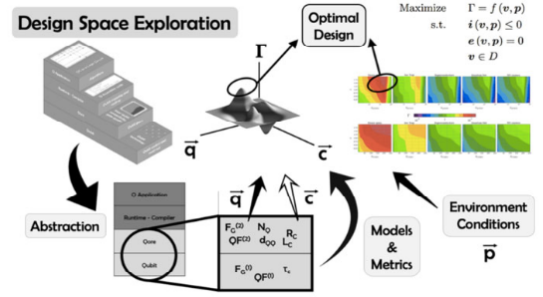


Fig. 2: Exploration framework for quantum computing architectures.

and classical control hardware, have been so far designed and provided solutions following a bottom-up approach; that is, they have been developed for a specific quantum device. This approach is appropriate for a single rigid design, which could be functional, but it is unclear how close it is to the optimal design in terms of overall performance and scalability, and how such performance holds in different specifications. This is particularly critical in the harsh constraints of quantum computing. In addition, a long-standing perceived need from the quantum community identifies the lack of design guidelines from top architectural layers down to physical ones or even cross-layer co-design [36], [37].

In this work, we propose to employ structured Design Space Exploration (DSE) methodologies to perform a cross-layer co-design of the full-stack quantum system, including both communication and computation, allowing for both top-down and bottom-up optimizations across layers (see Figure 2). To this purpose, models will be developed that describe (i) the computational part, from the distributed architecture down to the single Qcore and qubit impairments, and (ii) the classical and quantum communication parts from the perspective of performance (e.g. throughput, fidelity) and efficiency (e.g. power). Finally, we will create and profile a set of large-scale benchmarks able to stress the multi-Qcore platform and define different performance metrics of the overall architecture.

VIII. CONCLUSIONS

This position paper addresses from a full-stack architectural perspective the challenge of scaling up quantum computers. A vision is presented of a new generation of scalable quantum computing architectures in which distributed quantum cores consider quantum-coherent qubit state transfer links in the data plane to interconnect, and a wireless medium orchestrator. The scientific and technology needs at each architectural layer are critically discussed, and a cross-layer design-space exploration framework is proposed to assess the feasibility of the proposed architectures.

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REFERENCES

- [1] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. Brandao, D. A. Buell, *et al.*, "Quantum supremacy using a programmable superconducting processor," *Nature*, vol. 574, no. 7779, pp. 505–510, 2019.
- [2] J. Preskill, "Quantum computing in the NISQ era and beyond," *Quantum*, vol. 2, p. 79, aug 2018.
- [3] R. B. Staszewski, I. Bashir, E. Blokhina, and D. Leipold, "Cryo-CMOS for quantum system on-chip integration: Quantum computing as the development driver," *IEEE Solid-State Circuits Magazine*, vol. 13, no. 2, pp. 46–53, 2021.
- [4] L. Vandersypen, H. Bluhm, J. Clarke, A. Dzurak, R. Ishihara, A. Morello, D. Reilly, L. Schreiber, and M. Veldhorst, "Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent," *npj Quantum Information*, vol. 3, no. 1, pp. 1–10, 2017.
- [5] J. M. Chow, "Quantum intranet," *IET Quantum Communication*, vol. 2, no. 1, pp. 26–27, 2021.
- [6] N. LaRacuente, K. N. Smith, P. Imany, K. L. Silverman, and F. T. Chong, "Short-range microwave networks to scale superconducting quantum computation," *arXiv preprint arXiv:2201.08825*, 2022.
- [7] X. Xue, B. Patra, J. P. van Dijk, N. Samkharadze, S. Subramanian, A. Corna, B. Paquelet Wuetz, C. Jeon, F. Sheikh, E. Juarez-Hernandez, *et al.*, "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, vol. 593, no. 7858, pp. 205–210, 2021.
- [8] L. Petit, H. Eenink, M. Russ, W. Lawrie, N. Hendrickx, S. Philips, J. Clarke, L. Vandersypen, and M. Veldhorst, "Universal quantum logic in hot silicon qubits," *Nature*, vol. 580, no. 7803, pp. 355–359, 2020.
- [9] E. Schriek, F. Sebastiano, and E. Charbon, "A cryo-CMOS digital cell library for quantum computing applications," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 310–313, 2020.
- [10] B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, 2018.
- [11] D. Awschalom, K. K. Berggren, H. Bernien, S. Bhave, L. D. Carr, P. Davids, S. E. Economou, D. Englund, A. Faraon, M. Fejer, *et al.*, "Development of quantum interconnects (quics) for next-generation information technologies," *PRX Quantum*, vol. 2, no. 1, p. 017002, 2021.
- [12] S. Ritter, C. Nölleke, K. Hahn, A. Reiserer, A. Neuzner, M. Uphoff, M. Mücke, E. Figueroa, J. Bochmann, and G. Rempe, "An elementary quantum network of single atoms in optical cavities," *Nature*, vol. 484, no. 7393, pp. 195–200, 2012.
- [13] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim, "Large-scale modular quantum-computer architecture with atomic memory and photonic interconnects," *Physical Review A*, vol. 89, feb 2014.
- [14] C. J. Axline, L. D. Burkhardt, W. Pfaff, M. Zhang, K. Chou, P. Campagne-Ibarcq, P. Reinhold, L. Frunzio, S. Girvin, L. Jiang, *et al.*, "On-demand quantum state transfer and entanglement between remote microwave cavity memories," *Nature Physics*, vol. 14, no. 7, pp. 705–710, 2018.
- [15] P. Giounanlis, E. Blokhina, D. Leipold, and R. B. Staszewski, "Photon enhanced interaction and entanglement in semiconductor position-based qubits," *Applied Sciences*, vol. 9, no. 21, p. 4534, 2019.
- [16] S. E. Hosseininejad, E. Alarcon, N. Komjani, S. Abadal, M. C. Lemme, P. H. Bolívar, and A. Cabellos-Aparicio, "Study of hybrid and pure plasmonic terahertz antennas based on graphene guided-wave structures," *Nano communication networks*, vol. 12, pp. 34–42, 2017.
- [17] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 996–1006, 2018.
- [18] J. P. G. Van Dijk, B. Patra, S. Subramanian, X. Xue, N. Samkharadze, A. Corna, C. Jeon, F. Sheikh, E. Juarez-Hernandez, B. P. Esparza, H. Rampurawala, B. R. Carlton, S. Ravikumar, C. Nieva, S. Kim, H.-J. Lee, A. Sammak, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen, E. Charbon, S. Pellerano, M. Babaie, and F. Sebastiano, "A scalable Cryo-CMOS controller for the wideband frequency-multiplexed control of spin qubits and transmons," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 11, pp. 2930–2946, 2020.
- [19] B. Prabowo, G. Zheng, M. Mehrpoo, B. Patra, P. Harvey-Collard, J. Dijkema, A. Sammak, G. Scappucci, E. Charbon, F. Sebastiano, *et al.*, "A 6-to-8GHz 0.17 mw/qubit cryo-CMOS receiver for multiple spin qubit readout in 40nm CMOS technology," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, pp. 212–214, IEEE, 2021.
- [20] G. Kiene, A. Catania, R. Overwater, P. Bruschi, E. Charbon, M. Babaie, and F. Sebastiano, "A 1GS/s 6-to-8b 0.5mw/qubit Cryo-CMOS SAR ADC for quantum computing in 40nm CMOS," in *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 64, pp. 214–216, 2021.
- [21] W. Kuhn, N. E. Lay, E. Grigorian, D. Nobbé, I. Kuperman, J. Jeon, K. Wong, Y. Tugunaw, and X. He, "A microtransceiver for UHF proximity links including mars surface-to-orbit applications," *Proceedings of the IEEE*, vol. 95, no. 10, pp. 2019–2044, 2007.
- [22] S. Abadal, C. Han, and J. M. Jornet, "Wave propagation and channel modeling in chip-scale wireless communications: A survey from millimeter-wave to terahertz and optics," *IEEE Access*, vol. 8, pp. 278–293, 2020.
- [23] S. Huang, B. Lienhard, G. Calusine, A. Vepsäläinen, J. Braumüller, D. K. Kim, A. J. Melville, B. M. Niedzielski, J. L. Yoder, B. Kannan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "Microwave package design for superconducting quantum processors," *PRX Quantum*, vol. 2, Apr 2021.
- [24] A. Dahlberg, M. Skrzypczyk, T. Coopmans, L. Wubben, F. Rozpundedeck, M. Pompili, A. Stolk, P. Pawelczak, R. Knegjens, J. de Oliveira Filho, R. Hanson, and S. Wehner, "A link layer protocol for quantum networks," in *Proceedings of the ACM Special Interest Group on Data Communication, SIGCOMM '19*, (New York, NY, USA), pp. 159–173, Association for Computing Machinery, 2019.
- [25] S. Abadal, A. Mestres, J. Torrellas, E. Alarcon, and A. Cabellos-Aparicio, "Medium access control in wireless network-on-chip: A context analysis," *IEEE Communications Magazine*, vol. 56, no. 6, pp. 172–178, 2018.
- [26] N. Mansoor, P. J. S. Iruthayaraj, and A. Ganguly, "Design methodology for a robust and energy-efficient millimeter-wave wireless network-on-chip," *IEEE Transactions on Multi-Scale Computing Systems*, vol. 1, no. 1, pp. 33–45, 2015.
- [27] C. G. Almudever, L. Lao, R. Wille, and G. G. Guerreschi, "Realizing quantum algorithms on real quantum computing devices," in *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 864–872, IEEE, 2020.
- [28] L. Lao, H. Van Someren, I. Ashraf, and C. G. Almudever, "Timing and resource-aware mapping of quantum circuits to superconducting processors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 2, pp. 359–371, 2021.
- [29] P. Murali, N. M. Linke, M. Martonosi, A. J. Abhari, N. H. Nguyen, and C. H. Alderete, "Full-stack, real-system quantum computer studies: Architectural comparisons and design insights," in *2019 ACM/IEEE 46th Annual International Symposium on Computer Architecture (ISCA)*, pp. 527–540, IEEE, 2019.
- [30] J. M. Baker, C. Duckering, A. Hoover, and F. T. Chong, "Time-sliced quantum circuit partitioning for modular architectures," in *Proceedings of the 17th ACM International Conference on Computing Frontiers*, pp. 98–107, 2020.
- [31] S. Rodrigo, S. Abadal, E. Alarcón, M. Bandic, H. Van Someren, and C. G. Almudéver, "On double full-stack communication-enabled architectures for multicore quantum computers," *IEEE micro*, vol. 41, no. 5, pp. 48–56, 2021.
- [32] K. R. Brown, J. Kim, and C. Monroe, "Co-designing a scalable quantum computer with trapped atomic ions," *npj Quantum Information*, vol. 2, no. 1, pp. 1–10, 2016.
- [33] A. Wack, H. Paik, A. Javadi-Abhari, P. Jurcevic, I. Faro, J. M. Gambetta, and B. R. Johnson, "Quality, speed, and scale: three key attributes to measure the performance of near-term quantum computers," *arXiv preprint arXiv:2110.14108*, 2021.
- [34] R. Blume-Kohout and K. C. Young, "A volumetric framework for quantum computer benchmarks," *Quantum*, vol. 4, p. 362, 2020.
- [35] D. Mills, S. Sivarajah, T. L. Scholten, and R. Duncan, "Application-motivated, holistic benchmarking of a full quantum computing stack," *Quantum*, vol. 5, p. 415, 2021.
- [36] C. G. Almudever and E. Alarcon, "Structured optimized architecting of full-stack quantum systems in the nlsq era," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 762–767, IEEE, 2021.
- [37] T. Tomesh and M. Martonosi, "Quantum codesign," *IEEE Micro*, vol. 41, no. 5, pp. 33–40, 2021.