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Electric Vehicle Traction Drive using Si/SiC Hybrid Switches

MSc. Thesis Report

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TU Delft

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by

C. Tan

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C. Tan
Delft, August 2020

Contents

Abstract

The parallel connection of a Silicon (Si)-based IGBT and a Silicon Carbide (SiC)-based MOSFET forming a so called hybrid switch can be used to capitalize on the advantageous features of both semiconductor and materials technologies. In this thesis, a hybrid switch-based inverter designed for the application of Electric Vehicle (EV) traction drive is compared to the conventional inverter assembled with Si-based IGBTs, and SiC-based MOSFETs. According to different standardized driving cycles, Electric Vehicles operate in low partial load for a considerable amount of the time. Therefore, in this application, semiconductor conduction losses can be considerably reduced when unipolar switches such as MOSFETs are used. Collectively, this work shows that the hybrid switch configuration constitutes a good compromise between efficiency and cost when compared to a solution implementing only Si-based IGBT or solely SiC-based MOSFETs.

1 Introduction

1.1. Background

As the world moves towards a more sustainable future, the automotive industry aims to reduce its share of CO_2 emissions. Development of Electric Vehicles (EV) has become prominent as they produce substantially lower CO_2 emissions than internal combustion engine vehicles [1]. One of the research and development goals in this field is the improvement of the EV traction drive efficiency and the consequent extension of driving range. The traction drive, which converts electrical energy from the battery to mechanical energy in the wheels, consists of a DC-AC inverter and an electric motor, as shown in Figure 1.1. The inverter is a major contributor to the power loss of the traction drive [1, 2].

1.2. Switches for EV Drive Inverter

Currently, the majority of the commercial EV inverters consist of Silicon (Si)-based IGBTs, which are known for robustness, relatively low cost, and good current conduction performance at high currents. There are, however, several drawbacks of using Si IGBTs in the application of EV drives. Due to the bipolar junction characteristic, IGBTs have unsatisfactory performance at low current conditions. Additionally, in high voltage class devices, the current tail observed during an IGBT's turn-off may result in high switching losses [3]. In fact, standardized driving cycles demonstrate that consumer EVs operate at low partial load during the majority of its use [2], and in these operating conditions IGBT-based inverters perform poorly. This calls for a better suited semiconductor than the Si-based IGBTs.

Another candidate for the inverter switch is the Silicon Carbide (SiC) MOSFET. In recent years, it has gained popularity due to its excellent switching performance, easy paralleling feature which enables higher power handling, and above all, the higher temperature capability of the SiC material [3, 4]. The thinner n-doped region of SiC MOSFETs enables wider voltage ranges compared to the Si-based MOSFETs and have lower conduction and switching losses [3]. In particular, high power SiC MOSFETs show outstanding efficiency at low current, which makes them highly suitable for application in an EV

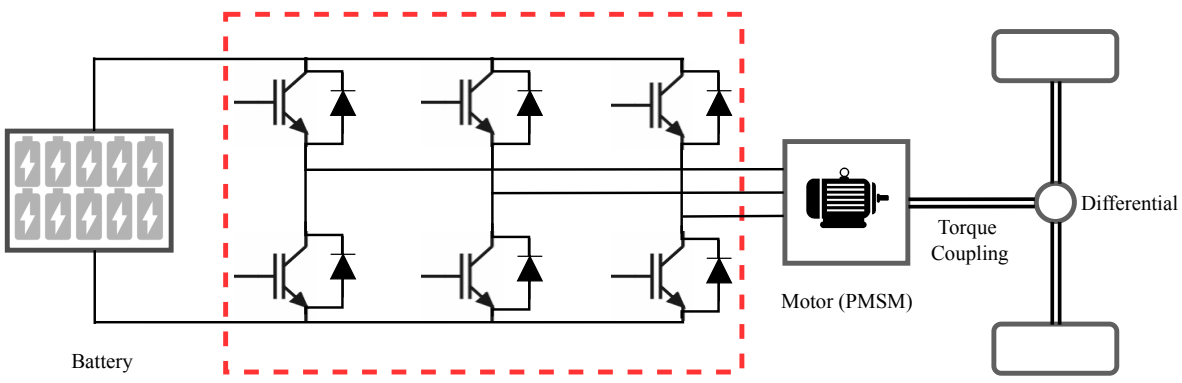


Figure 1.1: Electric vehicle motor drive system with Si-based IGBT inverter.

traction system from an efficiency standpoint [5, 6]. The major drawback of the SiC MOSFET is its higher manufacturing cost and lower reliability in comparison to the traditional IGBT-based inverters [5, 6].

The significantly higher cost of the SiC MOSFET calls for a compromised solution. In recent years, the Si IGBT and SiC MOSFET paralleled hybrid switch (cf. Figure 1.2) has shown promising results. In this thesis, this hybrid switch is examined for its performance as the switch for EV traction inverter.

1.3. Thesis Objective

The main research objective of this thesis is:

To analytically model, experimentally characterize, and optimize the hybrid Si-SiC switch, and to investigate and benchmark its use in EVs traction inverters vs traditional configurations.

The main challenges in reaching the objective are:

- Derive close form equations that accurately model the current sharing between parallel devices of different technologies;
- Optimize the switching performances of hybrid switch and find an optimal switching strategy;
- Benchmark the application of hybrid switches in EV traction inverters vs traditional configuration while performing standardized driving profiles.

1.4. Thesis Outline

The thesis report is structured into seven main chapters. The first chapter introduces the hybrid switch and the objectives of the project. In chapter 2, current literature on the hybrid switch is discussed. The analytical model and equations of the hybrid switch are discussed in chapter 3. Using the analytical equations, characteristics of the hybrid switch are investigated using selected semiconductors and its manufacture datasheet in chapter 4. In chapter 5, these characteristics are then determined experimentally. In chapter 6, the designed hybrid switch in a Electric Vehicle traction drive is evaluated using different driving profiles. The conclusion of the thesis and suggestions for future research are given in chapter 7.

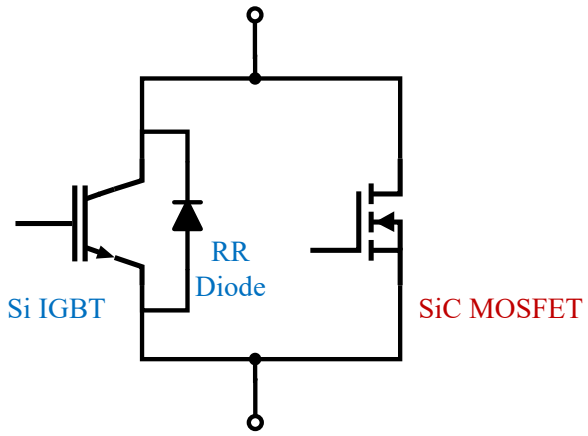


Figure 1.2: Si IGBT and SiC MOSFET paralleled hybrid switch.

2

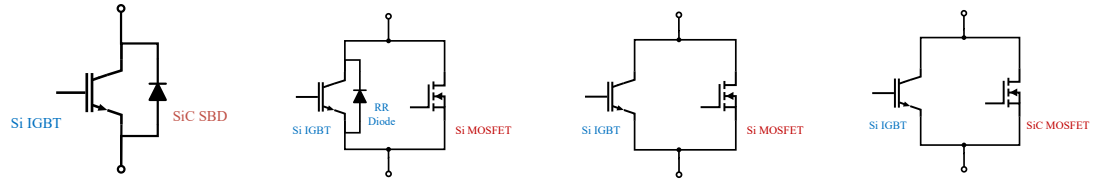
Literature Review On Si/SiC Hybrid Switch

2.1. Hybrid Switch Configurations

In power conversion circuits, IGBTs and MOSFETs are popular due to their controllability. However, due to the inherent weakness of each option separately, a better compromise between cost and efficiency is needed for the EVs' traction inverters. To overcome the shortcomings of either device, hybrid switches assembled paralleling different semiconductor technologies (e.g. Si and SiC) are introduced. The configurations can be seen in Figure 2.1.

One of the possible configurations is by paralleling a Si IGBT with a SiC Schottky Barrier Diode (SBD) shown in Figure 2.1 a). With SiC SBD, the IGBT switch is able to achieve lower reverse recovery and turn-on losses compared to the more common IGBT coupled with Si fast-recovery diode [7, 8]. It has been shown that Si IGBT with SiC SBD can decrease the total switching losses by 40% and increase the converter frequency capabilities by two folds compared to its full Si IGBT counterparts [7]. Furthermore, IGBT with SiC SBD hybrid has shown to be advantageous for traction inverter system with reduced weight and lower total energy loss [9].

Another configuration is paralleling Si IGBT and Si MOSFET [10] seen in Figure 2.1 (b) and (c). Configuration (b) is implemented with a reverse conduction diode and uses the Si MOSFET for soft switching for the IGBT in bridge type converters [10]. Configuration (c) uses the MOSFET for reverse conduction to reduce conduction losses [11]. By paralleling the MOSFET and IGBT, the advantage of both devices are utilized. The hybrid switch performs better than IGBT at lower current and better than the MOSFET at high current. This will be discussed further in the following section. Furthermore, due to the fast switching of the MOSFET, the hybrid switch is also able to reduce switching losses by providing Zero Voltage Switching (ZVS) for the IGBT [10, 12]. Examples of the Si MOSFET and Si IGBT hybrid has shown promising results in reducing losses in a solid state transformer and in traction motor inverter applications [10, 12]. One shortcoming of the Si MOSFET is its limited blocking voltage capability. As an unipolar power device with a thick and lightly doped n-base region, the Si MOSFET has an upper voltage limit of 1200V [6, 13] which makes it unsuitable for high power applications. With



(a) Si IGBT Hybrid with SiC SBD

(b) Si IGBT Hybrid and diode with Si MOSFET

(c) Si IGBT Hybrid with Si MOSFET

(d) Si IGBT Hybrid with SiC MOSFET

Figure 2.1: Different configurations of the Hybrid switch.

the Wide Band Gap (WBG), SiC MOSFETs can provide a wider voltage range desired in high voltage applications [6, 13]. In recent years, hybrid switch paralleling Si IGBT with SiC MOSFET (Figure 2.1 d)) has became a popular configuration [6]. Similar to Si IGBT and Si MOSFET, this hybrid configuration takes the advantages of both IGBT and MOSFET. As most of the electric vehicles do not constantly operate in full load conditions, this hybrid switch would increase efficiency over the entire load profile.

2.2. On-state Characteristics

The Si IGBT and SiC MOSFET hybrid takes advantage of the IGBT's low on-state resistance and the low switching losses of the MOSFET. The on-state characteristics of a 1200V class Si IGBT, a SiC MOSFET and the Hybrid switch with equivalent current ratings are shown in Figure 2.2 (from [6]). On the left, the on-state characteristics are compared showing the entire current range while the characteristics at low current are highlighted on the right. At low current, the MOSFET conducts most of the current as it does not have PN junction barrier potential [12]. However, at high current, the IGBT conducts a greater proportion of the total current because this device has typically lower on-state resistance. The output characteristics have shown that the hybrid switch has low conduction loss at both low current due to the MOSFET and high current due to the IGBT. Due to the intrinsic positive temperature coefficient of the used semiconductor devices, their on-state characteristic is strongly influenced by their junction temperatures [14]. The variation of the on-state characteristics of IGBT and MOSFET can be seen in Figure 2.3. As temperature increases, the on-state performance deteriorates because the equivalent on-state resistance increases. This relationship can be described by Equation (2.1), where $R_{\mathrm{on,ref}}$ is the reference on-state resistance (usually at 25°C), C_{T} is the temperature coefficient, and T_{j} and T_{ref} are the junction temperature and reference junction temperature corresponding to the $R_{\mathrm{on,ref}}$.

$$R_{\mathrm{on}}(T_{\mathrm{j}}) = R_{\mathrm{on,ref}} \cdot [1 + C_{\mathrm{T}} \cdot (T_{\mathrm{j}} - T_{\mathrm{ref}})] \tag{2.1}$$

The temperature coefficient C_{T} is positive because as temperature increases, the charge carriers undergo more collisions per unit time in the semiconductor lattice [14]. This results in lower carrier mobility which is inversely proportional to the on-state resistance. For the IGBT, the PN junction barrier voltage decreases as temperature increases (see Figure 2.3 (b)) because the intrinsic concentration, which is inversely proportional to this potential, increases with temperature [14].

2.2.1. Current Sharing

Sharing of current between the IGBT and MOSFET components in the hybrid switch (Figure 1.2) changes depending on the total load current and temperature [17]. At low current, the load current only flows through the MOSFET because IGBT does not conduct until its PN junction barrier voltage is reached. When the junction barrier voltage is reached, the IGBT starts to share the load current with

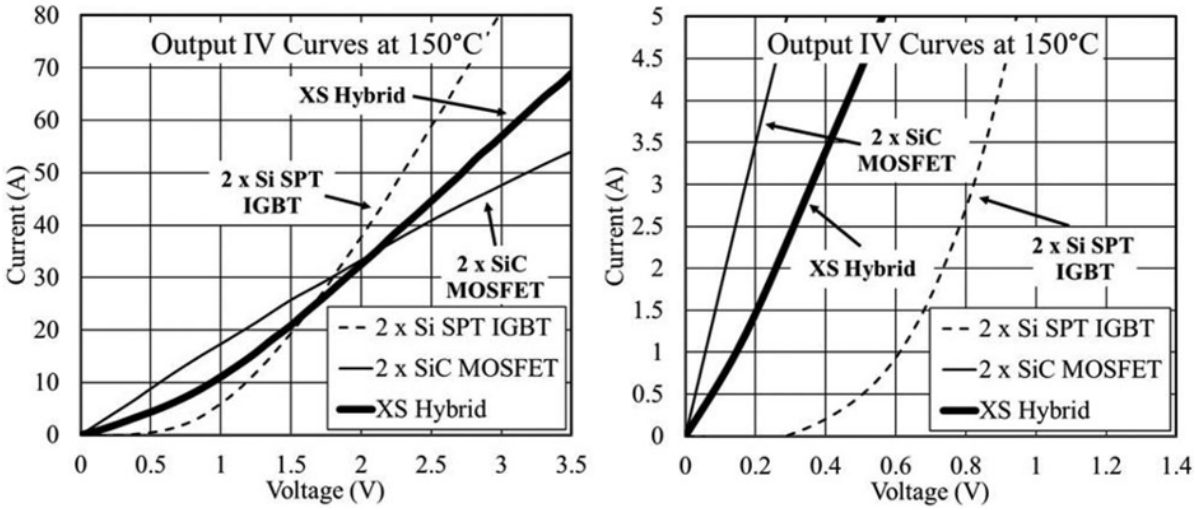
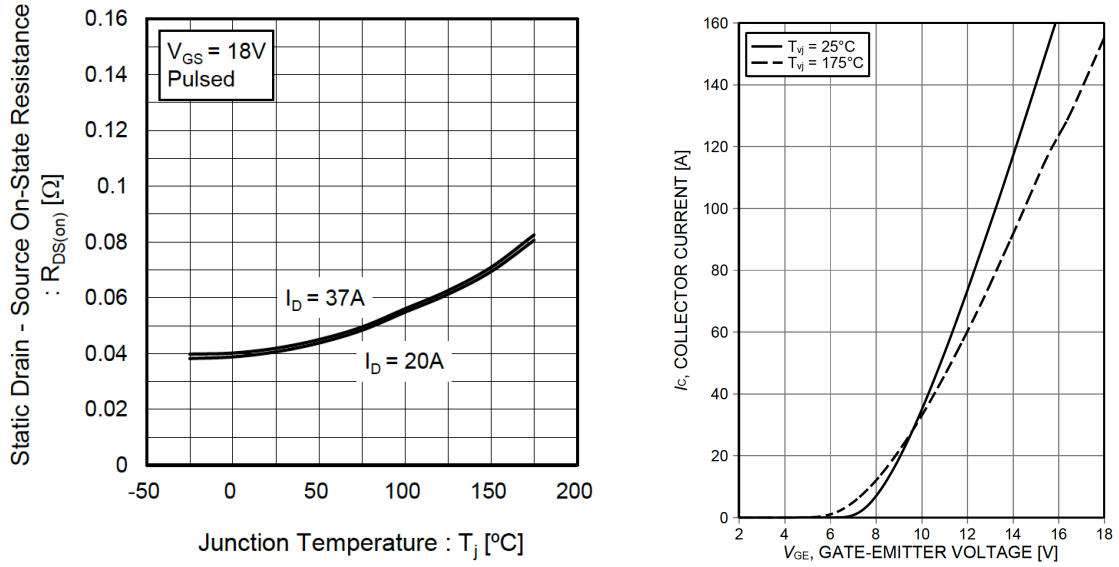


Figure 2.2: The on-state characteristics of the hybrid switch compared to pure Si IGBT and SiC MOSFET switches [6].



(a) (b)

Figure 2.3: Temperature's effect on the on-state characteristics of IGBT and MOSFET. (a) the on-state resistance as a function of temperature of a 1200V SiC MOSFET[15], (b) the IV curve a 1200V Si IGBT [16].

the MOSFET. As the current increases, more current flows through the IGBT because it typically has a lower on-state resistance at higher current.

2.3. Switching Characteristics

The switching characteristics of the hybrid switch are another major contributor to losses. Unlike the on-state characteristics, switching characteristics do not heavily depend on temperature as they are mostly determined by the gate resistance and the parasitic capacitances of the switch [14]. Optimizing the switching strategy of hybrid switches, losses can be further reduced.

2.3.1. Turn-on

The turn-on characteristics of the hybrid switch are dependent on the switching strategy in which the turn-on delay is varied between the IGBT and the MOSFET. However, the waveform is similar to that of the MOSFET and IGBT [6]. The MOSFET's turn-on waveform is shown in Figure 2.4. The turn-on waveform can be broken down into 5 stages [14]:

1. $t_{d,on}$: the gate voltage v_{gs} rise to the threshold voltage $V_{GS(th)}$.
2. t_{ri}: as the v_{gs} passes $V_{GS(th)}$, the drain current i_D starts to increase.
3. t_{rr}: with the presence of the freewheeling diode, i_D increases past the designed output current I_o. i_D decreases back to I_o after all the reverse recover charge in the diode is depleted.
4. t_{fv1}: the drain-source voltage v_{DS} decreases at the rate corresponding to the gate-drain capacitance during the active region.
5. t_{fv2}: the drain-source voltage v_{DS} decreases at the rate corresponds to the gate-drain capacitance during ohmic region. Eventually, the switch is fully turned on and the v_{DS} stays at the on-state voltage.

Furthermore, the non-ideal behavior of the switch and test setup result from the parasitic components (Figure 2.5) and will affect the switching waveform [18, 19]. This can be seen in Figure 2.7. The parasitic components include:

- The drain-source capacitance C_{ds} contributes to the total output capacitance C_{oss} of the switch. As the switch turns on, the output capacitance discharges, making the channel current larger than the drain current. This results in higher turn-on losses.

- The diode junction capacitance C_j charges during turn-on. This would add to the channel current during turn-off from the load current.

- The parasitic inductance L_{DS} in the circuit would result in a voltage dip in v_{gs} as the current increases. Furthermore, it would slow the speed of the current transition (seen in Figure 2.6). As previously mentioned, this would affect hybrid switching current sharing as well.

These non-ideal behavior will be observed further in experimental testing outlined in chapter chapter 5.

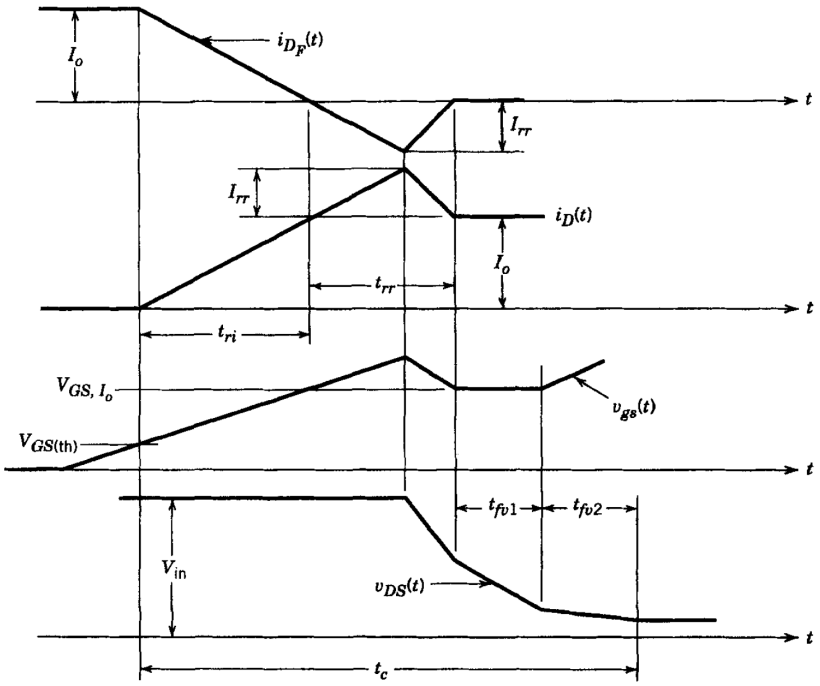


Figure 2.4: MOSFET Turn On waveform [14].

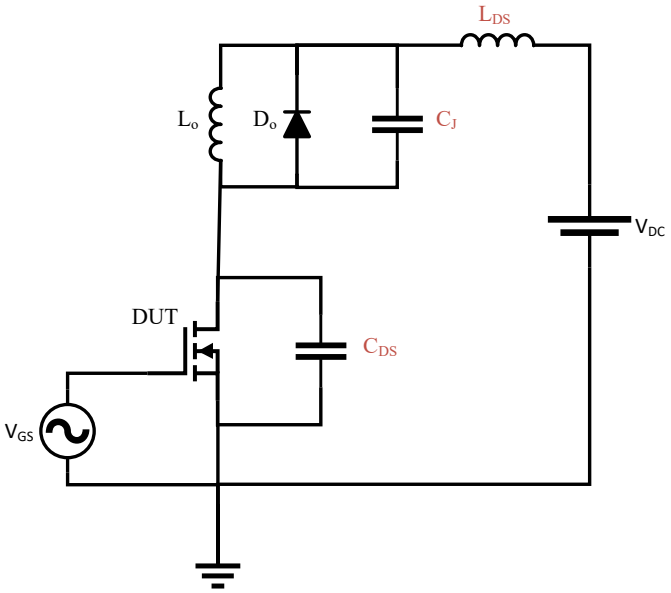


Figure 2.5: Parasitic components in MOSFET test circuit.

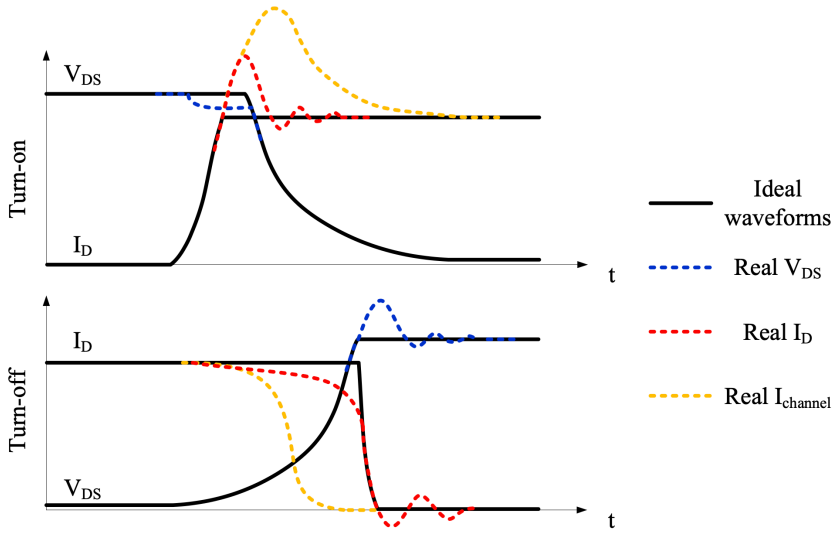


Figure 2.6: MOSFET switching waveform with effect of parasitic components [18].

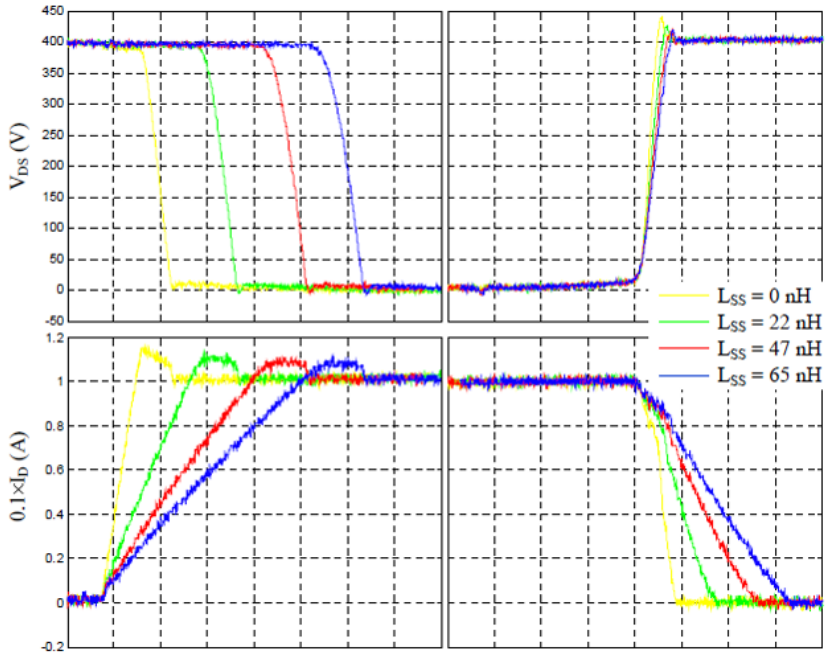


Figure 2.7: Effect of common source parasitic inductance on MOSFET switching waveform [18].

Turn-on Strategies

Different switching strategies for turn-on are compared in Table. 2.1. Since the SiC MOSFET switches faster than the IGBT switches, they have considerably lower turn-on losses [17]. For turn-on, IGBT Zero Voltage Switching (ZVS) can be achieved by turning on the MOSFET before the IGBT (option 2 in Table 2.1). However, it is shown in some studies that better performances can be achieved using 0 delay for turn-on when considering commercial 1200V MOSFET and IGBT [20, 21]. This is due to the fact that turn-on loss is dominated by the diode reverse recovery loss. With the IGBT turned on simultaneously with the MOSFET, both devices provide channels for the diode's current commutation. This shortens the turn-on time and reduces loss. Hence, option 2 in Table 2.1 would be unnecessary. Contrasting, when parasitic inductance is high, the current from the MOSFET to the IGBT commutates slower [17]. This is especially true when paralleling multiple discrete devices. If the MOSFET is turned on first, it would experience higher stress as the current is slowly commutated to the IGBT. Turning on

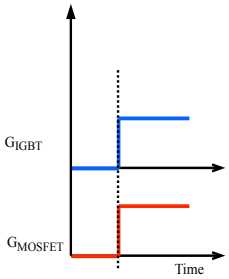
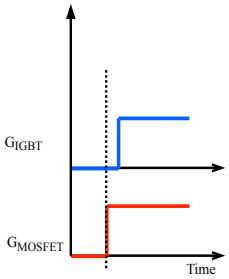
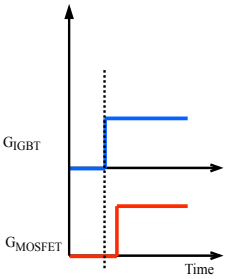
Switching Pattern	 Option 1	 Option 2	 Option 3
Option	Both Turn ON simultaneously	MOSFET Turn ON first	IGBT Turn ON first
Advantages	Lower switching losses (ZVS for IGBT)	Lower switching losses (ZVS for IGBT)	Reduce MOSFET stress
Disadvantages	High stress on MOSFET	High stress on MOSFET and higher conduction losses	Not ZVS, higher switching losses
Practical Issues	n/a	Parasitic interconnect inductance imbalance cause higher stress on MOSFET	n/a

Table 2.1: Turn-on strategies.

the IGBT first is only ideal when parasitic inductance is high, as it is more robust to high current stress. The effect on turn-on losses due to the switching delay between MOSFET and IGBT can be seen in Figure 2.8.

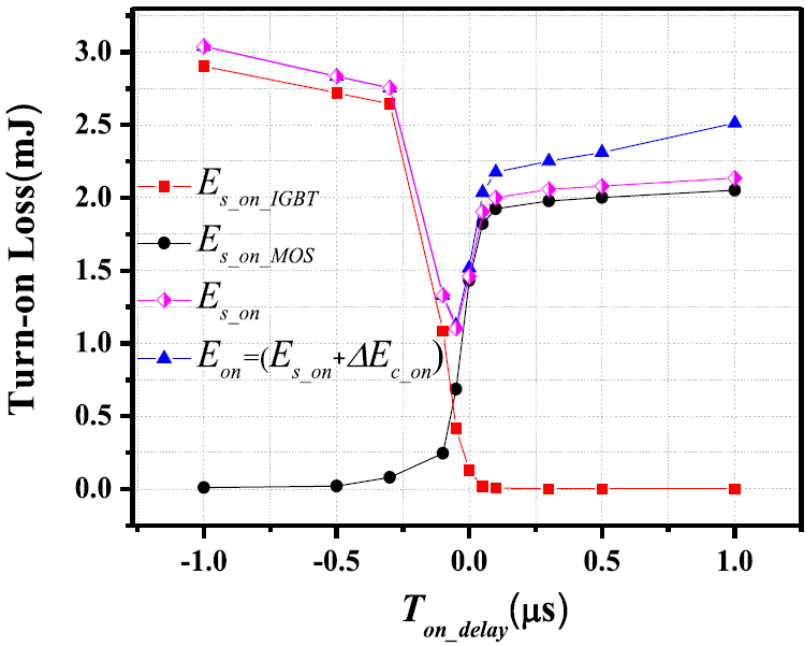


Figure 2.8: Turn-on Losses as a function of delay between turning on SiC MOSFET and Si IGBT [20].

2.3.2. Turn-off

Turn-off for the MOSFET is the opposite of the turn-on operation and can be seen in Figure 2.9. The IGBT turn-off has similar stages, albeit with a longer current tail (Figure 2.10). The IGBT turn-off stages

can be described as:

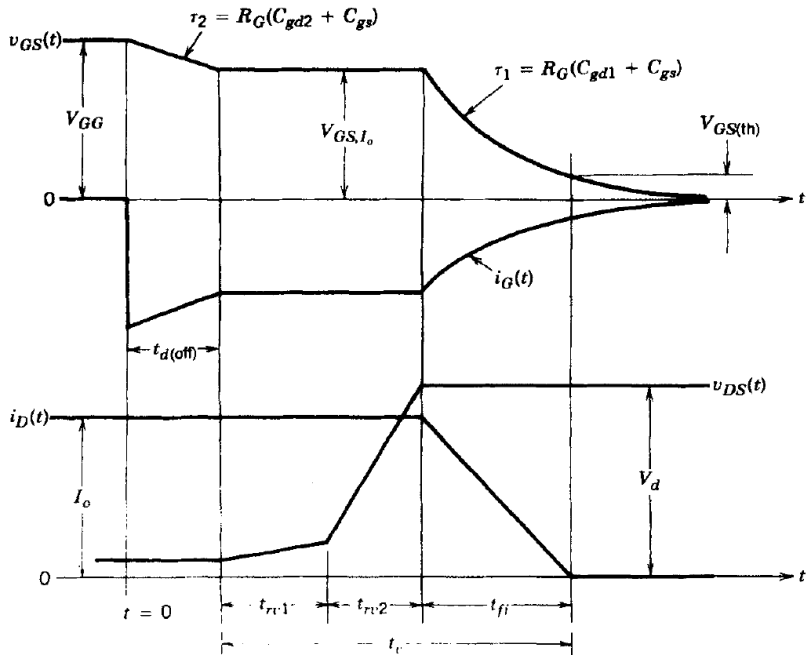


Figure 2.9: MOSFET Turn Off waveform [14].

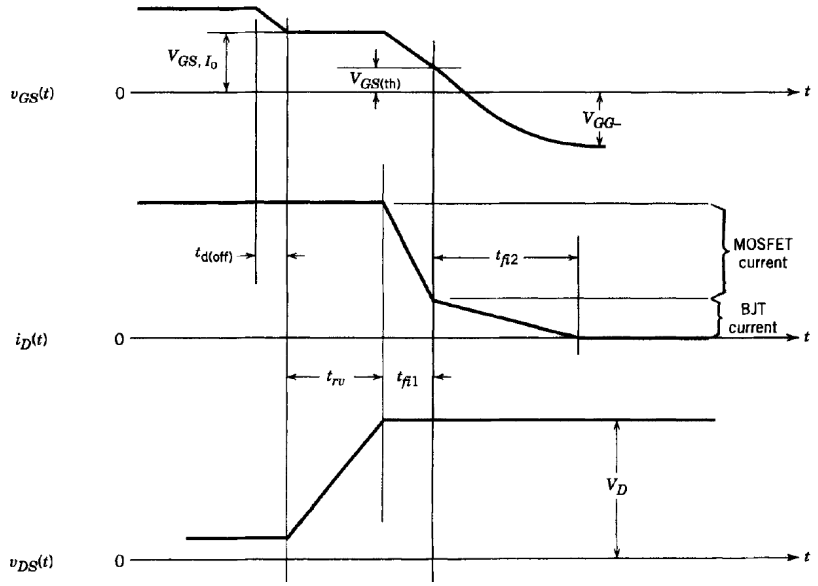


Figure 2.10: IGBT Turn Off waveform.[14]

1. $t_{d,off}$: the gate voltage v_{gs} falls to the voltage $V_{GS,Io}$.
2. t_{rv}: the drain-source voltage v_{DS} rises to V_D.
3. t_{fi1}: the drain current i_D decreases at the rate corresponding to the MOSFET until gate voltage reaches threshold $V_{GS(th)}$.
4. t_{fi2}: the MOSFET equivalent part of the IGBT is turned off, the drain current i_D decreases at a slower rate as the stored charge is removed only by recombination. The duration of this period increases with temperature and can resulting in high switching losses.

The higher turn-off losses is a trade off with on-state losses. The IGBT is designed so that the excess-carrier lifetime in n- region is large, which results in a lower on-state voltage. This would also mean that greater time is required to remove the charges after the gate voltage becomes lower than the threshold voltage. As temperature increases, the time to remove the charges would further increase, result in higher turn-off loss.

As noted, the non-ideal behavior of the switch and test setup results from the parasitic components (Figure 2.5) affects the turn-off waveforms as well as shown in Figure 2.7. For turn off:

- The drain-source capacitance C_{ds} contributes to the total output capacitance C_{oss} of the switch. As the switch turns off, the output capacitance charges, making the channel current smaller than the drain current. This results in lower turn-off losses. During turn-off, C_{ds} also contributes to voltage overshoot and parasitic ringing due to the resonance between C_{ds} and L_{DS}.

- The diode junction capacitance C_j discharges during turn-on. This would subtract the channel current from the load current during turn-off.

- In addition to the overshoot voltage and ringing, the parasitic inductance L_{DS} slows down the speed of the current transition. As previously mentioned, this would affect the hybrid switching with current sharing as well.

Turn-off Strategies

Different switching strategies for turn-off are compared in Table 2.2. SiC MOSFET has a low voltage drop and can provide ZVS for the IGBT if the MOSFET is switched off after the IGBT. This can reduce the effects of the current tail during normal IGBT turn-off. However, a prolonged turn-off delay between the IGBT and MOSFET would result in increment of losses (due to the increase in MOSFET conduction loss) and possibly a lowering on the maximum acceptable switching frequency [22, 23]. When switching off the IGBT first, the IGBT v_{GE} exhibits oscillation due to miller capacitance charged by the high dv/dt [17]. This would cause fault triggering, turning on IGBT for a short time after its turn off. As a result, it would cause more switching losses and potentially short circuit if it goes beyond the designed dead time between the upper and lower switch. Miller clamping can be used to avoid this phenomenon and was demonstrated in [17, 24]. The effect on turn-on losses due to the switching delay between MOSFET and IGBT can be seen in Figure 2.8.

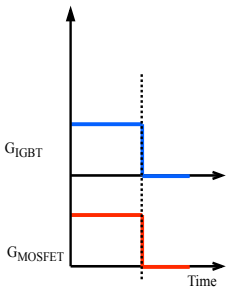
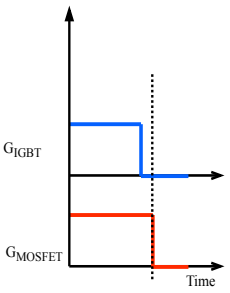
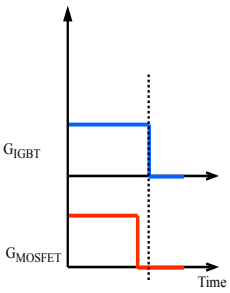
Switching Pattern	 Option 1	 Option 2	 Option 3
Option	Both Turn OFF simultaneously	IGBT Turn OFF first	MOSFET Turn OFF first
Advantages	Common gate driver	Lower switching losses (ZVS for IGBT)	Reduce miller affect
Disadvantages	Not ZVS, higher switching losses	Lower switching frequency required	Not ZVS, higher switching losses
Practical Issues	n/a	Miller Capacitance causes false IGBT turn on	n/a

Table 2.2: Turn-off strategies.

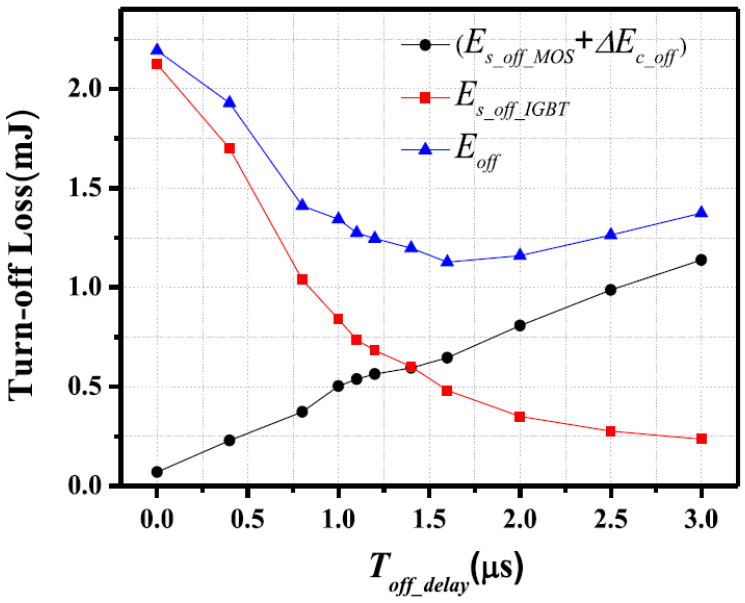


Figure 2.11: Turn-off Losses as a function of delay between turning on SiC MOSFET and Si IGBT [20].

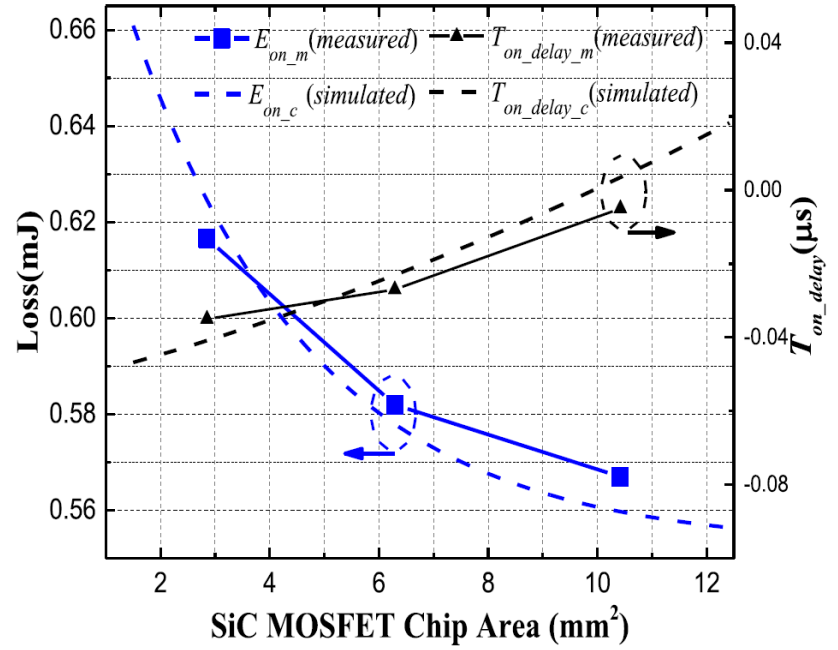
In the course of this document, the on-state and switching characteristics of the hybrid switches, the pure Si IGBT and the pure SiC MOSFET counterparts are evaluated theoretically using datasheets and experimentally using a double pulse test. The theoretical evaluation is shown in chapter 4 and the experimental evaluation is explained in chapter 5.

2.3.3. Current ratio and Chip Area of SiC MOSFET

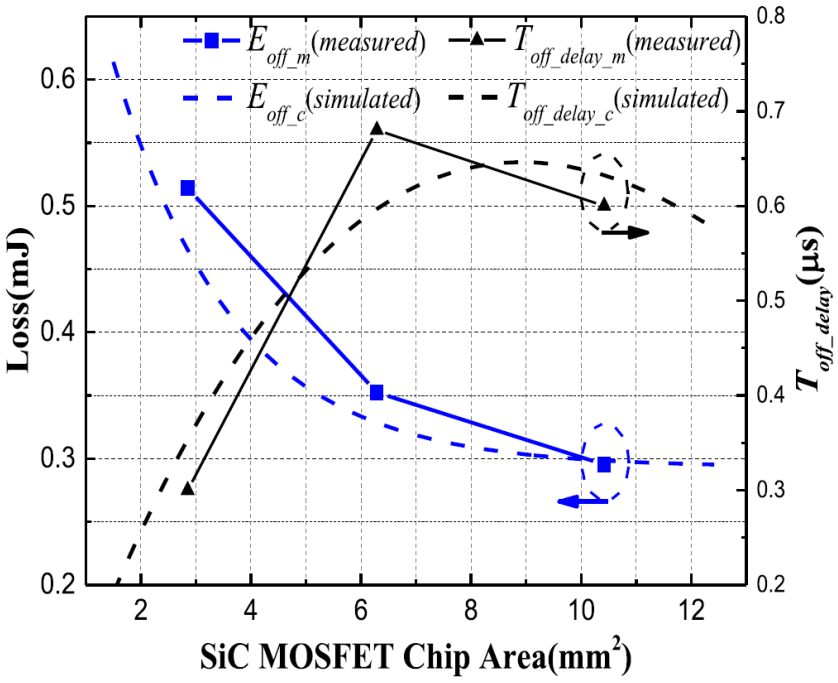
The current ratio between SiC MOSFET and Si IGBT can vary based on the switching strategy, total rated current, cost and junction temperature [17, 25]. With lower current ratio, a smaller SiC MOSFET chip area is used, thus reducing the cost of the switch. However, this means higher thermal stress and higher losses. It is possible for the hybrid switch to achieve 1:6 current ratio with optimal switching strategy and an active cooling system to ensure the switch stays below the maximum junction temperature [17]. The optimal switching strategy requires the SiC MOSFET to turn on before and turn off after the Si IGBT. This results in higher thermal stress with the trade off of lower switching losses. The turn-on and turn-off losses based on chip area with different delays can be seen in Figure 2.12. To ensure the safety of the switch, the current ratio between SiC MOSFET and Si IGBT is selected to be 1:1 in this thesis.

2.4. Hybrid Switch Applications

Si/SiC Hybrid switch has been investigated heavily in recent years, especially in a single switch or module form. Many recent studies also integrated the hybrid switch into converters such as hard-switching DC-DC converters, resonant converters and three-phase converters. Some examples are listed in Table 2.3.



(a) Turn-on Losses



(b) Turn-off losses

Figure 2.12: Turn-on and turn-off Losses and delay time as a function of SiC MOSFET chip area [25].

Ref	Application	Year	Topology	Switches (per phase)	Result
[26]	Wireless charging (AC/DC system)	2016	Rectifier with resonant gate drive	4xSiC MOSFET + 4xSi IGBT	Designed for a 22kW system. Preliminary experimental result shows hard switching efficiency of 98% at 5kW
[22]	Power module for 3 Phase voltage source inverter	2018	Half bridge	4xSi IGBT + 2xSiC MOSFET	- Switching strategy based on loss/MOSFET temperature rise index - The inverter base plate temperature was 67C at rated output power of 30kW at 30kHz.
[27]	General power conversion	2018	Three-level Active Neutral-Point-Clamped	4x Si IGBT Discrete + 2x SiC MOSFET	- Thermal balanced control switching strategy - The 650V converter is 50% cheaper than a full SiC solution and has 0.5-1.0 % efficiency increase compared to its full IGBT counterpart.
[28]	High speed drives	2018	T-type power electronic block	2x Si IGBT Discrete + 2x SiC MOSFET Discrete 2x Si IGBT module + 2x SiC MOSFET module	- The PEBB operates at 28kHz and has an apparent output power of 17.5kVA. - It achieves a specific power density of 27.7kW/kg and volumetric power density of 308.6 W/in3.
[17]	To evaluate Electromagnetic interference of hybrid switch	2019	DC-DC Boost	1xSiC MOSFET + 1xSi IGBT	- The fast switching of SiC MOSFET induces much higher EMI compared to its IGBT counterparts. - Extra CM capacitance and current paths to heatsink/ground also contribute to EMI.

Table 2.3: Hybrid switch applications in current literature

2.5. Current Research and Knowledge Gap

Many studies have already demonstrated that hybrid switches are a great compromise between efficiency and cost. Hybrid switches are significantly cheaper than full SiC MOSFET solutions [17, 29]. Furthermore, hybrid switch converters have demonstrated promising results in diverse applications. However, the application of Si/SiC Hybrid switch in EV traction drives has not yet been investigated. In addition, there has yet to be any comprehensive analyses on the Hybrid Switch inverter. In this thesis, a hybrid switch is designed and characterized for the Nissan Leaf 2011 EV traction drive. Using these characteristics, the hybrid switch based inverter is simulated through standardized EV driving cycles to demonstrate its advantages over the pure IGBT and the pure MOSFET solutions.

3

Analytical Equations for Inverter Switch

Developing close form equations to predict hybrid switches losses and current sharing between its components could be of great help for future researchers. In fact, these equations can substitute, with fair accuracy, complex and computationally demanding circuit simulations. This section explains the process to determine the current sharing and losses of the two-level voltage source inverter analytically.

3.1. Pure Switch Two Level Inverter

This chapter presents the derivation of analytical equation for the prediction of EV traction inverter accuracy. The assumption behind the derivation of the following equations are:

- the switching frequency f_s is much greater than the fundamental motor frequency;
- the EV is assumed to also implement a sinusoidal carrier based Pulse-Width-Modulation (PWM).
- the dead time between the upper and lower switch is negligible with respect to the switching period.

According to these assumptions it can be assumed that during a switching period the sinusoidal current can be considered constant.

3.1.1. Pure Switch Inverter Switching Losses

The switching loss of each switch is calculated using the switching energy $E_{\mathrm{on,off,rr}}$ provided by the manufacturer's datasheet or experimentally determined from a double pulse test (described in chapter 5). The switching loss is linearly scaled according to the applied switched voltage $V_{\mathrm{dc,sw}}$ and reference voltage V_{b}, which was used in the datasheet or experimental measurements:

$$P_{\mathrm{sw}} = \frac{f_{\mathrm{s}} V_{\mathrm{dc,sw}}}{2\pi V_{\mathrm{b}}} \int_0^{2\pi} E_{\mathrm{on,off,rr}}(I)\mathrm{d}\theta. \tag{3.1}$$

The switching losses dependence from the load current, $E_{\mathrm{on,off,rr}}(I)$, can be quadratically approximated, then Equation (3.1) is rewritten as:

$$P_{\mathrm{sw}} = \frac{f_s V_{\mathrm{dc,sw}}}{2\pi V_{\mathrm{b}}} \left[\frac{\pi b_2}{2} \hat{I}_{\mathrm{ac}}(\theta)^2 + 2 b_1 \hat{I}_{\mathrm{ac}}(\theta) + \pi b_0 \right] \tag{3.2}$$

where $\hat{I}_{\mathrm{ac}}$ is the peak AC sinusoidal load current and [b0, b1, b2] are the quadratic coefficients modeling the switching energies.

3.1.2. Pure Si IGBT Inverter Conduction Losses

For the full Si IGBT solution the conduction loss is calculated using the on-state resistance, R_{ce}, and the PN junction potential, V_{ce}, with the RMS, I_{rms}, and average current, I_{avg}, flowing through the device:

$$P_{\mathrm{cond,IGBT}} = V_{\mathrm{ce}} \cdot I_{\mathrm{avg}} + R_{\mathrm{ce}} \cdot I_{\mathrm{rms}}^2 \tag{3.3}$$

I_{rms} and I_{avg} flowing through the IGBT and diode of the full Si IGBT solution are calculated using the Equations (3.4)-(3.7), where m is the modulation index and ϕ is the phase shift between voltage and current at fundamental frequency.

$$I_{\mathrm{avg,T}_{1,2}} = \frac{\hat{I}_{\mathrm{ac}}}{8\pi}\left(m\pi\cos\phi + 4\right) \tag{3.4}$$

$$I_{\mathrm{avg,D}_{1,2}} = \frac{\hat{I}_{\mathrm{ac}}}{8\pi}\left(4 - m\pi\cos\phi\right) \tag{3.5}$$

$$I_{\mathrm{rms,T}_{1,2}} = \frac{\hat{I}_{\mathrm{ac}}}{2}\sqrt{\frac{8m\cos\phi + 3\pi}{6\pi}} \tag{3.6}$$

$$I_{\mathrm{rms,D}_{1,2}} = \frac{\hat{I}_{\mathrm{ac}}}{2}\sqrt{\frac{3\pi - 8m\cos\phi}{6\pi}} \tag{3.7}$$

As temperature increases, the conduction loss increases due the temperature dependency of R_{ce} and V_{ce}. This relationship can be observed in Equations (3.8) and (3.9), where $r_{\mathrm{ce,ref}}$ and $V_{\mathrm{ce,ref}}$ are the reference on-state resistance and PN junction potential at reference temperature $T_{\mathrm{ref,IGBT}}$.

$$R_{\mathrm{ce}}(T_{\mathrm{j}}) = R_{\mathrm{ce,ref}} \cdot [1 + C_{\mathrm{T,IGBT}} \cdot (T_{\mathrm{j,IGBT}} - T_{\mathrm{ref,IGBT}})] \tag{3.8}$$

$$V_{\mathrm{ce}}(T_{\mathrm{j}}) = V_{\mathrm{ce,ref}} \cdot [1 + C_{\mathrm{T,IGBT}} \cdot (T_{\mathrm{j,IGBT}} - T_{\mathrm{ref,IGBT}})] \tag{3.9}$$

3.1.3. Pure SiC MOSFET Inverter Conduction Losses

The conduction losses of the full SiC MOSFET solution are predicted as:

$$P_{\mathrm{cond,MOS}} = R_{\mathrm{dson}} \cdot I_{\mathrm{rms}}^2 \tag{3.10}$$

where R_{dson} is the on-state resistance of the MOSFET and the RMS current flowing through it, I_{rms}, is defined as:

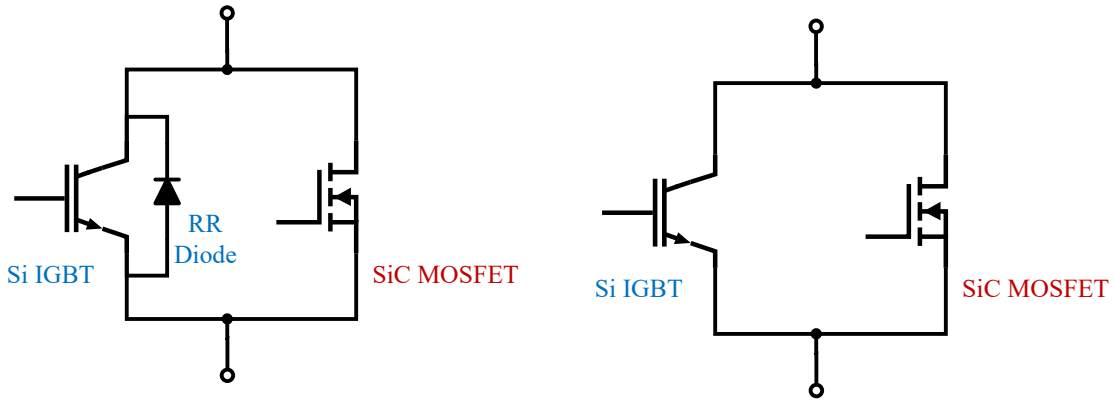
$$I_{\mathrm{rms}} = \frac{\hat{I}_{\mathrm{ac}}}{2} \tag{3.11}$$

Similar to the IGBT, the SiC MOSFET's R_{dson} is also dependent on temperature and is described as:

$$R_{\mathrm{dson}}(T_{\mathrm{j}}) = R_{\mathrm{dson,ref}} \cdot [1 + C_{\mathrm{T,MOS}} \cdot (T_{\mathrm{j,MOS}} - T_{\mathrm{ref,MOS}})] \tag{3.12}$$

3.2. Hybrid Switch Two Level Voltage Source Inverter

In this section, the losses of two types of Si/SiC Hybrid Switch are discussed (see Figure 3.1). Similar to Si/Si hybrid switches discussed in chapter 2, the first type uses the IGBT with anti parallel diode. The second type uses the MOSFET channel and its body diode for reverse conduction, which in turn eliminates the need of the IGBT diode. IGBTs without diode are usually only sold in discrete components or bare dies, which is why both types are investigated.



(a) Hybrid Switch using the IGBT with anti parallel diode

(b) Hybrid Switch using the MOSFET channel and its body diode for reverse conduction

Figure 3.1: Two types of Si/SiC hybrid switch.

3.2.1. Hybrid Switch Inverter Switching Losses

The hybrid switching loss can be calculated using Equation (3.1) and (3.2). However, the device that is used for switching is based on the switching strategy discussed in chapter 2, the current going through each device during switching would be different. If only the MOSFET is being used to turn on and off, the total peak load current is used in Equation (3.2). However, if both devices are used for turn on and off, then the load current used in Equation (3.2) is determined by current sharing described in the next section.

3.2.2. Hybrid Switch Conduction Losses using diode for reverse conduction

The conduction loss is calculated based on the conduction process shown in Figure 3.3. The current I_{knee} is the minimum current the switch need for the IGBT to overcome the PN junction barrier potential V_{ce} .

$$I_{\text{knee}} = \frac{V_{\text{ce}}}{R_{\text{ds}}} \tag{3.13}$$

Similarly, the current $I_{\text{knee,D}}$ is the minimum reverse current the switch need for the diode to start conducting, where V_{f} is the forward voltage and r_{f} is the diode on-state resistance.

$$I_{\text{knee,D}} = \frac{V_{\text{f}}}{R_{\text{f}}} \tag{3.14}$$

As mentioned in the previous chapter, the current sharing between the IGBT and the MOSFET in the Hybrid switch is dependent on the load current and temperature. The current sharing operation is summarized in Figure 3.2. A similar current sharing operation applies between the MOSFET and the diode of the IGBT or MOSFET body diode in the reverse conduction region. The current of the MOSFET and the IGBT based on current sharing is then defined by Equations (3.15) and (3.16) respectively. The same equations apply for the current sharing between the diode and the MOSFET during reverse conduction with V_{f} and R_{f} .

$$I_{\text{MOS,cs}} = \frac{R_{\text{ce}}}{R_{\text{ce}} + R_{\text{ds}}} i_{ac} + \frac{V_{\text{ce}}}{R_{\text{ce}} + R_{\text{ds}}} \tag{3.15}$$

$$I_{\text{IGBT,cs}} = \frac{R_{\text{ds}}}{R_{\text{ce}} + R_{\text{ds}}} i_{ac} - \frac{V_{\text{ce}}}{R_{\text{ce}} + R_{\text{ds}}} \tag{3.16}$$

To simplify, Equations (3.15) and (3.16) becomes:

$$I_{\text{MOS,cs}} = a_1 \cdot i_{ac} + c_1 \tag{3.17}$$

$$I_{\text{IGBT,cs}} = b_1 \cdot i_{ac} - c_1 \tag{3.18}$$

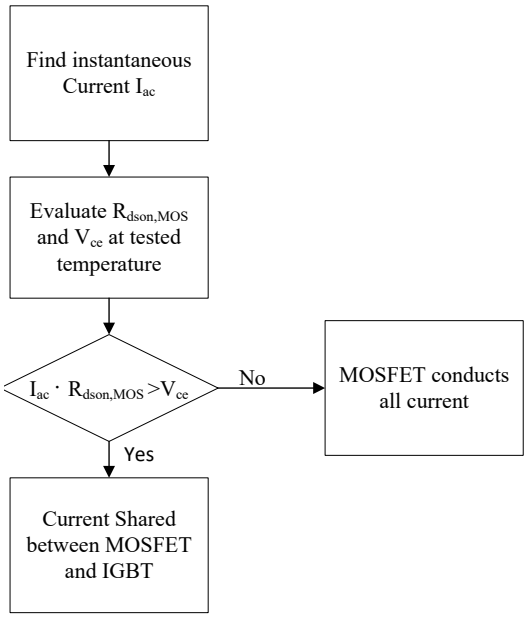


Figure 3.2: Flowchart of current sharing between the MOSFET and IGBT in the hybrid switch. Where I_{ac} is the instantaneous AC current flowing in the inverter arm, $R_{\mathrm{dson,MOS}}$ is the on-state resistance of the MOSFET and V_{ce} is the PN junction barrier potential.

Similarly, the current sharing between diode and MOSFET during reverse conduction is simplified to:

$$I_{\mathrm{MOS,cs}} = a_2 \cdot i_{ac} + b_2 \tag{3.19}$$

$$I_{\mathrm{DIODE,cs}} = c_2 \cdot i_{ac} - b_2 \tag{3.20}$$

The total conduction loss can be calculated by:

$$P_{\mathrm{cond}} = \frac{1}{2\pi}\int_0^{2\pi} E_{cond}(\theta)d\theta = P_{cond,IGBT} + P_{cond,DIODE} + P_{cond,MOS} \tag{3.21}$$

The current conduction is broken down into four different stages, shown in Figure 3.3. During $[0, \sigma]$ and $[\pi - \sigma, \pi]$ (stage 1), only the MOSFET is conducting, because the current is below I_{knee}. During $[\sigma, \pi - \sigma]$ (stage2), as the total load current increases, it is shared between the MOSFET and the IGBT. For reverse conduction, during $[\pi, \pi + \sigma_D]$ and $[2\pi - \sigma_D, 2\pi]$ (stage 3), only the MOSFET is conducting. During $[\pi + \sigma_D, 2\pi - \sigma_D]$(stage 4), current is shared between the IGBT diode and the MOSFET. σ is determined as the ratio between the junction barrier potential V_{knee} and the product of the MOSFET on-state and peak current $R_{ds} \cdot \hat{I}_{ac}$.

$$\sigma = \arcsin\left(\frac{V_{\mathrm{ce}}}{R_{\mathrm{ds}} \cdot \hat{I}_{\mathrm{ac}}}\right) \tag{3.22}$$

Under constant frequency conditions, the duty cycle of one phase for forward conduction and reverse conduction can be expressed as:

$$D = \frac{1}{2}[1 + m\sin(\theta + \phi)] \tag{3.23}$$

$$D' = \frac{1}{2}[1 - m\sin(\theta + \phi)] \tag{3.24}$$

The conduction loss of the IGBT can be determined by equation :

$$P_{\mathrm{cond,IGBT}} = R_{ce} \cdot I_{rms,IGBT}(\theta)^2 + V_{ce} \cdot I_{avg,IGBT}(\theta) \tag{3.25}$$

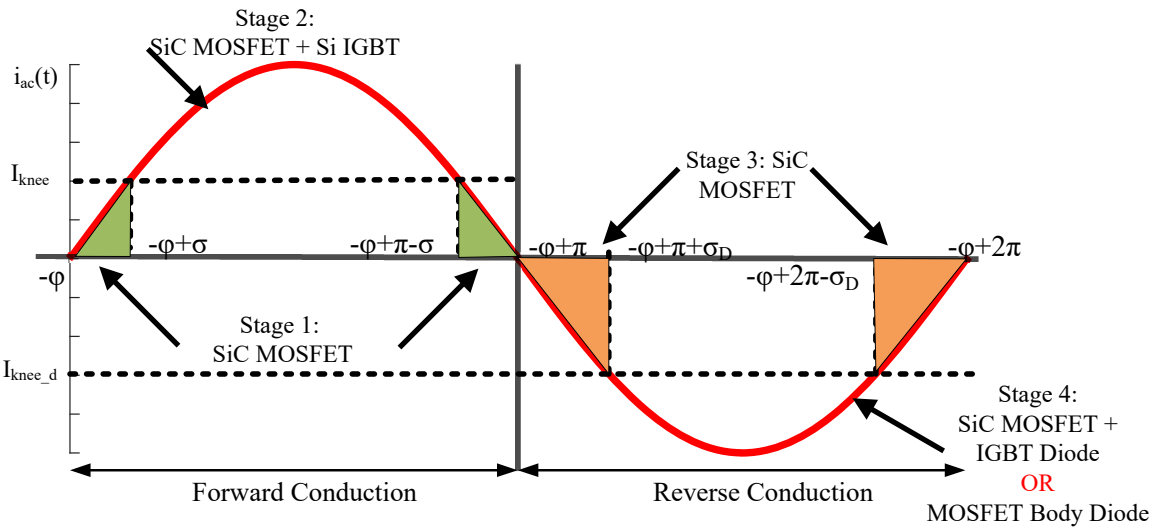


Figure 3.3: Conduction stages of the hybrid switch during fundamental period.

where the $I_{rms,IGBT}$ and $I_{avg,IGBT}$ are the IGBT RMS and average current value over the entire carrier period is calculated by Equations (3.26) and (3.27)

$$I_{rms,IGBT}(\theta) = \sqrt{\frac{1}{\pi}\int_{-\phi+\sigma}^{\frac{\pi-\phi}{2}} (i_{\mathrm{IGBT,cs}}(\theta))^2 \cdot D(\theta) d\theta} \tag{3.26}$$

$$I_{avg,IGBT}(\theta) = \frac{1}{\pi}\int_{-\phi+\sigma}^{\frac{\pi-\phi}{2}} i_{\mathrm{IGBT,cs}}(\theta) \cdot D(\theta) d\theta \tag{3.27}$$

If the phase shift between voltage and current is zero ($\phi = 0$), the conduction loss of IGBT becomes:

$$\begin{aligned} P_{\mathrm{cond,IGBT}} = \frac{1}{24\pi}\Bigg(&-4\hat{I}_{\mathrm{ac}}^2 R_{ce} c_1^2 \cos(\sigma)^3 m + \left(-12\left(-\hat{I}_{\mathrm{ac}} R_{ce} c_1 + m\left(b_1 R_{ce} - \frac{V_{ce}}{2}\right)\right) c_1 \hat{I}_{\mathrm{ac}} \sin(\sigma)\right. \\ &+12\hat{I}_{\mathrm{ac}}^2 R_{ce} c_1^2 m - 48\left(b_1 R_{ce} - \frac{V_{ce}}{2}\right) c_1 \hat{I}_{\mathrm{ac}} + 12 m b_1 (b_1 R_{ce} - V_{ce})\Bigg)\cos(\sigma) \\ &\left.+12\left(\sigma - \frac{\pi}{2}\right)\left(-\hat{I}_{\mathrm{ac}}^2 R_{ce} c_1^2 + m c_1\left(b_1 R_{ce} - \frac{V_{ce}}{2}\right)\hat{I}_{\mathrm{ac}} - 2R_{ce} b_1^2 + 2V_{ce} b_1\right)\right) \end{aligned} \tag{3.28}$$

The Diode conduction losses are:

$$P_{\mathrm{cond,DIODE}} = R_f \cdot I_{rms,DIODE}(\theta)^2 + V_f \cdot I_{avg,DIODE}(\theta) \tag{3.29}$$

where the $I_{rms,DIODE}$ and $I_{avg,DIODE}$ is the Diode RMS and average current value over the entire carrier period and calculated by Equations (3.30) and (3.31):

$$I_{rms,DIODE}(\theta) = \sqrt{\frac{1}{\pi}\int_{-\phi+\sigma_d}^{\frac{\pi-\phi}{2}} (i_{\mathrm{DIODE,cs}}(\theta))^2 \cdot D'(\theta) d\theta} \tag{3.30}$$

$$I_{avg,DIODE}(\theta) = \frac{1}{\pi}\int_{-\phi+\sigma_d}^{\frac{\pi-\phi}{2}} i_{\mathrm{DIODE,cs}}(\theta) \cdot D'(\theta) d\theta \tag{3.31}$$

If the phase shift between voltage and current is zero ($\phi = 0$), the conduction loss of Diode becomes:

$$P_{\text{cond,DIODE}} = \frac{1}{24\pi}\left(4\hat{I}_{\text{ac}}^2 R_f \cos(\sigma_d)^3 c_2^2 m + \left(12\left(\hat{I}_{\text{ac}} R_f c_2 + m\left(R_f b_2 - \frac{V_f}{2}\right)\right)c_2 \hat{I}_{\text{ac}} \sin(\sigma_d)\right.\right.$$
$$-12\hat{I}_{\text{ac}}^2 R_f c_2^2 m - 48c_2\left(R_f b_2 - \frac{V_f}{2}\right)\hat{I}_{\text{ac}} - 12mb_2\left(R_f b_2 - V_f\right)\Big)\cos(\sigma_d)$$
$$\left.\left.-12\left(R_f \hat{I}_{\text{ac}}^2 c_2^2 + mc_2\left(R_f b_2 - \frac{V_f}{2}\right)\hat{I}_{\text{ac}} + 2R_f b_2^2 - 2V_f b_2\right)\left(\sigma_d - \frac{\pi}{2}\right)\right)\right) \quad (3.32)$$

The MOSFET conduction losses are:

$$P_{\text{cond,MOS}} = R_{ds} \cdot I_{rms}(\theta)^2 \quad (3.33)$$

where the I_{rms} is the RMS value of the current over the entire carrier period and calculated by (3.34)

$$I_{rms,MOS}(\theta) = \left(\frac{1}{\pi}\left(\int_{-\phi}^{-\phi+\sigma} i_{\text{ac}}(\theta))^2 \cdot D(\theta)d\theta + \int_{-\phi+\sigma}^{\frac{\pi-\phi}{2}} (i_{\text{MOS,cs}}(\theta))^2 \cdot D(\theta)d\theta\right.\right.$$
$$\left.\left. + \int_{-\phi}^{-\phi+\sigma_d} (i_{\text{ac}}(\theta))^2 \cdot D'(\theta)d\theta + \int_{-\phi+\sigma_d}^{\frac{\pi-\phi}{2}} (i_{\text{MOS,cs}}(\theta))^2 \cdot D'(\theta)d\theta\right)^{\frac{1}{2}} \quad (3.34)$$

If the phase shift between voltage and current is zero ($\phi = 0$), the conduction loss of MOSFET becomes:

$$P_{\text{cond,MOS}} = -\frac{1}{6\pi}\left(R_{ds}\left(-a_2^2 + 1\right)m\hat{I}_{\text{ac}}^2 \cos\left(\sigma_d\right)^3 + \left(\left(\left(-3a_2^2 + 3\right)\hat{I}_{\text{ac}}^2\right.\right.\right.$$
$$\left. + 3b_2\hat{I}_{\text{ac}}a_2 m\right)\sin\left(\sigma_d\right) + \left(3a_2^2 - 3\right)m\hat{I}_{\text{ac}}^2 - 12b_2\hat{I}_{\text{ac}}a_2 + 3b_2^2 m\right)\cos\left(\sigma_d\right)$$
$$+ m\hat{I}_{\text{ac}}^2\left(a_1 - 1\right)\left(a_1 + 1\right)\cos(\sigma)^3 + \left(\left(\left(-3a_1^2 + 3\right)\hat{I}_{\text{ac}}^2 - 3b_1\hat{I}_{\text{ac}}a_1 m\right)\sin(\sigma)\right.$$
$$+ \left(-3a_1^2 + 3\right)m\hat{I}_{\text{ac}}^2 - 12b_1\hat{I}_{\text{ac}}a_1 - 3b_1^2 m\right)\cos(\sigma) + \left(\left(-\frac{3\pi}{2} + 3\sigma\right)a_1^2\right. \quad (3.35)$$
$$+\left(-\frac{3\pi}{2} + 3\sigma_d\right)a_2^2 - 3\sigma_d - 3\sigma\Big)\hat{I}_{\text{ac}}^2 + 3m\left(b_1\left(\sigma - \frac{\pi}{2}\right)a_1\right.$$
$$\left.\left.+\frac{a_2 b_2\left(\pi - 2\sigma_d\right)}{2}\right)\hat{I}_{\text{ac}} + (6\sigma - 3\pi)b_1^2 - 3b_2^2\left(\pi - 2\sigma_d\right)\right)$$

3.2.3. Hybrid Switch using the SiC MOSFET body diode for reverse conduction

For hybrid switch without the IGBT diode, the MOSFET channel and its body diode would be used for reverse conduction. The current I_{knee} and forward conduction currents are the same as the previous section, Equations (3.15) - (3.16). For reverse conduction, the MOSFET would take the entire load current, I_{ac} .

The total conduction loss again can be calculated by:

$$P_{\text{cond}} = \frac{1}{2\pi}\int_0^{2\pi} E_{cond}(\theta)d\theta = P_{cond,IGBT} + P_{cond,MOS} \quad (3.36)$$

where during $[0, \sigma]$ and $[\pi - \sigma, \pi]$ (stage 1), only the MOSFET is conducting. During $[\sigma, \pi - \sigma]$ (stage2), current is shared between the MOSFET and the IGBT. For reverse conduction, both during $[\pi, \pi + \sigma_D]$ and $[2\pi - \sigma_D, 2\pi]$ (stage 3) and $[\pi + \sigma_D, 2\pi - \sigma_D]$(stage 4), the current is conducted by the MOSFET only. σ is determined as the ratio between junction barrier potential V_{knee} and product of the MOSFET on-state and peak current $R_{ds} \cdot I_{peak}$.

With The IGBT conduction loss same as what was previously stated (Equation (3.25) - (3.27)), the only difference is the MOSFET conduction loss:

$$P_{\text{cond,MOS}} = R_{ds} \cdot I_{rms}(\theta)^2 \quad (3.37)$$

where the I_{rms} is the RMS value of the current over the entire carrier period and calculated by Equation (3.38). The shared current $i_{\mathrm{MOS,cs}}$ is described by Equation (3.15).

$$I_{rms,MOS}(\theta) = (\frac{1}{\pi}\int_{-\phi}^{-\phi+\sigma}(i_{\mathrm{ac}}(\theta))^2 \cdot D(\theta)d\theta + \int_{-\phi+\sigma}^{\frac{\pi-\phi}{2}}(i_{\mathrm{MOS,cs}}(\theta))^2 \cdot D(\theta)d\theta + \int_{-\phi}^{\frac{\pi-\phi}{2}}(i_{\mathrm{ac}}(\theta))^2 \cdot D'(\theta)d\theta)^{\frac{1}{2}} \quad (3.38)$$

If the phase shift between voltage and current is zero ($\phi = 0$), the conduction loss of MOSFET becomes:

$$\begin{aligned} P_{\mathrm{cond,MOS}} = -\frac{1}{2\pi}\Bigg(R_{ds}\Bigg(&\frac{m\hat{I}_{\mathrm{ac}}^2\,(a_1-1)\,(a_1+1)\cos(\sigma)^3}{3} + \Big(\Big(\big(-a_1^2+1\big)\hat{I}_{\mathrm{ac}}^2 \\ &-b_1\hat{I}_{\mathrm{ac}}a_1 m\Big)\sin(\sigma) + \big(-ma_1^2+m\big)\hat{I}_{\mathrm{ac}}^2 - 4b_1\hat{I}_{\mathrm{ac}}a_1 - b_1^2 m\Big)\cos(\sigma) \\ &+\Big(\Big(\sigma-\frac{\pi}{2}\Big)a_1^2 - \sigma - \frac{\pi}{2}\Big)\hat{I}_{\mathrm{ac}}^2 + m\Big(\sigma-\frac{\pi}{2}\Big)b_1 a_1\hat{I}_{\mathrm{ac}} + 2\Big(\sigma-\frac{\pi}{2}\Big)b_1^2\Big) \end{aligned} \quad (3.39)$$

An alternative way to determine the conduction losses of the hybrid switch is to calculate the product of the switch voltage and current through the entire conduction cycle interatively. The forward and reverse conduction losses can be generally described using Equations (3.40) and (3.40). The drawback of using this method is that it is computationally heavy as it calculates the voltage-current product at each data point in the conduction cycle.

$$P_{\mathrm{cond}} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} I(\theta+\varphi)\cdot V(I(\theta))\cdot D(\theta)d\theta \quad (3.40)$$

The reverse conduction losses of the hybrid switch are given by:

$$P_{\mathrm{cond}} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} I(\theta+\varphi)\cdot V(I(\theta))\cdot (1-D(\theta))d\theta \quad (3.41)$$

The comparison of the hybrid switch conduction losses calculated using the analytical equation method and the interative method is shown in Figure 3.4. The same set of parameters are used while sweeping across the load current from 0 to 300A. The analytical equation method, while requiring less computational time, produces findings relatively similar to the results calculated using the interative method.

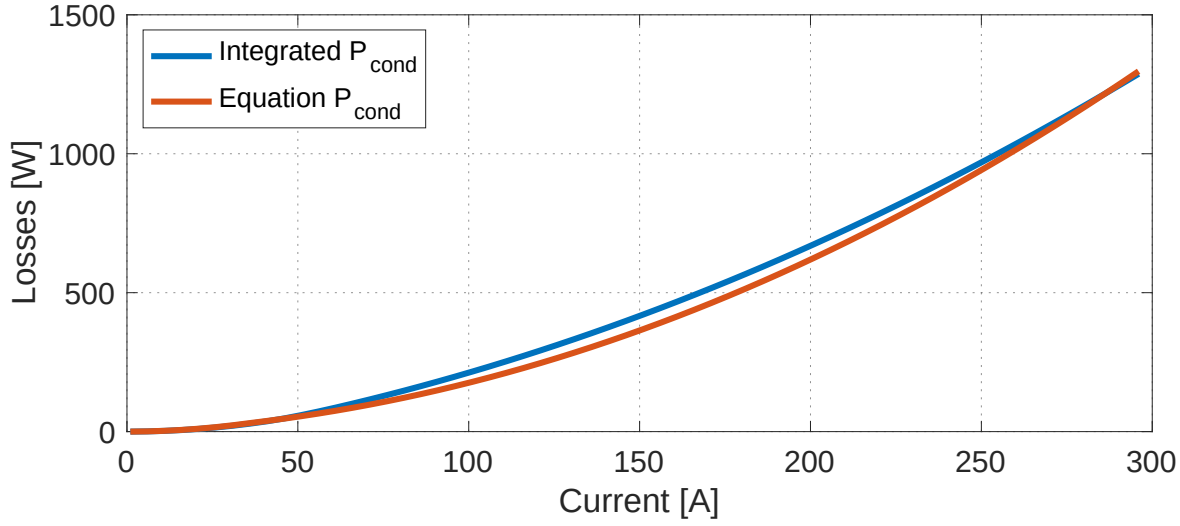


Figure 3.4: Conduction losses of the hybrid switch calculated using both the integration method (blue) and the analytical equations (red).

In the next two chapters, the on-state and switching characteristics such as $R_{\mathrm{dson,MOS}}$ are determined experimentally and compared to values obtained from the manufacturer datasheets. With these values, the EV traction drive inverter efficiency can be determined using the equations described in this chapter. In chapter 6, the inverter efficiency at static load condition and over standardized driving cycles are simulated and discussed.

4

Si/SiC Hybrid Switch Characterization

The Si IGBT and SiC MOSFET paralleled hybrid switch takes advantages of both IGBT and MOSFET characteristics. Prior research has demonstrated that the hybrid switch based inverter can outperform the IGBT based inverter at low current and the SiC MOSFET based inverter at high current [3]. This is ideal for the application of EV traction drives as the inverter mostly operates at low partial load profile. The characteristics of the different switches are examined in this section using the manufacturer's datasheet [15, 16] of the selected Si IGBT and SiC MOSFET and circuit simulations.

4.1. Selection of Devices

The realization of a hybrid switch can be achieved by paralleling Si IGBTs and SiC MOSFETs. These semiconductor devices are commercially sold as 62 mm power modules, as illustrated in Figure 4.1 (a) or as discrete TO-packaged devices as shown in Figure 4.1 (b). Both packaging configurations of Si IGBT and SiC MOSFET are popular solutions with many suppliers as the 62 mm modules can offer higher nominal current rating than the discrete packaging. Paralleling discrete devices introduce significant parasitic inductances that can negatively affect the commutation loop [17]. In this context, integrating the hybrid switch in a single module would reduce parasitic inductance and lead to optimal performance [22]. However, to our best knowledge a Si-SiC hybrid switch power module is not currently commercially available, and so, in this study, the hybrid switch is realized by paralleling several single switch discrete components.

The hybrid switch is designed for the implementation in the drive train of the Nissan Leaf 2011 Model, whose main electric parameters are listed in Table 4.1. Due to the available commercial products and the modularity of the design, the current rating of each hybrid switch is 300 A, assuming that the full peak current capability, i.e., 600 A, can be achieved through the paralleling of two identical switches. Paralleling discrete components for inverters is a common practice used Electric Vehicles. In Figure 4.2 the semiconductor arrangement of the Tesla Model S traction inverter is highlighted, where multiple Si IGBTs are paralleled in order to reach the required nominal current. Three different configurations

Figure 4.1: (a) Half-bridge SiC MOSFET Module [30] and (b) Discrete Si IGBT [16].

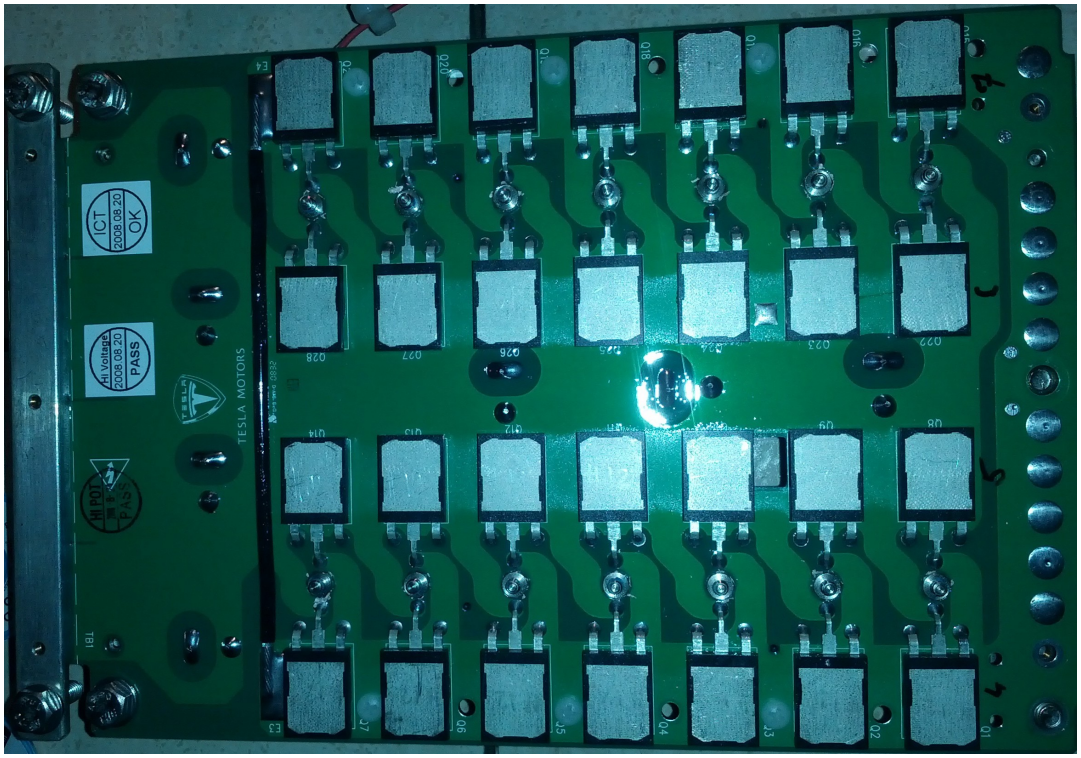


Figure 4.2: Inverter of Tesla Model S showing the paralleling of multiple discrete IGBTs [16].

Parameter	Value	Unit
Peak Phase AC Current	600	A
Battery DC Voltage	375	V
Battery Capacity	24	kWh
Output Power	80	kW
Switching Frequency	5	kHz

Table 4.1: Nissan Leaf Drive Train Parameters

of the same current rating, based on off-the-shelf components, are compared, and they are displayed in Figure 4.3. Specifically, Figure 4.3(a) and Figure 4.3(c) demonstrate the full Si IGBT and full SiC MOSFET configurations respectively, where eight discrete components are arranged in parallel for each inverter switch. For the hybrid solutions, four discrete IGBTs are placed in parallel with four discrete SiC MOSFETs per inverter switch, cf. Figure 4.3(b). Previous research has shown that by reducing the rated current ratio between the MOSFET and IGBT, costs can be lowered in a trade-off with higher thermal stress [17, 31]. A 1:1 Si/SiC rated current ratio has been considered in this study to ensure that the switch would operate within the thermal limitation. Therefore, the SiC MOSFETs and Si IGBTs in the hybrid switches are designed to have equal current rating. With the low voltage requirement of the EV, it is possible to use 650V voltage class components for the hybrid switch. However, due to the availability of products, 1200V voltage class components will be compared in this thesis. The specific selection of components and their ratings can be found in Table 4.2.

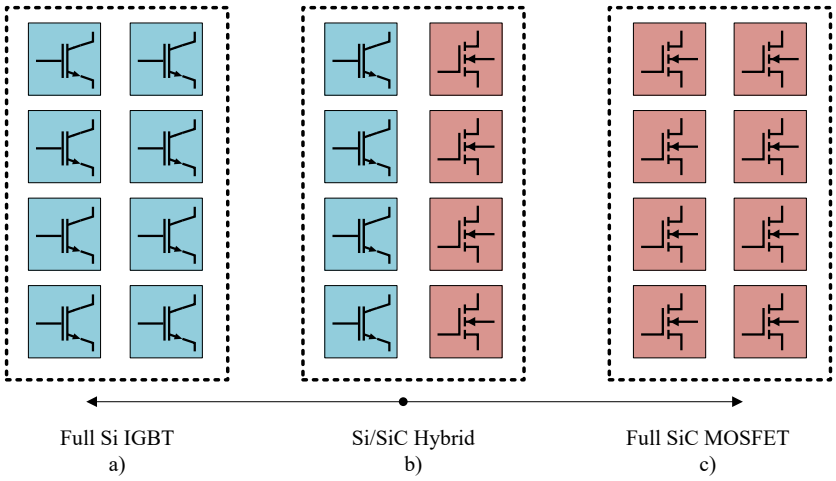


Figure 4.3: The three configurations for the inverter switches considered in this study: a) Eight discrete IGBTs in parallel, b) Four discrete IGBTs with four discrete MOSFETs in parallel, c) Eight discrete MOSFETs in parallel.

Product	Type	Package	Rating	Price [$]
ROHM SCT3030AL	MOSFET	Discrete	1200V/ 39A	30.61
Infineon IKW30N65ES5	IGBT	Discrete	1200V/ 40A	9.95

Table 4.2: Off-The-Shelf Components Selected For The Hybrid Switches Realization

4.2. On-state Characteristics

To compare the on-state characteristics of the switches, a linearized model was created in LTSpice based on the data extracted from the manufacturer's datasheet. During conduction, MOSFETs can be modeled as a resistor with the R_{dson} as the resistance, while the IGBTs can be modeled as a resistor and a voltage source modeling the PN junction potential. The on-state resistances and the PN junction potential are obtained from the datasheet. By paralleling the MOSFET and IGBT model, the hybrid switch can be realized. The LTSpice Model can be seen in Figure 4.4. By sweeping a DC voltage in LTSpice, the output characteristics are determined. The output characteristics are compared at 80°C, which is the average temperature that the switches would normally be operating at in an EV. The on-state characteristics of the hybrid switch are plotted in Figure 4.5. As it can be noted the hybrid switches take the output characteristics of the MOSFET at low current and of the paralleling of the IGBT and MOSFET at high current.

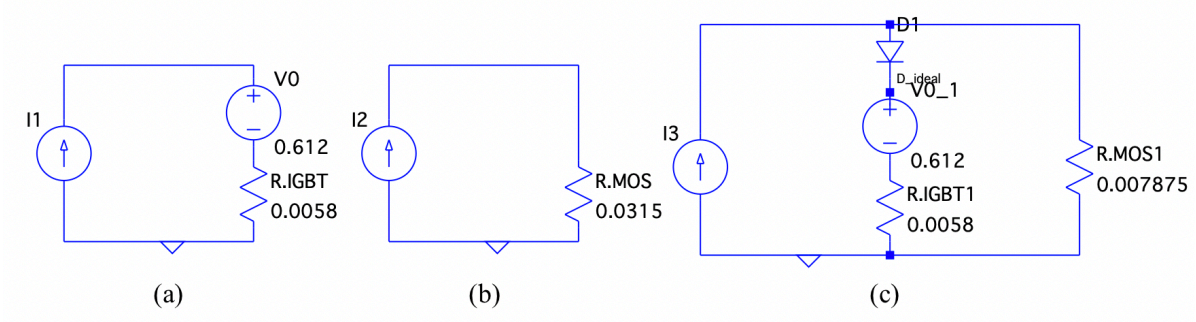


Figure 4.4: LTSpice linearized model for (a)IGBT, (b)MOSFET, and (c)Hybrid Switch.

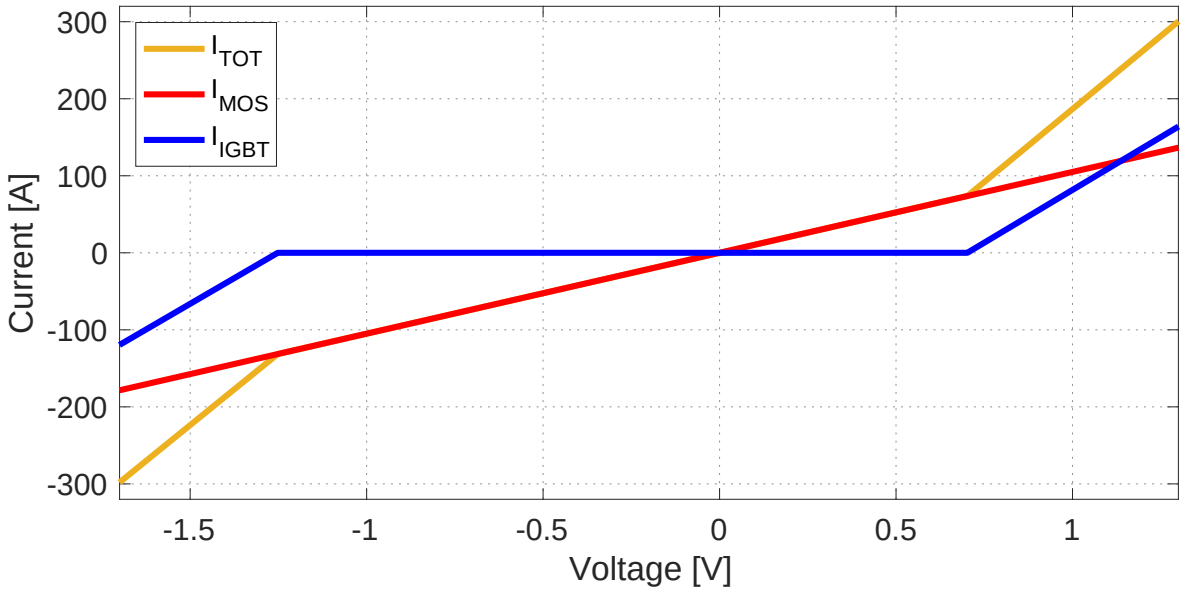


Figure 4.5: The linearized on-state characteristic of the hybrid switch (yellow) at 80 °C. The individual on-state characteristic of the MOSFET and IGBT in the hybrid switch are depicted in the red and blue lines respectively.

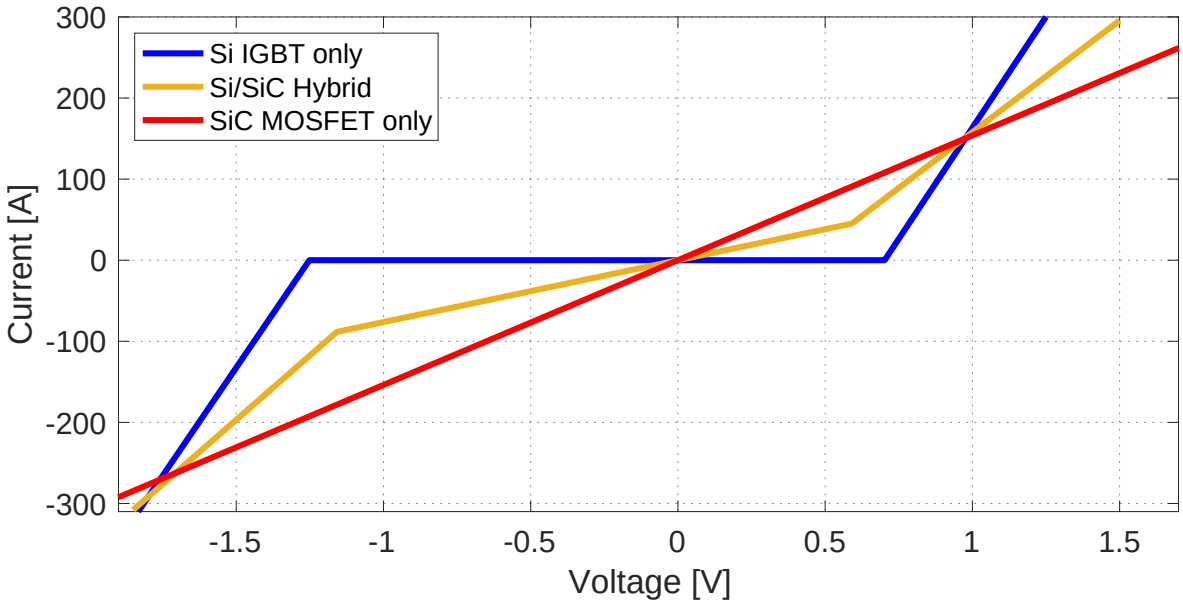


Figure 4.6: The on-state characteristics of the pure Si IGBT switch (blue), pure SiC MOSFET (red) and the Hybrid switch (yellow) considered in this thesis at 80°C.

The on-state behaviour of the discrete-only configurations considered in Figure 4.3 can be observed in Figure 4.6. As predicted, the hybrid switches have a trade-off performance when compared to the single technology configurations. As it can be noted the hybrid configurations demonstrate a lower voltage drop at equal forward current than the full Si IGBT switch at low currents and better performance than the full SiC MOSFET switch at high current. As discussed in chapter 2, as temperature increases, the on-state resistance increases and the PN junction barrier potential decreases. These change in on-state characteristics of all three configurations can be seen in Figure 4.7 and Figure 4.8.

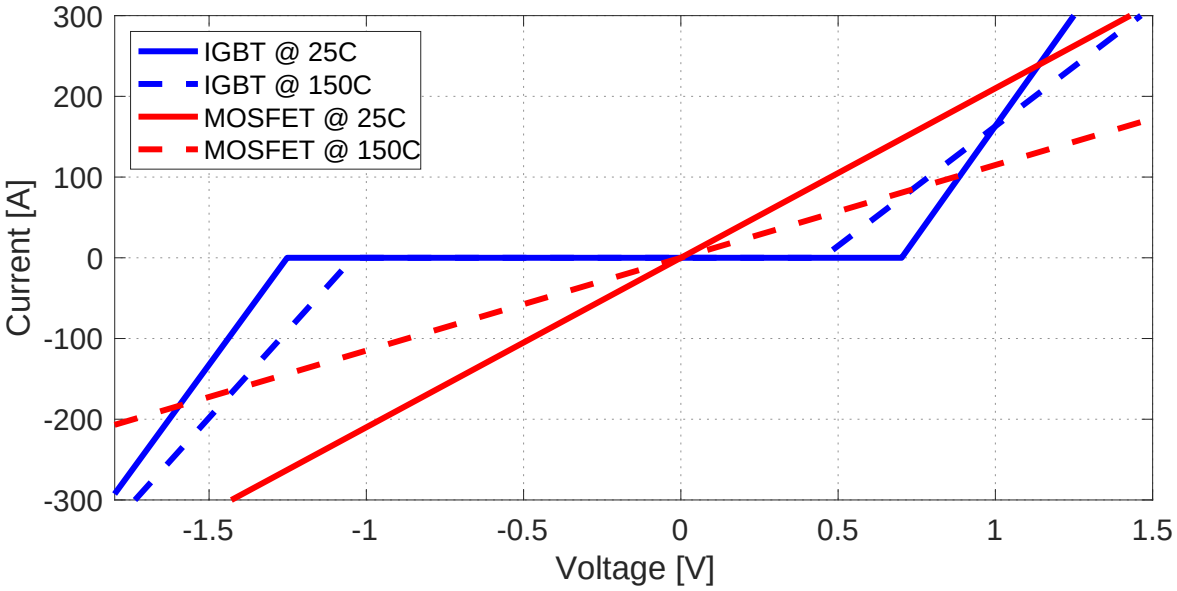


Figure 4.7: The linearized on-state characteristic of the pure Si IGBT (blue) and the pure SiC MOSFET (red) switches at 25 °C (solid line) and 125°C (dotted line).

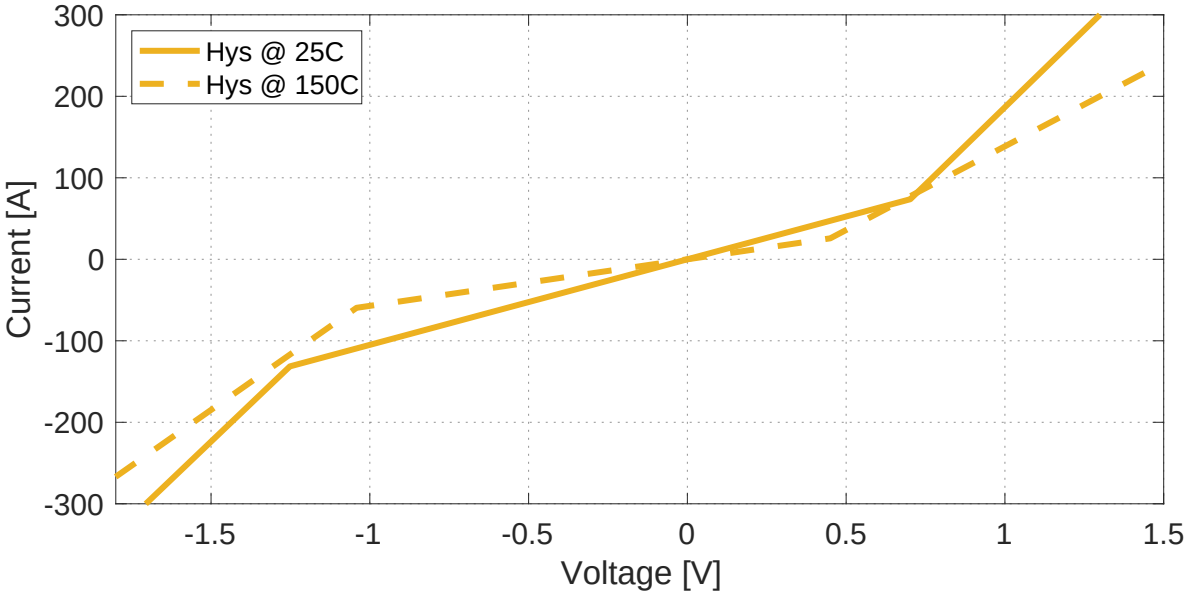


Figure 4.8: The linearized on-state characteristic of the hybrid switch at 25 °C and 125°C.

4.2.1. Current Sharing

As mentioned in Chapter chapter 2, the current sharing between the IGBT and the MOSFET changes due to the total load current and temperature. To visualize this, the output characteristic is linearized between 0°C and 150°C and swept between -300A to 300A (Figure 4.9). As predicted, the total current flows through the MOSFET at low current. As the load current increases, more current is being shared with the IGBT. A similar trend can be observed in the negative region for the IGBT diode and the MOSFET.

The SiC MOSFET component has a higher coefficient C_T than the Si IGBT. Therefore, the IGBT, with its lower on-state resistance, would conduct a higher percentage of the total load current at higher temperature. Furthermore, since the IGBT's junction barrier potential decreases as temperature increases, the IGBT starts conducting current at a lower total current value.

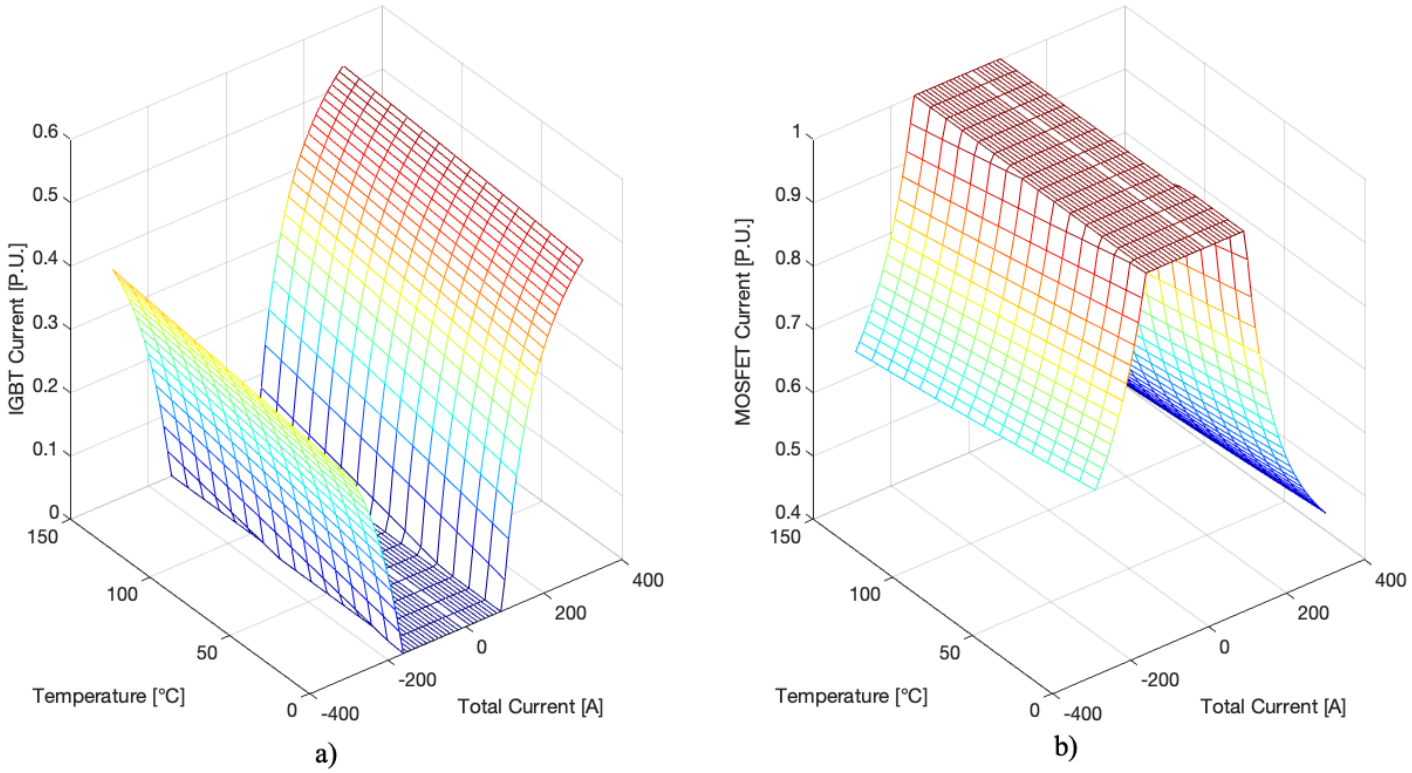


Figure 4.9: Current sharing between the MOSFET and IGBT in the hybrid as a function of total current and temperature. (a)Per Unit of current flowing through IGBT, (b) Per unit of current flowing through MOSFET.

4.3. Switching Characteristics

As mentioned in chapter 2, the MOSFET's switching loss does not heavily depend on the junction temperature, however this does influence the IGBT switching behaviour. In Figure 4.10, the temperature's effect on the IGBT switching losses is shown. Using the optimal switching strategy, the higher switching losses due to temperature increase can be alleviated as the MOSFET will be the only one switching. The gate resistance, which determines the switching time, affects the switching loss as well. In Figure 4.10, the gate resistor's effect on the switching losses are shown. With high gate resistance, further switching losses can be observed due to the slower turn on and off. However, this also means less oscillation due to resonance between the gate resistor and the switch capacitance, which causes overshoot and EMI noises.

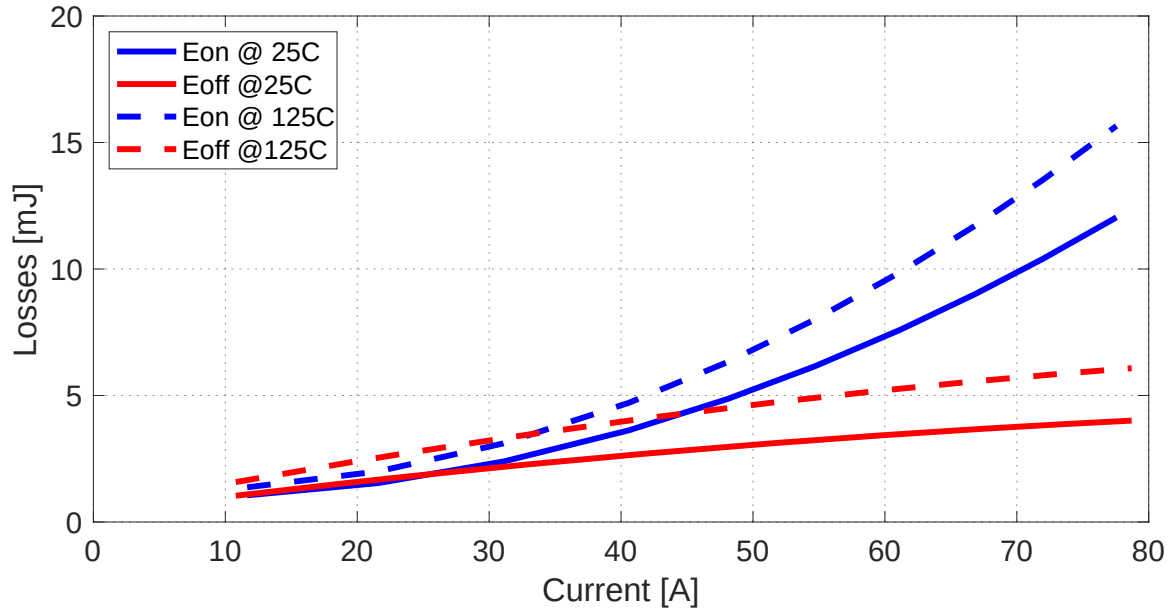


Figure 4.10: Temperature's effect on IGBT switching loss as a function of switch current.

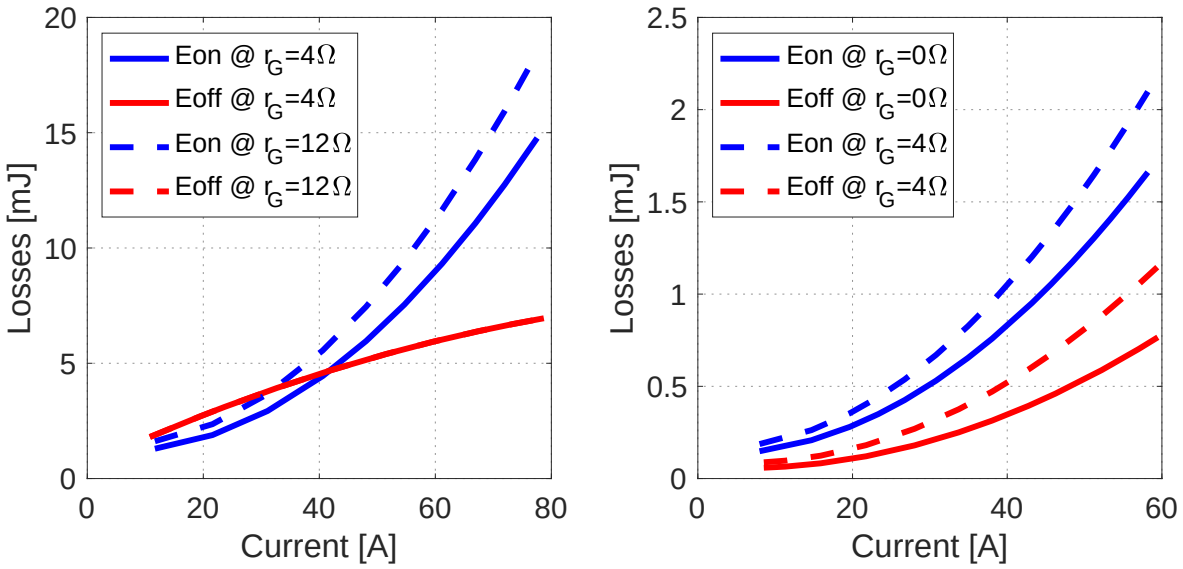


Figure 4.11: Gate resistance's effect on switching loss as a function of switch current for the IGBT (left) and the MOSFET(right).

5

Experimental Characterization of Si/SiC Hybrid Switch

5.1. Double Pulse Inductive Test

The Double Pulse Test (DPT) is performed to determine the switching losses of the switches. The circuit diagram of the Double Pulse Test can be seen in Figure 5.1. The ideal waveform of a DPT can be seen in Figure 5.2. The procedure is broken down into 3 phases:

1. First Pulse: The gate signal turns on the DUT which enables the DC source to charge up the inductor to the desired test current. For the hybrid switch, gate signals are sent to both device with the designed turn-on delay. The duration of the first pulse is varied to achieve different test current points. The determination of the pulse duration is discussed in subsection 5.1.4.
2. Turn-off: The gate signal turns off the DUT. The desired test current is held constant by the inductor. The turn-off characteristics are measured during this phase.
3. Second Pulse: The gate signal turns on the DUT again with the same current as turn-off (assuming the inductor is large enough to hold current constant for the duration between two pulses). The turn-on characteristics are measured in this phase.

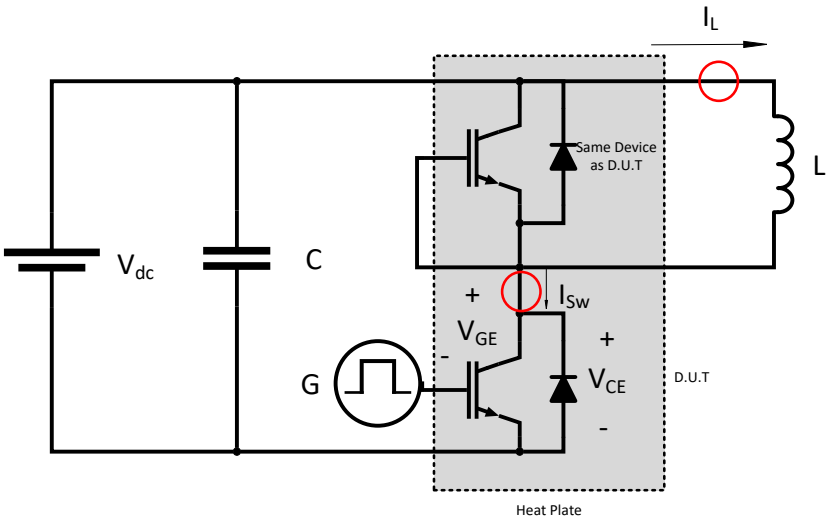


Figure 5.1: Simplified diagram of the Double Pulse Test. The voltage source applies voltage (V_{dc}) to the upper and lower switch (DUT). The gate signal G sends the double pulse signal to the DUT. L and C are the test inductor and the capacitor banks respectively.

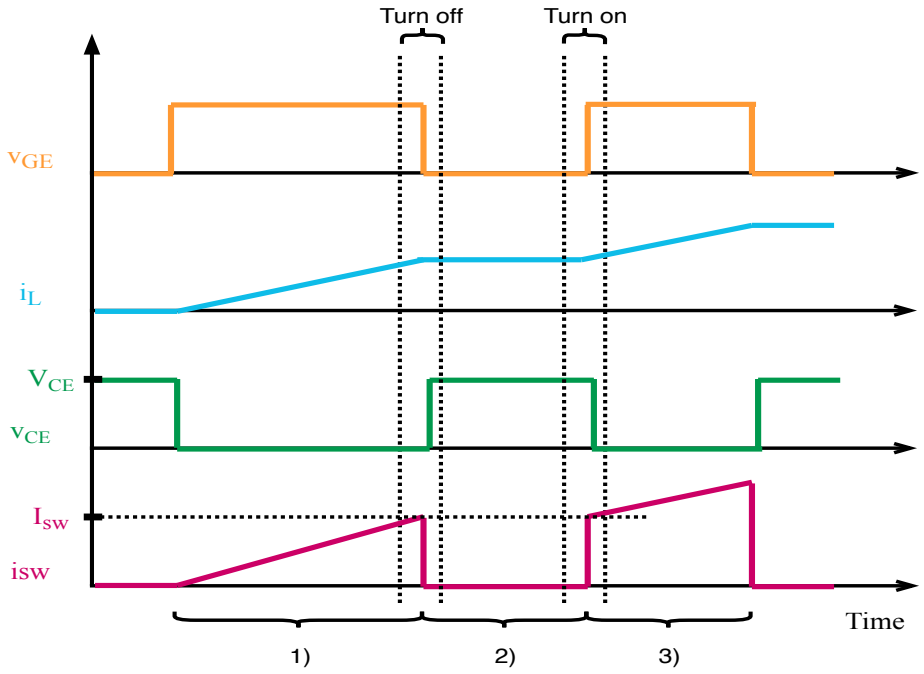


Figure 5.2: Ideal waveform of the Double Pulse Test of a single switch.

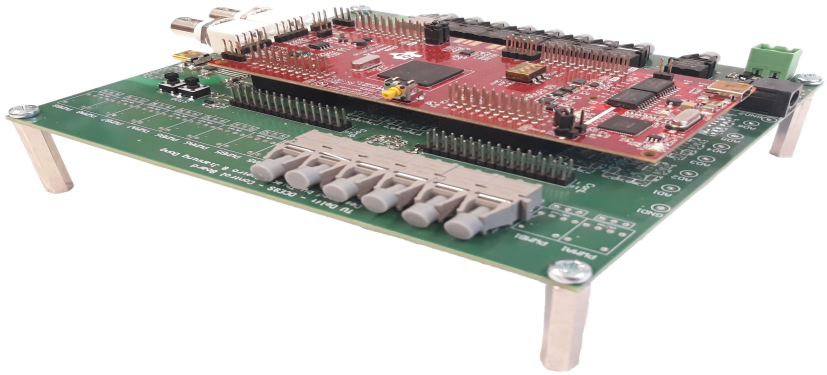


Figure 5.3: Control Board

5.1.1. Control Board

The control board (Figure 5.3) uses the Ti C2000x microcontroller to produce desired PWM waveforms to the Gate Driver Board through fiber optic signals. The microcontroller requires 5V from a DC power supply and requires a USB connection to a PC for the programmed code.

5.1.2. Gate Driver Board

The gate driver board (Figure 5.4) converts optical signal from the control board to gate control voltages v_{gs}. The range of the gate driver is -4V (blocking) to +19V (conducting).

5.1.3. Main Double Pulse Test Board

The main board of the DPT (Figure 5.5) is used to attach the MOSFET and IGBT (both module and discrete). Capacitor banks are included in the main board to ensure the stability of waveforms. The temperature of the switch is also controlled and monitored through the main board, this is further outlined in section subsection 5.1.5. The test measurements are taken from the main board. These include:

- Gate Voltage, v_{gs}:the voltage measured between the gate and the source of the MOSFET (Pin 1 and 3) or between the gate and the emitter of the IGBT (Pin 1 and 3). This voltage is measured

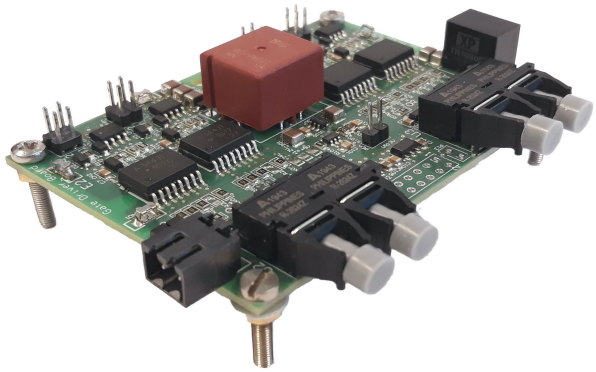


Figure 5.4: The Gate Driver.

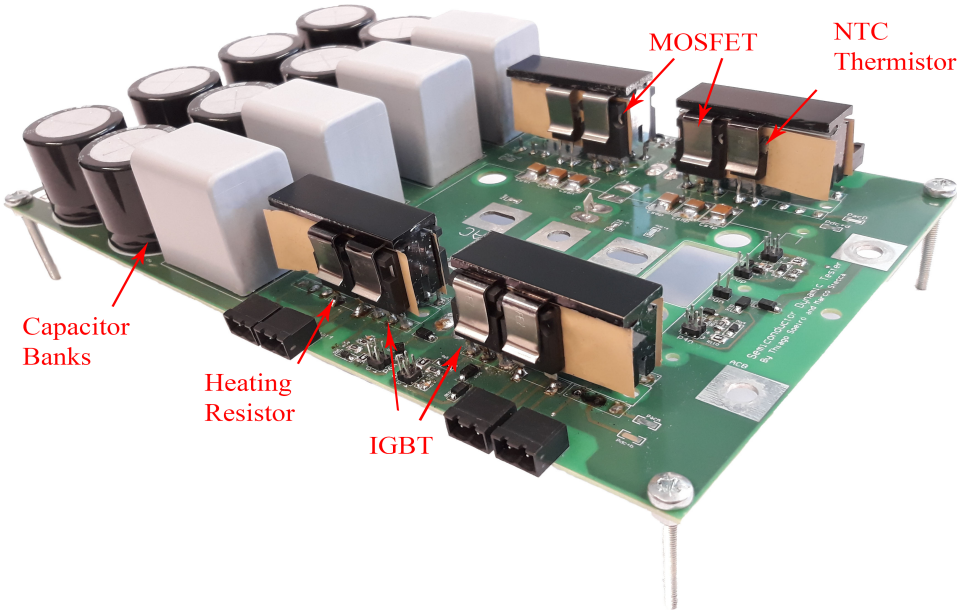


Figure 5.5: Main board for the Double Pulse Test.

using an differential voltage probe.

- Inductor Current, i_{sw}: the current measured through inductor winding using high current Pearson probe.
- Switch Voltage, v_{ds}: the voltage measured between the drain and source of the MOSFET (Pin 2 and 3) or between the drain and the emitter of the IGBT (Pin 2 and 3). This voltage is measured using an differential voltage probe.
- Switch Current, i_{sw}: the current measured through the extruded current tap using a Rogowski coil.

5.1.4. Inductor Design

The test inductor of the Double Pulse Test is used to hold the current constant between the two pulses, which ensures that the turn-on and turn-off losses are measured at the same current. The inductance of the test inductor depends on the DC Voltage, pulse width, and the desired current. This relationship can be described by Equation (5.1), where L is the inductance, V_L is the voltage across the inductor, Δt is the time of the pulse and Δi is the desired current increase during the pulse.

$$L = V_L \frac{\Delta t}{\Delta i} \tag{5.1}$$

Figure 5.6: The Test Inductor

the voltage across the inductor is 600V and the test current ranges from 25A to 300A. The switching losses are measured at different test current points by varying the gate pulse duration. With the minimum pulse duration at 1us, the inductance is designed to be 24uH. To efficiently reach the desired test current while ensuring that the inductor does not reach saturation, the inductor air gap is adjusted between tests with plastic spacers.

5.1.5. Temperature Control

During operation, the semiconductor junction temperature rises as the load increases. Since the temperature variation from the short pulses is negligible, stable external heating is required to observe the effect of temperature on switching losses. A heating resistor and a NTC thermistor are attached to the heat sink of the switches for this purpose. The heating resistor takes DC voltage from the power supply and heats the heatsink. The thermistor's resistance has a negative non-linear correlation with temperature. Three temperature points and their corresponding NTC resistances are chosen for the tests (Table 5.1). During the test, a FLIR thermal camera is also used to ensure the temperature is in the range of the test. The thermal image of the switches at 125°C is shown in Figure 5.7. The entire testing setup can be seen in Figure 5.8.

Table 5.1: Testing temperature and its corresponding thermistor resistances

Temperature [°C]	Resistance [kohm]	Power Supply Voltage [V]
25	9.8	0
75	1.48	25
125	0.341	37

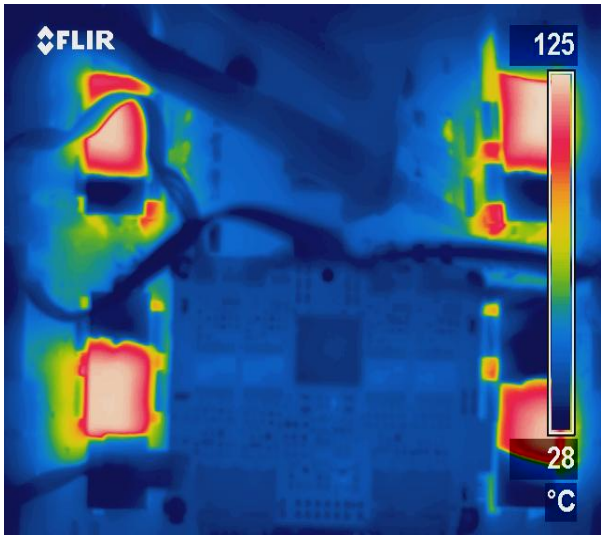


Figure 5.7: Thermal Image taken from FLIR thermal camera showing the discrete switches on the main board heated up to 125°C

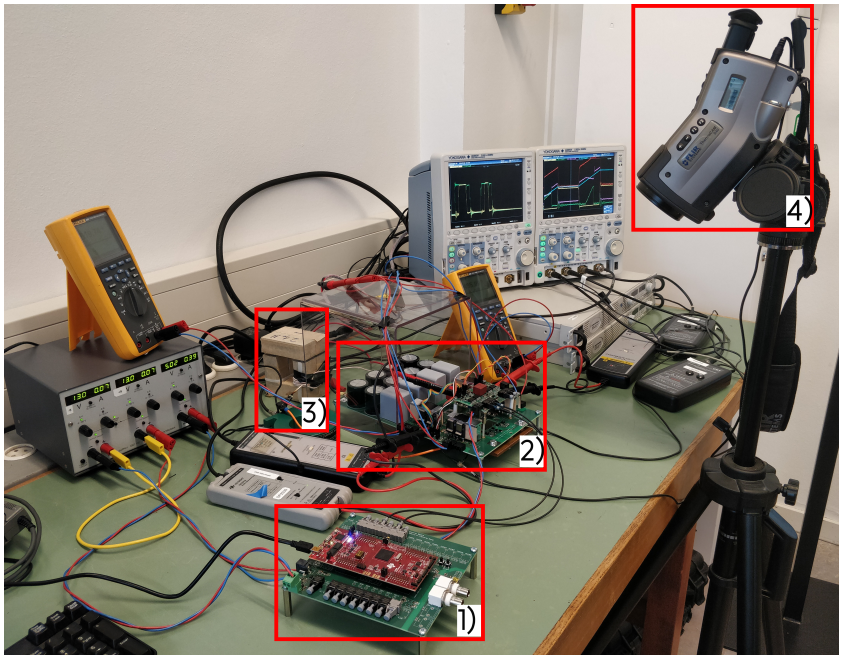


Figure 5.8: Actual Realization of the Double Pulse Test. (1) Control board, (2) Main board and gate driver, (3) Test inductor, and (4) Thermal camera.

5.2. Comparison of Switching Characteristics

All three configurations of the switch are put through the double pulse test described in previous section. For pure IGBT and MOSFET switches, 4 discrete components are associated in parallel for both the DUT and the upper switch. For the hybrid switch, 2 Si IGBT and 2 SiC MOSFET components are placed in parallel. The gate resistance is selected to be 4Ω for each switch. This is chosen to reduce ringing (which may cause the gate driver to exhibit unwanted behavior) while still have relatively short switching time. The switching characteristics of each switch are evaluated at different temperatures.

5.2.1. Pure IGBT Switch

The double pulse test waveform of Si IGBT Switch can be seen in Figure 5.9. The non-ideal behaviour described in chapter 2 can be clearly observed. The voltage dip at turn-on and overshoot at turn-off

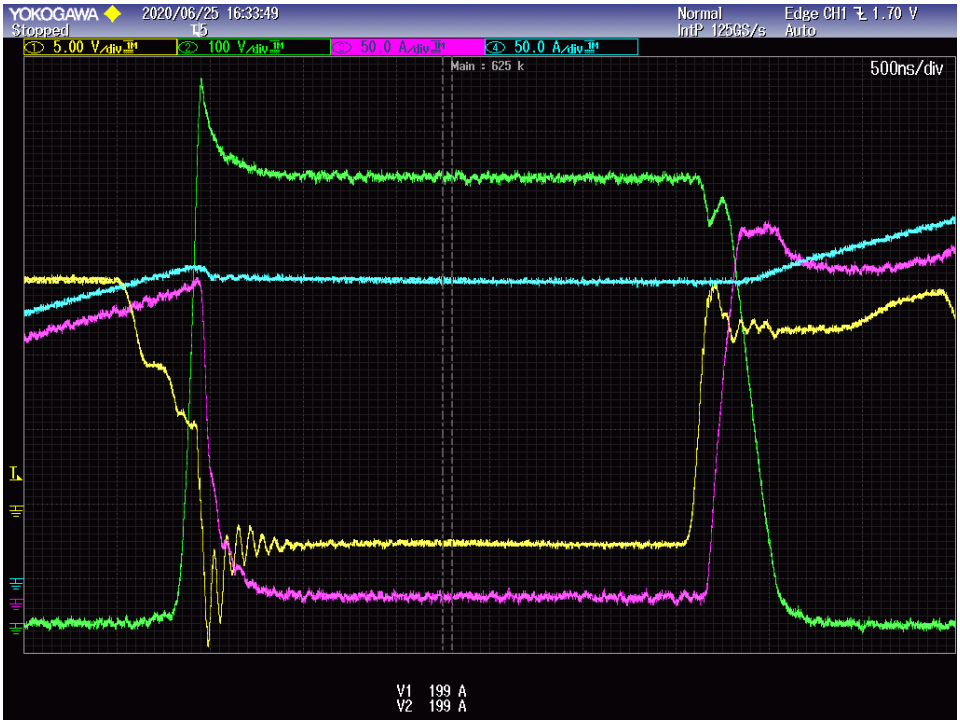


Figure 5.9: The Double Pulse Test Waveform of Si IGBT Switch at 125C for 200A. Channel 1 (yellow): gate voltage v_{ge}; Channel 2(green): switch voltage v_{ce}; Channel 3(magenta): switch current i_{sw};Channel 4(cyan): gate voltage i_L.

occur due to the circuit parasitic inductances and output capacitances respectively. Ringing in current at turn-on and turn-off is due to the resonance of the parasitic inductance and capacitance. Furthermore, the current tail can be observed at the end of turn-off as the switch current goes to zero slowly. The switching losses measured at different temperatures can be seen in Figure 5.10. As discussed in chapter 2, IGBT switching losses are influenced by temperature. As temperature increases, it takes longer for the IGBT to transport excess carrier. The switching losses' dependency on temperature is supported by the experimental results. With the temperature increasing from 25°C degrees to 125°C, both turn-on and turn-on losses increase by about 37%. As the temperature increases during the EV driving profile, it is important for the hybrid switch to reduce switching losses of the IGBT using optimal switching strategy.

In Table 5.2, the measured switching losses are compared with the ones in the datasheet. These datasheet values are scaled to the matching gate resistance and temperature. At low current, the losses difference is higher possibly due to the fact that the magnitude of noise is relatively high compared to the current. Also, the power capability of the gate driver used in the test influence considerably the switching losses, and in both cases they are different.

Temp [C]	Current [A]	Measured Eon [mJ]	Datasheet Eon [mJ]	Difference %	Measured Eoff [mJ]	Datasheet Eoff [mJ]	Difference %
25	20	2.739	2.674	+2	1.473	1.807	-18
	160	13.688	14.12	-3	9.011	8.576	+5
75	20	3.78	3.012	+25	1.505	2.275	-34
	160	16.54	15.91	+4	10.49	10.79	-3
125	20	4.658	3.476	+34	1.682	2.742	-39
	160	18.88	18.35	+3	12.29	13.01	-6

Table 5.2: Comparison between measured value and datasheet value of the IGBT switching Losses.

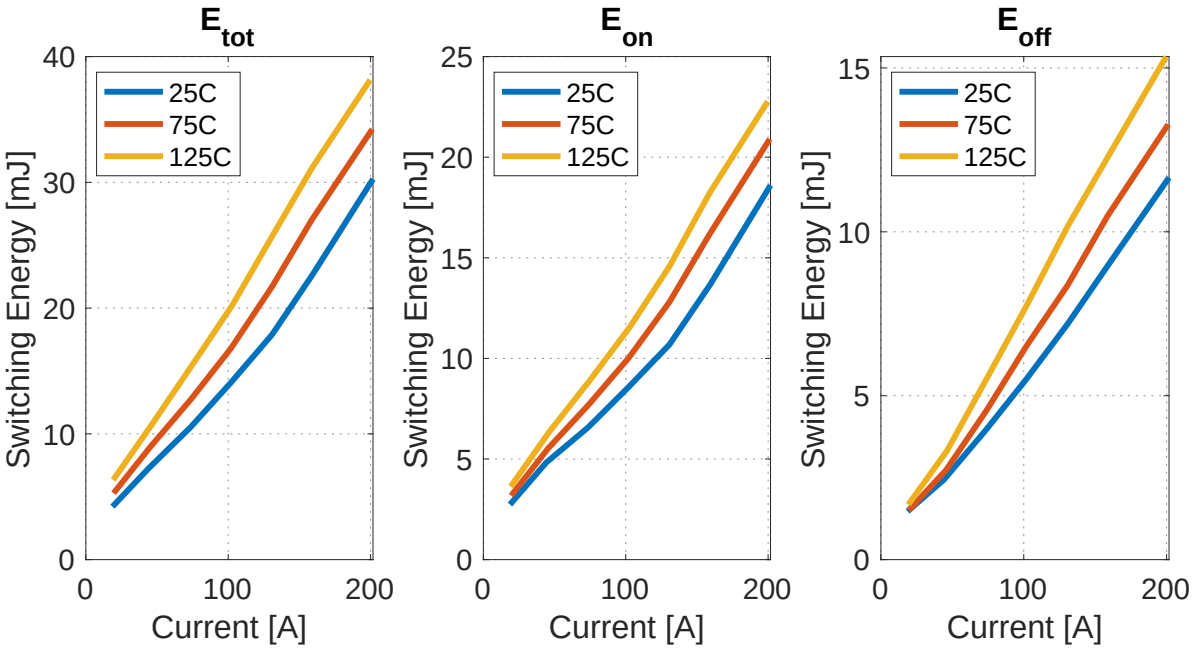


Figure 5.10: The IGBT switching losses at 25°C, 75°C and 125°C.

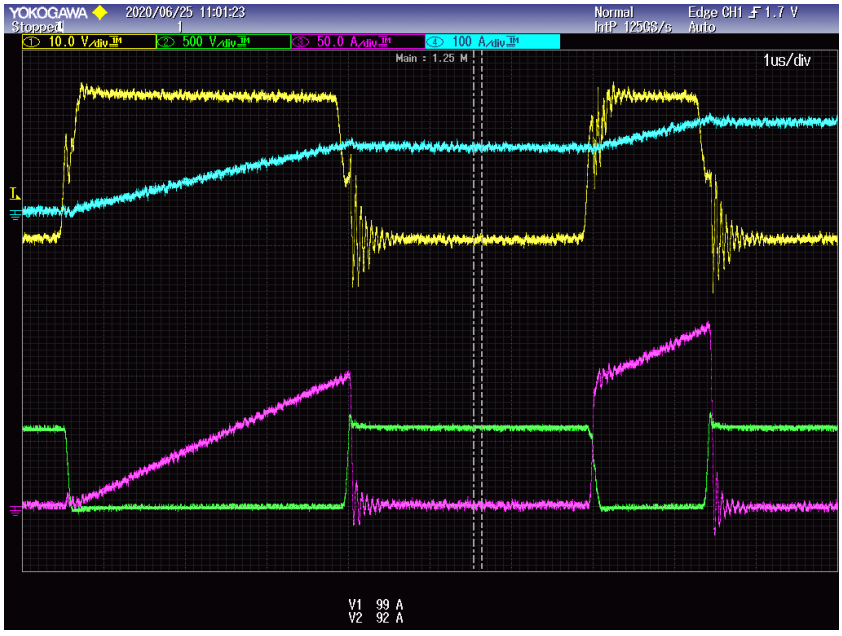


Figure 5.11: The Double Pulse Test Waveform of SiC MOSFET Switch at 25C for 100A. Channel 1 (yellow): gate voltage v_{gs}; Channel 2 (green): switch voltage v_{ds}; Channel 3(magenta): switch current i_{sw};Channel 4(cyan): gate voltage i_L.

5.2.2. Pure MOSFET Switch

The double pulse test waveform of SiC MOSFET Switch can be seen in Fig 5.11. The non-ideal behaviour described in chapter 2 can again be observed in a manner similar to the IGBT, with the exception of a current tail absence. The MOSFET switching losses are compared at different temperatures in Fig 5.12. As discussed in chapter 2, MOSFET switching losses are not strongly dependent on temperature. The independency to temperature is supported by the experimental result. For this reason, the measured switching losses are compared to the datasheet values only at 25°C (Table 5.3). The higher switching losses from the datasheet values are potentially due to gate voltage, which is 18V/0 in the datasheet instead of 18V/-4V in the experiment. The MOSFET has shown to have significantly

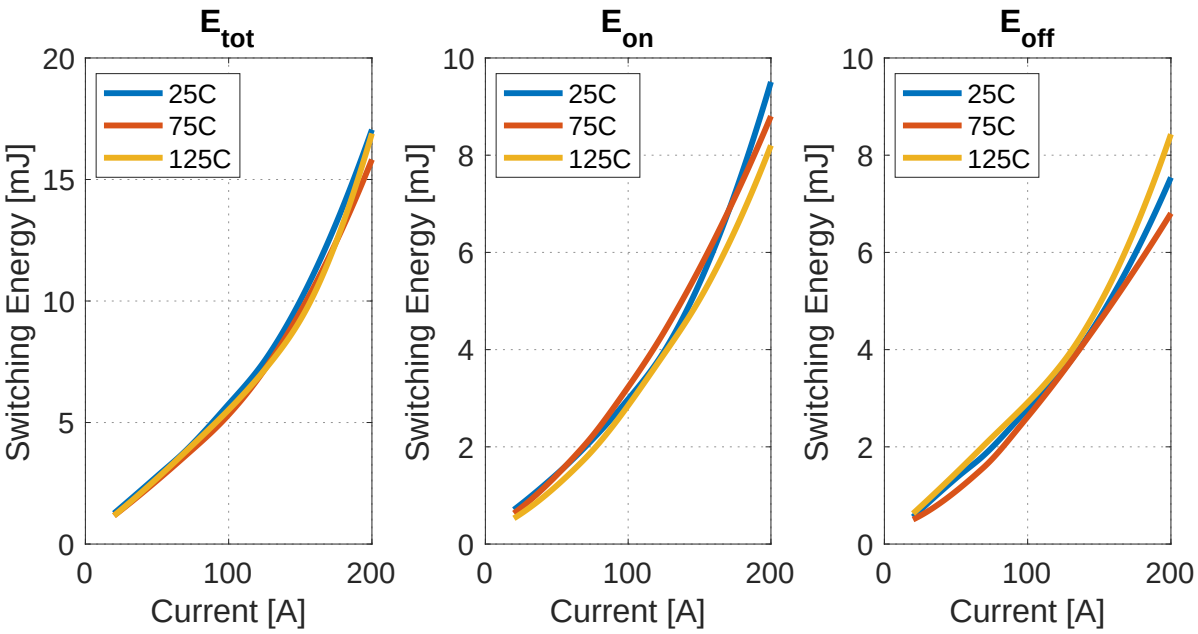


Figure 5.12: MOSFET switching losses at different temperatures.

lower switching losses than the IGBT and is less prone to higher switching losses due to temperature increase. This again demonstrates the importance of using the MOSFET to turn on and off the hybrid switch for reduction of switching losses.

Temp [C]	Current [A]	Measured Eon [mJ]	Datasheet Eon [mJ]	Difference %	Measured Eoff [mJ]	Datasheet Eoff [mJ]	Difference %
25	50	1.466	1.82	-19	1.38	1.457	-5
	180	7.6	10.1	-25	6.223	9.195	-32

Table 5.3: Comparison between measured value and datasheet value of the MOSFET switching Losses.

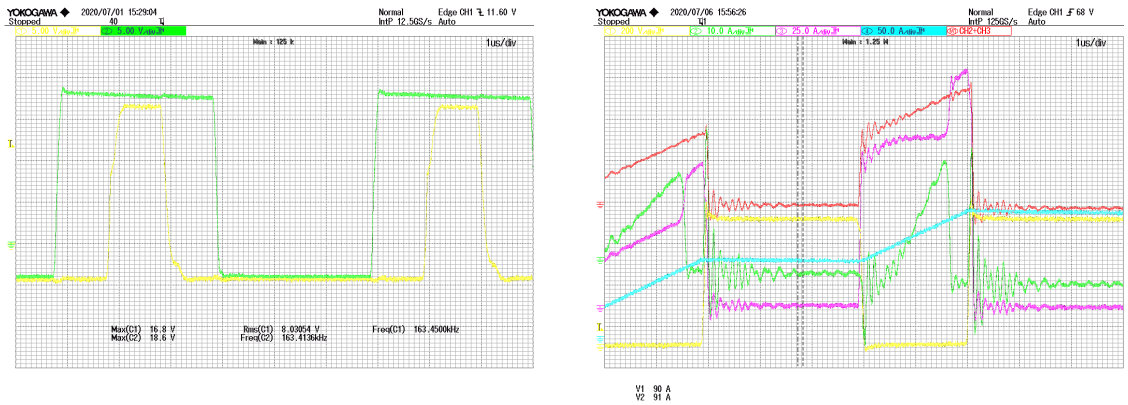
5.2.3. Hybrid Switch

The double pulse test waveform of the hybrid switch and its gate signals can be seen in Figure 5.13. The hybrid switch is tested with different gate delays between IGBT and MOSFET for both turn-on and turn-off. For each test, the turn-on and turn-off delay is set to the same value. It is important to note that the MOSET and the IGBT are driven by two separate gate drivers, the minimum delay between the switch is 50ns. In Figure 5.13, the IGBT is turned on 500ns after and turned off 500ns before MOSFET. The MOSFET takes on the entire load current after the IGBT is turned off and before the IGBT is turned on. The current of the hybrid switch has some ringing due to the parasitic inductance connecting the IGBT and MOSFET discrete components.

The turn-on and turn-off waveform can be further examined in Figure 5.14. During turn-on and turn-off, the IGBT current seems to have negative dip and positive dip respectively as the voltage changes. This is caused by the output capacitances as it discharges and charges due to the change in voltage as discussed in chapter 2.

From chapter 2, it is expected that turn-on and turn-off delays would affect the switching losses significantly. Minimal turn-on loss occurs with no turn-on delay. For turn-off, an optimal delay time that minimizes both conduction loss of the MOSFET and IGBT turn-off loss should be chosen.

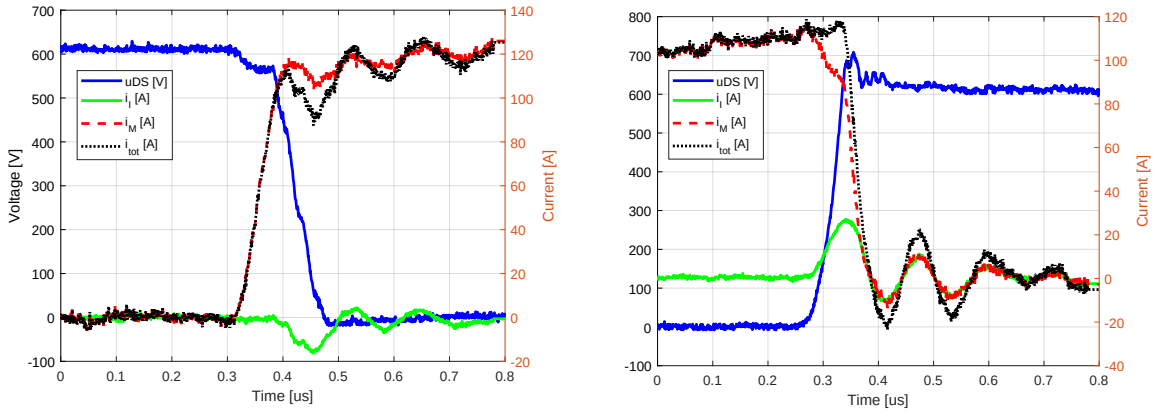
As a comparison, Figure 5.15 shows the switching waveforms of hybrid switch with a 200ns switching delay. It can be seen that the turn-on waveform is nearly identical to that of 500ns. For turn-off, the IGBT is not fully turned off within the the 200ns delay time, which results in higher turn-off loss. In Figure 5.16, the turn-on and turn-off losses are compared at different currents. It can be seen that



(a) The Gate signal of the IGBT (yellow) and MOSFET (green).

(b) The switch voltage (yellow), IGBT current (green), MOSFET current (magenta) and the inductor current (cyan).

Figure 5.13: The DPT waveforms of the hybrid switch with 500ns gate delay.



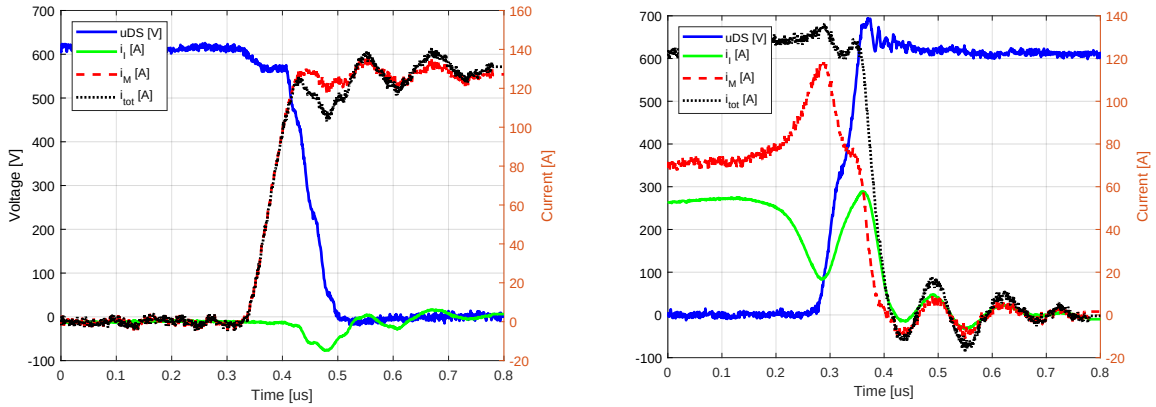
(a) The turn-on waveform

(b) The turn-off waveform

Figure 5.14: The switching waveforms of the hybrid switch with 500ns gate delay. The switch voltage (blue), IGBT current (blue), MOSFET (red) and the total switch current (black)

the turn-on loss only decreases at near zero delays and does not change much between 200ns to 1us. As the delay increases to 1us, the turn-off loss decreases. By varying the turn-off delay, a compromise between switching losses and the MOSFET conduction losses during the turn-off is made. The conduction energy loss of the MOSFET during turn-off before turning on IGBT can be expressed using Equation (5.2). As seen in Figure 5.17 (a): as the delay increases, the MOSFET conduction loss would increase as well while the switching loss decreases. Figure 5.17 (b) shows that as conduction energy loss increases as switch current increases. This signifies that at different current levels, the optimal turn-off delay varies. Furthermore, a current-dependent feedback control strategy can be used to ensure optimal switching during inverter operation. From chapter 2, similar trends can also be seen in Figure 2.8 and 2.11.

$$E_{cond,MOS} = t_{d,off} \cdot R_{ds} \cdot \hat{I}_{ac}^2 \tag{5.2}$$



(a) The turn-on waveform (b) The turn-off waveform

Figure 5.15: The switching waveforms of the hybrid switch with 200ns gate delay.

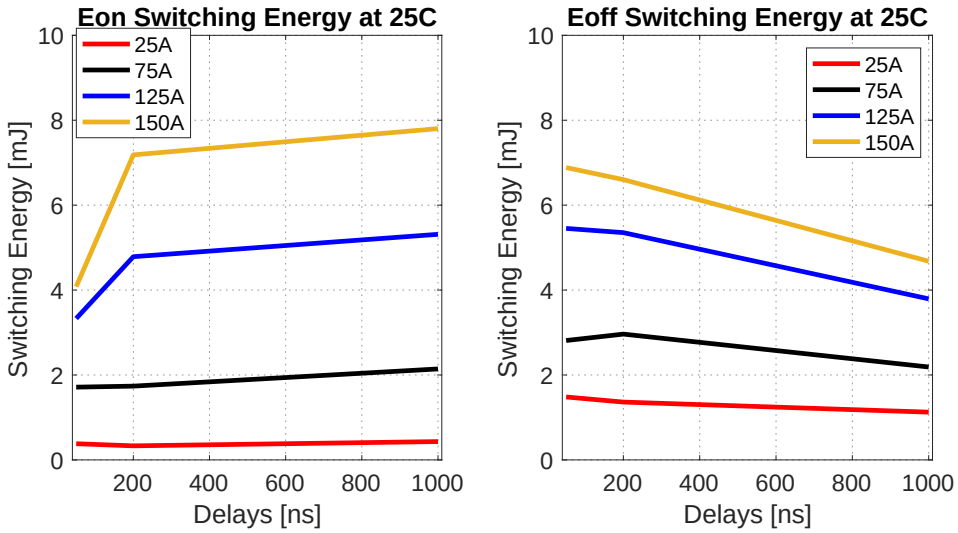


Figure 5.16: Comparison of turn-on and turn-off loss with different gate delays at 25C.

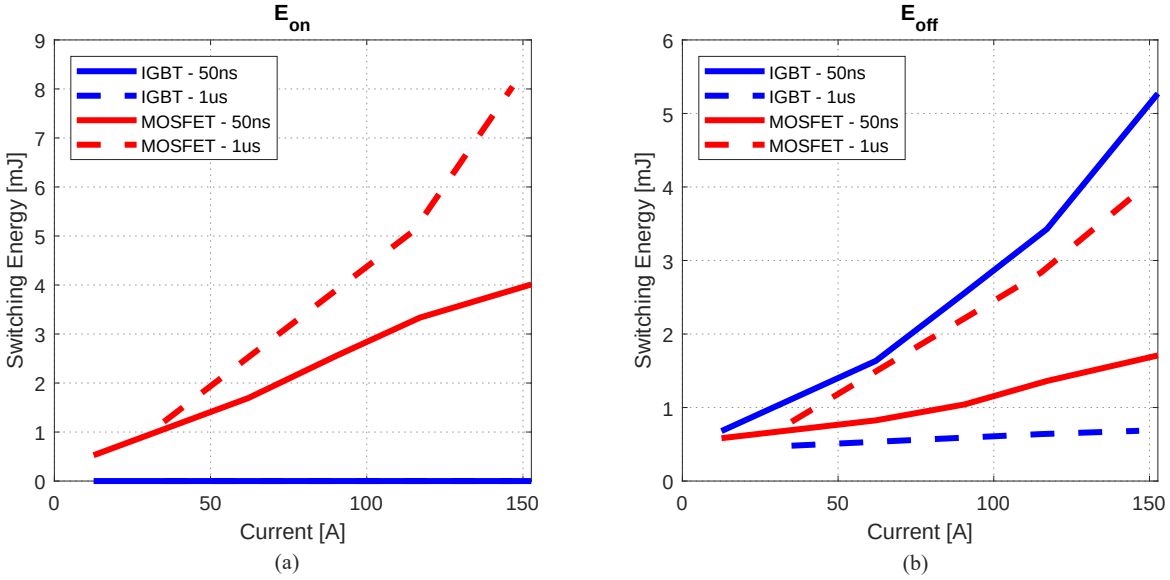
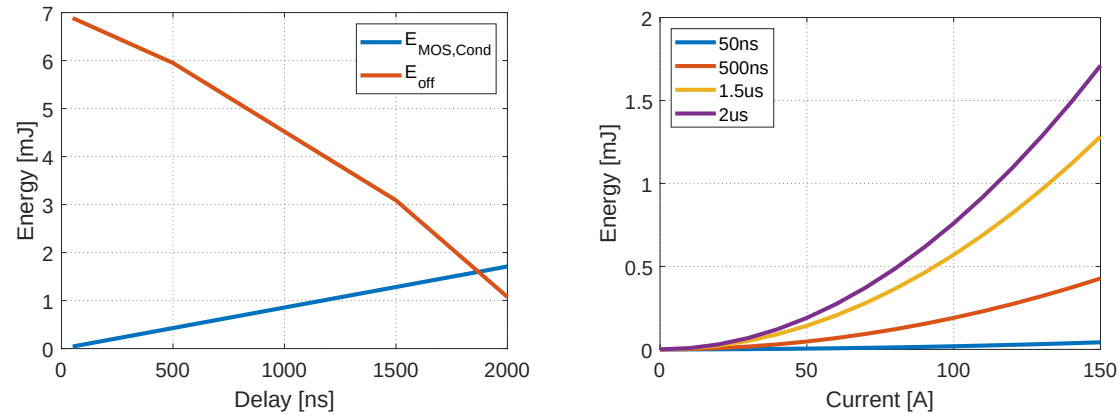
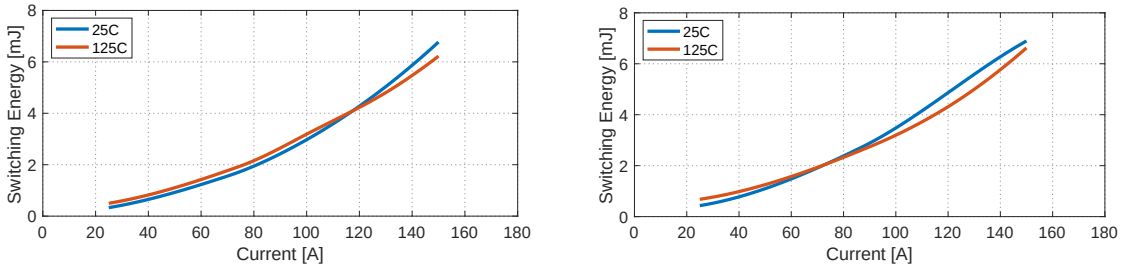


Figure 5.18: The losses of the individual component in the hybrid switch. (a) the turn-on losses and (b) the turn-off losses with both 50ns and 1us switching delay.



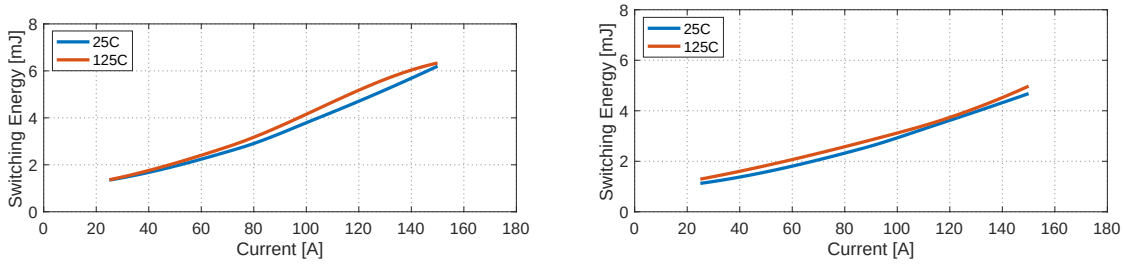
(a) (b)

Figure 5.17: The trade off between turn-off losses and MOSFET conduction losses. (a) turn-off switching energy (red) vs MOSFET conduction energy during the switching (blue) as a function of switching time at 150A, (b) MOSFET conduction energy during switching as a function current at different delays (50ns-blue, 500ns-red, 1.5us-yellow, 2us-purple).



(a) The turn-on loss with 200ns delay (b) The turn-on loss with 1us delay

Figure 5.19: The turn-on loss of the hybrid switch with different temperatures.



(a) The turn-off loss with 200ns delay (b) The turn-off loss with 1us delay

Figure 5.20: The turn-off loss of the hybrid switch with different temperatures.

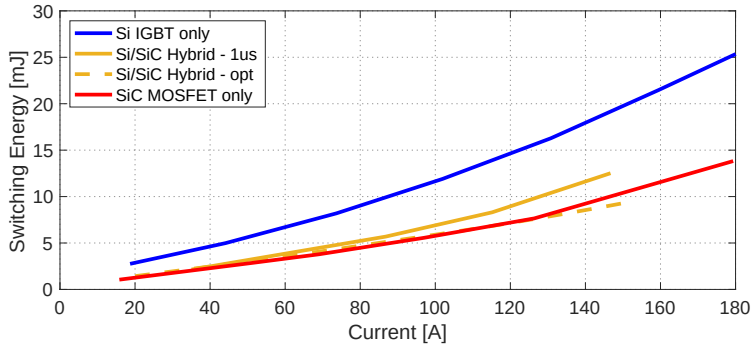
In Figure 5.18, the individual switching energy of IGBT and the MOSFET in the hybrid switch is shown. It can be seen that the turn-on losses of the MOSFET is reduced at lower turn-on delay. This is due to the fact that, while providing ZVS to the IGBT, less time is spent for the MOSFET to conduct by itself during the turn-on period. For turn-off, majority of losses transfers from the IGBT to the MOSFET as the delay increases. This is expected as IGBT would have enough time to turn off with a longer turn-off delay.

As explained in chapter 4, the switching losses are more dependent on the temperature if the IGBT is more involved. This means that with lower switching delay, a higher temperature results in higher switching losses. In Figure 5.19 and 5.20, the turn-on and turn-off losses at different temperature are compared with 200ns and 1us switching delay. The graphs do not show the strong dependence on

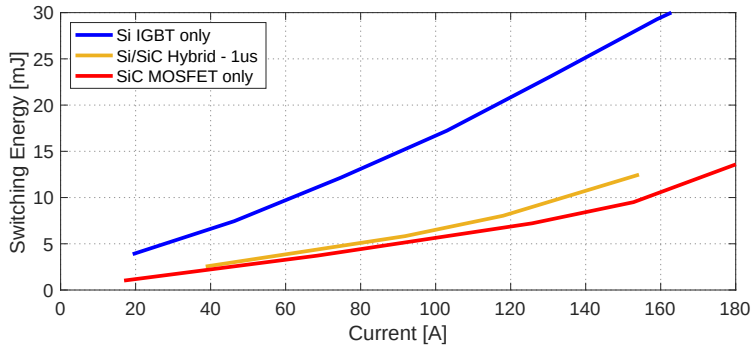
temperature. This means even at 200ns, the IGBT switching loss' dependency on temperature is not prominent in the hybrid switch.

5.2.4. Switching losses comparison

In Figure 5.21, the pure IGBT and the pure MOSFET switches are compared with the hybrid switch. For the hybrid switch, the total switching loss with 1us delays is used as it is the lowest among all the other delays. In addition, hybrid switch switching loss using a 50ns turn-on and 1us turn-off delay is plotted. Since this plot is interpolated from the two delay data points, this might be the reason why at 150A, the optimal switching loss for the hybrid is lower than the pure MOSFET switch. Note that the switching losses with 50ns switching delay is only recorded at 25°C, thus only the switching losses of the hybrid switch with 1us delay is considered at 125°C. All in all, it is demonstrated that the hybrid switch switching loss is lower than the IGBT which proves that is a great compromise between the pure Si IGBT and the pure SiC MOSFET solutions. Furthermore, this trend holds true for both 25°C and 125°C.



(a) 25°C



(b) 125°C

Figure 5.21: The total switching losses of the pure Si IGBT (blue), pure SiC MOSFET (red), and hybrid switch (yellow) at different temperatures.

5.3. Single Pulse Resistive Test for Static Characterization

To measure the on-state characteristics of the switches, the switch's voltage and current during a single longer pulse (10us) are recorded. In terms of test setup, everything remains the same except that parallel resistors are used in place of the test inductor (Figure 5.22). Temperature is again controlled using the heating resistor and monitored by the NTC Thermistor to measure the three temperature points listed in Table 5.1.

5.4. Comparison of on-state Characteristics

The Single Pulse Test waveform of all three configurations are shown in Figure 5.23. To determine the on-state characteristics, the voltage and current of each switch are taken between 1us after turn-on and right before turn-off. This would eliminate the effect of noise and overshooting due to switching.

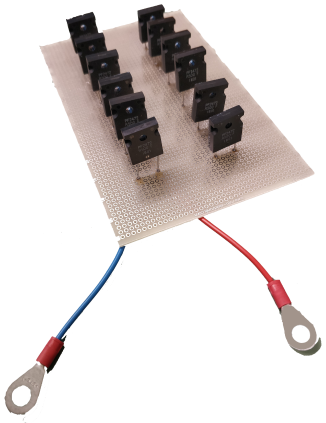
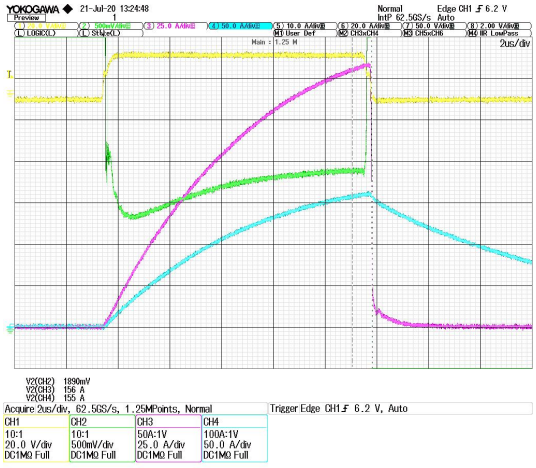
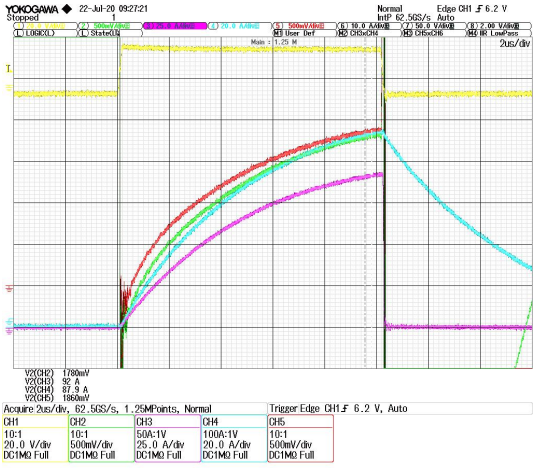


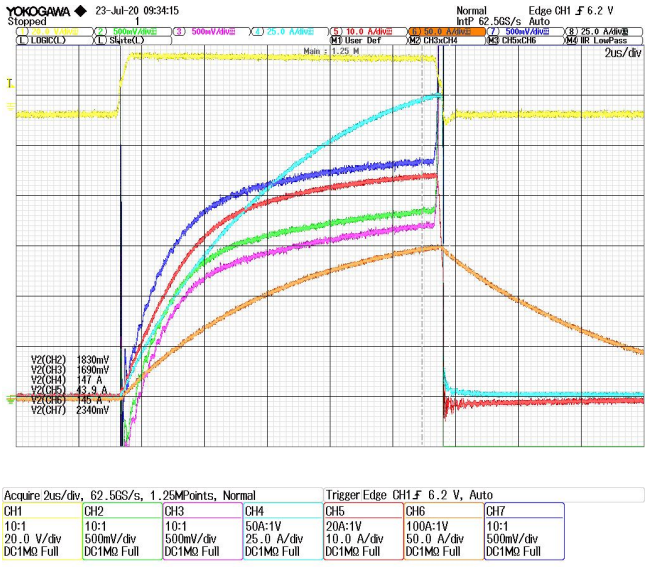
Figure 5.22: Parallel resistors used in place of test inductor for the load for the sinple pulse test.



(a) IGBT. Channel 1 - Gate signal (yellow), Channel 2 - Switch voltage (green), Channel 3 - Switch current (magenta), Channel 4 - Inductor current (cyan)



(b) MOSFET. Channel 1 - Gate signal (yellow), Channel 2 - Switch voltage (green), Channel 3 - Switch current (magenta), Channel 4 - Inductor current (cyan)



(c) Hybrid. Channel 1 - Gate signal (yellow), Channel 2 - MOSFET voltage (green), Channel 3 - IGBT voltage (magenta), Channel 4 - Total switch current (cyan), Channel 5 - MOSFET current (red), Channel 6 - Resistor current (orange), Channel 7 - midpoint voltage (purple)

Figure 5.23: The SPT waveforms for all three configurations.

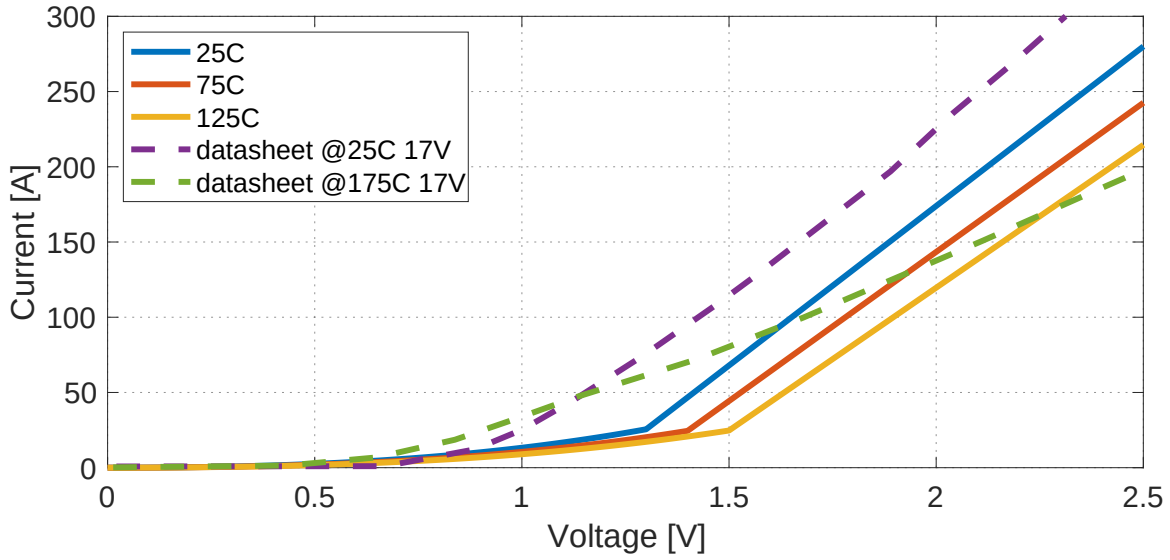


Figure 5.24: On-state Characteristics of the Pure IGBT switch compare to its datasheet values.

5.4.1. Pure IGBT Switch

The on-state characteristics of the IGBT switch is shown in Figure 5.24. The curve of the switch including the PN junction barrier potential is intepolated using MATLAB function PCHIP. The IGBT on-state characteristics are less ideal compared to its datasheet value. As a result, the hybrid switch would have relatively higher conduction loss than expected, especially during high current situation.

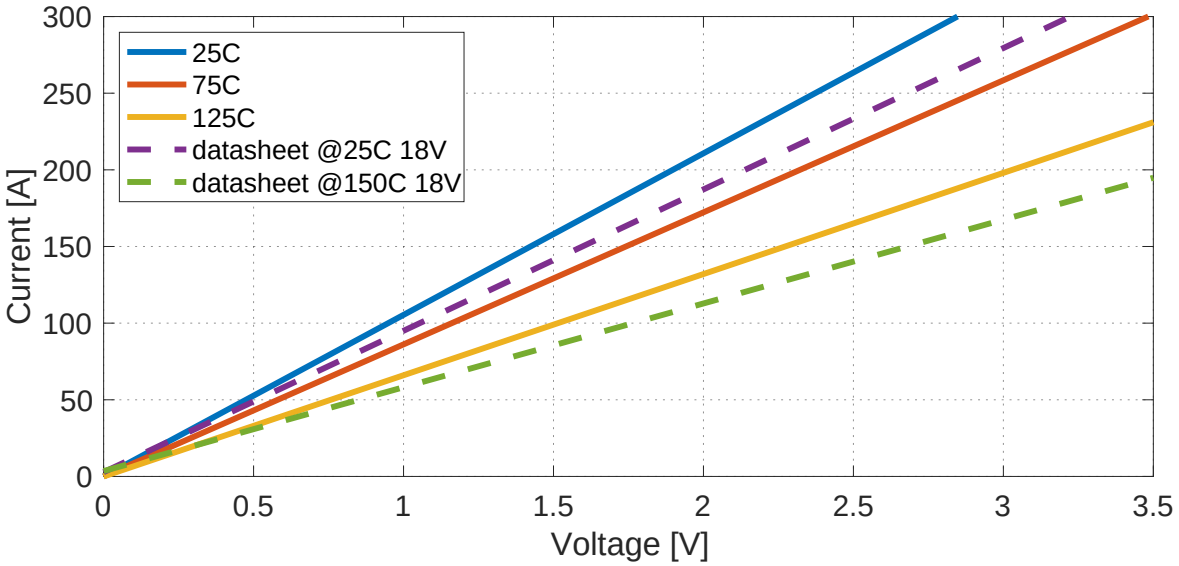


Figure 5.25: On-state Characteristics of the Pure MOSFET switch compare to its datasheet values.

5.4.2. Pure MOSFET Switch

The on-state characteristics of the MOSFET switch is shown in Figure 5.25. Unlike the IGBT, the MOSFET's experimental on-state characteristics are very similar to its datasheet values.

5.4.3. Hybrid Switch

In Figure 5.26 and 5.27, the hybrid switch experimental values are compared with its on-state characteristics extracted from the datasheet values and the experimental values of the SiC MOSFET switch as well as the Si IGBT. The measured hybrid switch on-state voltage are higher than the expected values. This is likely due to the parasitic inductances within the testing setup.

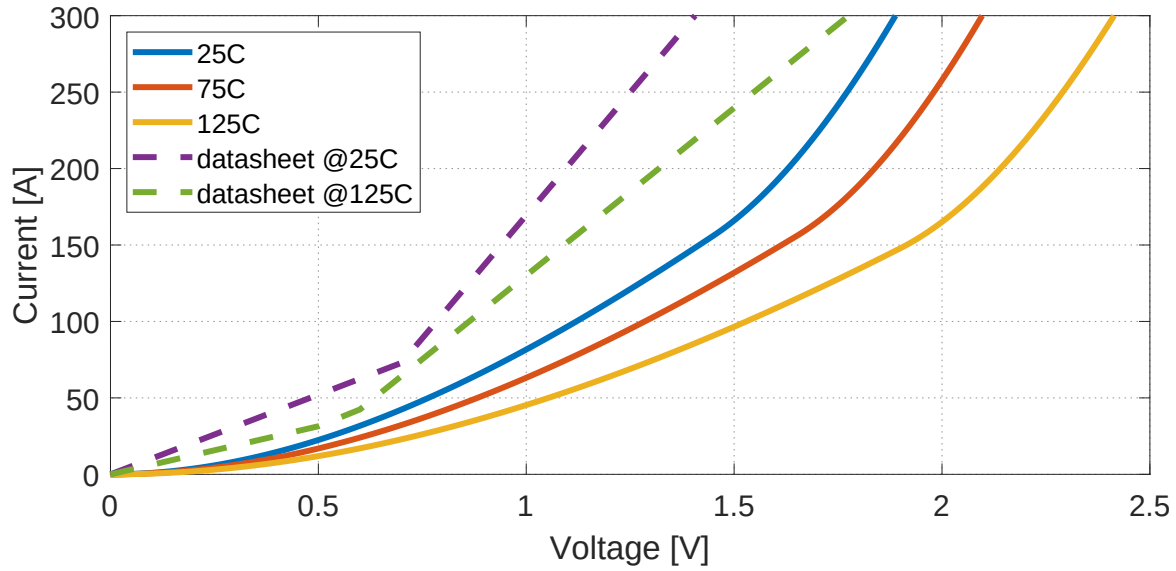


Figure 5.26: On-state Characteristics of the Hybrid switch compare to its datasheet values.

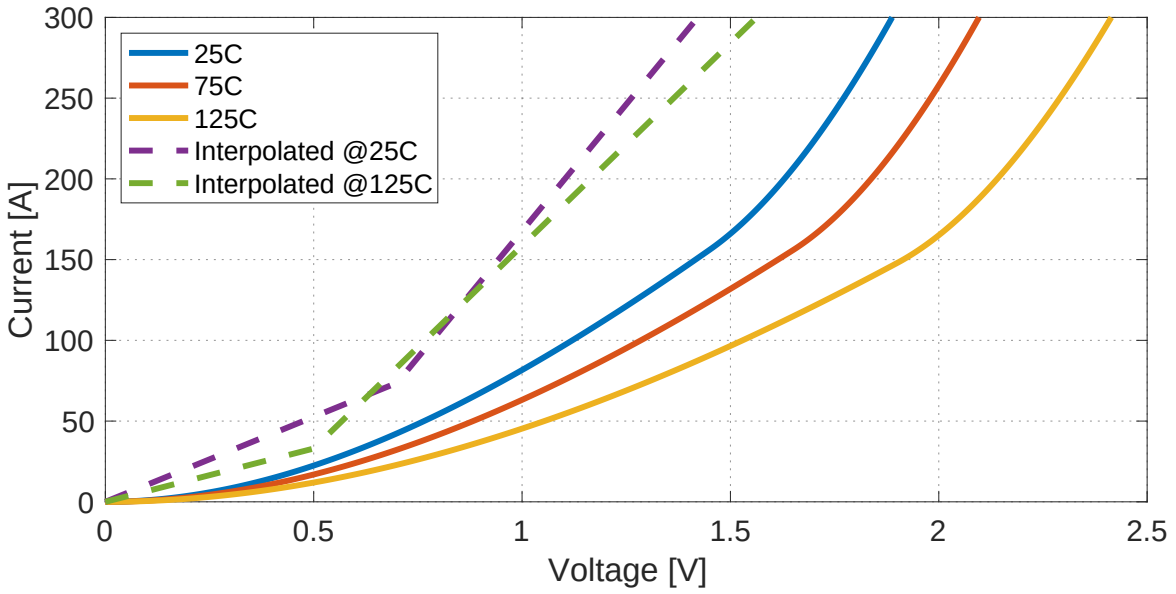


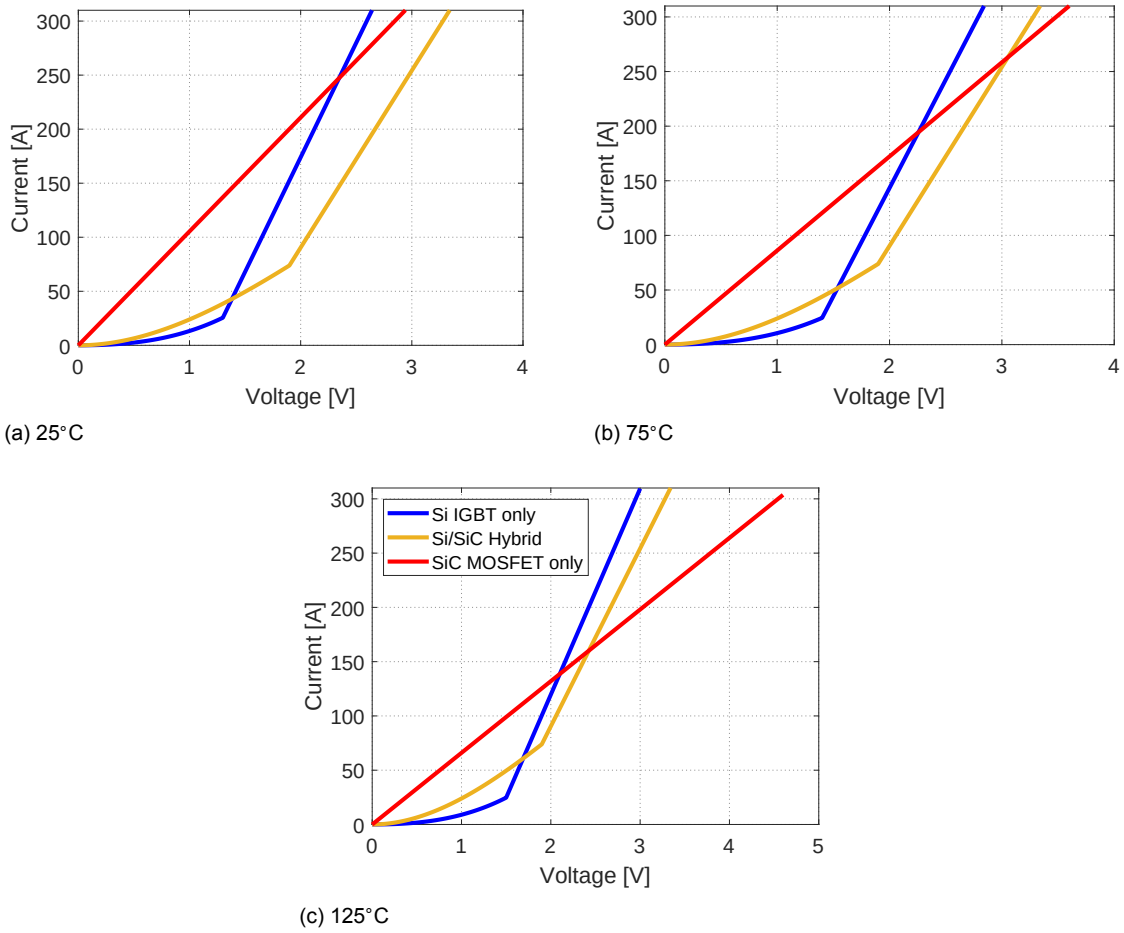
Figure 5.27: On-state Characteristics of the hybrid switch compare to interpolated values from pure IGBT and MOSFET data.

5.4.4. On-state characteristics comparison

The on-state characteristics of all three configurations at 25°C and 125°C are shown in Figure 5.28. Note that the three configurations are scaled so that the switch current rating is 300A. At both 25°C and 125°C, the hybrid switch performs better than the IGBT at low current. For high current, the hybrid switch performs better than MOSFET. This is especially obvious at 125°C. The experimental results of the on-state characteristics follow the expected trend discussed in chapter 4.

5.4.5. Current sharing of the hybrid switch

As mentioned in chapter 4, the current sharing of the hybrid switch changes as temperature varies. This is due to the fact that the IGBT and MOSFET have different temperature coefficient. The current sharing of the hybrid switch is shown in Figure 5.29. As temperature increases, the MOSFET conducts less current while the IGBT conducts more. This means that the MOSFET has higher temperature coefficient than the IGBT. Higher temperature is usually a result of high current across the switch.



(a) 25°C (b) 75°C

(c) 125°C

Figure 5.28: On-state Characteristics of all three configurations at different temperatures.

Since the IGBT has a lower on-state resistance than the MOSFET at high current, it is advantageous to have the hybrid switch conduct more current with IGBT at high temperature.

5.4.6. Cross temperature measurement of the hybrid switch

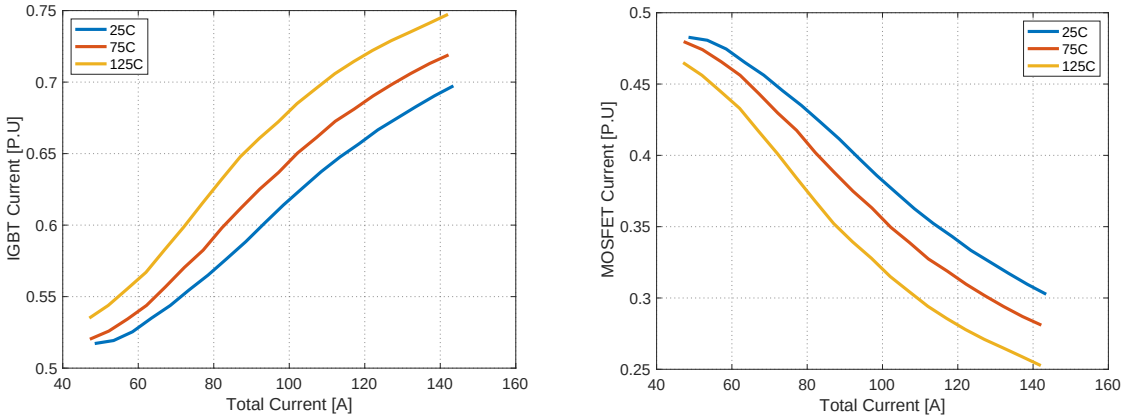
As the IGBT and MOSFET have different temperature coefficient, the change in their on-state behavior due to temperature differs. In an Electric Vehicle traction inverter setting, the configuration (module vs discrete) and the placement of the switch (relative to heatsink or other components) can cause a difference in temperature between the two devices. By understanding the cross temperature difference, the hybrid switch inverter can be designed to further reduce conduction loss.

To measure the cross temperature effect, the Single Pulse Test is performed with the IGBT and the MOSFET of the hybrid switch on different arms. This way, temperature can be controlled separately. However, this results in higher parasitic inductance, which in turn creates a voltage drop between the two arms. Consequently, the on-state characteristics measured with this test would be lower than the ones measured with the single arm setup used so far. Figure 5.30 shows the hybrid switch circuit with the parasitic inductances. Using Equation (5.3) and (5.4), the lumped IGBT and MOSFET branch parasitic inductances are calculated to be $39.7nH$ and $38.3nH$ respectively. These inductances results in the differences in voltage shown in 5.31.

$$L_{par,I,lumped} = L_{par,I1} + L_{par,I2} + L_{par,mid} = (V_{mid} - V_{IGBT}) \cdot \frac{dt}{di} \tag{5.3}$$

$$L_{par,M,lumped} = L_{par,M1} + L_{par,M2} + L_{par,mid} = (V_{mid} - V_{MOSFET}) \cdot \frac{dt}{di} \tag{5.4}$$

The on-state characteristics of the hybrid switch with the cross temperature test is shown in Figure



(a) Per unit of current flowing through IGBT

(b) Per unit of current flowing through MOSFET

Figure 5.29: Current sharing of the hybrid switch.

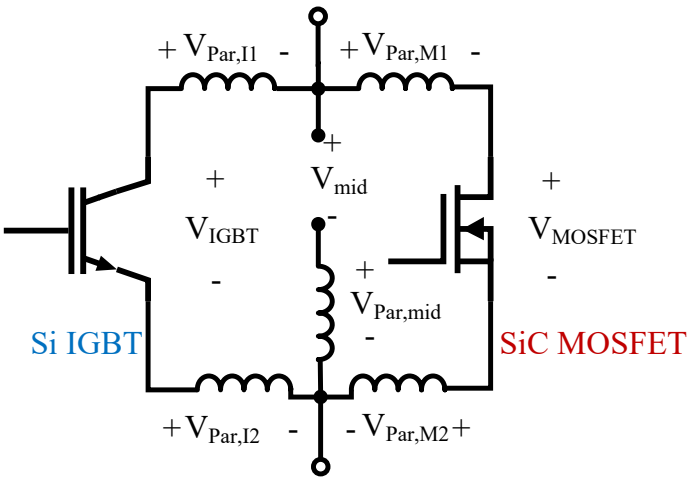


Figure 5.30: The hybrid switch with the parasitic inductances.

5.32. The first row of graphs varies the temperature of the MOSFET at each IGBT temperature point and vice versa for the second row. The on-state characteristics of the hybrid switch have a larger variance with temperature change of the MOSFET than the IGBT. This is again due to the fact that the temperature coefficient of the MOSFET is higher than the IGBT. As the temperature increases, the on-state performance of the MOSFET deteriorates faster than the IGBT. This further support the trend observed in current sharing, where as the temperature increases, more current is conducted by the IGBT. In addition to the thermal stress, the higher variance of on-state characteristics due to temperature should be considered when evaluating the trade off between the current ratio and cost of the MOSFET and the IGBT.

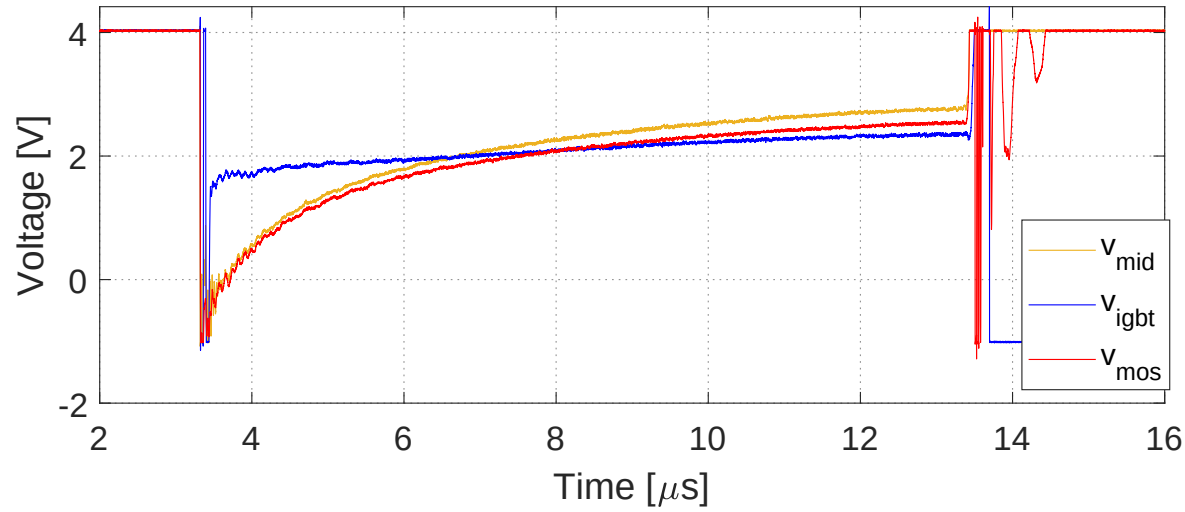


Figure 5.31: The voltage of the IGBT, the MOSFET and the midpoint of the Hybrid Switch.

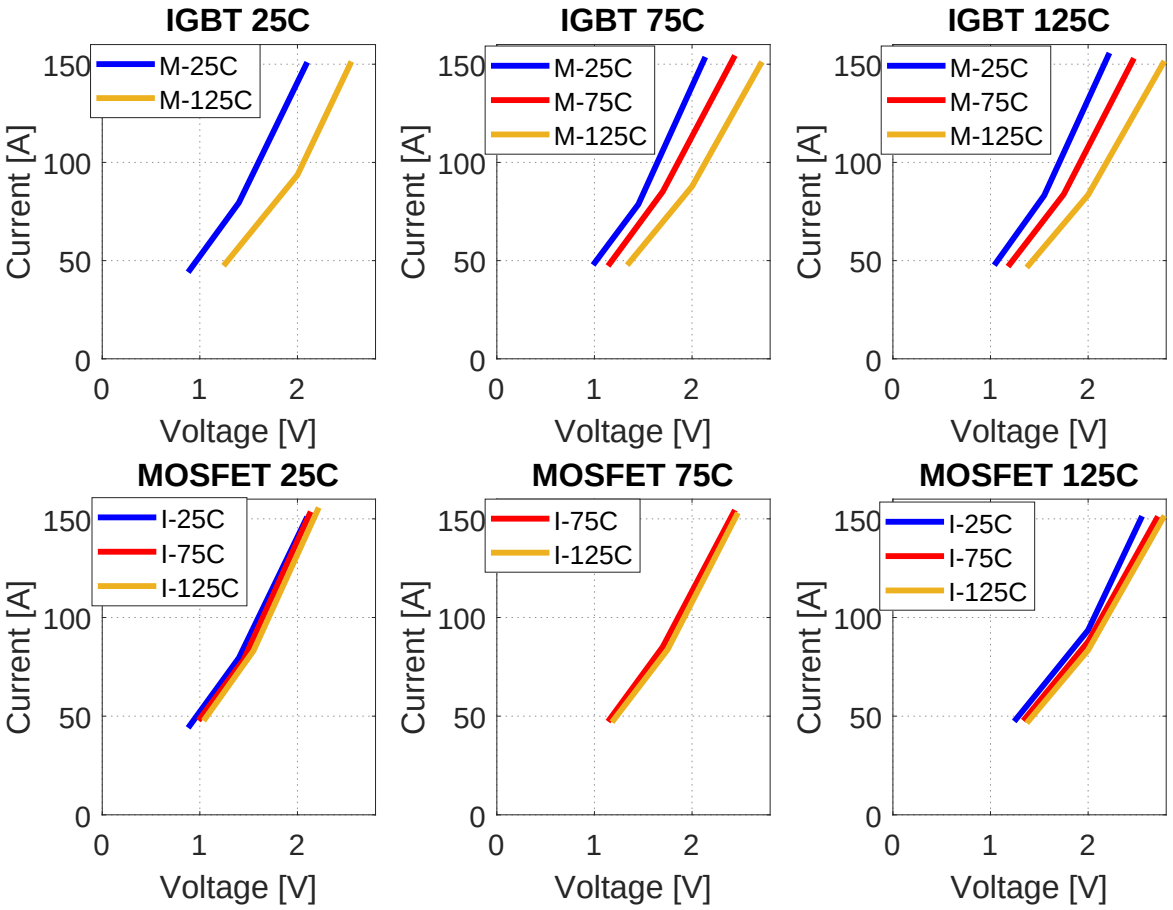


Figure 5.32: On-state characteristics of the hybrid switch cross temperature.

6

Electric Vehicle Traction Inverter Simulation

Using the switch characteristics determined from chapter 4 and chapter 5, the efficiency of the EV traction inverter is evaluated both at static load and over a standardized driving cycle. Instead of using only the Si IGBT shown in Figure 1.1, the three-phase two level EV inverter uses three switch configurations discussed in previous sections. The loss coefficient models are displayed in Table 4.1. It is also important to note that the hybrid switch compared in this section uses IGBT without diode. Thus, the MOSFET is used for reverse conduction.

6.1. Efficiency over Static Load Conditions

At static load, the efficiency of each switch inverter configuration is evaluated from 10% load to full load and the junction temperature is set to 125°C, which is a common temperature for an EV traction inverter [32]. The efficiency is calculated using the equations described in chapter 3. The modulation index is chosen to be 0.5, the switching frequency is 5000Hz and the fundamental frequency phase shift between the voltage and current is set to 0. The parameters of the IGBT and the MOSFET used are listed in Table 6.1. For the datasheet parameters, the values are scaled using Equation (3.8),(3.9) and (3.12) at 125°C. The static efficiency as a function of output power using the datasheet and experimental values can be seen in Figure 6.1. The efficiency variation between the experimental and the datasheet values are mainly due the difference in on-state performance as seen in Figure 5.24, 5.25 and 5.26. With the experimental values, the hybrid switch has a lower efficiency while the efficiency of the pure IGBT near full load is slightly higher.

Device	Symbol	Datasheet Value	Experimental Value
IGBT	[b2, b1, b0] for IGBT turn off	[2.52e-6, 3.89e-5, 0]*	[1.22e-7, 8.135e-5, 0]**
	[b2, b1, b0] for turn off	[-7.47e-7, 1.46e-4, 0]*	[1.02e-8, 7.51e-5, 0]**
	R_{ce}	0.02	0.02
	V_{ce}	0.59	0.59
Diode	[b2, b1, b0] for Reverse Recovery	Included with IGBT	[2.14e-8, -8.43e-7, 0]**
	R_f	0.0165	0.0165
	V_f	1.16	1.16
MOSFET	[b2, b1, b0] for turn on	[3.81e-7, 5.97e-6, 0]*	[1.20e-7, 1.63e-5, 0]**
	[b2, b1, b0] for turn off	[1.91e-7, 1.34e-4, 0]*	[1.47e-7, 9.88e-6, 0]**
	$R_{ds,on}$	0.052	0.047
Hybrid	[b2, b1, b0] for turn on	[3.81e-7, 5.97e-6, 0]*	[4.38e-8, 2.08e-5, 0]**
	[b2, b1, b0] for turn off	[1.91e-7, 1.34e-4, 0]*	[-3.23e-8, 3.67e-5, 0]**

Table 6.1: Parameters used for the static simulation.
*switching losses parameter per device
**switching losses parameter for four devices in parallel

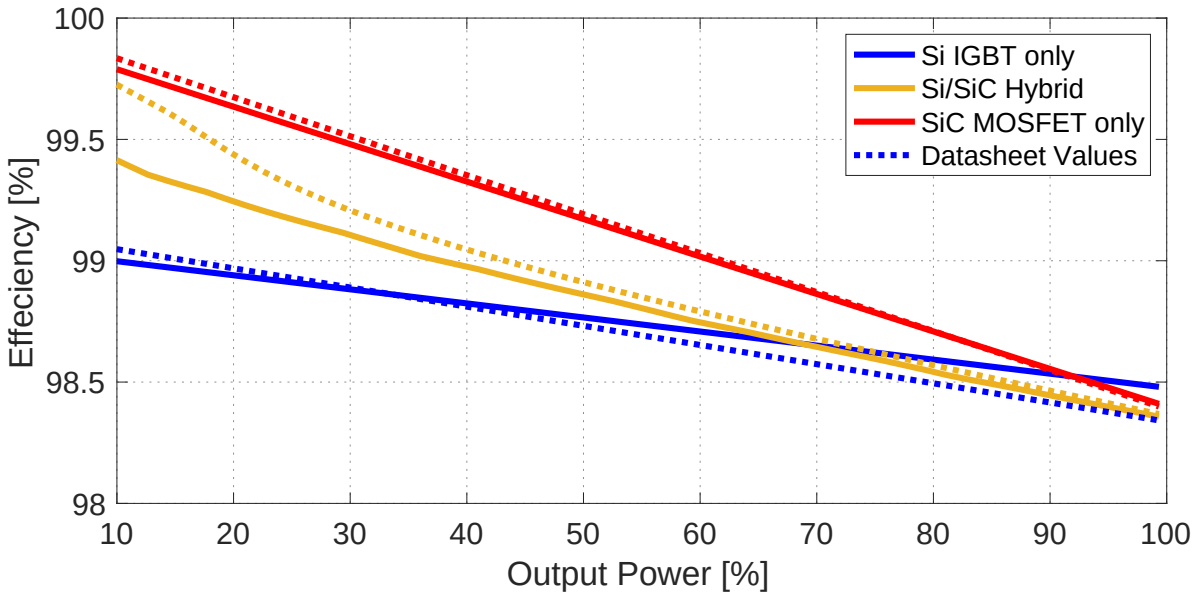
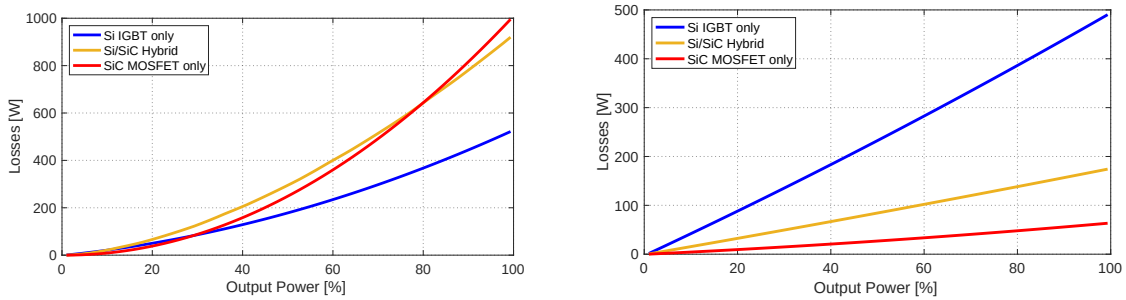


Figure 6.1: Efficiencies of the pure SiC MOSFET (red), the pure Si IGBT (blue) and the Hybrid Switch inverter (yellow) as a function of output power. The efficiencies of the experimental and datasheet values are represented by the solid and dotted lines respectively.

As expected, the pure Si IGBT inverter is shown to have the lowest efficiency at low load. It can also be observed that the hybrid switch benefits from the high efficiency of the MOSFET features at low load. As the load increases, the IGBT part of the switch has a more prominent effect on the switch's efficiency. This is mainly a result of the current sharing between the IGBT and MOSFET. As shown in Figure 5.29, the IGBT conducts more than 70% of the load current at 125°C near full load.



(a) Conduction Losses (b) Switching Losses

Figure 6.2: The (a) conduction and (b)switching losses of all three configurations as a function of current using experimental data.

In Figure 6.2, the conduction and switching losses as a function of load current determined using experimental data are shown for all three configurations. It can be seen that conduction losses of the MOSFET and the hybrid switch inverter are overall higher than the switching losses. For the IGBT inverter, switching losses becomes more prominent. Although the IGBT has better on-state performance at high current, the switching losses of the MOSFET and the hybrid switch are so low that they compensate for the higher conduction losses. The hybrid switch inverter has the similar efficiency to the MOSFET near full load.

6.2. Efficiency over Driving Cycles

The static load efficiency evaluation shows that the hybrid switch inverter is more efficient than the pure Si IGBT inverter for partial load under 65%. In this section, it will be demonstrated that greater efficiency under 65% load is advantageous for the hybrid switch inverter. This will be done by simulating the EV over standardized driving cycles.

6.2.1. Electric Vehicle Traction Inverter Simulation Setup

The process of the EV inverter simulation using driving cycles is shown in Figure 6.3.

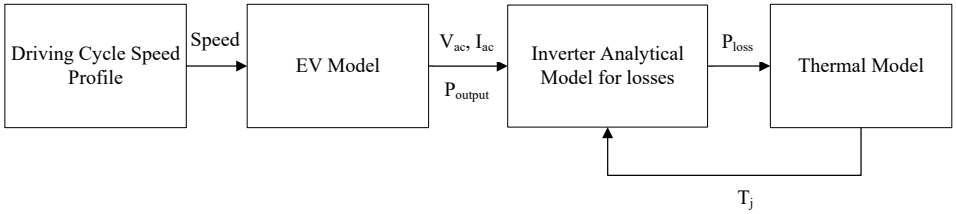


Figure 6.3: The flowchart of the EV Simulation .

The standardized driving cycle determines the speed of the EV. Three different driving cycle standards are used to measure the efficiency of the inverter: WLTP, NEDC and FTP. As seen in Figure 6.4, each driving cycle has a duration which varies from 20 to 30 minutes and captures the dynamic speed profile of a vehicle based on the respective driving standard. The speed data obtained is then used by the EV model to simulate the inverter, PMSM, the physics of the car and the feedback controller. The EV model, seen in Figure 6.5, is implemented in Simulink. From the EV model simulation, the voltage, current, and modulation of the traction inverter are determined. The specific details of the EV model are described in [33], this is not included in the scope of this thesis. The assumptions of the EV model are:

- the car is considered to run on a flat surface with zero inclination
- the resistance of the winding and the permanent magnet's flux do not suffer from thermal effects
- the electric machine does not suffer from thermal effects, thus the resistance of the winding, the flux and inductance of the machine stays constant

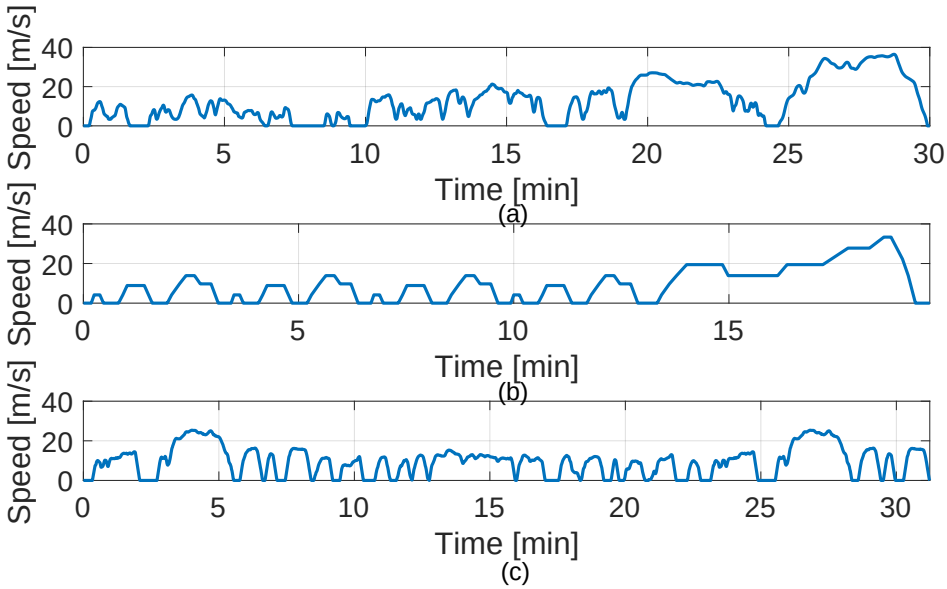


Figure 6.4: The speed profiles of a) WLTP, b) NEDC, and c) FTP driving cycle.

- no power loss between gear transmissions

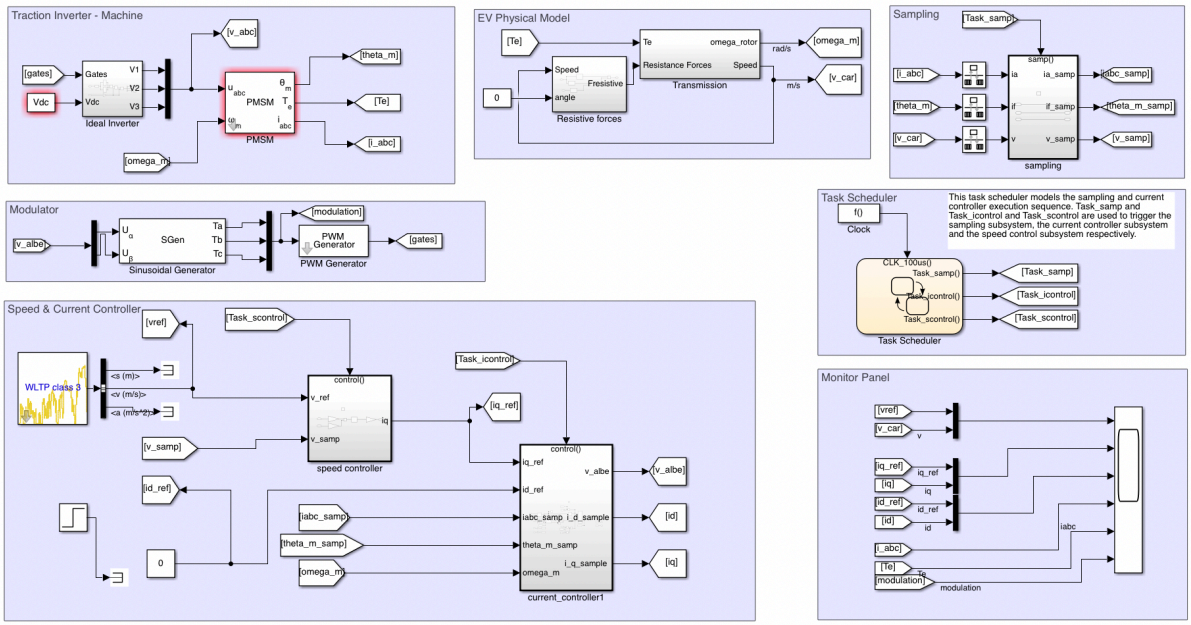


Figure 6.5: The EV Simulink Model.

Using the inverter data determined by the EV model, the losses of the inverter are calculated using the analytical equations in chapter 3. The initial junction temperature used to determine on-state and switching characteristics is set to 75 °C. The losses analytical model is coupled in a feedback loop with the thermal circuit, which models the junction temperature variation due to losses. In the feedback loop, the on-state and switching characteristics determined by the thermal circuit are used to calculate the losses for the next data point. The simplified thermal resistance circuit of the inverter is shown in Figure 6.6 and is implemented in Simulink. To ensure that the vehicle would operate within the thermal limits, a cooling system is designed for the inverter. The heatsink thermal resistance varies for each configuration and is determined by the equation (6.1), where $T_{\mathrm{a,max}}$= 75°C, $T_{\mathrm{j,max}}$ is the max junction

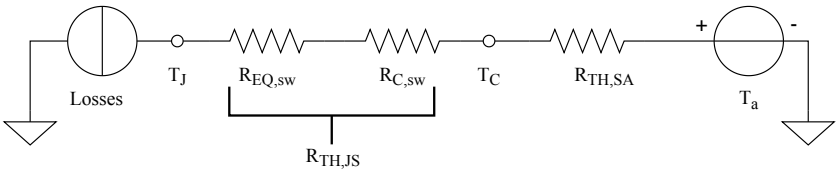


Figure 6.6: The simplified thermal circuit for Heatsink design.

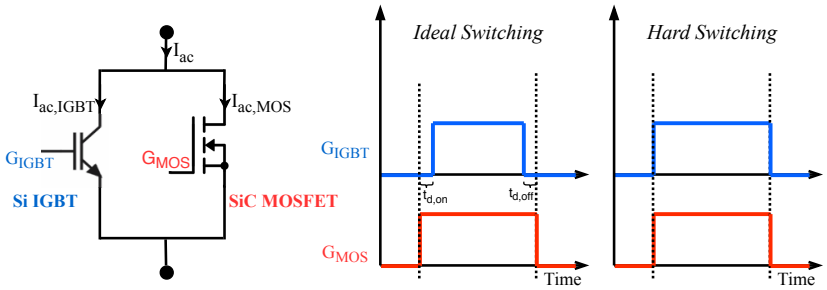


Figure 6.7: The simplified thermal circuit for Heatsink design.

temperature and P_{loss} is the total power loss of the inverter.

$$R_{\text{TH,SA}} = \frac{T_{\text{j,max}} - T_{\text{a,max}}}{P_{\text{loss}}} - R_{\text{TH,JS}} \tag{6.1}$$

The EV inverter simulation is run separately using the values from the datasheet and the experimental values. As discussed in chapter 3, the switching losses are calculated using a quadratic approximation of the measured values based on the total load current. For the simulations using datasheet values, ideal switching conditions as discussed in chapter 4 are used, i.e. the MOSFET takes the turn-on and -off losses while the diode takes the reverse recovery losses. For the simulations using experimental values, the optimal switching losses data is used, i.e. turn-on losses using 50ns switching delay and turn-off losses using 1000ns switching delay.

6.2.2. EV Traction Inverter Simulation Result

The efficiency of each configuration over the driving cycles using experimental values are shown in Figure 6.8. Through the driving cycles, the car is shown to be constantly operating at low partial load (as seen in Figure 6.9). The load current is mostly under 35% of the max rated current for all three driving cycles. This explains why the solutions employing SiC MOSFET perform considerably better. The pure MOSFET inverter has the highest efficiency over the driving cycle as expected as it is the most efficient under 90% static load. The pure IGBT inverter, which has the lowest static efficiency under 60%, has the lowest efficiency through the driving cycle. The hybrid switch inverter's efficiency is in between the pure MOSFET and the pure IGBT inverters. The comparison between datasheet values and the experimental values is shown in Table 6.2. With the lower experimental on-state performance, all three switches have lower efficiency for the experimental values as expected. In terms of cost, the hybrid switch inverter is 30% cheaper than the pure MOSFET inverter. In comparing the efficiency and cost, the hybrid switch has the best compromise for the EV traction application.

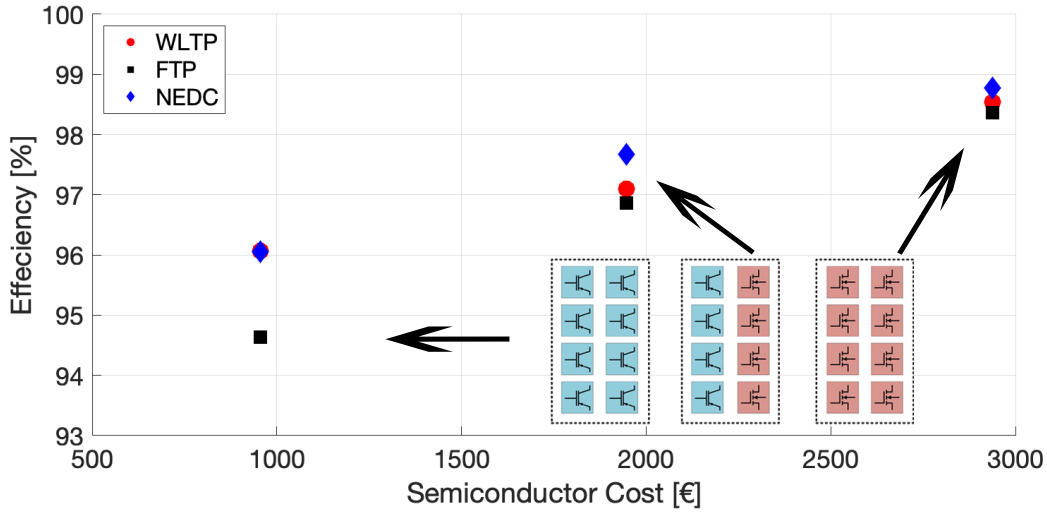


Figure 6.8: The efficiency of all configurations over WLTP(red circle), FTP(black square) and NEDC(blue diamond) driving cycles using experimental values.

Driving Cycle	Config.	Exp. eff. %	Datasheet eff. %	Difference %
WLTP	IGBT	96.07	96.26	-0.2
	Hybrid	97.10	97.15	-0.1
	MOSFET	98.54	98.92	-0.4
FTP	IGBT	94.63	94.93	-0.3
	Hybrid	96.86	97.00	-0.1
	MOSFET	98.54	98.89	-0.4
NEDC	IGBT	96.05	96.28	-0.2
	Hybrid	97.67	97.78	-0.1
	MOSFET	98.77	99.18	-0.4

Table 6.2: Comparison of efficiencies over the driving cycles for both datasheet and experimental values.

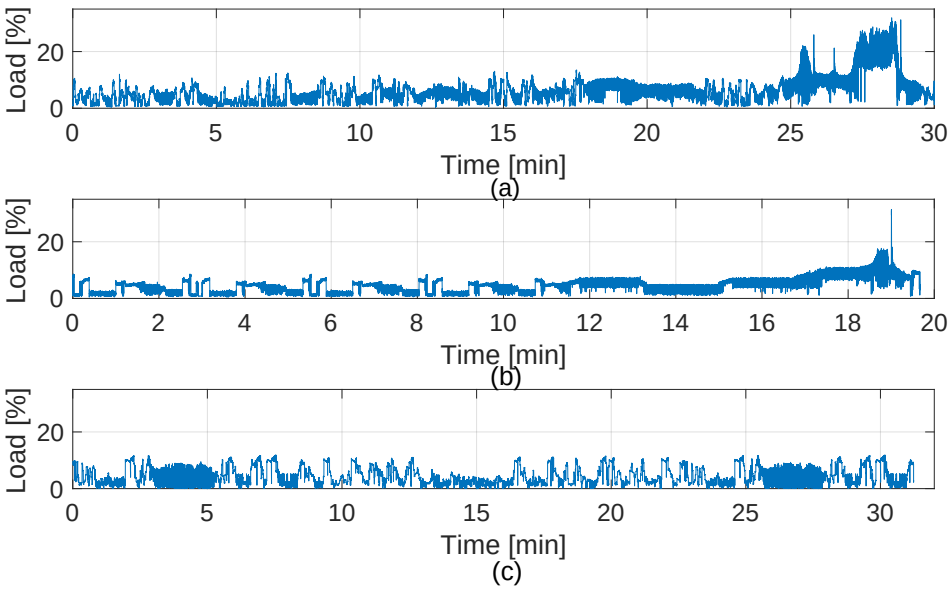


Figure 6.9: The percentage of max load current of the EV traction inverter over the driving cycles.

7

Conclusion

This thesis report investigated the performances of the Si/SiC hybrid switch inverters for a EV traction drive. Due to the fact that the EVs operate at low partial load for the majority of their use, the Si IGBT-based traction inverter operates at a disadvantage since it does not have the best performance at low current. The Si IGBT - SiC MOSFET paralleled hybrid switch constitutes a superior alternative. It has the advantages of both the Si IGBT and SiC MOSFET, and has better on-state characteristics over the entire operating range. In addition, its switching losses are lower than the pure IGBT switch. With the optimal switching strategy, switching losses can be reduced further by providing ZVS for the IGBT. Furthermore, the hybrid switch has a considerably lower cost than the full SiC MOSFET switch. In this thesis, three different configurations of the inverter switch are compared. The hybrid switch demonstrates top performance at a lower cost.

Future studies should examine the rated current ratio between Si IGBT and SiC MOSFET to further increase efficiency and decrease cost while considering optimal switching strategy, thermal stress and temperature variation. Furthermore, the traction inverter efficiency should be experimentally evaluated with the driving cycle load profile. A Hardware In the Loop implementation would be ideal for this test to prove the advantage of Si/SiC hybrid switch for commercial EVs. To evaluate the efficiency more realistically, the driving load profile of an actual EV car can be used.

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