Delft University of Technology

M.S.C thesis

ET4300

Negator-based Switch Capacitor Buck-boost DC-DC Converter

Authors:

Gary Wang (5486688)

August 24, 2023


TU Delft
Delft
University of
Technology

Acknowledgements

To begin with, I need to express my sincere gratitude to my supervisor, Sijun Du, who has offered splendid support and guidance throughout my last year, the marvelous projects and opportunities he provided, and the effort he made to cultivate me as an analog engineer. At the same time, I would like to thank every member of the department of Microelectronics, such as Dr.Kofi Makinwa, Dr. Ir. Michiel Pertijs, Dr.Klaas Bult, Dr. Ir. Qinwen Fan, for example, generously demonstrated their outstanding skills and knowledge during their lectures, which taught me the fundamental methodology of building a circuit and the related skills.

Special Thanks to all my group members in Sijun Du's Group. Shuangmu Li has shared his brilliant idea and experience in layout design and led me through the tape-outs. Ningchao Lin, who has worked together toward the tape-outs.And especially, I would like to thank PHDs in our group: Xinling Yue, Tianqi Lu, and Wenyu Peng, who have provided selfless assistance in the last year.

Last but not least, I should thank my parents for supporting me in studying in a foreign country and for their encouragement over the last year.

Contents

Abstract

The development of the Internet of Things has given rise to enormous new industries and applications, including automobiles, smart healthcare systems, smart houses, etc, and the power supply has become the major constraint preventing them from further increasing logic speed. Thus, a SC(switch-capacitance) DC-DC converter with high efficiency, integration on-chip, and multiple voltage conversion ratio (VCRs) is significantly important.SAR(successive Approximation Register) SC was published in 2013, it realized $2^n - 1$ voltage conversion ratios with n 2:1 SC stage with the cost of charge sharing loss. In 2014, Recursive topology minimized charge-sharing loss by maximizing the connection to the power rail to improve efficiency. While both topologies only offer 7 VCRs for 3 stages, the new topology utilizing the voltage negative feedback technique has expanded this range to 79 ratios, including all p/q rational ratios from 1/2 to 15/16.Each ratio is written in the form Vout=$A * V_{DD} - B * V_{out}$, and only three voltage negative feedback module(negators) are to be used :$V_{DD} - V_{out}$,$2V_{DD} - V_{out}$,$-V_{out}$.This paper presents an improved design to expand this VCR range to boost operation, achieving VCR from 15/16 to 16 times the input.

In total,3 2:1 SC stages and 3 negators are applied, with a total capacitance of 1.3nF. The capacitance of 3 stages and negators are 130p,260p,520p, and 130p respectively. The system was designed and fabricated in a 180-nm BCD process, the peak efficiency is achieved at a 2:1 ratio @20MHz, with an efficiency of 82.28%, reached load current =6.4mA. The layout area is approximately 2.084mm^2, and the current density estimated is 3.07 mW/mm^2.The design has remarkably expanded the 79 VCR options to both buck operation and boost operation.

Chapter 1

Introduction

The Internet of Things (IoT) has developed rapidly in recent years. It has profoundly influenced the way people live and various industries, including automobiles, smart healthcare systems, intelligent houses, as well as numerous sensors industries utilized in these applications. Apart from that,daily-used electronic devices such as cellphones and personal computers have already become indispensable parts of people's lives.

Over the past 60 years, the integrated circuit industry has seen rapid growth due to the increasing number of transistors on-chip and the speed of logic circuits. However, power has put a significant design constraint preventing the further increase of logic speed. To overcome this challenge, designers have applied parallem to face this challenge[1]. It is becoming increasingly important to optimize total chip power and circuit performance by utilizing an independent power supply for each core as parallelism increases the number of cores integrated into a chip.

Adding off-chip supplies is not an ideal solution due to the significant degradation of supply impedance and increased cost due to additional pins, resulting in a larger board size. Thus, fully integrated voltage conversion on the silicon chip is preferable, resulting in better energy density and efficiency in general. Meanwhile, separating the voltage supply for each core requires a flexible power supply that can support multiple voltage output levels, as shown in Figure1.2, which grants the necessity of developing minimized, low power cost, multiple conversion ratio DC-DC converters.

Despite many efforts taken to improve the power density and quality factor of inductor-based DC-DC converters by co-package and reducing the inductor size[2][3][4], Inductor-based DC-DC converter still suffers from high parasitic resistance of the inductor and the inductors parasitic capacitance towards substrate as well as skin effect in winding for system-on-chip design[5]. Switch-capacitor DC-DC converters are still advantageous over inductive DC-DC converters in

terms of integration on-chip, scalability to power requirement[1], especially suitable for fully-integrated,low-power systems. Meanwhile, the Modular Capacitor-based DC-DC converter can quickly achieve a balance between performance and energy efficiency through dynamic voltage scaling (DVS) of individual processing cores following performance needs. Considering these benefits of SC converters, many techniques are also designed to improve the efficiency and power rating. such as [6], which applied 16-phase interleaved topology to reach 82% efficiency with only 0.5% ripple voltage of the original design.

However, the Traditional Switch-Capacitor DC-DC converter is not applicable in all scenarios as the SC converter is only efficient at discrete VCRs, resulting in a system's lack of flexibility with variable input or output voltage. Such as the system shown in Figure1.1,if supplying all systems with single-VCR converters with VCR=1/4, only memory 1 would be efficient, while the processor and memory2 would suffer apparent degradation of efficiency. Meanwhile, the battery is always facing the challenge of voltage degradation, as the battery power is getting lower, the efficiency might drop drastically if only one VCR is applicable.

In 2013, [7] has proposed a successive-approximation-register(SAR) technique to create a fine-grained binary conversion ratio resolution of $V_{IN}/2^N$ by cascading multiple stages.[8] has improved this topology by maximizing the connection to VDD or VSS to reduce cascaded losses. In.2016,[9] has broadened the VCR to $0 < p < q < 2^(N + 1)$ with the help of 3 kinds of negative feedback modules generating three voltage levels: VDD-Vout, 2VDD-Vout,-Vout.Utilizing 3 2:1 converters and 2 out of 3 negators, any conversion ratio between 1/2 to 15/16, in total 79 VCRs, can be generated. However, this previous work only supports buck operation. Thus, this work expands the previous work to boost function, resulting in 2*79=158 VCRs.

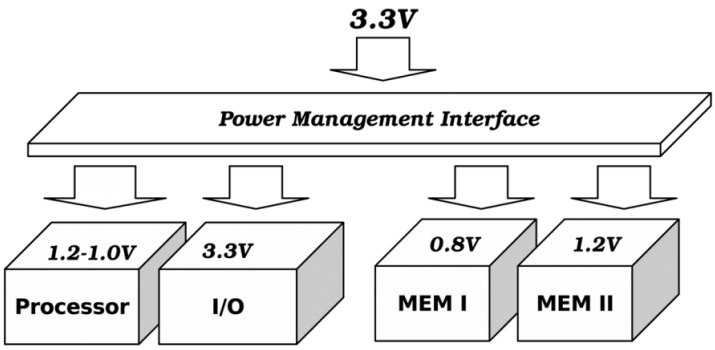

Figure 1.1: Power Management system
[5]

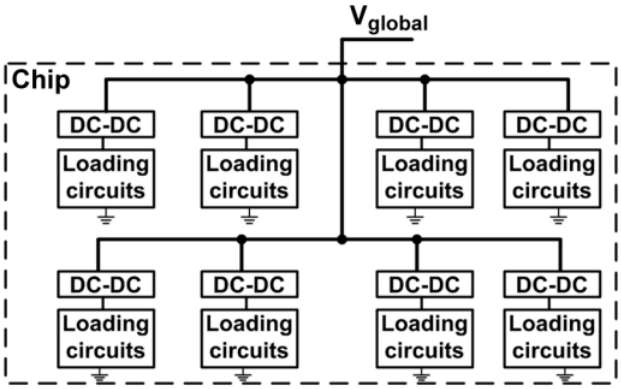

Figure 1.2: Power Distribution for separate cells[1]

1.1 Design Goal

This project aims to develop a buck-boost Switched-capacitor DC-DC Converter based on negative output feedback(negators). The whole system consists of a VCO(Voltage-Controlled Oscillator), Non-overlapping clock generators, three 2-to-1 switch capacitor stages with sizing ratio:4:2:1, as well as three negators producing voltage potential: VDD-Vout,2VDD-Vout,-Vout, and the corresponding transmission gates enabling each module and control the connection for each module. It is expected to successfully realize ratios from 1/2 to 15/16 and 15/16 to 2 for boost, both 79 VCRs, also a peak efficiency of 82%.

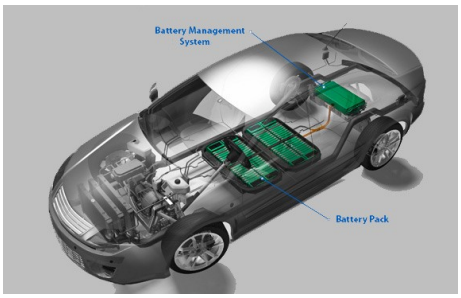

Figure 1.3: electrical vehicles[10]

Figure 1.4: smart healthcare[11]

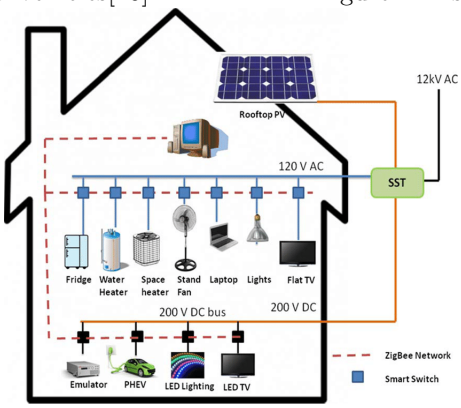

Figure 1.5: smart house[12]

Chapter 2

State of Art

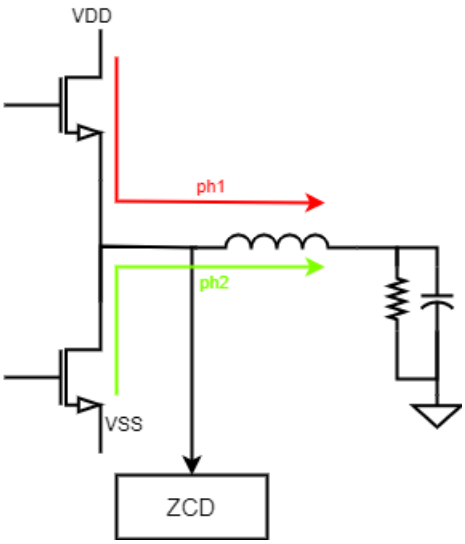

Figure 2.1: inductor-based converter

2.1 Inductor-based DC-DC Converter

2 most commonly used energy storage elements are respectively inductors and capacitances. The inductor is favored in many designs because of its high power rating and efficiency in high-power

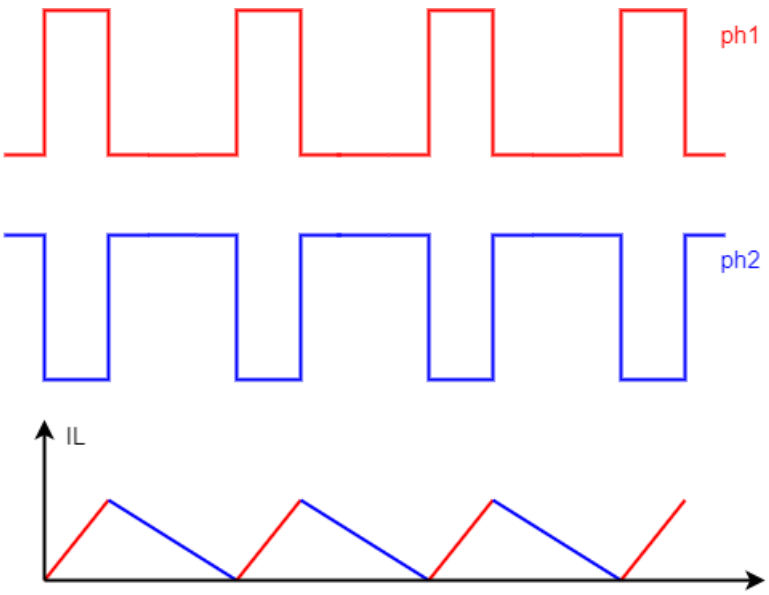

Figure 2.2: inductor-based converter waveform

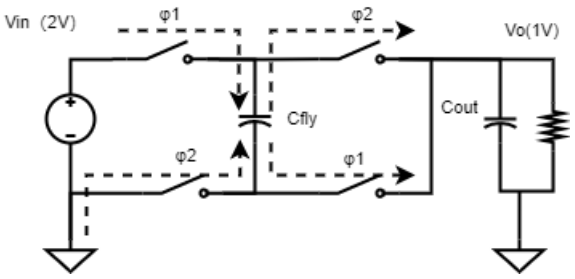

Figure 2.3: SC Dickson converter

scenarios. This section will introduce an inductor-based single-stage buck-boost converter that works in discontinuous conduction mode(DCM). The operation of the system can be separated into 2 phases; in phase 1, the high-side MOSFET is turned on, and the voltage across the inductor is $V_L = V_{in} - V_{out}$, which is constant after the start-up process. Thus, the inductor is charged with current rising with a constant slope. After an on-time, either defined by constant on-time or Pulse Width Modulation(PWM), phase 2 would be activated to load the stored energy to the load. The current flowing through the inductor would decrease linearly as the voltage difference on the inductor is $V_L = -Vout$.In DCM operation, a zero-current detector(ZCD) would be applied. When the inductor current drops to zero, the ZCD would be activated to start phase 1 to charge the inductor again. This module prevents the inductor from reversely charging, which will severely reduce the efficiency. The inductor-based DC-DC converter can also work in Continuous conduction mode (CCM) mode to supply a higher power, in which the inductor current is always above zero. This control scheme can be achieved by PWM control or the current sensor.

As the demand for minimization and integration on-chip rises, Fully integrated Switch-Capacitor(SC) converters are more welcomed by engineers as inductor-based design relies on the off-chip inductor; on-chip inductor requires a high-quality factor to have a better efficiency, which increases the costs on components. Meanwhile, as previously mentioned, parasitic resistance, capacitance, and skin effect in the winding are also aspects that cannot be ignored. Moreover, the inductor is difficult to scale with output power; low-power applications might need a larger inductor to accomplish, which limits the efficiency in terms of low-power applications.

2.2 Switched-Capacitor Power Converter

Capacitor-based DC-DC converters have aroused the interest of power management IC designers, especially for low-power applications. There are several benefits of Capacitor-based converters in integrated design. Capacitor-based converters can be implemented using CMOS technology, allowing them to be integrated directly onto a chip alongside other digital circuitry. This integration results in space-efficient designs, making them well-suited for miniaturized and portable devices. Additionally, they can be easily scaled to accommodate various power requirements by adjusting the number of switches and capacitors. Meanwhile, Capacitor-based converters can achieve relatively high conversion efficiencies[6] [13]in fully integrated design due to the absence of magnetic components like inductors. This efficiency can be particularly beneficial in low-power and energy-constrained applications, where minimizing energy losses is crucial. Moreover, they can be easily configured to provide multiple output voltage levels using a single topology. This

modularity is precious in applications where different components or subsystems require varied voltage levels. Last but not least, the capacitor-based converter is financially beneficial in fully integrated design as it requires fewer components and a more accessible control loop.

However, because of the intrinsic characteristic of the switches and capacitors used in the circuit, the efficiency may be limited[14]. Another challenge lies in regulating the load voltage, as the duty cycle does not scale with the output voltage, resulting in increased control system complexity.

SC circuits can also be combined with inductor-based structures to assemble a hybrid converter, improving the load voltage regulation and obtaining more conversion ratios. An example would be resonant SC converters, which have a higher power output capacity and power density, as shown in [15]. As the possible combinational topology of inductor and SC converters is massive, and as it is not the main topic of this essay, it would not be discussed in depth.

2.2.1 2:1 Dickson SC converter

The 2:1 Dickson Converter, a variant of the Dickson charge pump, is a widely used DC-DC converter topology with versatile applications in various electronic systems. This converter is renowned for its simplicity and efficiency, making it a valuable choice for voltage buck-boost applications. A typical Dickson SC converter stage consists of 4 switches and one capacitor. There would be 2 phases involved: phase 1 for charging and phase 2 for discharging, each taking half of the period. The operation is shown in Figure2.4 [16]. In phase 1, the top plate is connected to the input voltage V_{in}, while the bottom plate is connected to the output voltage V_{out}. Thus, a voltage potential of $V_{in} - V_{out}$ is created between both plates and meanwhile, the input charges the capacitor, and the charge would flow to the output. In the second phase, the capacitor is connected between V_{out} and V_{SS}.Thus, the output voltage V_{out}=$V_{in} - V_{out}$ leads to $V_{in} = 2V_{out}$, called 2:1 buck conversion. At the same time, the previously stored charge would also supply the output. Therefore, the charge output would be twice that of the current input from the voltage source, which would be a useful characteristic that can be utilized. Another noteworthy feature of Dickson 2:1 converters is their scalability. By adding more stages, the voltage multiplication factor can be further increased. This scalability allows the converter to generate higher output voltage levels without significantly complicating the design or sacrificing efficiency. Thus, most multiply-VCRs designs are built upon this structure.

SC converter is built based on capacitors and switches; both of them assemble some non-idealities that will result in power loss, which can be generally categorized into switching loss

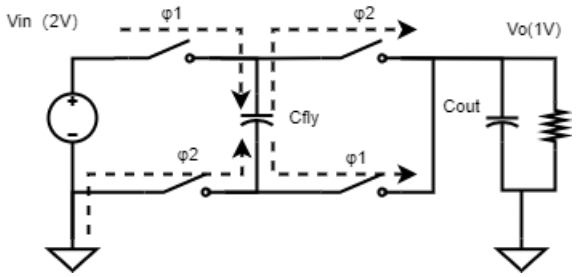

Figure 2.4: Dickson SC converter

and conduction loss, as well as power cost of clock generation circuit(VCO non-overlap, etc). Conduction losses of the SC converter can be further modeled into two types of impedance: Slow Switching Limit Impedance(R_{SSL}) and Fast Switching Limit Impedance(R_{FSL})[17].

2.2.2 switching loss

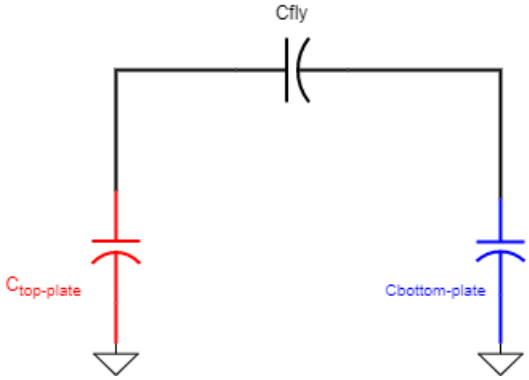

Figure 2.5: Parasitic Losses

In this subsection, switching loss is going to be analyzed. Generally, the switching loss can be separated into bottom-plate loss and gate-driver loss. To begin with, bottom-plate loss is caused by parasitic capacitance of flying capacitors, as shown in Figure2.5; whenever the flying capacitor is charged, the bottom plate and top plate would also be charged, leading to power loss. The bottom-plate parasitic capacitance is usually much larger than the top-plate capacitance. Thus, the top-plate loss and bottom-plate loss can be combined to be called bottom-plate loss. This loss is proportional to the cascaded stages, switching frequency, parasitic capacitance and squarely proportional to the voltage drop on the flying capacitors.

The gate driver loss is another dominant factor in switching loss. In many circumstances, the driving capability of the clock generation circuit is not enough to drive the power switches. Therefore, gate drivers would be applied to augment the clock signal's drive capability to drive the power switches' gate capacitance successfully. The parasitic capacitance of each buffer stage would also be driven when the clock signal flips. This is the reason that each stage of the buffer consumes enormous power.

Meanwhile, the intrinsic gate capacitance of the Power Switch would also consume a considerable amount of power. The switching loss is proportional to the switching frequency. Decreasing the switching frequency would result in Slow Switching Limit Impedance on the one hand, increase the settling time, and slow the transient response on the other hand.

2.2.2.1 Slow Switching Limit Impedance

If the operation frequency of the system is relatively slow, then the capacitor would be fully charged during the charging phase. Thus, it can be modeled as an open circuit, where the capacitance dominates the power loss while R is independent. The power loss during charge transition can be modeled as

$$E = \frac{q_{out}^2}{C} \tag{2.1}$$

Then, based on the following equation:

$$q_{out} = I_{out}T \tag{2.2}$$

$$P = \frac{E}{T} \tag{2.3}$$

We can obtain the following results:

$$P = \frac{I_{out}^2 T^2}{CT} = R_{SSL} I_{out}^2 \tag{2.4}$$

Thus,

$$R_{SSL} = \frac{1}{Cf} \tag{2.5}$$

With this derived equation, we can learn that we can decrease the output impedance by either increasing the capacitance or the switching frequency. The increase in capacitance is directly translated into an increase in area. A common approach is increasing the switching frequency until Fast Switching Limit Impedance becomes the dominant factor.

2.2.2.2 Fast Switching Limit Impedance

The previous section implies that the output impedance can be decreased by increasing operation frequency. However, switch resistance would begin to dominate the impedance at a certain

frequency. The energy loss at high frequency can be modeled as follows:

$$E = RI^2t = R\frac{q_{out}^2}{t^2} \tag{2.6}$$

The duty cycle is 50%,t=50%T, and there are four switches.

$$E = \frac{2q_{out}^2}{T}(R_1 + R_2 + R_3 + R_4) \tag{2.7}$$

Also based on equation2.2and equation2.3,

$$P = 2(R_1 + R_2 + R_3 + R_4)I_{out}^2 = R_{FSL}I_{out}^2 \tag{2.8}$$

result:

$$R_{FSL} = 2(R_1 + R_2 + R_3 + R_4) \tag{2.9}$$

As shown above,R_{FSL} is independent of capacitance and frequency. To minimize this impedance, the ON-resistance of power switches should be reduced. Based on the following equation, the length of MOSFET should be kept at a minimum, and the width of the switches should mitigate the conduction loss. While increasing MOSFET size results in a trade-off with area, the increased MOSFET size would result in larger parasitic capacitance, leading to much higher switching loss. In this design, the area is dominated by capacitance rather than power switches. Thus, the sizing is mostly based on balancing Conduction loss and switching loss.

$$R_{on} = \frac{L}{\mu C_{ox} W(V_{GS} - V_{th})} \tag{2.10}$$

The overall impedance is calculated by

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.11}$$

The diagram below demonstrates the relationship between frequency and overall impedance. Based on this relationship, we prefer to configure the circuit to operate at f_c frequency, as this frequency minimizes the overall output impedance by reducing the R_{SSL} without further increasing the switching loss, which is proportional to the switching frequency. The efficiency also depends on the output current. As the equation shows:

$$\eta = \frac{P_{out}}{Pin + I_{out}^2 R_{out} + P_{switch}} \tag{2.12}$$

The switching loss would be generally constant if the operation frequency is kept constant. Increasing the output current may help to improve the efficiency. While as the output current increases, the conduction loss $I_{out}^2 R_{out}$ might dominate the losses. Therefore, there is an optimal output current with the highest output efficiency.

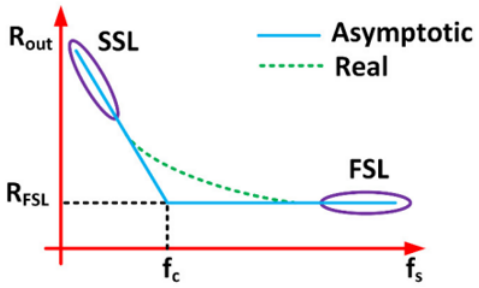

Figure 2.6: Output impedance versus frequency [17]

2.2.3 Multiple VCR techniques

As previously mentioned, despite the high power density and compatibility on a chip, SC converters are only efficient at a particular power conversion ratio, which leads to a limited input and output range. In application scenarios of DC-DC converter, multiple loads with different demanded output voltage or the need to configure output voltage are quite common. Meanwhile, the battery voltage may degrade over time owing to normal discharge, aging, high temperature, etc. A fix-VCR converter would not be efficient in such cases or even cannot reach the designated voltage. As shown in Figure Thus, multiple-VCR is an essential characteristic for SC converters to meet the requirements for various application situations. The conversion ratio could be extended by cascading fixed-VCR stages. For example, we can obtain 5/4 or 4/5 VCR by simply cascading 2 stages, or utilizing series-Parallel topology to reach multiple VCR while with the cost of system complexity[18].

2.2.3.1 successive approximation (SAR)SC converter

In 2013, A successive approximation (SAR) SC DC-DC converter topology[7] is presented, which offers fine-grained control of VCR, thus facilitating effective load in a much broader input and output range. Successive approximation (SAR) is a common technique used in ADC design. It usually consists of a comparator and a n-bit DAC, which separate the voltage range into 2^n region; by comparing the input with the current value fed from the DAC, the input can be quantified to a voltage level[20], as shown by figure2.8.

When applying this technique to a DC-DC converter, the concept is similar. By cascading n 2:1 stages, the voltage range can be separated into 2^n voltage domains; thus, a fine-grained

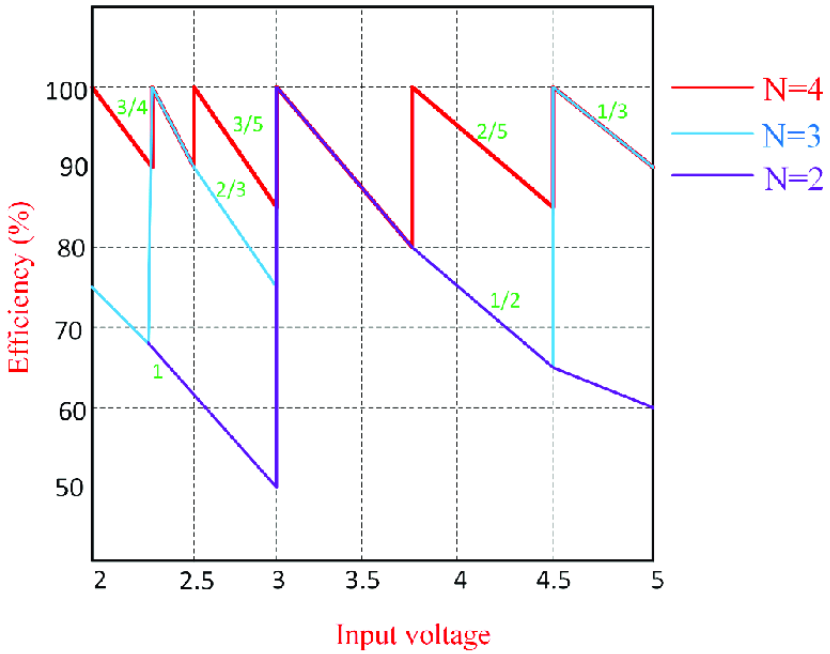

Figure 2.7: comparison of a multi-ratio-switched-capacitor-converters [19]

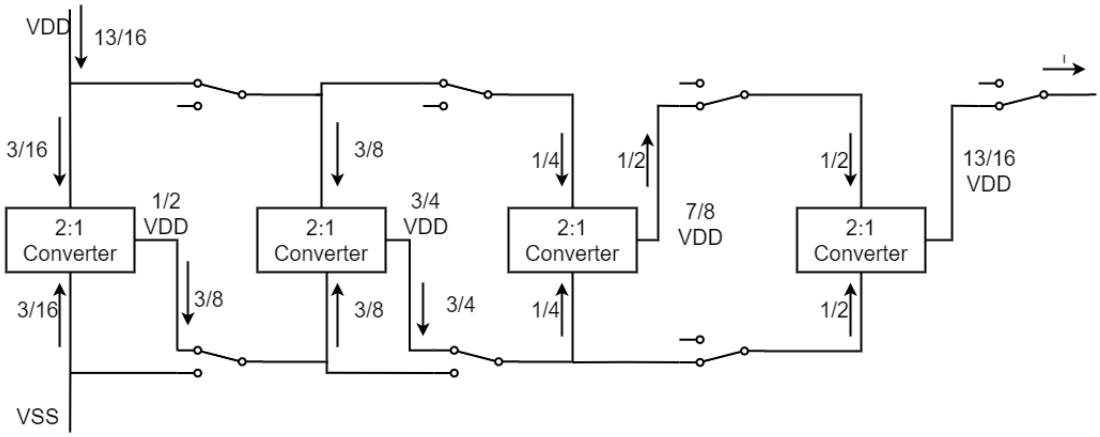

Figure 2.8: SAR ADC

$2^n - 1$ voltage conversion ratio could be obtained by configuring the connection between each stage.In figure2.9,each stage has two inputs:V_{high} and $V_low.V_mid$ is a middle voltage equals to $\frac{(V_{high}+V_{low})}{2}$,in the first stage, this voltage is $\frac{(V_{DD}+V_{SS})}{2}$ and this V_{mid} in second stage can generate $\frac{(V_{DD}+V_{mid})}{2}, \frac{(VSS+Vmid)}{2}$ in the second stage.In this case, is $frac3/4$ and $frac1/4$,3 voltage conversion ratio is generated by 2 stages. Moreover, this V_{mid} in stage 2 can in stage 3 also generate 4 different voltage potentials 1/8,3/8,5/8,7/8. Meanwhile, it enables easy binary control, and the voltage conversion ratio can be determined by

$$\frac{V_{out}}{V_{in}} = \frac{A+1}{2_n} \tag{2.13}$$

Where A is the n-bit configuration signal from a_1 to a_n. As an example, to obtain 7/16 voltage conversion ratios. The binary code A equals 0110.In this system,0 means connection to V_{high} while 1 means connection to V_low, In the first stage,V_{mid1}=$1/2 * V_{DD}$;The second stage is connected to V_{mid1} and V_{DD} to create V_{mid2}=3/4 *V_{DD};The third stage is connected to V_{mid2} and V_{DD} to generate V_{mid3}=7/8 *V_{DD} And the final stage, the 2:1 inputs are V_{mid4} and V_{SS}, in this way, 7/16 is generated.

The SAR-based SC converter has successfully expanded the voltage conversion ratio to $2^n - 1$ in an easily fulfilled topology with the cost of a relatively lower peak efficiency of 72%[7]. The cascaded loss is the dominant factor as the stages are linearly cascaded.

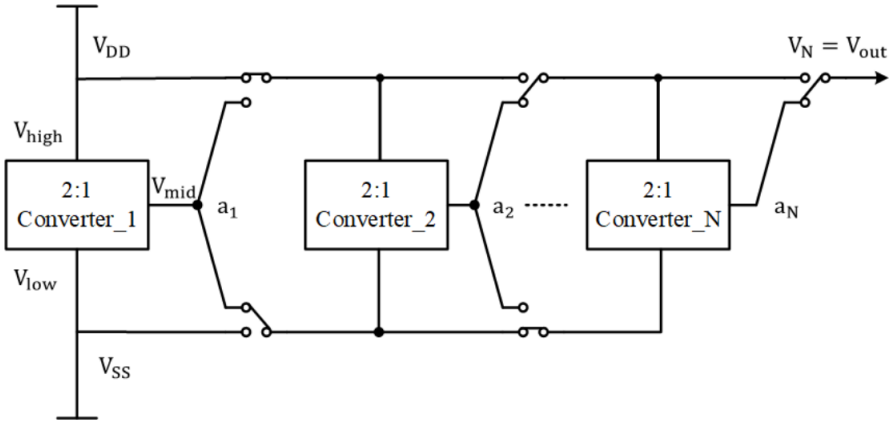

Figure 2.9: SAR SC converter

2.2.3.2 Recursive SC converter

In order to mitigate the cascaded loss, in 2014, a recursive switch-capacitor (RSC) topology that can also generate $2^n - 1$ VCRs with n 2:1 stages was introduced with a higher efficiency and an even smaller number of devices. Figure2.11 has demonstrated the simplified topology. The advantage of RSC topology lies in the maximized connection with the power rails. Each stage receives input from the previous stage and the other from VDD or VSS, determined by the binary code a_1 to a_N. The MSB is a_N while the LSB is a_1. As an example, Figure2.11 has demonstrated an example of how to build a 3/8 ratio by three 2:1 stages and the corresponding current flowing through each stage(or, more precisely, charges). As the binary code of 3 is $(011)_2$, the first stage is connected to VDD, and the first stage produces 1/2 VDD; The second stage is also connected to VDD, and the output of the second stage becomes 3/4 VDD; Then The final stage is connected to VSS, the previous 3/4 VDD is divided by 2 to generate 3/8 VDD.

To demonstrate the advantage of RSC topology, Figure2.12 and 2.13 are the topology diagrams showing voltage and current for each stage, both with a VCR of 13/16 of SAR and Recursive topology. As depicted because both inputs are from the previous stage. Obviously, more charges are shared between intermediate stages than Recursive topology, which will significantly increase the charge-sharing loss. As recursive topology maximizes the connection to the power rail, each stage took $1/2^(N + 1 - n)$ of the total charge from the power rail and the previous stage. (N is the total stage number, and n is the stage number). The efficiency of this topology has been notably improved as the transfer of charge is minimized.

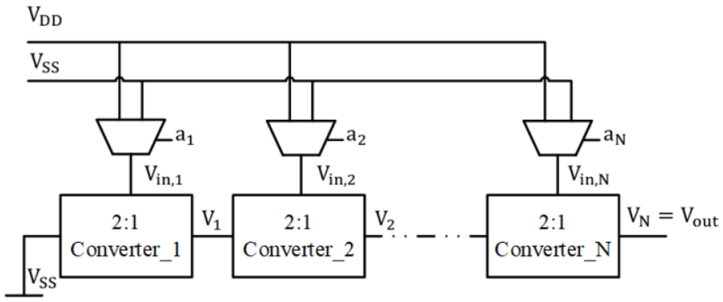

Figure 2.10: RSC SC converter[8]

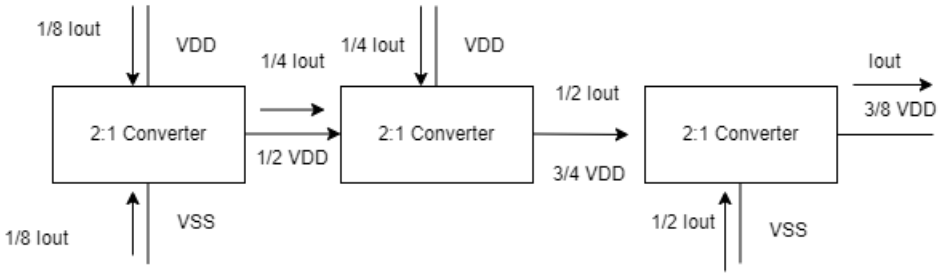

Figure 2.11: RSC SC converter example

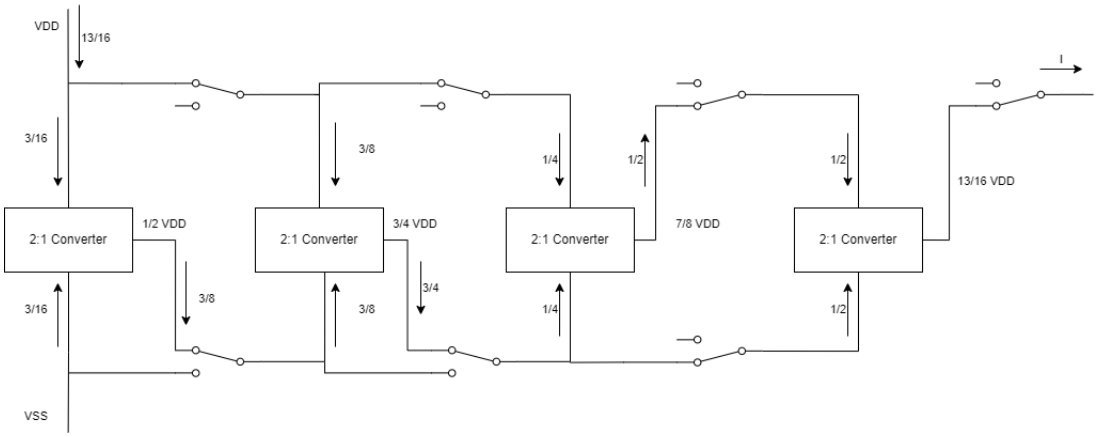

Figure 2.12: SAR SC converter VCR=13/16

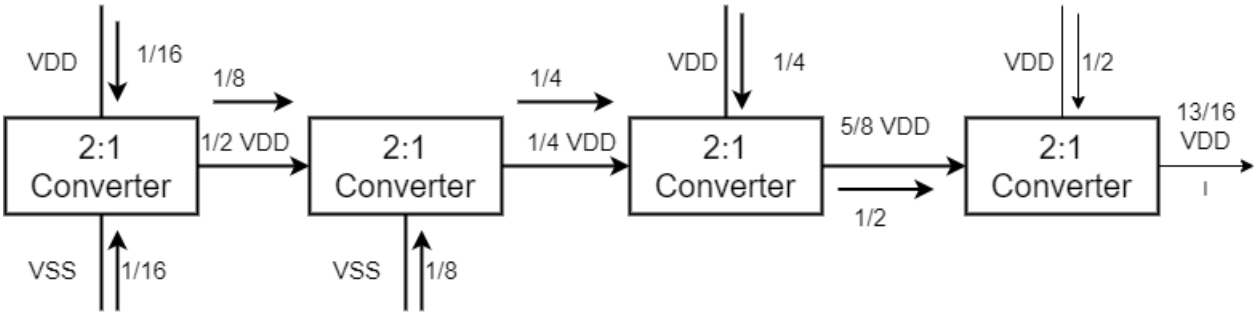

Figure 2.13: Recursive SC converter VCR=13/16

2.2.4 Proposed Topology

The Negator-based Rational Conversion Ratio topology was developed by Wanyeong Jung at the University of Michigan in 2016[9]. It dramatically increases the rational voltage conversion ratio range to p/q, $0 < p < q < 2^n$, using n 2:1 SC converters with the help of 3 kinds of negators. It can generate 79 voltage conversion ratios, while RSC can only generate 7 voltage conversion ratios with 3 stages and 15 conversion ratios with 4 stages. Every conversion ratio lies between 1/2 and 15/16 can be rewritten into the form of V_out=$A * V_{DD}$-$B * V_{out}$, as shown in figure 2.14, 2.15, 2.16. Based on this decomposition equation, only 3 kinds of negators are required to realize all VCRS:$V_{DD} - V_{out}$,$2V_{DD} - V_{out}$, and $-V_{out}$.Noticeably,$2V_{DD} - V_{out}$and $-V_{out}$ would not be applied simultaneously, as this combination will be simplified to $2 * V_{DD} - V_{out}$.

Noticeably, every negator supply current to V_{out} and the other output: $V_{DD} - V_{out}$, $2V_{DD} - V_{out}$, or-V_{out}. It is a beneficial characteristic of negators that they can supply current to the output, which can effectively increase the load current capacity and improve the output conductance for each stage. This topology can also easily realize capacitor sizing as the current flowing through the latter stage is simply twice that of the previous stage. Therefore, the normalized output impedance is no greater than few-VCR converters even though this topology supports much more VCR[9].To compare with the beforehand topologies, a topology also realizes VCR=13/16 is shown below in Figure 2.2.4: As shown, the 2:1 stages still ensure that the minimum charge is transferred between 2 stages, and the other half charge is supplied by negators. Besides, it realizes 13/16 with only 3 stages rather than 4 in SAR and Recursive topologies, even though 2 negators are added while their area on-chip is much smaller than one additional SC stage because of the capacitive sizing.

1:2
$V_{out} = \frac{1}{2}V_{DD}$
1:3
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{2}V_{out}$
2:3
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{2}(V_{DD} - V_{out})$
1:4
$V_{out} = \frac{1}{4}V_{DD}$
3:4
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD}$
1:5
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{4}V_{out}$
2:5
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{4}V_{out}$
3:5
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} - \frac{1}{4}V_{out}$
4:5
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{4}(V_{DD} - V_{out})$
1:6
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{2}V_{out}$
5:6
$V_{out} = \frac{1}{4}V_{DD} + \frac{1}{2}(2V_{DD} - V_{out})$
1:7
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
2:7
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
3:7
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
4:7
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{2}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
5:7
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{2}V_{DD} - \frac{1}{2}V_{out} + \frac{1}{4}V_{DD} - \frac{1}{4}V_{out}$
6:7
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{2}(2V_{DD} - V_{out}) - \frac{1}{4}V_{out}$
1:8
$V_{out} = \frac{1}{8}V_{DD}$
3:8
$V_{out} = \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD}$
5:8
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{8}V_{DD}$
7:8
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD}$
1:9
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{8}V_{out}$
2:9
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{8}V_{out}$
4:9
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{8}V_{out}$
5:9
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{8}(V_{DD} - V_{out})$
7:9
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{8}(V_{DD} - V_{out})$
8:9
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{8}(2V_{DD} - V_{out})$
1:10
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{4}V_{out}$
3:10
$V_{out} = \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{4}V_{out}$
7:10
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}V_{DD}$
9:10
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}V_{DD}$
1:11
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
2:11
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
3:11
$V_{out} = \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
4:11
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
5:11
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
6:11
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
7:11
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
8:11
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} - \frac{1}{4}V_{out} + \frac{1}{8}(2V_{DD} - V_{out})$
9:11
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$
10:11
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out})$
1:12
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{2}V_{out}$
5:12
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out}$
7:12
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out}^2$

Figure 2.14: VCR equation from 1/2 to 7/12

11:12
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD}$
1:13
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
2:13
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
3:13
$V_{out} = \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
4:13
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
5:13
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
6:13
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
7:13
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{8}V_{out}$
8:13
$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}V_{DD} + \frac{1}{8}(2V_{DD} - V_{out})$
9:13
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$
10:13
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out})$
11:13
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}V_{DD} + \frac{1}{8}(V_{DD} - V_{out})$
12:13
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}V_{DD} + \frac{1}{8}(2V_{DD} - V_{out})$
1:14
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
3:14
$V_{out} = \frac{1}{4}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
5:14
$V_{out} = \frac{1}{2}V_{DD} + \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out}$
9:14
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{8}V_{DD} - \frac{1}{4}V_{out}$
11:14
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}V_{DD} - \frac{1}{4}V_{out} + \frac{1}{8}V_{DD}$
13:14
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}V_{DD}$
1:15
$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
2:15
$V_{out} = \frac{1}{4}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
4:15
$V_{out} = \frac{1}{2}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out}$
7:15
$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$
8:15
$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out})$
11:15
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$
13:15
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$
14:15
$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out})$

Figure 2.15: VCR equation from 11/12 to 14/15

1:16

$$V_{out} = \frac{1}{8}V_{DD} - \frac{1}{2}V_{out} - \frac{1}{4}V_{out} - \frac{1}{8}V_{out} - \frac{1}{8}V_{out}$$

3:16

$$V_{out} = \frac{1}{2}(-V_{out}) + \frac{1}{4}((V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out}) + \frac{1}{8}(-V_{out})$$

5:16

$$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}(-V_{out}) + \frac{1}{8}(V_{DD} - V_{out}) + \frac{1}{8}(-V_{out})$$

7:16

$$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out}) + \frac{1}{8}(-V_{out})$$

9:16

$$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$$

11:16

$$V_{out} = \frac{1}{2}(V_{DD} - V_{out}) + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}V_{DD} - \frac{1}{8}V_{out} + \frac{1}{8}(2V_{DD} - V_{out})$$

13:16

$$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}(V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out}) + \frac{1}{8}(V_{DD} - V_{out})$$

15:16

$$V_{out} = \frac{1}{2}(2V_{DD} - V_{out}) + \frac{1}{4}(2V_{DD} - V_{out}) + \frac{1}{8}(2V_{DD} - V_{out})) + \frac{1}{8}(V_{DD} - V_{out})$$

Figure 2.16: VCR equation from 1/16 to 15/16

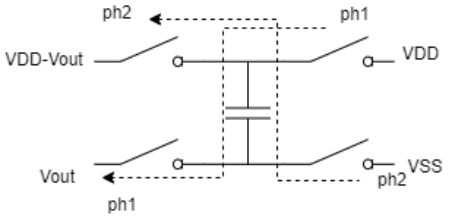

Figure 2.17: $V_{DD} - V_{out}$

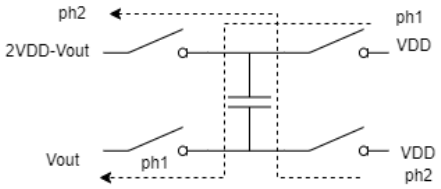

Figure 2.18: $2V_{DD} - V_{out}$

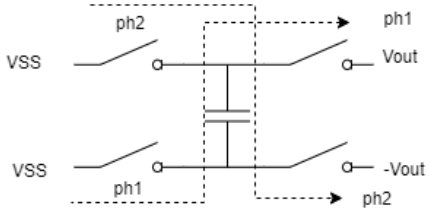

Figure 2.19: $-V_{out}$

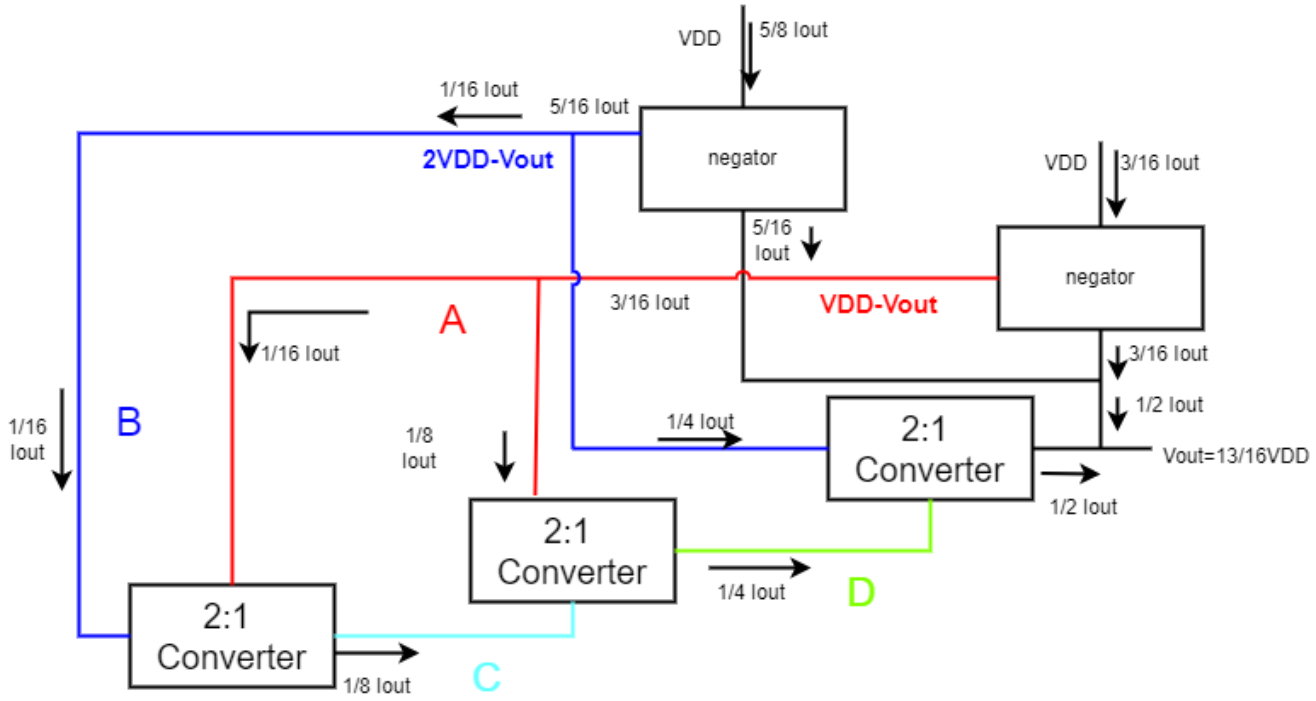

Figure 2.20: Negator-based SC converter VCR=13/16

Chapter 3

System Design

The system is shown in Fig.3.1, 3 2:1 SC stages with scaled capacitive sizing is involved, which means the capacitor in the latter stage is twice that of the former stage in buck operation, and vice versa for boost operation. Thus, in buck operation, the VM port in the 2:1 SC stage with a capacitance sizing of 1 would be the input, while the VH of the 2:1 SC stage with a capacitance sizing of 4 would be the output port. Noticeably, there are 7 connection choices for each port of the SC stage(actually 8; the additional one is a float connection), which can conclude every connection choice for all 158 topologies. Each connection choice module contains a connection to V_{in},V_{out},V_{SS}, and A, B, C, D, which are 4 intermediate ports for connection. The reason why there are 4 intermediate ports lies in the topology diagram of each VCR shown earlier. There are no more than 4 intermediate connection nodes required for all topologies. Meanwhile,V_{in},V_{out},V_{SS},4 intermediate nodes, and one float connection, in together is 8 choices, which can be easily represented by 3 bits, enabling an easy and flexible binary reconfiguration. This system can also optimize capacitive sizing for 1 or 2 stages by freely configuring the input and output ports. For example, when implementing VCR =2:1, all VMs can be connected to the input voltage and all VHs are connected to V_{out}, which ensures maximum utilization of capacitance.V$V_{DD} - V_{out}$ would only be connected to A, while $2V_{DD} - V_{out}$, or-V_{out} would only be connected to B to reduce the reconfiguration bits, as 2VDD-Vout and -Vout would not be utilized simultaneously. Moreover, A VCO and non-overlap clock generator,as well as clock switches, are not shown in the diagram. This chapter will discuss the design procedure of each block separately.

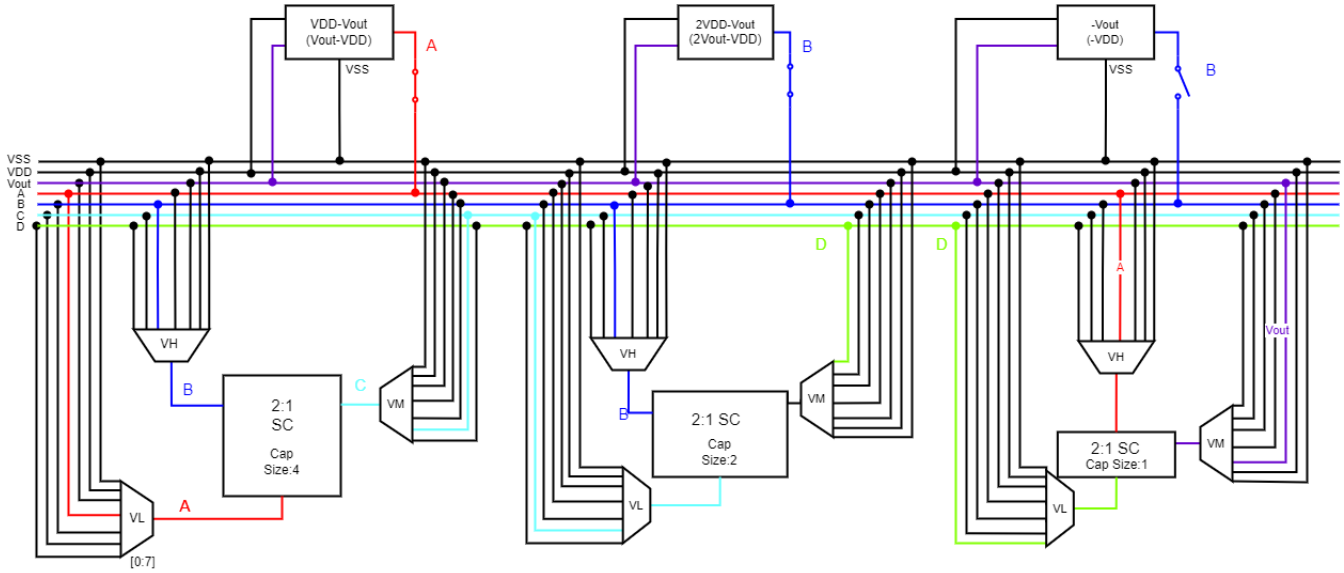

Figure 3.1: Simplified Structure of the negator-based system

3.1 SC stages

The specific 2:1 SC stage and corresponding gate driver implementation are shown below: All NMOS switches are 2V Deep N-well NMOS, as their bulk can connect to other nodes with lower potential rather than its source to alleviate the bulk effect and prevent current from leaking through the body diode. This sizing-optimized module can reach 88.7% peak efficiency when the load current is 64uA with an ideal 20MHz clock signal.Figure3.4 has demonstrated the relationship between load current and efficiency of this basic 2-to-1 module. Around 4% of power is dissipated by output impedance and bottom-plate loss, while 7% of power dissipation is switching loss. The 5V 2-to-1 stage is also tested, while the intrinsic gate charge loss heavily limits the efficiency.

Meanwhile, a clock switch module is also integrated to control the activation of each module. The clock signal needs to go past the clock switch, followed by gate drivers to drive the power switches. The switches utilize the Deep N-well model as this specific model allows us to connect the bulk of NMOS to other voltage potentials rather than the source, which is essential in the Switch Cap as the source of the switch is not always the node with the lowest voltage potential, which might cause current leakage through the body diode of the MOSFET, significantly damaging the efficiency. The NMOS of gate drivers are also Deep Nwell MOSFET. This is because the implementations of some voltage conversion ratios involve the operation that VL or even VH is negative voltage (such as generating -1/2 Vout by inputting -Vout into a 2-to-1

stage, thus clock needs to support a voltage swing from VH to VL rather than VH to VSS. The $V_{DD} - V_{out}$,$2V_{DD} - V_{out}$,-V_{out}, are implemented in a similar way.Only one transmission gate of the -Vout module is replaced by only NMOS, as -Vout is definitely the lowest voltage in the module, and a 2V clock can definitely turn the switch on.

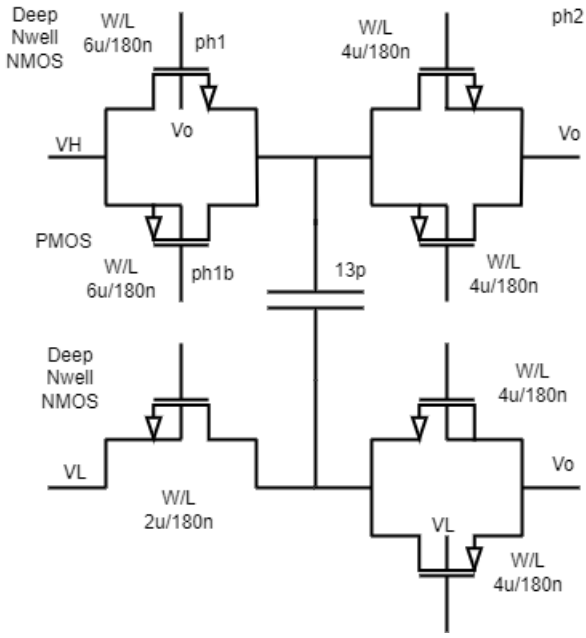

Figure 3.2: 2:1 SC stage implementation

3.2 interleaved SCPC

To mitigate the voltage ripple and increase the power density, interleaved technique is applied. The interleaved technique separates the 2-to-1 stage into N parallel stages with different clock

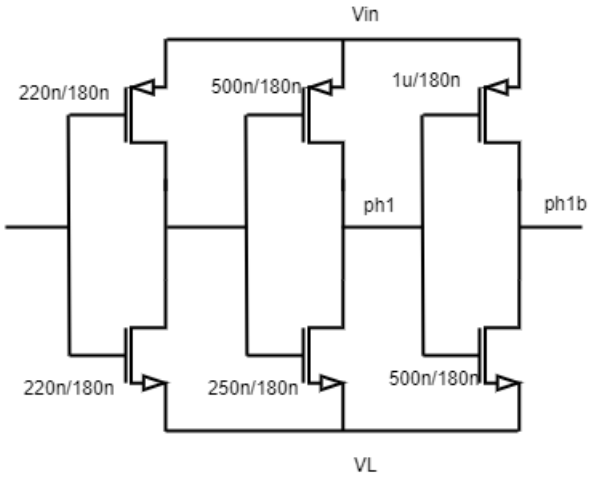

Figure 3.3: gate driver implementation

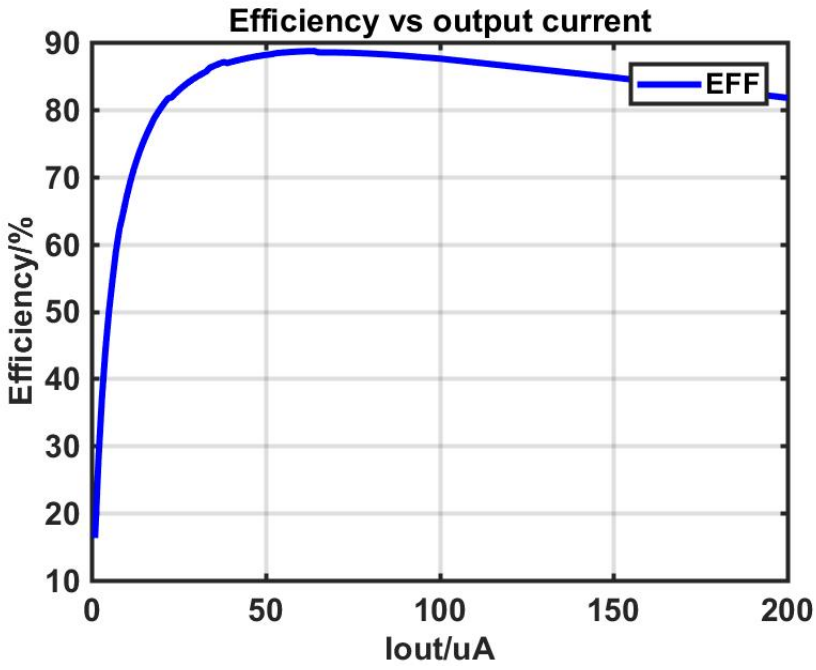

Figure 3.4: 2:1 SC stage Efficiency vs output current

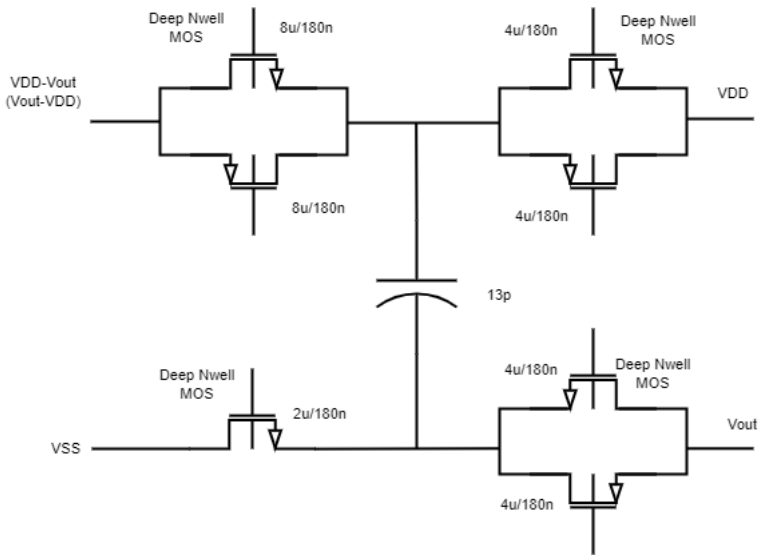

Figure 3.5: VDD-Vout implementation

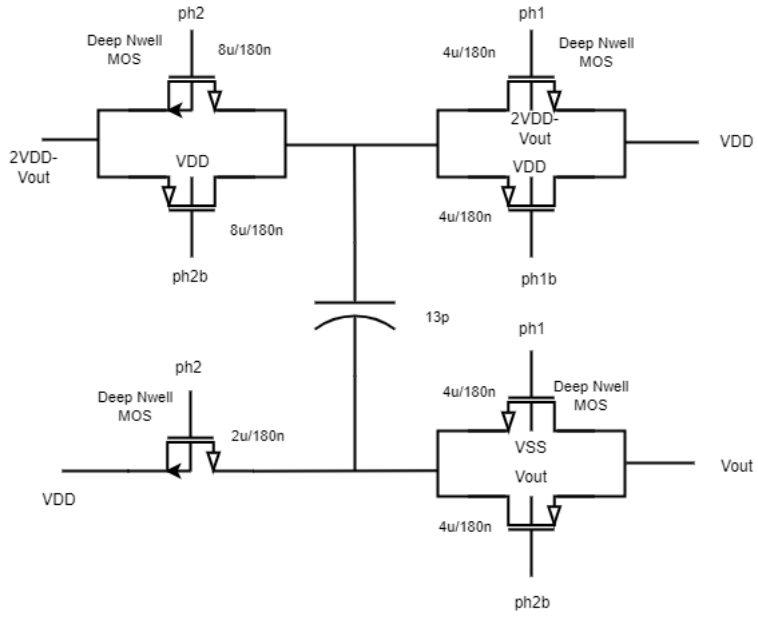

Figure 3.6: 2VDD-Vout implementation

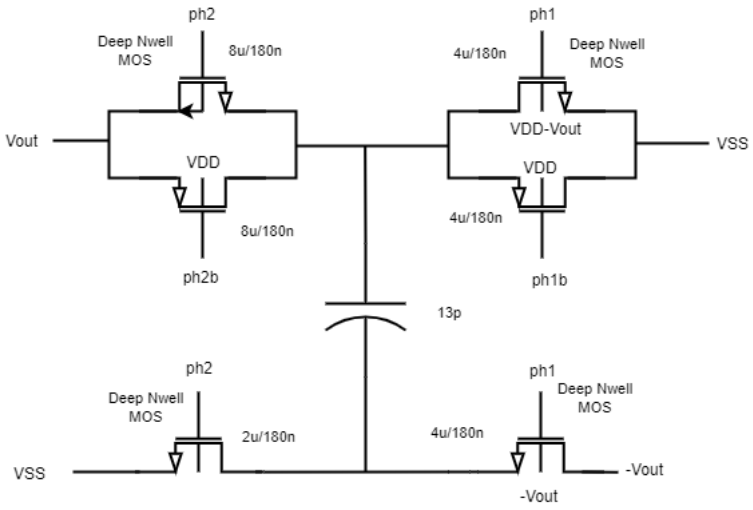

Figure 3.7: -Vout implementation

phases. In this way, the charge injected to V_out is smaller by N-times. Therefore, the voltage ripple is reduced by N times. In the meantime, typically, large decoupling capacitors are required between cascaded stages, which occupy a large chip area, significantly reducing the power density. While, the interleaved technique utilizes N cells and N phases when one cell is supplying charge to the output, the other N-1 cells can act as decoupling capacitors; thus, no additional decoupling capacitor is required for interleaved SCPC, which is also an essential advantage of the interleaved technique. The implementation of interleaved SCPC in this design is shown in Figure3.10. The angle difference between 2 cells is 36 degrees, and in total, there are 10 phases involved with a capacitance of 130p in total.

3.3 Stage Capacitive Sizing

In this 3-stage design, the load current drive capability is multiplied by 2 in buck operation and divided by 2 in boost operation. For buck situations in which no negator is applied(working like an RSC), each stage loads half of the output charge on the input and VDD or VSS. For 3-stage cascaded SC converter, the output charge for each stage can be expressed by $q_{out,i} = \frac{qout}{2^{3-i}}$, which gives $q_{out,1}$,$q_{out,2}$,$q_{out,3}$ are separately 1/4 q_{out},1/2q_{out},q_{out}.Thus,The R_{SSL} and R_{FSL} can be summarized in the following equations:

$$R_{SSL} = \frac{1}{64}\frac{1}{f_s C_1} + \frac{1}{16}\frac{1}{f_s C_2} + \frac{1}{4}\frac{1}{f_s C_3} \tag{3.1}$$

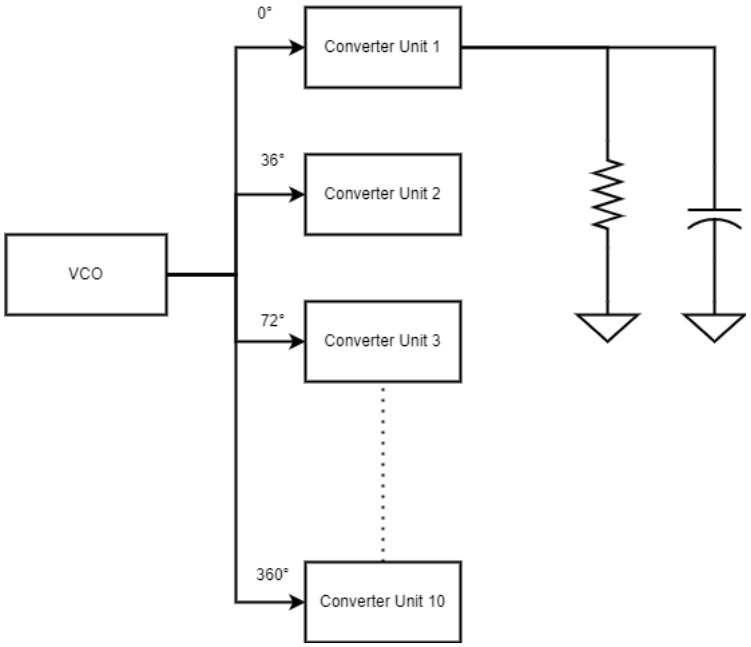

Figure 3.8: interleaved 10-phase SCPC

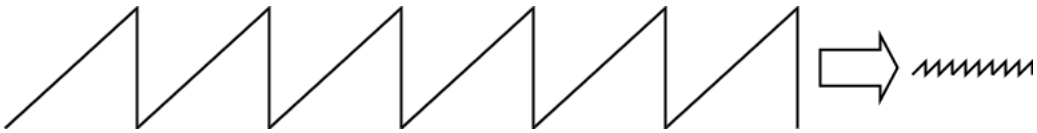

Figure 3.9: interleaved 10-phase SCPC

$$R_{i,FSL} = 2(R_i, 1 + R_i, 2 + R_i, 3 + R_i, 4)R_{FSL} = \frac{1}{64}R_{1,FSL} + \frac{1}{16}R_{2,FSL} + \frac{1}{4}R_{2,FSL} \tag{3.2}$$

R_i, j indicates resistance of jth switch of i SC stage.

Based on these 2 equations, we can apply Lagrange multiplier to calculate the optimum Capacitance and Resistance for each stage. Based on the equation 3.1 and 3.3,

$$C_1 + C_2 + C_3 = C_{total} \tag{3.3}$$

we can get the following:

$\frac{\partial R_{SSL}}{\partial C} =$

$$\begin{cases} -\frac{1}{64fC_1^2} = \lambda \\ -\frac{1}{16fC_2^2} = \lambda \\ -\frac{1}{4fC_3^2} = \lambda \end{cases} \tag{3.4}$$

thus,

$$\frac{1}{64fC_1^2} = \frac{1}{16fC_2^2} = \frac{1}{4fC_3^2} \tag{3.5}$$

$$C_3 = 2C_2 = 4C_1 \tag{3.6}$$

$$\begin{cases} C_3 = \frac{4}{7}C_{total} \\ C_2 = \frac{2}{7}C_{total} \\ C_1 = \frac{1}{7}C_{total} \end{cases} \tag{3.7}$$

In similar way, we can get

$$R_1 = 2R_2 = 4R_3 \tag{3.8}$$

Based on the calculation above, we can easily find the solution to minimize the R_{FSL} and R_{SSL}, that is, to parallel two interleaved stages in the second stage and parallel 4 interleaved stages for the final stage. each cell has a capacitance of 13p,10 phases in total is 130p, and 1+2+4 units are required for 2:1 stages, there are also 3 units reserved for negators, therefore, in total, the system consists of 10 10-phase interleaved stages with total capacitance of 1.3nF.

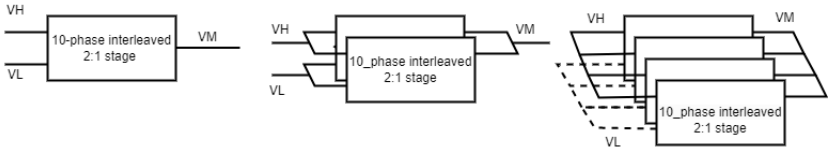

Figure 3.10: 3 stage capacitive sizing

3.4 VCO

As previously explained,we need 10-phase clock signals to drive interleaved cells. And our designed optimized switching frequency is 20MHz. The VCO applied in this design can realize 5-bit binary fine-grain control of the switching frequency. It consists of 5 inverter cells to form a ring oscillator. Ring oscillator is an astable circuit that ties N inverters in a loop to get N phases[21], and by inverting these N phases, 2N phases can be obtained. The oscillation frequency is determined by the propagation delay of each inverter. Thus, in this design, every inverter cell has a binary configurable current source to alter the delay of the inverter cell. cn and cp are the bias voltage of NMOS and PMOS, respectively.The implementation is shown in Figure3.11 and Figure3.13

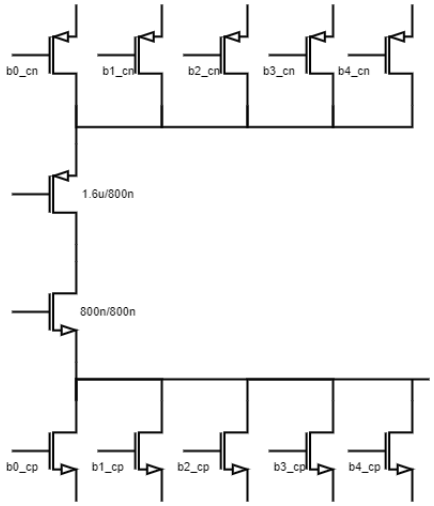

Figure 3.11: VCO inverter cell

3.5 Non-overlap Circuit

The SC stages should work in 2 inverse phase with phase difference 180°.Owing to the propogation delay of clock signal, the clock signal may coincide with each other, this will create a direct low impedance path from VDD to ground and would leakage significant current and cause severe power losses.Thus,Non-overlap Circuits are necessary to every clock signal with different phases.The input clock would generate 2 clock signals with inverse phase with a deadtime lies between them.During dead time, both phases are set to low, preventing both switches from opening at the same time,thus avoiding the shoot-through current and reducing the power losses.

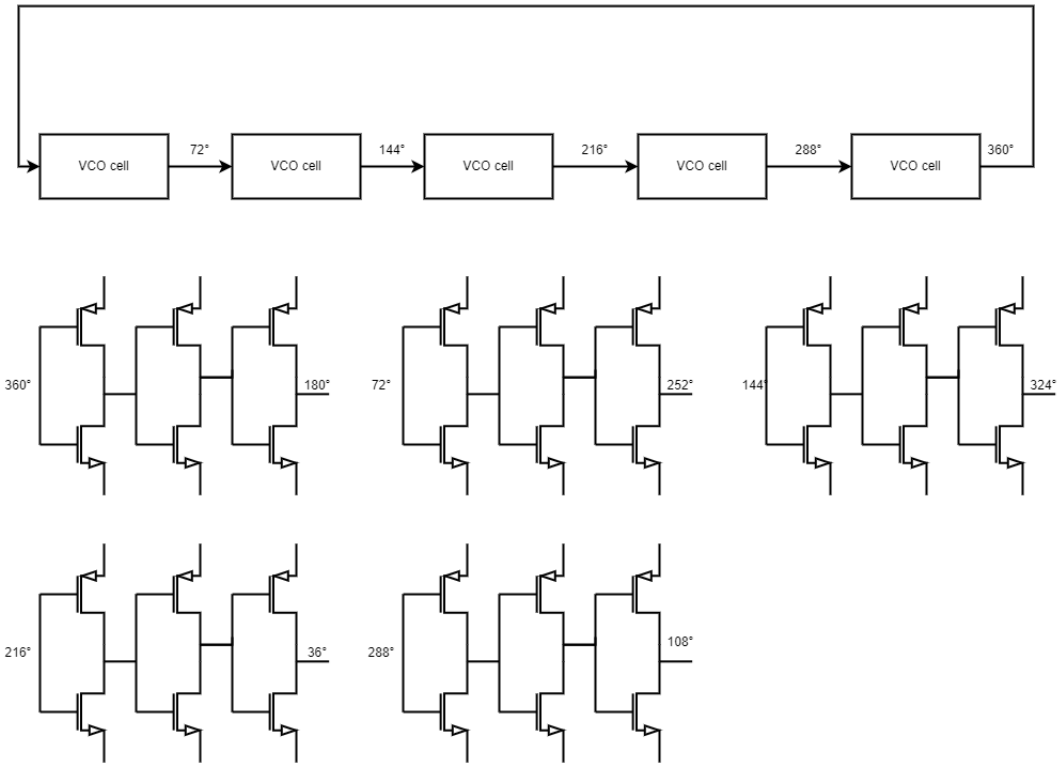

Figure 3.12: 10-phase VCO

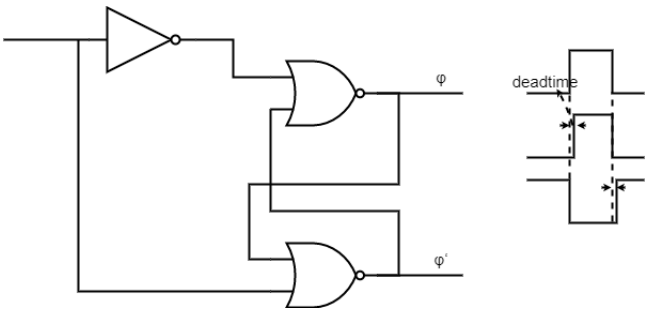

Figure 3.13: Non-overlap Circuit

3.6 VCR configuration

The VCR configuration module includes a decoder that receives 3 binary inputs to control the node connection from:VDD,Vout,VSS, A,B,C,D, float, in total 8 choices. This scheme can realize standardized code configuration and involve all possible situations, as there are no more than 4 intermediate nodes in all 158 VCRs.Take Figure 3.14 as an example; one of the most complex VCR topologies of the system, there are still only 4 intermediate nodes. The decoder setting is as follows:000 represents V_{SS},001 represents V_zin,010 represents V_{out},011 represents A,100 represents B,101 represents C., 110 represents D,111 represents floating. This only applies to the 3 2-to-1 stages, and negators only use 2-bit control; 00 stands for not activating the module.01 config the modules into buck operation, the negators are configured as $V_{DD} - V_{out}$, $2V_{DD} - V_{out}$,$-V_{out}$; while 10 configs the modules into buck operation, the negators are configured as $V_{out} - V_{DD}$, $2V_{Out} - V_{DD}$,$-V_{DD}$.In total, 3*3*3+3*2 control bits are utilized to configure the system. The translation rule is summarized in Table3.1

Table 3.1: Connection Configuration Translation

Connection	Code	Connection	Code	Connection	Code		
VSS	000	Vin	001	Vout	010		
Connection	Code	Connection	Code	Connection	Code		
A	011	B	100	C	101		
Connection	Code	Negator Mode	Code	Negator Mode	Code	Negator Mode	Code
D	110	Disable	00	Buck	01	Boost	10

Considering the control code,the situation that VCR =9/16 can be taken as an example.For 2:1 stage 1,VH1 is connected to B,thus the code is 100, VL1 is connected to A,the code is 011,VM1 is connected to C,the code is 101;In terms of second stage,VH2 is connected to A, the code is again 011,VL2 is connected to C, the code is 101,VM2 is connected to D,the code is 110,and the 2 negators are activated and works in buck operation,thus the code are both 01,$-V_{out}$ is not applied, thus the code is 00.Therefore,The whole controlling sequence is 100 011 101 011 101 110 011 110 010 01 01 00. Figure3.2 is a more intuitive table demonstrating the configuration of VCR=9/16

Table 3.2: Example Configuration of VCR=9/16

VCR	VH1	Code	VL1	Code	VM1	Code
9/16	B	100	A	011	C	101
	VH2	Code	VL2	Code	VM2	Code
	A	011	C	101	D	110
	VH3	Code	VL3	Code	VM3	Code
	A	011	D	110	Vout	010
	V4	Code	V5	Code	V6	Code
	Buck	01	Buck	01	Disable	00

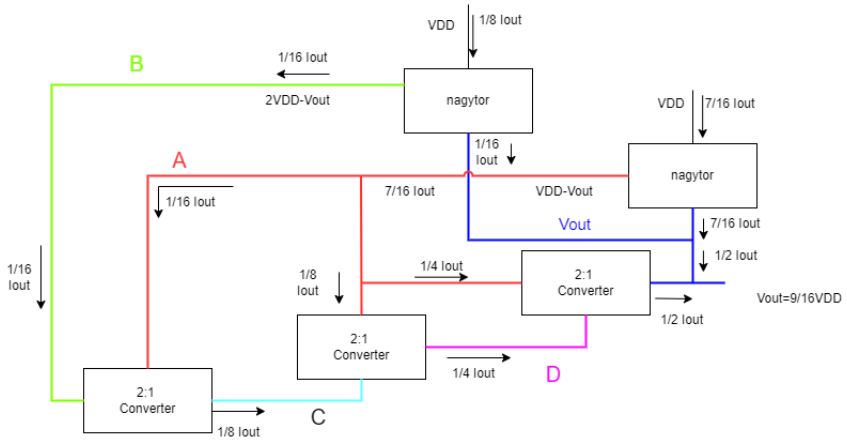

Figure 3.14: Example Connection of VCR=9/16

Chapter 4

Simulation Result

In this project, all post-layout simulations are done by cadence fabricated in a 180nm BCD process. Figure4.1 is the layout design finished for this project. Noticeably, there are ten columns of switch capacitor units, which are 3 SC stages with a capacitance ratio of 4:2:1 in addition to 3 negators. And there are also 10 rows of identical modules, which are 10-phase interleaved SC cells. The small module on the left hand is the VCO feeding clock signal to SC stages. There are also VCR Configuration Switches on top to control the connection of stages in each topology. The total area without the pad is 983μ m*1920μ m, which is 1.887 mm^2 without pads. Considering the pads, a space around 200um should also be included. The total area should be 983μ m*2120μ m= 2.084 mm^2. All the transistors utilize NMOS2V and PMOS2V model from the tsmc18 library, and the supply voltage is a nominal voltage of 2V.

The peak efficiency is obtained at VCR=1/2 with an efficiency of 82.38% @V_{in}=1V,I_{out}=6.4mA with an operation frequency of 20MHz.Figure4.3 has demonstrated the power loss breakdown of this system. Nearly 10%(9.38%) of the energy is consumed by output impedance, while the drivers consume 5.69% of the power, the VCO consumes 1.178% of total power, and the non-overlap circuits consume 1.168%. The conduction loss and switching loss are generally balanced. The output resistance can be calculated by the slope of the output voltage, which is 15$m\Omega$.

Figure4.4, 4.5, 4.6, 4.7demonstrates the topologies of VCR=7/8 and VCR=13/15 and their efficiency comparisons both for buck and boosting operation.when the system is configured as VCR=7/8(0.875),the topology is the same as Recursive topology.13/15(0.867) is the ratio closest to 7/8 negator-based topology can realize. The respective Peak Efficiencies are 75.77% and 70.45%(72.83% and 65.35% respectively for boost).The negator-based topology has expanded the VCR range with the cost of an acceptable efficiency drop. This additional loss is the result of switching loss of negators and cascaded charge-sharing loss,moreover, the output resistance

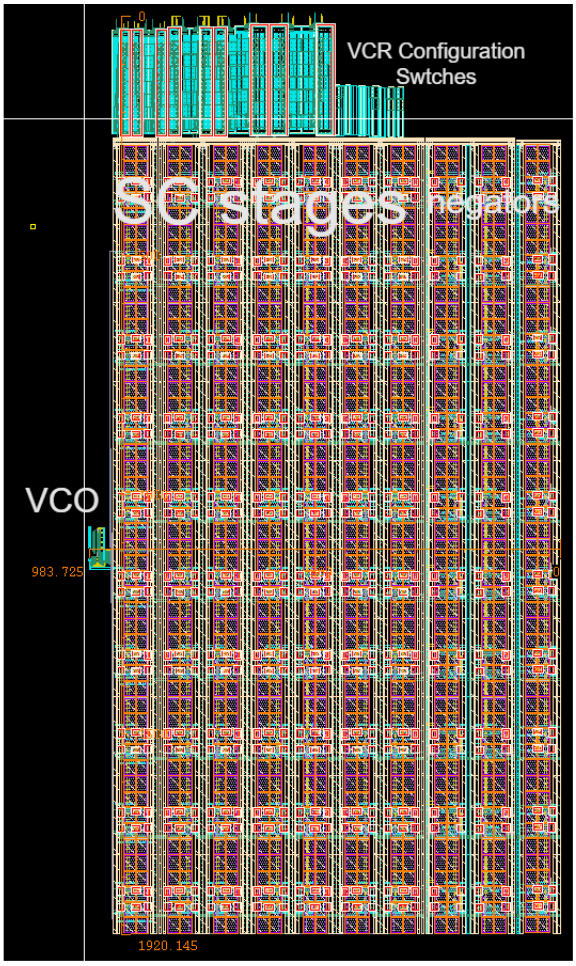

Figure 4.1: Layout design of the negator-based 79-VCR buck-boost converter

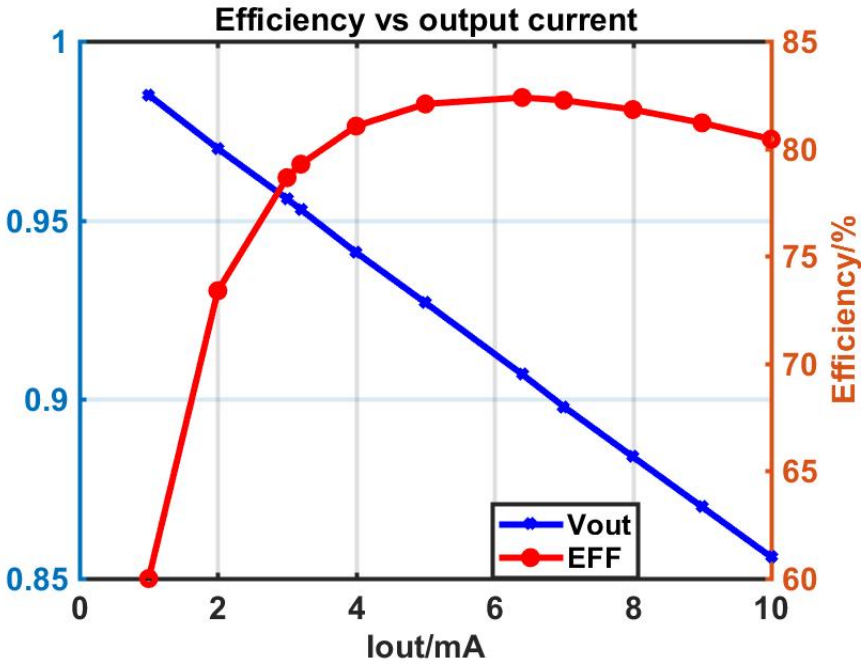

Figure 4.2: output voltage and Efficiency vs output current(VCR=1/2)

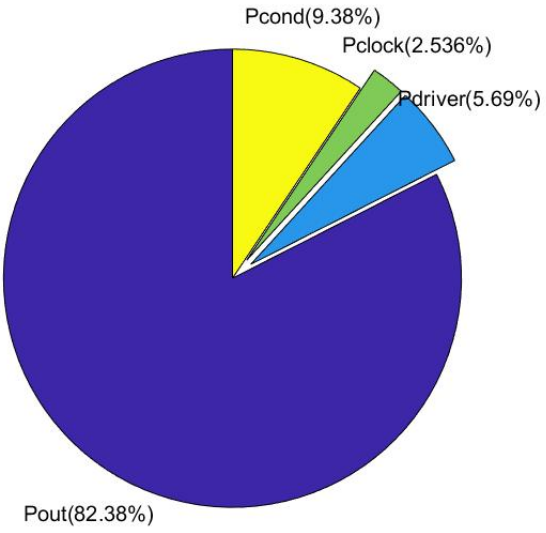

Figure 4.3: output voltage and Efficiency vs output current(VCR=1/2)

also increases as the stages increases.

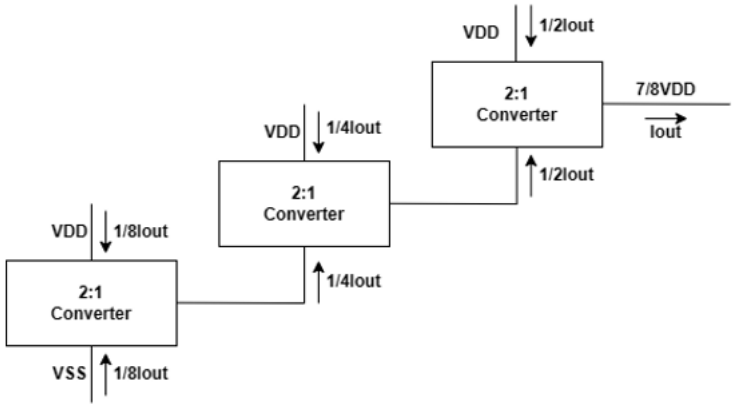

Figure 4.4: topology of VCR=7/8)

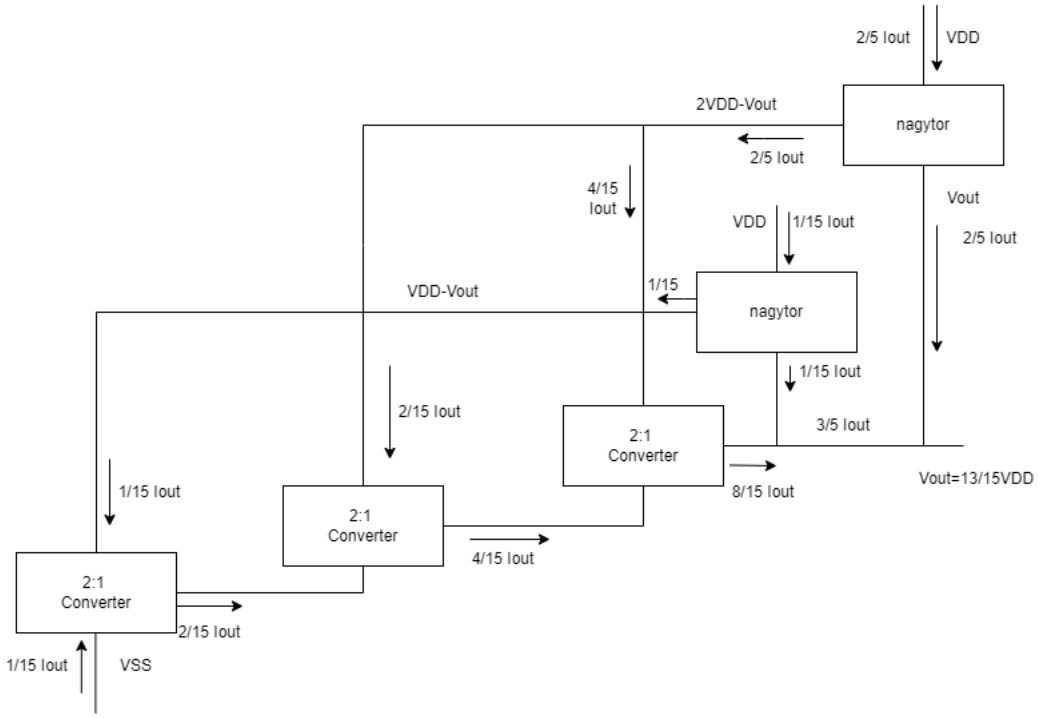

Figure 4.5: topology of VCR=13/15)

Figure4.8, 4.9 4.10 and4.11 also present another efficiency comparison and respective topology of similar ratios(3/4 and 10/13 and vice versa for boost operation).The peak efficiencies are respectively 71.23% and 63.89% for buck conversion and that for boost conversion are separately

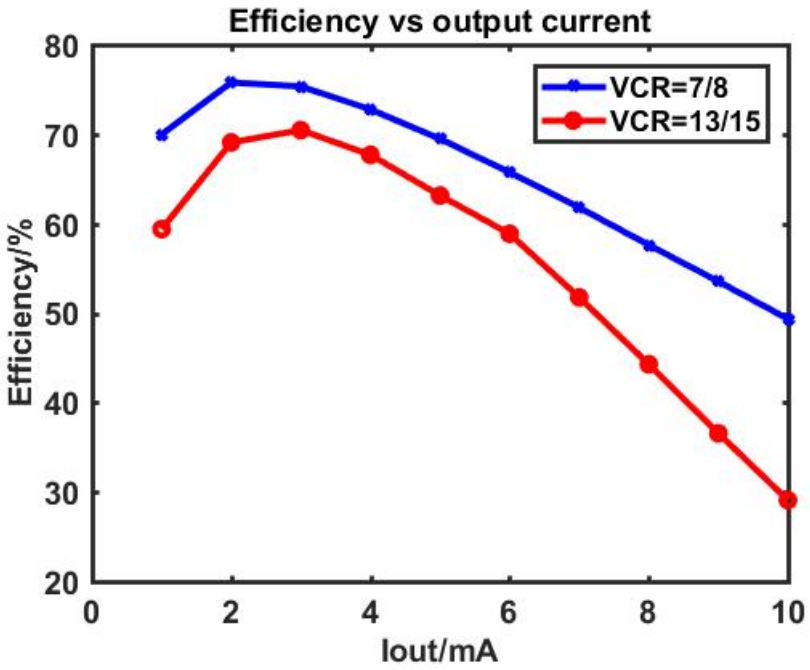

Figure 4.6: output voltage and Efficiency vs output current(VCR=7/8 and VCR=13/15)

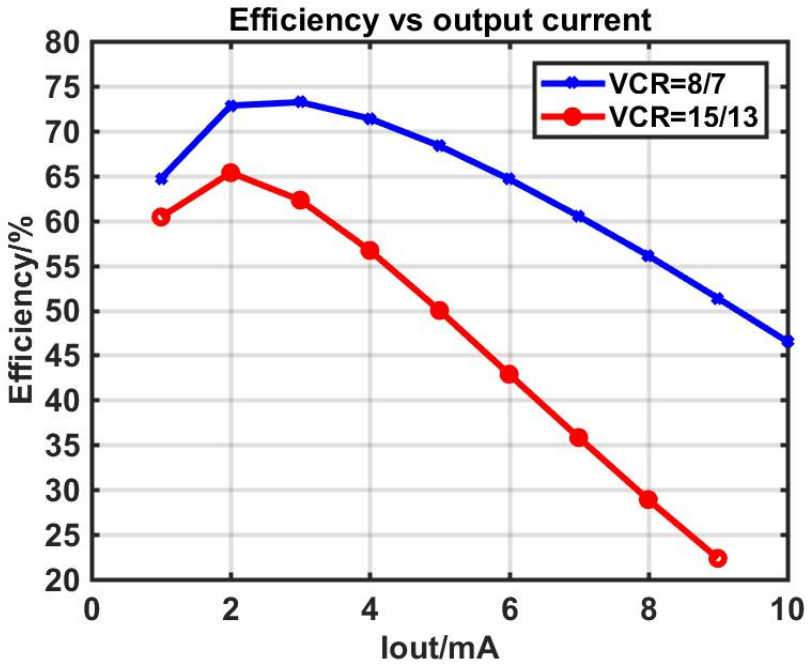

Figure 4.7: output voltage and Efficiency vs output current(VCR=8/7 and VCR=15/13)

71.67% and 62.73%.It fit the intuition that a simpler topology has less power loss than a more complex one.In 3/4 topology, only 2 SC cells are involved. While when the circuit is configured as 10/13,all 3 SC stages are utilized along with a negator.Therefore,more switches to be switched and a longer current path to follow, which naturally cause more switching loss and charge sharing loss and higher output impedance.

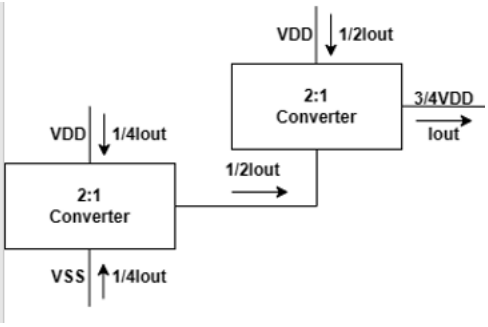

Figure 4.8: Topology of VCR=3/4)

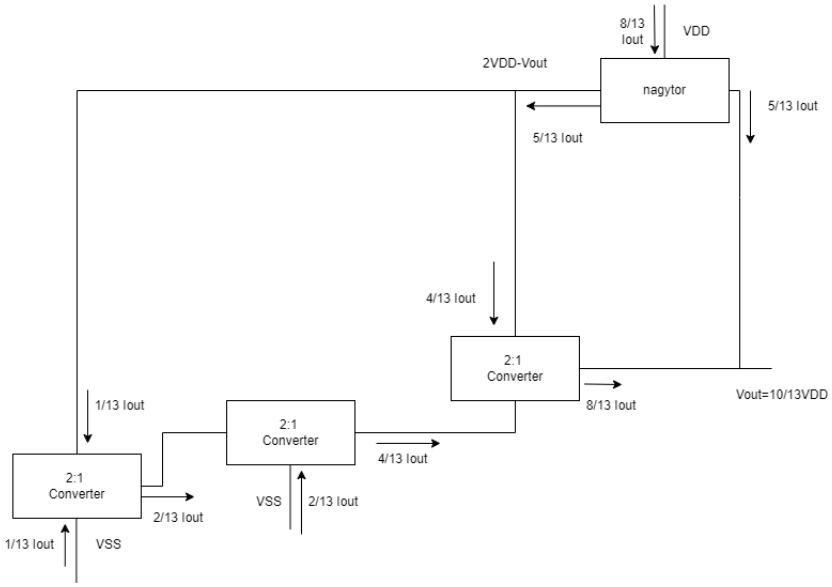

Figure 4.9: Topology of VCR=10/13

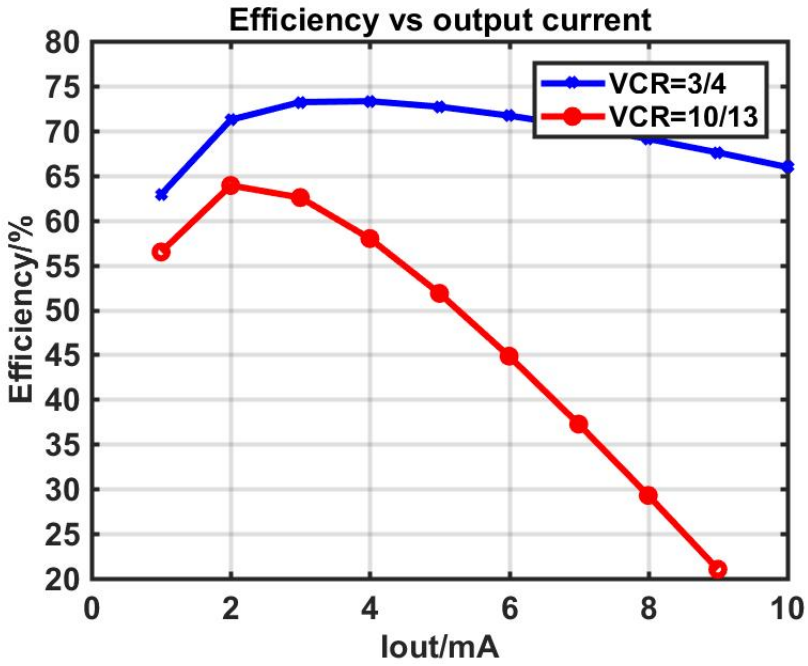

Figure 4.10: output voltage and Efficiency vs output current(VCR=3/4 and VCR=10/13)

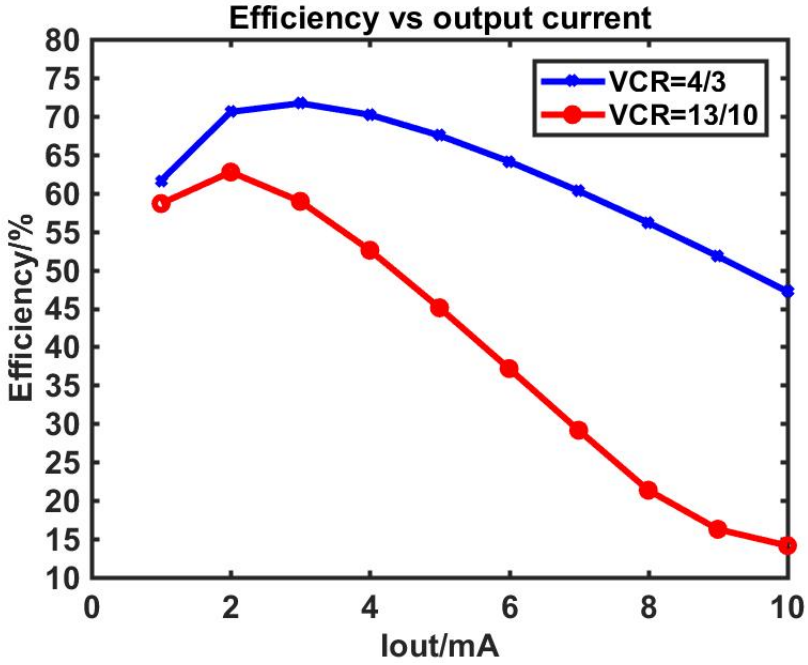

Figure 4.11: output voltage and Efficiency vs output current(VCR=4/3 and VCR=13/10)

Chapter 5

Conclusion

This paper proposes a 3-stage Switch-Capacitor system that can generate 79 Voltage Conversion Ratios for both buck operation and boost operation. The system consists of 3 SC stages with a capacitance size ratio 4:2:1 and three negator modules to provide voltage feedback of $V_{DD} - V_{out}$,$2 * V_{DD} - V_{out}$,$-V_{out}$.By written the Voltage conversion ratio into the form of $AV_{DD} - BV_{out}$,every rational ratio p/q between $1/2^{n+1}$ and $(2^{n+1} - 1)/2^{n+1}$ can be realized(79 rather than 7 in previous multi-VCRs design). The boost operation can be realized by exchanging ports for V_{in} and V_{out} because of the duality of Switch Capacitors. The total capacitance included is 1.3nF.Peak efficiency is obtained at 2:1 ratio @V_{in}=1V,I_{out}=6.4mA.Thus, output power with peak efficiency is 6.4mW. As the estimated layout area with pads addon is 2.084 mm^2, the estimated power density at maximum efficiency would be 3.07 mW/mm^2.The voltage conversion ratio is successfully expanded with the cost of an acceptable efficiency degradation owing to switching loss and cascaded charge-sharing loss. With an input voltage of 2V, the output voltage range can vary from 125mV to 1.875V with fine-grained 79 intermediate voltage choices.

5.1 Future Work

- **Self Clock Activation** Currently, the VCO of the system is supplied by external power supplies.An improved edition could offer modes with options to choose between internal and external supplied clock.The challenge lies in the generation of a higher voltage to supply the clock signal and allow VCO to operate normally in a much lower voltage range, and undoubtedly, efficiency is expected to be low as the resistance increase dramatically without a sufficient supply voltage.Meanwhile, the supply need to be separately generated for each stage,as each stage has a different dynamic range,resulting in increase of system complex-

ity.The boosting of clock signal can apply circuit structure like shown in Figure5.1.There would be a voltage difference around V_{DD} stored on both capacitors, whenever CK is pulled high, the capacitor would boost the clock signal to $2 * V_{DD}$, turning on the upperleft NMOS,charging the capacitor on left with voltage potential of V_{DD}. When CK is pulled low, this voltage potential can also open the upperright NMOS to charge the capacitor on right with voltage potential of V_{DD}.This module can solve the problem of clock boosting of 2:1 stages, while negators, in many cases, would have a voltage range larger than $2 * V_{DD}$,such as $2 * Vout - VDD$ with a large VCR, which would be a challenge to be solved.As a negative feedback system, if the voltage of one module fails to establish, then the whole system would work incorrectly as expected.

- **The voltage range can be further expanded to 5V.** Currently the system can only support input and output voltage of 2V,owing to the reason that 5V suffers from intrinsic high parasitic resistance and capacitance.Meanwhile, the voltage range of each SC stage and negator is not constant in each topology.Thus, the 2V transistors and 5V transistors need to be switched by off-chip signals, resulting into more pins to be added,increasing the cost and difficulty of packaging.

- **Reducing the switching loss** Currently, the switching loss of the system is a quite significant portion of total power loss.Interleaved and capacitive sizing reduces the output ripple and output impedance, while breaking the system into small modules results into more phases of signal to be generated and more switches to be driven.The switching loss may be improved by interleaving 5 phases rather than 10 phases,which may trade better efficiency with releasing the boundary for voltage ripple.

- **Closed feedback loop control** Currently,the system regulates the output voltage only by open loop intrinsic voltage conversion ratios,which results in output voltage variation for different output current.With a closed feedback loop control, the output can be regulated to constantly supply one voltage.The closed feedback loop control system can be chosen including CFM(Continuous Frequency Modulation),Hysteresis Control,Pulse-skipping Control, etc.

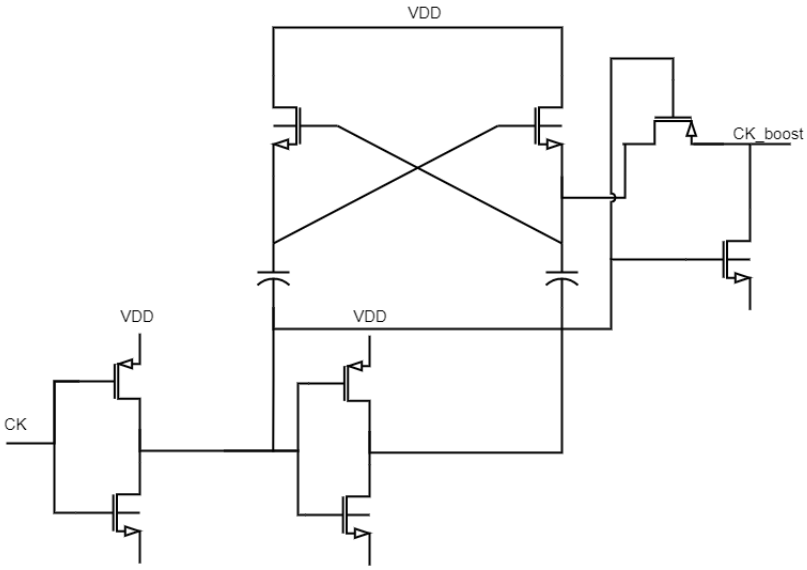

Figure 5.1: clock booster

Bibliography

[1] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, 2011. 1, 1.2

[2] Q. Li, Y. Dong, and F. C. Lee, "High density low profile coupled inductor design for integrated point-of-load converter," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 79–85. 1

[3] J. Wibben and R. Harjani, "A high-efficiency dc–dc converter using 2 nh integrated inductors," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, 2008. 1

[4] M. Wens and M. Steyaert, "A fully-integrated 130nm cmos dc-dc step-down converter, regulated by a constant on/off-time control system," in *ESSCIRC 2008 - 34th European Solid-State Circuits Conference*, 2008, pp. 62–65. 1

[5] T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic capacitive dc-dc converter with single boundary–multiphase control and voltage domain stacking in 90 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1715–1727, 2011. 1, 1.1

[6] T. V. Breussegem and M. Steyaert, "A 82integrated capacitive voltage doubler," in *2009 Symposium on VLSI Circuits*, 2009, pp. 198–199. 1, 2.2

[7] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, "A fully integrated successive-approximation switched-capacitor dc-dc converter with 31mv output voltage resolution," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 370–371. 1, 2.2.3.1, 2.2.3.1

[8] L. G. Salem and P. P. Mercier, "4.6 an 85%-efficiency fully integrated 15-ratio recursive switched-capacitor dc-dc converter with 0.1-to-2.2v output voltage range," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 88–89. 1, 2.10

[9] W. Jung, D. Sylvester, and D. Blaauw, "12.1 a rational-conversion-ratio switched-capacitor dc-dc converter using negative-output feedback," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 218–219. 1, 2.2.4

[10] S. THOMAS, "Understanding the role of bms in electric vehicles," https://www.einfochips.com/blog/understanding-the-role-of-bms-in-electric-vehicles/. 1.3

[11] D. N. Williams, "Future of smart health systems," https://www.news-medical.net/health/Future-of-Smart-Health-Systems.aspx. 1.4

[12] J. Yan, X. Zhu, and N. Lu, "Smart hybrid house test systems in a solid-state transformer supplied microgrid," 07 2015, pp. 1–5. 1.5

[13] H.-P. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor dc-dc converter delivering 0.55w/mm2 at 81Solid-State Circuits Conference - (ISSCC) 2.2

, 2010, pp. 210–211.

[14] G. Zhu and A. Ioinovici, "Steady-state characteristics of switched-capacitor electronic converters," *Journal of Circuits, Systems and Computers*, vol. 07, 11 2011. 2.2

[15] Z. Ye, Y. Lei, and R. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1–1, 10 2019. 2.2

[16] H.-P. Le, S. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *Solid-State Circuits, IEEE Journal of*, vol. 46, pp. 2120 – 2131, 10 2011. 2.2.1

[17] S. R. Pasternak, M. H. Kiani, J. S. Rentmeister, and J. T. Stauth, "Modeling and performance limits of switched-capacitor dc–dc converters capable of resonant operation with a single inductor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1746–1760, 2017. 2.2.1, 2.6

[18] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93reconfigurable switched-capacitor dc-dc converter using on-chip ferroelectric capacitors," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 374–375. 2.2.3

[19] G. K. Kumar, T. Kobaku, S. Sahoo, B. Subudhi, D. Elangovan, and F. Blaabjerg, "An overview of fully integrated switching power converters based on switched-capacitor versus

inductive approach and their advanced control aspects," *Energies*, vol. 14, p. 3250, 06 2021. 2.7

[20] A. Bonetti, "Low power and compact successive approximation adc for bioelectronic chips," Ph.D. dissertation, 04 2012. 2.2.3.1

[21] S. L. Harris and D. Harris, "5 - digital building blocks," in *Digital Design and Computer Architecture*, S. L. Harris and D. Harris, Eds. Morgan Kaufmann, 2022, pp. 236–297. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780128200643000052 3.4