High energy yield Bifacial-IBC solar cells enabled by poly-SiO_x carrier selective passivating contacts

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High energy yield Bifacial-IBC solar cells enabled by poly-SiO_X carrier selective passivating contacts

By

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Conference Abstract

Evaluation and demonstration of bifacial-IBC solar cells featuring poly-Si alloy passivating contacts- Guangtao Yang, Zakaria Asalieh, Paul Procel, YiFeng Zhao, Can Han, Luana Mazzarella, Miro Zeman, Olindo Isabella – *EUPVSEC 2021*

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Zakaria Asalieh

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Abstract

Carrier selective passivating contacts (CSPC) are promising contact structures for high efficiency silicon solar cells. They provide silicon surface passivation as well as high carrier selectivity. In this thesis, the bifacial interdigitate back contacted cell concept (bifacial IBC) is combined with the interdigitated back-contacted (IBC) structure with the bifacial concept for the purpose of further improve the solar cell output. It is enabled by poly-SiO_X as CSPCs. The main aim of this thesis project is the preparation of proof of concept bifacial IBC cells. In this work, two process flowcharts for bifacial IBC solar cell fabrication are presented: (1) poly-SiO_X fingers patterned by ion-implantation through photoresist masking layer, (2) wet chemical patterning of in-situ doped poly-SiO_X. In the first process, the optimization of poly-SiO_x passivating contact was performed by varying the intrinsic a-SiO*x*:H layer thickness. The best passivation results obtained from this approach was 646 mV, and 623 mV for the n^+ and p^+ layer, respectively. In the second process, the thickness of doped p^+ and n^+ poly-SiO_x layers was also optimized for the symmetrical test samples based on the requirement of bifacial IBC solar cell flowchart. As a consequence, a 25 nm thick p^+ poly-SiO_x layer and a 40 nm thick n^+ poly-SiO_x layer recorded highest iV_{OC} performance. Next, the hydrogenation treatment is applied to further optimize the samples passivation quality. This results in an overall passivation of 714 and 730 mV for p^+ and n^+ poly-SiO_X symmetrical samples, owed to the fact that the high hydrogen content in SiN_X layer boosting the passivation properties of the poly-SiO_X passivating contacts.These findings of the optimized poly-SiO_X passivation contacts are used to fabricate the bifacial-IBC solar cell. As a result, using the wet-etching patterning of in-situ poly-SiO_X CSPC flow chart, a demonstration proof of this cell principle is obtained with V_{OC} of 649 mV, FF of 44,3 %, J_{SC} of 40,7 mA/cm^2, and efficiency of 12% for the best solar cell. The losses analysis of such cell performance was also conducted.

Contents

Nomenclature

Poly-SiO_X	Oxygen Alloyed Polycrystalline Silicon
Poly-Si	Polycrystalline Silicon
τeff	Minority Carrier Lifetime
Eg	Bandgap
η	Conversion efficiency
EC	Conduction Band
ρ_C	Specific Contact resistance
EV	Valance Band
a-Si	Amorphous Silicon
FBC	Front and Back Contacted
Ag	Silver
FF	Fill Factor
Al	Aluminum
FG	Forming Gas
ALD	Atomic Layer Deposition
FZ	Float Zone
ARC	Anti-reflection Coating
HF	Hydrofluoric Acid
B	Boron
HNO_3	Nitric Acid
BHF	Buffer Hydrofluoric Acid
iV_{OC}	Implied open-circuit voltage
c-Si	Crystalline Silicon
IBC	Interdigitated Back Contact
CSPC	Carrier Selective Passivating Contacts

ITO	Indium Tin Oxide
TMAH	Tetramethylammonium Hydroxide
J_0	Recombination Current Density
VOC	Open-Circuit Voltage
JSC	Short-circuit Current density
PECVD	Plasma Enhanced Chemical Layer Deposition
LPCVD	Low Pressure Chemical Vapor Deposition
PV	Photovoltaics
NAOS	Nitric Acid Oxidation of Silicon
Rs	Series Resistance
N_2	Nitrogen
Rshunt	Shunt Resistance
O_2	Oxygen
Cu	Copper
P	Phosphorous
ITO	Indium Tin Oxide
SEM	Scanning Electron Microscopy
J_0	Recombination Current Density
SRH	Shockley-Read-Hall
JSC	Short-circuit Current density
STC	Standard Test Conditions
SiH4	Silane
SiN_X	Silicon Nitride
TCO	Transparent Conducting Oxide

1 Introduction

One of the most significant challenges that Humanity has to face nowadays, with the increasing population, is growing worldwide demand for energy. EIA projects that world energy consumption will increase by almost 50% by 2050 led by Asia [1]. The loss of traditional energy sources such as coal, oil and natural gas is increasing which will arise the problem of the scarcity and environmental impact. All previous reasons will place the human beings against the predicated energy crisis in the next decades [2]. Despite the increasing of energy demand, approximately 1.1 billion people are still living without having access to these goods [3]. These circumstances indicate the importance of shifting from conventional energy to a more renewable and abundant source. Comparing all energy resources, solar energy represents one of these alternatives and play a vital role in this energy transition. Figure 1 indicates the approximate of finite and renewables planetary energy reserves by International Energy Agency (IEA) [4]. Analyzing solar energy sources, it is very clear that it has gained so much attention in recent years because of its abundance relative to other energy sources. Theoretically, solar energy can produce 10,000 times more energy in comparation with current energy demand [5].

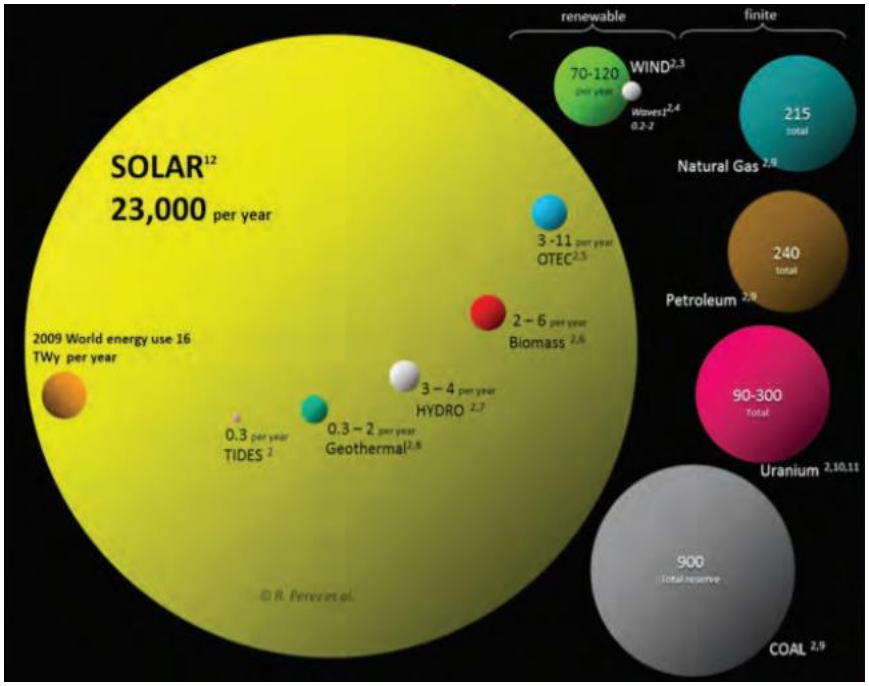

Figure 1.1: Energy sources power availability [4].

The French physicist Alexandre Edmond Becquerel discovered the photovoltaic effect in 1839. He Analyzed that conductance increases with illumination during his experiment with metal electrodes and electrolyte. Daryl Chapin, Calvin Fuller, and Gerald Pearson invented the first silicon solar cell at Bell Labs in 1954, with 4% efficiency. [6]. Addressing the current state of this technology, photovoltaic (PV) based on silicon have ruled the PV market over the last years. It worth to mention that silicon has significant advantages over other technologies since it is an abundant, cheap and non-toxic material [7].The silicon solar cell was governed in the early years by multi-crystalline solar cells , however in the recent years mono-crystalline silicon solar cells dominate the market by 39.6 and 89.7 GWp, respectively [8].

To harvest solar energy, photovoltaic (PV) system can directly convert the solar irradiance to electricity. The annual PV module global production from 2010 to 2019 are shown in Figure 2. The number of the annual PV module production increased from lower than 18 GW in 2010 to over 140 GW in 2019. The increase in PV production indicates that countries all over the world pay more attention to solar energy development. The Asian countries, especially China and Japan, contributes the most in the increment in PV market in last ten years [8].

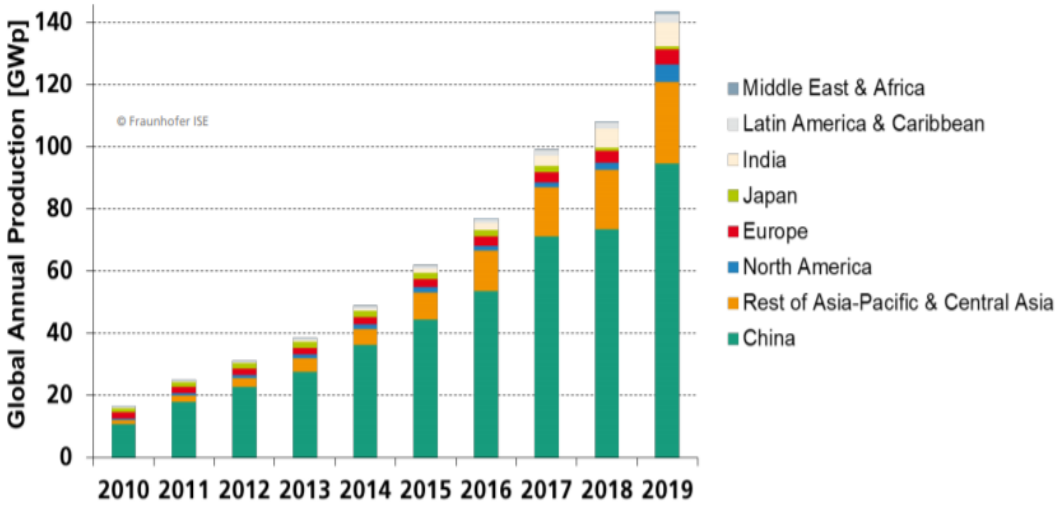

Figure 1.2 Global annual production [8]

Bifacial solar cell gains more attention in the solar cells research field because it not only captures the incident light on the solar cell front side but also the diffused and scattered light on the rear side as shown in figure 1.3. Therefore, in contrast to monofacial cells, bifacial solar cells will significantly increase power generation [5]. The last Research shows that the same active area can be expected to harvest 50 percent more electricity than the traditional monofacial solar cells [61]. However, this improvement can vary depending on the local albedo and the nonuniform shading conditions. A further advantage is that the solar cell working temperature is reduced due to the infrared absorption reduction in the rear metallization [62] which will enhance the solar cell performance.

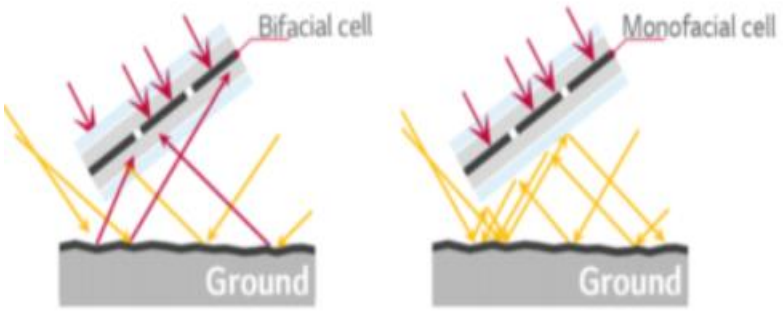

Figure 1.3: Comparison between the monofacial and bifacial solar cell [63].

1.1 Solar cell working principle

Photovoltaic (PV) effect is the core concept of the solar cell operation in which the light beams is converted into electricity using a solar cell. The photovoltaic effect provides a difference in the potential between two different materials due to the incident radiation. If the previous two materials were connected to an external circuit, it can be used to power a load. A solar cell's fundamental operating theory includes three main processes:

- Charge carrier generation occurs when an incident photon with a specific energy is absorbed by a semiconductor material. This results in an excitation of an electron from the valence band to the conduction band leaving a hole behind in the valence band. Thus, an electron-hole pairs are created within the material. The difference in energy between the valence band (Ev) and the conduction band (Ec) of the material is known as the band gab (Eg). It is worth noting that the electron-hole pair is produced only for absorption with energy equal to the material band gab e.g. Eg for crystalline silicon is 1.12 eV.
- Charge carrier separation this subsequent step is to prevent the generated charge carriers from recombining. This separation can be represented as the membrane that allows the passage of one form of charge carrier. This membrane is called the p-n junction in solar cells, which is created when semiconductors of the p-type and n-type are placed in contact.
- Collection of charge carriers is the last step which take place at the electrodes to extract the separated charge carriers from the solar cell. Electrons are passing through the external circuit, to utilize the electron energy, and recombine at the metal side with holes. In this particular step, the chemical energy is converted to useable electrical energy.

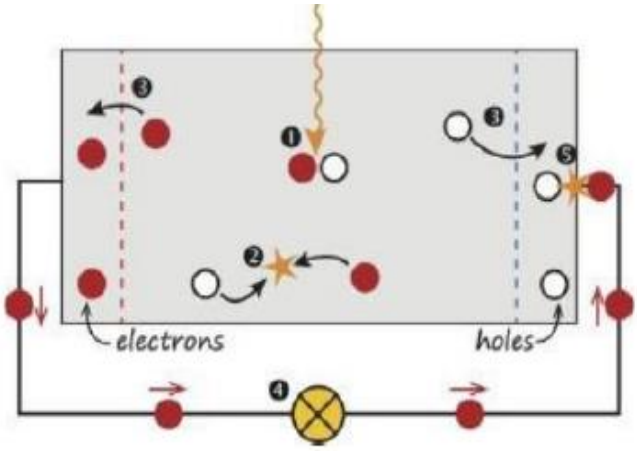

Figure 1.3 solar cell under the operation [5]

1.2 Loss Mechanisms

The losses in the solar cell are discussed in this section. There are two different losses categories optical and electrical losses. The spectral mismatch concerns a single-junction solar cell while optical and electrical represents the unsuccessful generation and absorption of the electron-hole pair.

1.2.1 Optical losses

The spectral mismatch is considered the largest optical loss mechanism. The spectral mismatch considers two important losses that suppress the efficiency of a solar cell. There other forms of optical losses that occur in the solar cell such as parasitic absorption, reflection and shading losses which can be explained as follow:

Thermalization: Photons with energy higher than material band gap is able to produce an electron-hole pair while excess energy of the photons will be lost and released as a heat in the semiconductor material.
Non-absorption: On the other hand, the absorption for photons with energy lower than the semiconductor band gap will not be possible. Due to this unsuccessful absorption, these photons do not produce electron-hole pairs and will pass through the semiconductor.
Parasitic absorption: The semiconductor material will absorb photons with energy equal to the semiconductor band gap and these photons will travel through the semiconductor material. However, these photons can be absorbed in non-photoactive areas such as ARC and TCO layers and do not contribute to charge carrier generation; this is called parasitic absorption.
Reflection losses: is the next main loss mechanism where the incidents photons can be reflected before reaching the absorber layer. These losses can be minimized by introducing ARC layer or by using a transparent conducting oxide (TCO) layer. Additionally, to achieve a better light trapping in the cell, surface texturing is applied to increase the photons path length through the cell.
Shading losses: These losses are mainly due to the metallization fingers at the solar cell front side that blocks the incident light on the surface reducing the short circuit current. Therefore, the metal contacts geometry should be optimized to reduce the shading effect. These losses can be fully eliminated by introducing the IBC solar cell topology, in which all the contacts are located at the solar cell rear side.

1.2.2 Electrical losses

Electrical losses take place within the absorber material due to the ineffective utilization of excited electrons. This can be attributed to the recombination of the electrons before being collected which results in the reduction of the available charge carriers and eventually undermine the solar cell performance. It is possible to separate these recombination losses into two main mechanisms: surface and bulk recombination. The bulk recombination was categorized into Radiative recombination, Auger recombination and Shockley-Read-Hall (SRH), Figure 1.4.

Surface recombination

Thanks to the progress made by the silicon manufactures, the material quality has improved and thus the bulk recombination suppressed significantly. Therefore, the major recombination mechanism for most c-Si solar cells is surface recombination. Surface recombination occurs due to the presence of dangling bonds on the semiconductor surface that acts as a defect state. These defects state later capture the charge carriers which boost the SRH recombination rate. In a p-type semiconductor, the surface recombination rate can be described by equations (1.1)

$$R_s \approx v_{th}\sigma_p N_{sT}(p_s - p_0) \qquad (1.1)$$

Where vth represents the surface recombination velocity, NsT the trap density at the surface σp is the holes capture cross section. According to the above equation, the surface recombination can be minimized in two ways. The first method is to reduce the number of dangling bonds (trap state) as the higher the trap density the higher probability of electron-hole recombination. On the other hand, increasing the doping concentration at the semiconductor surface can decrease minority carriers on the material surface. This creates a barrier that prevents minority charge carriers from being transmitted to the semiconductor material surface.

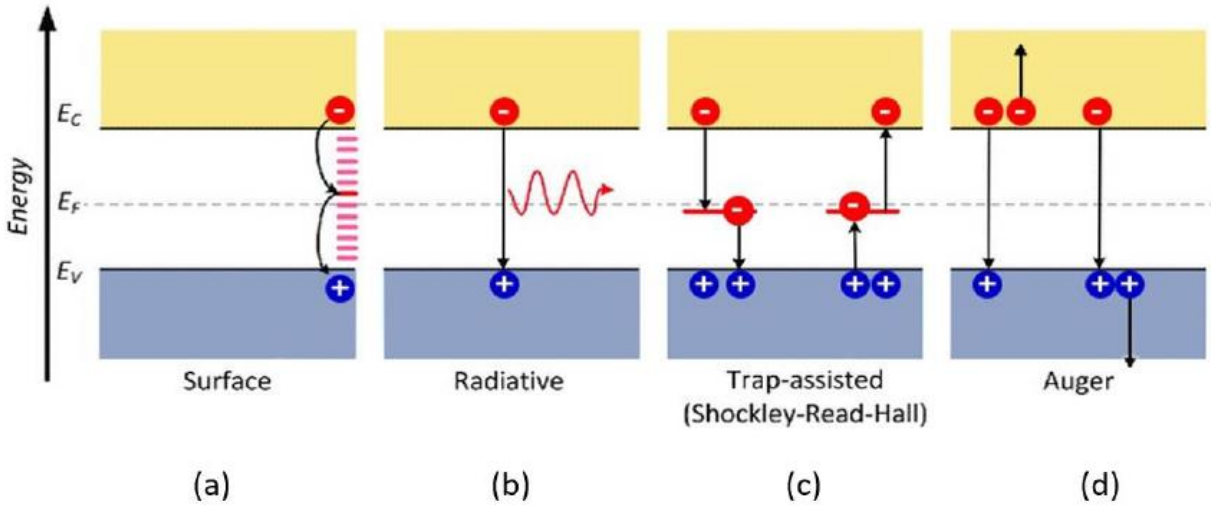

Figure 1.4: Diagram demonstrate the recombination mechanisms [5].

Radiative recombination

Radiative recombination is the reverse action of photon absorption, where an excited photon relaxed back to the original energy state and emit a photon with energy equal to the band gap. For the direct bandgap semiconductor materials, the radiative recombination is dominant such as gallium arsenide (GaAs). Therefore, it does not play a vital role in the c-Si solar cells and the excited electron will not easily relax back to the initial state of energy.

Auger recombination

This type of recombination in contrast is dominant in the direct materials. Auger recombination is a process that needs three particles where the excess energy is transferred to a third particle(hole/electron). This third charge is therefore excited to a higher energy level and relax back again to semiconductor edge by thermalization. As Auger recombination requires three particles, it represents a dominant recombination mechanism in the highly doped regions and depletion region due to the large number of free carriers.

Shockley Read hall Recombination

SRH recombination occurs due the presence of an intermediate energy level between the valence and conduction bands in the c-Si band gap. This trap state can be induced by the existence of a structural defects or material impurities. The charge carrier is trapped in the introduced energy level which introduce a path to move the electron down to the valence bard. Therefore, SRH decreases with increasing the material quality.

Resistive losses

It worth to mention that there are other types of losses in the c-Si solar cell. Charge carriers encounter different layers within the solar cell to reach the metal electrode. This is known as a series resistance experienced by the charge carrier. For better charge carrier collection at the electrode side, this value should be kept at low level to maximize the cell performance. Additionally, the leakage current through the p-n junction corresponds to the shunt resistance. For better performance, this value has to be as high as possible.

1.3 External Solar cell parameters

Solar cell parameters help to identify the properties and performance of the solar cell. These parameters are defined in this section, since they will be used in this thesis.

Short circuit current density

The short circuit current, Isc, is the current that run in the cell when the voltage across the solar cell is zero [5]. It depends on several factors such as the cell area, photon numbers and other optical properties (absorption and reflection). To neglect the dependency on area of the solar cell, the sort circuit current density is used rather than short circuit current.

Open circuit voltage

The open circuit voltage, Voc, is the maximum voltage that can be produce by the solar cell and it occurs when the current of the solar cell is zero [5]. Looking at Equation (1.2), it shows that Voc is related to I0 which depends on recombination in the solar cell. Therefore, it is used as a measure of the solar cell quality.

$$V_{OC} = \frac{k_B.T}{q}\ln\left(\frac{J_{ph}}{J_0}\right) \quad (1.2)$$

Fill factor

As shown above the short circuit current and open circuit voltage represent the maximum current and voltage respectively of the solar cell, but at these both points the power delivered by the device is zero [5]. Therefore, the maximum power of the solar cell is indicated by the fill factor, FF, as it is a key indicator of the cell performance. The FF can be calculated by the equation (1.3)

$$FF = \frac{P_{mpp}}{V_{oc}J_{sc}} \quad (1.3)$$

Conversion efficiency

The conversion efficiency of the solar cell is defined as the ratio of the energy out of the solar cell to the incident energy from the sun under standard test conditions (STC) [5]. STC conditions are at power available from the sun 1000 [W/m2] with the irradiance spectrum equal to AM1.5 spectrum and at a temperature of 25°C. The open circuit voltage (VOC) is calculated from Equation 1.4

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{SC}.V_{OC}.FF}{P_{in}} \quad (1.4)$$

1.4 Surface Passivation

As described above in section, solar cell influenced severely by surface recombination and it represent the major loss mechanism. In this section two treatment process namely chemical passivation and field-effect passivation are described which can be used to overcome this problem. A combination of these two techniques helps in creating a carrier selective passivating contact (CSPC) which results in a high passivation quality and it is discussed in detail later in the following section.

Chemical passivation

As discussed in section 1.2.2, to minimize the density of defects on the surface of the semiconductor material passivation techniques are used. Chemical passivation is done by introducing an ultra-thin layer which acts as insulation material on surface of the semiconductor material. The thin insulation layer will saturate the dangling bond at surface and usually also provide hydrogenation effect Figure 1.5. Common chemical passivation layers are silicon oxides (SiO_X), hydrogenated amorphous silicon (a-Si:H) and hydrogenated amorphous silicon nitride (a-SiNx:H) [9][10]. SiO_2 can be grown chemically, deposited by plasma enhanced chemical vapor deposition (PECVD) or thermally formed [11].

Next, silicon nitride is a hydrogen rich material and used to saturate the dangling bonds with the help of hydrogen. This process called hydrogenation and it explained in detail in section. Silicon nitride can also be deposited by PECVD and it used as anti-reflection coating material [10][11]. Finally, Aluminum oxide (Al2O3) is applied to provide good passivation property deposited by atomic layer deposition (ALD) [12].

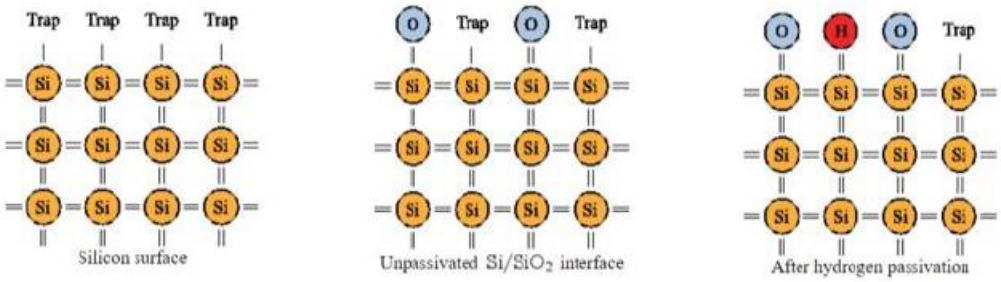

Figure 1.5: Chemical passivation of the silico surface using SiO_2 and hydrogen atoms [5].

Field-effect passivation

Another method to reduce the surface recombination is to reduce one type of carrier concentration by introducing a highly doped layer, which is known as field-effect passivation. The electric field repels the minority carrier from the highly doped region. Figure 1.6 demonstrate this technique of an n-type c-Si solar cell, in which the emitter is a highly boron-doped region, it rejects electrons and only accept holes to pass through. In this way, the surface recombination reduced significantly. However, a too high doping level will cause a poor passivation quality and the Auger passivation becomes dominant [13].

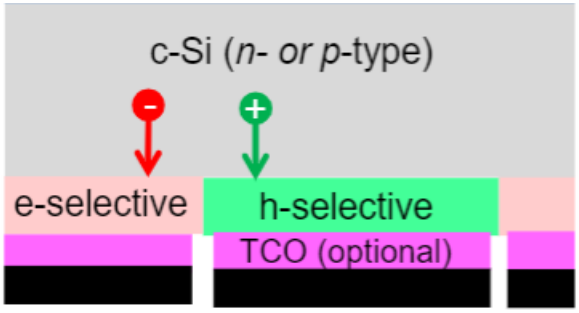

Figure 1.6: Selective passivation layers of the hole and the electron on the solar cell rear side [12].

1.5 Carrier selective passivation contacts definition and techniques

As mentioned before, the implantation of carrier selective passivating contact (CSPC) brings a major improvement in solar cell design. An explanation of definition with some important examples is given in this section.

Thanks to the constant improvement in c-Si resulted in a substantial reduction of recombination losses at both bulk and surface level [11]. However, recombination at the metal/semiconductor interface is currently the controlling factor for to have high efficiency solar cells. Therefore, CSPC used to overcome this limitation factor. To present a better understanding of CSPC, two main parameters should be considered to achieve high solar cell quality which are the recombination current density, J_0, (non-collected charge carriers) and contact resistivity, ρc, (collected charge carriers). These values have to be minimized to realize a highly selective contacts [14]. An ideal CSPC enables the following:

Firstly, implementing a passivating layer between the metal/c-Si interface. This facilitate an efficient interface passivation (minimize the defect density) and surface passivation. The high passivation quality result in lowering the J_0 which enable higher Voc values. Next, a good field effect passivation by introducing a doped p^+ or n^+ layer. The excellent charge carrier selectivity enables the conductivity for majority charge carrier type (elections/holes) must be higher. In other words, it passes one type of charge carrier and block the other [15]. This good selectivity reduces the contact resistivity ρc significantly. The carrier selectivity can be achieved by many ways and the major forms of the passivation techniques are tunnel oxide passivation contact (TOPCon), silicon-heterojunction (SHJ), and doped poly-Si interdigitated back contacted (IBC) cell and explained in detail in this section.

Tunnel oxide passivating contact solar cells

The TOPCon technology is a selective contact structure can be formed by an ultrathin tunnel oxide layer (typically <1.5nm) together with doped poly-Si layer [24]. The basic working principle of this passivating contact structure is based on two aspects: First, the ultrathin oxide which is typically grown by thermal or chemical oxidation, provides chemical passivation at the oxide/c-Si interface. It allows charge transfer from c-Si to poly-Si, while it repels the dopant movement from poly-Si to c-Si [24], figure 1.7 right. Next, the doping in the poly-Si layer increase the transmission possibility for electrons (in this case) while reducing the conductivity of the other charge carrier type (holes) [17]. Figure. 1.7 left is an example of TOPCon where the back-surface field (BSF) at the solar cell rear side replaced with tunnel oxide passivated contacts.

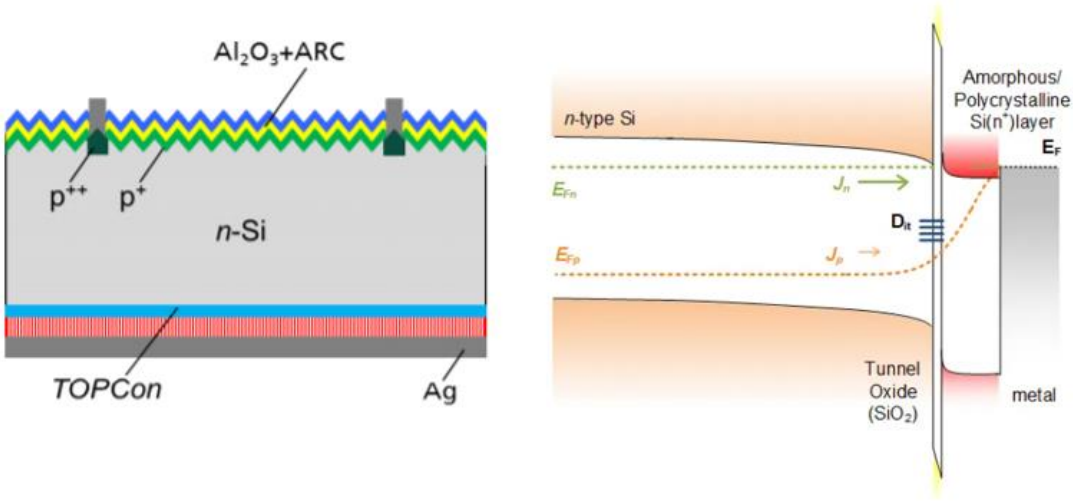

Figure 1.7: left: TOPCon cell structure with tunnel oxide at the rear side. Right: Band bending diagram at the tunnel oxide layer [19].

This technology is considered relatively thermally stable; however, the main advantage of this specific topology is the simple manufacture steps. This is realized by the fact that the metal on the rear side can be performed in on step rather than the complex pattering techniques for the back contact. The maximum achieved efficiency is 25.7[%] using this design [20]. On the other hand, this technique has some drawbacks because the doped poly-Si on the front side results in large parasitic absorption and on the rear side the heavily doped poly-Si, needed to obtain good carrier selectivity, increases the free-carrier absorption (FCA) [21].

Silicon heterojunction solar cell

The silicon heterojunction (SHJ) was fabricated in the early 1990s and has been trademarked under the name of HIT (heterojunction with intrinsic thin layer). When two material are connected to each other it is called heterojunction. Applying this concept, Kaneka Corp. has reached SHJ cells with an outstanding conversion efficiency of 26.7 % [22]. The diagram of this cell is presented in figure.1.8 left.
The silicon heterojunction working mechanism is based on two passivation approaches mentioned in previously. Firstly, it comprises a thin intrinsic hydrogenated amorphous silicon a-Si: H layer on the silicon surface to provide high surface passivation (chemical passivation) [23]. Secondly, the doped a-Si:H layers (p/n type) are applied on top of it to enhance charge carrier selectivity by introducing band bending in the c-Si [see Fig. 1.8 right]. Additionally, the heavy doping layer increase the conduction of electrons and holes, which is further aided by the fact that a-Si:H has a wider bandgap than c-Si [24]. Finally, between the metal and a-Si layers, transparent conductive oxide (TCO) layers are introduced to promote the lateral conductivity, giving the fact that a-Si has a poor conductivity. Moreover, TCO acts as an antireflection coating which results in enhanced optical performance [5].

Utilizing these advances, leads to the fact that SHJ cells have very high Voc, which can reach a value of 750 mV [25]. Furthermore, one of the main advantages of SHJ cell is because it has a low thermal budget as a-Si doping is applied with low temperature processing. Additionally, the disadvantages are the a-Si:H layers introduce a significant optical absorption loss (parasitic absorption) and requires a TCO layer due to the poor conductivity [24].

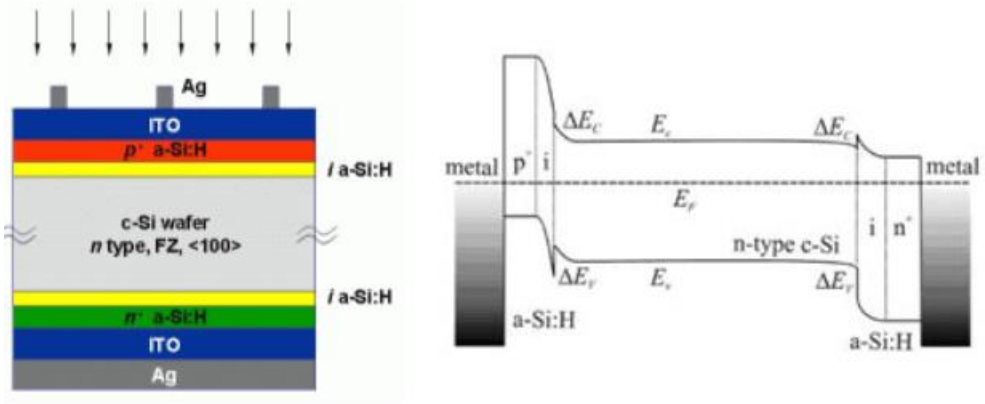

Figure 1.8: left: schematic of the SHJ cell structure. Right: SHJ cell band diagram [26]

Poly silicon interdigitated back contacted solar cells

All previously mentioned solar cells technologies have both front and rear metal contacts, thus metal contacts at the front side induces optical losses caused by the shading effect, the interdigitated back contact (IBC) solar cells is developed to overcome the shading effect by moving all metal contacts to the solar cell rear side [59]. It is a successful structure with growing importance for high performance devices to be obtained. The world record holder efficiency is 26.1% for IBC cells designed by ISFH using this structure [27].

As shown previously in Figure 1.7 right which depict the band diagram of the poly-Si passivating contact. Looking to the diagram, it consists of a highly doped poly-Si layer and a SiO*x* layer. The dissimilarity of the work function between the n-Si bulk and the heavily doped n-type Si results in the band bending. This means that electrons can tunnel through oxide layer (green arrow) to the poly-Si layer, however holes will be repelled from the oxide layer. The oxide layer should be thin enough typically around 1.1 nm allowing electron tunneling [28].

Figure 1.9 left demonstrates an IBC solar cell, where all the metal contacts are on the back side. First the front side, SiN_x layer that acts as passivation and anti-reflecting coating. Next, another passivation material such as SiO_2 or a-Si is added to improve the passivation quality. The n^+ front diffusion region is called front surface field (FSF), which minimize front surface recombination through field-effect passivation. Moving to the rear side, an ultra-thin oxide layer is deposited on the Si bulk material. Below the oxide layer, the p^+ and n^+ regions are formed. Finally, another locally opened SiN_x layer to enhance the passivation with the metal electrodes.

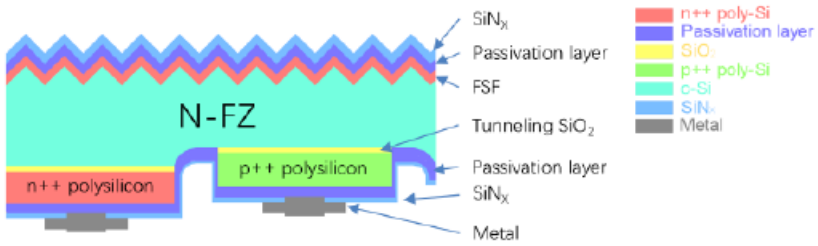

Figure 1.9: Structure of Poly-Si IBC formed by PVMD group [29].

This structure can obtain high efficiencies as it combines the best aspects of the IBC and TOPCon topologies. Utilizing this with optical changes by eliminating front metal contacts and the ability to design the rear metal leads to excellent performance. Consequently, as seen in other high-performance structures, compared with a-Si, the use of poly-Si provides greater adaptability in the design process. As poly-Si has a higher thermal budget, it can withstand more intensive steps such as high temperature annealing.

The primary downside of this structure is the complexity needed for manufacturing process. For IBC solar cell fabrication, there are already several steps to perform. Thus, adding a tunnel oxide layer will further complicate the process. Therefore, despite the high thermal stability, it is not optimal for industry [31]. The other drawback of this topology is parasitic absorption in the highly doped layers (at both front and rear) mostly due to FCA in these layers. Parasitic absorption can be decreased by using other doping methods for example in situ doping or reducing the doped layer thickness [31]. This thesis focuses mainly on this side to minimize these losses by varying the thickness of the doped layer in terms by using plasma enhanced chemical vapor deposition (PECVD) rather than ion implanting.

1.6 Thesis objectives

The purpose of this thesis project is for the preparation of proof of concept (PoC) bifacial IBC solar cells through the implantation of poly-SiOx passivating contacts, to produce a highly efficient, high energy yield c-Si solar cell. Many experiments must be carried out to successfully produce the solar cell. The main objectives are (1) to study the most suitable approaches to pattern the poly-SiOx fingers, which could deliver/maintain the highest passivation qualities of the passivating contacts; (2) applying the ultimate patterning approach to the solar cell process flowchart to fabricate the proof of concept cell. Different manufacturing parameters must also be tested in order to achieve acceptable results namely annealing time, annealing temperature and other checks for material etching methods. In addition, the effect of hydrogenation mechanism was also checked, which has crucial importance on the cell parameters. Bifacial-IBC solar cells with poly-SiOx passivating contacts have been developed by seeking a compromise between several decision variables of the production process. The main research objectives of this thesis are:

- Compare masked ion-implantation and wet-etching approaches for patterning of BSF and emitter fingers.
- Optimize the passivation of the patterned BSF and emitter fingers at the solar cell rear side.
- Investigating best Bifacial-IBC solar cells flow chart.
- The optimal patterning approach for ITO fingers.

1.7 Thesis outline

This work consists of 5 chapters. The fabrication and measurement techniques used in this thesis are described in Chapter 2. In chapter 3, the ion-implantation of poly-SiO_X as patterning step of proposed flow chart is tested and evaluated. The passivation tests for fabrication of the bifacial-IBC solar cell using wet etching of in-situ doped poly-SiO_X as patterning approach is introduced and evaluated in chapter 4. Also, in this chapter, the results of PoC bifacial IBC solar cell and the losses analysis are discussed. Finally, in chapter 5, the thesis concludes with a discussion of the findings and recommendations for further studies.

2 Experimental methods

This chapter is separated into two major sections: Firstly, the fabrication processes to manufacture the test samples and solar cell are introduced. Next, it explains how the measurements are conducted with the aid of characterization equipment.

2.1 Fabrication process

The various manufacturing processes involved in the processing of bifacial-IBC solar cells are presented in this section. Starting from wafer cleaning step and finishing up with metallization step. These processes are not only applied to manufacture bifacial-IBC solar cells, but also for symmetrical samples which are crucial to analyze the carrier selectivity and passivation quality.

Wafer qualification

In this project, phosphorous (n-type) doped crystalline silicon (c-Si) wafers manufactured by TOP-SIL are used. The wafer material properties are presented in table 2.1. The reason behind the choice on n-type wafer is motivated by two crucial properties. First, n-type have higher bulk minority carrier lifetime because it has lower sensitivity to recombination. Second, p-type material suffers from oxygen impurities due to wafer fabrication, therefore n-type are more used to avoid the boron-oxygen related light-induced [32].

Table 2.1 c-Si material properties.

Parameter	Value
Diameter [mm]	100 +/-2
Thickness [μm]	$260 \simeq 300$
Doping	n-type
Finish	Polished
Resistivity [ohm.cm]	1-5
Orientation	<100>

Standard cleaning

Before starting any process, silicon wafers must first be properly cleaned to remove any organic or inorganic contaminants. The standard cleaning technique, used in Else Kooi Laboratory (EKL), consists of 5 main steps. First, to eliminate the organic contamination of the wafers it is immersed for 10 minutes in

a 99% HNO3 solution. After that, the wafers are rinsed for 5 minutes in deionized water (DI water). Next, Inorganic contamination is removed at 110 °C in a 68 % HNO3 solution for 10 minutes, also followed by a 5 minutes rinse in a DI water solution for 10 minutes. The final step is to dry the wafers in a Spin Rinse Dryer (SRD).

It is important to mention that, a native oxide layer is created at the surface of the wafer after different process such as standard cleaning although the wafer is kept in the cleanroom atmosphere. Therefore, this native oxide should be removed right before the next step this is done by immersing wafers in hydrofluoric acid (HF) 0.55% solution for 4 minutes until the entire surface become hydrophobic. Next, the wafer is rinsed with DI water for 4 minutes, with additional 1 minute of isopropyl alcohol (IPA) to dry the wafer.

Chemical silicon oxide growth

The growth of a thin silicon layer SiO_x layer is the next step of the manufacturing process. The goal of this step is to establish the best passivation ultra-thin SiO_x layer thickness typically 1.5 [nm] [33]. In this thesis work, the so-called Nitric Acid Oxidation of Silicon (NAOS) via the chemical oxidation method is used to develop this layer. Thus, the wafer is immersed for 60 minutes in a 69.5% HNO3 solution at room temperature to achieve this ultra-thin oxide layer. As mention previously, this step is carried out directly after removing the native oxide layer by Marangoni (0.55% HF). Finally, wafers should wash out in DI water for 5 minutes after NAOS oxidation.

The major benefit of chemically generated oxide is that it creates a homogenous layer thickness, thus it has a very low leakage current. Additionally, NAOS is easy to apply, and it is a very low thermal budget process compared with thermal oxidation which required a temperature 600 to 700°C [34]. However, the only downside of this method is that it is less thermally stable in comparation with other oxidation methods. Therefore, the oxide layer may not withstand the followed high temperature process [35].

Low Pressure chemical Vapor Deposition (LPCVD)

Low Pressure chemical Vapor Deposition (LPCVD) is one of many deposition methods used to deposit Si based layers (figure 2.2). This method allows layers with a thickness between a few nanometers and a few micrometers to be deposited.

The key advantage of this method is the high homogeneity and purity of the layers deposited by LPCVD, which is essential for the conducted experiments. Further, LPCVD deposited layer are pin-hole-free [36]. This ensures the safety of the ultra-thin oxide layer in the subsequent deposition and chemical steps.

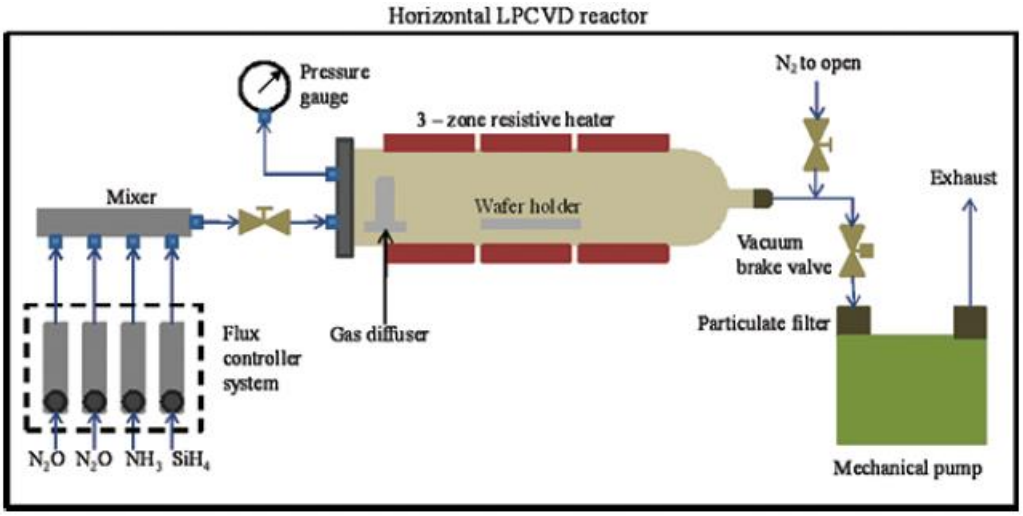

Figure 2.2: Schematic of LPCVD system [37]

The LPCVD tube furnace developed by TEMPRESS SYSTEMS is used during the described thesis project. This system applied in order to deposit an intrinsic amorphous silicon layers [(i)a-Si] on both the symmetrical and bifacial-IBC cells. The (i)a-Si layer was deposited using an optimized recipe with the following parameters: Silane (SiH_4) is the used gas with a constant flow rate at 45 sccm during the deposition. The temperature and pressure in the system in kept at 580°C, 20 Pa, respectively. Using these parameters, the a-Si deposition rate occurs on both side of the wafer was 2.2 nm/min. The furnace implements a post annealing at 600°C for 60 minutes. After the deposition step to remove stress from the sheet. This layer will be annealed later to formulate doped poly-Si layer at rear side of the solar cell. It should be noted that the sample must be dipped in 0.55% solution directly before performing the next process. This is done to remove the easily formed native oxide layer on the amorphous silicon surface.

Plasma enhanced chemical vapor deposition (PECVD)

Next deposition method used in this project is plasma enhanced chemical vapor deposition (PECVD). It is used in the deposition of a large variety of materials in solar cell research. This machine runs only at low temperature typically between 200-400. This is due the presence of plasma that deliver ions and energetic free electrons that capable of breaking the gases' chemical bonds [38]. By applying a highly energetic field on each side of the chamber across the electrodes, plasma is ignited. The PECVD layers can be formed with high levels of uniformity, quality and at desirable thicknesses [39]. Figure 2.3 illustrates the PECVD machine.

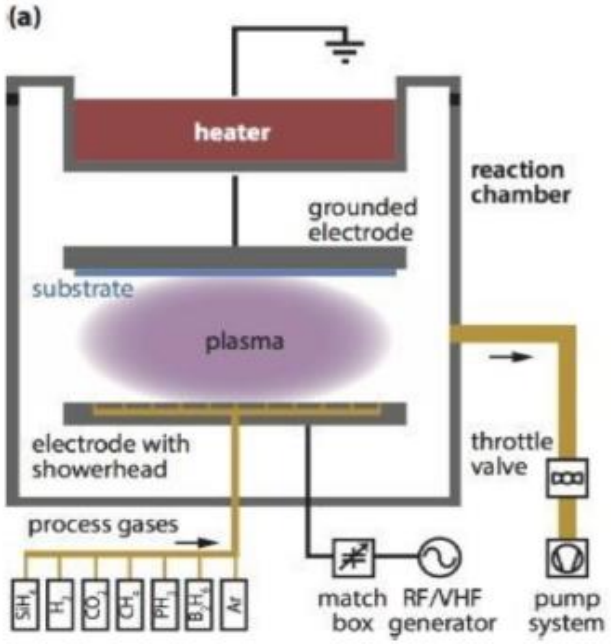

Figure 2.3: PECVD chamber configuration [40].

In this thesis project three different PECVD machines are used. First, Novellus was used to deposit a thick SiN_x in the form of capping layer on the bifacial-IBC solar cell rear side. The function of this layer is to protect the doped region (p/n type) on the rear side during the front side texturing. The next PECVD is Plasmalap system 100 manufactured by Oxford instruments. This instrument is used first for hydrogenation step on the rear side to deposit SiNx at 400°C with 12 [nm/min] as deposition rate. Next, it is also used to form the front side passivation layers mainly a-Si at 250°C with deposition rate 45[nm/min] and again SiNx as ARC layer.

Finally, AMOR manufactured by Elettrorava is the last PECVD tool used in this project in order to deposit intrinsic, p doped and n-doped materials. The deposition using this device is done in four different chambers dedicated to particular material to avoid contamination of the deposited layers. To process the wafer both sides without breaking the vacuum an additional chamber is added. The descriptions of the deposited layers with deposition parameters are given in table 2.2.

Table 2.2 Deposited layers using PECVD.

Layer	Gas	Gas flow rate[sccm]	Pressure[mbar]	Temperature[°C]
Intrinsic	SiH_4	45	1-2	180
p	SiH_4	110	1	180
	CO_2			
	B2H6	115		
n	SiH_4	39	2	180
	CO_2			
	PH_3	43.8		

Ion implantation

In solar cell processing, Varian ion implanter is used to form n^+ and p^+ doped poly-Si layers using Phosphorous and Boron dopants, respectively. Figure 2.4 demonstrates the schematic of such an implanter. Using plasma, the dopant ions are formed and guided with the aid of a magnetic field into the accelerator. In order to filter the desired ions before entering the accelerator, a mass separation slot is used. Next, the ion beams are concentrated, with the help of magnetic lenses, on the target surface.

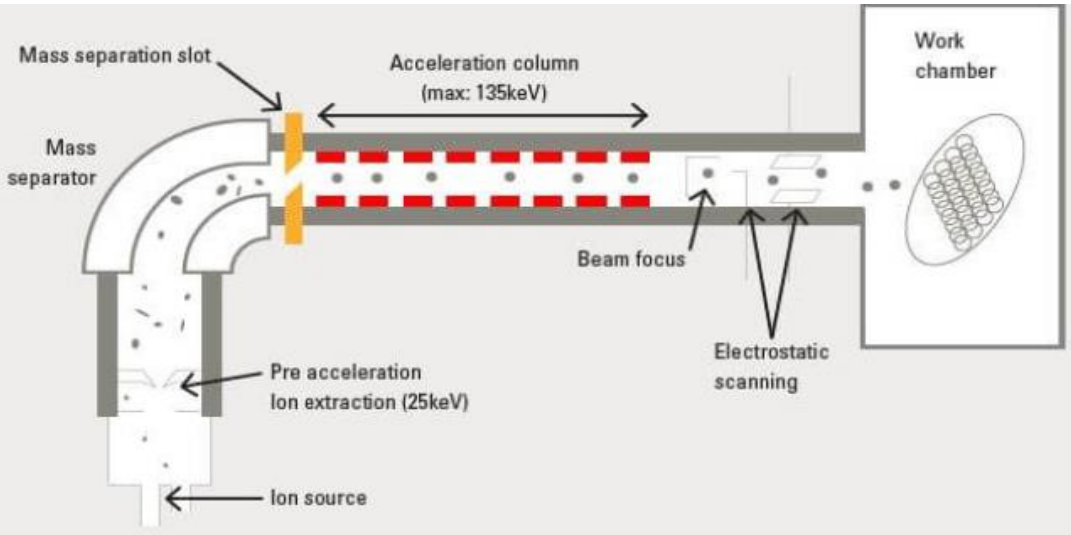

Figure 2.4: Schematic of ion implantation system [41].

One of key advantages of ion implantation that there is a large amount of control on the degree to which the ions would penetrate inside the substrate. This is done by varying the implantation energy, dopant species and ion dosage. However, this method may cause damage the target surface. The used ion dosage and energy for the formed FSF, BSF and emitter regions used in this thesis project are outlined in table 2.3.

Table 2.3: Ion implantation parameters

Region	Ion dopants	Energy [keV]	Dose [ions-cm^{-2}]
FSF	P	10	1e14
BSF	P	20	5e15
Emitter	B	20	6e15

Photolithography

Photolithography is the most common used method to perform complex pattering of the p and n type contacts on the silicon wafer same surface. The key advantage of this technology its low typical feature size < 1 micrometer compared to other technologies; thus, it can be used for the most precise classification of structure. However, the downside of photolithography is the high equipment and process cost [42]. The brief explanation of photolithography process is as follow:

First, a photoresist layer is formed on the clean solar cell surface. The photoresist (PR) is an organic polymer substrate sensitive to ultraviolet radiation [43]. It has two different types positive photoresist and negative photoresist. The coating is done using EVG 120 tool from EV Group and the thickness of the PR layer depends on the chosen PR viscosity, the spin rotating speed and time. After the PR has been uniformly spread on the substrate, the wafer is pre-baked properly in the same machine. Next the exposure stage where the photoresist is subjected to intense light through chromic patterned mask. The light source illuminates the coated wafers with an ultraviolet (UV) light. The light exposure of the PR induces a chemical sift that ultimately enables the PR to be extracted. Exposure is applied with EVG 420 contact aligner manufactured by EV Group. The final step is development which is done again using EVG 120 tool from EV Group. In this process, the exposed/non-exposed areas differ chemically as one of the areas stay or dissolve during the development. The exposed region, in the case of a positive PR, is dissolved. However, this is not the case when negative PR is used where the exposed area remains. Figure 2.5 depicts the photolithography steps.

Photolithography process is applied a lot during this thesis work to process the solar cell. First, three photolithography steps are used to form the emitter and back surface field (BSF) regions on the rear side of the bifacial-IBC solar cell using PN mask. Next, it is also used to pattern the ITO layer using wide opening mask. Finally, two steps are applied to form the metal fingers on top of the TCO layer using narrow metal mask.

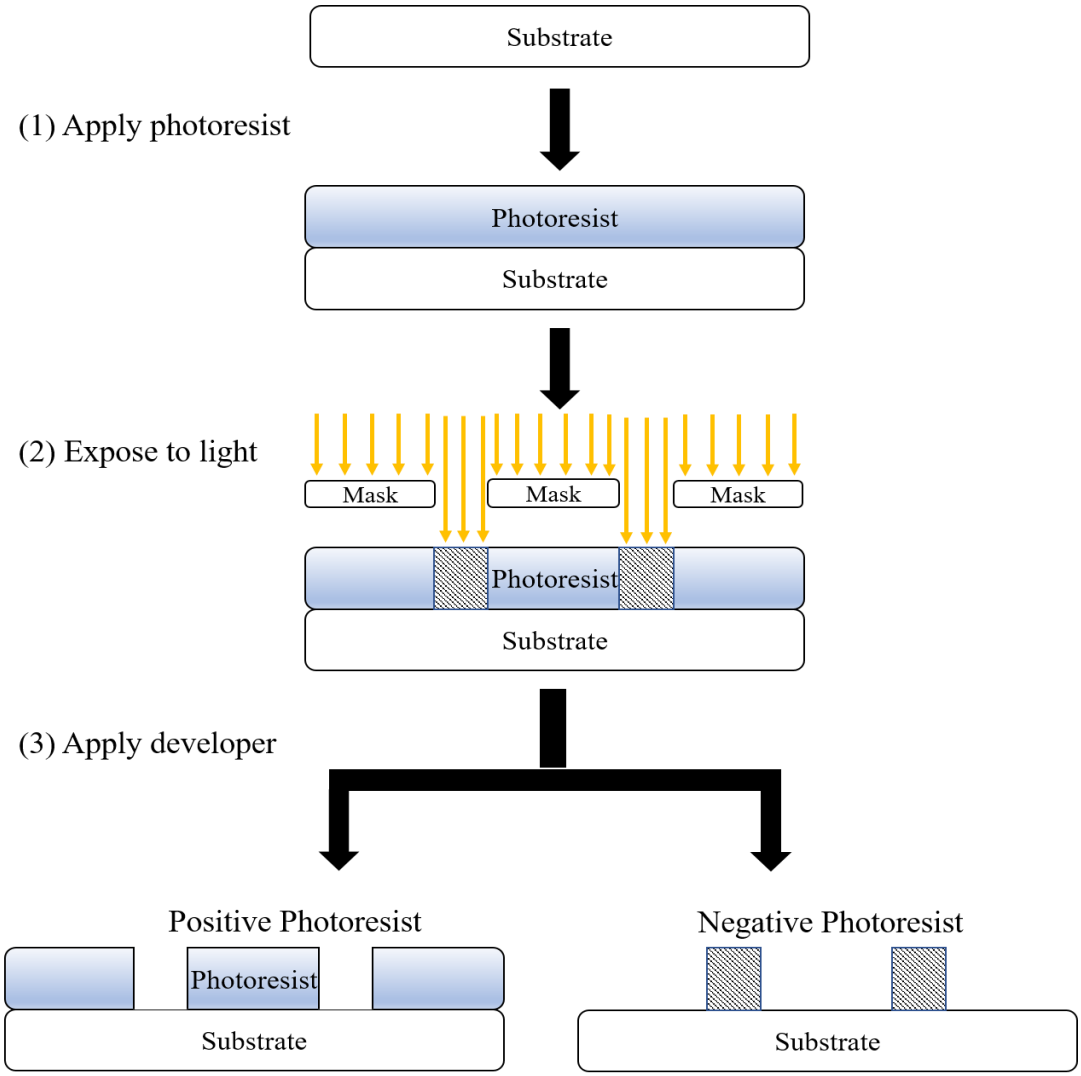

Figure 2.5: Photolithography steps [44].

High temperature annealing

After the deposition of the highly doped amorphous oxide layer, high temperature annealing is applied. There are several goals for this annealing step in order to activate the dopants and transform the a-Si layer into poly-Si layer [45]. Also, the diffusion of the dopants can also be enhanced through high temperature annealing. In other words, the deposited dopants will be activated and transferred. However, some of the dopants can be diffused into the bulk material which minimize the passivation quality. Additionally, the structure of the tunnel oxide layer will also be influenced by this step, Inducing pinhole formation at long annealing time and most possibly the layer breakdown. Samples are placed inside a Tempress furnace and annealing is performed on various time periods at high temperature between 850-950°C with pure N2 atmosphere to fabricate the bifacial-IBC solar cells.

Hydrogenation

One of the passivation methods used in this thesis is hydrogenation. It is one of the chemical passivation methods as it saturates, with the help of hydrogen atoms, the surface silicon atom dangling bonds. Two steps are involved in hydrogenation: the hydrogen rich capping layer (SiN_x) deposition, which is followed by forming gas annealing (FGA).

The SiN_x layer was deposited using PECVD method using the Oxford supplied instrument Plasmalab80plus. It is important to note that for this process ammonia (NH_3) and Silane (SiH_4) gasses are used, and it is performed under optimized conditions: a pressure of 87 [Pa] at 400°C as temperature.

The forming gas annealing is carried out to release H atoms embedded in the hydrogen rich SiN_x layer and to deliver additional hydrogen needed to passivate defects at the SiO_2/poly-SiO_X interface [46]. In this thesis, the furnace developed by TEMPRESS SYSTEMS is the machine used for FGA. It was carried out for 30 minutes at a temperature of 400°C in the mixture of H_2 and N_2 atmosphere.

Texturing

Texturing is used in solar cells to maximize light absorption. This is accomplished by etching the cell surface by an alkaline solution. Two orientations can be represented in the c-Si lattice: <100> and <111>. The <100> crystal lattice orientation has an etching rate 50 times higher than that for the <111> orientation when it is exposed to this solution [47]. This is done until the lattice structure becomes <111> which means that the flat surface of the cell changes into a sequence of random pyramids [48]. The textured surface is shown in figure 2.6.

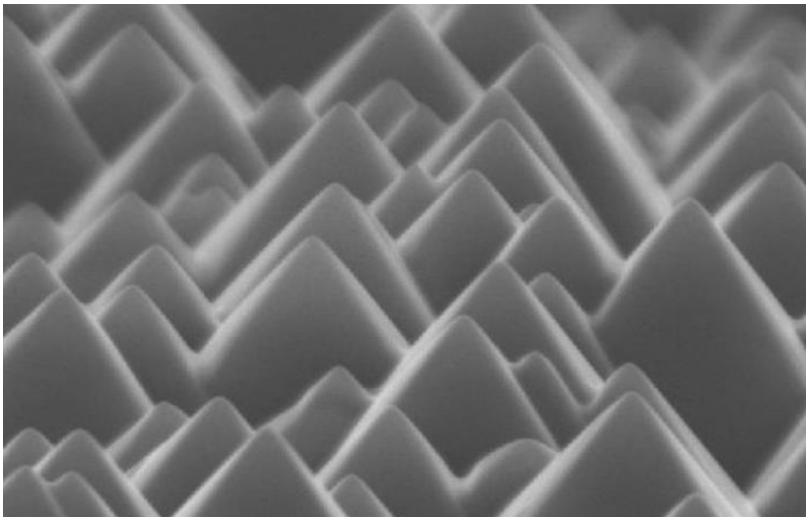

Figure 2.6: c-Si textured surface [49].

In this thesis, texturing is performed on the solar cell front surface to minimize the reflection losses. The used alkaline solution is held at high temperature 80°C prepared using a 4:1 ratio mixture of water and tetramethylammonium hydroxide (TMAH) with an additional 120 ml solution of ALKA-TEX.

Transparent conductive oxide (TCO) layer

The Transparent conductive oxide (TCO) layer is used in this thesis project for two main reasons: First, doped poly-SiOx layers are used as rear contacts in the bifacial-IBC solar cell. Compared to poly-Si, the poly-SiOx has relatively low conductivity. In other words, TCO layer serves as an electrical contact for solar cell operation as the transport of charge carriers may be inefficient at the poly-SiOx/metal interface. Second, for better light It may also function in the cell as an anti-reflection coating (ARC) film. Thus, to maximize the solar cell performance in the active wavelength range, this layer should be highly transparent by optimizing the refractive index and highly conductive by increasing the charge carrier's mobility [81].

Typical TCO layers are formed from fluor-doped tin oxide (SnO_2: F), aluminum-doped zinc oxide (ZnO:Al), boron-doped zinc oxide (ZnO:B), hydrogen-doped (hydrogenated) indium oxide (In_2O_3:H) [50]. For this thesis, the Indium Thin Oxide optimized with PVMD group was chosen, which is a mixture of about 90% indium oxide (In_2O_3) and 10% tin oxide (SnO_2). It is chosen because it provides the trade-off between transparency and conductivity [51]. It can be applied using physical vapor deposition, namely sputtering method which results in a layer with high mobility as well as a proper work function without causing serious damage for both the semiconductor and metal contact [5]. The deposition of the ITO layer was performed with patterned structure at the rear side of the bifacial-IBC solar cell with a target thickness around 80 nm. This thickness maintains appropriate light trapping and charge carrier's transport.

Metallization

Metallization is the last step in the solar cell fabrication. This process plays a vital role is the solar cell output optimization. First, optically by the means of metal gridlines, as the gridlines width increases it introduces more shading effect which ultimately affects the short circuit current. Second electrically, the metal fingers on the surface add more series resistance to the solar cells, which influences the fill factor [52]. For this project, the first used metal deposition method is the metal evaporation. It used to deposit both silver and aluminum or the solar cell rear side. Figure 2.7 shows a schematic drawing of the process. Typically, in this process either resistive evaporation or electron beams are applied to warm the metal ingots above the material melting point. The substance that has been evaporated would uniformly fill the deposition chamber, which subsequently cover the target surface. The metal evaporation is executed at high vacuum 10^5, which means that the material oxidation and deposition thickness is well controlled [53]. After deposition, the target cools down and the metal condense back into a solid.

The used machine in this project is Provac evaporation machine at PVMD group. It worth to mention that to pattern the metal on the bifacial IBC solar cell rear side, a thick a uniform three photoresist layers is first applied to cover the wafer surface. This is done to accomplish a well patterned and thick metal layer. Next, a full area metal deposition is performed and the undesirable metal region on the solar cell surface is extracted by a metal lift-off step using acetone or by etching the metal seed layers after performing cupper plating process.

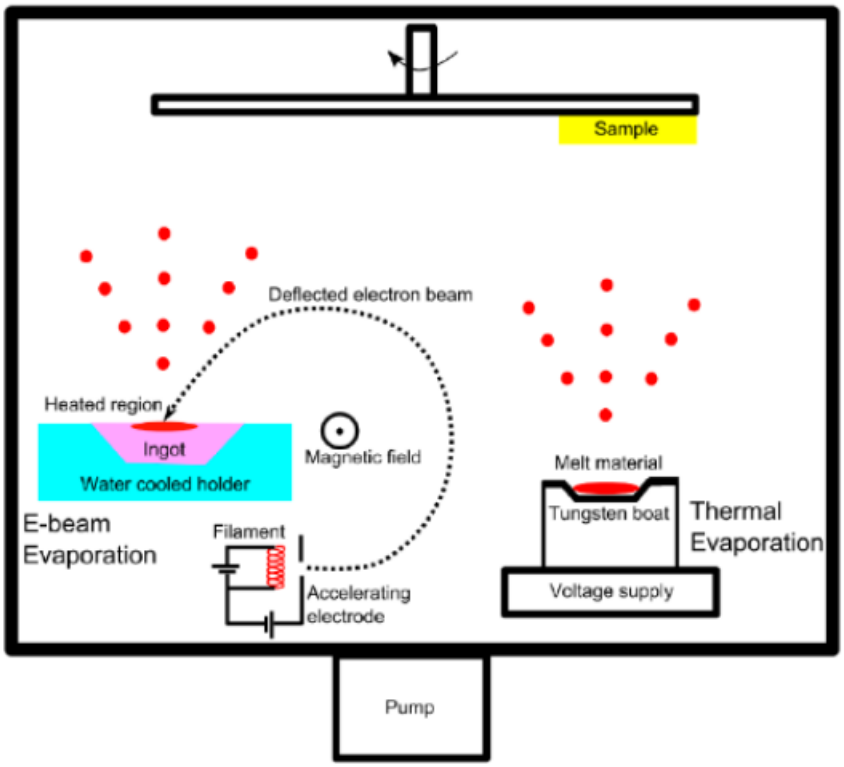

Figure 2.7: Schematic of metal evaporation process [53].

Cu electroplating

Cu electroplating is an electrochemical (redox) reaction. This reaction requires the presence of two electrodes anode and cathode and electrolyte solution. The basic working principle is done as follow the wafer is placed at the cathode and the cupper source material at the cathode with $CuSO_4$ as an electrolyte solution. When the reaction takes place, the cupper at the cathode is dissolved in the solution and transported to the anode in our case is the solar cell. A schematic overview of copper plating process is shown in figure 2.8.

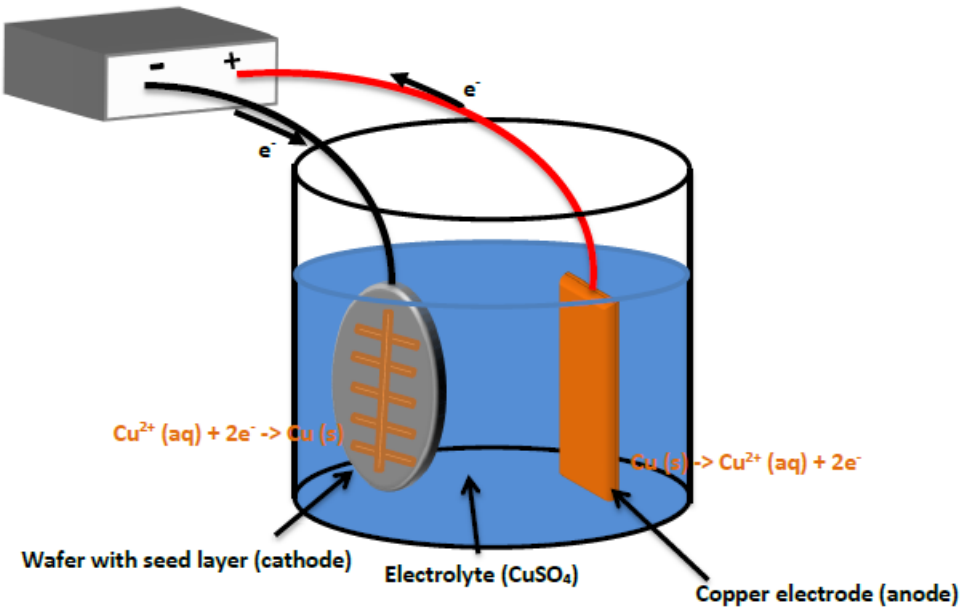

Figure 2.8: schematic of Cu plating.

The used machine during this thesis is an inhouse built-in machine in the MEMS lab. The wafer is placed horizontally on the holder and fixed with four clamps at the wafer edge. Next, the wafer holder is immersed in the plating bath at 28°C and the anode (copper plate) is fixed above facing the wafer holder. Bothe the copper plate and the wafer holder is connected to a power booster (10A) where the copper plate is connected to the negative side and the wafer holder to positive resulting in a negative current which is important to perform the reaction. During this process, the current is kept constant however the voltage is cannot be controlled, and it keeps changing during the process.

It is worth to mention that this process is very critical because copper diffusion to the silicon layer occurs at high speed levels leading to a serious impurities which will act as a recombination centers leading eventually to lower the carriers lifetime and the overall cell performance. Therefore, the silicon layer should be protected against the copper diffusion. This is done by adding a metal seed layer which acts as a barrier for the copper and as s a seed layer for the used current during the process. For our process, an added two metal seed layer a 200 nm aluminum and a 200 nm silver which will be etched away after performing the cupper plating process.

2.2 Characterization techniques

The characterization method and techniques used to assess the material quality for the optimization of the manufacturing process and the performance of the devices are described in this section. It is performed on different sample types: the symmetrical samples used to test the passivation quality and the full fabricated solar cells.

Photo-conductance lifetime measurement

The passivation quality of a silicon wafer can be specified through the effective lifetime (eff) of the minority charge carriers. The lifetime of the minority carrier is determined by the average time that the excess minority carrier need before it recombines. The effective lifetime of the carrier largely depends on the recombination process on both the wafer bulk and surface. Having the carrier density and lifetime, the recombination current density (J_0) also can be calculated [55].

For the detection of the minority carrier lifetime (eff) and implied voltage (iV_{oc}), the Sinton WCT-120 lifetime tester (Figure 2.98) was used. This unit is fitted with a filtered xenon flash lamp that provides a red range red color light. In the wafer bulk, the light flash requires the production of excess charge carriers which it will subsequently recombine until the balance is achieved. Next, the eddy-current conductance sensor is another unit that is used in the Sinton WCT-120. It tests the intensity of the light given by the lamb described above and the photoconductance of the wafer.

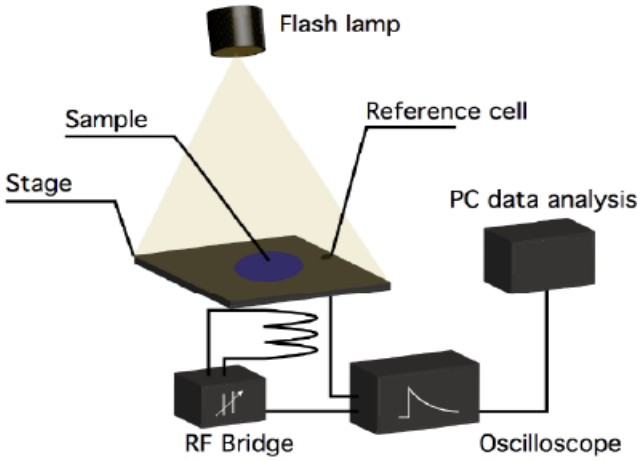

Figure 2.9: Measurement setup of photoconductance lifetime tester [55].

Ellipsometry

Ellipsometry is primarily used to measure the thickness of the examined layer and its optical constant. The measurements of the layers thickness should be accurate, because it plays a vital role in the solar cell designing. Ellipsometry tests the difference in incident light polarization relative to the light detector of the reflected light from the sample. Figure 2.10 shows the ellipsometry setup.

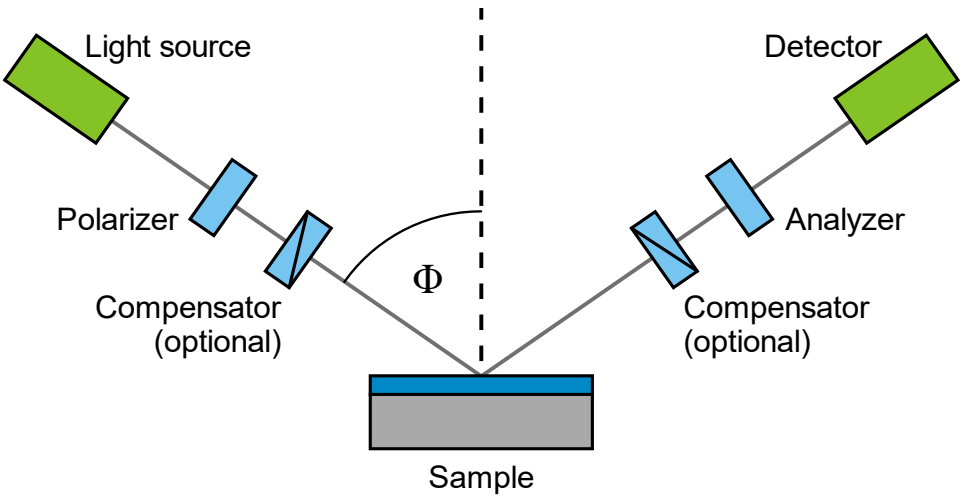

Figure 2.10: Ellipsometry setup [56].

The EC-400 manufactured by J.A Woolam Co. is the tool used in this project. Measurements were predominantly carried out on layers deposited on a wafer substrate. This allowed the thickness of the deposited layers to be found and further optimized for the best possible cell outcomes.

Current-Voltage measurements

Current and voltage characterization are the most significant parameters to describe the bifacial-IBC solar cells. Current-voltage measurements can be used to obtain these parameters. The typical test conditions are simulated with a AAA class Wacom WXS-156SL2 solar simulator [57] with the following setup: First a Halogen and a Xenon lamp are combined to correctly simulate the illumination of one sun using AM 1.5 spectrum and irradiance equal to 1000 W/m^2. Next, a temperature controller is mounted on the test stage where the solar cells are positioned to ensure that the temperature of the solar cell is kept constant at 25°C. Figure 2.11 shows the current-voltage measurements setup.

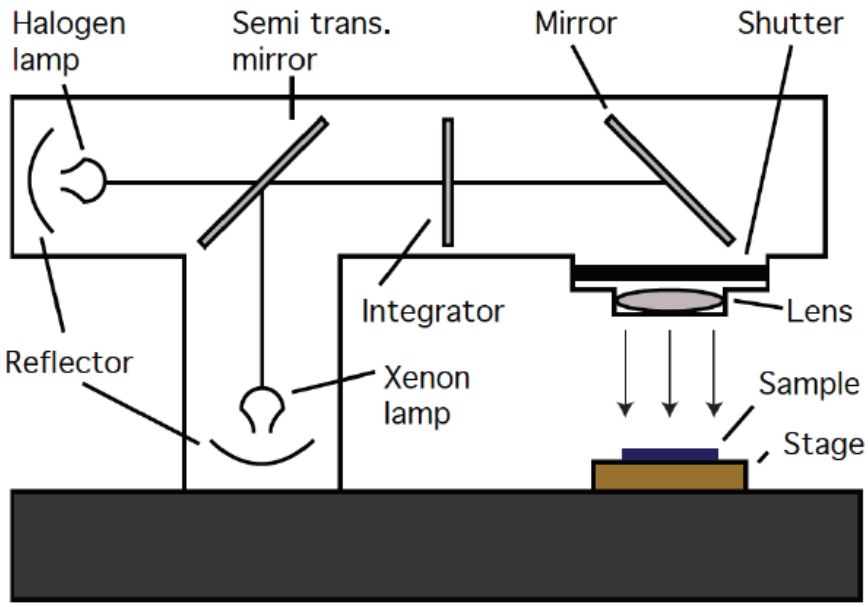

Figure 2.11: Current-voltage measurements setup [57].

Profile analyzing Laser Microscope

The profile analyzing laser microscope can be used to measure the film thickness and roughness in addition to the ability to take an optical image of the material surface with nanometer resolution. This microscope is even able to measure any object with bumpy surface. The basic working principle of this microscope is by incorporating the laser light with a white light and observing the reflected laser light from the material surface [58].

During this thesis, the used microscope was VK-X250K manufactured by KEYENCE. It is used to take an optical image of the tested samples to compare the blistering effect. This is performed by simply placing the sample test on the device stage and it will automatically scan the sample. Figure 2.12 shows an image of the used microscope.

Figure 2.12: Profile analyzing laser microscope device [60]

3 Ion-implantation for bifacial-IBC solar cell

The aim of this chapter is to test the feasibility of the ion-implantation as doping and patterning approach for the fabrication of bifacial IBC solar cells. Therefore, the optimization of ion-implanted poly-SiO_X carrier selective passivation was conducted. In section 3.1, it is aimed to discuss the crucial requirements for optimizing the passivation quality. The proposed process for bifacial-IBC solar cell and the necessary passivation tests were discussed in the section 3.2. Next in section 3.3, the thickness of the intrinsic a-SiO_x:H layer deposited by PECVD at different annealing conditions is optimized. This is done to have a sufficiently crystallized structure and a desirable doping profile. Finally, the essential hydrogenation process is also examined to minimize defects, dangling bonds, at the interface between the c-Si bulk surface and poly-SiO_x layer.

3.1 Requirements for poly-SiO_X passivation contact

As mentioned in chapter 2, the tunnel oxide carrier selective passivation contact for poly-SiO_x required the presence of an ultra-thin SiO_x layer formed on a doped poly-SiO_X layer. This section discusses the requirements and factors needed to optimize the carrier selectivity of the **ion-implanted** poly-SiO_x CSPCs which can be summarized as follow:

Silicon oxide layer

Tunnel oxide layer provides the chemical passivation of the c-Si surface by bonding with the Si dangling bonds. It should be thin enough to facilitate the charge carrier tunneling through it to the doped poly-SiO_x layer. To obtain a better passivation quality of the CSPC, the integrity and the thickness of the formed tunnel oxide layer should be optimized.

First, the integrity of the tunnel oxide layer is crucial to provide the high passivation and it should be strong enough to stand the following high temperature processes. For example, the chemical oxidation NAOS used during in our thesis has low thermal stability which means the high temperature process may damage the tunneling oxide layer and might generate a local pin hole. These pin holes' increased with increasing the annealing thermal budget. Increasing the pin holes density reduces the contact resistivity and thus enhancing the charge carrier collection, however this brings an increasing in the recombination current density. Therefore, this layer must be optimized to provide an excellent passivation.

Second, the thickness of the tunneling oxide layer should be optimized to obtain the sufficient thickness required for the charge carrier tunneling to the doped poly-SiO_x layer to provide the field effect passivation. According to previous PVMD group research, the best passivation effect for both contacts

were obtained with an oxide layer thickness of ~1.4 nm prepared by keeping the wafer in 69.5% HNO_3 solution for 60 minutes [9]. Therefore, we followed the findings of the previous work in our research.

Doped poly-SiO_X layer

The doped poly-SiO_x layer plays a vital role in providing a good performance of the passivating contact by providing field effect passivation through introducing a sufficient band bending at the poly-SiO_X/SiO_2/c-Si interferences. To obtain a better optical and electrical properties, the doping concentration, and the thickness of the doped poly-SiO_X layer should be optimized.

First, the doping concentration play a vital role in the passivation quality of the doped poly-SiO_X layer. The ideal doping profile is the one which provides the field effect passivation without passing the limit where the Auger recombination in the c-Si surface becomes dominant. In addition, if the doping concentration is too high, this may reduce the field effect passivation due to the increasing doping level and depth of the in-diffusion area of the dopants in the c-Si bulk material during the following high temperature process [64]. On the other hand, if the doping concentration was too shallow in the poly-SiO_X layer the field effect passivation will be very poor, due to the non-sufficient filed effect passivation. By adjusting the implantation dose, the doping concentration of the poly-SiO_X layer can be controlled. There is a wide variety to choose the implantation dose, however, the implantation energy is limited to 5 keV by the implanter. It is worth to mention that, it is suggested that a higher impanation energy for Phosphorous implantation than that for Boron implantation can be accepted. The low energy is requited due to the smaller size of boron atoms and their high diffusivity in silicon relative to Phosphorous atoms [65].

Second, optimizing the doped poly-SiO_X layer thickness is also very important to achieve a high-quality passivation. On one hand, controlling the doped layer thickness using an optimized doping concentration and annealing conditions will results in a good electrical performance [66]. On the other hand, using a thinner layer thickness can reduce the optical losses (parasitic absorption) [67] induced by the doped layer significantly. The using of the thick poly-Si layers in the IBC solar cells is a not serious problem because both contacts are located at the solar cell rear side [31]. However, this is not an option for our bifacial-IBC solar cell because it benefits from the incident light on both the front and rear side of the solar cell.

Finally, the doped layer can be further optimized by increasing its transparency to limit the light absorption within this layer which will results in high optical performance. This can be achieved by controlling the layer oxygen content during the PECVD deposition process [68]. The absorption coefficient is shown to be decreasing with increasing the oxygen content, especially at long wavelength region, indicating that the material becomes more transparent [69].

High temperature annealing conditions

During the high temperature annealing step, three key occurrences take place. First, the dopant atoms (Phosphorous and Boron) are being activated and diffused within the poly-SiO_X layers, therefore the intrinsic buffer layer (a-SiO_X:H) becomes doped. Second, the used thermal budget crystallizes the a-SiO_X layer into poly-SiO_x. Third, some of the dopants diffused into the bulk material (in-diffused area), which is not preferred.

As mentioned previously, if most of the ion-implanted dopants are confined inside the poly-SiO_X layer, a high passivation quality can be obtained. However, this is a tricky process and required multiple tests to be optimized due to the difference in the diffusion properties of the Phosphorous and Boron atoms. In

other words, the energy required to activate and diffuse the Boron atoms is higher than the energy needed for Phosphorous atoms [70]. Additionally, the high mobility of boron atoms distribution in the silicon material relative to the Phosphorous atoms since the Boron atoms have a smaller size than Phosphorous atoms which means that Boron atoms are easily implanted much deeper into the poly-SiO_X materials [71]. Therefore, the higher thermal budget process enhances the dopants activation on the p^+ contact, however it may rise the Boron atoms diffusion into bulk material resulting in a weak field effect passivation, and enhanced Auger recombination.

Previous studies executed at PVMD group, claimed that a high passivation quality can be obtained at high temperature and short annealing time for both contacts [33]. Therefore, the annealing conditions used during this thesis project are decided to vary between 850°C and 1000°C as an annealing temperature with different annealing duration. It is worth to note that applying a hydrogenation treatment after the high temperature annealing process can further enhance the passivation quality through reducing the defect density at the c-Si/SiO_2 /poly-SiO_X interfaces.

3.2 Sample preparation

In this section, the various manufacturing process that were implemented in order to obtain a good passivation quality are explained. On various passivation structure, passivation tests are conducted on symmetrical double side flat and textured samples. The test samples are fabricated at nearly the same conditions but the examined one to have a superior comparison between the expected results. In arrange to make the fabrication process clearer, a schematic sketch of all fabrication steps and deposited layers are indicated in figure 3.1 including the symmetrical test samples (a) and the ion-implanted bifacial-IBC solar cell (b).

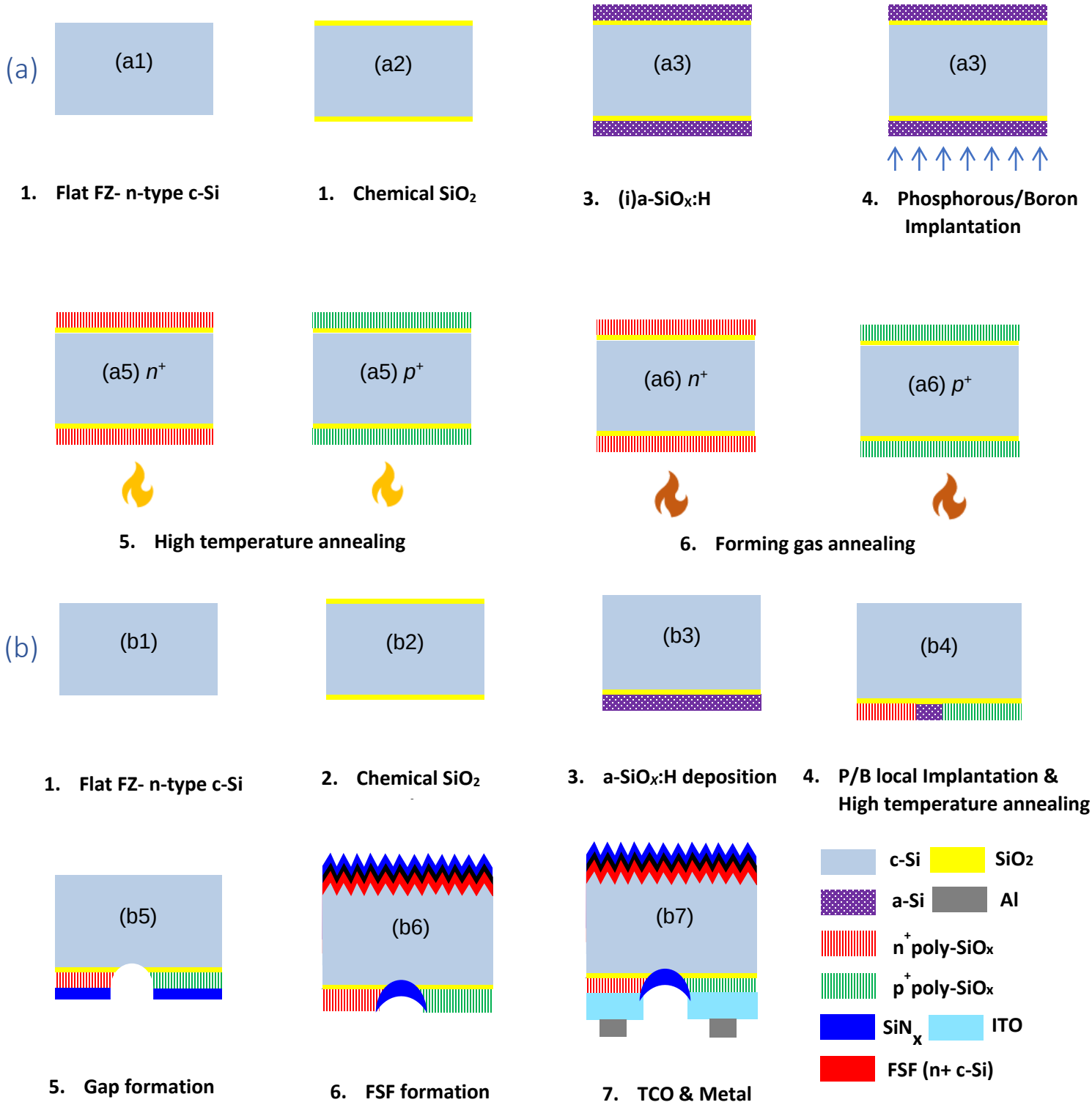

Figure 3.1: (a) process flow for symmetrical samples preparation for passivation tests. (b) proposed flow chart of the Bifacial-IBC solar cell when deploying ion-implantation as doping and patterning approach.

Figure 3.1(b) indicates the proposed bifacial-IBC solar cell flow chart using ion-implantation. First, the oxide layer is formed chemically by immersing the wafer in 69.5% solution for 1 hour. Next, the a-SiO_X:H layer is deposited via PECVD at the rear side. Then, the boron and the phosphorous regions are locally implanted into the intrinsic a-SiO_X layer by applying a lithography process. Next, an etching step is used to separate the BSF and the emitter fingers through lithography process followed by wet etching. Further, the textured front surface field on the front side formed chemically by TMAH with a lightly doped FSF implantation and SiNx as a passivation and ARC layer. Finally, on the rear side the ITO layer is formed by sputtering with the metal contact using copper plating.

The passivation properties need to be tested before the IBC cell process, in order to see the feasibility of ion-implantation for such IBC cell processes. Therefore, same processes, applied on the solar cell rear side Figure 3.1(b1-b3) , are performed at the symmetrical test sample both sides.

As mentioned previously in section 2, the fabrication process starts using an n-type double side polished Float Zone (FZ) Si wafer with <100> surface orientation and an initial thickness of 280 ± 20 µm. Below, details for only the most important manufacturing steps are mentioned. However, some required steps, like standard wafer cleaning, are not listed below to provide clarity to the examined process. Furthermore, other layers with a protective feature such as SiN_X and photolithography steps are not shown in figure 3.1, as they are etched away before conducting the measurements. The symmetrical test samples based on poly-SiO_X carrier selective passivating contacts are fabricated as follow:

1. The starting point of preparing the symmetrical test samples was using a flat polished surface, Figure 3.1(a). However, it is worth to mention that textured surface can also chemically formed on the front surface by immersing the wafer in Tetramethylammonium Hydroxide (TMAH) solution for approximately 12 minutes at 80°C temperature to obtain a randomly textures silicon surface Figure3.1(b5). Then, the wafers are dipped for 2 minutes in HNO_3/40% HF to obtain a slightly rounding of the pyramid to minimize the defects centers. It is important to note that the other side of the wafer (rear side) should be protected during the texturing process using a SiN_X layer which can easily be removed afterwards during an etching step in BHF solution.
2. Next, after removing the SiN*x* on the other side, the tunneling oxide layer is formed chemically by immersing the silicon wafer in the 69.5% solution for 60 minutes at the room temperature. The resulting ultra-thin oxide layer has a thickness of approximately 1.4-1.5 nm [24].
3. Then, samples are processed in the PECVD chamber to deposit an intrinsic a-SiO_X:H layer on the oxide layer. To obtain the intrinsic layer, the doping gases (PH_3 and B_2H_6) were set to zero, during the deposition.
4. After the intrinsic layer deposition, an implantation step is performed using Varian ion implanter E500HP where Phosphorous and Boron atoms, at certain implantation dosage and energy, are used to form the n^+ and p^+ regions, respectively.
5. Further, a post implantation high temperature annealing is performed at multiple temperature and duration to activate the dopants and to crystalize the amorphous silicon oxide layers and transforming to poly-SiO_X layer. The annealing time and temperature are changed to identify the optimal passivation conditions.

6. Finally, to further enhance the chemical passivation at the interfaces a forming gas (10% H_2 in N_2) annealing treatment is carried out in a tube furnace at constant temperature of 400°C for 30 minutes.

3.3 Optimization of PECVD intrinsic a-SiO_X:H thickness

This section presents the influence of the intrinsic a-SiO_X:H layer on the passivation quality of the carrier selective passivation contact enabled by poly-SiO_X, prepared with **ion-implantation** as doping approach. As previously introduced in section 3.1, combining both the optimum interlayer thickness and the doping concentration using a proper annealing conditions can boost the passivation, corresponding to the improvement in the electrical and optical properties of the tested wafer. The tested intrinsic layer deposited in PECVD chamber studied at different thicknesses (30, 50, 75 nm, respectively). The main aim of varying the thickness of the a-SiO_X:H layer is to check whether the **ion-implantation** energy was already sufficient for dopants to be implanted through this layer. The deposition is performed using an optimized recipe taken from a previously conducted study at PVMD group [72]. This study claims that the best deposition parameters are SiH_4 flow of 45 sscm, (1-2) mbar deposition pressure and 180°C as deposition substrate temperature. The studied symmetrical samples are depicted in figure 3.1(a). The doping concentrations of these samples is kept constant during the experiment. The ion implantation energy and dosage for the n^+ and p^+ regions are 20keV 5e15 ion/cm^2 and 20keV 6e15 ion/cm^2, respectively.

The a-SiO_X:H layer thickness tests were initially performed using flat symmetrical (n^+) poly-SiO_x samples as shown in figure 3.1(a). Figure 3.2 shows the iV_{OC} as a function of intrinsic layer thickness at different annealing time and temperature. Looking at the figure, we notice that all studied intrinsic layer thickness follow the same trend where the passivation quality decreases with increasing the temperature and annealing time. The optimum annealing temperature for the studied samples is obtained at lower temperature with a slightly higher iV_{OC} at 900°C. Analyzing the different thicknesses in the annealed state, the best results have been obtained for the intrinsic a-SiO_X:H layer with a thickness of 30 nm annealed at 900°C/5min with iV_{OC} value of 646 mV and τeff of 312 µs .

Additionally, considering Figure 3.2, it is hard to miss that the use of thicker intrinsic layers results in affects the level on cell passivation, with obviously decreasing trend. It is suspected that this low passivation qualities and trend can be attributed to the fact that the use of the doping concentration was not sufficient. It is mainly due to the oxygen existence within the a-SiO_x:H layer increases the difficulty to implant P and B into the thin film, as what was reported for the SiO_2 materials [73]. Thus, this will result in a poorer field-effect passivation. Furthermore, all testes samples show a very bad passivation with increasing the thickness and annealing temperature and time. This can be explained that due to the limited doping atoms that are implanted into the a-SiO_x:H, increasing the layer thickness or annealing thermal budget will decrease the doping level within the poly-SiO_x materials, therefore limits the field effect passivation. On the other hand, when a too high annealing thermal budge is used, in the oxide layer, pinholes are formed before the breaking of the oxide layer. The presence of this tiny pinholes enhances the charge carrier conductivity through introducing a local contact between the doped poly-SiO_X layer and the c-Si bulk material. This will increase the recombination current as the Auger recombination becomes dominant and the passivation decreases significantly. Moreover, Phosphorous dopants may diffuse too far into the bulk material at higher temperature which lowering the field effect passivation [74] and increasing the Auger recombination.

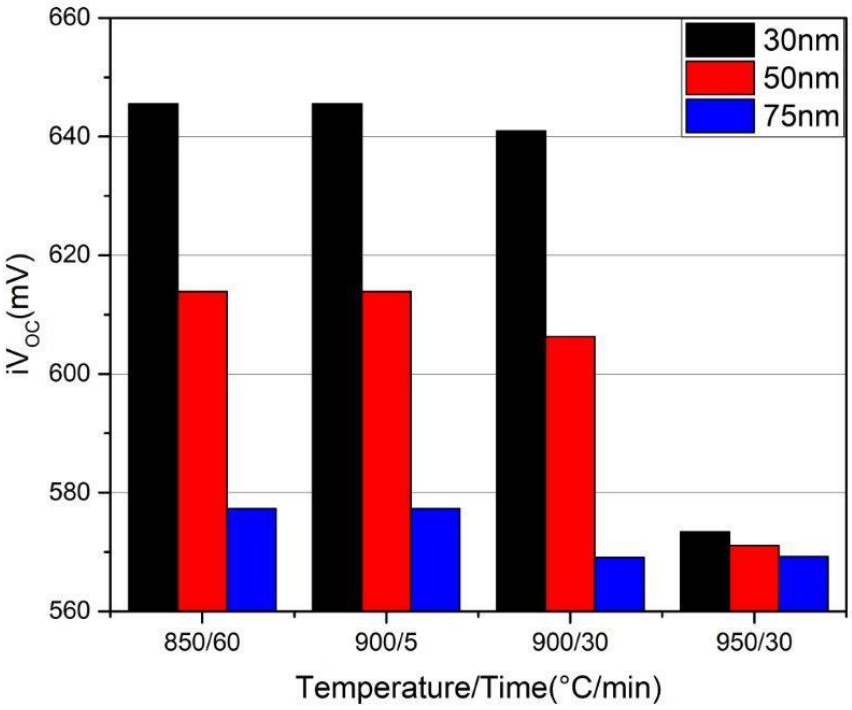

Figure 3.2: Passivation properties of various intrinsic layer thickness after annealing for the symmetrical (n^+) poly-SiO_X samples.

The optimization of the intrinsic a-SiO_X:H layer thickness was not only studied for (n^+) poly-SiO_X symmetrical samples but also for the (p^+) poly-SiO_X symmetrical test samples as shown in figure 3.1(a). The main aim of this test is to optimize the passivation quality in the emitter region at the bifacial-IBC solar cell rear side.

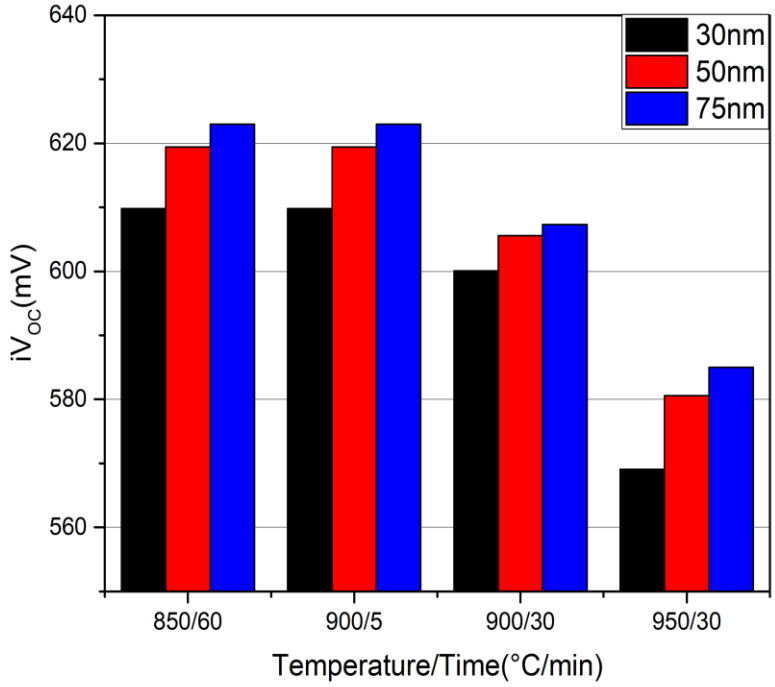

Figure 3.3: Passivation properties of various intrinsic layer thickness after annealing for the symmetrical (p^+) poly-SiO_X samples.

Figure 3.3 indicates the passivation properties of various intrinsic layer thickness for the (p^+) poly-SiO_X symmetrical test samples at different annealing conditions. Analyzing the figure 3.3, we notice again that all studied intrinsic layer thickness follow the same trend where the passivation quality decreases with increasing the temperature and annealing time. The optimum annealing temperature for the studied samples is obtained at lower temperature. However, looking at the different thicknesses in the annealed state, in contrast to n^+ layer results, the best results have been obtained for the intrinsic a-SiO_X:H layer with a thickness of 75 nm annealed at 850°C/60min with iV_{OC} value of 623 mV and τeff of 73 µs.

Further, considering Figure 3.3, it is recognizable that the use of thicker intrinsic layers results in slightly better passivation properties. It's suspected that since B atoms are smaller than P atoms, they can be implanted much deeper. As a result, the B may already be implanted into the a-SiO_X/NAOS-SiO*x* for thinner a-SiO_X layers. Thus, the passivation is low for thinner sample. Same findings hold for 75nm thick layer. This is due to the insufficient doping level as the a-SiO*x* is difficult to be implanted. Furthermore, all testes samples show a very bad passivation with increasing the annealing conditions (temperature and time). This may be due to the fact that using these conditions for the test could be too extreme, causing a break in the tunneling oxide layer, resulting in pinhole formation, and thereby reducing chemical passivation [70]. Furthermore, at higher temperatures, phosphorus dopants can diffuse too far into the bulk material, reducing field effect passivation.

3.4 Hydrogenation effect

Hydrogenation process is used to further improve the passivation quality by eliminating defects at the SiO_2/poly-SiO_X interface. As mentioned previously in chapter 2, the hydrogenation treatment is very important for improving the passivation by introducing additional hydrogen atoms needed to further enhance the chemical passivation. The improvement of chemical passivation will result in an increasing in the minority carrier lifetime and the implied open circuit voltage and eventually better solar cell performance. The objective of this section is to decide the best hydrogenation configuration for the cell rear structure. This is accomplished by preparing three poly-SiO_X symmetrical n^+ test samples on flat surface using ion implantation. The tests three samples are compared as follow: the first sample is only annealed at 850°C for 60 min as it gives the best passivation quality from the previous test. The second sample prepared by performing a forming gas annealing (FGA) treatment in tube furnace for 30min at 400°C. For preparing the last sample, a 75nm SiN_X layer is deposited by PECVD followed by an FGA step. The passivation quality of these samples is measured and showed in figure 3.4.

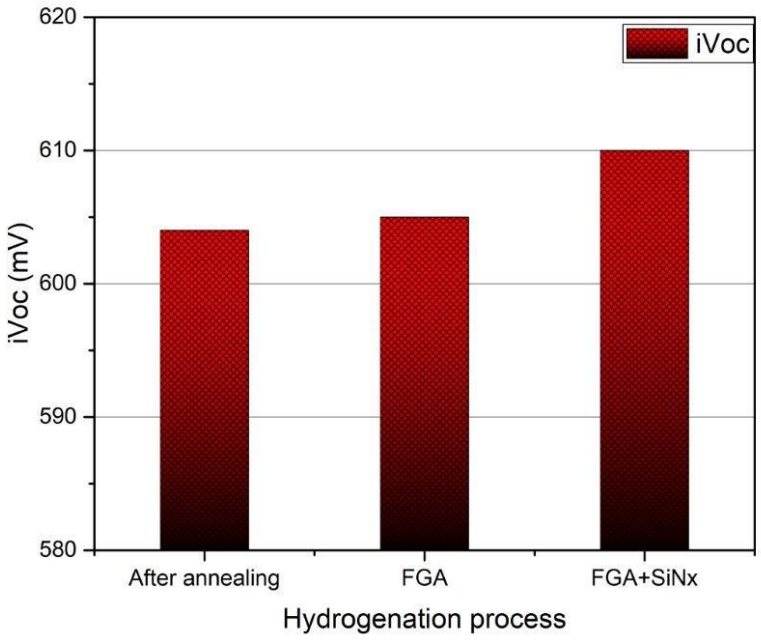

Figure 3.4: The influence of Hydrogenation on the passivation qualities of n^+ poly-SiO_x passivating contacts.

Analyzing the previous results, we notice that the tested symmetrical samples demonstrate different level of passivation qualities. The passivation measurement of the first sample with no hydrogenation treatment after annealing gives an iV_{OC} 604 mV which will be used as a reference. The second sample with only FGA had a slight gain of iV_{OC} of only 1mV. However, measuring the third sample SiN_X+FGA showed an increasing in the iV_{OC} (from 604mV to 610mV) but it still very poor optimized passivation quality.

As indicated above in figure 3.5, it is hard to conclude whether the samples benefit from the hydrogenation treatment, however no significant improvement for the measured iV_{OC} is achieved for all the tested samples. This means that the additional hydrogen atoms are passivating small portion of defects at SiO_2/poly-SiO_X interface. Which dominates the recombination, when the field effect passivation is too weak due to the low doping level

To proof the previous hydrogenation results, the hydrogenation process is also performed on the test samples used to test intrinsic a-SiO_X:H layer thickness in section 3.3. Results show again no additional gain in the passivation properties which means that hydrogenation process cannot further enhance the passivation.

3.5 Conclusion

In this chapter the optimization of the carrier selective passivation contacts is examined using a new doping and pattering approach of poly-SiOX passivating contacts with ion implantation to fabricate a bifacial-IBC solar cell. First, the crucial requirements to enhance the passivation quality is discussed.

Next, the optimization of the intrinsic a-SiO*x*:H layer thickness deposited by PECVD at different annealing conditions is examined. The best passivation results obtained from this approach was 646 mV, and 623 mV for the n^+ and p^+ layer, respectively with the annealing thermal budge of 850/60min giving the best annealing conditions.

Then, the best hydrogenation configuration was explored. Hydrogenation results show no significant improvement in the implied open circuit voltage using two different hydrogenation approaches with slightly better improvement using SiN_x+ FGA as hydrogenation treatment [75].

The passivation qualities for both the n^+ and p^+ were very low. This can be further optimized by investigating the doping concentration using different ion dosage and energy to obtain the best doping profile. However, due to limitation in the implanter range used in the EKL lab, 5 keV as a minimum value, and the machine maintenance/down time we cannot further proceed with this flow chart.

Therefore, we decided to shift to the already developed more complicate IBC solar cell flow chart used at PVMD group with adjusting some few steps to fabricate a high energy bifacial-IBC solar cell, which will be introduced in the next chapter.

4 In-situ doped poly-SiO_X passivating contacts for Bifacial-IBC solar cell

The aim of this chapter is to optimize the passivation quality of passivating contacts made of PECVD in-situ poly-SiO_X carrier selective passivation contact to fabricate bifacial-IBC solar cell. Each process of the IBC cell process is optimized separately in order to investigate different variable parameters of the process phase. The first goal was to optimize the doped n^+ and p^+ layer thickness using different intrinsic layer deposition methods. Next, the essential hydrogenation process is also examined to further enhance the passivation quality. Subsequently, tests are performed to determine the best sequence of implementing the FSF passivation and poly-SiO_x hydrogenation steps. The patterning of ITO layer is also studied before the cell fabrication. Finally, the optimized obtained results are applied to fabricate the bifacial-IBC solar cell.

4.1 Solar cell fabrication

The complete fabrication processes for the bifacial-IBC solar cell is proofed to be implementable and will be explained step by step in this section. Figure 4.1 illustrates the schematic sketch of the used flowchart to fabricate the solar cell.

Starting from n-type float zone c-Si wafer <100> orientation, resistivity of 1-5 ohm.cm, and a thickness of 260≃300 μm. It is worth to note that multiple cleaning steps were applied during the cell fabrication, but it is not mentioned here to keep the structure clear. The fabrication steps of the bifacial-IBC solar cell enabled by poly-SiO_X carrier selective passivating contacts is done as follow:

1. First, a standard cleaning step, defined in section 2.1, is used to clean the n-type wafer. However, a thin SiO_X layer is formed during this process. Therefore, this thin oxide layer must be removed later by dipping the wafer in 0.55% HF solution for approximately 4 minutes remove this layer and any native oxide layer.
2. After that, the tunneling oxide layer is grown chemically by immersing the wafer in 69.5% HNO3 solution for 60 minutes at room temperature. This step results in a tunnel oxide layer of approximately 1.5 nm on the wafer both sides [24].
3. Next, a thin 10 nm a-SiO_X:H layer is deposited on both wafer sides in the LPCVD furnace on top of the tunnel oxide layer.
4. Subsequently, a doped (p^+) poly-SiO_X layer is deposited with different layer thicknesses on the cell rear side. The deposition of the doped layers is performed through PECVD deposition approach.
5. Afterwards, a SiN_X layer with a thickness of 250 nm is deposited using PECVD on cell rear side. This layer will be used as a protective layer, using photolithography process, during the emitter region

formation which will be removed later using dry etching. This is followed poly etching step to remove the undesirable buffer layers. Finally, the wafer is dipped again in 69.5 % HNO3 solution for 1 hour to shape the thin oxide layer before forming the BSF contact.

6. Following, the deposition of the intrinsic and doped (n^+) poly-SiO_X layers on the cell rear side is applied via PECVD deposition method.
7. Again, a SiN_X protective layer with a thickness of 250 nm is deposited using PECVD to protect the cell rear side during the texturing of the front side using TMAH solution at 80°C for 15 min.
8. Then, the second photolithography step is performed to protect BSF contact during the following BHF (15 min) and poly-etch (10 min) steps used to remove the desirable SiN_X and doped (n^+) poly-SiO_X layers at the cell rear side.
9. Further, an implantation step is implemented using Varian ion implanter E500HP, 10 keV and $1e^{14}$ implantation energy and dosage, to form a lightly doped FSF layer on the cell front side.
10. The entire structure is annealed in one step using a high temperature annealing process at 850°C for 53 min, as optimized in section 4.4, to activate and drive in dopants for both passivating contacts at rear side and FSF.
11. Next step is the hydrogenation process that is applied to further optimize the passivation. It is done by depositing a 75 nm SiN_X layer using PECVD method on the rear side followed by a forming gas annealing treatment which carried out in a tube furnace at constant temperature of 400°C for 30 minutes.
12. On the front side, a 9 nm thin a-Si:H passivation layer is deposited at 250°C using PECVD method. Followed by the deposition of a 75 nm SiN_X capping layer deposited at 400°C through PECVD method.
13. On the rear side, an etching phase was used to separate the emitter and BSF areas, eliminating the possibility of a shunt area until the SiNx layer was etched. The third photolithography process was used to determine the isolation regions. It is worth to note that a photoresist layer is coated on the front side to protect the front passivation layers during performing the etching step.
14. Next, an 80 nm ITO layer thickness is deposited on a silicon wafer using Zorro sputtering machine on the wafer rear side. This is followed by a photolithography process to indicate the isolated regions (BSF and emitter) during an etching step in HCL solution to etch the ITO layer in the gab.
15. Afterwards, two different metal seed layers are deposited (200 nm Aluminum and 200nm Silver) using e-beam evaporation followed by the last photolithography process to pattern the metal fingers before the copper plating.
16. Finally, the cell is immersed in the copper plating bath to form the metal fingers with about 15 µm. This is followed by an etching step using (NH_4OH+ H_2O_2+ H_2O) solution to etch away the Al and Ag seed layers between the Cu fingers.

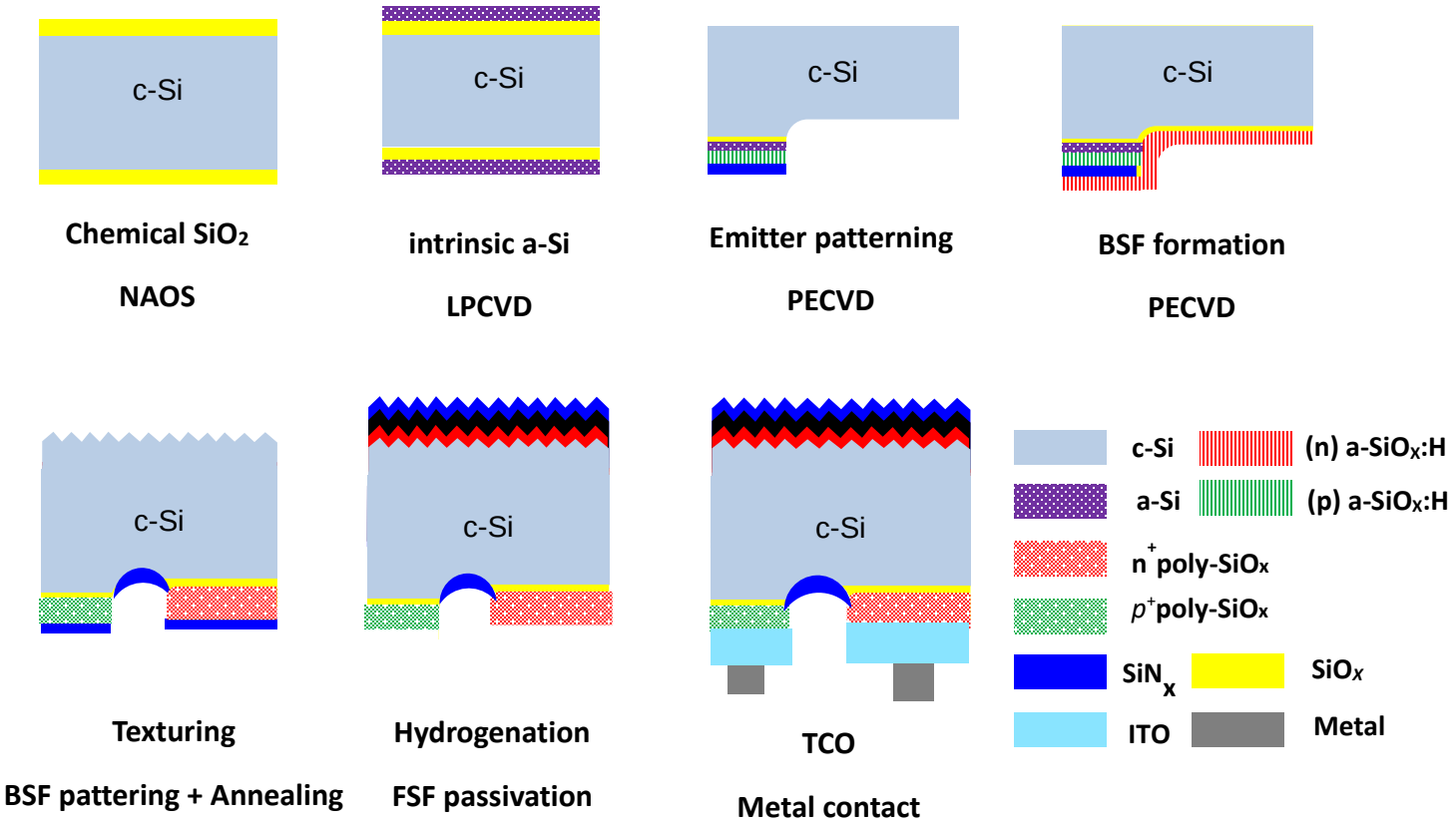

Figure 4.1: Schematic sketches of the fabrication of poly-SiO_x Bifacial-IBC solar cell.

4.2 Experimental details

This section includes the explanation of the implemented different fabrication processes to obtain the best passivation quality of the passivating contacts. The passivation tests are performed on a flat surface symmetrical test samples to examine the passivation properties on both rear contacts of the solar cell. The symmetrical test samples are fabricated with the exact steps needed to fabricate the bifacial-IBC solar cell to obtain the best imitation of the final solar cell. A schematic of all the processing steps and deposited layers are shown in figure 4.2 in order to give a clear overview of the manufacturing process.

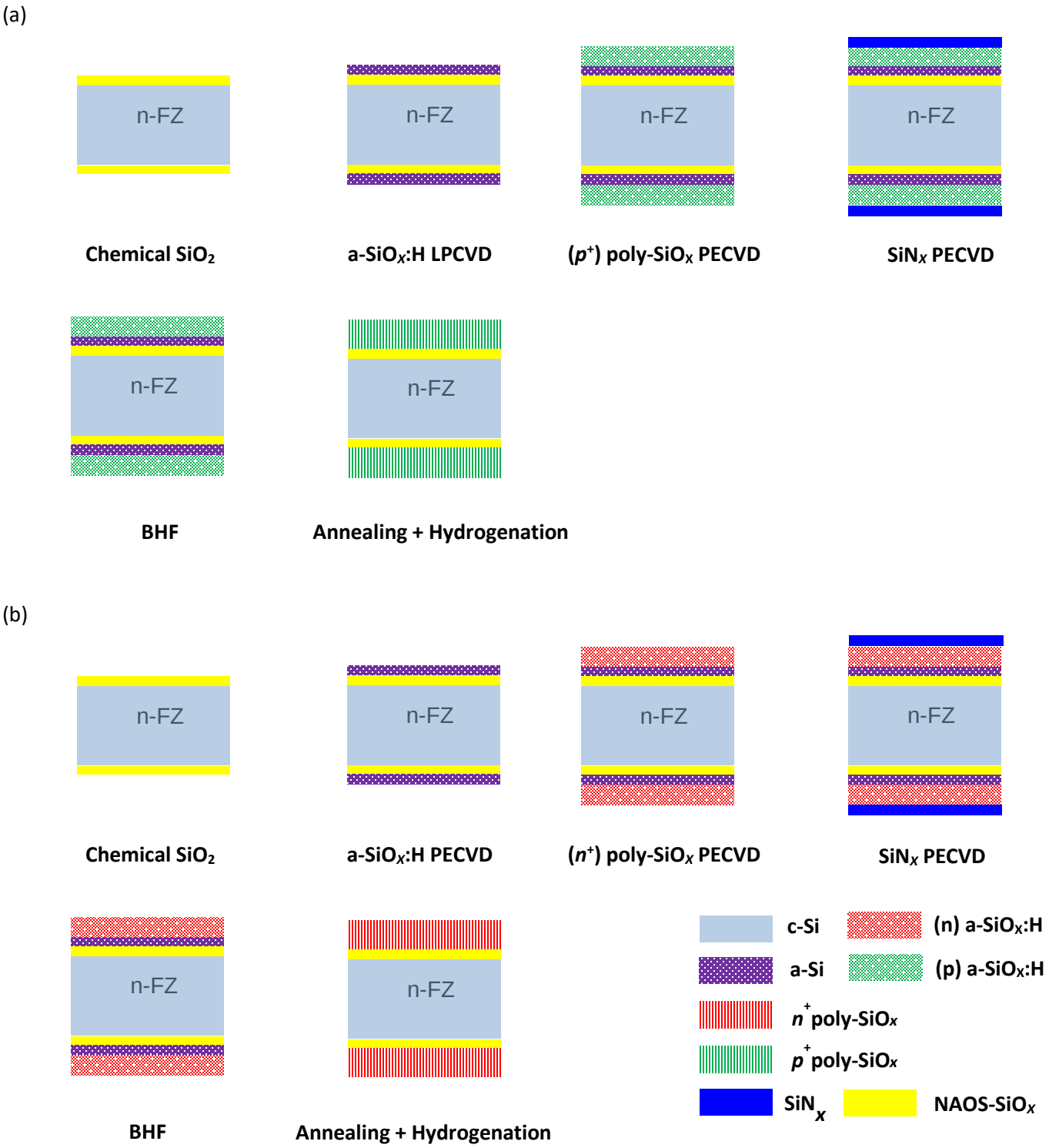

Figure 4.2: Symmetrical sketches for processing the passivation test samples: (a) p^+ poly-SiO_X test sample. (b) n^+ poly-SiO_X test sample.

7. The first point of the fabrication process is the use of an n-type double side polished FZ Si wafer with <100> surface orientation and with an initial thickness of 280 µm. It is worth to mention that only the crucial steps are indicated in this section, however the other non-crucial steps such as cleaning is skipped in order to keep the examined process clear. The fabrication of the symmetrical test samples based on poly-SiO_X carrier selective passivating contacts is shown in figure 4.2 and test samples are prepared as follow: The starting point of preparing the symmetrical test samples was using a flat polished surface.
8. Then, the formation of the tunneling oxide layer (typically 1.4-1.5nm) [24] is prepared chemically by dipping the silicon wafer in the 69.5% solution at the room temperature for 1 hour.
9. Next, samples are processed either in LPCVD tube furnace or in the PECVD chamber to deposit a thin intrinsic a-SiO_X:H layer with approximate thickness of 10 nm on the tunnel oxide layer. The reason behind using both PECVD and LPCVD will be discussed in detail in section 4.3.1.
10. After the intrinsic layer deposition, a doped (p/n) a-SiO_X layer is deposited at different thicknesses. The deposition of the doped layers is performed through PECVD deposition approach.
11. Later, a SiN_X layer with a thickness of 250 nm is deposited through PECVD method which will be used as a protective layer during the formation of the emitter region and back surface field (BSF) contact during the following etching step.
12. Subsequently, an etching step in BHF solution is performed to etch away the undesirable buffer layers. This etching step is included in the symmetrical test because it is an important step in the used flow chart to fabricate the solar cell.
13. Further, a high temperature annealing is performed at 850°C and different duration to activate and drive in the dopants in the emitter and BSF contacts. The annealing time is varied to identify the best passivation conditions.
14. Finally, to further optimize the chemical passivation at the interfaces a hydrogenation step consists of the deposition of 75 nm SiN_X using PECVD method followed by a forming gas annealing (FGA) treatment which carried out in a tube furnace for 30 minutes at constant temperature of 400°C.

4.3 Optimization of the (p^+) poly-SiO_X layer thickness

In the bifacial IBC solar cell, in order to achieve a higher bifaciality factor, the passivating contacts layer should be as thin as possible, for the aim of minimizing the parasitical absorption on the rear side. The main goal of this section is to optimize the doped (p^+) poly-SiO_X layer thickness while maintaining the passivation quality. The deposition of this layer is only applied through PECVD at a constant gas flow level using an optimized recipe taken from a previously conducted study at PVMD group [69]. During this experiment, two intrinsic layer deposition methods are investigated to achieve the best passivation quality namely PECVD in the deposition chamber and LPCVD in the tube furnace. According to the previous investigation at PVMD group, results claim that the use of 10 nm as an intrinsic layer thickness gives the best passivation results for poly-SiO_X passivating contacts [76].Therefore, the deposition of the intrinsic layer thickness was decided to be constant 10 nm on the wafer flat surface.

4.3.1 PECVD intrinsic a-SiO_X:H layer

The first examined deposition method of the intrinsic buffer layer was PECVD. This method is preferred because it can be applied on one side of the wafer which adds a simplicity to the solar cell fabrication process. Additionally, it can be formed at desirable layer thickness. However, after the deposition of the SiN_X layer through PECVD at 400°C, which is a crucial step in the solar cell fabrication as this layer is used as an etching barrier, a massive blistering effect is noticed on the wafer surface. Blistering formation is a common problem in the TOPCon structure in which PECVD is used to deposit the intrinsic a-Si:H layer on the tunneling oxide thin film [77]. Blistering is commonly appearing on the wafer surface after the following high temperature annealing process [78]. It occurs when hydrogen rich species, a-Si:H or SiN_X in our case, release its hydrogen content which cannot diffuse out as the SiN_X layer acts as a barrier preventing the diffusing of the hydrogen atoms [77]. The blister takes the shape of white dots (bubbles) on the capping layer surface which not only affect the appearance of the wafer but also results in a degradation in the passivation quality [77].

It is worth to mention that the blister formation is still a question as the blister effect reduction is not yet fully understood. To suppress the blister formation, the effect of the deposited intrinsic layer thickness and the SiN_X layer deposition temperature is studied. The tested intrinsic layer, deposited in PECVD chamber, compare the deposition of three different thicknesses (10 nm, 15 nm, and 20 nm). Next, a 20 nm doped (p^+) layer deposited through PECVD followed by an annealing process at 850°C for 60 min for which kept constant for all the examined tests. Additionally, three different SiN_X deposition temperature at (300°C, 350°C, and 400°C) are also studied. The optical images of the tested samples surface are shown in figure 4.3.

First, the intrinsic thin layer thickness effect is studied and indicated in Figure 4.2(a-c). Looking at the optical images taken using a profile analyzing laser microscope, it is very clear that decreasing the intrinsic layer thickness reduces the blister effect significantly. This is an obvious result as decreasing the layer thickness will lower the hydrogen content in the deposited layer.

Next, the effect of the PECVD SiN_X layer deposition temperature is also examined. Analysing the optical images in figure 4.2(d-f), it is hard to miss that lowering the deposition temperature reduces the blister formation dramatically where the best results obtained in case (f) using 300°C as a deposition temperature. These are not surprizing results as increasing deposition temperature enhance the H_2 effusion from the a-SiO_X layer during the SiN_X deposition which eventually increases the blistering effect.

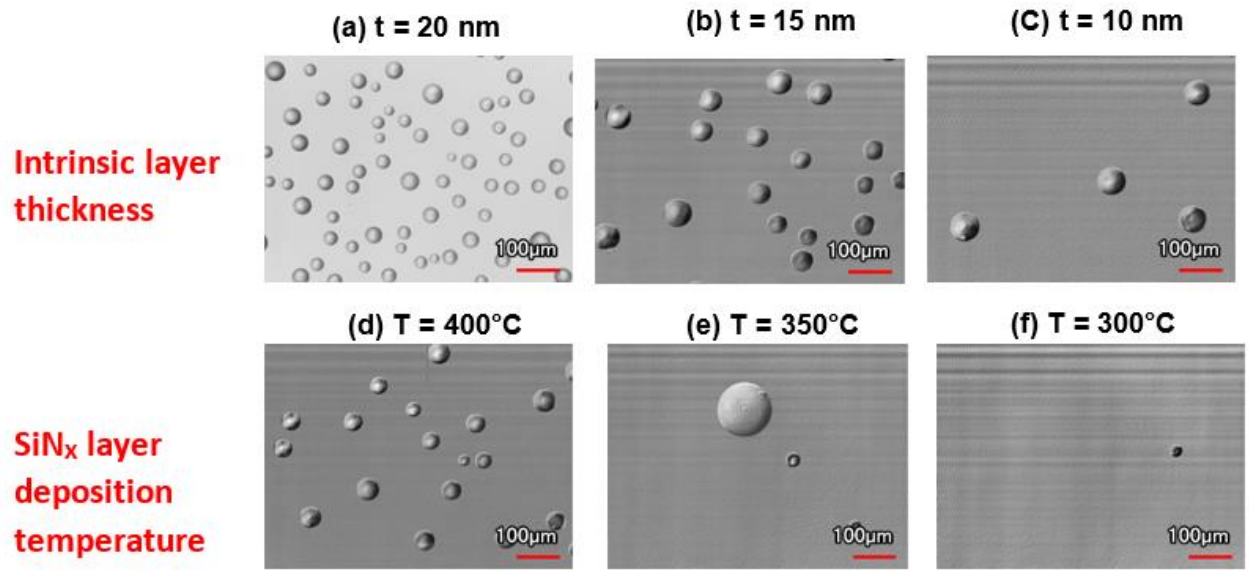

Figure 4.3: Series of an optical images of test samples surface. (a-c) show deposition at three different intrinsic layer thickness (20, 15, and 10 nm). (b-d) indicate images after the deposition of SiN_X layer at various temperature (400°C, 350°C, and 300°C).

Figure 4.4 demonstrates the iV_{OC} values as functions of different intrinsic layer thicknesses and the variable SiN_X layer deposition temperature for the tests discussed above. All studied cases show an overall low iV_{OC} despite the reduction in the blister density at thinner interlayer thickness and lower deposition temperature. The best obtained iV_{OC} was 575 mV for test sample (f) after performing the hydrogenation treatment, which is mainly due to the blistering of poly-SiO_x layers. This passivation quality is not sufficient to fabricate our high efficiency solar cell, thus it is decided to deposit the intrinsic layer through LPCVD although it adds complexity to our process, because of the already proofed fact that no blistering was observed for the LPCVD intrinsic layer.

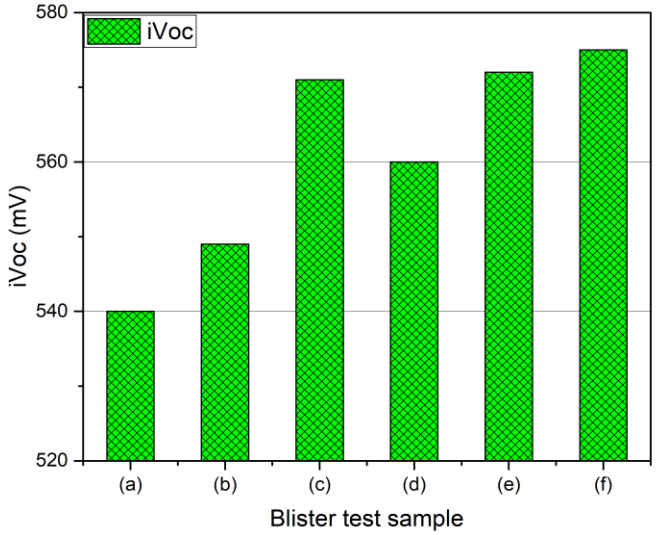

Figure 4.4: iVoc as a function of (a-c) various intrinsic layer thickness (20, 15, and 10 nm) and (d-f) different SiN_X layer deposition temperature (400°C, 350°C, and 300°C).

4.3.2 LPCVD intrinsic a-SiO_X:H layer

The second examined deposition method of the intrinsic buffer layer was LPCVD. This method in applied as we cannot eliminate the blistering effect from the test sample surface in which the intrinsic layer is formed by PECVD. Initially, a simple test is performed to see whether the blister on the sample still appear. Fortunately, the blistering problem is observed. Therefore, a fixed 10 nm intrinsic layer deposited through LPCVD in the tube furnace for 5 min is used for all the following tests. As shown in section 3.1, varying the thickness of the doped layer affects the diffusion of the dopants in the intrinsic layer during the annealing step. Thus, the optimization of the p^+ doped layer was subjected to the change of the thickness to obtain the best layer thickness. Therefore, three different doped p^+ layer thickness (20, 25, and 25 nm) is deposited on the top of the intrinsic layer using PECVD. Next, a SiN_X layer is deposited and removed again to copy the same flow chart fabrication applied steps. This is followed by a constant high temperature annealing step at 850°C but using different annealing time range (37-60 min).

The thickness of the p^+ poly-SiO_X layer was varied using relatively thin layer thickness in the range of 20-30 nm as showed in figure 4.5. It is important to note that the use of a thinner layer is more beneficial for our cell as it leads to less optical losses. However, the test of a thicker doped layers is crucial here due to the applied BHF etching step needed to fabricate the solar cell. The BHF solution may also remove a fraction of our doped layer that is the reason why we increase the doped layer thickness to ensure that the doped layer in not completely etched away during the proof of concept cell processes.

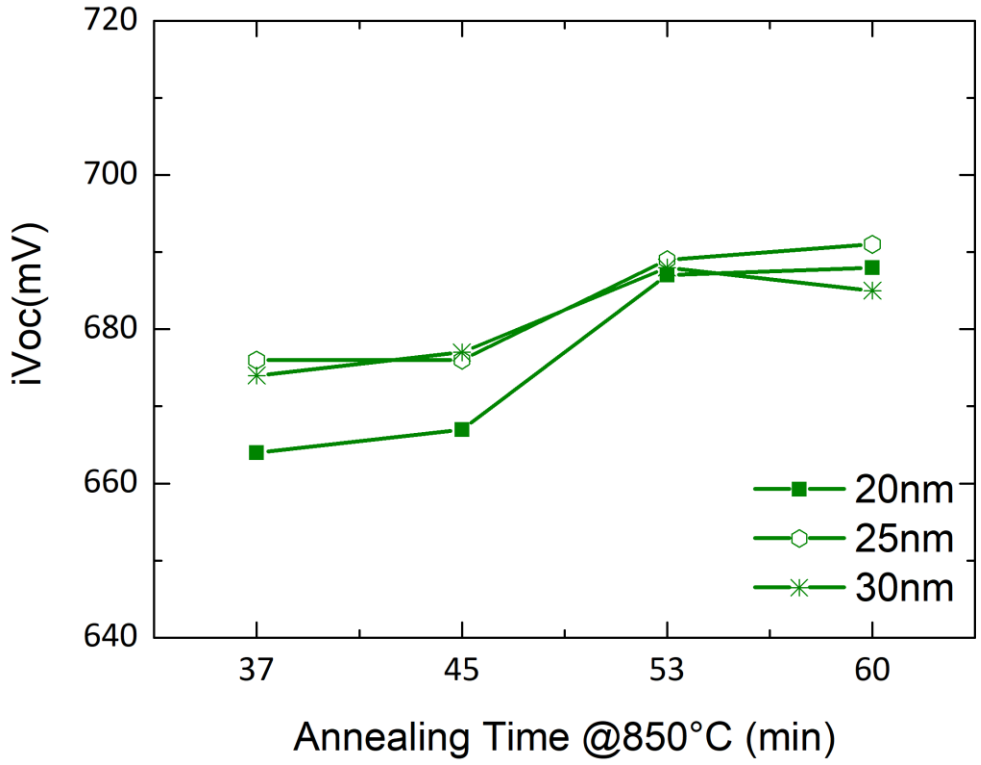

Figure 4.5: Passivation quality of p^+ poly-SiO_X test samples annealed at 850°C for different annealing time before hydrogenation.

Looking at Figure 4.5, we see that the annealing temperature is kept constant at 850°C while the annealing time is increased from 37 to 60 min. Results show an increasing trend for all the testes samples with increasing the annealing time. The maximum obtained iV_{OC} was 691 mV at 60 min before hydrogenation for the p^+ contact. The highest iV_{OC} value is obtained with a moderate doped layer thickness of 25 nm. This may be attributed to that the use of a thin or thick doped layer thickness results in a low or high doping level, respectively. In other words, the low doping level leads to a poor field effect passivation while the high doping level cause a deeper dopant diffusion in the bulk material surface. Both cases result in an insufficient band bending, and increased Auger recombination, which will eventually lower the passivation quality.

4.4 Optimization of the (n^+) poly-SiO_X layer thickness

The deposition for the n^+ contact region is applied through PECVD for both the intrinsic and doped layer as shown in section 4.1. The use of PECVD to form the intrinsic and doped layer will ease the fabrication process of our bifacial IBC solar cell. As mentioned previously, the optimization of the n^+ poly-SiO_X layer thickness plays a vital role in enhancing the passivation characterization. The optimization is done by varying the doped layer thickness to have the best passivation properties as the back-surface field (BSF) for the bifacial solar cell. First a varied thin intrinsic layer thickness (7, 10, 13 nm) deposited by PECVD. This is followed by also PECVD deposition of the doped layer at different thickness (13, 20, 27 nm). Next,

a SiN_X layer is deposited and removed again to copy the same performed steps used in the bifacial solar cell flow chart. Finally, an annealing step at constant temperature 850°C is applied using different annealing time range (37-60 min).

As shown in figure 4.6, the thickness of the p^+ poly-SiO_X layer was varied by using relatively thin layer thicknesses in the 13-27 nm range. It's worth noticing that using a thinner layer is better for our cell because it results in less optical losses. But since BHF etching solution can remove a fraction of our doped layer, we increase the thickness of the doped layer to ensure that it is not fully etched away. Therefore, testing thicker doped layers thicknesses is also essential because of the BHF etching phase used to fabricate the solar cell.

Figure 4.6 indicates the passivation quality of n^+ poly-SiO_X test samples annealed at constant temperature 850°C for different annealing time increased from 37 to 60 minutes. It is hard to miss that increasing the annealing period shows an increasing trend for all test samples. The obtained maximum iV_{OC} was 694 mV at 53 min before hydrogenation for the n^+ contact. Additionally, increasing the doped layer thickness yields the higher iV_{OC} value. The best iV_{OC} value is obtained with a thicker doped layer thickness of 40 nm. This may be due to the fact that the use of a thick doped layer results in a better dopants profile at the interfaces which contributes a better field effect passivation.

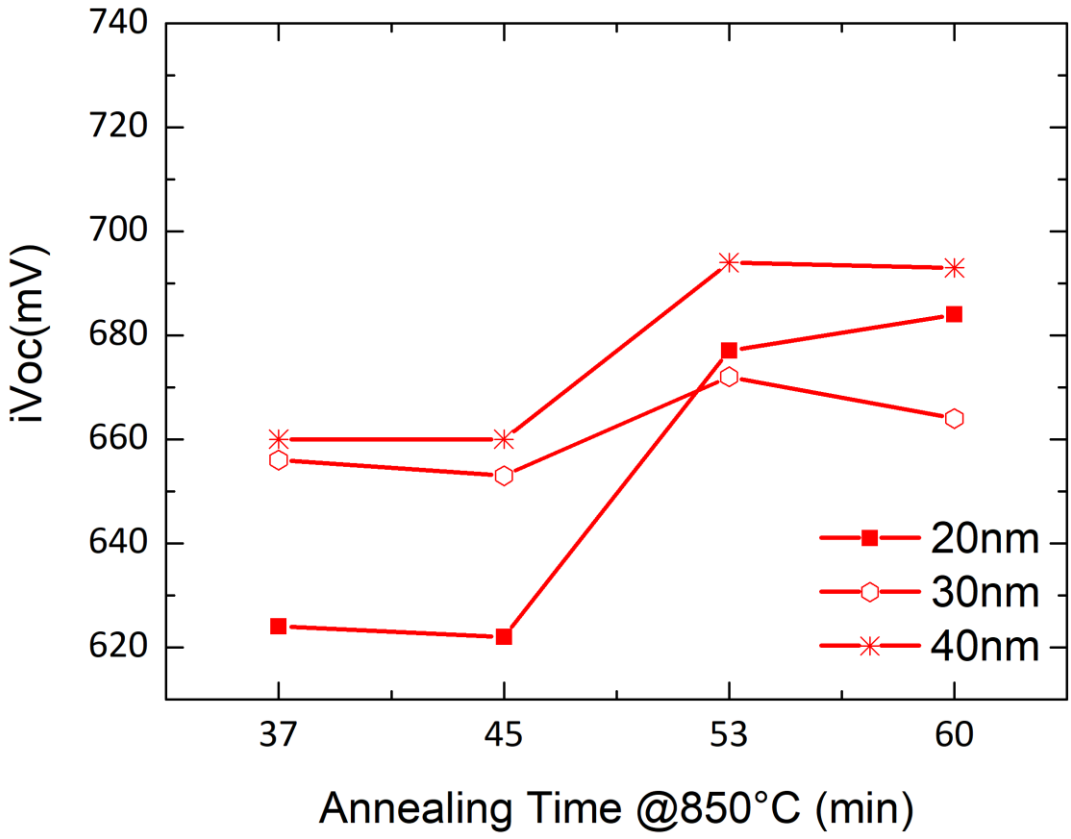

Figure 4.6: Passivation quality of n^+ poly-SiO_X test samples annealed at 850°C for different annealing time before hydrogenation.

4.5 Hydrogenation optimization

The optimization of the hydrogenation process for the poly-SiO_X contact is examined in a previous thesis work in PVMD group [71]. The previously conduct study claims that the best hydrogenation treatment is obtained with combining a thin SiN_X layer (75nm) deposited by PECVD followed by a direct forming gas annealing process in the tube furnace for 30min at 400°C. Therefore, this hydrogenation scheme is applied to both p^+ and n^+ symmetrical test samples and the passivation properties was as follow:

First, the passivation quality of the p^+ contact is shown in figure 4.7. Results show an excellent passivation improvement for all the test samples after performing the hydrogenation step based on the optimized recipe. This increase in passivation properties shows that the additional provided hydrogen atoms from the capping layer effectively passivates the defect-rich c-Si /SiO_2 interfaces. Looking at figure 4.7(a), we see that the passivation results follow the same trend before hydrogenation. In other words, an increasing trend is noticed with increasing annealing time despite some declining at 45 min. However, the iV_{OC} has improved significantly reaching the highest value of about 714 mV at 53 min.

The passivation quality of n^+ contact after hydrogenation is also considered and shown in figure 4.7(b). Results show an excellent passivation improvement for all the test samples after performing the hydrogenation step. This boost in passivation quality means that the additional hydrogen atoms, provided by the SiN_X capping layer, excellently passivates the high defect density at c-Si/SiO_2 interface. Interestingly, in contrast with results before hydrogenation process, good passivation results were achieved with less annealing time after hydrogenation treatment. The best passivation so far is achieved for n^+ contact reaching 730 mV when annealed at 850°C for 37 min.

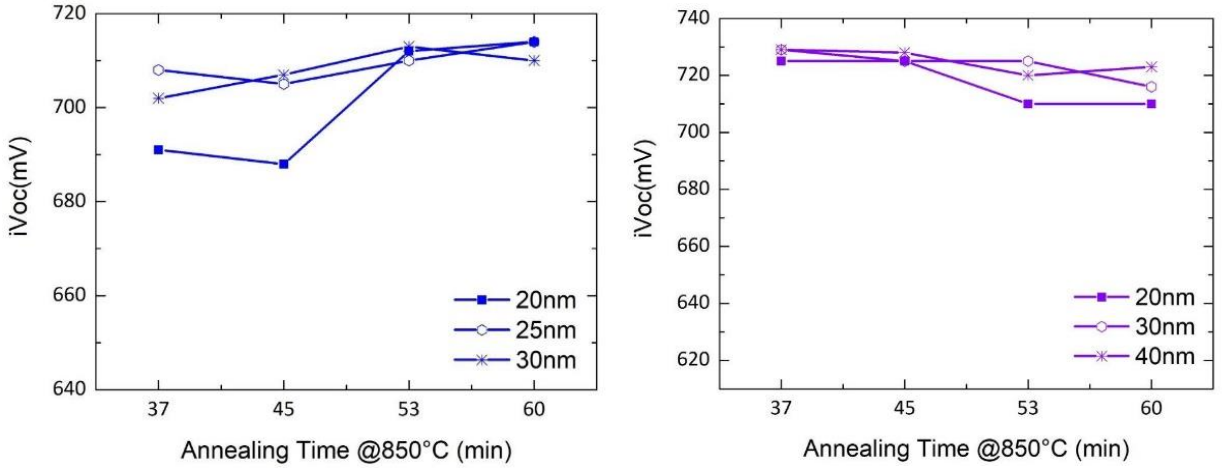

Figure 4.7(a): Passivation quality of p^+ poly-SiO_X test samples annealed at 850°C for different annealing time after hydrogenation. Figure 4.7(b): Passivation quality of n^+ poly-SiO_X test samples annealed at 850°C for different annealing time after hydrogenation.

4.6 Front surface field (FSF) passivation test

The output of the bifacial-IBC solar cell enabled by poly-SiO_x passivating contacts is impacted not only by the passivating contact at the back side, but also by the front surface field passivation quality. This section is focusing on FSF optimization in terms of investigating the effect of rear hydrogenation process on the FSF passivation quality. This is done to determine whether the FSF passivation should be applied before or after the crucial hydrogenation treatment at the bifacial-IBC solar cell rear side.

Before discussing the executed test, it is worth to note the benefit of adding front surface field to enhance the solar cell performance. Typically, a stack of a Phosphorus implanted surface, passivation layer, and an anti-reflecting coating (ARC) layer form the front surface field. These layers should be optimized to obtain the highest possible passivation quality; however, this is outside the scoop of this project.

First, the Phosphorous implanted c-Si surface provides an electric field needed to reject the minority carriers (holes) generated near the front surface and eventually increase the short circuit current due to promoting the solar cell blue response [5]. However, high doping concentration is needed to generate a sufficient electric field. On other hand, a too high doping concentration can increase Auger recombination and induce a high level of parasitic absorption in the solar cell front side. Therefore, the optimization of the implantation dose in the FSF is crucial to enhance both the iV_{OC} and J_{SC}.

Next, a-Si:H deposited through PECVD is used as a passivation layer during this experiment. It has already been shown to be a reliable material for surface passivation and allowing a V_{OC} of 750 mV [79]. The optimization of this layer enhances both the optical and electrical properties of the solar cell. In other words, if the a-Si:H deposited on the front surface is too thick, this will increase the parasitic absorption and, as a result, a lower J_{SC} will be obtained. On the other hand, if the a-Si:H layer is too thin, this may result in an insufficient passivation at the front side and thus reduces the iV_{OC} of the solar cell.

Finally, the additional SiN_X capping layer deposited by PECVD can further enhance the passivation on the front side. This layer acts as anti-reflection coating (ARC) layer that helps to capture more incident light on the solar cell front side, minimizes the surface recombination by passivating the surface defects, and the contained hydrogen atoms in this layer can also enhance the surface passivation.

In this section, the previously optimized FSF conditions are applied to conduct the experiment [80]. The starting point of fabrication process is the use of an n-type double side polished FZ Si wafer with <100> surface orientation and with an initial thickness of 280 µm. The test fabrication steps are shown in figure 4.8 and done as follow: First, to replicate the structure of the front surface, a symmetrical textured samples are prepared by immersing the sample in TMAH bath at 80°C for about 10 minutes until the <111> lattice is created. Next, an implantation step is implemented using Varian ion implanter E500HP, where Phosphorous atoms, at 10 keV $1e^{14}$ implantation dosage and energy, to form a lightly doped FSF layer. Further, a thin a-Si:H passivation layer with 9 nm thickness is deposited at 250°C deposited using PECVD method. Finally, a 75 nm SiN_X capping layer thickness deposited through PECVD method at 400°C. The fabrication steps of the textured symmetrical sample for FSF test are shown in Figure 4.7.

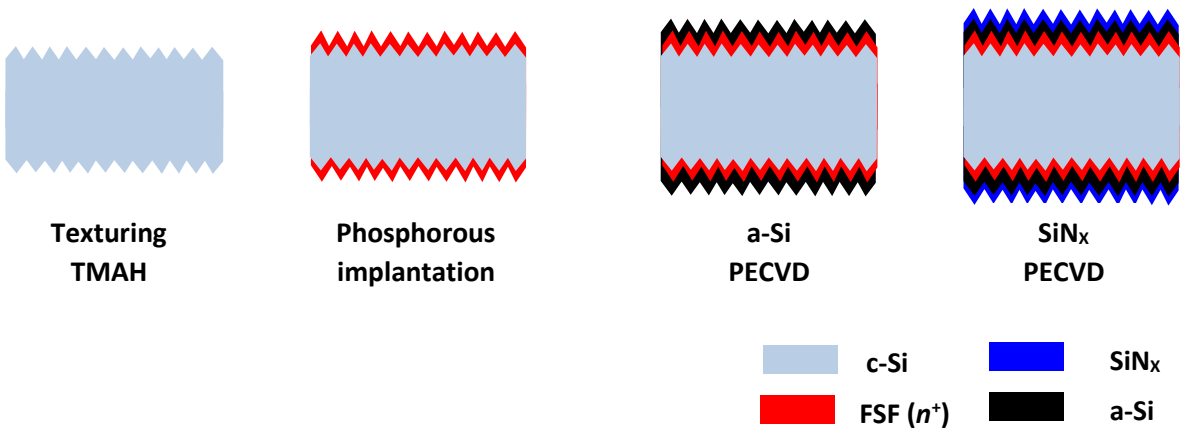

Figure 4.8: Fabrication steps of the textured symmetrical sample for FSF test.

The passivation results of the symmetrical test sample are presented in table 4.1. Measuring the iV_{OC} of the test sample after preparing the FSF stack layers gives a good passivation value of 714 mV. As shown in section 4.5, the hydrogenation treatment (SiN_X+FGA) on the solar cell rear side gives a boost in the passivation quality for both n^+ and p^+ contacts. However, after performing FGA process on the FSF test sample lowered the iV_{OC} with about 35 mV. This brings us to an important conclusion that the FGA process needed to improve the passivation on back side should be done before preparing the FSF passivation on the front side of the solar cell. Therefore, the Hydrogenation treatment is performed first then the FSF is applied during the fabrication of the bifacial-IBC solar cell.

Table 4.1: Passivation quality of the FSF test sample.

Parameter	Before FGA	After FGA
iV_{OC}	714 mV	679 mV
iFF	83.2%	81.7%

4.7 TCO layer (ITO) patterning test

As mentioned in section 2.1, the transparent conductive oxide (TCO) layer is used for two main reasons: first, to enhance the lateral transport of the charge carrier at the poly-SiO_X/metal interface. Second, to be used as anti-reflection coating (ARC) layer for better light capturing at the solar cell rear side. The optimization of this layer is important to maximize the solar cell performance. This is done by increasing the transparency of the TCO layer through modifying the reflective index and enhance its conductivity by

increasing the charge carrier conductivity [81]. However, the optimization of this layer is outside the scoop of this project. The main goal of this section is to check the working mechanism of TCO layer pattering using Hydrochloric Acid (HCL) to see if it's compatible with lithography process of the bifacial IBC cell flowchart. Therefore, the test is performed as follow: first, a 120 nm ITO layer thickness is deposited on a silicon wafer using Zorro sputtering machine. Then, the test sample was covered by photoresist and immersed in HCL acid at different concentration until the ITO layer is completely etched away. The test results are presented in table 4.2. The test worked as expected and the etching rate for each agent concentration was found visible as the lithography process. It is noticed the etching at 30% was much uniform with a relatively high etching rate, thus it is used during the solar cell fabrication.

Table 4.2: ITO layer etching test.

HCl (%)	**Etch time (min:sec)**	**Etch rate (A/s)**
36	01:05	18.5
30	**02:00**	**10**
25	03:30	5.7
20	47:00	0.4

4.8 Solar cell results

A demonstration proof of this cell concept is obtained using above presented flow chart. Figure 4.9 shows the images captured in the lab on both the front and rear sides of the solar cell to give a clear view of the final bifacial-IBC solar cell structure.

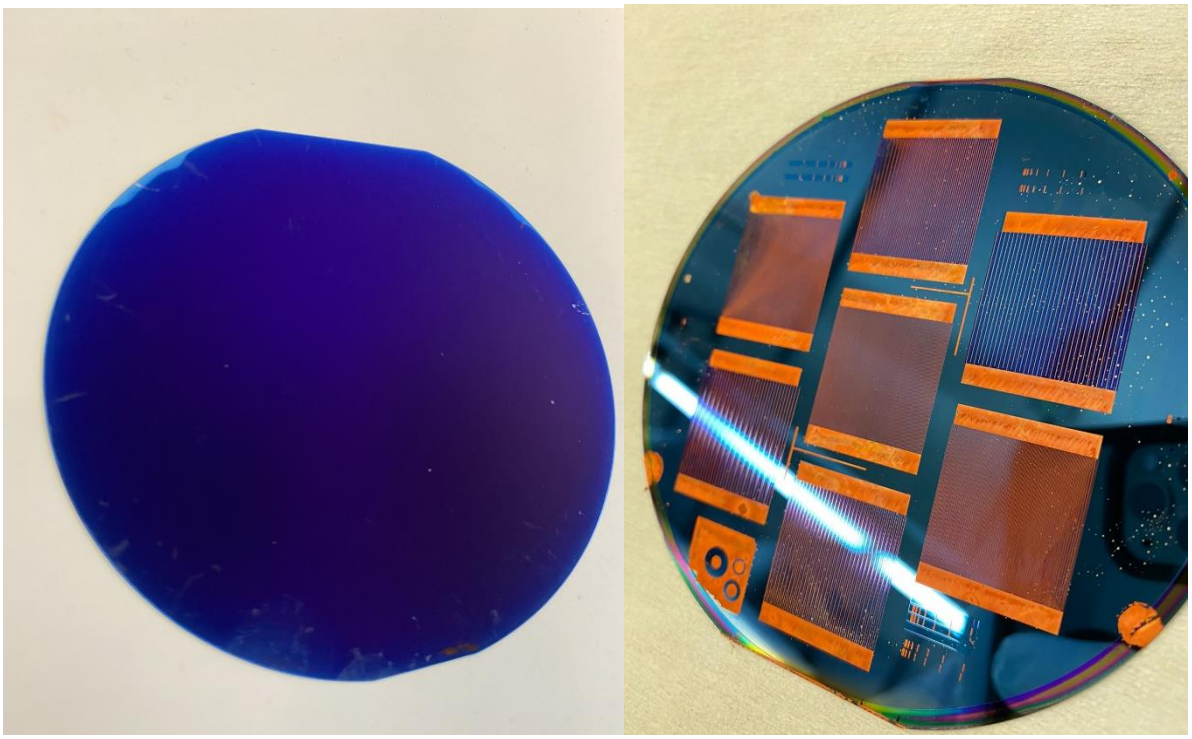

Figure 4.9: Cu plated Bifacial-IBC solar cell enabled by poly-SiO_X passivating contact: (a) front side. (b) rear side.

As shown above, a successful proof of concept cell is obtained using this fabrication process. This section discusses the results of the bifacial-IBC solar cell enabled by poly-SiO_X carrier selective passivating contact. Unfortunately, the solar cell fabrication was successful for only 2 cells after performing the metallization stage. This can be attributed to the very poor adhesion of the copper metal fingers on the cell flat rear surface. The results of the functioning solar cells are presented in table 4.3.

Table 4.3: Results of the poly-SiO_X passivating contacts bifacial-IBC solar cells.

Parameter	V_{OC} **[mV]**	J_{SC} **[mA/cm²]**	R_{sh} **[ohm·m²]**	**FF [%]**	**Efficiency [%]**
Solar cell 1	619	37.6	9.0	42.0	9.8
Solar cell 2	649	40.7	32.6	44.3	12.0

Results in table 4.3, recorded for the best cell performances after the measurement, show a high current density but a low open circuit voltage values with 40.7 [mA/cm^2] and 649 [mV], respectively. As is shown in table 4.3, we notice that a very low FF and R_{shunt} are obtained. These low values proof that a significant shunt path exist in the solar cell [82]. Therefore, SEM images are taken for the flat rear side and the cross-section near the finger gap of the bifacial solar cell, which are shown in figure 4.10.

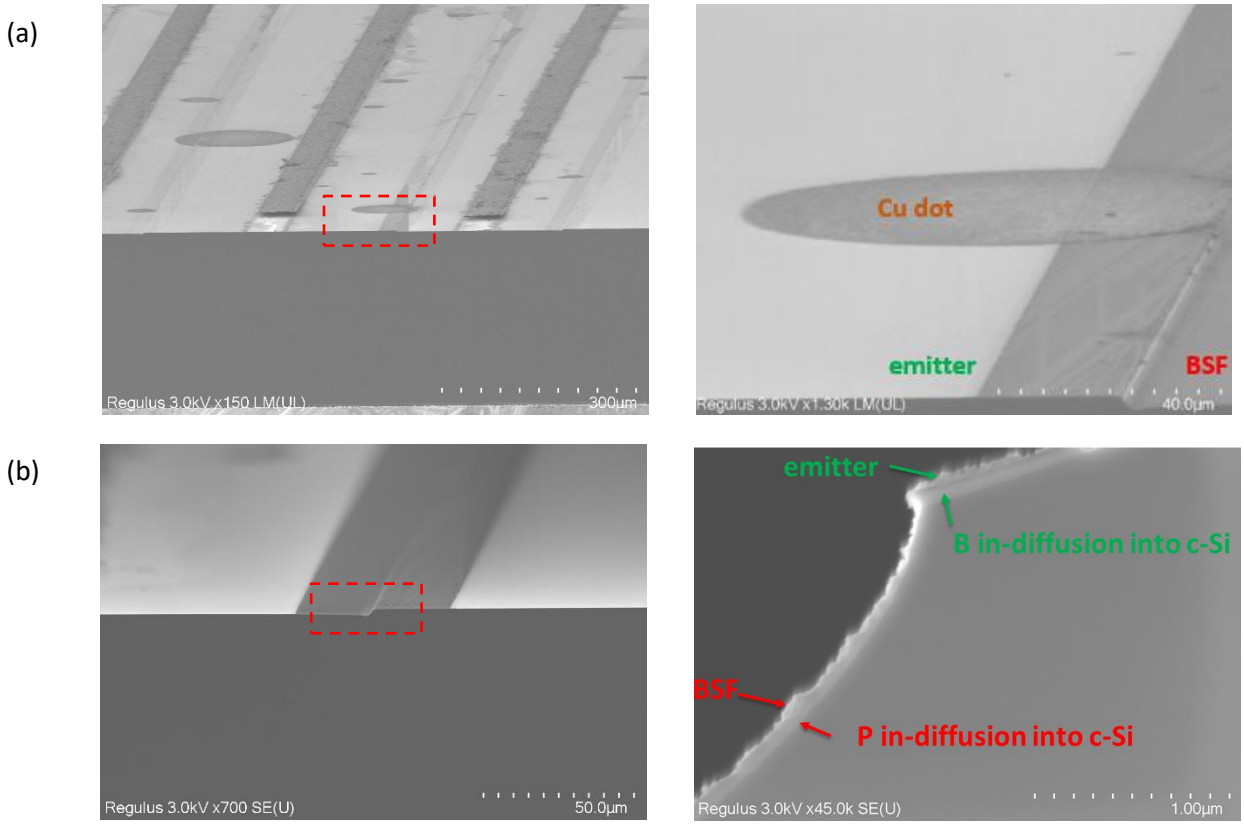

Figure 4.10: SEM images after Copper plating step. (a) shows the growth of Cu dots on the back surface. (b) indicates the unsuccessful poly-SiO_X contacts separation.

Figure 4.10(a) shows the growth of unwanted Copper spots on the cell rear side which were already noticeable on the wafer rear side surface in figure 4.9 (b). These spots formation is called as the background plating effect. The possible physical reason of this effect is current leakage at these points during Cu plating, thus the plating current can induce some copper growth in these undesired areas [76]. These Cu spots connects the poly-SiO_X/TCO regions of emitter and BSF fingers resulting in a shunt path. Therefore, the existence of this Cu particles, despite that the solar cell still work, results in a low FF and V_{OC}. Thus, it decreases the overall bifacial-IBC solar cell performance.

In order to avoid this problem, the so-called pulse plating can be implied, which consists of applying, for a certain period, forward bias (growing copper) and for a shorter time reverse bias (depleting copper to remove the undesired spots) [83]. The process is performed in a cycle, so in this way, we plate and de-plate in the unwanted regions. It is worth to note that during the reverse bias a small part of the material is removed in the conductive regions (seed layers) but this does not affect the process.

Figure 4.10(b) shows SEM images of the contacts on the rear side. We believe that the second reason for the cell low FF value is that the separation of the p^+ and n^+ contact regions was not successful, which results in a serious shunting path. This may be attributed to the non-enough etching process to form a large enough cantilever [84] at the gap between rear BSF and emitter contacts. In other words, the time

used for etching back by poly-etch (HF and HNO_3 mixture) were not long enough to form the deep step between the emitter and the BSF regions. Therefore, to ensure a complete separation of the rear contacts more etching time and concentration should be tested.

Finally, it worth to note that the results presented in table 4.3 are only from solar cells illuminated from the solar cell front side. Therefore, to measure the bifacial-IBC solar cell overall performance the illumination on the rear side should be considered as well. Unfortunately, the measurement of the solar cell performance from rear side is not executed due to the poor adhesion of the copper metal fingers to the cell flat surface. It is noticed that, after performing the measurements on front side, some busbars were scratched, and others were peeled off. Thus, to eliminate the poor adhesion problem different factors should be studied. First, same concept can be applied with replacing the flat surface with textured one to fabricate the double side textured bifacial-IBC solar cells. Next, the use of different metal seed layers, for example, Ni, at different thicknesses must be investigated. Finally, the use of a thin poly-Si contacts surface morphology can be studied to see if it gives a better adhesion feature. In conclusion, there is a large room for improvement of the bifacial-IBC solar cell overall performance using this concept.

4.9 Conclusion

In this chapter, we discussed the proposed flowchart for fabricating bifacial IBC solar cells with in-situ doped PECVD poly-SiO_x passivating contacts. According to the flow chart, the optimization of the passivation quality of the used in-situ poly-SiO_X carrier selective passivating contacts was performed.

The deposition of the buffer layer using PECVD results in a massive blister effect. To eliminate the blister formation, the effect of the deposited intrinsic layer thickness and the SiN_X layer deposition temperature is studied. Results show a less blister effect with decreasing the intrinsic layer thickness and the SiN_X layer deposition temperature. However, the blister still brings a significant reduction in the passivation quality.

Second, the intrinsic PECVD layer was replaced with LPCVD deposition method, fortunately the blistering is no longer exist. The optimization the doped (p^+) and (n^+) poly-SiO_X layer thickness was performed for symmetrical test samples. Results show that the highest iV_{oc} were found for a 25 nm thick (p^+) poly-SiOx layer and a 40 nm thick (n^+) poly-SiO*x* layer. This is followed by hydrogenation process. As a consequence, the best symmetrical polished p^+ and n^+ poly-SiO_X sample passivation quality has an implied V_{OC} of 714 mV and 730 mV, respectively.

Later, the effect of rear hydrogenation process on the FSF passivation quality is investigated. Results show that after performing FGA process on the FSF test sample lowered the iV_{OC} with about 35 mV. Therefore, it is concluded that the crucial hydrogenation treatment to improve the passivation at the rear side must be applied before FSF preparation. Additionally, an etching test for the ITO layer is performed to check the working mechanism of TCO layer pattering using Hydrochloric Acid (HCL) to see if is compatible with lithography process. The best etching agent was found using 30% HCL concentration resulting in much uniform surface.

Next, the fabrication of the bifacial-IBC solar cell is applied as follow. First, the growth of thin tunnel oxide layer about 1.5 nm is formed chemically by NAOS. Next, a 10 nm interlayer layer thickness is deposited

via LPCVD and PECVD deposition process for the p^+ and n^+, respectively. Subsequently, the doped layers are deposited through PECVD with thickness of 25 nm and 40 nm to form the p^+ an n^+ contacts, respectively. Further, the texturing and an implantation steps are implemented using Varian ion implanter E500HP, 10 keV and $1e^{14}$ implantation energy and dosage, to form a lightly doped FSF layer on the cell front side. The entire structure is annealed in one step using a high temperature annealing process at 850°C for 53 min. Next step is the hydrogenation process that is done by depositing a 75 nm SiN_X layer using PECVD method on the rear side followed by a forming gas annealing which carried out at constant temperature of 400°C for 30 minutes. Further, an 80 nm ITO layer thickness is deposited on a silicon wafer using Zorro sputtering machine on the wafer rear side. Finally, the cell is immersed in the copper plating bath to form the metal fingers with about 15µm.

Finally, a demonstration proof of this cell concept is obtained using in-situ poly-SiO_X CSPC flow chart. The best cell performance parameters were Voc of 649 mV, FF of 44,3 %, J_{SC} of 40,7 mA/cm^2, and efficiency of 12 %. A very low FF values are obtained due to a significant shunt path in the solar cell. The cross-section SEM images shows two probable shunt paths. First, the growth of unwanted Cu spots on the cell rear side after copper plating process which connects the poly-SiO_X/TCO regions resulting in a shunt path. Second, the separation of the p^+ and n^+ contact regions was not successful causing a serious shunting path.

5 Conclusions and Outlook

The main goal of this project was to fabricate proof of concept bifacial IBC solar cells with poly-SiOx passivating contacts. The project including tasks on the optimization of the poly-SiO_X passivating contacts according to the proposed cell process flowchart. This chapter summarizes the key findings of the completed work. Finally, suggestions for further development on this research topic are also given.

5.1 Conclusions

In this project, we proposed two process flowcharts for bifacial IBC solar cell fabrication. The first process flow is the ion-implanted bifacial-IBC solar cell flow chart. It is showed that using this flow chart may make the entire fabrication process easy and safe as it reduces the fabrication steps and avoid the use of the heavy chemicals. Besides, when it comes to industrial manufacturing, it is more cost-effective to keep the number of used machined to a minimum. The second used flow chart was designed to use in-situ doped poly-SiO_X, which is much complicated owning to extra process steps compared with the first flow chart. Therefore, the main aim was to use PECVD deposition method to form the contacts as it allows for the deposition of the inter and doped layers in the same device, resulting in a more cost-effective and efficient industrial process.

In Chapter 3, for the first process flow, we tested the optimization of the PECVD intrinsic a-SiOx:H layer thickness using different annealing levels is examined. The best passivation results obtained from this approach was 646 mV with 30 nm layer thickness and 623 mV with 75 nm layer thickness for the n^+ and p^+ layer, respectively at 850/60min giving the best annealing conditions. Next, the best hydrogenation configuration was applied. Unfortunately, the passivation quality for both the n^+ and p^+ was not as expected and the passivation was not sufficient. The further passivation optimization could not be pursued owing to a limitation in the implanter range used in the EKL lab and the machine maintenance/down time. Thus, future work should be applied to further optimize the passivation using this concept with variable parameters of the Varian ion implanter E500HP.Therefore, it was decided to follow the already developed IBC solar cell flow chart used at PVMD group.

For the second process flow, two intrinsic layer deposition methods are investigated namely PECVD and LPCVD to achieve the best passivation quality. The deposition of the PECVD buffer layer, leads to a significant blister formation on the wafer surface. The blister effect test showed a lower blister formation with reducing the intrinsic layer thickness and the deposition temperature of the SiN_X layer. Nevertheless, the blister still brings a major decrease in the passivation quality. The maximum achieved iV_{OC} value was 575 mV. Therefore, it was decided to use LPCVD deposition method of the intrinsic layer to test the p^+ passivation performance and the blister effect in no longer an issue. Future tests should be applied to eliminate the blister formation.

The thickness of doped p^+ and n^+ poly-SiO_X layers was then optimized for symmetrical test samples. According to the previous optimization for the p^+ and n^+, a 10 nm interlayer layer thickness is deposited via LPCVD and PECVD deposition processes. As a consequence, a 25 nm thick p^+ poly-SiOx layer and a 40 nm thick n^+ poly-SiOx layer recorded highest implied Voc performance. The hydrogenation process was

again studied in order to increase the passivation efficiency even further. Combining a thin 75nm SiN_X layer deposited by PECVD followed by a direct forming gas annealing process in the tube furnace for 30 minutes at 400°C yields the best hydrogenation results. As a result, the implied V_{OC} for the best symmetrical p^+ and n^+ poly-SiO_X sample passivation value were 714 mV and 730 mV, respectively.

Next, test on the FSF passivation quality is performed to examine the effect of the hydrogenation process. Results show a reduction in the passivation quality with about 35mV of the FSF test sample after performing the hydrogenation treatment. Therefore, it is decided to apply first the crucial hydrogenation treatment, to improve the passivation at the rear side, then the FSF should be prepared. Additionally, other test on the ITO layer is applied to test if pattering the TCO layer using HCL is compatible with lithography process. Results demonstrate that the best etching agent was found using 30% HCL concentration resulting in much uniform surface.

Finally, the findings of the optimized poly-SiO_X passivation contacts are used to fabricate the bifacial-IBC solar cell. As a result, using an in-situ poly-SiO_X CSPC flow chart, a demonstration proof of this cell principle is obtained with V_{OC} of 649 mV, FF of 44,3%, J_{SC} of 40,7 mA/cm2, and efficiency of 12% for the best solar cell. Due to a significant shunt path in the solar cell, very low FF values are obtained. SEM images show two probable shunt paths causes. First, after the copper plating procedure, unwanted Cu spots appear on the cell back side, connecting the poly-SiO_X/TCO regions and forming a shunting path. Second, the miscarried isolation step of the p^+ and n^+ interaction regions, resulting in a major shunting region.

5.2 Outlook

Even with the progress made in this master thesis project, there is still space for improvement. Poly-SiOx passivating contact layer research could lead to higher performance bifacial-IBC solar cells. This section briefly addresses potential strategies for further enhancing the parameters of cells with poly-SiOx passivating contacts.

On the fabrication process flow

The ion-implanted bifacial-IBC solar cell flow chart was first presented. This optimistic flow chart was not used in this project due to insufficient passivation quality owed to the limitation in the implanter energy range and to the long maintenance time. Thus, future work should be applied to further optimize the passivation using this concept with variable parameters of the Varian ion implanter E500HP.

The second used flow chart was designed to use in-situ doped poly-SiO_X, which is much complicated owning to extra process steps compared with the first flow chart. Therefore, the main aim was to use PECVD deposition method to form the contacts as it allows for the deposition of the inter and doped layers in the same device. However, the blister formation at the p^+ contact force us to switch to LPCVD for the interlayer deposition which add extra physical and chemical steps to fabricate the solar cell. Therefore, more tests should be executed to eliminate the blister effect which simplify the entire process and reduce the number of the used solar cell fabrication steps.

On the solar cell FF

The metallization process used during the thesis work was copper electroplating method. It is applied as copper provide a cheap and relatively good conductive alternative material with high aspect ratio which can enhance the FF value of the solar cell, while minimizing the reflective loss when illuminating from the rear [77]. However, the measured solar cells showed a very low FF values owing to serious shunting path in the solar cells. SEM images show two probable shunt reasons namely the background plating effect and the unsuccessful separation between doped regions for BSF and emitter. Therefore, further research and tests should be conducted to solve these issues. There are two possible ways may be implemented to solve the background plating effect issues reported in a previous work of the PVMD group [83]. It is suggested the use of pulse plating and a thicker dielectric layer may overcome the undesirable background plating. Additionally, more etching tests should be performed to find an efficient etching agent with certain concentration to ensure a complete separation of the rear contacts.

On the adhesion issue of copper fingers

The main drawback of the copper plating in this work is that the cupper plated contacts suffer from adhesion problems. The adhesion issue may be related to the poor adhesion of either the seed layer to Si or the Cu to the seed layer. In this research, a stack of Al and Ag layers are used as seed layer, however an overall poor adhesion of the Al/Ag/Cu metal fingers is obtained on the cell flat surface. The adhesion problem still existed for Al even for the cells with relatively good adhesion. It is observed that some busbars had been scratched, while others had been peeled away. Therefore, various factors should be explored in future work to eliminate the poor adhesion issue. As a strong suggestion, the same principle can be used to fabricate a bifacial-IBC solar cell by replacing the flat surface with a textured one. Next, the use of various metal seed layers such as Ni or Ti of various thicknesses can then be examined. Finally, the use of textured metal oxide as a TCO layer, such as ZnO which can benefit from its nano-porous structure which allows plated Cu has a better mechanical bonding [85].To conclude, the overall efficiency of the bifacial-IBC solar cell can be further improved through testing these presented solutions.

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