The read-out circuit for a novel 3-D Hall magnetic sensor

by

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Abstract

Magnetic sensors play a crucial role in various fields. The 3-D magnetic field sensing capability is becoming increasingly important in applications such as navigation, position detection and consumer electronics. The final goal of this work is to design an analog front-end circuit to read out a novel 3-axis Hall magnetic sensor at the transistor level. The design of the IC front-end is an extension of the PCB characterization of the Hall sensor. In this work, a PCB (printed circuit board) is designed first for the characterization of the sensor. The measured specs are used for the IC front-end design. Finally, this current spinning read-out system achieves a residual offset of 1 mT and a dynamic range of 58 dB.

Contents

1

Introduction

Magnetic sensors have assisted mankind in the analysis and control of thousands of functions for many decades. The ability to accurately sense three-dimensional magnetic fields enables position sensing [1], system inspection[2], navigation[3], and bio-magnetic [4] measurements. The most prevalent types of microelectronic magnetic sensors are magnetoresistive (xMR), micro-electromechanical systems (MEMS) and Hall effect sensors. As shown in Figure 1.1, Hall sensors are more competitive in magnetic field ranging from several millitesla to hundreds of millitesla, which is larger than those of most other magnetic sensors.[5] Though xMR sensors have similar properties in this range, they are not as cheap and easy to fabricate as Hall sensors[6]. These factors make 3-D Hall magnetic sensors a suitable choice in certain application fields, such as consumer electronics and navigation. Various structures have been developed for 3-D Hall sensors, including integrated or discrete ones. Some typical examples are discussed in the following parts.

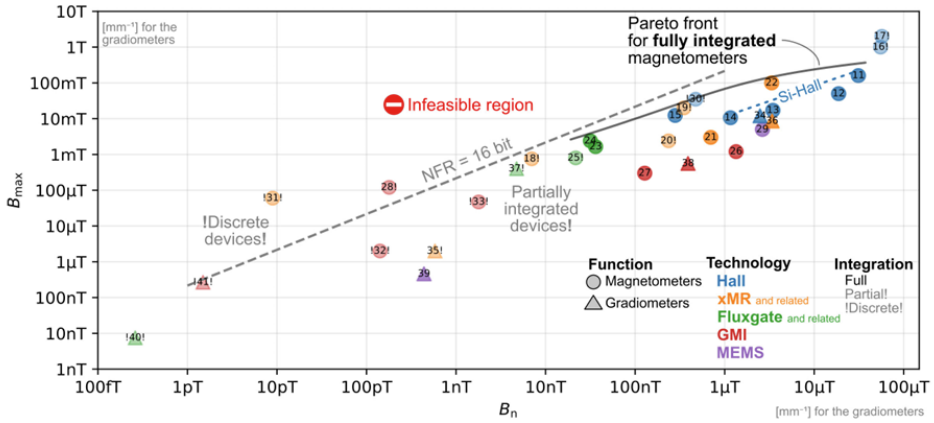


Figure 1.1: Trade-off curve of magnetic sensors. Maximum full-scale field vs noise (in 500 Hz bandwidth) [5]

1.1. Existing 3-D Hall magnetic sensors

Three-dimensional (3-D) Hall magnetic sensors have vast application potential due to their ability to measure magnetic fields in all spatial directions with high precision. Unlike traditional single-axis Hall

sensors, 3-D Hall sensors provide complete vector information of all 3 axis, enabling more accurate position, orientation, and motion detection. They are increasingly used in automotive systems for gear and pedal sensing, in industrial automation for contactless control, and in consumer electronics for gesture recognition and navigation[5]. As devices continue to demand higher integration and smarter sensing capabilities, 3-D Hall magnetic sensors will play an essential role in advancing next-generation sensing technologies.

One of the most conventional ways to achieve 3-D sensing is to combine horizontal and vertical Hall sensors, enabling simultaneous sensing of in-plane and out-of-plane fields. Pascal et al. proposed a CMOS integrated Hall probe, in which two vertical Hall devices (VHD) are sensitive to the components of the magnetic field oriented in the plane of the chip and a horizontal Hall device (HHD) is sensitive to the component of the magnetic field orthogonally oriented to the plane of the chip. [7]. This is a typical structure of 3-D magnetic field sensing utilizing separate Hall devices. In the work mentioned above, the vertical Hall device is chosen from [8], which is shown in Figure 1.2. This sensor is designed in the shallow N-well of a low cost 0.35 µm standard CMOS technology, with its contacts located outside the sensor active area.

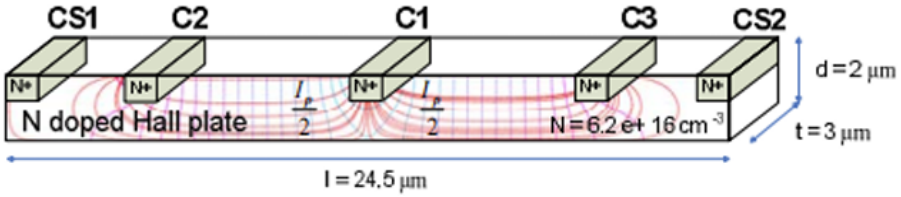


Figure 1.2: Vertical Hall device used in [8]

Although the sensor shown in Figure 1.2 represents a relatively inexpensive and simple solution for 3-D field sensing, it has several drawbacks. First, they suffer from relatively large offsets. Secondly, due to limited active area depth of vertical Hall devices in the CMOS process, their flicker noise increases while the sensitivity decreases.[9]

Zhang et al. proposed a 3D Hall sensor that used lateral combined with vertical Hall devices, and made great progress in the sensitivity compared with earlier PHD and VHD combinations.[10]. The Hall device is fabricated on 0.15 µm bipolar-CMOS-DMOS (BCD) platform, which is shown in Figure 1.3. The lateral Hall device used in the work is octagon shaped, and the vertical Hall device has the same geometry as the VHD used by Pascal et al. By optimizing the position of the Hall electrodes and the width of the device, the current-related sensitivity of the vertical Hall device, which defines the Hall voltage generated by 1 A current in 1 T magnetic field, reaches 161 V/A/T, which is much higher than its typical counterparts. However, due to its high input resistance (10 $k\Omega$), the voltage-related sensitivity, which is the Hall voltage generated by 1 V biasing voltage in 1 T field, is much lower than conventional PHD + VHD sensors (15 mV/V/T). This work mainly focuses on demonstrating the cost-efficient feasibility of fabricating high-performance Hall sensor chips using a 0.15 µm BCD platform. However, the optimized device size can be as large as 110 µm, considering it is supposed to be integrated with CMOS circuits, the area of the Hall device is in fact limited.

To find a balance among device size, cost and performance, efforts are made on single-device 3-D Hall sensors. Many single-device 3-D Hall magnetic sensors are introduced.

A proposed structure by Schott et al. in 2000 is a planar, eight-contact 3-axis Hall effect sensor. [11],

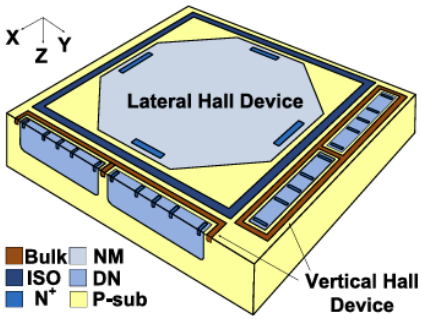


Figure 1.3: PHD+VHD 3D Hall sensor with improved sensitivity[10]

which is shown in Figure 1.4. The sensor mainly consists of a square bulk of low n-doped silicon

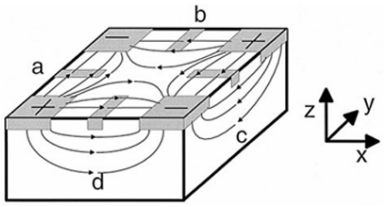


Figure 1.4: 3-axis planar Hall Sensor[11]

substrate with eight n+ electrodes at the surface forming a square structure. It uses the magnetic flux in 3-axis to generate voltage at each contacts that contains the information of different directions. By subtracting voltages of these contacts, the signals of different field component can be extracted. The in-plane and out-of-plane sensitivity of this device are 50-830 V/A/T and 17-900 V/A/T varying with the increasing active zone area, which is up to 500 µm by 500 µm.

When not applying external field, Hall sensors produce a voltage that is defined as its offset. To reduce this offset, the current spinning technique is introduced, which will be elaborated in details in later sections. It should be noted that all the sensors discussed above are not current spun. This fact limits their offset performance.

One single 3-D Hall device that can be current-spun is proposed by Sander et al., which uses a single hexagonal structure, shown in Figure 1.5.[9] This sensor features high isotropy, meaning that it is able to measure three orthogonal components of magnetic field with equal sensitivities and similar offsets. It performs 3-D field sensing by sending currents obliquely across the device , which allows it operates as three mutually crossing, identical, and effectively orthogonal Hall sensors. This sensor exhibits high isotropy also in the offsets of each axis. However, this hexagonal device still suffers from large size which is over 500 µm.

A more recent work of 3-D Hall sensor is proposed by Q. Wang et al. [12]. In this work, a 3-D GaAs-based Hall sensor with a dual active structure, which can be fabricated only by a planar process is proposed. The primary structure, comprises a low-resistance GaAs layer, an isolation layer, and an N-doped GaAs epitaxial layer from bottom to top, as shown in Figure 1.6. This structure improves sensitivity in vertical magnetic field direction. However, the cost is its large volume of hundreds of µms and there are no characterization of its offset in the proposed work.

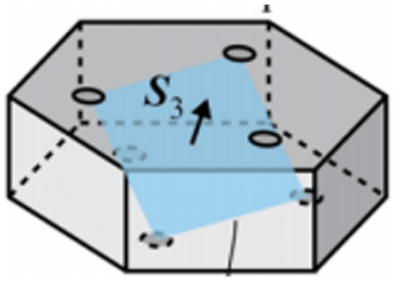


Figure 1.5: Hexagonal isotropic 3-D Hall Sensor[9]

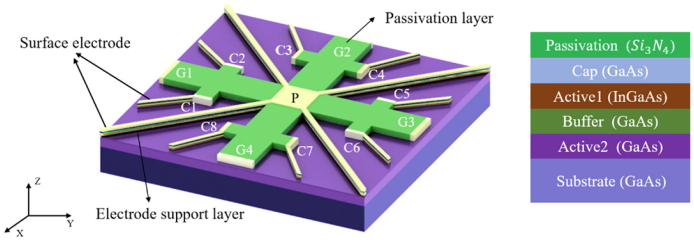


Figure 1.6: 3-D GaAs based Hall sensor[12]

A competitive 3-D IMC (integrated magnetic concentrator) sensor with current spinning is proposed by C Schott et al[3] which combines a magnetic concentrator and Hall elements. The IMC is a thin soft ferromagnetic layer, which is structured onto the silicon surface as shown in figure 1.8. It locally rotates and amplifies the external in-plane magnetic field, so that it can be measured by conventional Hall devices. The whole structure is shown in figure 1.7. This configuration present the high sensitivity

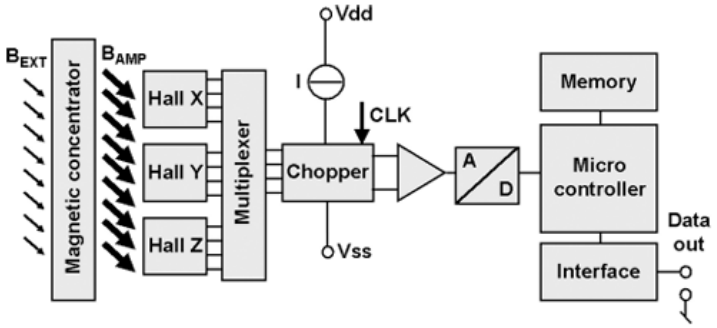


Figure 1.7: Architecture of the IMC + Hall sensor[3]

and low offset typical of Hall plates, and it can be integrated in a CMOS process. However, these devices may exhibit hysteresis issues, higher temperature drifts, and saturation at high magnetic fields due to the use of ferromagnetic materials. In addition, this sensor is inherently anisotropic[3]. Lastly, J. Ruggeri et al. proposed a novel 3-D Hall magnetic sensor structure which achieves relatively high sensitivity for both in-plane and out-of-plane magnetic fields[13]. The sensor is an eight-contact inverted pyramid with four contacts positioned at the corner of the base, while the remaining four are located at the midpoint of each side, as shown in Figure 1.9. The pyramid sensor achieves 64-82 V/A/T current sensitivity for in-plane field, and 95-198 V/A/T for out-of-plane field. This is not high value compared to the sensors mentioned earlier, but considering its smaller size and simpler realization, it has reached a balance point of performance and size. Another notable feature of this novel sensor is that it is proved that the offset of this sensor can be greatly reduced by current spinning in the proposed work. That

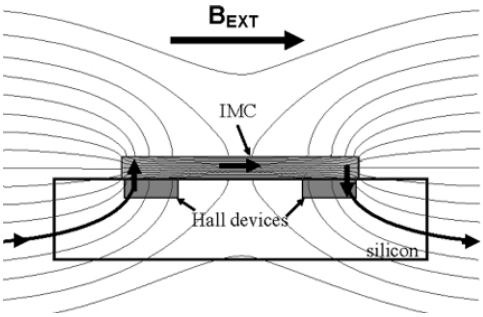


Figure 1.8: IMC working principle[3]

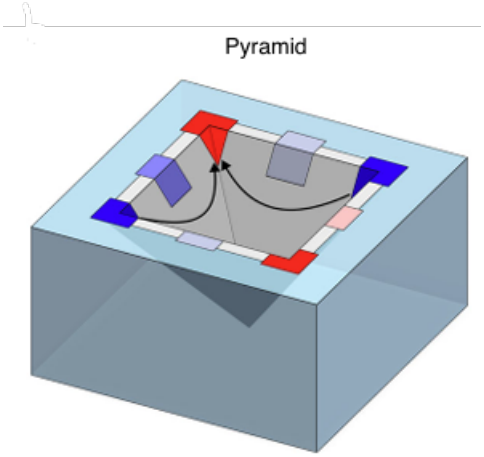


Figure 1.9: Pyramid Hall sensor[13]

also effectively improves the noise performance of the device. The pyramid 3-D Hall sensor represents a promising and simpler alternative to existing 3-D magnetic sensors, offering a viable solution for precise and reliable magnetic field sensing. The detailed working principle of offset cancellation will be discussed in the later sections.

Table 1.1 shows the comparison of the pyramid 3-D Hall sensor with the state-of-the-arts.

Table 1.1: Comparison of the pyramid Hall sensor with the state-of-the art

Sensor	S_i(V/A/T)		S_v(mV/V/T)		Residual offset(mT)	Spatial resolution(µm)
	XY	Z	XY	Z		
PHD+VHD[7]	6.4	90.1	1.9	27.3	-	44
PHD+VHD[10]	161	378	-	-	-	110
3-axis planar[11]	46-827	17-909	20-54	20-33	-	50-500
Hexagonal[9]	8.6-8.8	8.7	33.0-33.9	33.3	0.04	850
Dual active 3-D	700	1005	10	46	-	360
Pyramid[13]	64.1-82.2	94.8-198	14.8-17.1	19.6-21.4	0.2-4	50
IMC Hall[3]	1500	250	300	50	-	2000

This thesis project focuses on the characterization of the pyramid sensor and the design of an analog front-end circuit to read out the current-spun signals from the sensor as depicted in the red dash line area of figure 1.10

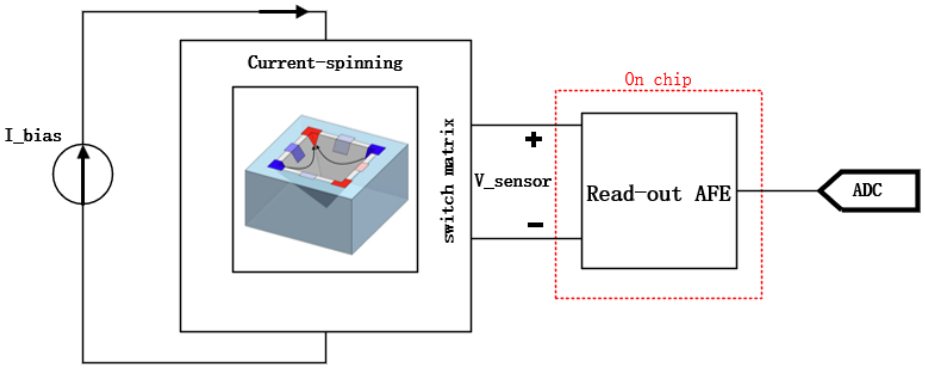


Figure 1.10: Block diagram of the project

1.2. Thesis organization

The remainder of the thesis is organized as follows: chapter 2 gives the theory background of Hall effect magnetic sensing, Hall offset cancellation and pyramid Hall sensor's working principle. chapter 3 describes the procedure of the characterization of the pyramid sensor using a PCB (print-circuit-board) system and shows the test result: offset, noise and sensitivity. chapter 4 steps into transistor level design of the read-out circuit for the pyramid sensor in Cadence Virtuoso. The design exploits the specifications measured in chapter 3, and derives the requirements of the read-out system from these specs. An architecture from existing read-out circuits is selected for the pyramid sensor. Then the design considerations and final implementations of each circuit block are discussed. Then, chapter 5 presents the simulation result of the read-out circuit and discusses the improvements that can be made. Chapter 6 gives the conclusion and future works.

2

Theory Background

This chapter establishes the theoretical foundation required to interpret the operation, performance limitations, and signal characteristics of Hall sensors. It begins with an overview of the Hall effect and its governing equations, followed by an analysis of the offset mechanisms that significantly influence sensor accuracy. The discussion then introduces the current spinning technique, an effective method for offset reduction and noise suppression. Finally, the pyramid Hall sensor concept is presented, providing insight into its geometry, sensing mechanism, and the offset cancellation schemes.

2.1. Hall Effect Magnetic Sensing

The Hall effect is a fundamental physical phenomenon describing the emergence of a transverse voltage across a current-carrying conductor or semiconductor placed in a perpendicular magnetic field. When an electric current I flows through a conductive plate of thickness t under a magnetic flux density B, the charge carriers experience a Lorentz force $\mathbf{F} = q(\mathbf{v} \times \mathbf{B})$, where q is the charge of the carrier and v is the instantaneous drift velocity vector of the moving carrier. This force drives them to one side of the material as shown in Figure 2.1.

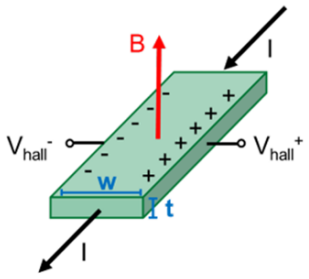


Figure 2.1: Hall effect[14]

This redistribution of charge establishes an electric field E_H across the plate, leading to the measurable Hall voltage expressed in 2.1.

$$V_H = \frac{IB}{nqt} \tag{2.1}$$

where n is the carrier concentration and q is the elementary charge. The proportionality constant $R_H = \frac{1}{nq}$ is referred to as the Hall coefficient, which characterizes the sensitivity of the material to magnetic fields and depends on the type and density of charge carriers. In semiconductors, where the carrier density is relatively low, the resulting Hall voltage is significantly higher than that in metals, making them particularly suitable for magnetic sensing applications. Furthermore, the polarity of the Hall voltage provides information about the dominant carrier type (electrons or holes). This theoretical foundation forms the basis of Hall effect magnetic sensors, which enable the precise conversion of magnetic field variations into electrical signals for subsequent signal processing and measurement. For convenience during sensor characterization and circuit design, the expression below is often used instead of Eq(2.1), where S stands for the combination of n q and t:

$$V_H = S\,I\,B \tag{2.2}$$

2.2. Offset of Hall magnetic sensors

2.2.1. Offset sources of Hall magnetic sensors

As mentioned in the introduction, Hall sensors usually have offset. The most dominant source of Hall sensor offset is due to geometry asymmetry. This asymmetry is provoked by lithographic inaccuracies and doping inhomogeneities. In reality, any deviation from symmetry causes the electric field and current flow to become slightly unbalanced, which produces a parasitic voltage mixed with the real Hall voltage. Some factors that cause the geometry offset are discussed as follow.

Lithographic inaccuracies

Hall sensor geometry is defined by photolithography. Any small error during this process breaks the geometric symmetry, such as: one contact slightly larger or smaller, edges not perfectly straight, misalignment between layers. The Hall voltage is usually microvolts, so even nanometer-scale geometric error can produce comparable parasitic signals.

Doping inhomogeneities

As shown by Eq.(2.1), the Hall effect depends directly on the carrier concentration. If the doping concentration is not perfectly uniform across the Hall device, the mobility, the sheet resistance, and the conductivity vary spatially. This means the current density becomes non-uniform. Some regions carry more current than others and again produces a small DC voltage even when B = 0.

As shown in Figure 2.2, as long as the sensor has two current biasing terminals and two voltage sensing terminals, it can be approximately modeled as an unbalanced resistor Wheatstone bridge. Without external magnetic field, the output voltage at the differential sensing nodes can be expressed as:

$$V_{\text{Hall,OS}} = I_{\text{Bias}} \left(\frac{2R}{4R + \Delta R} \cdot (R + \Delta R) - \frac{2R + \Delta R}{4R + \Delta R} \cdot R \right) \tag{2.3}$$

which can be approximated as:

$$V_{\text{Hall,OS}} = \frac{\Delta R}{4}\, I_{\text{bias}} \tag{2.4}$$

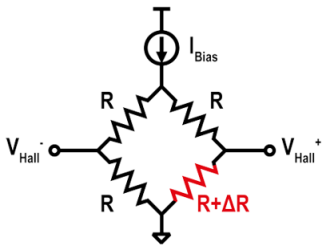


Figure 2.2: Asymmetric Hall sensor model

For the pyramid used in this work, the equivalent magnetic offset with a biasing current of 200 µA can be up to hundreds of mTs respectively for Z-field sensing mode and XY-field sensing mode[13]. According to J.Ruggeri et al., the large offset of the pyramid Hall sensor is related to the patterning and implantation during its fabrication[13].For most applications, this is a very large equivalent input signal, for example, the magnetic compass[15] that detects the earth magnetic field of µTs and positioning system in joysticks[16] that operates in mTs. Therefore, the pyramid Hall sensor cannot be used alone without any offset reduction method.

2.2.2. The cancellation of geometry offset

The most commonly used offset cancellation technique for Hall sensors is the current spinning technique introduced by Munter.[17] The original principle of current-spinning is to periodically swapping the read-out and biasing terminals, thus up-modulating the offset or signal to a higher frequency. Then the desired signal and the offset can be separated by implementing filtering circuits. If the spinning frequency is high enough, it can also remove other low frequency interferences such as the flicker noise.

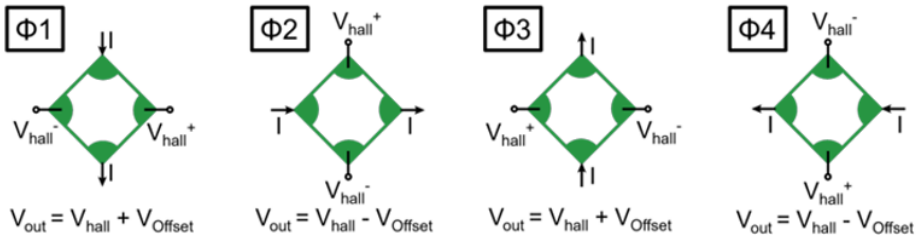


Figure 2.3: 4-phase current-spinning up-modulating the offset[14]

Figure 2.3 shows a 4-phase current spinning scheme that up-modulates the offset. The offset polarity changes at twice the spinning frequency and the Hall signal remains in the base-band.

The spinning can also be implemented the other way around, that is up-modulating the Hall signal and leaving the offset in the base-band. The modified spinning method is shown in figure 2.4. The choice between these two methods is based on circuit design considerations, which will be addressed in the later sections.

However, even if the sensor is current-spun, the offset can not be completely removed, leading to so-called residual offset. This is caused by several factors. One of the causes of the residual offset that exists in Hall sensors is the junction field effect (JFET). It refers to the modulation of the local electric field and current distribution within the Hall device due to the presence of nearby p-n junctions or depletion

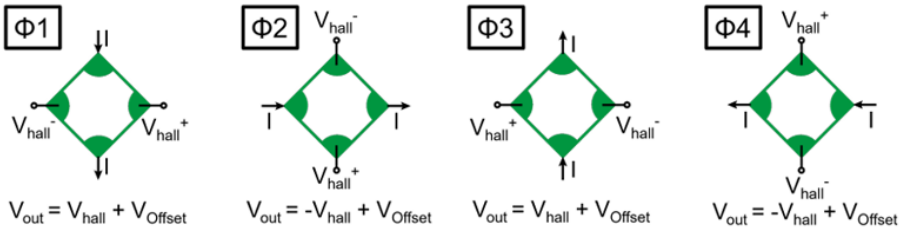


Figure 2.4: 4-phase current-spinning up-modulating Hall signal[14]

regions formed by the semiconductor's doping profile and surface potentials. In CMOS-integrated Hall sensors, the active Hall region is often surrounded by isolation wells or guard rings, creating depletion layers whose width varies with the applied bias voltage. These variations distort the originally uniform current flow through the Hall plate, leading to asymmetric potential distributions even in the absence of a magnetic field. This asymmetry manifests as an unwanted modulation of the sensor resistance.

Another cause of the residual offset is thermal effect. Due to resistance asymmetry, when biased with certain current or voltage, there will be a temperature difference in different parts of the Hall sensor. This will lead to a residual offset due to the Seebeck effect, which is described by equation 2.5.

$$V_{\mathrm{SB}} = \alpha_{\mathrm{SB}} \cdot \Delta T \tag{2.5}$$

where α_{SB} is the Seebeck coefficient and ΔT is the temperature difference between the measured two terminals.

2.3. Working principle and current spinning of the pyramid sensor

As shown in figure 1.9, the pyramid sensor active area is defined by doping the sloped sidewalls. The contact locations are defined by n+ implantations. To clearly explain the sensing principle of the pyramid sensor, we can take figure 2.5 as an example.

Three key assumptions are made: 1. The four sloped faces of the inverted pyramid are separate Hall elements, each having a same slanted angle. 2. The four devices are identical, and no mismatch due to processing is present. 3. Each device is ideal with no doping inhomogeneities or lithography inaccuracies/errors. If we push the biasing currents as the black arrows shown in figure 2.5, the Hall voltage produced between the two nodes 1 and 2 can be expressed as:

$$V_{\mathrm{H}}^{12} = S\sin(\theta)B_x + S\cos(\theta)B_z \tag{2.6}$$

In the same way, the Hall voltage between node 3 and 4 is expressed as:

$$V_{\mathrm{H}}^{34} = -S'\sin(\theta)B_x + S'\cos(\theta)B_z \tag{2.7}$$

where S represents the term $\frac{I}{nqt}$ in equation 2.1, and θ is the etching angle of the device. According to the assumptions, S is equal to S'. As a result, the voltage difference between node 1 and 4 is:

$$V_{\mathrm{H}}^{z} = 2S\cos(\theta)B_z \tag{2.8}$$

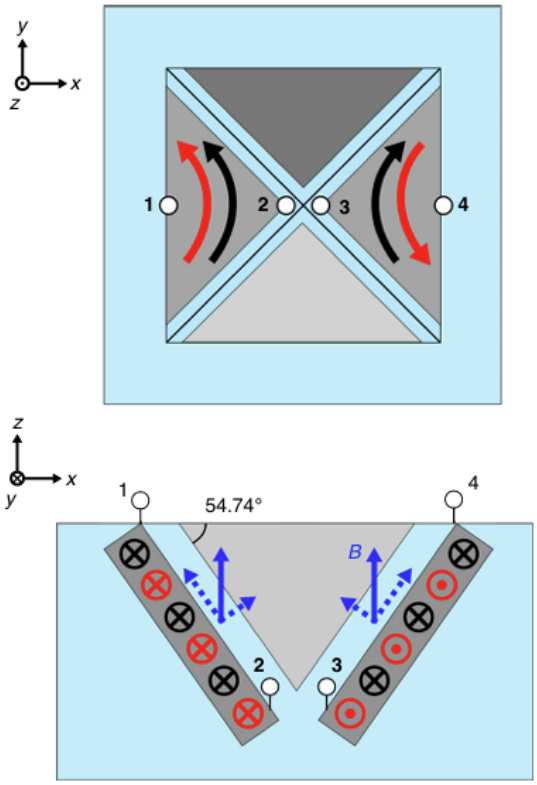


Figure 2.5: Simplified model of the pyramid device. The sensor is treated as four separated Hall plates. The black arrows represent the biasing configuration for z-field detection, while the red arrows display the biasing scheme for x-field sensing.[13]

which is the extracted Z-field induced voltage. Similarly, if we push the biasing current as the red arrows, then we can extract the X-field Hall voltage as:

$$V_{\mathrm{H}}^{x} = V_{\mathrm{H}}^{12} - V_{\mathrm{H}}^{34} = 2S\sin(\theta)B_x \tag{2.9}$$

In this way, the crosstalk between the in-plane and out-of-plane component is discarded by symmetry.

However, as mentioned in 2.2.1, the geometry offset exists because of mismatch between the four sloped faces. Therefore, the pyramid needs to be current-spun. Biasing current and sensing voltage nodes can be selected and changed in such a way that both X/Y and Z field voltage component can be extracted after a whole spinning sequence. The operation modes are depicted in figure 2.6 and table 2.1:

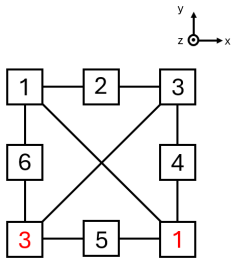


Figure 2.6: Operation mode of pyramid sensor

Phase	Input	Output
1	I_{13}	V_{46} & V_{52}
2	I_{46}	V_{31} & V_{52}
3	I_{52}	V_{31} & V_{64}
4	I_{31}	V_{64} & V_{25}
5	I_{64}	V_{13} & V_{25}
6	I_{25}	V_{13} & V_{46}

Table 2.1: Pyramid sensor current-spinning logic

Table 2.1 gives the configuration of biasing and sensing terminals of all phases in one spinning period which consists of 6 phases. The expression I_{nm} means that contact n is the positive current biasing terminal and m is the negative terminal. V_{kl} means that contact k is the positive read-out voltage and l is the negative one. Figure 2.6 shows the diagram of the contacts. The diagonal contacts are shorted with external connection wires, so they are labeled with same numbers, resulting in four anti-parallel currents as shown in figure 2.7. This configuration ensures that with the voltages measured in the six phases in table 2.1, all three axis Hall voltage can be extracted. The mechanism of sensing different axis is the same as the example in figure 2.5: If the current flows are antiparallel, the device senses the in-plane components, while when the flows are parallel, it senses the out-of-plane field. Using this principle, the magnetic signals of three directions are extracted with the combinations of these voltages and the corresponding field components listed below:

$$V_x = [V_{46}(1) + V_{31}(2) + V_{64}(4) + V_{13}(5)]/4 \tag{2.10}$$

$$V_y = [V_{52}(1) + V_{31}(3) + V_{25}(4) + V_{13}(6)]/4 \tag{2.11}$$

$$V_z = [V_{52}(2) + V_{64}(3) + V_{25}(5) + V_{46}(6)]/4 \tag{2.12}$$

where $V_{kl}(p)$ means voltage measured between contact k and l during phase p. For each component,

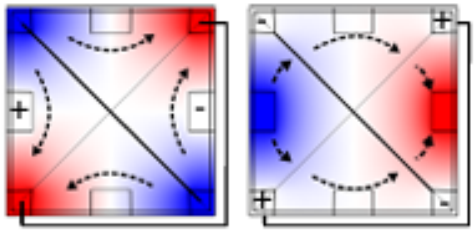


Figure 2.7: Two types of current flow with given operation mode[13]

there are only 4 contacts that are used for current-spinning, which means that it effectively operates in the same way as a standard 4-terminal Hall plate. The read-out voltages are a mixture of the Hall voltage and the offsets. They can be sent to succeeding stages, such as analog amplifiers, or stored and averaged in digital domain. Therefore, the following chapters will figure out what are the voltages generated by the current-spun sensor and how to extract the desired Hall from these voltages signal by designing a read-out circuit.

3

Pyramid Hall Sensor Characterization

Before stepping into the design of the pyramid sensor read-out circuit, it is essential to thoroughly characterize the specs of the pyramid Hall sensor. The key specs are: the raw offset of each phases during current spinning, the residual offset after current spinning, the sensitivity of in-plane and out-of-plane magnetic field, and the noise performance.

First, the pyramid samples are fabricated and wire-bonded to a small PCB carrier. Figure 3.1 shows the sensor with the carrier PCB.

Then, the noise test is performed with external wire connections and spectrum analyzer. Lastly, a larger PCB is designed to perform the current spinning to test the raw and residual offsets and the sensitivity. Table 3.1 lists the test items and the corresponding approaches.

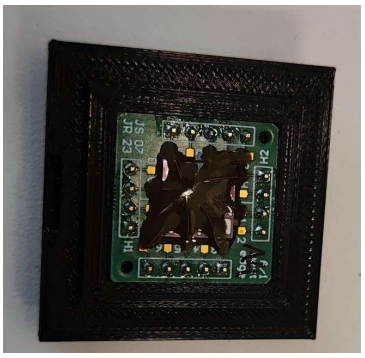


Figure 3.1: Pyramid sensor wire-bonded to a small PCB carrier

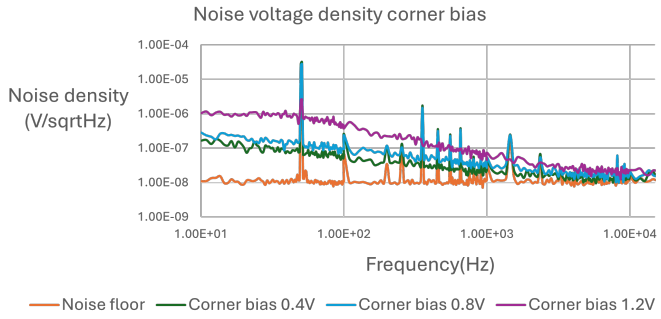
Test items	Test method
Noise performance	Spectrum analyzer + sensor
Sensitivity	Coil + sensor + PCB + laptop
Offset	Shielding chamber + sensor + PCB + laptop

Table 3.1: Test items and methods

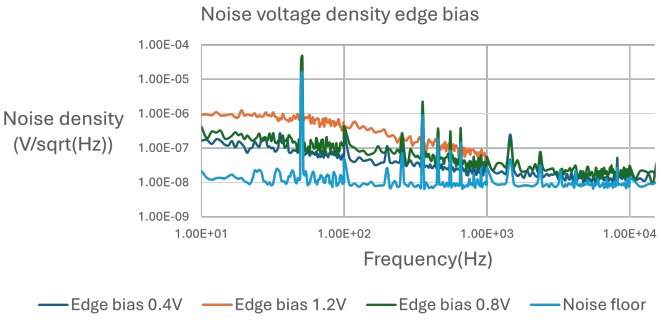
3.1. Noise and impedance characterization

3.1.1. Noise characterization

The noise floor defines the sensor's resolution, and the flicker noise corner determines the spinning frequency. Noise characterization is performed by directly connecting the pins of the sensor carrier to the spectrum analyzer for two biasing modes: corner-biasing and edge biasing (shown in figure 2.7) at three different supply voltages: 0.4 V, 0.8 V, 1.2 V and without supply. The resulting noise voltage density plots are shown in figure 3.2.



(a) Corner-biasing



(b) Edge-biasing

Figure 3.2: Noise spectral density of both biasing modes

The intersection frequency between the extrapolated flicker noise and the thermal noise floor is known as the corner frequency. A clear trend can be observed from the plots: with the biasing voltage increasing, the flicker noise corner frequency gets higher, but the noise floor remains the same. The measured noise floor and flicker noise corner for each mode and biasing voltage is shown in figure 3.2 This corresponds to the Hooge model [18]:

$$S_{vf}^2 = V_{\text{supply}}^2 \frac{\alpha_H}{N} \frac{1}{f^\gamma} \tag{3.1}$$

where S_{vf}^2 is the power spectral density of the flicker noise, V_{supply}^2 is the supply voltage, α_H is the Hooge parameter, N is the total number of carriers, and is a dimensionless factor that should be close to 1 [13]. This model explains the trend of the increasing flicker noise frequency.

		0 V	0.4 V	0.8 V	1.2 V
Corner bias (X/Y)	Noise floor	$7.42\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	-	-	-
	1/f corner	-	6.70 kHz	8.45 kHz	9.15 kHz
Edge bias (Z)	Noise floor	$9.62\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	-	-	-
	1/f corner	-	7.83 kHz	8.61 kHz	10.01 kHz

Table 3.2: Noise floor and 1/f corner of the pyramid sensor

3.1.2. Impedance characterization

The input impedance of the Hall sensor determines the response of its output when giving a step input. In other words, it decides how fast the sensor can be spun. The input DC resistance of the pyramid sensor is measured with multimeter. The input DC resistance of corner-biasing and edge-biasing are 3.3 kΩ and 5.1 kΩ respectively, which also correspond to the noise floor in table 3.2. The frequency response of the pyramid input impedance is shown in figure 3.3. According to this frequency response,

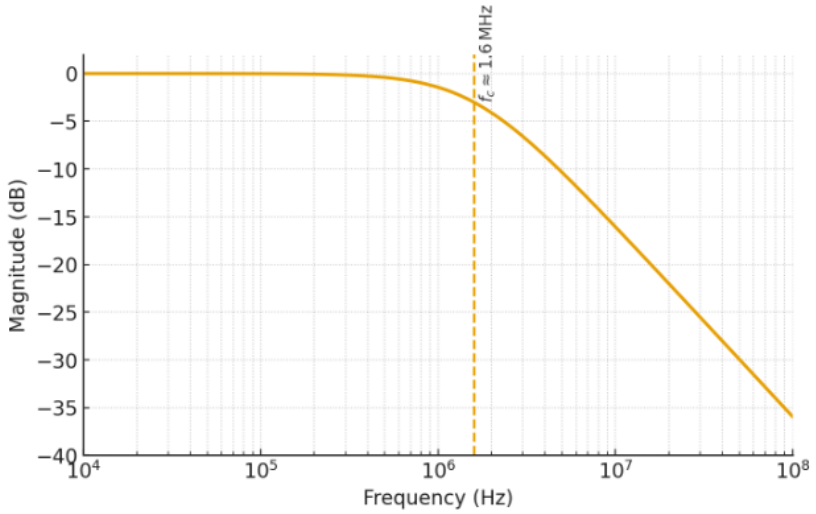


Figure 3.3: Pyramid sensor input impedance frequency response

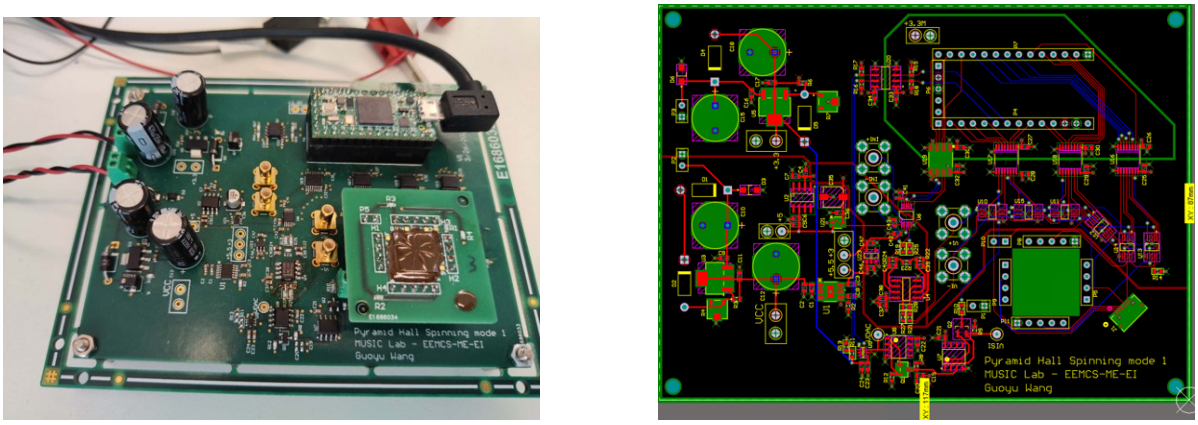
the settling time to 0.1 % accuracy is 0.7 µs.

3.2. PCB characterization

A PCB is designed for current-spinning of the pyramid sensor. This section describes the PCB system and sub-circuits design, and the tests performed with this PCB. The PCB schematic and layout are designed with Altium Designer. Figure 3.4a is the photo of the assembled current-spinning PCB with the Hall sensor carrier installed (bottom right). Figure 3.4b is the layout of the current-spinning PCB.

3.2.1. Current-spinning PCB design

Figure 3.5 shows the system diagram of the current-spinning PCB. It consists of several blocks: the current source, the switch matrix, the output stage and the micro-controller unit (MCU). The current source provides biasing current for the Hall sensor. The magnitude of current is controlled by the MCU, and connected to the biasing port of the switch matrix. The output stage includes a fully-differential



(a) Assembled current-spinning PCB

(b) Current-spinning PCB layout

Figure 3.4: Current-spinning PCB

pre-amplifier and an analog-to-digital converter (ADC). The pre-amplifier amplifies the Hall voltage from the sensor, and the ADC converts and sends the data to MCU. The data is then process by the MCU. The switch matrix consists of several multiplexers, which selects the Hall sensor contacts connected to the current biasing terminal and the input terminal of the output stage. The logic of the multiplexers are also controlled by the MCU. Thus, the current spinning modes are performed by programming the logic of the multiplexers.

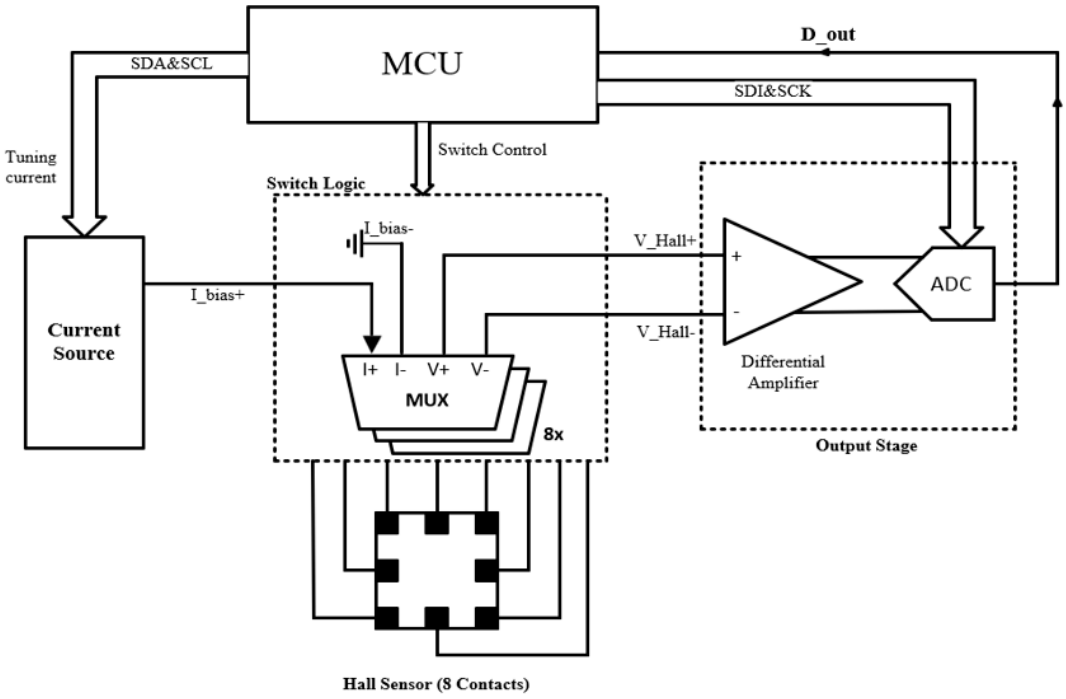


Figure 3.5: PCB system diagram

Power supply

Figure 3.6 shows the architecture of the power supplies of the PCB. An external 14-V supply is first pre-regulated by the NCV317, reducing the voltage drop on subsequent regulators while attenuating

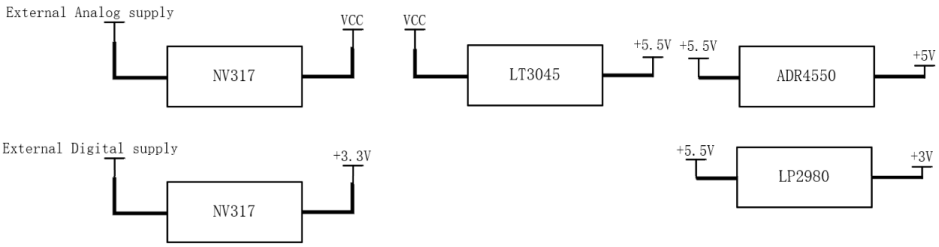


Figure 3.6: Power supply architecture

large-amplitude disturbances from the input source. The ultra-low-noise LT3045 then generates a clean 5.5V analog master rail for the front-end operational amplifiers and buffer amplifiers. To ensure high-accuracy data conversion, the ADC reference voltage is derived from this rail using the ADR4550, which offers high temperature stability and microvolt-level noise. The ADC analog supply is generated by the LP2980 converting 5.5 V to 3 V.

In parallel, a second independent 14-V input is regulated by another NCV317 to provide a dedicated 3.3-V digital supply for the multiplexers, digital isolators and the ADC digital supply, thereby preventing digital interference from contaminating the analog domain.

Current source

To better control the voltage drop on the Hall sensor to be less than ADC reference, the current should be sourced. Figure 3.7 shows the architecture of the biasing current source. AD5602 is a digital-to-

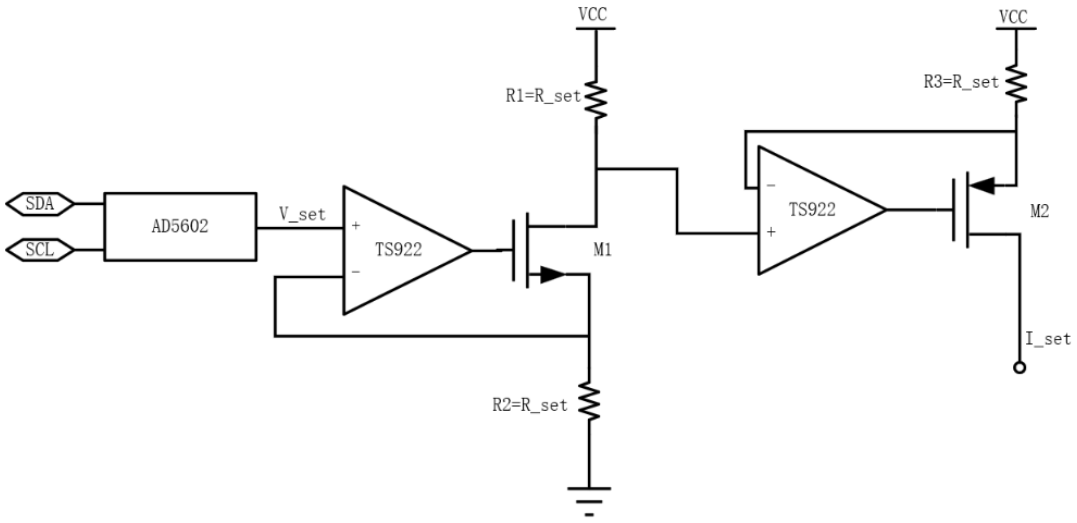


Figure 3.7: PCB current source

analog converter (DAC) controlled by the MCU. The DAC uses a 3.3V voltage supply, and is controlled by the MCU via I^2C communication. It generates a reference voltage which then produces a reference current via a buffer amplifier TS922 and a resistor. Then the current on R_1 and R_2 are is defined as:

$$I_{\text{set}} = \frac{V_{\text{set}}}{R_{\text{set}}} \tag{3.2}$$

Several factors have influence on the output current: the fluctuation of VCC and GND, component mismatches, and the inaccuracy of the reference voltage from the DAC. The first term is dynamic (supply ripples) and the others are deterministic. The VCC and GND are both provided by an external power source, but for a linear laboratory power supply, the GND terminal serves as the reference node of the internal regulation loop and is usually stable. In contrast, the VCC terminal passes through the power transistor stage and the feedback network, so its ripple and transient variations are typically larger than those on GND. To prevent the current from being affected by the ripples, the second branch with another OPAMP is introduced. The drain voltage of $M1$ is:

$$V_{d1} = V_{CC} - I_{\text{set}} R_{\text{set}} \tag{3.3}$$

, which is then copied by a same amplifier to the source of $M2$. Therefore, the voltage drop on R_3 is defined as:

$$V_{R_3} = V_{CC} - V_{d1} = V_{CC} - V_{CC} + I_{\text{set}} R_{\text{set}} = I_{\text{set}} R_{\text{set}} \tag{3.4}$$

Thus, the final biasing current is defined only by V_{set} and R_{set}. Any interference from VCC is canceled. The output terminal injects the current to the Hall sensor, and determines the total voltage drop on it. In this way, the common mode voltage of the Hall voltage is also defined, which is equal to half of the total voltage drop. Then, among the deterministic factors, the mismatches of the resistors and the input offsets of the buffer amplifiers will cause errors in the output current, but the actual current magnitude can be measured directly on the PCB at a testing via, and then be used for sensitivity and offset test. Thus, the result will not be affected by errors in the biasing current.

Spinning switches

Figure 3.8 shows the configuration of current spinning switches that use the phases mentioned in table 2.1. The diagonal contacts are shorted with traces on the sensor carrier PCB, which is shown in figure 3.9. Each multiplexer has four selective signal inputs and two address inputs. The four signal inputs are: positive/negative current biasing terminal ($I+/I-$) and positive/negative voltage read terminal($V+/V-$). The positive biasing terminal is connected to the output node of the current source, and the negative biasing is connected to the analog ground. The voltage read terminals are the two differential input terminals of the output stage. The output of the multiplexers is selected among the four inputs by the multiplexer address pins $A1$ and $A0$.

The selection of the multiplexers needs to be considered. First of all, to avoid attenuation more than 3 dB of the signal, the bandwidth of the switches should be at least equal to the signal frequency. Secondly, the on-resistance of the switches is in series with the input terminals of the output stage, and it adds noise to the stage.

To satisfy these requirements, the analog switch multiplexer ADG804 is chosen, which has a low on-resistance of 0.8Ω and a high bandwidth of over 10MHz. For the tested signal of 10-20kHz and sensor noise level of $7.42\,\text{nV}/\sqrt{\text{Hz}}$, ADG804 is a suitable choice.

Since the Helmholtz coil in the laboratory can only generate magnetic field in one direction at one time, the current spinning logic is designed to sense one axis at one time. For example, according to equation (2.9), to extract X field, only four phases (phase 1,2,4,5) and four contacts (contact 1,3,4,6) are needed. Therefore, only the multiplexers controlling contact 1,3,4,6 are enabled. Table 3.3 gives the

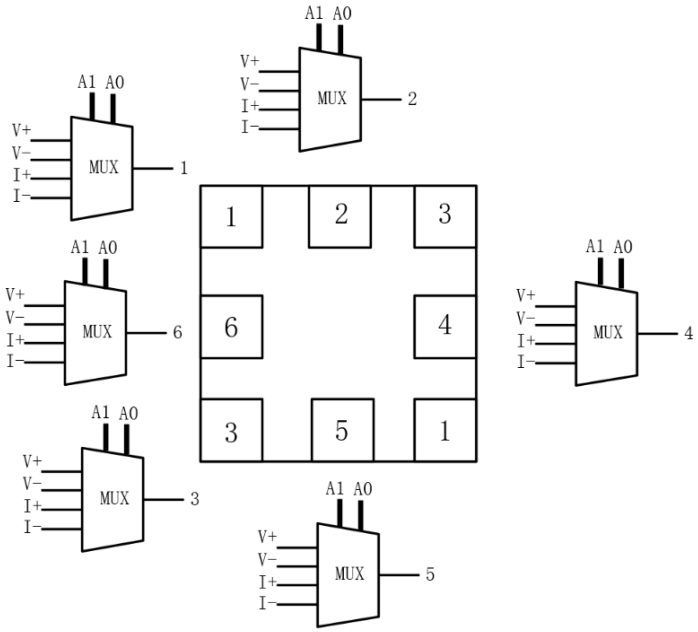


Figure 3.8: Spinning switches

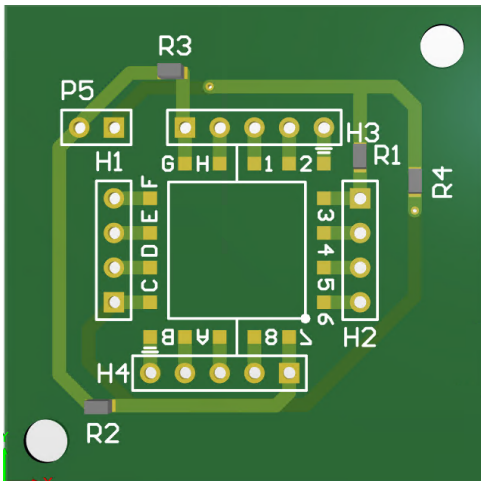


Figure 3.9: Sensor carrier

status change of the contacts during sensing mode for X field. After the programming code for testing X field is loaded to the MCU on the PCB, the multiplexers can only operate as table 3.3 lists.

According to table 2.1, to extract all the three fields, all the 6 phases and 6 contacts are needed, which means the circuit need to have two output stages working at the same time in each phase. To make the circuit less complex, the configuration that extracts one field using 4 phases is used. It requires only four active terminals at the most, thus only requiring one active output stage in each phase.

Phase	Contact 1 status	Contact 3 status	Contact 4 status	Contact 6 status
1	I+	I-	V+	V-
2	V-	V+	I+	I-
4	I-	I+	V-	V+
5	V+	V-	I-	I+

Table 3.3: X field contact switching logic

Output stage

The output stage has two functions: First, it should amplify the small Hall signals to a level that can be recognized by the ADC. Second, it should convert the Hall signal to digital data that can be processed by the MCU. Therefore, the architecture of this stage should be "Pre-amplifier + ADC". Figure 3.10 shows the diagram of this stage. Since the input common mode is equal to half voltage drop on the Hall

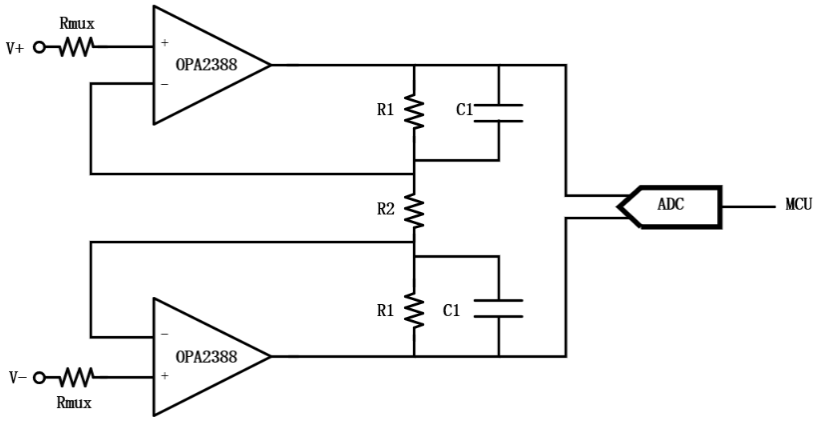


Figure 3.10: Output stage

sensor, it varies with the biasing current. Normally, for a fully differential amplifier stage, a common mode feedback circuit should be designed to fix the common mode of the output terminal. However, an ADC allowing a varying input common mode can be chosen to relax the common mode requirement and simplify the circuit.

Moreover, the ADC also needs sufficient sampling rate to convert the signal after current spinning. In this part, the spinning frequency range is set to include the largest flicker noise corner obtained in the noise test, which is 11 kHz. Therefore, the highest spinning frequency is set at 12 kHz, making the highest signal bandwidth 24 kHz. This requires the ADC sampling frequency to be higher than 50 kHz. However, in reality, an anti-alias filter is needed before the signal goes into the ADC to filter out the interference higher than half the sampling frequency. Otherwise, these interferences will be folded back

to the signal bandwidth due to sampling. The sampling frequency of 50 kHz assumes that the anti-alias filter has an ideal brick wall shape, which is impossible. Therefore, the sampling frequency (also sampling rate for a SAR ADC) should be much higher than twice the signal bandwidth, for instance, 10 times higher.

Thus, the ADS8881 is chosen, which uses a 5 V reference and have a sampling rate of 1 MSPS. Then, the gain of the pre-amplifier stage can be set in such way that the minimum input is amplified to at least an LSBs of the ADC to be recognized, while the maximum signal after being amplified does not exceed the supply range of the ADC. The DC gain is defined as:

$$G = 1 + \frac{2R_1}{R_2} \tag{3.5}$$

To test the output stage function without interference, it is first disconnected to other stages. An external voltage source is used to provide the test signal. The smallest voltage step it can generate is 1 µV. Therefore, the minimum gain to recognize the input signal is initially defined as:

$$G_{\min} = \frac{\text{LSB}}{1\,\mu\text{V}} \tag{3.6}$$

To deal with varying input magnitude, the resistors of the ladder is designed to be adjustable. Together with the parallel capacitors that are used for anti-aliasing filter, the bandwidth of the pre-amplifier stage is limited to:

$$BW = \frac{1}{2\pi R_1 C_1} \tag{3.7}$$

This bandwidth should be at least equal to the signal bandwidth of 24 kHz. Considering it also needs to be high enough for the signal settling, the capacitance can be changed to less value by making the capacitors adjustable.

Then, the input-referred noise should be considered. For the given topology, the input-referred noise is calculated for a half-circuit, which is shown below in figure 3.11 The main noise sources are: OPAMP

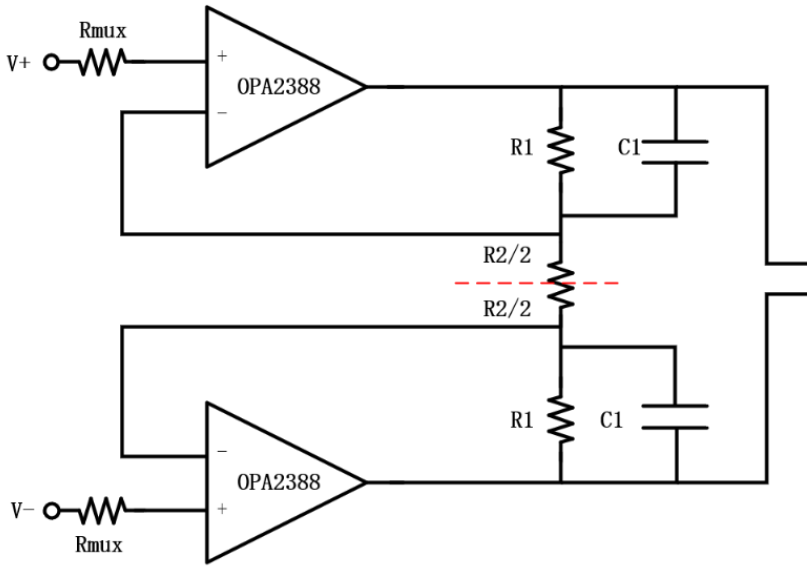


Figure 3.11: Half circuit for noise analysis

input voltage noise and the resistor thermal noise referred to the input. The resistor noise is analyzed as follow: For R_1, the output noise is:

$$e_{\text{out},1} = \sqrt{4kTR_1} \tag{3.8}$$

For $R_2/2$, the output noise is:

$$e_{\text{out},2} = \sqrt{4kTR_2/2} \cdot \frac{R_1}{R_2/2} \tag{3.9}$$

The multiplexer on-resistance noise and the OPAMP input current noise are negligible compared with OPAMP input noise, thus the total output noise voltage for a half circuit is:

$$e_{\text{out,single}} = \sqrt{e_{\text{out},1}^2 + e_{\text{out},2}^2 + e_{\text{out,AMP}}^2} \tag{3.10}$$

The input referred noise is the output noise divided by the gain:

$$e_{\text{in,single}} = \frac{e_{\text{out,single}}}{G} \tag{3.11}$$

And the input noise for the whole circuit is then:

$$e_{\text{in}} = \sqrt{2\, e_{\text{in,single}}^2} = \sqrt{2}\, e_{\text{in,single}} \tag{3.12}$$

This noise density should be lower than the lowest sensor noise density. Given an initial value of the resistors, the OPAMP input noise requirement can be derived.

Another criteria of choosing the OPAMP is the CMRR. The combined common-mode rejection of the preamplifier stage and the ADC input stage must be quantitatively evaluated. Let the differential input signal be V_d and the input common-mode voltage be V_{CM}, with the preamplifier providing a differential DC gain of G. The effective differential output in the presence of finite CMRR values is

$$V_{\text{out}} = GV_d + \left(\frac{G}{H_1} + \frac{1}{H_2}\right) V_{\text{CM}} \tag{3.13}$$

where H_1 and H_2 denote the CMRR (in linear scale) of the preamplifier front-end and the ADC input stage, respectively. The CMRR of the pre-amplifier stage is related to the CMRR mismatch of the two OPAMPs:

$$H_1 = \frac{H_{\text{OA}}(1-\gamma^2)}{2\gamma} \approx \frac{H_{\text{OA}}}{2\gamma} \tag{3.14}$$

where γ is the mismatch factor, and H_{OA} is the ideal OPAMP CMRR. The second term on the right side of equation (3.13) represents the differential error caused by common-mode leakage through both stages. The resulting relative error is therefore

$$\epsilon = \frac{V_{\text{err}}}{GV_d} = \left(\frac{1}{H_1} + \frac{1}{GH_2}\right) \frac{V_{\text{CM}}}{V_d}. \tag{3.15}$$

If for example use a 10-bit ADC, the gain error should be less than $\epsilon \leq 0.1\%$ which is an LSB , the combined CMRR must obey

$$\frac{1}{H_1} + \frac{1}{GH_2} \leq \frac{0.001}{V_{\text{CM}}/V_d}. \tag{3.16}$$

This relation sets limitation for the CMRR of both the buffer OPAMPs and the ADC. Finally, to meet all the requirements above, the OPA2388 is chosen for its low input noise (no 1/f noise), sufficient GBW and CMRR. A 10-bit ADC allowing varying input common mode and 1 MSPS sampling rate is chosen.

Another issue that affects the sensor characterization is the input offset of the buffer OPAMPs. Usually they are at several µVs, which is already comparable to the resolution of the circuit. However, for PCB characterization, this offset can be calibrated by first measuring it and storing it in digital domain. Since the offset is a certain DC value, it can be removed from the results by programming. Therefore, it is not considered as a factor for choosing the OPAMP.

MCU

To simplify firmware development in the Arduino IDE environment, a Teensy 4.0 micro-controller operating at 600 MHz is selected. It provides the required SPI and I^2C interfaces as well as a sufficient number of GPIO pins to manage the contact-switching network. The micro-controller is powered through USB and is fully isolated from the rest of the system by digital isolators, preventing any additional noise from coupling into the PCB circuitry. Figure 3.12 is the MCU Teensy 4.0.

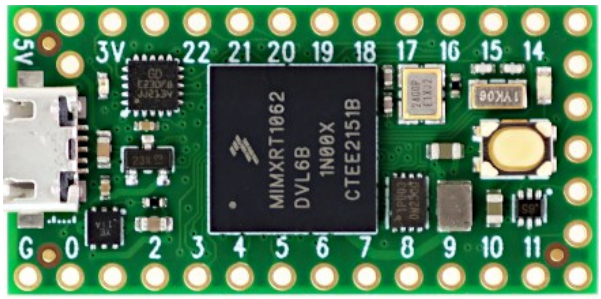


Figure 3.12: The MCU: Teensy 4.0

3.2.2. Offset and sensitivity test results

Two tests are performed using the current spinning PCB: the offset and the sensitivity. To prevent the Hall sensor from being magnetized, the offset test is taken first, which shield the system from the ambient field.

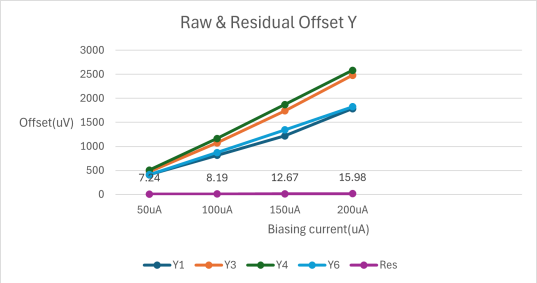
Offset test

First, the offset measurements are carried out with the system and sensor placed in a Gauss chamber to avoid external field. The MCU is loaded with the switch control program for X/Y and Z field. For each mode, biasing current ranging from 50 µA to 200 µA is applied.

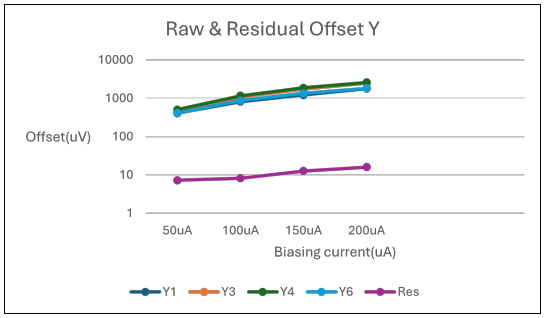
The output of each spinning phase is defined as the raw offset, which is related to the geometry asymmetry and the biasing current. These voltages are added up and then averaged over the four phases in each mode in digital domain to complete the operation of canceling the offset. The averaged result of the 4 phases raw offsets is defined as the residual offset.

The current spinning frequency is chosen to be higher than the 1/f corner frequency of the sensor. According to the figure 3.2, the maximum 1/f corner with biasing current of 50-200 µA is below 10 kHz. Therefore, the spinning frequency is set at 10 kHz. The results of raw and residual offset with different biasing are shown below in figure 3.13.

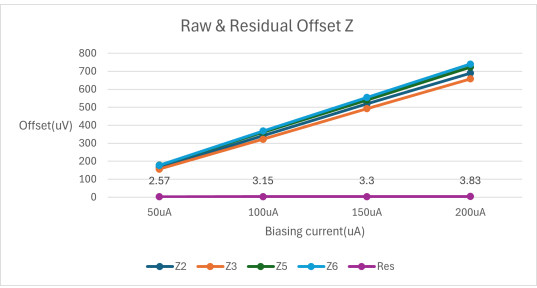
From the result, a clear trend is observed: for each mode, the raw offset increases linearly with the biasing current, which corresponds to the model described in Section 2.2. The raw offset of mode X/Y is much higher than that of mode Z, which implies the anisotropy of the sensor. The residual offsets after spinning are around 3 µV and 10 µV for mode Z and X/Y respectively.



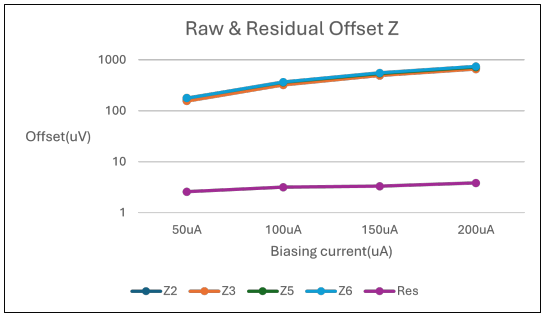
(a) Mode X/Y offset linear scale



(b) Mode X/Y offset log scale



(c) Mode Z offset linear scale



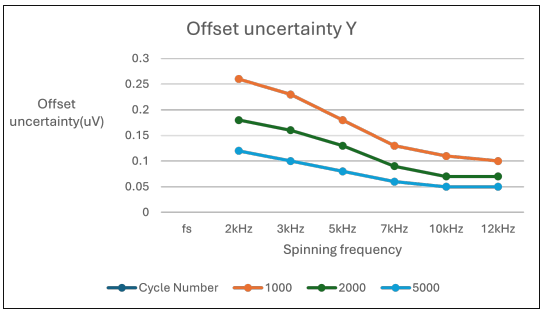
(d) Mode Z offset log scale

Figure 3.13: Raw and residual offset of mode X/Y and Z vs biasing current in µV

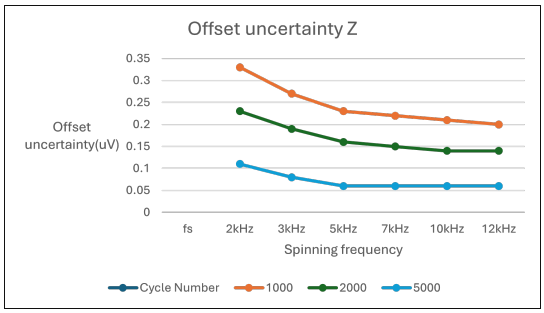
To evaluate the influence of spinning frequency on the residual offset, the uncertainty of the residual offsets with different spinning frequency from 2 to 12 kHz are tested. The uncertainty is defined as:

$$Uncertainy = \frac{\sigma}{\sqrt{N-1}} \tag{3.17}$$

where σ is the standard deviation of all the offset results measured in 1000, 2000, and 5000 times. N is the total number the results.



(a) Mode X/Y Residual offset uncertainty vs spinning frequency

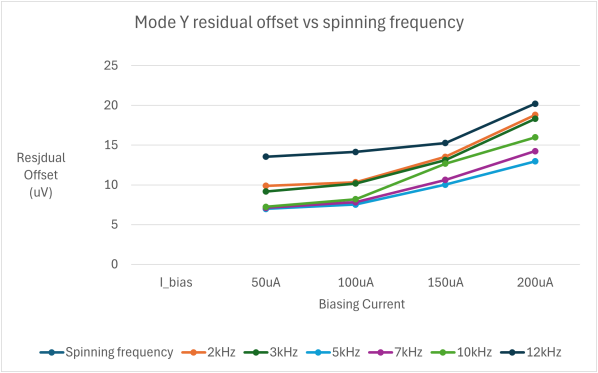


(b) Mode Z Residual offset uncertainty vs spinning frequency

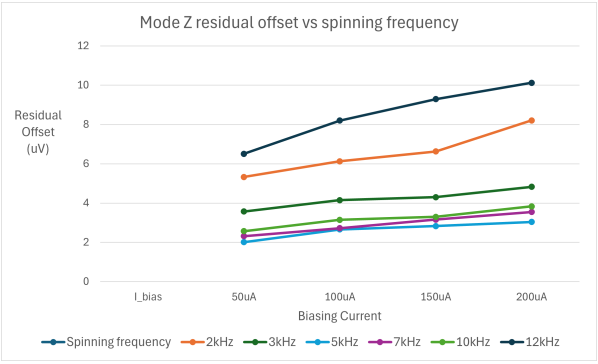
Figure 3.14: Residual offset uncertainty vs spinning frequency

From the figures 3.14, it can be observed that the residual offset uncertainty decreases when the spinning frequency and the sample number N increases. When lower than the 1/f noise corner, the current spinning cannot remove the flicker noise completely, which causes large spread of the residual offset. Once it reaches 1/f corner, the flicker noise no longer dominates the residual offset uncertainty, and starts to be flat. One could argue that with spinning frequency lower than 1/f corner, the residual

offset might be less due to less charge injection, as described by equation 3.18. It is basically a trade-off between resolution (noise) and accuracy (offset). The relation between spinning frequency and residual offset is shown in figure 3.15. From figure 3.15, it can be observed that from 5 kHz to 10 kHz, the residual offset increases with the spinning frequency. However, for spinning frequency 2 kHz, 3 kHz, and 12 kHz, the residual offset becomes higher. For the spinning frequency lower than the 1/f noise corner, the residual offset appears to be higher mainly because of the flicker noise. If we increase the sampling number N, this high residual will be mitigated. However, the decrease of the residual offset with lowering spinning frequency is not significant, while the uncertainty increment of the residual offset due to flicker noise is obvious. Therefore, the results implies that for both modes 10 kHz is a reasonable choice for spinning frequency.



(a) Mode X/Y Residual offset vs spinning frequency



(b) Mode Z Residual offset vs spinning frequency

Figure 3.15: Residual offset vs spinning frequency

$$V_{\text{error}} \propto f_s \cdot Q_{\text{inj}} \tag{3.18}$$

Sensitivity test and equivalent magnetic offset

The sensitivity is measured in for both X/Y and Z modes. First, the switches are configured into the logic for sensing the corresponding field. Then , the sensor is biased with 200 µA current and installed at the center of the coil in X/Y and Z direction. The Hall voltage varying with the magnetic field is shown in figure 3.16. By calculating the slope of each curve, the sensitivity for X/Y and Z mode are derived: X/Y sensitivity is 79 V/A/T, and Z sensitivity is 26 V/A/T.

To coherently compare different devices and technologies, the residual offset is typically scaled by the sensitivity and reported in magnetic field units. This quantity, referred to as the equivalent magnetic offset, sets a bound on the device's limit of (zero magnetic field) detection. These results are shown in

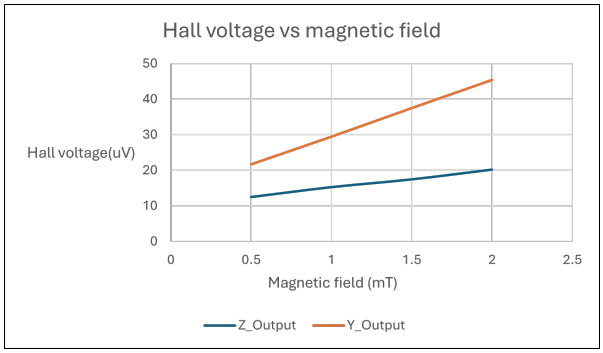
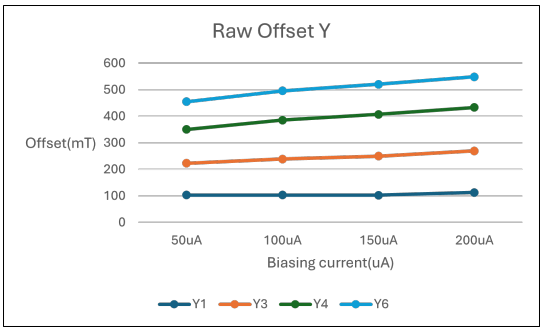
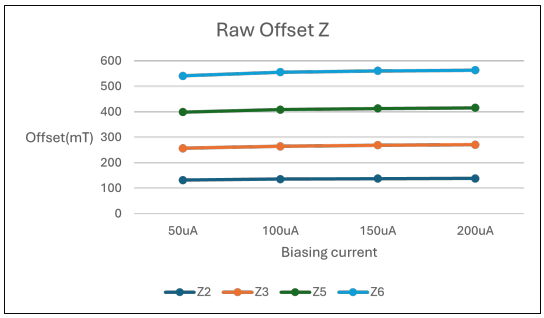


Figure 3.16: Hall voltage vs magnetic field

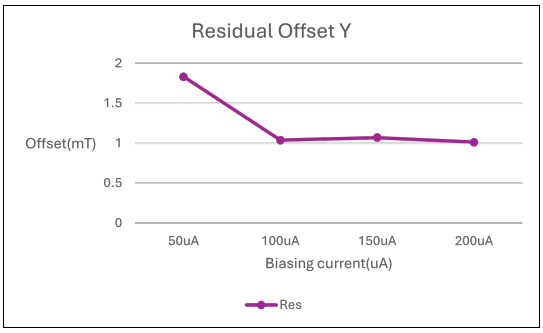
figure 3.17.



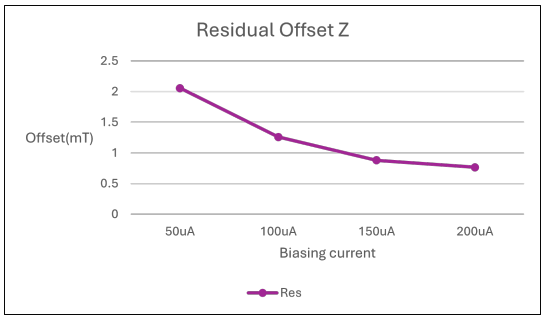
(a) Mode X/Y raw offset in mT



(b) Mode Z raw offset in mT



(c) Mode X/Y residual offset in mT



(d) Mode Z residual offset in mT

Figure 3.17: Raw and residual offset of mode X/Y and Z vs biasing current in mT

In the equivalent magnetic offset plots, the raw offset curves are divided by the product of sensitivity and biasing current, thus becoming much flatter compared with figure 3.13 , but still increases with the biasing current. Although the reduction of residual magnetic offset and the increment of biasing current are correlated, no clear theory supports that the residual offset decreases because of increasing biasing current. The summary of tested pyramid Hall sensor specs are in table 3.4. The resistance of the sensor is directly measured on the sample using multimeter.

Parameter	X/Y	Z
Residual offset	15.98 µV (1 mT)	3.83 µV (0.74 mT)
Resistance	3.3 kΩ	5.1 kΩ
Noise floor	7.42 nV/$\sqrt{\text{Hz}}$	9.62 nV/$\sqrt{\text{Hz}}$
1/f corner	9 kHz	8 kHz
Sensitivity	79 V/A/T	25.86 V/A/T
Bias current	200 µA	200 µA

Table 3.4: Pyramid Hall sensor specs

4

Transistor level circuit design

In this chapter, the design of a transistor circuit is explored to show the possibility of reading the sensor out with an IC. The design is based on the characterization result of chapter 3.

4.1. System requirements

This section discusses the signals that the system is designed to read out. Then the system topology and requirement for reading out are obtained.

4.1.1. Hall signal definition

At the beginning of this chapter, it is necessary to define the signal that the read-out circuit is designed to read. First, to have the best noise and offset sensor performance, the bias current and the spin frequency are determined according to the characterization results in chapter 3: 200 µA and 10 kHz.

As introduced in the chapter 1, one of the suitable applications of the pyramid is the motion sensing device of the joysticks. Hall sensors used in joysticks typically operate in magnetic field ranges on the order of only a few tens of millitesla and require signal bandwidths of 1-5 kilohertz according to several existing Hall sensor products.[19, 20, 21]. In this thesis, the target maximum operating field of the pyramid is 0-50 mT, and the magnetic signal bandwidth is set to be 5 kHz. The largest Hall signal voltage is then derived according to the sensitivity test result, which is 800 µV.

4.1.2. Current-spinning method consideration

As discussed in Chapter 2, to extract the Hall signal and remove the Hall offset, current spinning should be used. The working principle of current-spinning is to separate the Hall signal and the Hall offset in frequency domain, and it can be done in two ways: either up-modulating the Hall signal and keeping the offset in base band, or up-modulating the Hall offset. Let's first consider up-modulating the offset. The diagram of this architecture is shown in figure 4.1. The spinning frequency is defined here as the number of complete sequences in table 3.3 per second. The Hall offset is up-modulated to twice the spinning frequency in the 4-phase spinning sequence. Since the Hall voltage is only hundreds of µVs, amplification is needed in subsequent circuits. However, amplifiers suffer from the input offset voltage,

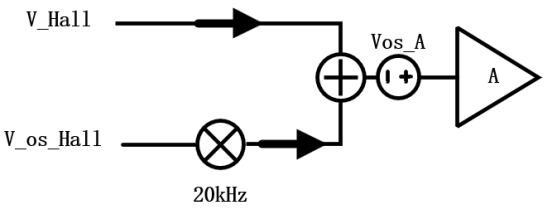


Figure 4.1: Up-modulate the Hall offset

as modeled in figure 4.1. If we leave the Hall signal in the base band, the amplifier offset will be a severe low frequency interference in the signal bandwidth, as shown in figure 4.2 . To avoid this, the

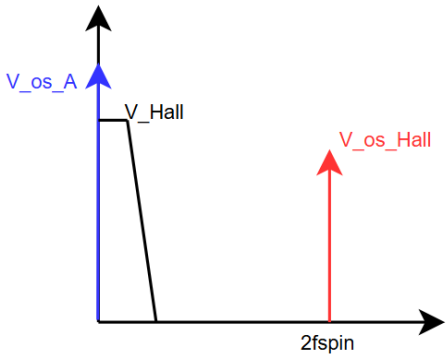


Figure 4.2: Signal spectrum of up-modulating the Hall offset

offset requirement of the amplifier becomes strict and additional circuits such as choppers and auto-zero switches will be used.

Another way of current spinning is to up-modulate the Hall signal and leave the Hall offset in the base band, as shown in figure 4.3. In this configuration, the Hall signal is separated from the Hall offset and the amplifier offset, thus leaving a clean signal band, as shown in figure 4.4.

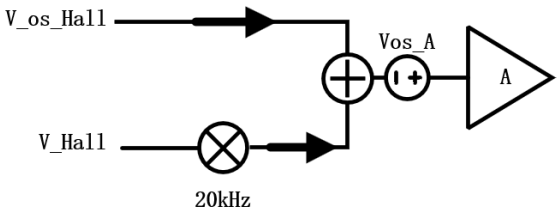


Figure 4.3: Up-modulate the Hall signal

The low offset requirement of the amplifier is then relaxed. However,this current spinning method does not eliminate the influence of the amplifier offset. One problem of this offset voltage is that it could make the amplifiers saturated if the total gain is high enough. Considerations on this issue is discussed later in section 4.3.2.

4.1.3. Overall input signal spectrum analysis

In the above section, the current spinning method is decided to be up-modulating the Hall signal. By implementing this method, the signal components at the input of the read-out stage can be seen as

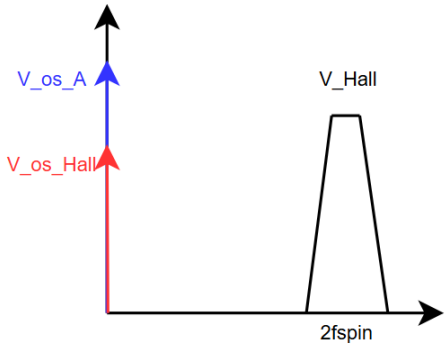


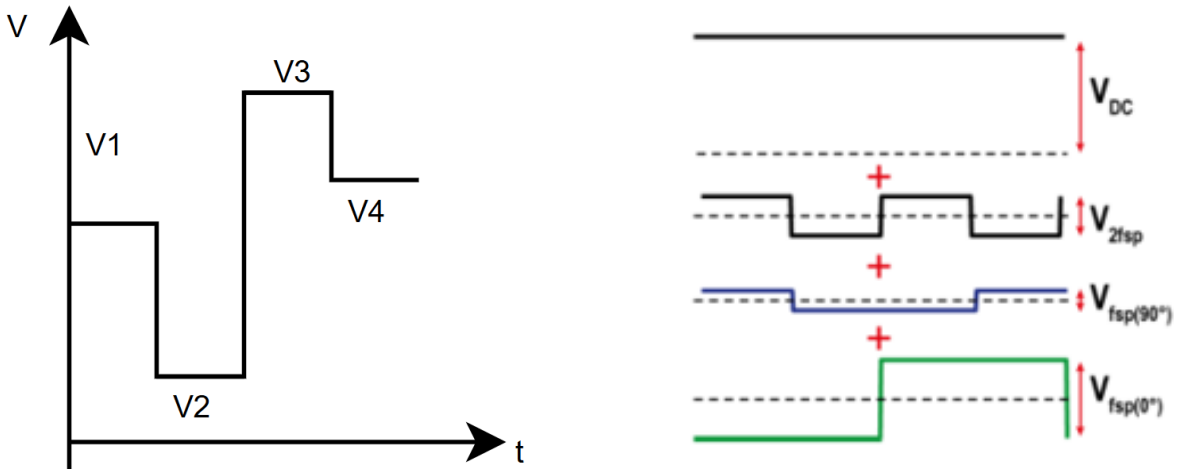
Figure 4.4: Signal spectrum of up-modulating the Hall signal

the superposition of the Hall signal at twice spinning frequency and the Hall offset at the base band. However, the Hall offsets of each spinning phase for both modes are not ideally DC voltage as in figure 4.4, but different voltages according to figure 3.13, which are extracted and shown in table 4.1.

Phases of mode X/Y	Raw offset X/Y (µV)	Phase of mode Z	Raw offset Z (µV)
Y1	2583	Z2	690
Y3	2479	Z3	658
Y4	2582	Z5	723
Y6	2623	Z6	740

Table 4.1: Raw offset of mode X/Y and Z with 200 µA biasing current

The reason of this phenomena is the different resistances for different current directions in the pyramid sensor, which, in turn, generate different offset voltages during the various spinning phases rather than a DC offset, as depicted in figure 4.5a.



(a) 4-phase offset voltage ripple

(b) Decomposed offset ripples[14]

Figure 4.5: The 4-level Hall offset and its decomposition

This 4-level offset ripple can be decomposed into four components: a DC component, two ripples at the spinning frequency with different phases, and another ripple at twice the spinning frequency[14]. The decomposition is shown in figure 4.5b.

The magnitude of the four components are derived from equation 4.2 to equation 4.5, where the four voltages correspond to the raw offsets of each spinning phases in table 4.1.

$$V_{\mathrm{DC}} = \frac{1}{4}\left(V_1 + V_2 + V_3 + V_4\right) \tag{4.1}$$

$$V_{2f_{\mathrm{sp}}} = \frac{1}{4}\left(V_1 - V_2 + V_3 - V_4\right) \tag{4.2}$$

$$V_{f_{\mathrm{sp}}(0^\circ)} = \frac{1}{4}\left(-V_1 - V_2 + V_3 + V_4\right) \tag{4.3}$$

$$V_{f_{\mathrm{sp}}(90^\circ)} = \frac{1}{4}\left(V_1 - V_2 - V_3 + V_4\right) \tag{4.4}$$

$$\tag{4.5}$$

Then the spectrum of figure 4.4 becomes more complex as shown in figure 4.6.

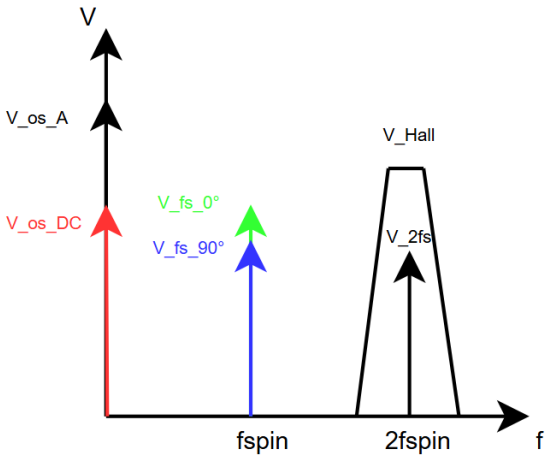


Figure 4.6: Real spectrum of up-modulating the Hall signal

4.1.4. Read-out circuit requirements

After the discussions above, the problem is clear: how to remove all the interfering components and keep the desired Hall signal? From the spectrum of figure 4.6, the read-out circuit should have such functions: 1). Block the DC Hall offset; 2) Suppress the Hall offset ripple at spinning frequency; 3) Amplify the Hall signal. For the Hall offset ripple at twice the spinning frequency, it has the same frequency as the Hall signal. Therefore it will be a residual offset and cannot be removed from the Hall signal. First of all, the DC component in the offset can be easily blocked by using a capacitive-coupled amplifier as the input stage. Then the components left are two ripples at spinning frequency and the residual ripple at twice the spinning frequency.

According to equations 4.2 to 4.5 and table 4.1, the magnitude of the ripple square waves $V_{f_{\mathrm{sp}}(0^\circ)}$ and $V_{f_{\mathrm{sp}}(90^\circ)}$ can be calculated: $V_{f_{\mathrm{sp}}(0^\circ)} = 36$ µV, $V_{f_{\mathrm{sp}}(90^\circ)} = 35$ µV. To achieve a clean spectrum which doesn't affect the Hall signal read-out, the offset ripples at the spinning frequency should be 'invisible'. In other words, it should be less than the minimum detective level, which is determined by the input integrated noise and the system bandwidth. Therefore, the second requirement for the read-out circuit is to reduce the 36 µV ripple to less than the 0.8 µV integrated input noise, which is the system resolution.

This requires a reduction of 35 dB at 10 kHz in the total system transfer function.

The third requirement should take into account the magnitude of the signal. The maximum Hall voltage is 700 µV. The amplified signal should not saturate the amplifier which uses 1.8 V supply, also considering the headroom of output transistors in the amplifier. Meanwhile, the amplified signal should be larger than an LSB of the ADC after the amplifier stage. Assuming an ADC with 1.8 V reference on the same chip is used, the total gain is set to be 900.

To summarize, the total read-out system requirements are:

- Suppresss the DC component in the Hall offset
- Input noise floor equal to the Hall sensor
- Suppress the Hall offset ripples at the spinning frequency by 35 dB
- Provide total gain of 900 for the Hall signal

4.2. Architecture design

In the above section, the total system requirements are obtained. To satisfy these requirements, the system must have two core functions: amplifying and filtering. This section discusses two different architectures to realize these functions, then selects one as the architecture used for this project.

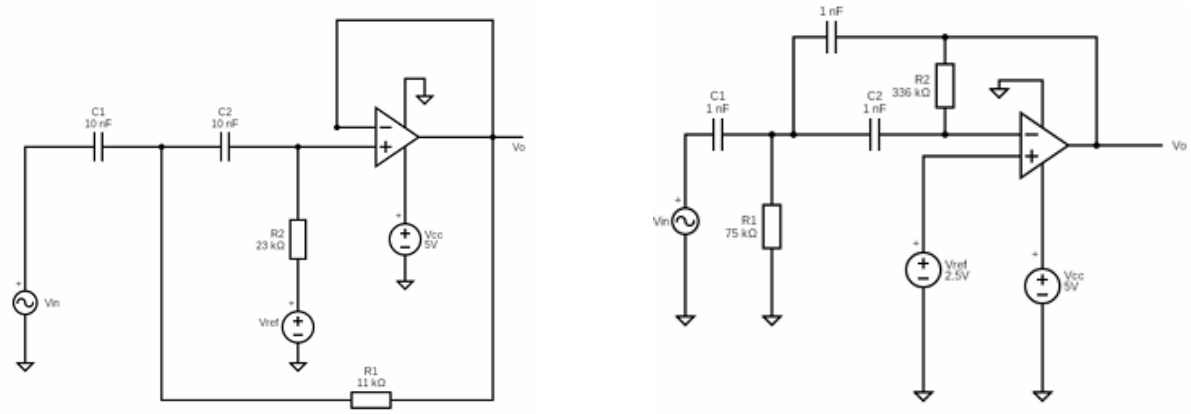
4.2.1. Amplifier + High pass filter

For the amplifying function, operational amplifiers with feedback can be used. For the filtering function, since the system needs to remove the DC components and ripples at the spinning frequency, an intuitive solution is to use a RC high pass filter (HPF). Considering the Hall signal bandwidth and suppression at the spinning frequency, the HPF should provide 35 dB suppression at 10 kHz while the high pass corner should be lower than 15 kHz, which is the lower boundary of the Hall signal bandwidth in figure 4.6. It is clear that a single-order HPF cannot reach the required suppression, since it offers only 6 dB reduction from 20 kHz to 10 kHz. Then, assuming a higher-order Butterworth filter is used, the following specifications are imposed:

- Attenuation at 10 kHz: $\geq 35\,\mathrm{dB}$.
- Attenuation at 15 kHz: $\leq 3\,\mathrm{dB}$.

Thus, a 10th-order Butterworth high-pass filter is required to achieve the specified attenuation characteristics. Such a high-order HPF can be realized by 5 second-order HPF cascaded [22] [23]. A second-order HPF can be realized in several configurations. Sallen-Key and multiple-feedback are two commonly used topologies, as shown in figure 4.7. The working principles of these HPFs are not discussed in this thesis, but it is notable that both topologies use OPAMPs. Therefore, to realize a 10th-order Butterworth high-pass filter, 5 times power and area of one second-order HPF are needed.

A digital HPF could be an alternative to avoid multiple cascaded filter stages. However, any noise or interference present above half of the sampling frequency is aliased into the base band during the ADC conversion. Since aliasing occurs before the digital filter is applied, these unwanted spectral components cannot be separated from the useful signal once folded. Thus, a purely digital approach cannot prevent high-frequency noise from corrupting the 15–25 kHz signal band.



(a) Sallen-Key second-order HPF

(b) Multiple-feedback second-order HPF

Figure 4.7: Two typical second-order HPF topologies[24]

Moreover, the quantization process introduces noise folding. Wide-band input noise is sampled and folded into the Nyquist band, raising the in-band noise floor by an amount proportional to the square root of the input noise bandwidth. Therefore, the digital filter can only attenuate deterministic frequency components but cannot reverse the noise folding that has already occurred during sampling.

4.2.2. Amplifier + Ripple reduction loop

From the analysis above, it can be seen that it is relatively hard to use conventional high pass filters to achieve the required attenuation without affecting the signal bandwidth. For an analog HPF, the fundamental issue is the trade-off between its attenuation capability, high pass corner frequency and the power consumption. For a digital HPF, the issue is the noise folding and aliasing due to discrete-time sampling.

To create a notch filter that suppresses only certain frequency tones, another topology, the ripple reduction loop (RRL) is proposed [25]. The RRL effectively plays the role of a notch filter with a narrow notch width, and due to its steep roll-off characteristic, the attenuation of desired signal bandwidth is small. The working principle of the RRL is shown in figure 4.8. The amplified offset ripple at the spinning frequency is sensed and converted to an AC ripple current. The ripple current is then demodulated to DC by a chopper that chops at the spinning frequency. The DC current is converted to a ramping voltage by an integrator, and the ramping voltage becomes a constant voltage when the feedback loop is stable. Finally the DC voltage is converted to a ripple voltage which has opposite polarity to the original offset ripple, thereby compensating for the offset voltage ripple in the main path.

The corresponding transfer function plot is shown in figure 4.9. The notch frequency is determined by the chopping frequency in the loop, and the notch width is determined by the unity-gain frequency of the RRL loop transfer function. Specifically, when the loop has unity gain, it does not provide suppression, and its transfer function becomes flat. Therefore, the suppression target can be selected accurately by the chopper, and the notch width can be controlled not too wide to reduce the Hall signal. The realization of the circuit is also much simpler than cascaded high order HPF. In addition to the main amplifiers, the RRL has much less active blocks, thus having much less power consumption.

By comparing the two ways of realizing the amplifying and filtering functions, it is clear that the RRL

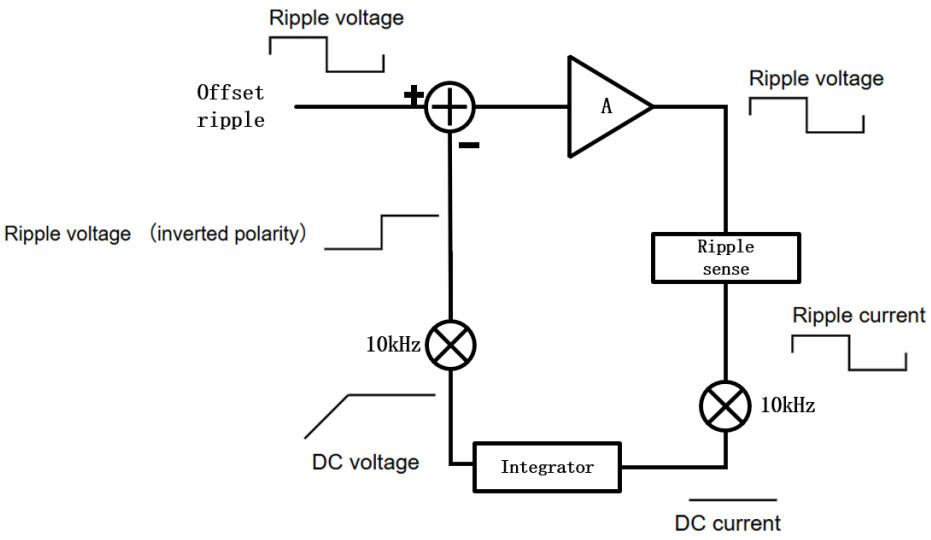


Figure 4.8: Block diagram of RRL

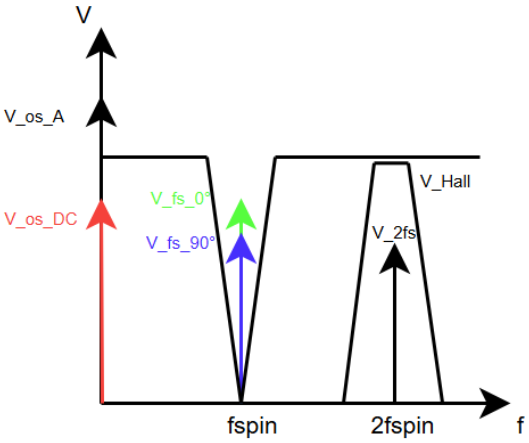


Figure 4.9: Transfer function of RRL

is more reasonable to be implemented. Therefore, the system architecture is selected as 'amplifier + RRL'

4.3. Sub-circuit design of amplifier + RRL structure

The circuit architecture is determined to be amplifier + RRL in the above section. In this section, the design of each circuit block in the amplifier + RRL structure is discussed.

4.3.1. Main amplifiers

Starting from the main amplifiers, according to the system requirement of total gain of 900, it can be easily achieved by using two cascaded amplifiers and distribute the gain between them.

Since the RRL only provides reduction in a narrow frequency range, it does not remove the DC component in the Hall offset. Therefore, this task is taken by the input stage of the main amplifiers by making it capacitive-coupled. But this brings another issue: the input transistor pair is not biased. To solve this issue, a DC feedback loop is added in parallel with the feedback capacitor, with the existing common mode feedback (CMFB) inside the amplifier to bias the input pairs. The values of C_2 and R_b is not selected randomly. Since they effectively form a high pass filter in the feedback path, the time constant should be selected so that the signal attenuation due to high pass filtering is less than 0.1 % with a 10-bit ADC, whose LSB is around 0.1 % of its full scale.

The second stage only provides the rest of the total gain. The noise requirement is more relaxed than the input stage. Moreover, with the CM provided by the CMFB of the first stage, it doesn't need additional biasing loop. The block diagram of the main amplifiers are shown in figure 4.10.

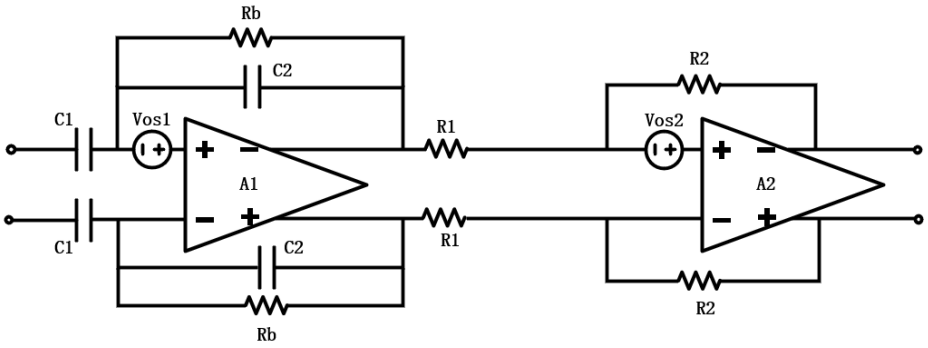


Figure 4.10: Block diagram of main amplifiers

The input referred noise analysis of the cascaded amplifiers is as following:

The total input-referred thermal noise is derived by referring all internal noise sources back to the input of the first stage. The first stage has a closed-loop gain $A_1(s)$, while the second stage has a closed-loop gain $A_2(s)$, yielding an overall gain of

$$A_{\mathrm{tot}}(s) = A_1(s)A_2(s). \tag{4.6}$$

The following noise sources contribute to the overall input-referred noise:

- The first-stage op-amp input voltage noise: e_{n1}

- Thermal noise from the first-stage feedback network: $e_{n,Rb,\text{in}}(s)$
- Thermal noise from the inter-stage series resistor:

$$e_{n,R1} = \sqrt{4kTR_1}$$

- Equivalent input voltage noise of the second stage: $e_{n2,\text{eq}}$, including both op-amp noise and feedback resistor noise

The noise of the inter-stage resistor, after being amplified by $A_2(s)$ and referred back through the total gain, gives the following.

$$e_{n,R1,\text{in}}(s) = \frac{e_{n,R1}}{|A_1(s)|}. \tag{4.7}$$

The input referred noise of the biasing resistor R_b is proportional to the thermal noise current of R_b: $\sqrt{4kT/R_b}$, and since R_b is large to reduce high pass attenuation to the signal, its noise contribution is negligible. Similarly, the second-stage equivalent input noise contributes

$$e_{n2,\text{eq,in}}(s) = \frac{e_{n2,\text{eq}}}{|A_1(s)|}. \tag{4.8}$$

The total input-referred thermal noise of one side (single-ended) is given by the root-sum-square of all independent noise sources:

$$e_{n,\text{in,single}}(s) = \sqrt{e_{n1}^2(1 + C_2/C_1)^2 + e_{n,Rb,\text{in}}^2(s) + e_{n,R1,\text{in}}^2(s) + e_{n2,\text{eq,in}}^2(s)} \tag{4.9}$$

Since the topology is fully differential and both halves are assumed to be noise uncorrelated, the total differential input noise is

$$e_{n,\text{in,diff}}(s) = \sqrt{2}\, e_{n,\text{in,single}}(s) \tag{4.10}$$

This total input referred noise should be designed to be less than Hall sensor noise floor. From equation 4.10, the dominant contributor is the input noise of the amplifier A_1.

4.3.2. Multiplexed RRLs

This part discusses the working principle and implementation of a multiplexed RRL topology to suppress different Hall offset ripples.

RRL for one offset ripple component

According to figure 4.8, there are several functioning blocks in the RRL: the ripple sensing component, the integrator, the choppers and the subtractor. The first two items can be implemented as an R-C + OPAMP integrator, as shown in figure 4.11. The input signal of this block is the offset ripple demodulated to DC by the chopper. Since the input resistor R_1 in figure 4.10 converts the ripple voltage to a current, we can create a ripple current with inverted polarity to compensate for it. Therefore, the ripple voltage with inverted polarity in figure 4.8 should be converted to a current by a trans-conductance amplifier (G_m). And the output current of this G_m module is injected to the virtual ground node of A_2. Thus the output of A_2 is the generated by the compensated current through R_2. The total diagram of the RRL (including the second amplifier)is shown in figure 4.12. From figure 4.12, we can derive the transfer function from V_1 to V_2, and the loop gain of the RRL by assuming the two choppers

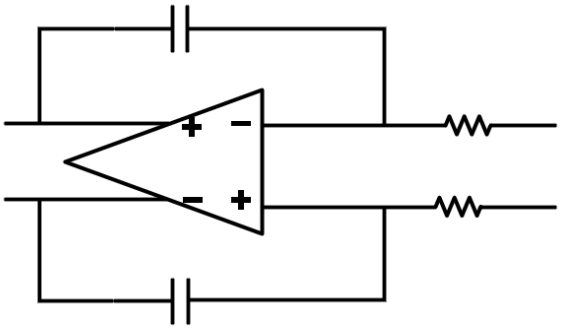


Figure 4.11: Block diagram of the RRL integrator

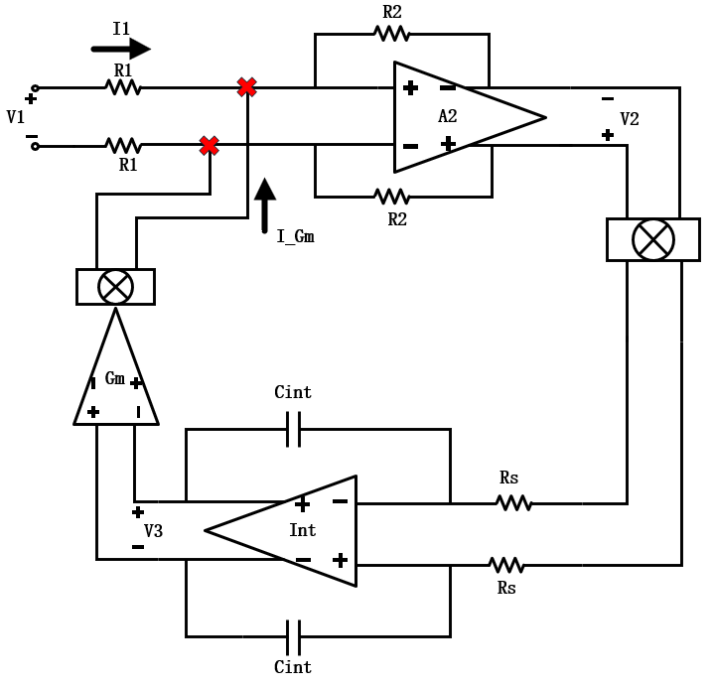


Figure 4.12: Block diagram of the total RRL

stop switching. First, we cut the loop as shown in figure 4.12, and write KCL equations at the cut node assuming A_2 is an ideal amplifier:

$$I_{\mathrm{Gm}} = \frac{A_{\mathrm{int}} G_m V_2}{1 + (1 + A_{\mathrm{int}}) s R_s C_{\mathrm{int}}} \tag{4.11}$$

$$I_1 = \frac{V_1}{R_1} \tag{4.12}$$

$$(I_1 - I_{\mathrm{Gm}})\, R_2 = \frac{V_1}{R_1} \tag{4.13}$$

where I_1 is the current on R_1 and I_{Gm} is the output current of the G_m block.

By solving the equations we have:

$$\frac{V_2}{V_1} = \frac{\frac{R_2}{R_1}}{1 + \frac{A_{\mathrm{int}} G_m R_2}{[1 + (1 + A_{\mathrm{int}}) s R_s C_{\mathrm{int}}]}} \tag{4.14}$$

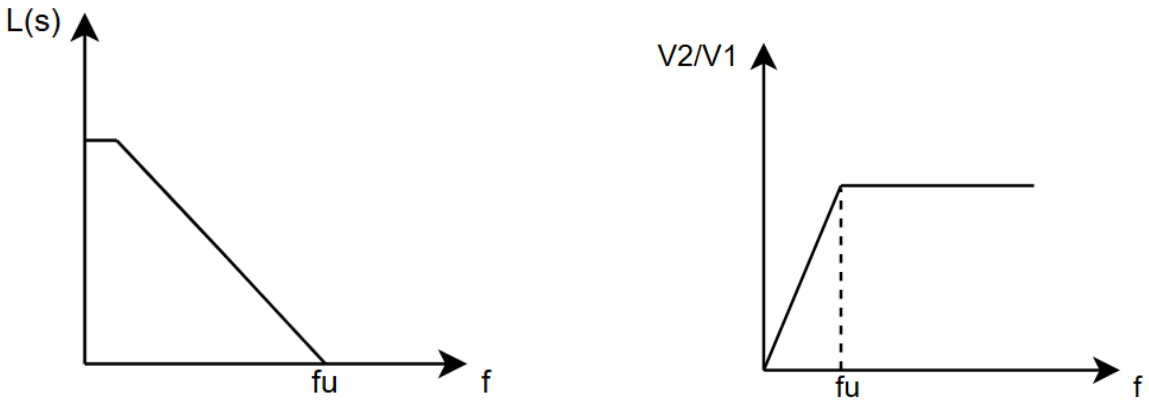
The fraction term in the denominator of the transfer function is denotes the loop gain of the RRL, which is:

$$L(s) = \frac{A_{\mathrm{int}} G_m R_2}{1 + (1 + A_{\mathrm{int}}) s R_s C_{\mathrm{int}}} \tag{4.15}$$

The unity gain frequency of this loop gain is given by:

$$f_u \approx \frac{1}{2\pi} \cdot \frac{R_2 G_m}{R_s C_{\mathrm{int}}} \tag{4.16}$$

The plots of transfer function magnitude from V_1 to V_2 and the RRL loop gain are shown in figure 4.13. It can be observed that when the choppers are not switching, the overall transfer function from V_1 to V_2 is high-pass with a corner frequency of f_u. And with this assumption, the RRL is actually suppressing the DC component of V_2. The suppression ratio is equal to the numerator of the RRL loop gain.



(a) RRL loop gain Bode plot

(b) Transfer function from V_1 to V_2 Bode plot

Figure 4.13: Bode plots of RRL transfer (without phase curve)

If the choppers start to switch at frequency f_s, it effectively shifts the transfer function curve to the right. The zero is moved from the origin to f_s, as shown in figure 4.14.

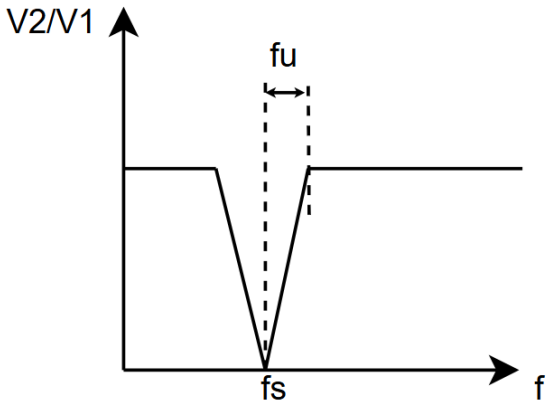


Figure 4.14: Transfer function from V_1 to V_2 Bode plot with chopping

Thus, the RRL now realizes the function of suppression at certain frequency. The suppression ratio is the same as the suppression to DC when choppers are not switching, which is determined by the open-loop gain of the integrator amplifier, the trans-conductance and the feedback resistance of the second amplifier stage. The notch width is $2f_u$, which is related to the trans-conductance, the feedback resistance of the second amplifier stage, the sensing resistor and the integrator capacitor. The constraints for the notch width and notch width are:

$$A_{\text{int}} G_m R_2 > 35\,\text{dB} \tag{4.17}$$

$$\frac{1}{2\pi} \cdot \frac{R_2 G_m}{R_s C_{\text{int}}} < 5\,\text{kHz} \tag{4.18}$$

The integrator amplifier and the trans-conductance should be designed to satisfy these requirements.

Apart from the ripple suppression requirements, the noise that RRL adds to the system should also considered. The noise referred to the input of A_1 contributed by the RRL can be expressed as:

$$e_{n,RRL} = \frac{\sqrt{V_{no,int}^2 + V_{ni,Gm}^2}\, G_m R_1}{\frac{C_1}{C_2}} \tag{4.19}$$

where $V_{no,int}$ is the output noise of the integrator, and $V_{ni,Gm}$ is the input noise of the trans-conductance module. This noise of RRL can be mitigated by designing the factor below small:

$$\frac{G_m R_1}{\frac{C_1}{C_2}} \tag{4.20}$$

where the capacitance are selected according to the closed-loop gain, and the G_m is the input transistor gm value of the trans-conductance module, which is at 10^{-6} - 10^{-3} level. Thus, R_1 can be designed to make the RRL noise negligible compared to the main amplifier input noise.

Multiplexed RRLs for all ripple components

The diagram in figure 4.8 only resolves one offset ripple of spinning frequency. To suppress the two ripples at 10 kHz with different phases, the choppers in the RRL should be controlled with 10 kHz clock with corresponding phases (0 or 90 degree). A intuitive solution is to have two RRL in parallel which are only different in the chopper frequency [26]. But it consumes more power and area.

Thus, the multiplexed RRL is proposed [14]. The total diagram is shown in figure 4.15. In this

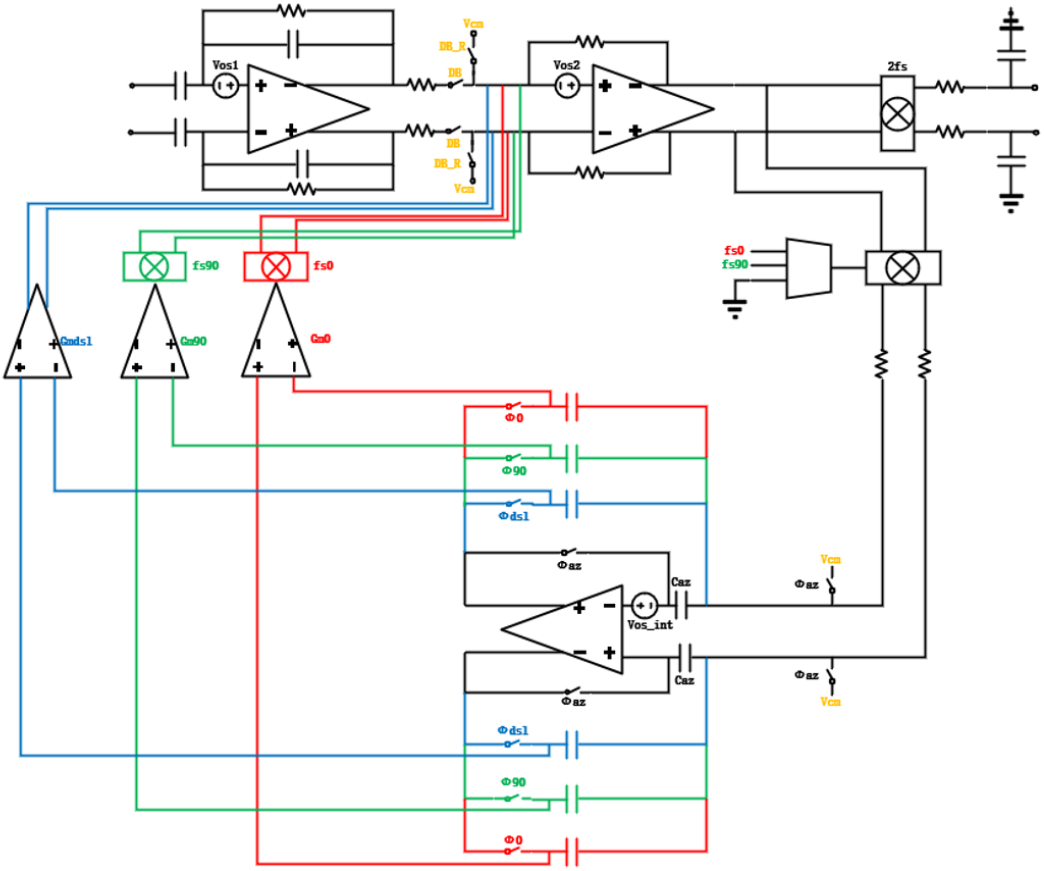


Figure 4.15: Total diagram of the read-out circuit with multiplexed RRL

topology, the chopper at the input of the integrator is controlled by a multiplexed clock, which has four non-overlapping operating phases. In the first phase, the integrator amplifier is auto-zeroed. Its input offset is stored on the two auto-zero capacitors, otherwise it will cause an ripple at 10 kHz in the signal path. The G_m amplifiers also have input offset voltage, but it can be referred to the input of the integrator thus attenuated. During the next two phases, the choppers switch with clocks of different phases. The integration capacitors start to be charged by the integrator amplifier and the voltages on these capacitors start to ramp. The loop generates corresponding compensation current ripples and injects them into the main path. Once the magnitude of this current reaches the level that satisfies the equation 4.13. The last phase is to deal with the input offsets of the main amplifiers. These offsets are similar with the offset ripple and the only difference is that they are DC components. If they are amplified without suppression, the total gain of the main amplifiers will make the offsets clipping the supply rail. Therefore, with the existing structure of RRL, we only need to make the choppers stop switching, and the loop will suppress the amplifier offsets in the same manner as suppressing the Hall offset ripples. The timing diagram of the phases are shown in figure 4.17a.

Meanwhile, a set of dead-band switches are added to the main path. This is because during the transient of the input signal, the offset ripple and the compensation ripple have different edge slopes, which is related to the bandwidth of A_1 and the RRL, The simplified diagram is shown in figure 4.16.

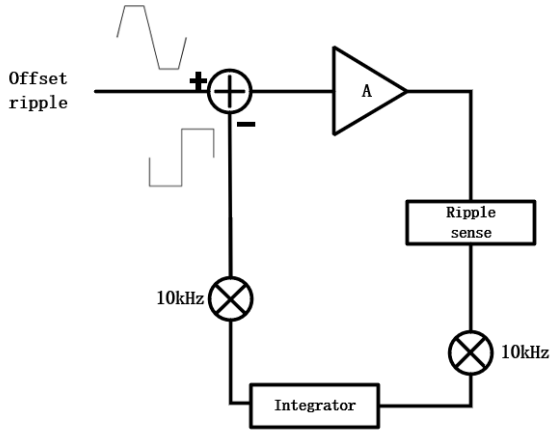
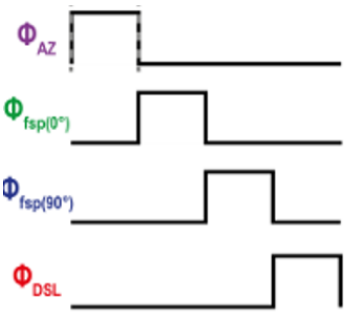
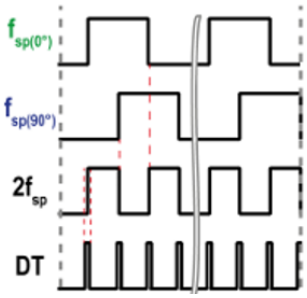


Figure 4.16: Hall offset and its compensation signal with different edge slopes

This difference causes a ripple at the spinning frequency. By cutting off the main path with the dead-band switches at the transient moments of the signal, these ripples can be avoid. The timing diagram of the chopper clocks and the dead-band switches are shown in figure 4.17b,based on prior art from A. Jouyaeian et al .



(a) Four working phases of the RRL[14]



(b) Chopper clock and the dead-band switch timing diagram[14]

Figure 4.17: RRL timing diagram

4.4. Circuit implementation

In the sections above, the total diagram of the read-out circuit with multiplexed RRL and the sub-circuit requirements are decided. In this section, the transistor level circuit design is addressed with the derived specifications.

4.4.1. Main amplifiers

The requirements for the main amplifiers are summarized below:

- Total gain: 900.

- Gain accuracy: 0.1%.
- Settling time to 0.1%: 0.7 µs
- Total input noise:

$$\sqrt{e_{n,\text{in,diff}}^2 + e_{n,\text{RRL}}^2} < 7.42\,\text{nV}/\sqrt{\text{Hz}} \tag{4.21}$$

First of all, the total gain of 900 is distributed equally to the two amplifiers giving them each 30 dB closed-loop gain. To reach the gain accuracy of 0.1%, the loop gain of both amplifiers should be at least 60 dB. Therefore, the two amplifiers should have at least 90 dB open-loop gain. This is large for a single-stage amplifier. So it is reasonable to use a two-stage structure for both amplifiers. This allows more open-loop margin in different process corners, for example 10 dB, and the open-loop gain is set to be 100 dB.

Knowing the open-loop gain, closed-loop gain and the settling time to 0.1% accuracy, the gain-bandwidth product (GBW) of the amplifiers can be derived. Since a 1-pole amplifier settles with 8.6 dB/τ, where τ is the closed-loop time constant, the GBW is calculated to be larger than 45 MHz.

Then, the input referred noise, ignoring the RRL noise, set constraints to the gm of the input pair transistors. In equation 4.9, apart from the input noise of A_1, the other terms are attenuated by the gain of A_1. So for estimation of the input pair gm, only the input noise of A_1 is considered. The calculated required gm is larger than 0.462 mS.

Since the amplifiers should have low input noise and high open-loop gain, the current-reuse telescopic is suitable for the first stage in the amplifier topology. This topology has both PMOS and NMOS working as the input at the same time, thus it generates twice input trans-conductance as the amplifiers using only one-side input. The output current noise of the current-reuse first stage is:

$$\overline{i_{o1,\text{noise}}^2} = 8kT\gamma\left(g_{m2} + g_{m8} + \frac{g_{m4}}{1 + g_{m4}r_{o4}} + \frac{g_{m6}}{1 + g_{m6}r_{o6}}\right) \tag{4.22}$$

which shows that the current noise from the cascode transistors are negligible. Then the input noise voltage density is derived:

$$v_{\text{in,noise}} = \sqrt{\frac{8kT\gamma}{(g_{m2} + g_{m8})}} \quad \left[\text{V}/\sqrt{\text{Hz}}\right] \tag{4.23}$$

As a result, the gate noise voltage power is only half of those of one-side input amplifiers when consuming same current. Due to the six stacked transistors in the first stage between VDD and GND, it has a small output swing. Therefore, a common-source second stage is added with Miller compensation and a resistor compensating for the right-plane zero. The diagram is depicted in figure 4.18.

Since the output resistance is similar to that of a conventional telescopic or folded-cascode amplifier, which is at the order of $(g_m r_o)^2$, the doubled input trans-conductance also brings doubled open-loop gain.

4.4.2. Multiplexed RRLs

The main constraints of designing the RRL is given by equation 4.17 and equation 4.18. It can be observed that the factor $G_m R_2$ is limited by the two equations. For the G_m module, it should have a large output resistance to load the feedback resistor R_2, and its trans-conductance should be neither too small to generate the compensation current nor too large to make the notch width small. For R_2

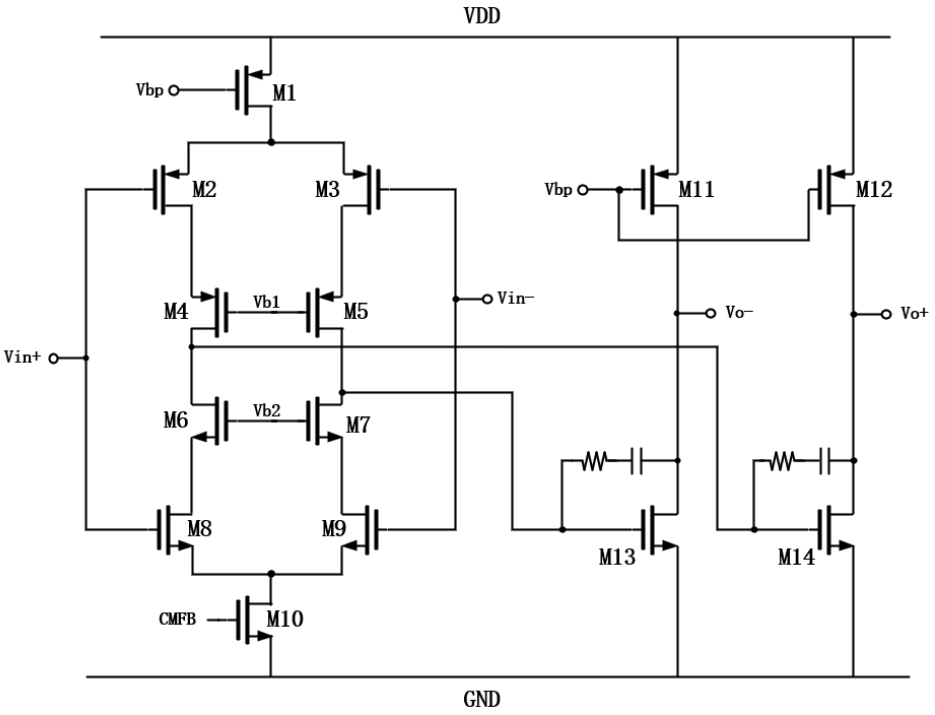


Figure 4.18: Diagram of amplifier A_1

and R_1, R_1 should not be too small to load A_1, and R_2 should not be too large that the notch becomes wide. In this thesis, the G_m is chosen to be 0.6 mS, and R_1 is 10 $k\Omega$. The G_m module reuses the first stage of A_1, as shown in figure 4.19, with the size of transistors scaled.

The open-loop gain of the integrator amplifier only needs to ensure the attenuation satisfying equation 4.17. It also takes advantage of the large gain of the current-reuse structure of A_1, and has 80 dB open-loop gain.

There are large value resistors used in this system: the DC biasing resistor of A_1 and the sensing resistor at the output of A_2. They are at the order of several giga ohms and difficult to be realized with poly resistors or diffusion resistors due to the limited sheet resistance. Therefore, there are several solutions to achieve high value resistance. First, pseudo resistor using back-to-back transistors is proposed[27], as depicted in figure 4.20a. It is a circuit element that exploits the extremely small drain current of MOS transistors operating in the subthreshold (weak inversion) or near-cutoff region to realize ultra-high equivalent resistances. Unlike physical resistors in CMOS processes, pseudo-resistors can achieve giga-ohm level resistances. But the pseudo resistance is strongly nonlinear and depends on the voltage across the device.

Another solution is the switched-resistor, also known as duty-cycle resistor[28] as shown in figure 4.20b. A duty-cycle resistor is an effective technique for realizing large equivalent resistances in standard CMOS processes. The concept relies on periodically switching a much smaller physical resistor with a certain duty cycle. When the switch is on for a fraction D of the period, the resulting average resistance becomes $R_{\text{eq}} = R_d/D$, enabling values in the hundreds of mega-ohms to tera-ohm range. The duty-cycle resistor doesn't vary with the input signal, but its value depends on the accuracy of the switch clock. Since both the DC biasing resistor and the sensing resistor see a varying input signal in this circuit, they are chosen to be duty-cycle resistors with values higher than 5 $G\Omega$.

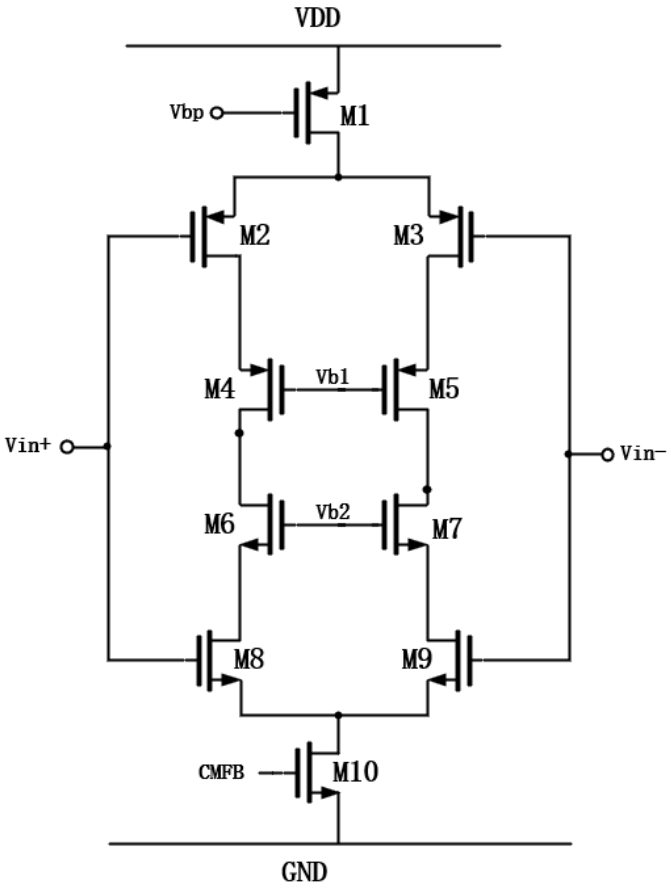


Figure 4.19: Diagram of G_m and A_{int}

(a) Pseudo resistor

(b) Duty-cycle resistor

Figure 4.20: Two solutions to big value resistor

The switches used in the RRLs have different design considerations. First, for the switches in series with the integration capacitors, the task is to disconnect the capacitors and the output of the integrator amplifier, ensuring the DC voltage at the input of the G_m will hold when the corresponding phase is low. Therefore, the off-resistance and the leakage current through this switch are crucial, because they will cause the DC voltage slowly decreasing and affecting the magnitude of the compensation current. To avoid this, these switches are single PMOS transistors with small W/L. The same requirement also applies to the integrator auto-zeroing switches, since they ensures the stored offset voltage on C_{az} not leaking.

The dead-band switches have the opposite resistance requirement. Since they are in series with the input resistor R_1, their on-resistance are added to R_1 thus directly affecting the closed-loop gain of A_2. Therefore, they should have low on-resistance. The value of the on-resistance should be designed according to the 0.1 % accuracy requirement of A_2. They are then implemented using transmission gate switches with large W/L.

4.5. Summary

To summarize, this chapter discusses the design of a transistor level read-out circuit for the current-spun Hall sensor. First, the system requirements are derived using the measured sensor specifications in chapter 3. Then, the design considerations of each sub-circuit block are discussed. The simulation of this system is discussed in chapter 5 given a input signal that models the superposition of the Hall voltage and the offsets.

5

Simulation results

This section discusses the simulation results of the read-out analog front end circuit built in Cadence Virtuoso, including the specifications of the amplifiers A_1 and A_2 used in the main path, the integrator amplifier, and the overall noise and suppression performance of the system. The results are simulated for five corners (tt, ff, ss, fs, and sf) and mismatch. The corners are defined to describe variation of NMOS/PMOS speed. T = typical, F = fast, S = slow. TT: both typical (nominal case). FF: both fast (best speed, more leakage). SS: both slow (worst speed). SF: slow NMOS, fast PMOS. FS: fast NMOS, slow PMOS.

5.1. Main amplifier specifications

The main amplifiers A_1 and A_2 shares the same topology and transistor size, so the results in this section applies to both of them.

5.1.1. Open-loop gain simulation

A_1 and A_2 have a DC open-loop gain of 111.3 dB at the ss corner and 99.8 dB at the ff corner, and the gain-bandwidth product is from 133 MHz to 149 MHz, as shown in figure 5.1.

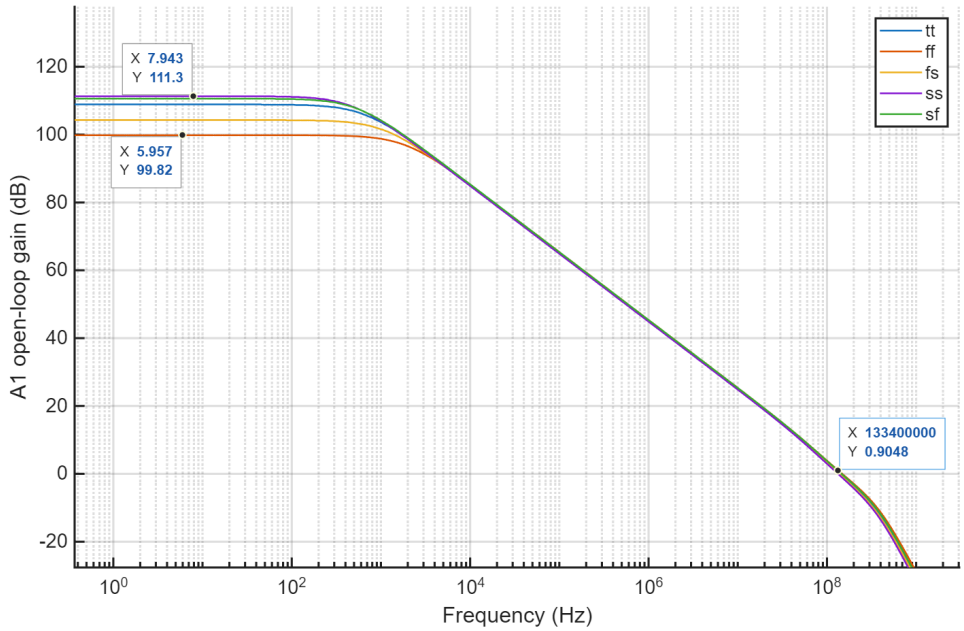


Figure 5.1: Open-loop gain of the main amplifiers

The open-loop gain and the bandwidth satisfy the design requirements determined in chapter 4.

5.1.2. Input offset voltage histogram

The test bench of input offset voltage of A_1 is shown in figure 5.2. It is measured at the differential output of A_1 when making the amplifier in unity gain feedback.

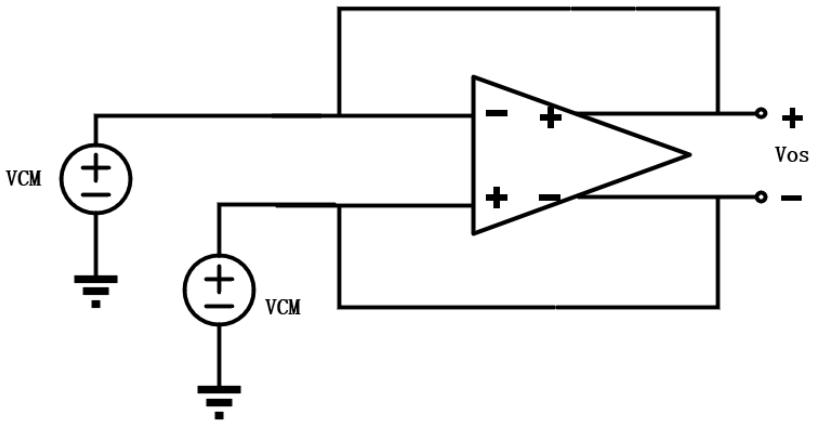


Figure 5.2: Test bench of input offset voltage of A_1

The histogram of the main amplifier input offset is shown in figure 5.3.

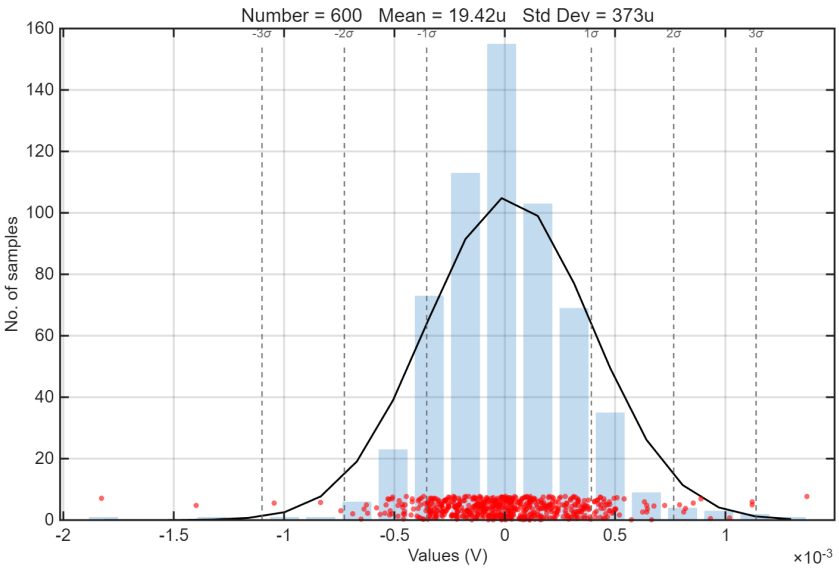


Figure 5.3: Histogram of the main amplifier input offset

The 3σ offset is +/-1.23 mV. Therefore, its input offset is modeled as +/- 1.23 mV in all the simulations.

5.2. Overall system simulation

In this section, the system performance is tested. First, the testing input signal V_i is defined. Then, the system input referred noise density is measured. Then the waveform and spectrum of output at V_{out} are plotted to show that the 10 kHz offset ripples are suppressed and the 20 kHz desired Hall signal are attenuated less than 3 dB. The test bench is shown in figure 5.4.

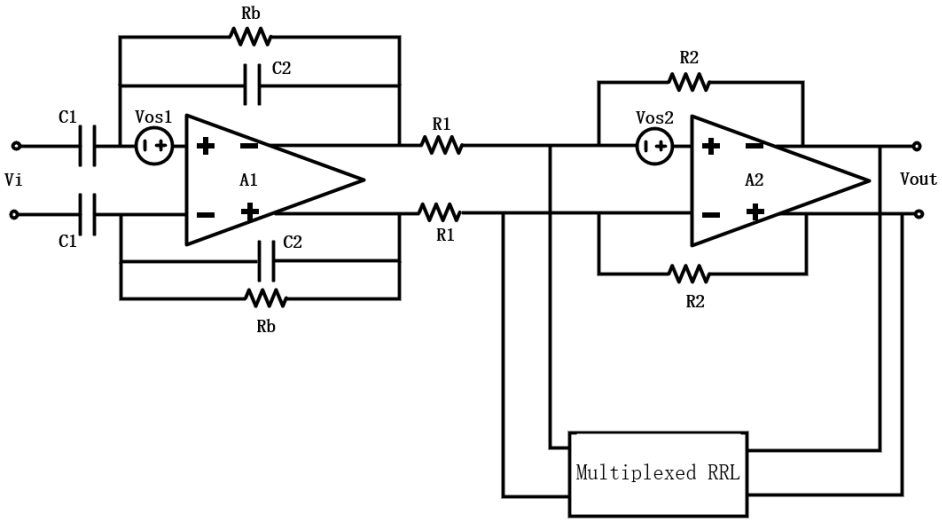
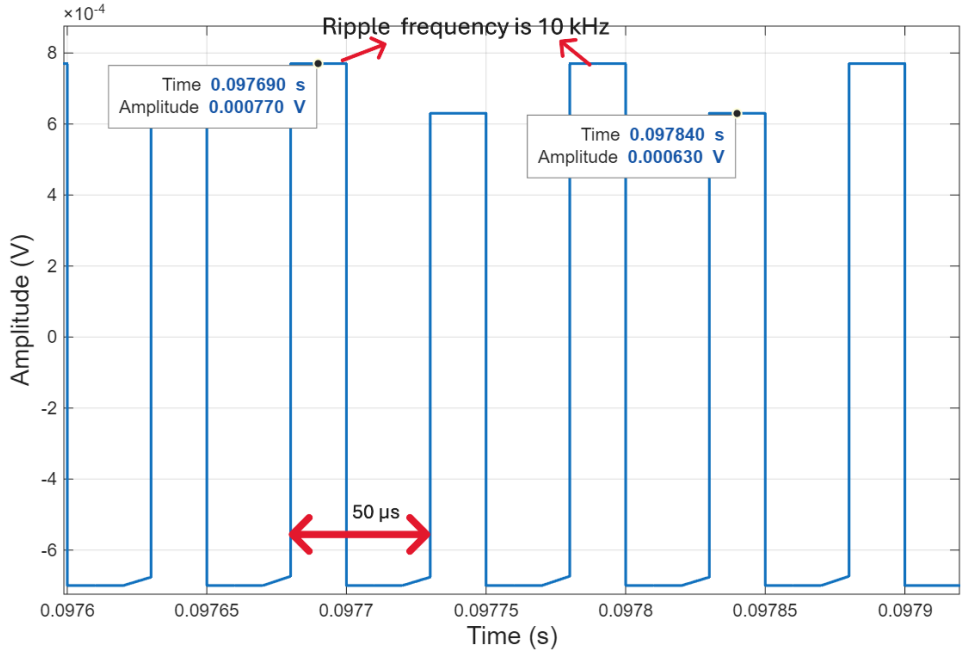


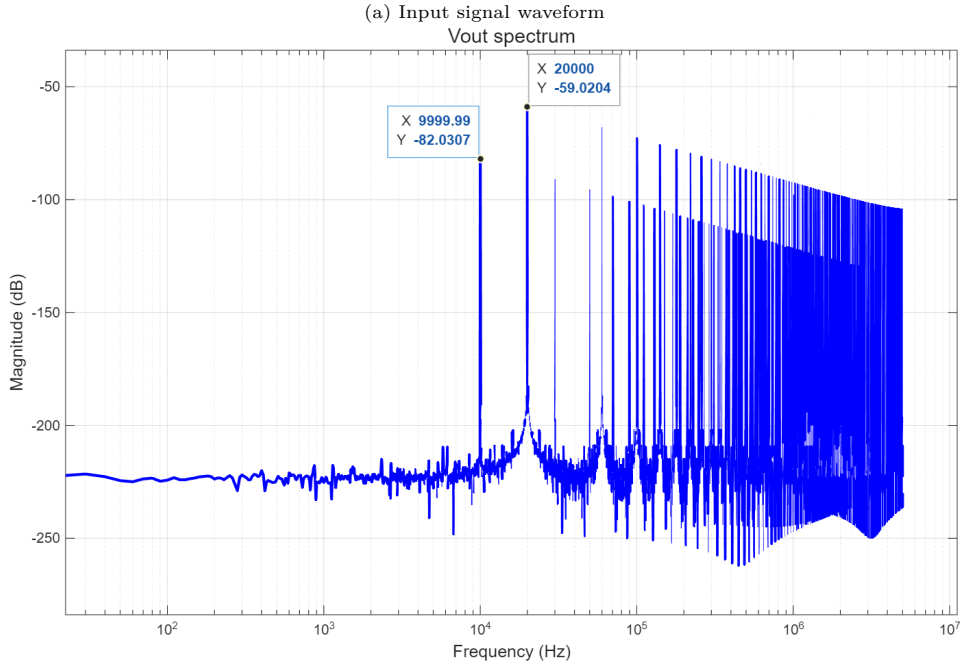
Figure 5.4: Overall system test bench

5.2.1. Input spectrum and waveform

The test input signal is the superposition of two 10 kHz offset ripples (35 µV and 36 µV), one 20 kHz offset ripple (16 µV) and the Hall voltage (700 µV). These values are given in section 4.1.4. The waveform and the spectrum is shown in figure 5.5.



(a) Input signal waveform



(b) Input signal spectrum

Figure 5.5: The waveform and the spectrum of the input signal

The 20 kHz component has a magnitude of -60 dB and the 10 kHz component has a magnitude of -82 dB.

5.2.2. Input noise voltage density

The input noise voltage density is measured at the system input V_i. It is designed to not exceed the Hall sensor thermal noise floor. The system input noise voltage density is shown in figure 5.6. The input noise voltages at the signal frequency 20 kHz are below 7.42 nV/$\sqrt{\text{Hz}}$.

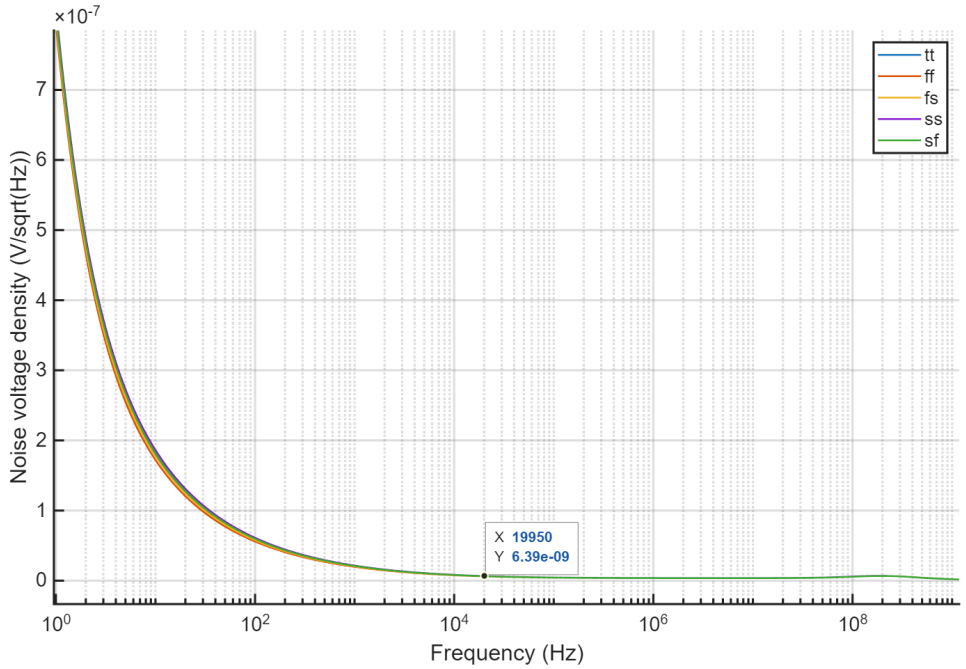


Figure 5.6: Input noise voltage density of 5 corners

The input integrated noise within the Hall signal bandwidth of 15 kHz - 25 kHz is shown in table 5.1.

Corner	Input integrated noise
ff	$6.10 \times 10^{-7}\ V_{\text{rms}}$
fs	$6.30 \times 10^{-7}\ V_{\text{rms}}$
sf	$6.42 \times 10^{-7}\ V_{\text{rms}}$
ss	$6.60 \times 10^{-7}\ V_{\text{rms}}$
tt	$6.38 \times 10^{-7}\ V_{\text{rms}}$

Table 5.1: Input integrated noise with Hall signal bandwidth for 5 corners

It can be seen that the input integrated noise within the signal bandwidth is lower than the 0.8 μV_{rms} resolution requirement.

5.2.3. Spectrum and waveform of A_2 output

After the main amplifiers and the RRL, the expected result is that the 20 kHz signal is amplified by 900 times (60 dB) to around 0 dB, and the 10 kHz component is amplified by 60 dB then suppressed by 35 dB reaching at around -57 dB. The simulated result is shown in figure 5.7 to figure 5.11.

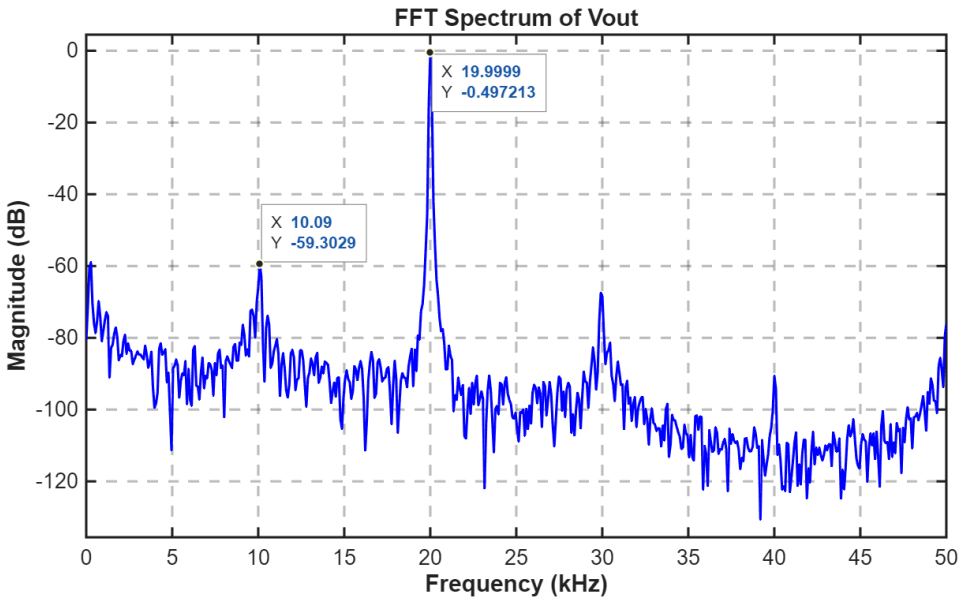


Figure 5.7: Spectrum of A_2 output for tt

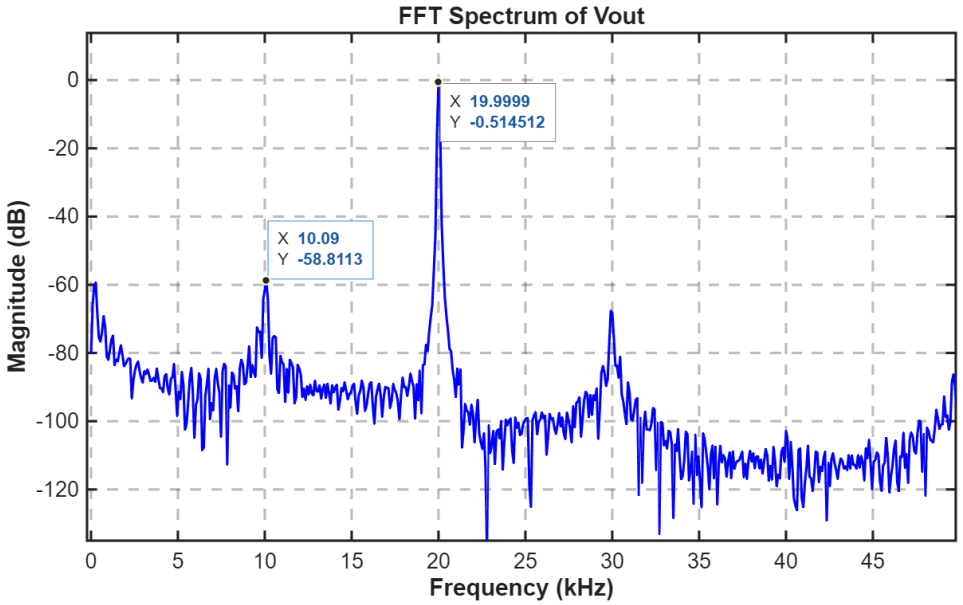


Figure 5.8: Spectrum of A_2 output for ff

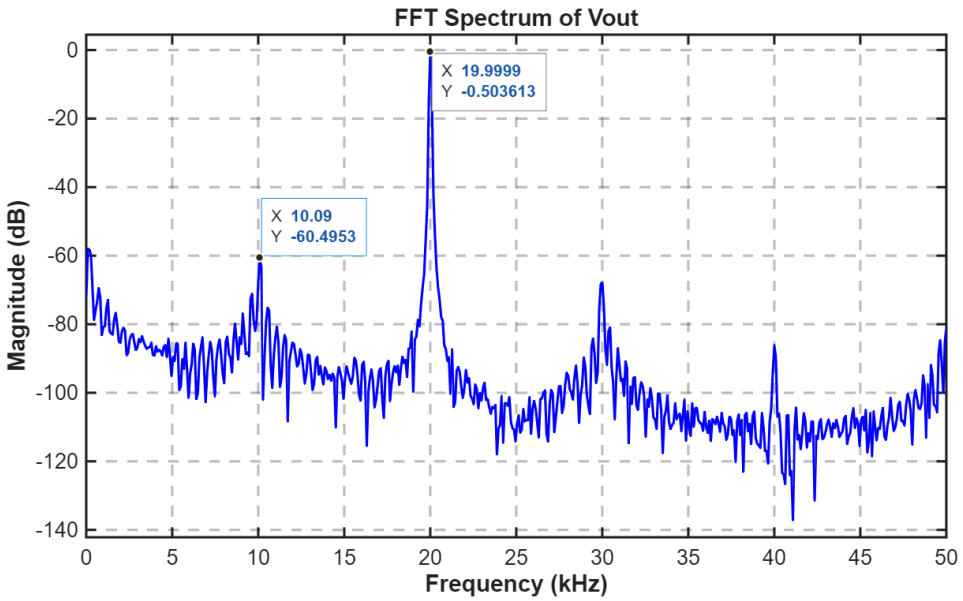


Figure 5.9: Spectrum of A_2 output for fs

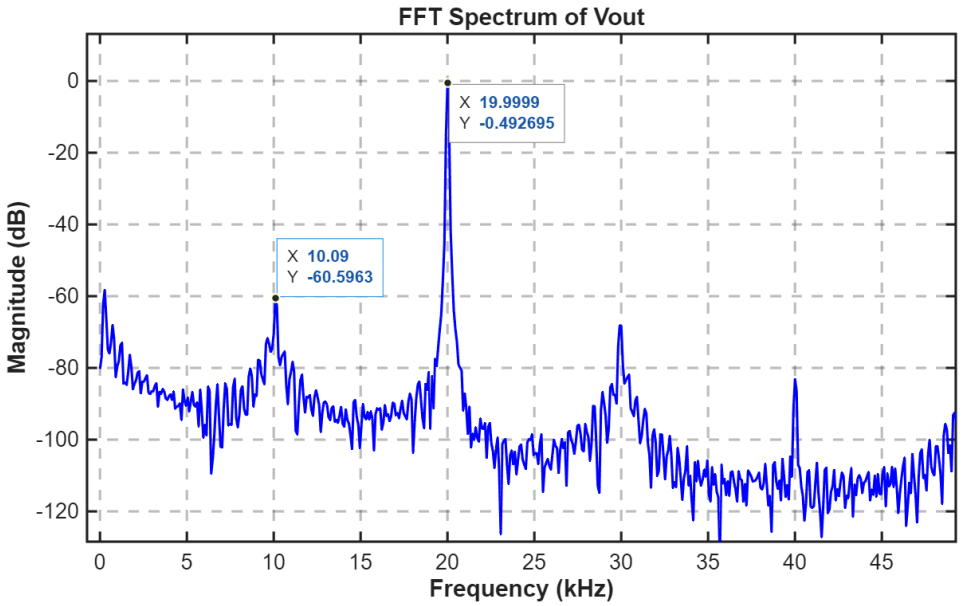


Figure 5.10: Spectrum of A_2 output for ss

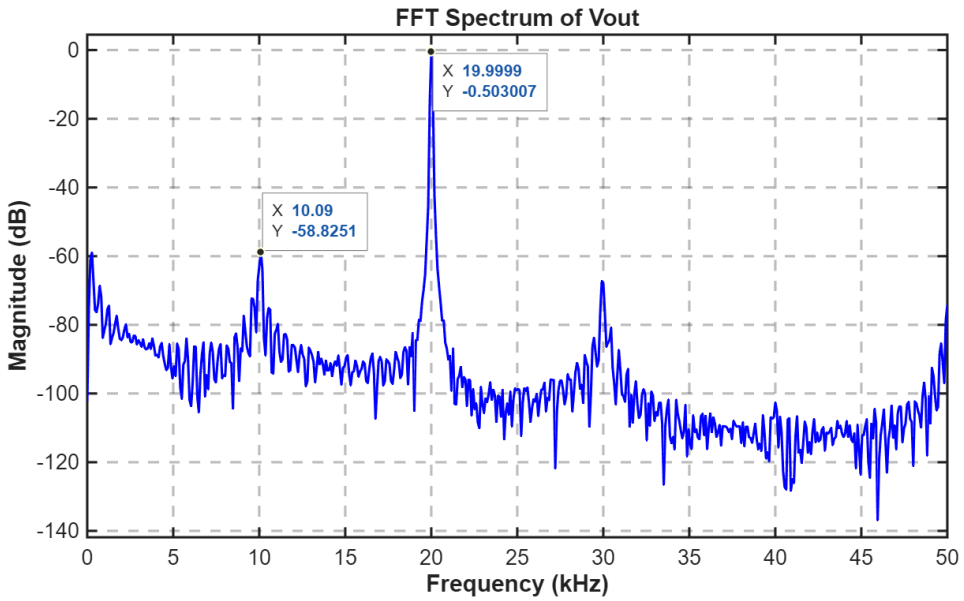


Figure 5.11: Spectrum of A_2 output for sf

From these plots of different corners, the 10 kHz components are suppressed to the magnitude from -60 dB to -58 dB, which are below -57 dB. Therefore, the RRL suppresses the 10 kHz ripples by at least 35 dB in all corners. The 20 kHz signal is amplified to the magnitude around 0.5 dB, which means the maximum signal loss less than 1 dB. The waveform at the output of A_2 is plotted in figure 5.12.

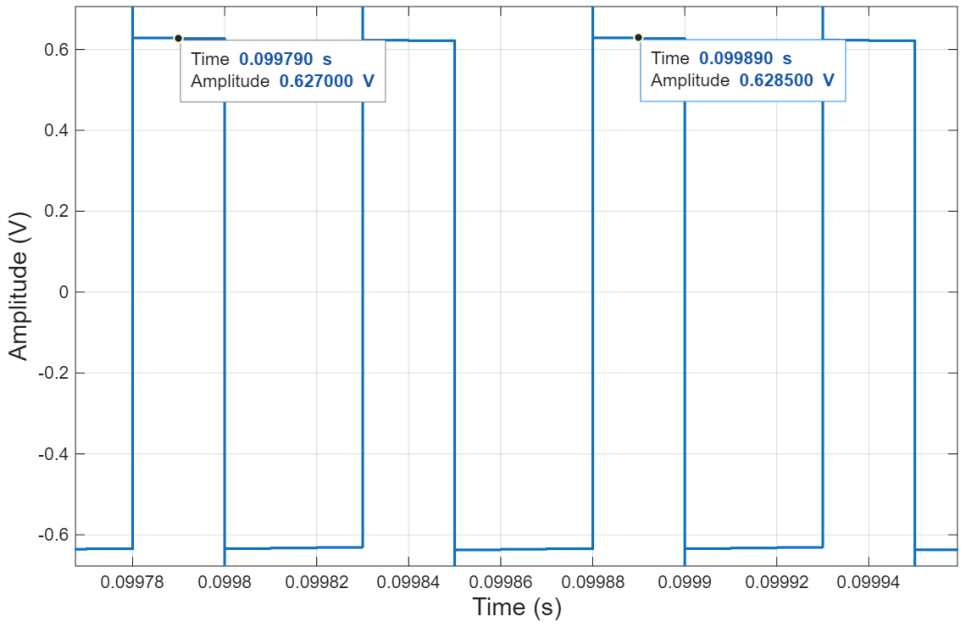


Figure 5.12: Waveform at the output of A_2

Compared with the input waveform of figure 5.5a, it can be observed that the 10 kHz ripples are much suppressed, and the 700 µV Hall signal is amplified to around 630 mV, which is within the design expectation.

The simulated result proves that the read-out circuit has basically completed its task of amplifying

the Hall signal and suppressing the Hall offset. The overall specifications of the final circuit and its comparison with two typical magnetic Hall sensor circuits are shown in table 5.2. From this table, it can be seen that the magnetic field range that this circuit can read is relatively wide, but the residual offset of the pyramid is much larger. Unlike the sensors with combined high frequency and low frequency paths[26], or the sensor with Hall and coil combined, this work has only one signal path. Thus this circuit is design to read only a 5 kHz bandwidth low frequency magnetic field.

	This work	[29]	[26]	[14]
Sensor type	Hall	Hall	Hall	Hall + Coil
Dynamic range (dB)	58	-	33[b]	54
Maximum input magnetic field (mT)	50[a]	10.8	12.5	2.07
Bandwidth (Hz)	5 k	-	400 k	5 M
Equivalent magnetic residual offset	1.01 mT	3.65 μT	40 μT	57 μT

Table 5.2: Performance comparison between this work and reported Hall sensor systems.
[a] Extrapolated. [b] Calculated with input range and resolution.

6

Conclusion

The thesis discusses the procedure of designing a read-out circuit for a novel 3-D Hall sensor. In the first chapter, an overview of 3-D Hall magnetic sensors and their working principle are given. Then a PCB characterization circuit is designed to measure the pyramid Hall sensor specifications. The characterization results are used to derive the requirements of the read-out IC design. Finally, the analog front-end of the read-out circuit is implemented in CMOS 180 nm process at transistor level in Cadence Virtuoso. It achieves an equivalent magnetic residual offset of 1 mT and a resolution of 0.47 μT with a highest operating magnetic field of 50 mT, thus exploring the possibility for pyramid Hall sensor of being current-spun and read out with an IC.

Though the circuit is proved to have the two basic functions we have summarized in chapter 4, its architecture can be improved. An alternative that can mitigate the influence of the amplifier offset is to use a capacitive coupling topology for the second main amplifier (A_2)[14]. By doing this , the offset of A_1 can be blocked, and the requirement of the RRL DC offset suppression can be relaxed. The crucial point of this structure is that the compensation current generated by the RRL can no longer be injected into the virtual ground of A_2, because the offset ripples now are not square waves but spike voltages. But the differential input voltage at the A_2 virtual ground is still a square wave, so is the drain current of A_2 input transistors. Therefore, one possible solution is to inject the compensation current to a node inside A_2 using an auxiliary input stage where the ripple is a square wave current.

Finally, some future work on this project can be carried out. First, in this thesis, the current spinning switches and the Hall sensor biasing source are not implemented in transistor level but on PCB instead. Though the pyramid sensor is not yet CMOS compatible, it has the potential to be fabricated with a flip chip and integrated with the biasing sources and the spinning switches. Second, the sensor performance in different temperatures is not yet characterized. If this part of data can be obtained, the design of the read-out IC will also change to satisfy different temperatures. Lastly, the layout and post-layout test of the read-out IC can be carried out to see how the circuit specifications are affected by the parasitic factors.

7

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A

Appendix-a

This part shows the schematic of each PCB sub-circuit in Altium Designer.

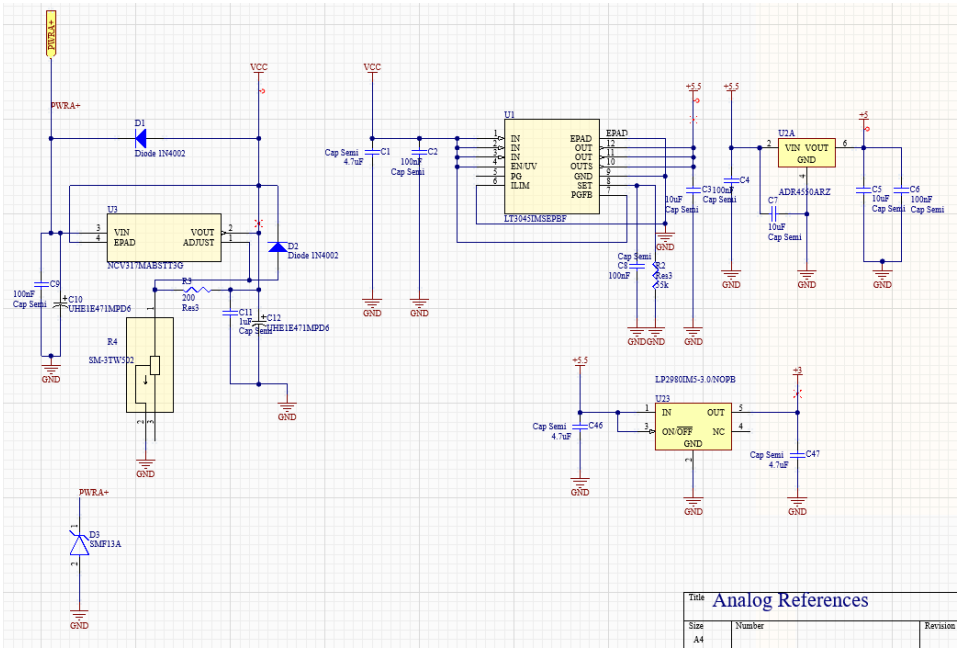

Figure A.1: Analog power supply

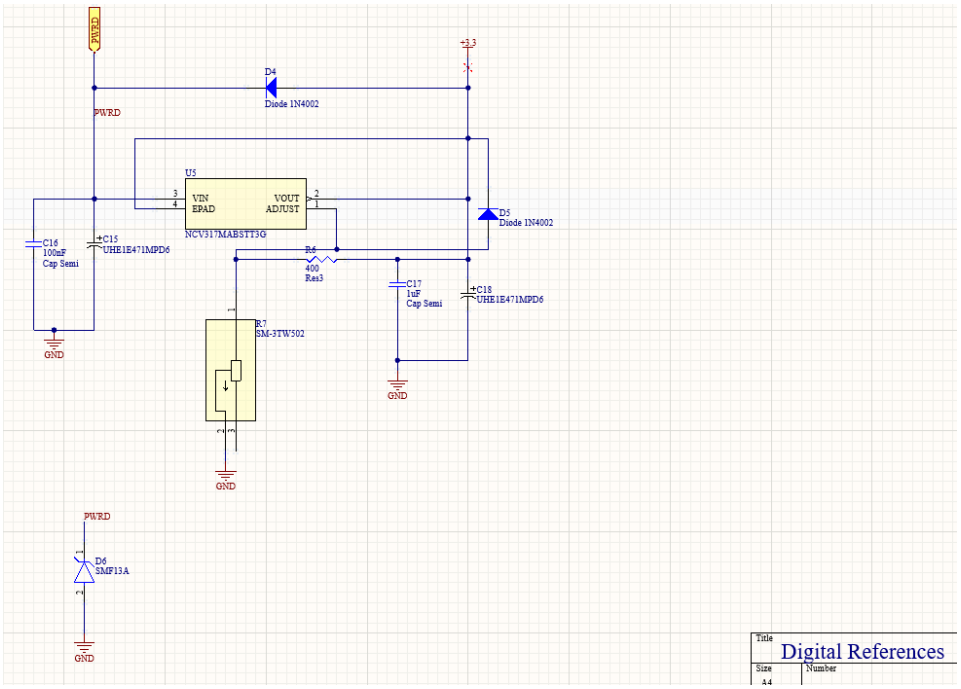

Figure A.2: Digital power supply

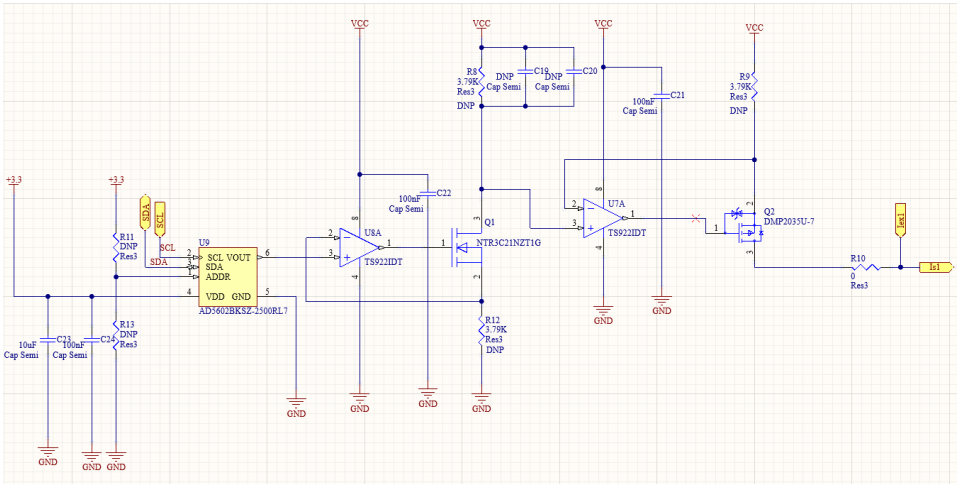

Figure A.3: Biasing current source

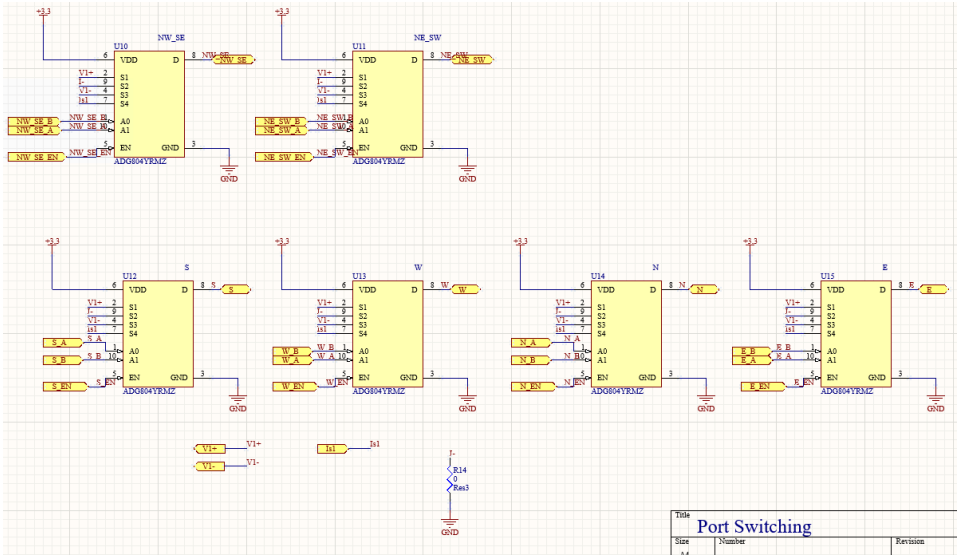

Figure A.4: Current spinning switch matrix

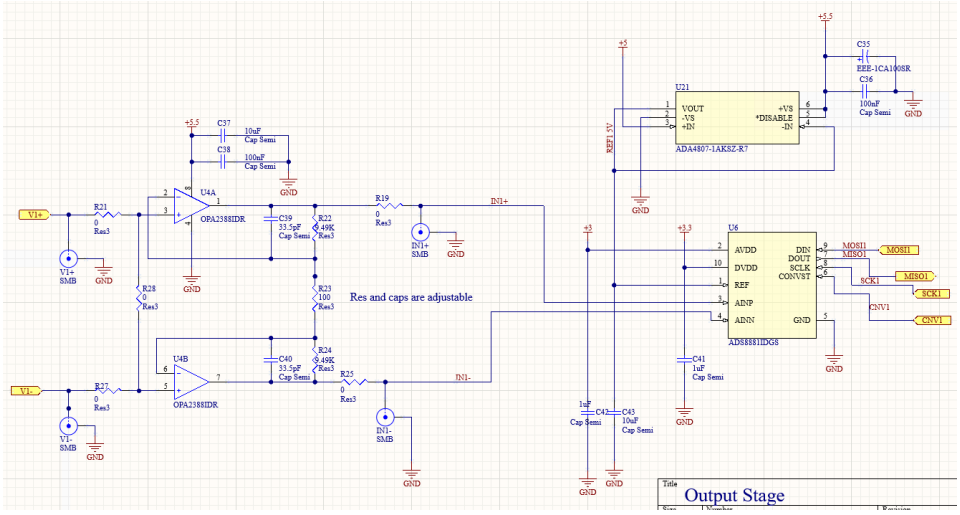

Figure A.5: Output stage

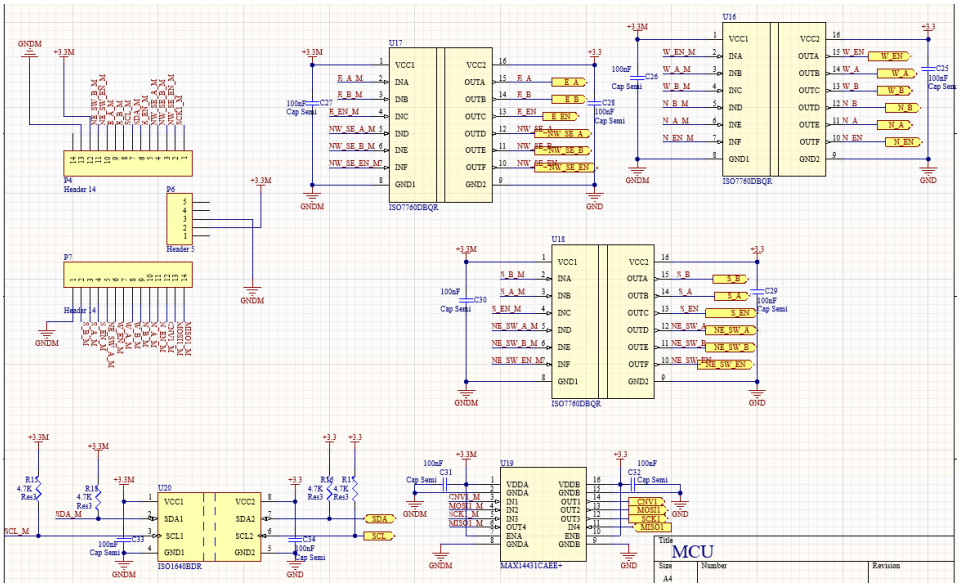

Figure A.6: MCU and isolators

B

Appendix-b

This part gives the simulation results of the output of the LPF. This is the result after down-modulating the Hall signal and low-pass filtering the other components. The desired DC Hall voltage is labeled with a dashed line in the plots. The offset ripples are suppressed further than that in the output of A_2, and the DC components in the main path is up-modulated to 20 kHz and suppressed. The test bench is shown in figure B.1.

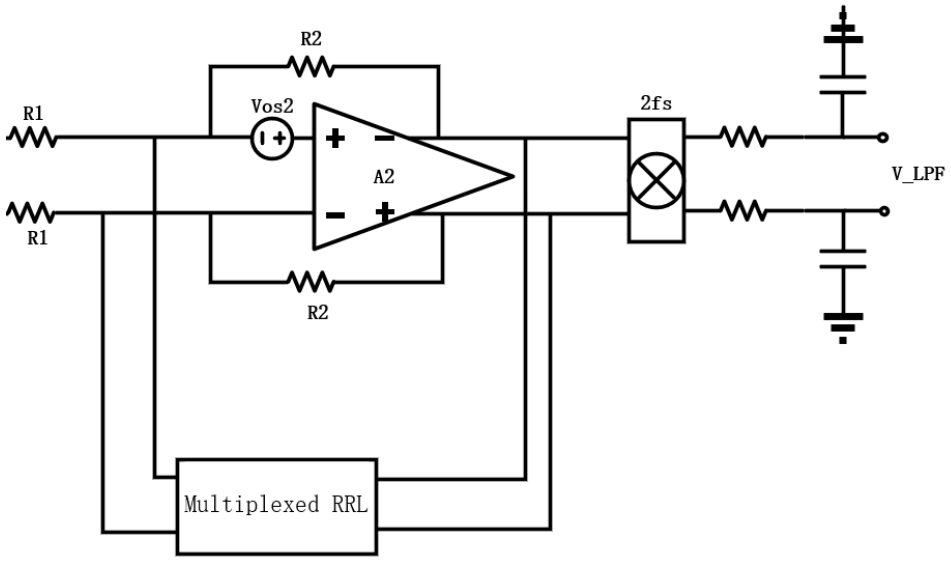

Figure B.1: Test bench with an output LPF

The simulated LPF output spectrum is shown in figure B.2 to figure B.6.

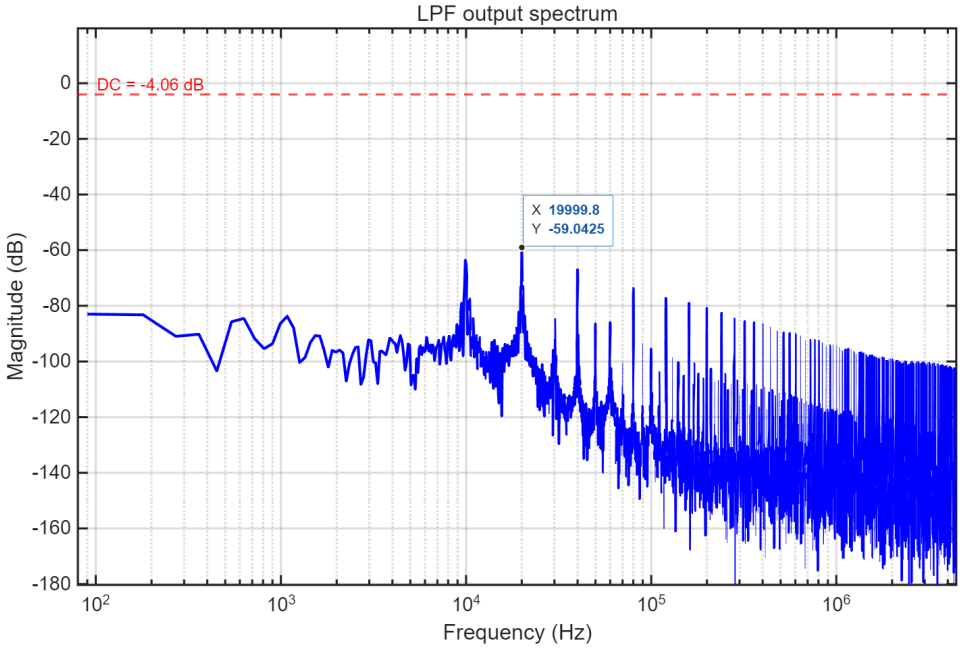

Figure B.2: Spectrum of LPF output for tt

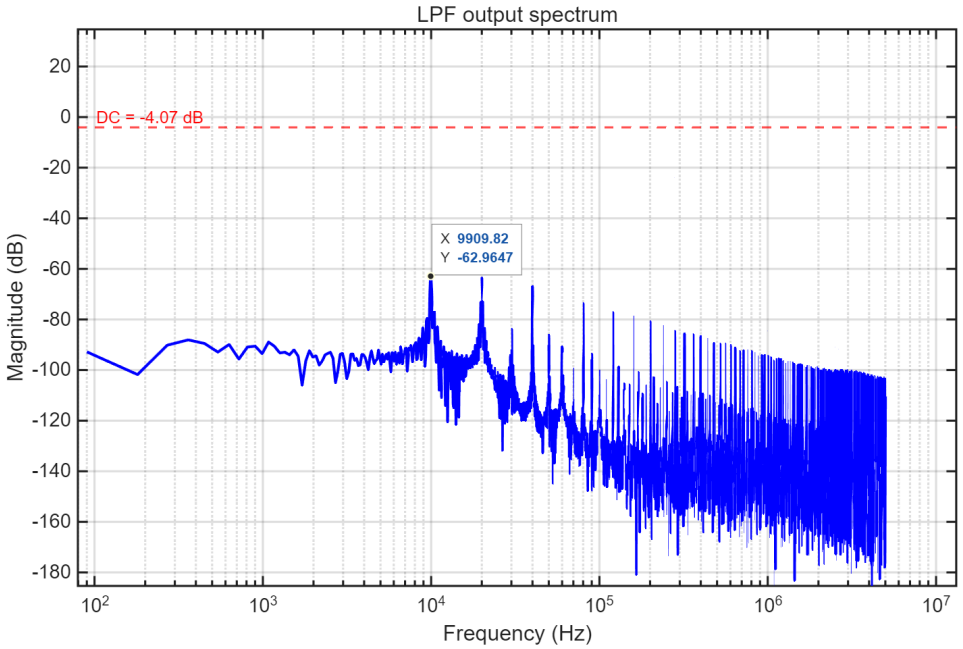

Figure B.3: Spectrum of LPF output for ff

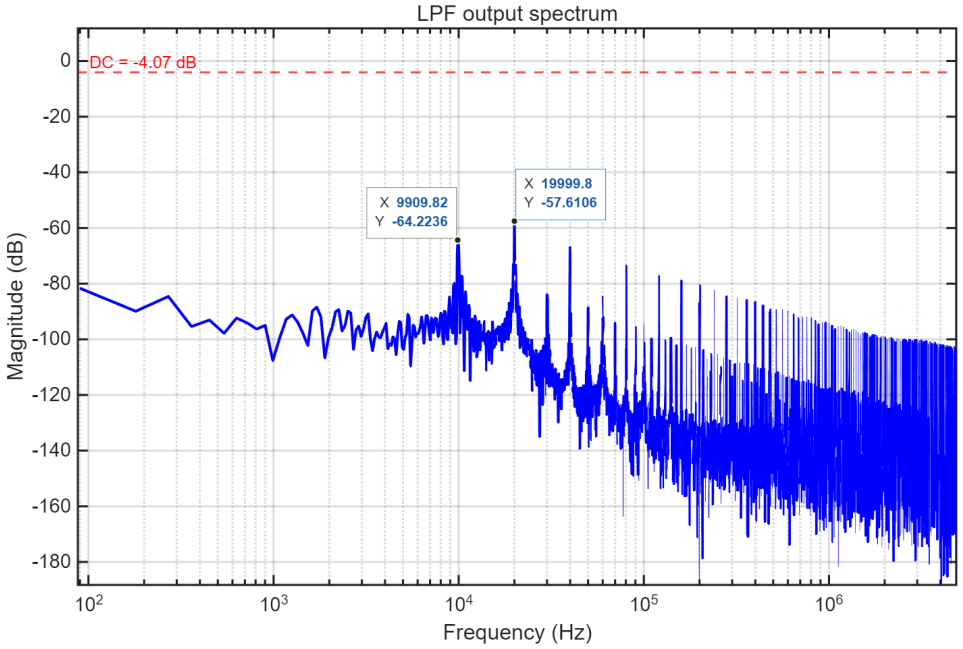

Figure B.4: Spectrum of LPF output for fs

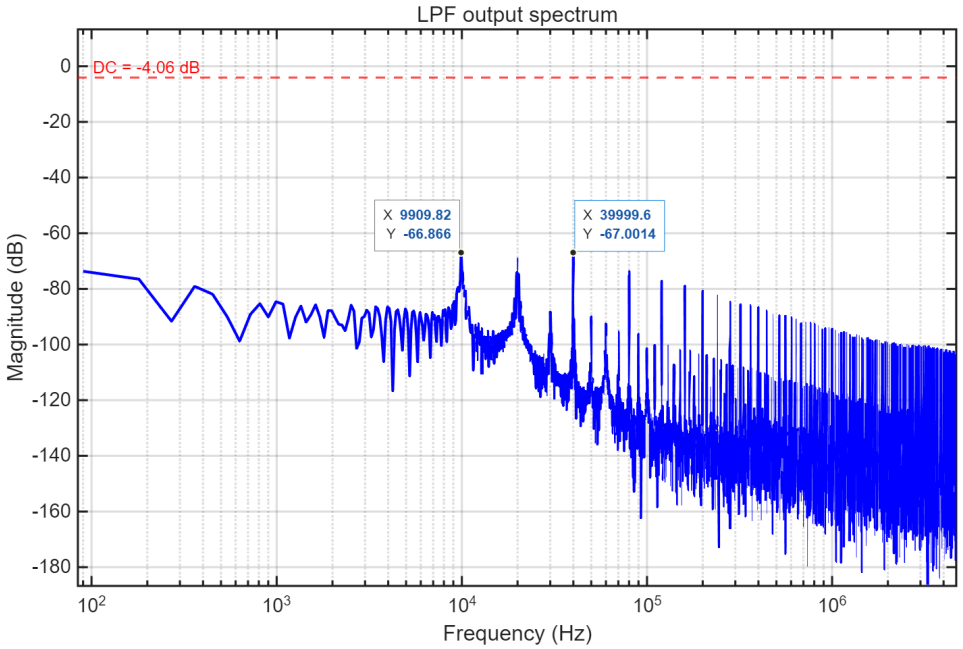

Figure B.5: Spectrum of LPF output for ss

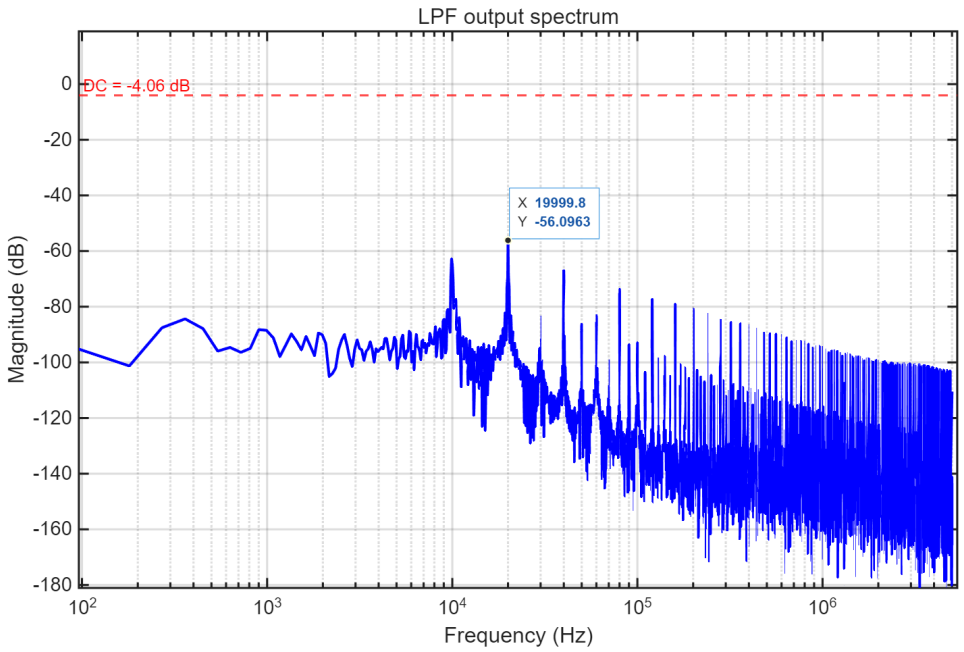

Figure B.6: Spectrum of LPF output for sf

C

Appendix-c

This appendix gives the estimation of the flicker noise corner frequency using the Hooge model:

$$S_{vf}^2 = V_{\text{supply}}^2 \frac{\alpha_H}{N} \frac{1}{f^\gamma} \tag{C.1}$$

The 1/f noise can be modeled as a linear equation: y = b + ax, which is derived by taking the logarithm of both sides of the Hooge equation. Thus, the factor b is approximately equal to the y-axis intercept of the curve in figure 3.2, while $-\gamma/2$ is the curve slope. The estimated factors for 200 μA biasing current are shown in the table below.

	Edge bias 1.2 V	Corner bias 0.8 V
γ	1.29	0.82
α_H/N	1.08×10^{-11}	1.43×10^{-13}

Table C.1: Extracted flicker-noise parameters under different bias conditions