An energy-efficient BJT-based temperature sensor with a continuous-time readout

By

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Abstract

This thesis presents an energy-efficient high-accuracy temperature sensor that combines a BJT front-end with a continuous-time readout circuit. Its front-end is based on PNP transistors, which, compared to NPNs, are more widely available in CMOS processes and less sensitive to stress. In this design, proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) currents are created by forcing ΔV_{BE} and V_{BE} over two resistors of the same type, after which their ratio is digitized by a continuous-time Delta-Sigma Modulator (CTDSM). As a result, the sampling noise present in traditional switched-capacitor (SC) modulators is eliminated, which improves the sensor's energy efficiency. High accuracy is achieved by the liberal use of chopping and dynamic element matching techniques. Fabricated in a 0.18µm CMOS process, the sensor achieves a 0.15°C (3σ) inaccuracy over the industrial temperature range (-45°C to 85°C) after a 1-point temperature calibration. It also achieves a 1.24mK resolution in 56.3ms, while consuming only 16µW. This corresponds to a state-of-the-art resolution Figure-of-Merit (FoM) of 1.4pJ°C^2.

Acknowledgments

While looking back to when I first started working on this project, it is impossible to ignore the amount of support and contribution I received, without which I would not have been where I am today. There are a number of people I would like to thank for this incredible learning experience.

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1 Introduction

Temperature sensors are widely used in many applications, such as medical devices and high accuracy frequency references. Recently, integrated temperature sensors, especially those realized in CMOS technologies, have gained great popularity due to their small size, low cost, and digital output. In general, a CMOS temperature sensor should be designed to achieve a specified accuracy over the specified temperature range. This must be achieved at a low production cost, meaning as little temperature calibrations as possible. Also, it should achieve high resolution while consuming as little power as possible in a specified conversion time.

1.1 Types of CMOS temperature sensors

Several different types of temperature sensors can be realized in standard CMOS processes. BJT-based temperature sensors rely on voltages created by two BJTs biased at a non-unity collector current density ratio. As will be explained in the following sections, the base-emitter voltage (V_{BE}) of a single BJT is complementary-to-absolute-temperature (CTAT), while the base-emitter voltage difference (ΔV_{BE}) is proportional-to-absolute-temperature (PTAT). The temperature can then be read out by combining the two signals. Although the sensor's energy efficiency is limited by the low temperature sensitivity of ΔV_{BE}, high accuracy (<0.1°C) over a large temperature range (>100°C) can be achieved with a low-cost single-point trim [1].

Resistor-based temperature sensors rely on the temperature dependence of on-chip resistors. Compared to BJTs, their higher sensitivity to temperature (up to 0.4%/°C) allows them to achieve much higher (one or two orders of magnitude) energy efficiency [2]. However, they typically require a two-point calibration to achieve good accuracy, which increases their production cost [3].

When biased in the subthreshold region, the temperature dependency of MOSFETs is similar to that of BJTs. They can operate at the low supply voltages used in modern CMOS technologies and can achieve higher energy efficiency. However, due to the large spread of gate-oxide thickness and channel doping, such sensors typically require a two-point temperature calibration to achieve good accuracy [4].

Electro-Thermal Filters (ETFs) sense the well-defined and temperature-dependent thermal diffusivity of silicon. A heating element creates temperature fluctuations in the substrate of a chip, whose phase shift when measured at a well-defined distance is a function of temperature. Due to precise lithography and the high purity of silicon in modern CMOS technologies, such sensors can achieve high accuracy without any trimming [5, 6]. However, they require a power-hungry heater, which significantly lowers their energy efficiency.

Of all these sensors, BJT temperature sensors are the most widely used, mainly due to their desirable balance between energy efficiency and accuracy. The current state-of-the-art

inaccuracy for a BJT temperature sensor is ±60mK from -70°C to 125°C after one temperature calibration [7].

As most precision sensors are limited by thermal noise, a trade-off exists between energy and resolution. This trade-off is quantified by the resolution Figure-of-Merit (FoM), which is defined as the amount of energy used for a conversion multiplied by the achieved resolution squared [8]. The best (lowest) FoM that has been achieved for a high-accuracy BJT-based temperature-to-digital converter (TDC) is 5.4pJ°C [9].

The goal of this project is to achieve state-of-the-art energy efficiency while maintaining an inaccuracy that is competitive to earlier BJT temperature sensors. The previously mentioned sensors set the benchmark for the proposed TDC.

1.2 Working principle of BJT-based temperature sensors

In general, the sensor core of a BJT-based temperature sensor consists of two diode-connected BJTs, as shown in Figure 1.1. The base-emitter voltage of a BJT with $I_C >> I_S$ can be expressed as:

$$V_{BE} \approx \frac{k_b T}{q} \ln\left(\frac{I_C}{I_S}\right) \tag{1.1}$$

Where k_b is the Boltzmann constant (1.38×10^{-23} J/K), T is the absolute temperature in °K, and q represents the electron charge (1.6×10^{-19}C). I_C and I_S represent the collector current and the saturation current flowing through the transistor, respectively. Because the saturation current increases exponentially with temperature ($I_S \sim T^4$), V_{BE} decreases with a slope of ≈-2mV/°C as temperature increases, and therefore it is CTAT.

When biased at different current densities, the difference between the base-emitter voltages of these two BJTs can be expressed as:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{k_b T}{q} \ln(pr) \tag{1.2}$$

Where p is the collector current ratio and r is the emitter area ratio between the two BJTs. As a result, ΔV_{BE} is a well-defined voltage that is PTAT. In other words, ΔV_{BE} can be used as an accurate measure of absolute temperature. As shown in Figure 1.1, by amplifying ΔV_{BE} and combining it with V_{BE}, a temperature-constant reference voltage V_{ref} is created [10], which can be used by an ADC to digitize the amplified ΔV_{BE}, thus generating a temperature-linear digital output μ:

$$\mu = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} = \frac{\alpha \Delta V_{BE}}{V_{ref}} \tag{1.3}$$

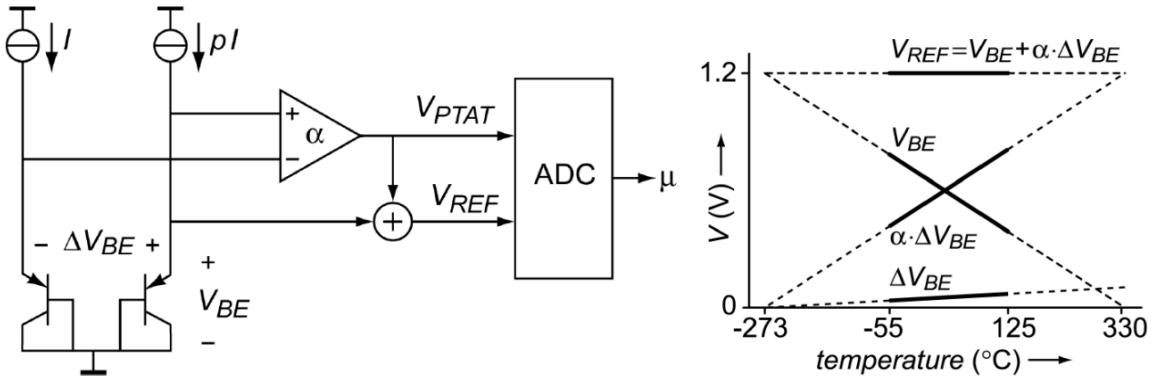


***Figure 1.1**: A block diagram of a BJT-temperature sensor (left), a plot showing how the temperature-independent V_{ref} is created (right) (retrieved from [11]).*

In temperature sensors, vertical BJTs are preferred over lateral BJTs, since lateral BJTs inevitably have a parasitic junction to the substrate, which results in a non-ideal V_{BE}-I_C behaviour [11]. In deep N-well technologies, both vertical PNPs and NPNs are available. In contrast to NPNs, PNPs offer a smaller but more constant current gain β, making it easier to compensate for the resulting error in I_C. Furthermore, vertical NPNs are not available in all technologies, and are more sensitive to mechanical stress.

1.3 Prior-art of BJT-based temperature sensors

Traditionally, BJT-based temperature sensors used switched-capacitor Delta-Sigma Modulators (SC-DSMs) to digitize the ratio of the voltages created in the analog front-end. Since the front-end voltages (V_{BE} and ΔV_{BE}) only need to be accurately settled at the sampling moment, and the ratio of the sampled voltages can be made quite accurate by applying Dynamic Element Matching (DEM) to the DSM's sampling capacitors, such designs can achieve excellent accuracy (0.1°C inaccuracy from -55 to 125°C) after a one-point calibration [1]. However, their resolution is limited by the kT/C noise of the sampling capacitors, while the power of the readout circuit is limited by the settling requirements of the SC integrator.

To improve the energy efficiency of these types of SC designs, the power dissipated by the readout circuit needs to be minimized. A state-of-the-art design [7], uses an efficient zoom ADC architecture [12] to achieve a resolution FoM of 7.8pJ°C^2. After applying various dynamic techniques, it also achieves a state-of-the-art inaccuracy of 0.06°C from -70°C to 125°C.

On the other hand, BJT sensors based on continuous-time readout circuits have a better theoretical energy efficiency. As no sampling takes place, kT/C noise, which is the major noise contributor of discrete-time designs, can be eliminated. In [13], an early continuous-time TDC was proposed. It converts the PTAT and CTAT voltages in the analog front-end to currents using V-to-I converters, which are balanced by the CTDSM, as illustrated in Figure 1.2. Although impressive at the time, the relatively complex readout circuit led to an 11nJ°C^2 FoM, which leaves a lot of room for improvement. Moreover, the sensor's inaccuracy (0.5°C from -50 to 120°C) is limited by resistor mismatch and its non-ideal trimming method.

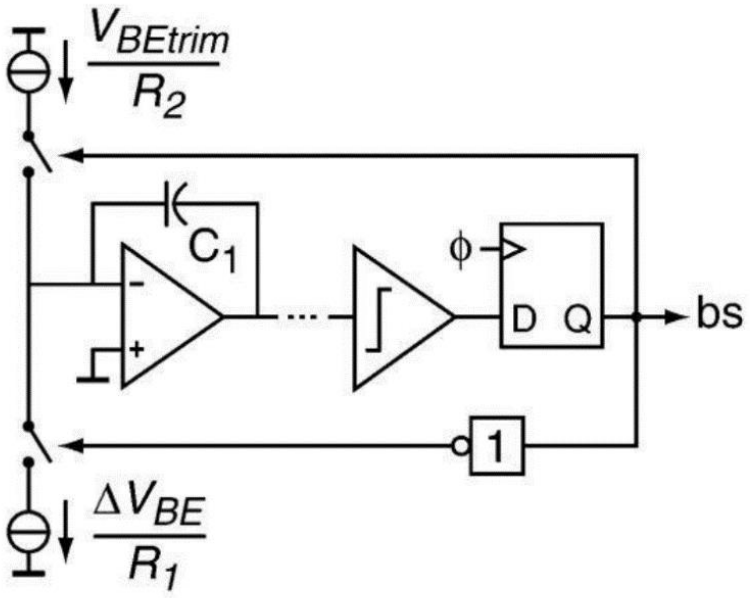


Figure 1.2: *Block diagram of a CT readout circuit for a BJT temperature sensor (retrieved from [11]).*

Another early instance of a high accuracy, continuous-time BJT temperature sensor is [14]. It balances two currents with opposite temperature dependencies against each other with the help of an integrator and a Schmitt trigger, whose output is a duty-cycle modulated signal. By adjusting the temperature dependencies of the two currents, the dynamic range of the duty-cycle output can be designed to vary by 80% instead of 30% over the industrial temperature range. The sensor achieves a FoM of 3.6pJ°C^2, and a 1-point trimmed inaccuracy of 0.15°C from -45°C to 130°C. Due to its duty-cycle output, however, this sensor is not strictly a temperature-to-digital converter, and a high-frequency counter is needed to digitize its output.

Another way to achieve a highly efficient CT-BJT sensor is by using a Capacitively-Coupled Instrumentation Amplifier (CCIA) to amplify ΔV_{BE} [9]. As shown in Figure 1.3, the CCIA efficiently boosts ΔV_{BE}, while the use of an NPN front-end topology eliminates the need for a biasing opamp. In theory, this design should be as accurate as SC designs, since the gain of a CCIA is also set by a capacitor ratio. In addition, the CCIA's relatively high input impedance relaxes the loading of the BJT front-end. However, its NPN front-end is more sensitive to stress, and the CCIA's gain error limits the sensor's accuracy and had to be calibrated [15]. This work achieves a 5.4pJ°C^2 FoM, which was the state-of-the-art efficiency for a BJT-based TDC at the time it was published, and a 0.13°C inaccuracy from -40°C to 125°C.

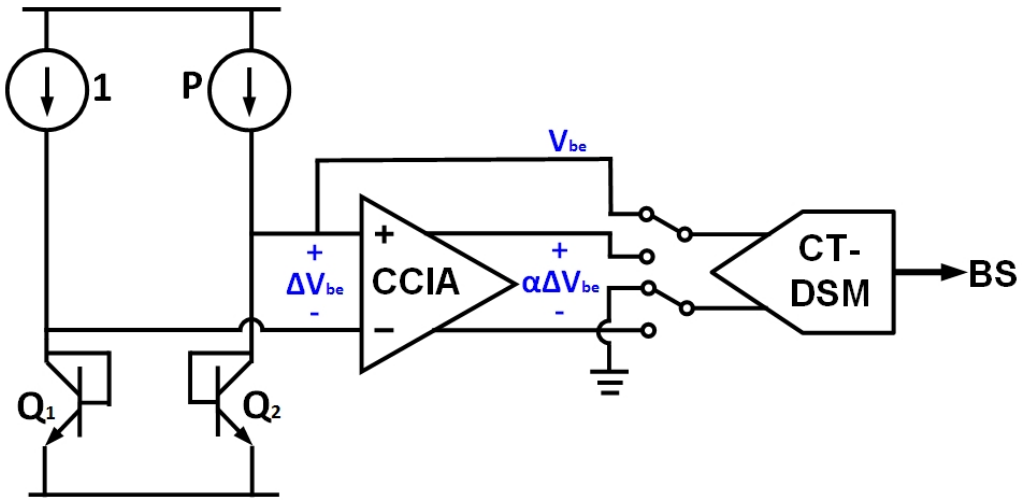


***Figure 1.3**: Block diagram of the topology used in [9].*

More recently, another BJT temperature sensor utilizing a very simple, continuous-time readout was proposed [16], as shown in Figure 1.4. Realized in a 16nm FinFET technology, the PTAT and CTAT voltages are generated by NPNs biased at 1:8 emitter area ratio, which an opamp converts into currents flowing through an integration capacitor. As in [14], a Schmitt trigger drives a resistor-DAC that balances the integrated current, resulting in a temperature-dependent duty-cycle modulated output signal. This simple circuit can function at the low supply voltage used in advanced CMOS technologies while occupying little area. The circuit achieves a non-trimmed inaccuracy of 1.56°C and a FoM of 8.3pJ°C^2.

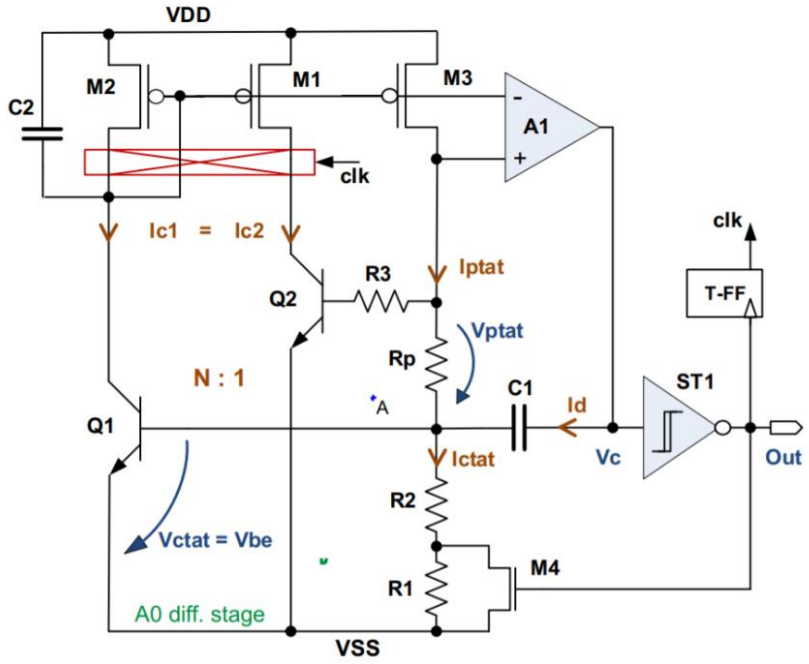


***Figure 1.4**: Circuit diagram of the topology used in [16].*

Another CT design based on PTAT and CTAT current balancing was proposed in [17], as shown in Figure 1.5. It employs a large emitter area ratio of 24 to improve the PTAT current sensitivity. Meanwhile, the CTAT current is generated as $I_{CTAT}=V_{BE}/R_{\Delta VBE}-V_{gp}/R_{\Delta VBE}$, in which the second term is PTAT, which increases the sensor's temperature sensitivity. The sensor

achieves a state-of-the-art 190fJ°C^2 FoM. However, the design is also based on stress-sensitive NPN transistors, and its inaccuracy is limited by the matching of multiple resistors (4) and BJTs (3). As a result, the sensor requires a multi-point temperature calibration to achieve good accuracy, which significantly increases production costs.

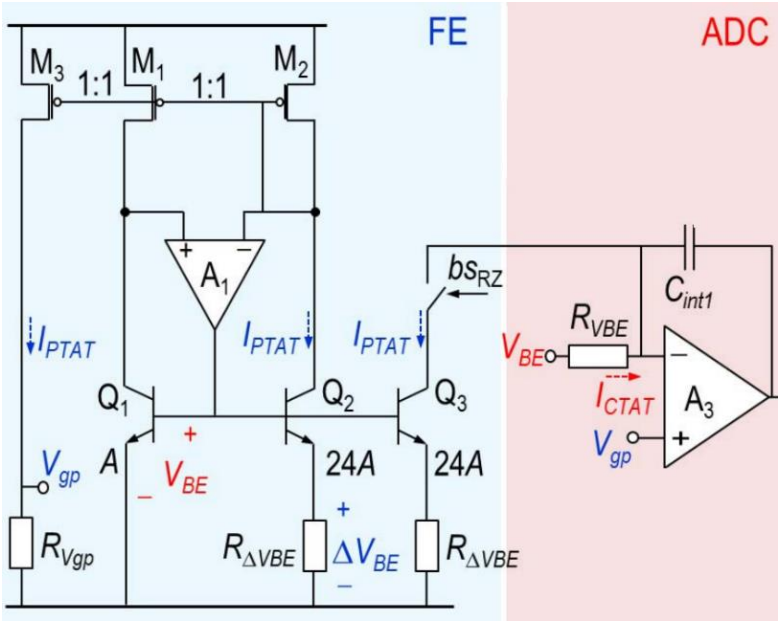


***Figure 1.5**: Diagram of the circuit used in [17].*

Table 1.1 summarizes the performance of the various state-of-the-art BJT-based temperature sensors described above. This table will be used as a benchmark for the performance achieved by this work.

	JSSC'17 [7]	CICC'21 [18]	ISSCC'14 [14]	ASSCC'19 [9]	ISCAS'21 [16]	ISSCC'20 [17]
Sensor type	PNP	PNP	PNP	NPN	NPN	NPN
Architecture	DTΔΣM	DTΔΣM	DCM	CTΔΣM	DCM	CTΔΣM
Technology	0.16µm	55nm	0.7µm	0.18µm	0.016µm	0.11µm
Supply current [µA]	4.6	2.2	55	5.5	30	550
Supply voltage [V]	1.5 to 2	1	2.9 to 5.5	1.6 to 2.2	0.95 to 1.15	1.125
Temperature range	-55°C to 125°C	-55°C to 125°C	-45°C to 130°C	-40°C to 125°C	-30°C to 130°C	-35°C to 95°C
3σ Inaccuracy [°C] after a 1-pt trim	±0.06	±0.77	±0.15	±0.13	±1.56*	-
Resolution FoM [pJ°C2]	7.8	3.1	3.6	5.4	8.3	0.19

*Non-trimmed inaccuracy

***Table 1.1**: Performance summary of prior-art BJT temperature sensors*

The goal of this project is to realize a PNP-based CT temperature sensor with state-of-the-art resolution FoM while maintaining high accuracy (<0.2°C) after a 1-point trim over the industrial temperature range (-45°C to 85°C). This temperature range was chosen to facilitate a head-to-head comparison with the results of the design described in [17].

1.4 Organization of the thesis

The rest of the thesis is structured as follows. In chapter 2, the proposed architecture is introduced. Furthermore, the system-level design considerations to achieve high energy efficiency and accuracy are discussed.

In chapter 3, the circuit-level implementation of the sensor is presented. This is divided into 2 main blocks: The BJT front-end and the DSM. Afterward, an analysis of the simulated power and noise is done, along with a description of the signal timing.

Chapter 4 will illustrate the various measurement results that were obtained from the chip. After the measurement setup is described, the resolution, power consumption, power supply sensitivity, and inaccuracy are presented.

Lastly, chapter 5 contains the conclusion of the project and a discussion about possible future work.

2 Architecture considerations

Since achieving both high energy efficiency and good accuracy in a TDC is no trivial task, careful considerations must be made before starting the circuit design. This chapter discusses the architectural considerations that influence the design choices made in the implementation of the individual blocks of a TDC.

2.1 Proposed architecture

In the previous chapter, various energy-efficient TDCs were discussed. It was concluded that designs with CT front-ends can achieve high energy efficiency while still maintaining competitive accuracy. In this work, a new architecture, which consists of a minimalistic PNP-based front-end and a CT-DSM, is proposed.

The basic aim of the new architecture is to balance currents that are proportional to ΔV_{BE} and V_{BE} with the minimum number of resistors and amplifiers. As shown in Figure 2.1, a PTAT current $\Delta V_{BE}/R_{PTAT}$ is readily available in a regular BJT front-end, and this can easily be mirrored to the integrator of the DSM. If V_{BE} is applied to the non-inverting terminal of the DSM's integrator, it will be copied to the inverting terminal. A resistor R_{CTAT} placed between the inverting terminal and ground, will then draw a CTAT current V_{BE}/R_{CTAT}, which can then be balanced by the PTAT current $\Delta V_{BE}/R_{PTAT}$. The resulting structure is similar to that described in [16], although in that circuit the accuracy of the PTAT current is limited by the finite current gain of the BJTs, and four resistors are used to generate a duty-cycle output.

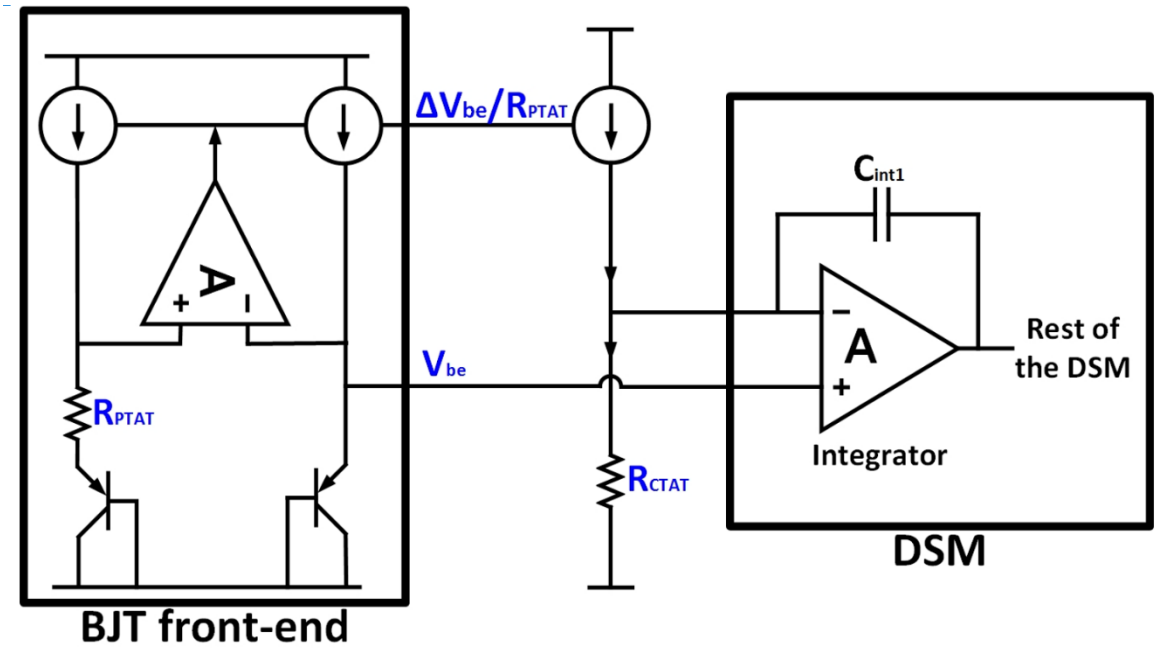


***Figure 2.1**: Simplified diagram of the proposed readout circuit.*

When compared to the design in [14], one less amplifier is required to create V_{BE}/R_2, meaning that power, noise, and area will be reduced. Although the design in [17] uses a similar topology, it relies on the matching of four different resistors, meaning that the proposed design, which only relies on the matching of two resistors, should, in principle, achieve better accuracy.

To regulate the average integrator input current to zero via the DSM's bitstream output, an IDAC is required. Two options are possible: a resistive DAC and a current DAC, as shown in Figure 2.2.

A resistive DAC can be realized by adding a properly scaled resistor R_{CTAT}/x in series or parallel with R_{CTAT} [16], where the 'x' factor needs to be chosen so that the input range of the DSM is properly utilized over the desired temperature range. This resistor is preferably located in parallel with R_{CTAT} and can be connected or disconnected by a switch connected to ground.

A current DAC, which regulates the amount of PTAT current that will flow into the DSM, can be realized by using PMOS current mirrors [14] or BJT current mirrors [17]. Since the CTAT current will be sunk from the input node of the DSM, the PTAT current will need to be sourced to this node in order to establish a current balance. For this PNP-based design, this can be realized as an additional PMOS in series with a switch that is controlled by the bitstream (BS).

To achieve a highly accurate DAC ratio ('x') and to minimize the gain error of the sensor, Dynamic Element Matching (DEM) must be applied. Compared to resistors, applying DEM to current mirrors introduces less error due to the finite on-resistance of switches, making the current DAC topology favourable, at the expense of more supply current (=xI_{PTAT}).

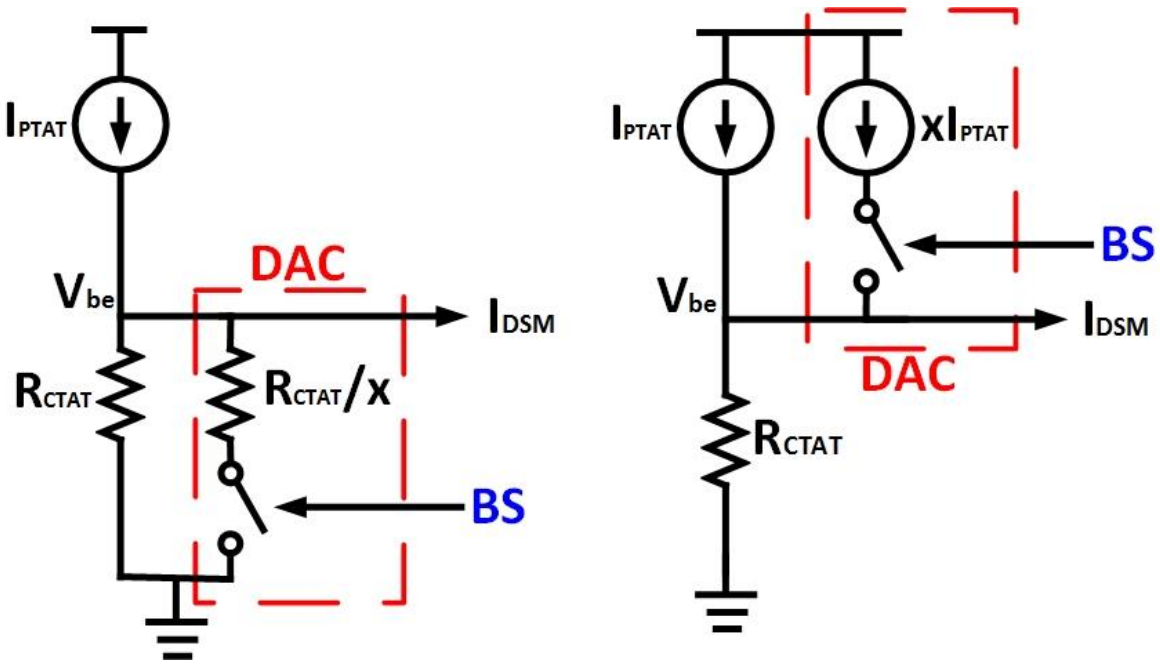


***Figure 2.2**: A resistor-DAC (left), and a current-DAC (right).*

2.2 Coefficients scaling

2.2.1 Scaling parameters

As in earlier work [7] [14] [17], the dynamic range of the DSM over the desired temperature range should be maximized. To achieve this, good understanding and fine-tuning of different scaling parameters are required. Figure 2.3 visualizes the various coefficients that are relevant for the output of the sensor.

A BJT temperature sensor relies on the accurate collector current ratio of two BJTs, whose magnitude defines the sensor's temperature sensitivity through ΔV_{BE}. This current ratio determines the baseline for the sensor's achievable energy efficiency and accuracy, and is defined as 'p'. Then for two identical BJTs:

$$p = \frac{I_{C,Q2}}{I_{C,Q1}} \rightarrow I_{PTAT} = \frac{k_b T ln(p)}{q R_{PTAT}} \tag{2.1}$$

As mentioned in the previous section, two different PTAT currents will flow into the 1st integrator of the DSM depending on the state of the bitstream (BS), while a fixed CTAT current will flow out of the integrator. In Figure 2.3, I_{out} constantly flows into the DSM, while a variable current flows to the DSM depending on the DAC state. The ratio between the PTAT current flowing into the DSM for BS=0 and BS=1 is defined as 'n', i.e.:

$$n = \frac{I_{PTAT,BS=0}}{I_{PTAT,BS=1}} = \frac{I_{out} + I_{DAC}}{I_{out}} \tag{2.2}$$

The ratio between the unit bias current I_{bias} in the analog front-end and the PTAT output current I_{out} flowing to the DSM defines the amount of current that is used by the current balancing circuit and is denoted as 'k'. In practice, k=1 in order to facilitate the implementation of DEM.

$$k = \frac{I_{out}}{I_{bias}} \tag{2.3}$$

Lastly, the ratio between the PTAT bias resistor R_{PTAT} in the front-end and the CTAT resistor R_{CTAT}, and thus the PTAT/CTAT scaling factor, is defined as 'm':

$$m = \frac{R_{CTAT}}{R_{PTAT}} \tag{2.4}$$

The currents flowing into the DSM can then be defined as:

$$I_{CTAT} = -\frac{V_{BE}}{R_{CTAT}} = -\frac{V_{BE}}{m R_{PTAT}} \tag{2.5}$$

$$I_{PTAT,BS=1} = k I_{bias} = \frac{k \Delta V_{BE}}{R_{PTAT}} \tag{2.6}$$

$$I_{PTAT,BS=0} = n k I_{bias} = \frac{n k \Delta V_{BE}}{R_{PTAT}} \tag{2.7}$$

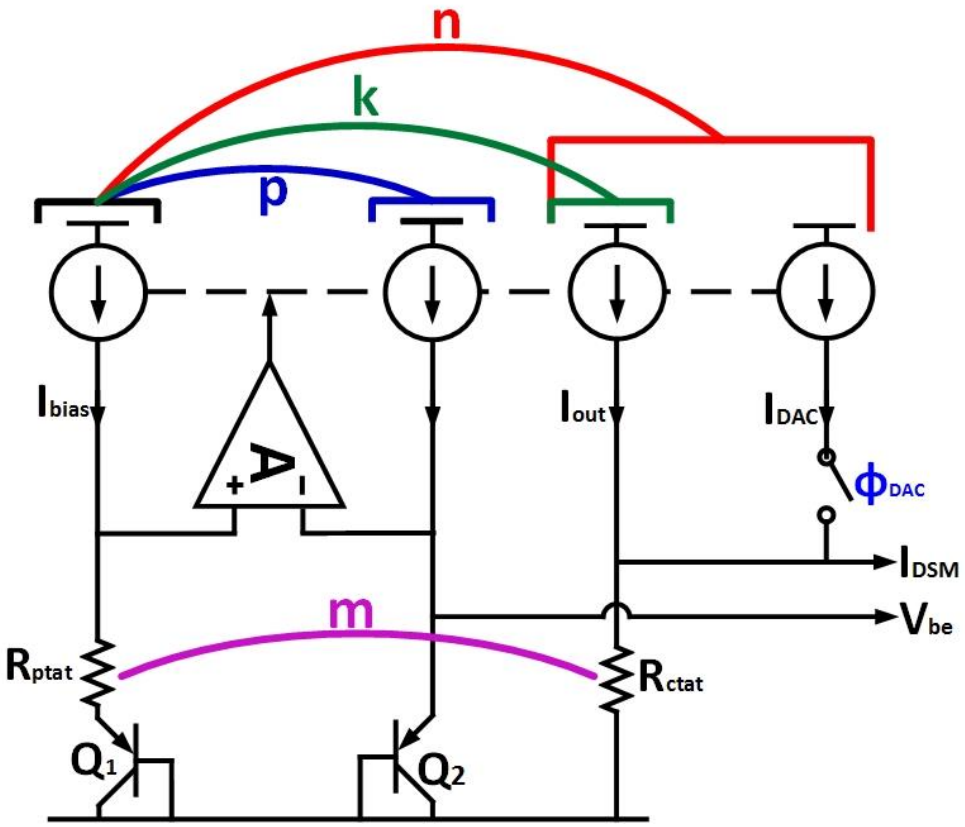


***Figure 2.3**: A representation of the coefficients present in the front-end.*

Note that, if the bitstream average is μ, then the number of times that BS=0 occurs can be represented by '1-μ', while the number of times that BS=1 can be represented by 'μ'. Considering that the weighted average of the integrator's charge during a conversion must be zero, μ can then be derived using the charge balancing equation:

$$\mu\left(I_{PTAT,BS=1} - I_{CTAT}\right) + (1-\mu)\left(I_{PTAT,BS=0} - I_{CTAT}\right) = 0 \tag{2.8}$$

And μ can be expressed as:

$$\mu = \frac{nmk\Delta V_{BE} - V_{BE}}{(n-1)mk\Delta V_{BE}} = \frac{n}{n-1} - \frac{X}{(n-1)mk} \quad where\ X = \frac{V_{BE}}{\Delta V_{BE}} \tag{2.9}$$

Equation 2.9 can be interpreted in the following way: as a function of X, the sensor's gain is affected by two effective variables 'n' and 'm·k', while only 'n' affects the sensor's offset. With these two degrees of freedom, it is possible to scale the sensor's output over an arbitrary temperature range. For DEM and layout convenience, however, integer ratios are preferred.

The targeted temperature range of this design is the industrial range, i.e., from -45°C to 85°C. The next chapter will clarify how a current density ratio 'p' of 7 was found to be a good compromise between energy efficiency and accuracy. It then follows that if n=3 and m·k=8 are chosen, μ will range from 0.16 to 0.88 over the temperature range. Figure 2.4 shows that the proposed nonlinear μ uses 72% of the DAC range, which relaxes the quantization noise requirements of the DSM compared to the μ of a traditional SC temperature sensor (Equation 1.3).

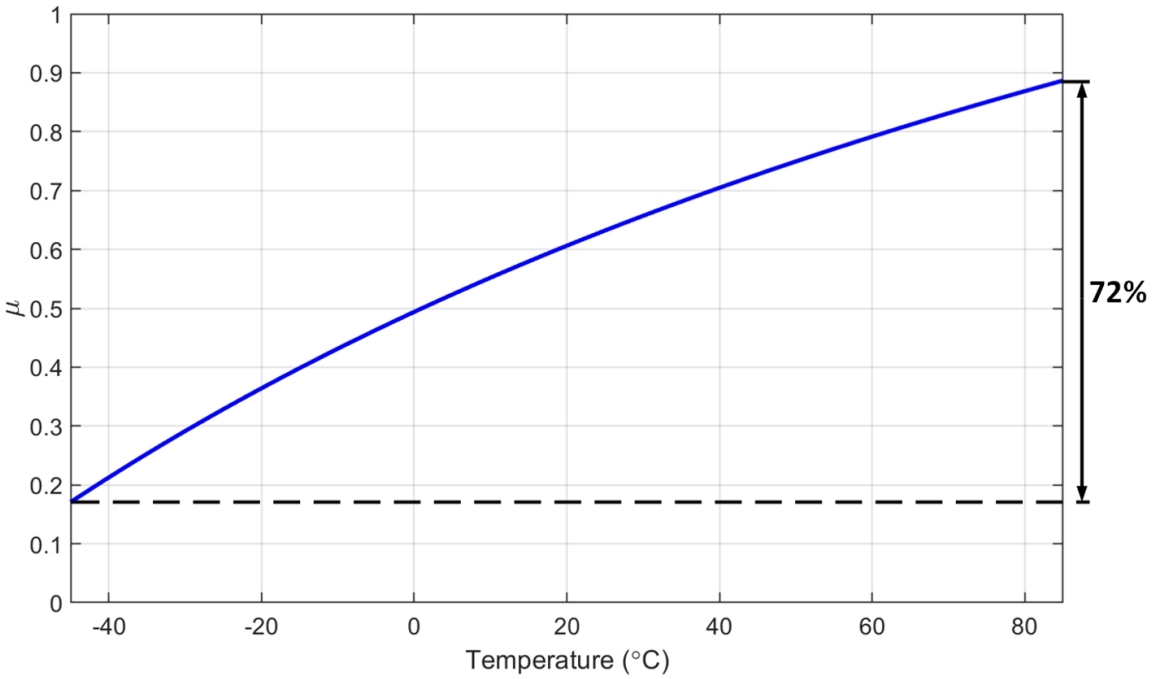


***Figure 2.4**: The average of the proposed sensor's bitstream output over the industrial temperature range.*

Since the current mirror ratio 'k' is designed to be 1 for easier DEM, it follows that a resistor ratio 'm'=8 is required. The simplified schematic of the proposed sensor can then be found in Figure 2.5.

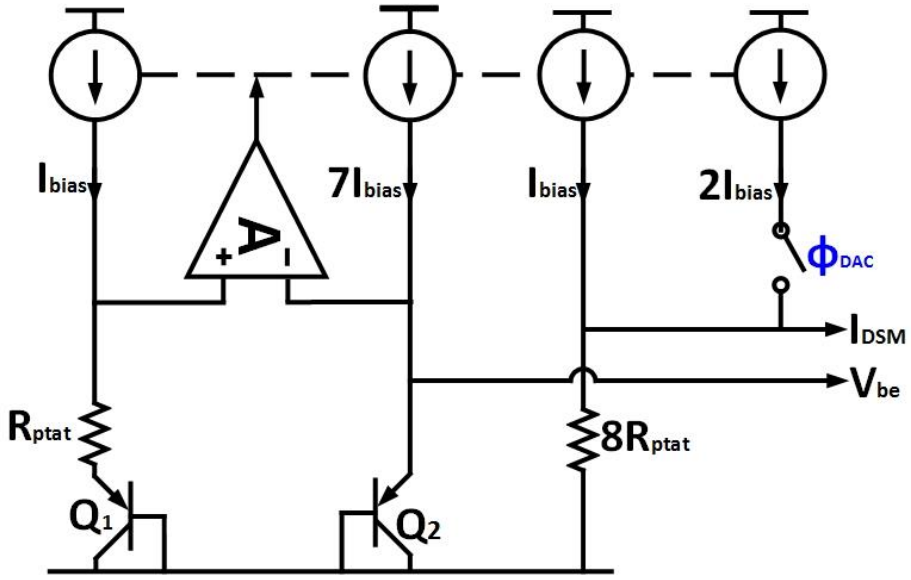


***Figure 2.5**: Circuit diagram after the coefficients have been scaled.*

2.2.2 Matching considerations

The spread in the four coefficients ('n', 'm', 'k', and 'p') mentioned in the previous sector all directly contribute to the inaccuracy of the sensor. When equation 2.9 is rewritten in the following way, all four coefficients appear in the output expression:

$$\mu = \frac{n}{n-1} - \frac{V_{BE}}{(n-1)mk\frac{k_b T}{q} ln\,(p)} \tag{2.10}$$

The sensitivities of the measured temperature to the coefficients can then be expressed as:

$$S_p^{D_{out}} = \frac{dT}{dp} = \frac{X}{(n-1)mkpln(p)} \frac{dT}{d\mu} \tag{2.11}$$

$$S_k^{D_{out}} = \frac{dT}{dk} = \frac{X}{(n-1)mk^2m} \frac{dT}{d\mu} \tag{2.12}$$

$$S_m^{D_{out}} = \frac{dT}{dm} = \frac{X}{(n-1)m^2k} \frac{dT}{d\mu} \tag{2.13}$$

$$S_n^{D_{out}} = \frac{dT}{dn} = \frac{(X-km)}{(n-1)^2mk} \frac{dT}{d\mu} \tag{2.14}$$

Over the industrial temperature range, X ranges from 21.6 to 9.8, while the temperature sensitivity to μ (dT/dμ) ranges from 100°C to 250°C per unit BS average. In Figure 2.6, the allowable spread of each coefficient for an individual untrimmed temperature spread of 0.1°C over the temperature range is shown. With p=7, m=8, k=1, and n=3, it follows that 'm', and 'k' can spread by 0.057%, 'n' can spread by 0.064%, and 'p' can spread by 0.113%. To achieve such levels of matching, DEM and very careful layout are required to minimize the temperature error.

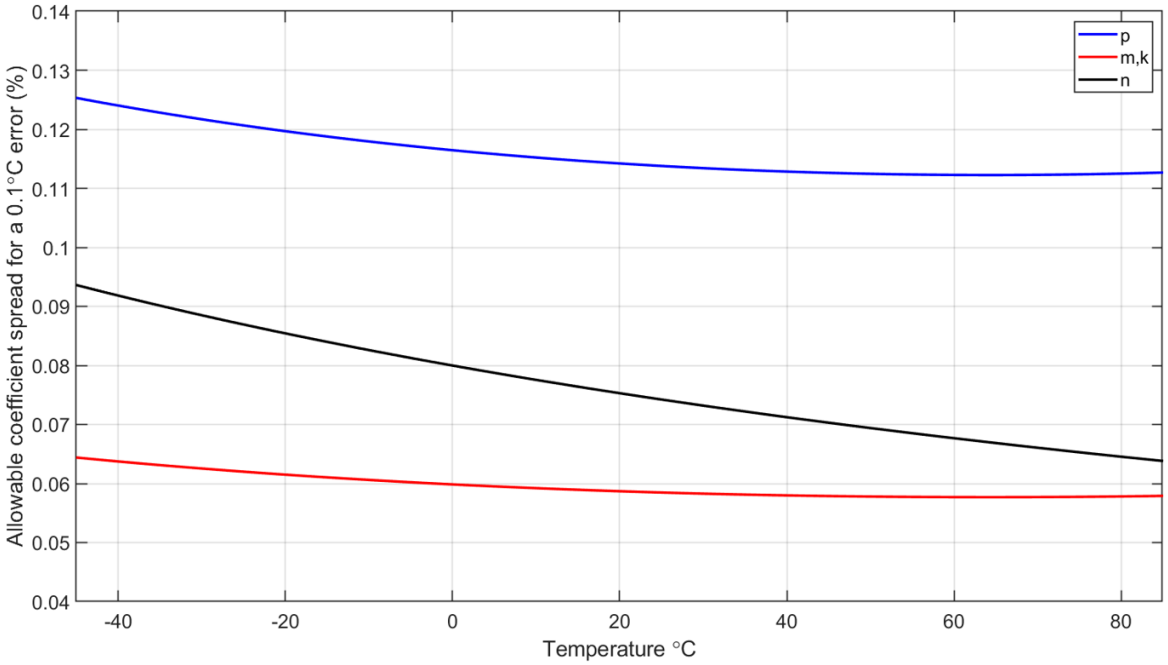


***Figure 2.6**: Comparison of the allowable offset of the several coefficients for a 0.1°C temperature error.*

2.2.3 Noise considerations

With a continuous-time topology, the sensor's resolution should be purely limited by thermal noise instead of kT/C noise. The main thermal noise contributors are the PTAT and CTAT resistors, the BJTs, the current mirrors (CM), and the bias opamp.

The 1/f noise contribution of the resistors and BJTs is negligible, but both the current mirrors and the opamp suffer from significant 1/f noise, which will degrade the achieved resolution if not removed. In the case of the opamp, 1/f noise is removed by chopping, while for current mirrors, it is done by performing DEM. Both techniques must be operated above the 1/f noise corner to achieve a thermal-noise-limited resolution.

For energy efficiency optimization, it is advantageous to normalize the current noise power contributions of each block to the consumed current, represented by the unit bias current I_{bias}, so that an objective noise comparison can be done. The calculations in the following analysis are based on [19]. The normalized current noise power of the four sub-blocks is given by:

$$\frac{I_{n,R_{PTAT}}}{I_{bias}} = \frac{\frac{4k_bT}{R_{PTAT}}}{\frac{k_bTln(p)}{qR_{PTAT}}} = \frac{4q}{\ln(p)} \tag{2.15}$$

$$\frac{I_{n,R_{CTAT}}}{I_{bias}} = \frac{4q}{\mathrm{m}\ln(p)} * \frac{1}{(n-1)k}^{2} = \frac{q}{8\ln(p)} \tag{2.16}$$

$$\frac{I_{n,BJT}}{I_{bias}} = \frac{\frac{k_bT}{R_{PTAT}}\left(1+\frac{2}{pln(p)}\right)}{\frac{k_bTln(p)}{qR_{PTAT}}} \approx \frac{1.15q}{\ln(p)} \tag{2.17}$$

$$\frac{I_{n,CM}}{I_{bias}} = \frac{\frac{8(k_bT)^2\ln(p)\frac{g_m}{I_{D\ CM}}}{3qR_{PTAT}}\left(1+\frac{1}{ln(p)}\right)}{\frac{k_bTln(p)}{qR_{PTAT}}} \approx 6kT\frac{g_m}{I_{D\ CM}} \tag{2.18}$$

$$\frac{I_{n,opamp}}{I_{bias}} = \frac{\frac{NEF*16q}{3\ln(p)\,R_{PTAT}a\frac{g_m}{I_{D\ opamp}}}}{\frac{k_bTln(p)}{qR_{PTAT}}} \approx 1.37\frac{q^2NEF}{akT\frac{g_m}{I_{D\ opamp}}} \tag{2.19}$$

In these equations, $(g_m/I_D)_{CM}$=5, $(g_m/I_D)_{opamp}$=25, and a Noise Excess Factor (NEF) of 3 are assumed. Since the FoM contributions of the BJTs and resistors are constant for a set collector current ratio 'p', they provide the baseline for the achievable energy efficiency. In equation (2.19), 'a' signifies the ratio between the current flowing through the input transistor of the opamp and the bias current. When scaling the amplifier current so that it contributes similar noise to the resistors and BJTs, a=3 is found. The relative noise contributions and current consumption of the components at room temperature can then be found in Table 2.1. In this table, 'b' indicates the number of current branches in the opamp. It can be observed that a

topology using a minimal number of current branches must be applied for optimal energy efficiency.

	Component	Thermal noise contribution (%)	Current consumption
PTAT current	R_{PTAT}	37	
	BJTs	11	
	Current mirrors	13	$11I_{bias}$ ($8I_{bias}$ to BJTs)
	Opamp	38	$3b \cdot I_{bias}$
CTAT current	R_{CTAT}	1	-

***Table 2.1**: Estimation of the power contributions of the several front-end components.*

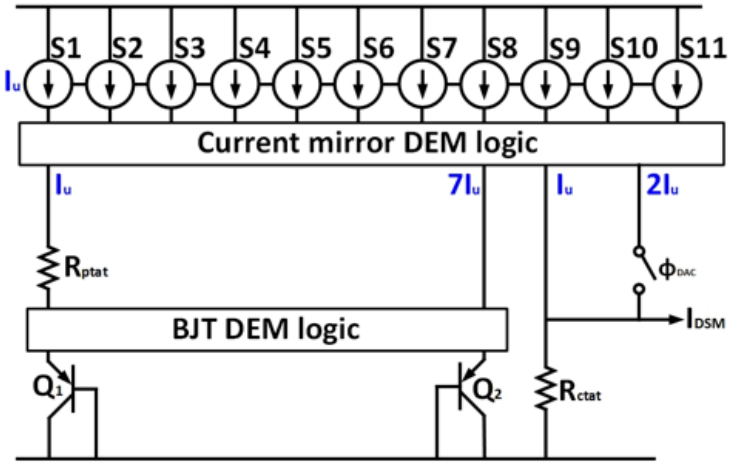
It can be observed that 49% of the total noise power originates from the BJTs and resistors. Furthermore, it is apparent how the amplification of ΔV_{BE} compared to V_{BE} makes the PTAT current noise dominant compared to that of the CTAT current. The input-referred voltage noise of the DSM will be converted to a current by the CTAT resistor, meaning that it will be added to the CTAT noise component. Therefore, it can be assumed to have a negligible contribution to the total noise.

2.3 Dynamic techniques for better matching

As mentioned earlier, various dynamic techniques are required to satisfy the stringent matching requirements. In this work, DEM is applied to both the current mirrors and the BJTs.

For simplicity and easy implementation, barrel-shifting DEM is applied. Thus, the 11 current mirrors in the front-end lead to an 11-state state-machine, as shown in Figure 2.7. In state 1, current mirror S1 is connected to Q_1, S2-8 to Q_2, S9 directly to the DSM, and S10-11 to the DAC branch. In state 2, all the indexes are shifted by 1 compared to state 1, e.g., S2 is connected to Q_1 and S3-9 to Q_2, and so on and so forth. As for the BJT DEM (or BJT swap), the difference between the two states lies in whether Q_1 and Q_2 is connected to the R_{PTAT} resistor. After a complete DEM cycle of the 11 current mirrors, the position of the BJTs is swapped in order to mitigate their mismatch. The timing of the DEM for the BJTs and current mirrors is illustrated in Figure 2.7.

When barrel-shifting DEM is applied to the DAC of a DSM, mismatch will cause the DAC to be non-linear, as stated in [20]. This causes some of the DSM's quantization noise to be folded to the signal band, which limits the achievable resolution. One way to reduce the folded quantization noise is to reduce the DEM speed. However, slowing the DEM may result in insufficient 1/f noise suppression, especially when the DEM frequency is lower than the 1/f noise corner of the current mirrors, which is simulated to be at 200Hz. Therefore, a trade-off exists for the DEM speed.



DEM period	CM DEM state	BJT DEM state
1	1	1
2	2	1
...	...	...
11	11	1
12	1	2
13	2	2
...	...	...
21	10	2
22	11	2
23	1	1

***Figure 2.7**: A circuit diagram containing the DEM circuitry (left) and the DEM control signals (right).*

Since the resistors R_{ptat} and R_{ctat} share no common nodes, a large number of switches would be required to apply DEM. Apart from on-resistance and leakage current, swapping the position of the resistors in the circuit also introduces significant transients, which will directly affect the accuracy of the sensor. For this reason, no DEM is applied to the resistors, meaning that the accuracy of the resistor ratio will rely on precise layout.

2.4 Trimming and readout

Typically, non-trimmed BJT temperature sensors show a PTAT temperature spread due to the spread of its saturation current. This can most effectively be removed by applying a PTAT trim, either physically [14] or in the digital processing of the output [12]. It was found in [7] that, when the ADC output is $X=V_{BE}/\Delta V_{BE}$, this PTAT temperature spread manifests itself as an offset spread to μ. In this case, an offset trim effectively removes the V_{BE} spread. The same can be applied to the proposed BJT sensor, since the output of the proposed sensor is a scaled version of X (equation 2.9). Figure 2.8 illustrates this effect.

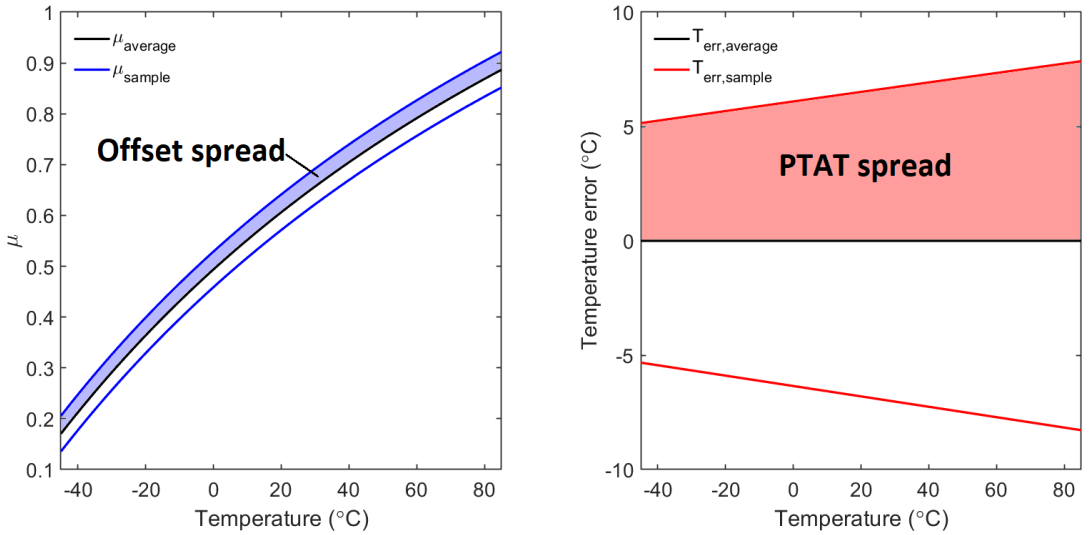


***Figure 2.8:** A representation of offset spread of the bitstream average μ (left), and how this results in a PTAT spread in the simulated output temperature (right).*

Most of the sensor's spread will be cancelled after the aforementioned offset trim, but a large non-linearity remains. To remove this, the ratio X can be converted into a linear function of temperature, as in equation 1.3. The comparison between the non-linear and the traditional sensor output can be observed in Figure 2.9. Given chosen parameters, equation 2.9 can be rewritten as:

$$\mu = 1.5 - \frac{X}{16} \tag{2.20}$$

This can be converted to the classical expression as:

$$\mu_{lin} = \frac{\alpha}{\alpha + X} = \frac{\alpha}{\alpha + 24 - 16\mu} \tag{2.21}$$

α would be acquired using batch calibration, after which the gain factor A and offset B can be found to convert the output to °C:

$$T(°C) = A\mu_{lin} + B \tag{2.22}$$

Alternatively, the output of the sensor could be fitted to a high-order polynomial function. However, a 5th order polynomial would be required to reduce the nonlinearity below 0.01°, resulting in a significantly more complex readout circuit.

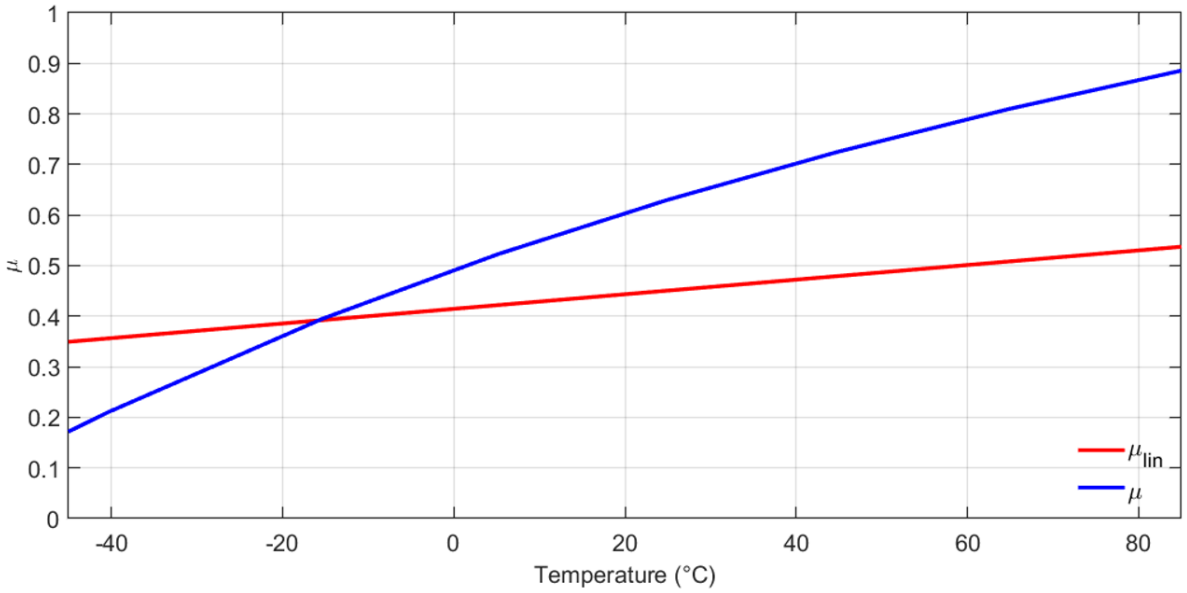


Figure 2.9: *A comparison between the μ before and after mathematical linearization had been applied.*

2.5 Summary

This chapter discusses the various design considerations that were done in order to arrive at the chosen system architecture. These considerations must be kept in mind while designing the circuit.

3 Circuit implementation

In this chapter, the circuit implementations of the two main blocks are discussed: The BJT front-end and the Delta-Sigma Modulator. After this, an analysis of the noise performance, and a description of the signal timing is presented.

3.1 BJT front-end

As highlighted in Figure 3.1, the four main components in the front-end are the BJTs, the resistors, the current mirrors, and the bias opamp.

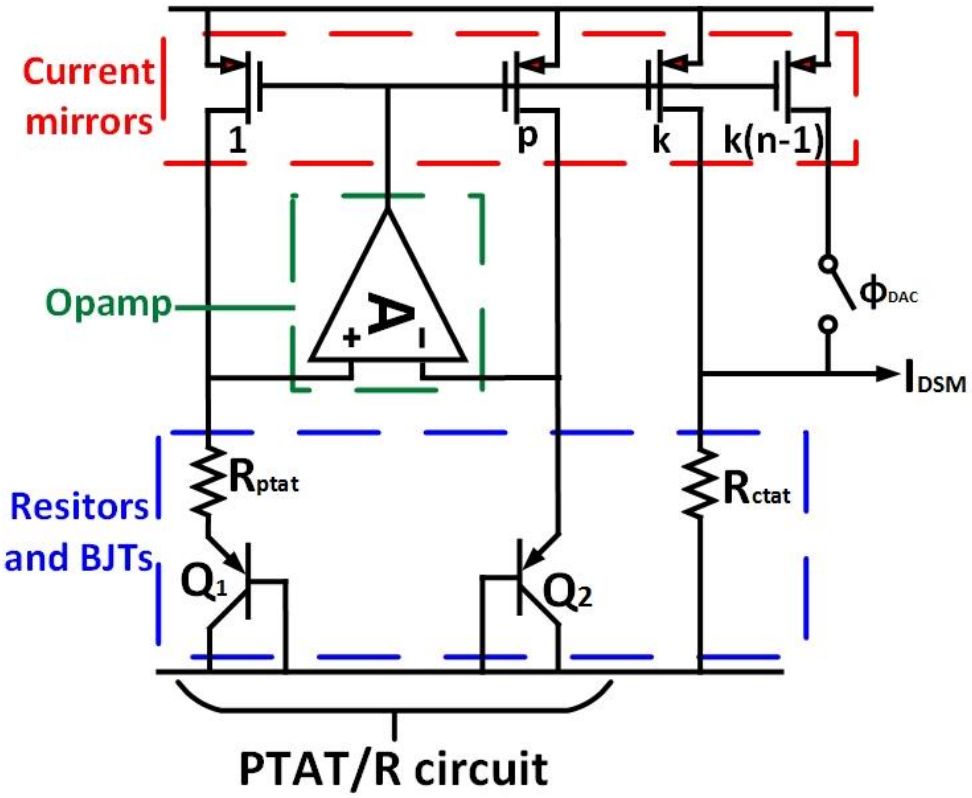


***Figure 3.1**: The sub-blocks of the BJT front-end.*

3.1.1 BJTs and resistors

Generally, the biasing block in a BJT temperature sensor consists of a PTAT/R circuit [21], as shown in Figure 3.1. In this circuit, two PNPs ($Q_{1,2}$) are biased at a current density ratio 'p', and a resistor is added at the emitter of Q_1. An opamp forces the difference between the base-emitter voltages ΔV_{BE} over the resistor, ensuring that a PTAT current flows through the emitter

of Q_1 according to the equation below. This current is used as a representation of temperature, and as the bias current for the rest of the sensor.

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R_{PTAT}} = \frac{k_b T ln\left(\frac{I_{C2}}{I_{C1}}\right)}{qR_{PTAT}} = \frac{k_b T ln(p)}{qR_{PTAT}} \quad (3.1)$$

When high accuracy is desired, it is critical to tackle the various non-idealities of BJTs in CMOS technology, which are illustrated in Figure 3.2. The largest source of spread is the spread in V_{BE} due to its dependence on the BJT's saturation current I_s. As discussed in section 2.4, this can be removed by performing a PTAT trim on V_{BE} after a calibration at a single temperature.

The following equation shows the effect of I_S and the parasitic emitter resistance R_E on the measured V_{BE}.

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S} + 1\right) + I_E R'_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_S} + 1\right) + I_E \left(R_E + \frac{R_C}{\beta}\right) \quad (3.2)$$

To achieve the desired exponential relationship between I_C and V_{BE}, I_C must be significantly larger than I_S (24.7fA at 85°C). However, as I_C, and thus I_E, increases, the presence of R_E and R_B (25Ω and 30Ω, respectively) also causes significant errors. The optimal I_C level for temperature sensing inaccuracy is thus bounded by the two constraints.

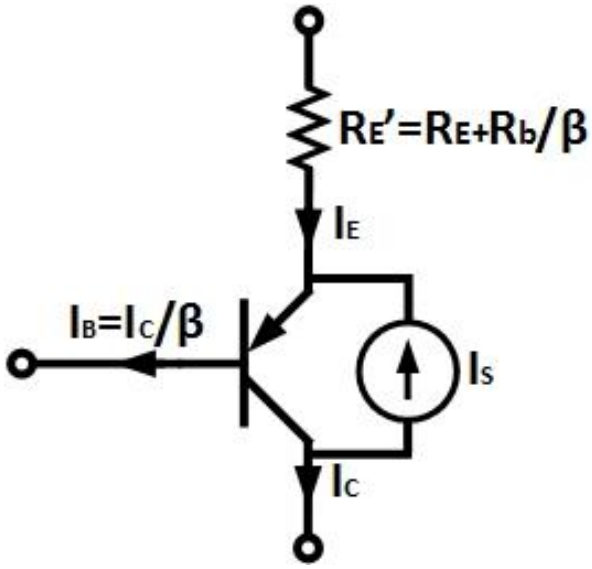


***Figure 3.2**: Non-idealities of a PNP transistor.*

The most detrimental non-ideality in the BJTs is their limited current gain (β), which means that a current I_C/β will flow from the emitter to the base. PNPs are biased via their emitter, while ΔV_{BE} is defined by a collector current ratio, meaning that β will affect the PTAT voltage. This is expressed in equation 3.3.

$$\Delta V_{BE} = \frac{k_b T}{q} \ln\left(\frac{I_{C2}}{I_{C1}}\right) = \frac{k_b T}{q} \ln\left(\frac{p * I_{PTAT} \frac{\beta_1}{\beta_1 + 1}}{I_{PTAT} \frac{\beta_2}{\beta_2 + 1}}\right) = \frac{k_b T}{q} \left(\ln(p) + \ln\left(\frac{\beta_1(\beta_2 + 1)}{\beta_2(\beta_1 + 1)}\right)\right) \quad (3.3)$$

From this equation, it follows that β of both PNPs must be identical for ΔV_{BE} to be unaffected. Since the PNPs are biased at different current levels, this can only be ensured by biasing the PNPs in their known "flat β region" [22]. Here, β stays roughly constant within a certain current range, such that the second term in equation 3.2 approximates 0. This region can be observed in Figure 3.3, which shows the β of a standard 5µm×5µm PNP over its collector current. It can be observed that the PNPs should be biased in the nA to µA current range, where its current gain is flattest. While increasing ΔV_{BE}, and thus improving energy efficiency, choosing a large collector current ratio 'p' will result in a larger β-mismatch, which will reduce the accuracy. A current ratio of 7 was found to provide a good trade-off between energy efficiency and accuracy.

The effect of β on the CTAT current through V_{BE} will remain, as is expressed in equation 3.4. Since the sensitivity of the measured temperature to V_{BE} is far smaller than to ΔV_{BE}, this extra source of spread can be tolerated, and is suppressed after a PTAT trim.

$$V_{BE} = \frac{k_b T}{q} \ln\left(\frac{I_{C2}\frac{\beta_2}{\beta_2+1}}{I_{S2}}\right) = V_{BE,desired} + \frac{k_b T}{q} \ln\left(\frac{\beta_2}{\beta_2+1}\right) \tag{3.4}$$

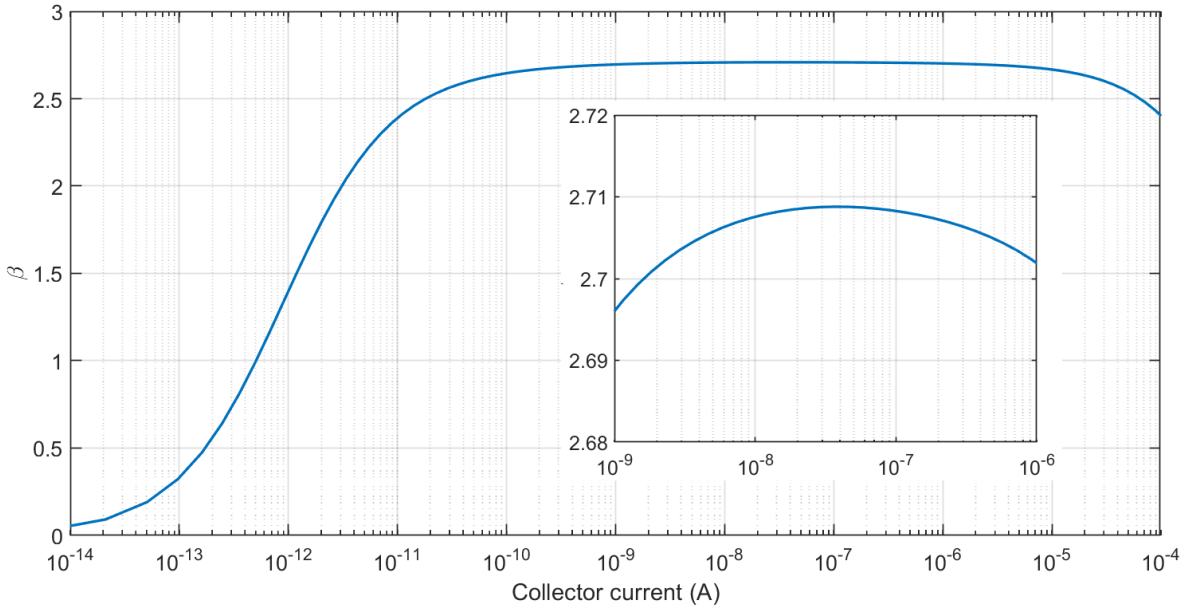


***Figure 3.3**: The temperature dependence of the current gain of a 5µm×5µm PNP.*

In this design, 5µm×5µm PNP transistors are used, whose ΔV_{BE} spread over process and temperature reaches a minimum when I_{bias}=390nA at room temperature. This current ensures a flat-β region, is sufficiently high so that the saturation current has a negligible effect on the accuracy, while still being low enough so that the parasitic resistances of the BJTs do not cause a significant voltage drop. In order to find the optimal inaccuracy for this front-end, a circuit was simulated in which only the PNPs experience corner spread. Figure 3.4 shows that the simulated maximum trimmed temperature spread due to BJT corner spread is 80mK over the PVT corner conditions.

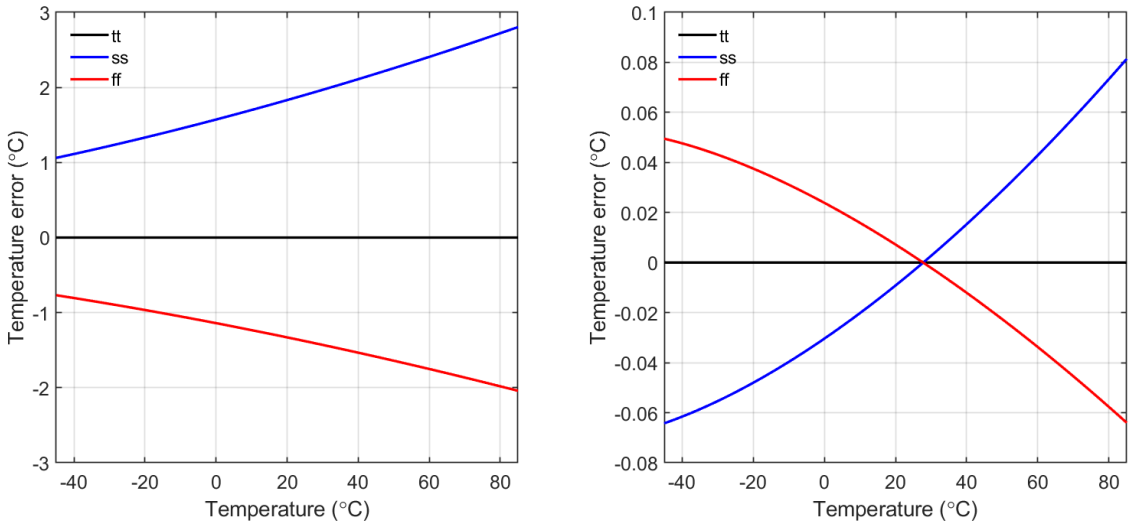


Figure 3.4: *Left: Simulated untrimmed temperature error due to corner spread of the PNPs. Right: Simulated trimmed temperature error due to corner spread of the PNPs.*

The I_{bias} of 390nA corresponds to a PTAT resistor of 130kΩ when p=7. In this circuit, both the PTAT and CTAT resistors were implemented using p+ polysilicon, since it has the best matching given the same silicon area in simulation. By utilizing the same type of resistors in the front-end, the effect of their temperature dependencies on their ratio, and thus sensor inaccuracy, is cancelled out.

3.1.2 Current mirrors

The current mirrors in the front-end must be designed with three design constraints in mind: thermal noise, since it directly affects the sensor's resolution; parasitic gate capacitance, since it determines the size of the switching transients in the front-end, which degrade the accuracy; and matching, since it will affect the sensor's accuracy, even after DEM [11].

Different noise sources in the front-end are referred back to ΔV_{BE} during noise analysis, which enables a fair comparison. In the case of the current mirrors, the noise current at the drain of the MOSFETs will flow through the PTAT resistance, and thus affect ΔV_{BE}. The equation for the current noise at the drain of a MOSFET is given by:

$$I_{n,D} = 4k_b T \gamma g_m \tag{3.5}$$

where g_m is the transconductance, I_D is the drain current, and γ is related to the channel conductance of the MOSFET. From this equation, it follows that the g_m should be minimized given a certain I_D, which indicates a strong inversion operation region. Since the g_m/I_D of a MOSFET in strong inversion can be expressed as shown below, the current mirrors should have a small W/L ratio.

$$\frac{g_m}{I_D} = \sqrt{\frac{2\mu_p C_{ox} \frac{W}{L}}{I_D}} \tag{3.6}$$

Mismatch in MOSFETs is mainly caused by spread in V_{th} and lithography mismatch [23]. Errors due to V_{th} can be minimized by biasing the transistors at a large overdrive voltage (V_{GS}-V_{th}),

and thus again using a small W/L ratio, while lithography errors can be minimized by using large transistors. However, increasing the transistor area results in a large gate capacitance, which must be charged and discharged during the various phases of DEM and chopping, and may cause spikes in the bias current.

The circuit diagram of the analog front-end is shown in Figure 3.5. The 11 current mirrors ($M_{1\text{-}11}$) were sized as W=1.2µm, L=19.5µm, from which it follows that their g_m/I_D=3.8, and consequently, the current mirrors contribute 62% less thermal noise power compared to the resistors and BJTs. Their mismatch before DEM stays below 1.3% (3σ). Using equations retrieved from [11], it can be estimated that this will result in a temperature spread below 10mK (3σ) after DEM is applied. Cascodes ($M_{12\text{-}22}$) with dimensions W=1.2µm, L=0.6µm were added to improve power supply sensitivity. The saturation voltage of the current mirrors at room temperature is set to 380mV, reserving enough voltage headroom for V_{BE} and the cascodes. The start-up circuit consists of a diode-connected HV_t PMOS which pulls the gate of $M_{1\text{-}11}$ down to 888mV, causing each branch to conduct 340nA (at room temperature). The start-up circuit is turned on or off by an externally controlled switch. The cascode biasing branches ensure that all PMOS transistors are in the saturation region over PVT, while only drawing a quarter of the unit bias current each.

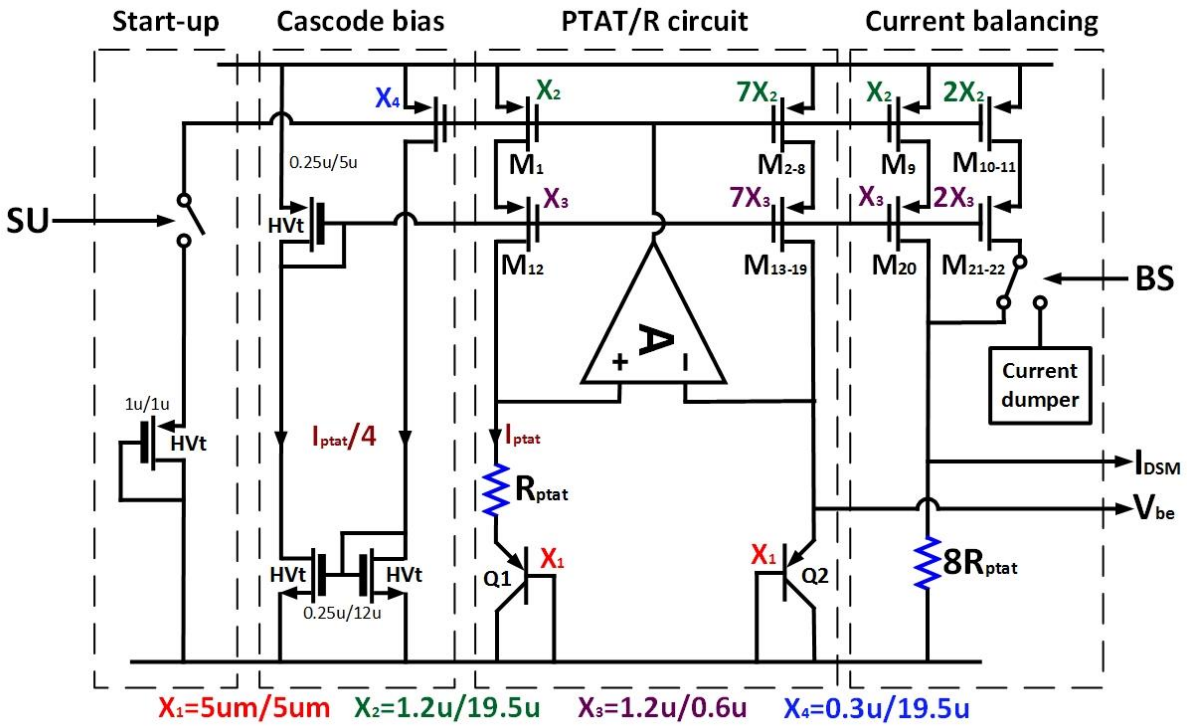


***Figure 3.5**: Schematic representation of the front-end.*

3.1.3 Bias amplifier

The bias opamp is critical for the accurate realization of the PTAT current, and its non-idealities, including offset, noise, and finite gain and speed, directly affect the output of the sensor.

Offset at the input terminals of the bias opamp will affect both the PTAT and CTAT voltage in the following way:

$$V_{CTAT} = V_{be2} + \frac{V_{os}}{\ln(p)} \tag{3.7}$$

$$V_{PTAT} = \Delta V_{BE} + V_{os} \tag{3.8}$$

For a temperature deviation of 0.1°C the maximum offset can be 30µV in this design. This requirement is stricter than in voltage-domain PNP front-ends, because the offset affects both ΔV_{BE} and V_{BE}, instead of just V_{BE}. Therefore, chopping the amplifier is essential, which additionally cancels its flicker noise. In this design, chopping is performed at the sampling frequency f_s of the DSM, such that the folded quantization noise is minimal. Though with this stringent offset requirement, even the residual offset after chopping must be carefully examined. In other words, the opamp should be fast enough to suppress the spike-related errors caused by the finite charging time of the large current mirrors. Simulation results show that the minimum bandwidth to ensure an added temperature error below 0.1°C over PVT is 200kHz.

In a similar fashion, the minimum closed-loop gain of the opamp is found to be 66dB given a translated temperature error of 0.1°C. The required open-loop gain of the opamp can then be found as:

$$A_{OL} = \frac{A_{CL}}{g_{m,M1} * \left(R_{ptat} + \frac{1}{g_{m,Q1}}\right)} = \frac{A_{CL}}{3.8 I_{ptat} * \left(R_{ptat} + \frac{kT}{qI_{ptat}}\right)} \tag{3.9}$$

It follows that the required open-loop gain for the amplifier is 77dB over PVT.

The input common-mode voltage of the opamp is equal to V_{BE2}, which is 590mV-820mV over the temperature range. Its output voltage is equal to the gate voltage of the current mirrors and varies from 840mV-940mV. The relatively small input and output voltage range allows the use of an energy-efficient telescopic cascode amplifier, as shown in Figure 3.6. This topology only utilizes two current branches, which was determined to be favourable for energy efficiency in section 2.2.3

An NMOS-input pair is adopted, as the output voltage of the amplifier is higher than its input. At 85°C, the input voltage (V_{BE2}) will be 590mK. To keep V_{ds}>V_{dsat} for the tail current source (M_9), V_{gs} of the input pair ($M_{1,2}$) should be less than 350mV, which is achieved by using medium-Vt NMOS transistors. At room temperature, these transistors have a threshold voltage of 400mV, and are biased in weak inversion at V_{GS}=280mV, leaving 70mV of headroom for the tail transistor.

The gate voltages of the NMOS tail transistor (M_9) and cascodes ($M_{3,4}$) are both generated using a separate biasing branch using a quarter of the PTAT bias current. The gate voltages of the PMOS current mirrors ($M_{7,8}$) and cascodes ($M_{5,6}$) from the front-end were reused to avoid additional biasing branches. In order to ensure a proper NMOS cascode gate voltage over the temperature range, a diode-connected NMOS (M_{10}) is inserted between the cascode's gate and the drain of the tail transistor.

The input-referred voltage noise of the amplifier is added to ΔV_{BE}, and therefore needs to be minimized. To achieve this, the g_m related to a bias current of the input transistors must be maximized, as was expressed in equation 2.19; therefore, the input transistors are biased in weak inversion. The PMOS current mirrors ($M_{7,8}$) are sized for low g_m, so that they contribute little noise. With both branches using three times the biasing current, as was calculated in the previous chapter, the opamp contributes 38% less noise power compared to the resistors and BJTs, ensuring a good compromise between the opamp's noise contribution and power consumption [19]. Furthermore, it achieves a closed-loop gain-bandwidth product of 325kHz, ensuring a temperature error due to residual offset below 60mK. The amplifier's worst-case open-loop gain over PVT is 82dB.

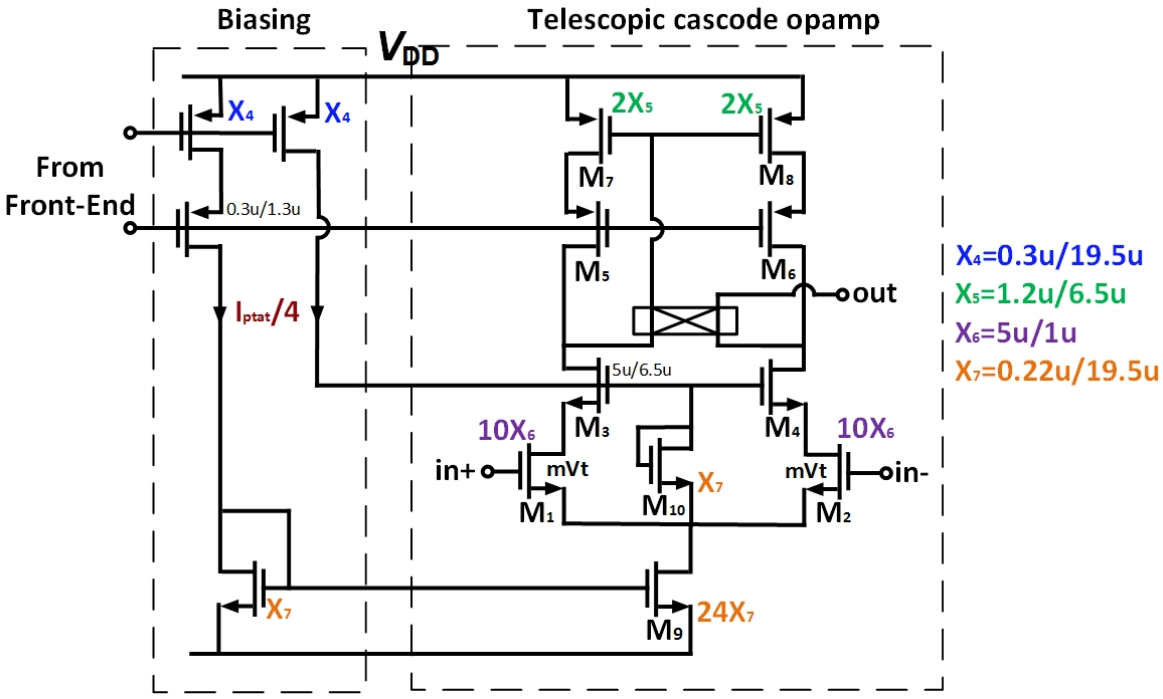


***Figure 3.6**: Schematic of the bias amplifier.*

3.1.4 DEM circuitry

Figure 3.7 shows the DEM switches of a single current branch. To achieve accurate current ratios p, n, and k, the DEM circuitry should allow the 11 current mirrors ($M_{1\text{-}11}$) to be connected to 4 different branches: The emitter of Q1 (1x), the emitter of Q2 (7x), the branch directly connected to the DSM (1x), and the DAC branch (2x). This is realized by 44 NMOS switches, connected under the cascodes of the current mirrors. For flexibility, the DEM logic is implemented by an FPGA off-chip, and the switch status is controlled by shift-registers. In order to reduce the number of shift-register signals, 11 2-to-4 decoders are used.

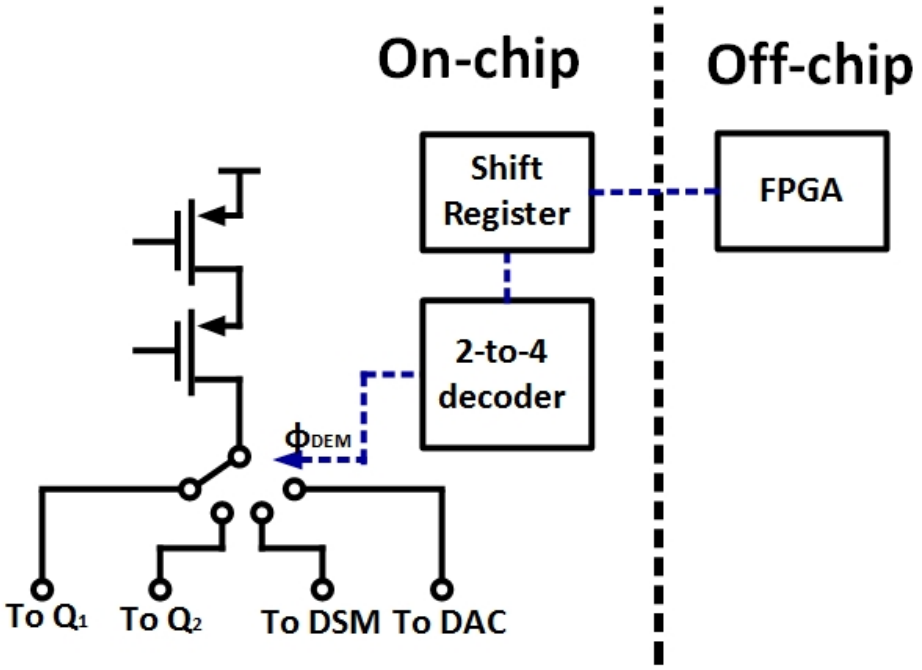


***Figure 3.7**: The DEM switches of a single current branch.*

3.1.5 BJT swap circuitry

Mismatch in the BJT's saturation current affects ΔV_{BE} in the following way:

$$\Delta V_{BE} = \frac{kT}{q}\left(ln\left(\frac{I_{C2}}{I_{S2}}\right) - ln\left(\frac{I_{C1}}{I_{S1}}\right)\right) = \frac{kT}{q}\left(ln\,(p) + \ln\left(\frac{I_{S1}}{I_{S2}}\right)\right) \tag{3.10}$$

To suppress this error, it is necessary to swap the positions of the BJTs during a conversion period. As shown in Figure 3.8, Kelvin connections are used to realize this BJT swapping, so that the ON-resistance of the switches does not affect the sensor's accuracy. The principle of Kelvin connections relies on the use of a "force line" and a "sense line". The force line is driven by a high-Ohmic current source and can therefore contain an arbitrary switch-resistance. The sense line, the input terminals of the opamp in this case, does not carry any current and is therefore also independent of switch resistance. The main advantage of using Kelvin connections is that minimum size switches (0.22µm×0.18µm) can be used, whose small gate capacitance ensures small switching transients while introducing minimal bulk leakage. An additional bias resistor R1' is added so that the circuit topology remains the same under both BJT swap states and to ensure that no switch is needed in series with the PNPs. Two extra switches (bottom of Figure 3.8) are required so that the V_{BE} voltage, which is connected to the positive terminal of the first integrator, stays at the same voltage level. Since BJTs barely introduce any flicker noise, the DEM frequency can be much lower than fs.

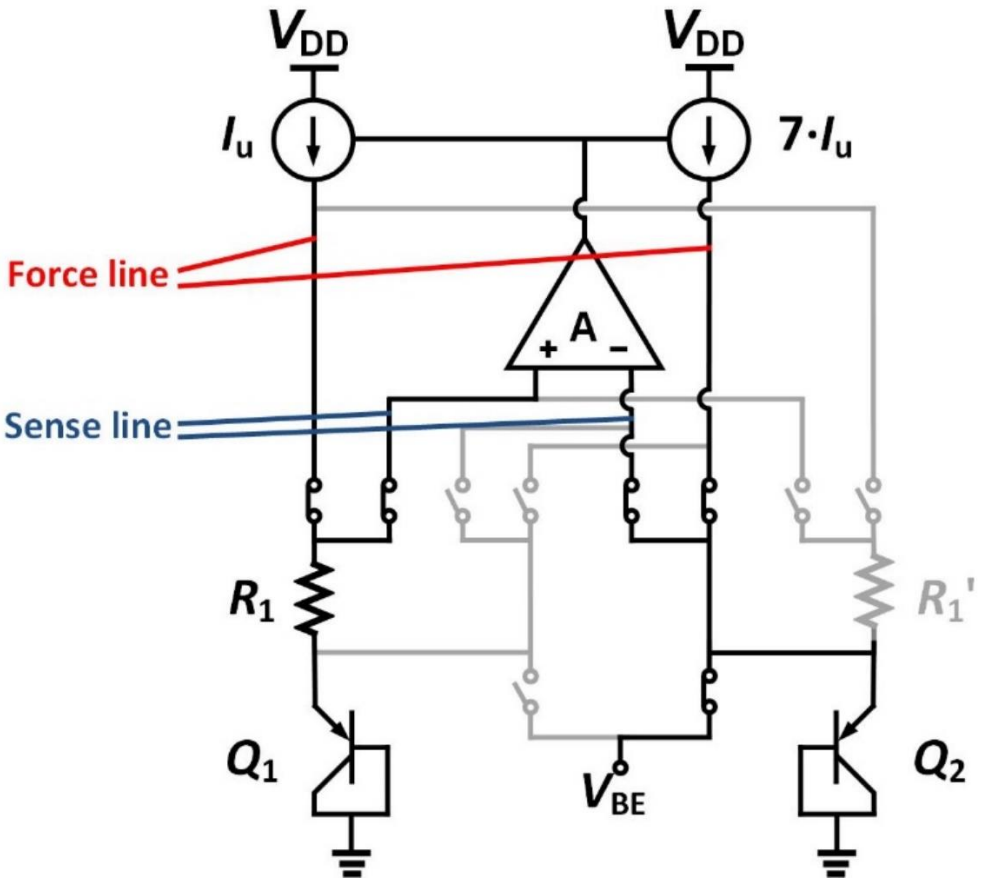


***Figure 3.8**: Kelvin connections used for BJT swapping.*

3.1.6 DAC circuit

Figure 3.9 shows the implementation of the DAC. To reduce current transients caused by charging and discharging of the parasitic capacitors, which degrade the accuracy of the sensor, large voltage swings should be avoided. Therefore, a dumper circuit is added which keeps the unused DAC current flowing when the bitstream is 1. Since this branch will conduct twice the PTAT current, its load impedance should be half of the impedance of the Q1 branch in the bias circuit. This is realized by two PNPs in parallel, in series with a resistor that is half the size of the PTAT bias resistor. Two switches guide the DAC current to either the DSM or the dumper circuit.

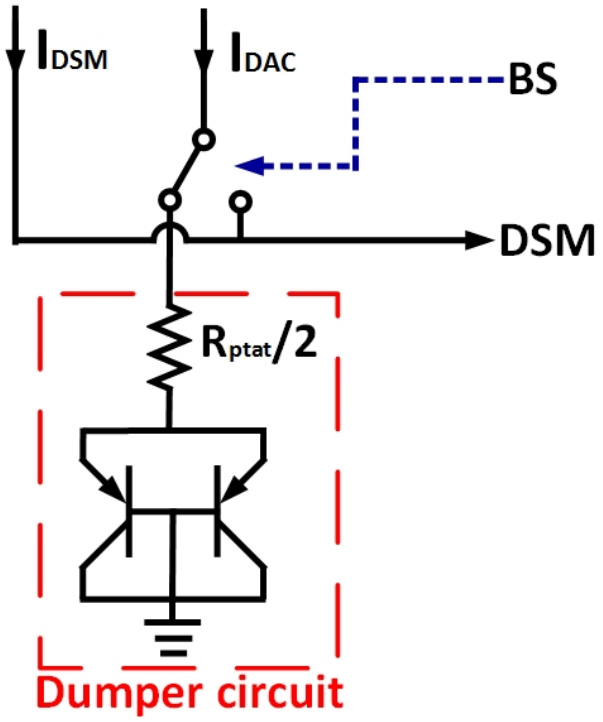


***Figure 3.9**: The DAC circuit including the current dumper.*

3.1.7 Switch leakage

The effect of bulk leakage of the various switches was also investigated. Bulk leakage has an exponential dependence on temperature, and a linear dependence on the area of the switch. As mentioned, minimum size switches were used, which experience a bulk leakage below 3pA up to 125°C. Figure 3.10 shows the temperature error caused by the total switch leakage in the circuit. Up to 125°C, the resulting temperature error stays below 0.01°C, while the effect over the desired industrial temperature range is negligible.

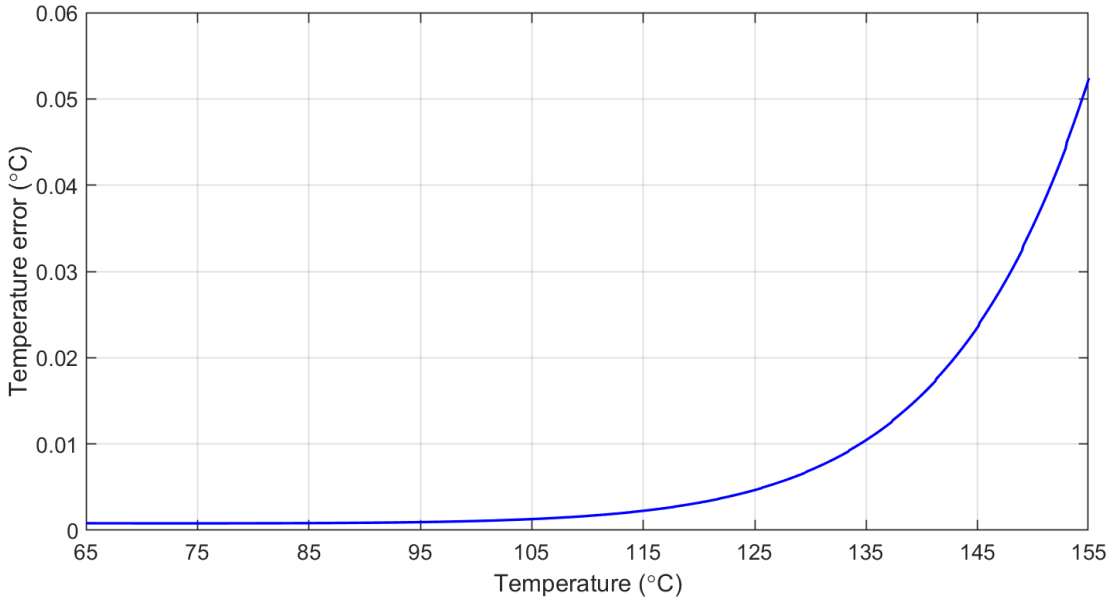


***Figure 3.10**: Temperature error due to bulk leakage of the switches.*

3.2 Delta-Sigma Modulator

3.2.1 DSM topology

As mentioned in the previous chapter, a Delta-Sigma Modulator is used to balance PTAT and CTAT currents and digitize their ratio. It needs to ensure that the quantization noise is lower than the expected thermal noise, which will be dominated by the front-end, as was established in the previous chapter. Inserting I_{bias}=390nA in the noise equations in section 2.3.3 yields a 0.18mK/√Hz thermal noise floor. Combined with the conversion time, this thermal noise floor decides the required quantization noise level of the DSM. Also, the modulator should be able to source or sink the current that will flow from the BJT front-end.

Figure 3.11 shows the achieved SQNR of a 1st and 2nd order DSM over its oversampling ratio (OSR) (retrieved from [24]), along with the front-end's SNR assuming f_s=20kHz and a 0.18mK/√Hz noise floor over the -45°C to 85°C temperature range. For a 1st order DSM, the OSR should be larger than 4000 for the sensor resolution to be dominated by thermal noise. For a clock frequency of 20kHz, this translates to a minimum conversion time of 400ms, which is beyond the specification. With a 2nd order filter, a minimum OSR of 160 should assure that the quantization noise is reduced to below the thermal noise floor, resulting in a minimum conversion time of 15ms for a 20kHz clock frequency.

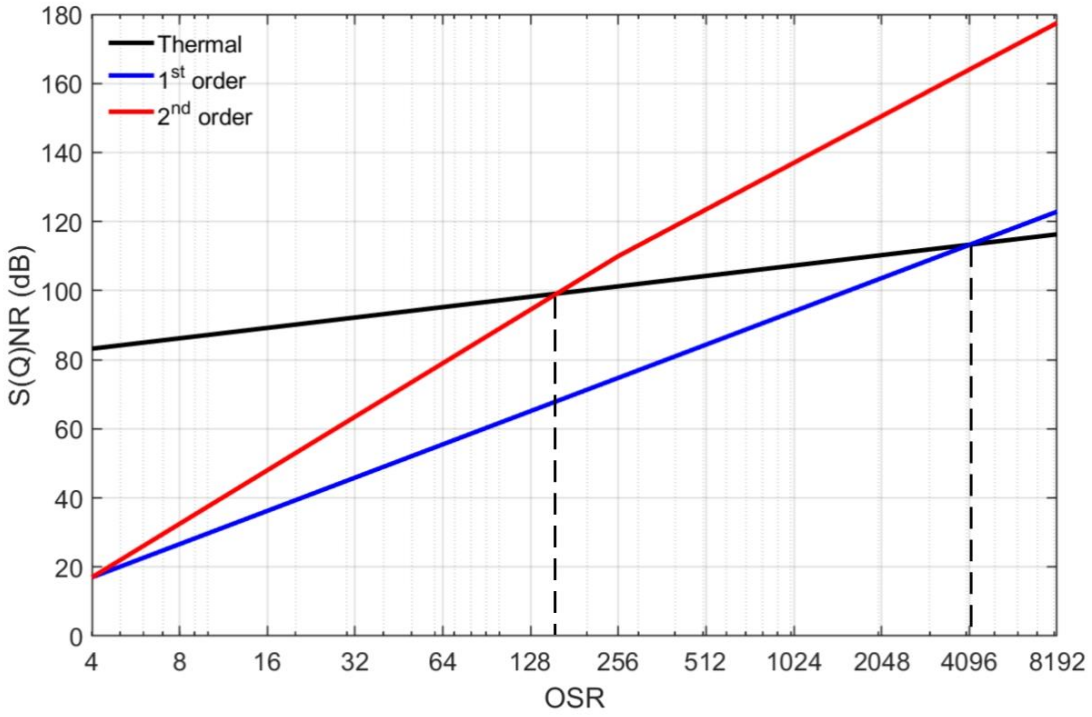


***Figure 3.11**: Comparison of the SNR of the front-end (f_s=20kHz) and the SQNR of a 1st and 2nd order DSM over its OSR.*

Figure 3.12 shows a block diagram of the feed-forward DSM. The first stage is realized by an active integrator, which will integrate the PTAT and CTAT current. Since the noise of the 2nd integrator is attenuated by the gain of the 1st integrator, it can be realized with an area-

efficient switched-capacitor integrator. A feed-forward topology is utilized since this ensures a smaller signal swing at the output of the 1st integrator [25].

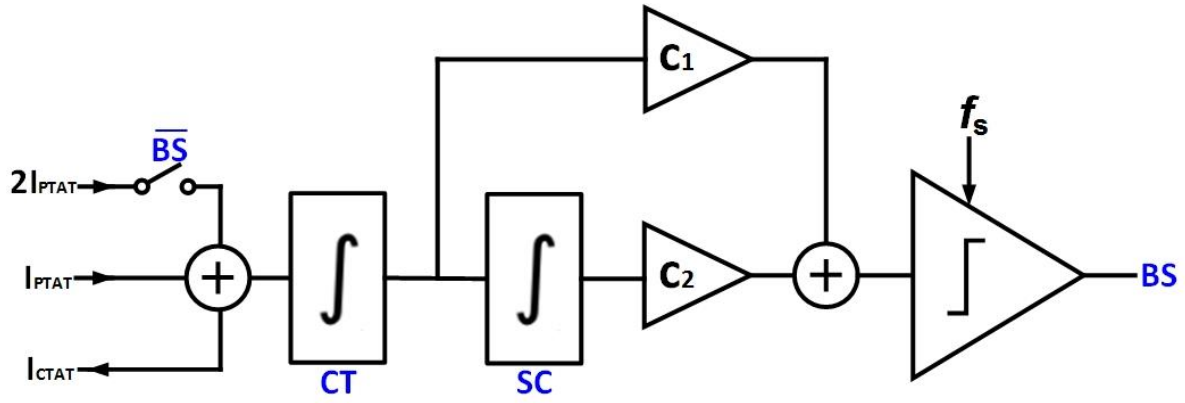


***Figure 3.12**: Block diagram of the feed-forward CT-DSM.*

3.2.1 Implementation of the 1st integrator

The first integrator has the important role of balancing the various currents while introducing little noise and signal degradation. Furthermore, it must force V_{BE} over the CTAT resistor, in order to create an accurate CTAT current. To achieve these, it needs to have a large gain, high speed, and sufficient current driving capability. An open-loop gain of at least 85dB is required to ensure that the gain error of V_{BE} to the virtual ground contributes an error smaller than 10mK.

For simplicity, the biasing current is mirrored from the PTAT current generated by the BJT front-end. Figure 3.13 shows the ratio of the integrated current over the biasing current, I_{int}/I_{bias}, over the temperature range. It can be observed that the maximum ratio is around 2 at the temperature extremes, which indicates the required current driving capability of the opamp. A gain-bandwidth product in the MHz range is required so that the overdrive voltage related to the voltage spikes at the input of the amplifier is minimal. In the previous chapter, it was explained that the DSM has a relaxed noise requirement since the noise is added to the CTAT current noise, which is attenuated when referred to ΔV_{BE}.

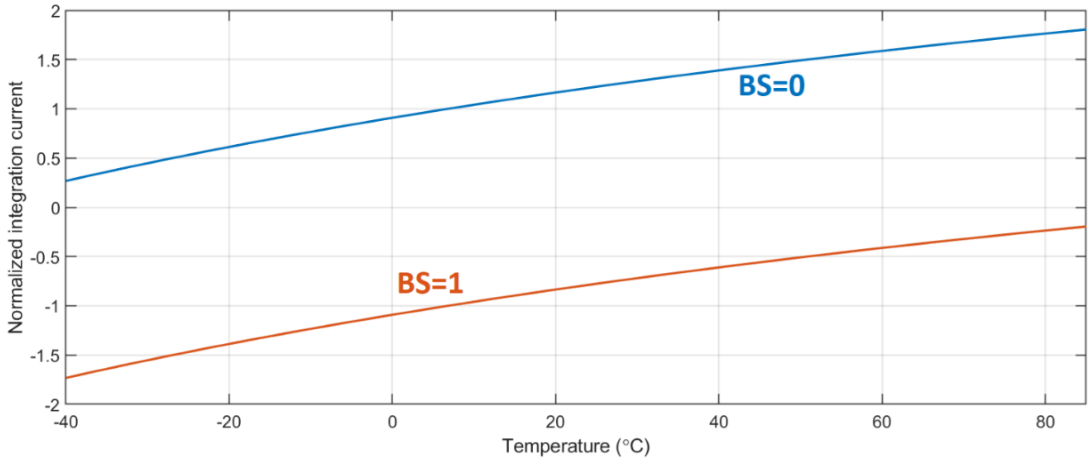


***Figure 3.13**: Integration current normalized to the bias current for both bitstream outcomes.*

Figure 3.14 shows the block diagram of the first integrator. The current flowing in or out of the DSM is integrated by the capacitor C_{int1}, which is sized to be 50pF to prevent clipping of the output voltage at temperature extremes for a clock frequency down to 20kHz. A two-stage topology was chosen to minimize the overdrive voltage and maximize the output voltage swing. The first stage is chopped in order to remove its offset and flicker noise [26], and a Miller capacitor and a nulling resistor are added to stabilize the amplifier.

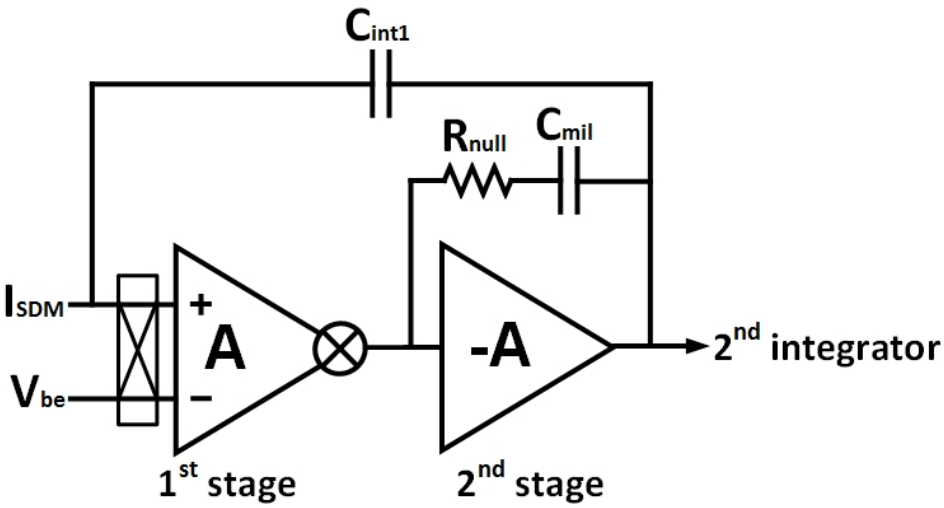


***Figure 3.14**: Block diagram of the CT first integrator.*

Figure 3.15 shows the schematic of the two-stage amplifier. The first stage is a telescopic cascode amplifier as in the front-end, whose bias voltages are reused. As in the bias amplifier, the high-g_m input transistors are medium-Vt so that they leave enough voltage headroom for the tail transistor. Since the noise requirements are not strict, each branch of the first stage uses the unity bias current (390nA at room temperature).

To ensure that the opamp can provide sufficient current over the full temperature range, the second stage draws 3.5 times the unity biasing current. As can be observed in Figure 3.10, this should be able to comfortably drive or sink the required integration current. For the amplifier to achieve high speed, the PMOS transistor in the output stage must have a large g_m, and thus a large W/L ratio. To achieve this while keeping the PMOS cascode of the first stage in saturation, a high-Vt PMOS is used. The output stage can supply a wide range of output voltages, which can range from 0.3V to 1.5V at V_{DD}=1.8V for a clock frequency of 20kHz at 85°C.

The amplifier achieves a worst-case open-loop gain of 110dB over corners, temperature, and its output current and voltage range. The 3MHz bandwidth ensures that the error due to switching transients at the input contributes a temperature error smaller than 20mK. A sub-mV overdrive voltage can be found between the input terminals of the amplifier, which is relative to the direction and magnitude of the integrated current. Since no net current flows into the DSM, this error will essentially be averaged out over time. The amplifier contributes less than 1% of the total noise power.

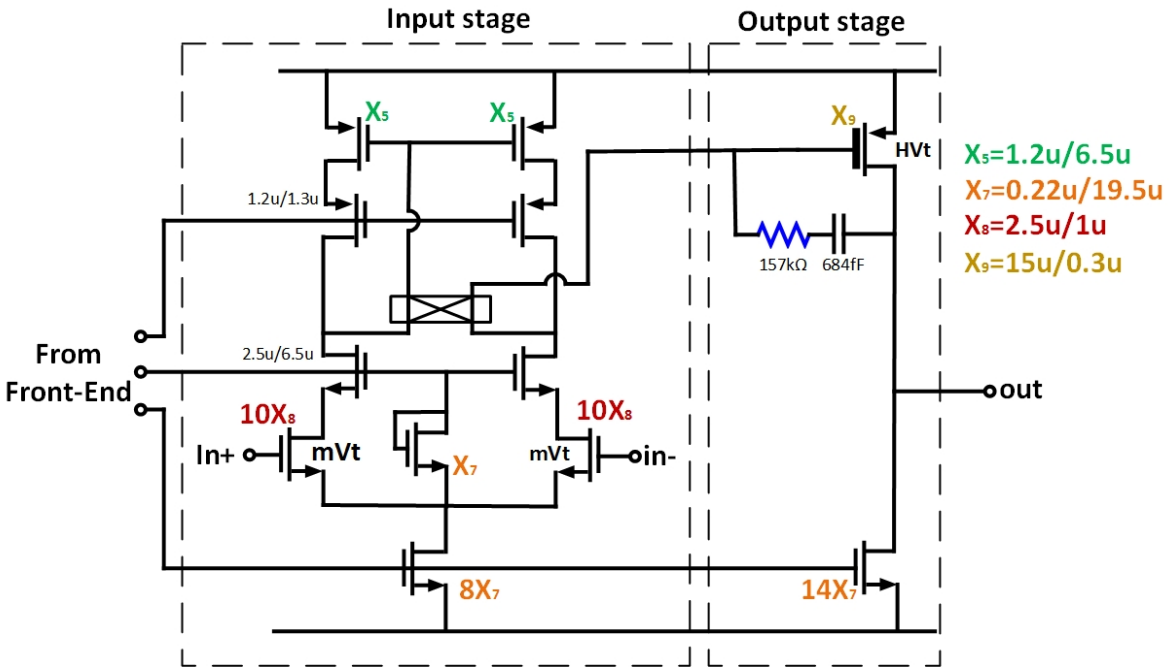


***Figure 3.15**: Schematic representation of the two-stage amplifier used in the first integrator.*

3.2.2 Implementation of the 2nd integrator

Figure 3.16 shows a diagram of the second integrator. It is a switched capacitor circuit, where ϕ_1 and ϕ_2 represent non-overlapping clocks. The reference voltage V_{cm} is the biasing voltage of the NMOS cascodes created in the front-end, which stays in the middle of the supply rails. In this way, no extra power and area are required for creating the common-mode (CM) voltage. Since the first integrator gain is sufficiently large, the sampling noise of the 100fF sampling capacitor (C_s) has a negligible contribution to the total noise. C_{ff} is 200fF in order to realize a feed-forward coefficient of 2. C_{int2}=1.2pF was scaled so that the output voltage of the 2nd stage stays between 0.6V and 1.2V over the temperature range, relaxing the amplifier's output swing requirement. When comparing the size of C_{int1} and C_{int2}, it becomes apparent that the choice for an SC 2nd integrator saves a significant amount of chip area.

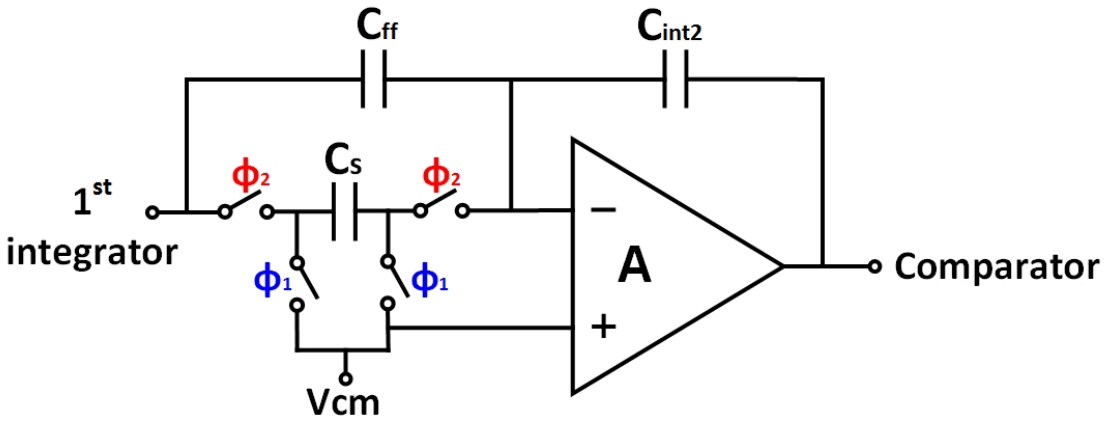


***Figure 3.16:** Block diagram of the SC second integrator.*

Since the opamp needs to function over a large input voltage range, a folded-cascode topology is used. The amplifier has a unity gain frequency of 1.4MHz, and a worst-case open-loop gain of 65dB, ensuring a sufficient overall loop gain of the filter. The 2nd integrator uses 3.5× less current than the 1st integrator.

3.4 Power and noise analysis

The simulated thermal noise contributions (referred to ΔV_{BE}) and current consumption of the several components at 27°C can be found in Table 2.1. The results agree with the noise estimations made in table 1.1. As desired, the DSM contributes less power and noise than the sensor front-end.

From the total noise of the circuit, it follows that a thermal noise floor of 0.19mK/√Hz can be achieved, which resembles the 0.18mK/√Hz that was expected when designing the DSM. When 9.28 µA is used from a 1.8V supply, a theoretical FoM of 590fJ°C^2 is obtained.

As mentioned in the previous chapter, the resistors and BJTs set the baseline for optimal noise performance. They consume 34% of the total current, while contributing 46% of the total noise power, indicating that the FoM could be further reduced 6× when compared to the theoretical limit.

Subcircuit	Component	Noise (nV/√Hz)	Noise power contribution (%)	Consumed current (µA)	Current usage (%)
Front-end	BJTs	21.7	8	4.64 (BJTs: 3.12)	50 (BJTs: 34)
	PTAT resistor	45.4	37		
	CTAT resistor	7.03	0.9		
	Current mirrors	30.1	16		
	Bias opamp	46.5	38	2.22	24
DSM	1st integrator	5.03	0.4	1.83	20
	2nd integrator	-	-	0.59	6
Full circuit		75.3	100	9.28	100

Table 2.1: *Table comparing the noise performance and current consumption of the circuit components.*

3.5 Signal generation

The clock signals which need to be generated include chopping signals for both the bias- and the first integrator amplifier, the non-overlapping clock signals for the SC 2nd integrator, and the triggering signal for the comparator. For flexibility, the DEM control signals are created off-chip by an FPGA.

In Figure 3.17 the timing of the various signals can be observed. To create the clocks with several phases, the signals are derived from a master clock with a frequency 4 times higher than the DSM frequency. After the comparator of the DSM is triggered, its output is sampled by the FPGA after ⅛ of a DSM period. The FPGA then receives another ⅛ of a DSM period to calculate the next DEM state before the result is loaded to the on-chip shift registers (SRs).

The non-overlapping 2nd integrator signals are synchronized with the SR enable signal so that their switching transients overlap. After this, the opamps are chopped.

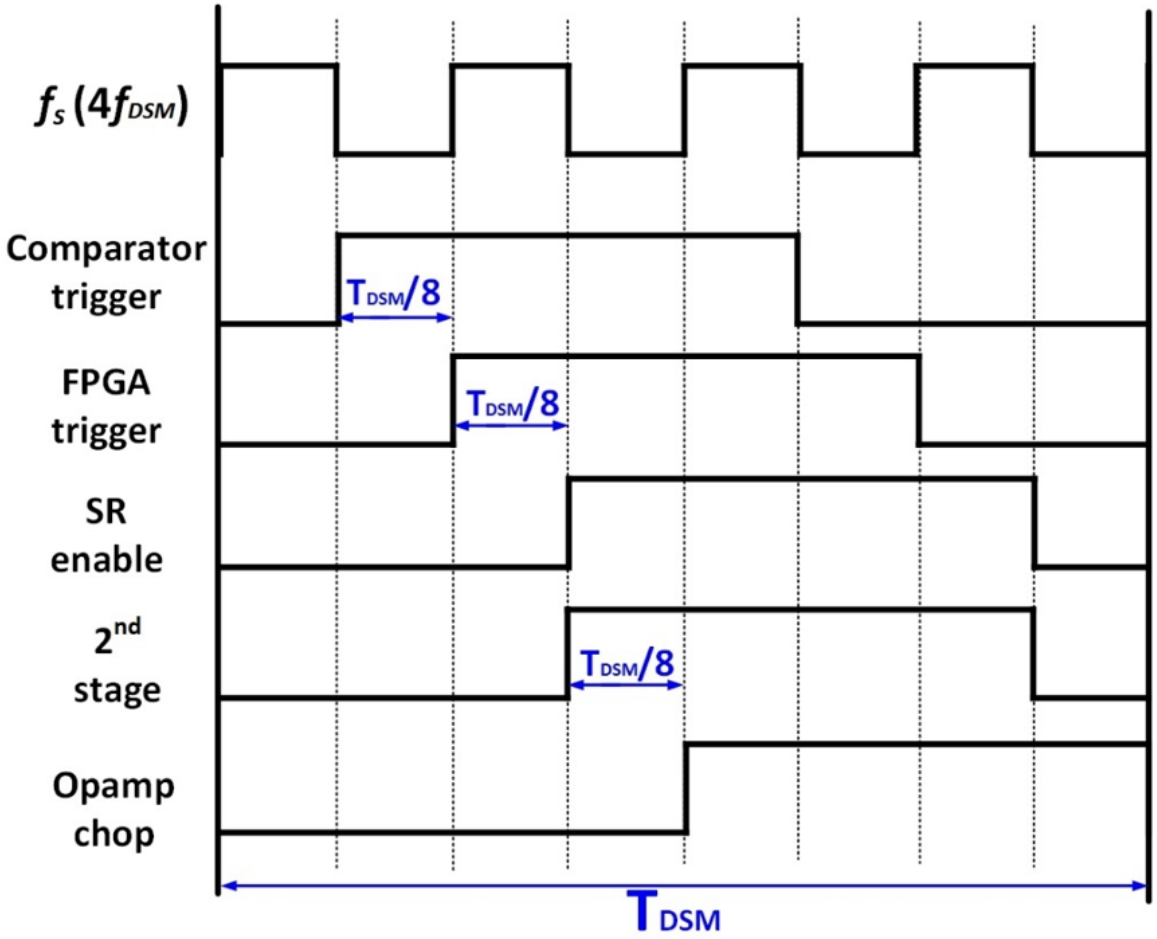


***Figure 3.17**: Timing diagram of the various control signals.*

3.6 Summary

In this chapter, the circuit implementation of the main blocks in the sensor was discussed, namely the BJT front-end and the DSM. After this, an analysis of the power and noise contributions of the several circuit components was done. Furthermore, a description of the signal generation was provided. The next chapter will introduce the various measurements performed on the taped-out chips.

4 Measurement results

The chip was fabricated in a TSMC 180nm CMOS process. The die micrograph can be observed in Figure 4.1 and 4.2. Two sensors were placed on a chip, so that differential measurement can be performed to cancel out the ambient temperature drift. The total die area is 1mm^2, while a single sensor occupies 0.13mm^2.

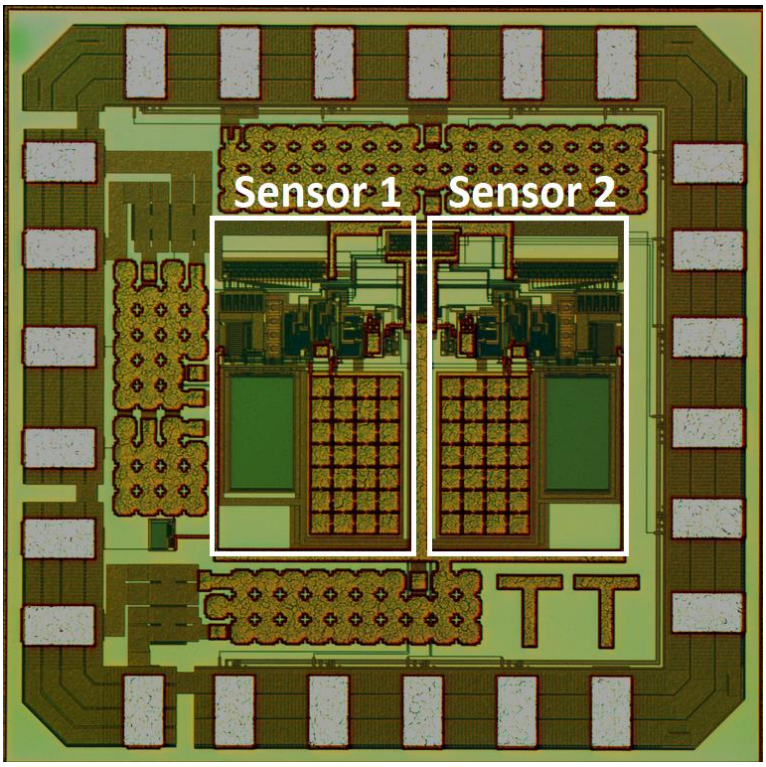


***Figure 4.1**: Die microphotograph.*

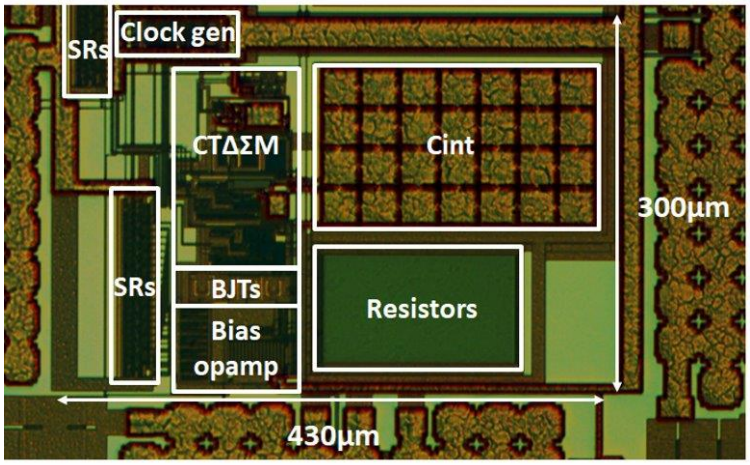


***Figure 4.2**: Zoomed in version of the die microphotograph.*

4.1 Measurement setup

In Figure 4.3 a block diagram of the measurement setup can be observed. The measurements were performed by placing the chips in a Votsch 7004 temperature-controlled oven and sweeping the temperature over the desired range. The chips are mounted on a PCB, which is bolted on a large metal block, which acts as a low-pass thermal filter. The temperature in the block is acquired from a Kelvin-connected Pt-100 temperature sensor placed inside the large metal block, such that the sensor temperature equals the Pt-100 temperature after the system achieves thermal equilibrium. The Pt-100, which inaccuracy is calibrated to 10mK, is read out by an 8.5-bit Keithley 2002 multimeter. The master clock is provided by a Keysight 33120A function generator. The DEM signals written to the on-chip shift-registers are generated by a Cyclone V DE1-SoC FPGA development board. The oven, function generator, multimeter, DC power supply, and FPGA are controlled by a PC, which also performs data acquisition.

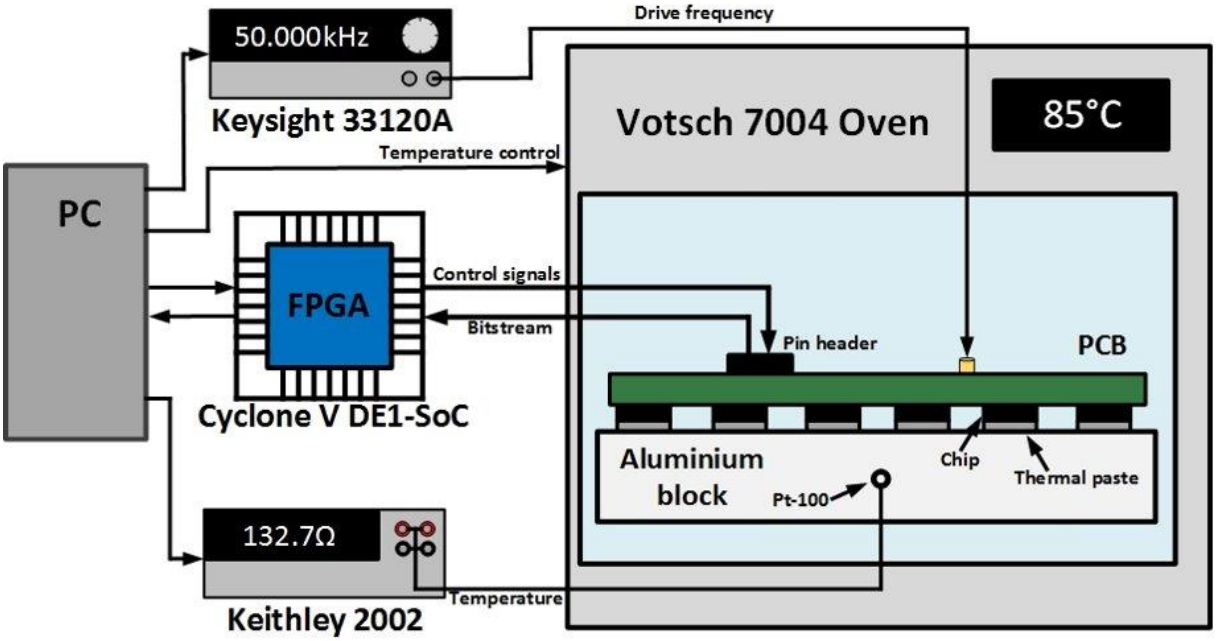


***Figure 4.3**: Block diagram of the measurement setup.*

4.2 Resolution

As presented in section 2.3, the DEM frequency should be chosen to achieve a good balance between folded quantization noise and remaining 1/f noise. Increasing the DSM sampling frequency helps mitigate this issue, but at the price of increased digital power. After testing different combinations, f_s of the DSM and the DEM frequency are set to f_s=50kHz and $f_{DEM}=f_s/64$, respectively. The sensor then draws 9.38µA from a 1.7V supply at 27°C, of which 6% is consumed by digital logic, as was expected from simulation.

The BJT's are swapped after a full DEM cycle, from which it follows that the BJT swapping frequency is 35.5Hz. A $sinc^2$ decimation filter is applied in order to filter out the high-frequency noise. Moreover, by setting the conversion time T_{conv} to be two complete BJT swapping cycles,

as shown in Figure 4.4, the DEM- and BJT swapping spikes can be eliminated by the notches of the decimation filter. As a result, a conversion consists of 64*11*2*2=2816 clock cycles, resulting in a 56.32ms conversion time.

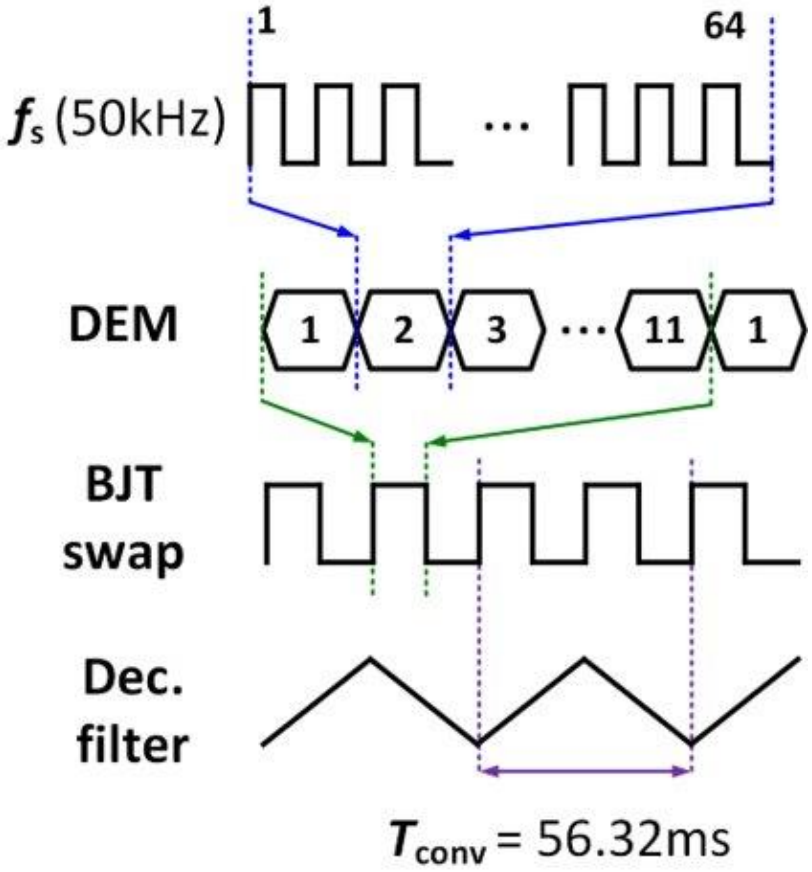


***Figure 4.4**: Timing diagram of a full conversion.*

Figure 4.5 shows the FFT resulting from a bitstream of 3000000 bits while the sensor runs freely without any resets in between. Two situations are shown: No dynamic techniques applied, and opamp chopping, current mirror and BJT DEM enabled. It can be observed that the flicker noise is cancelled by the dynamic techniques, and frequency spikes at integer multiples of 35.5Hz are introduced. These spikes are removed by the notches of the $sinc^2$ decimation filter, as shown in Figure 4.6.

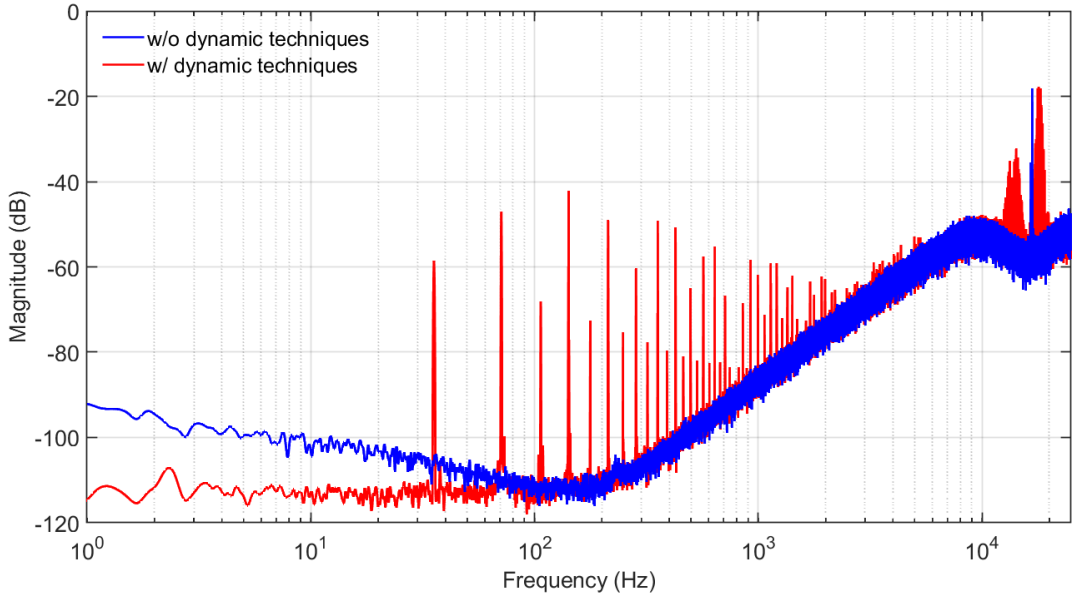


***Figure 4.5**: FFT comparing the noise spectrum before and after dynamic techniques are enabled.*

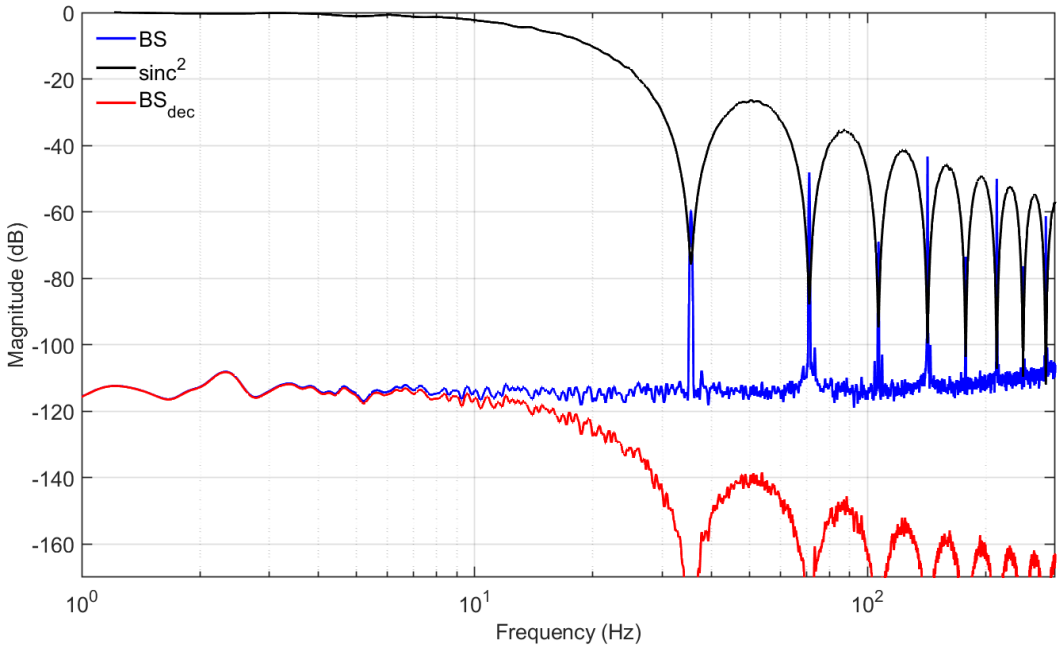


***Figure 4.6**: FFT comparing the raw bitstream, the sinc^2 filter, and the filtered bitstream.*

In Figure 4.7 the noise floor for three situations is shown: $f_{DEM}=f_s$, $f_{DEM}=f_s/64$ and $f_{DEM}=f_s/1024$. It can be observed how DEM'ing at f_s increases the noise floor due to current mirror mismatch residuals being modulated to the signal band. On the other hand, when $f_{DEM}=f_s/1024$, a full DEM cycle happens at 4.4Hz (50kHz/1024/11), meaning that a significant amount of flicker noise remains. This experiment validates the choice of $f_{DEM}=f_s/64$ for resolution optimization.

It follows that the full DEM-cycle frequency is 71Hz, which means that not all flicker noise from the current mirrors is removed. Because of this, the thermal noise floor is 3dB higher

than previously simulated, which constitutes a 2x increase in FoM. This was confirmed by simulation when the used DEM- and clock frequency are applied.

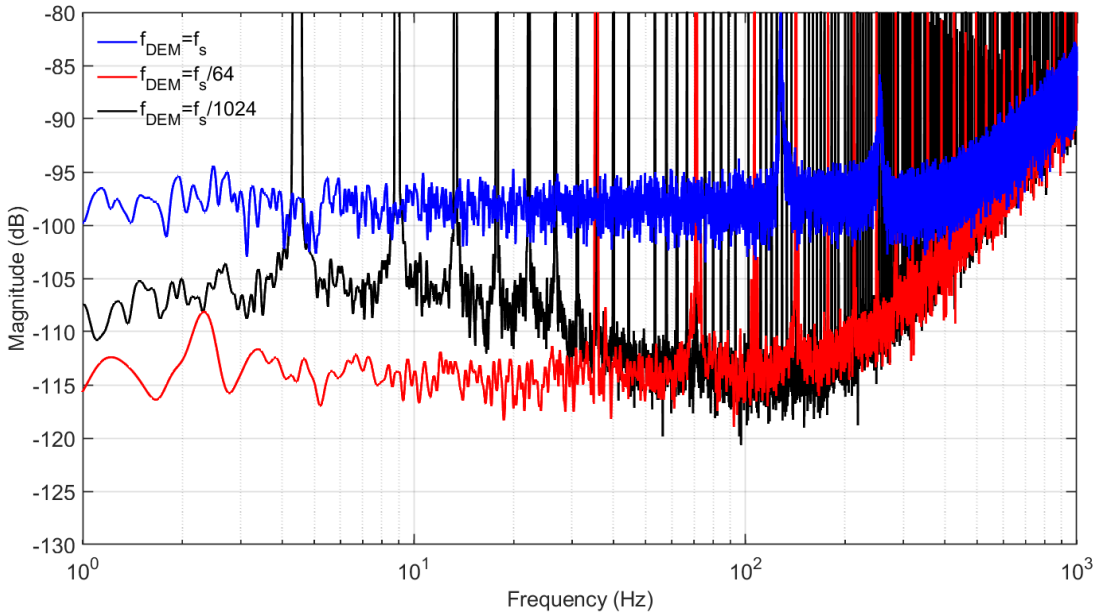


***Figure 4.7**: FFT comparing the noise floor for various DEM speeds.*

Figure 4.8 shows the resolution over conversion time for integer multiples of the conversion time corresponding to the applied sinc^2 window. Since the resolution is already thermal noise limited at the minimal T_{conv}, no quantization noise limited region can be observed. A noise density of 0.29mK/√Hz is found, which is higher than the simulated 0.19mK/√Hz due to the previously mentioned noise floor increase, and because the effective noise bandwidth of a sinc^2 filter is 1.33× larger than that of a brick-wall filter, resulting in a √1.33 higher noise density at the output [27].

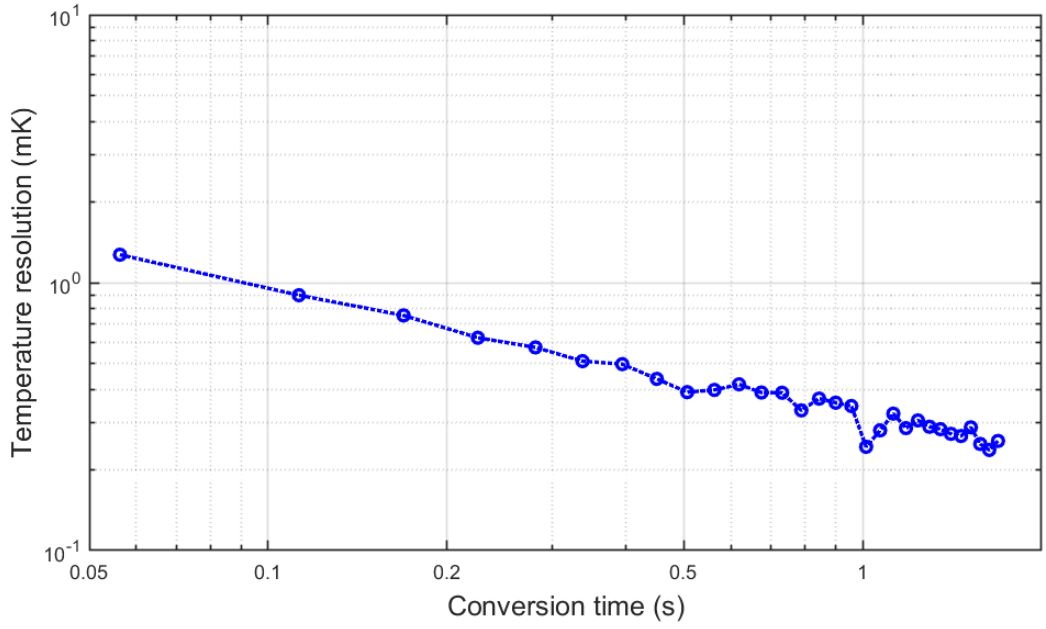


***Figure 4.8:** Plot showing the temperature resolution over conversion time after a sinc^2 decimation filter is applied.*

Figure 4.9 shows the FoM value over the conversion time at integer multiples of the minimum conversion time. Since a relatively quick conversion time (<100ms) is desired, the reported FoM of this sensor is 1.4pJC^2, achieving a 1.24mK resolution in 56.3ms, while drawing 9.4µA from a 1.7V supply. This is the highest reported energy efficiency for a high-accuracy TDC to date, surpassing the previous number of 5.4pJC^2.

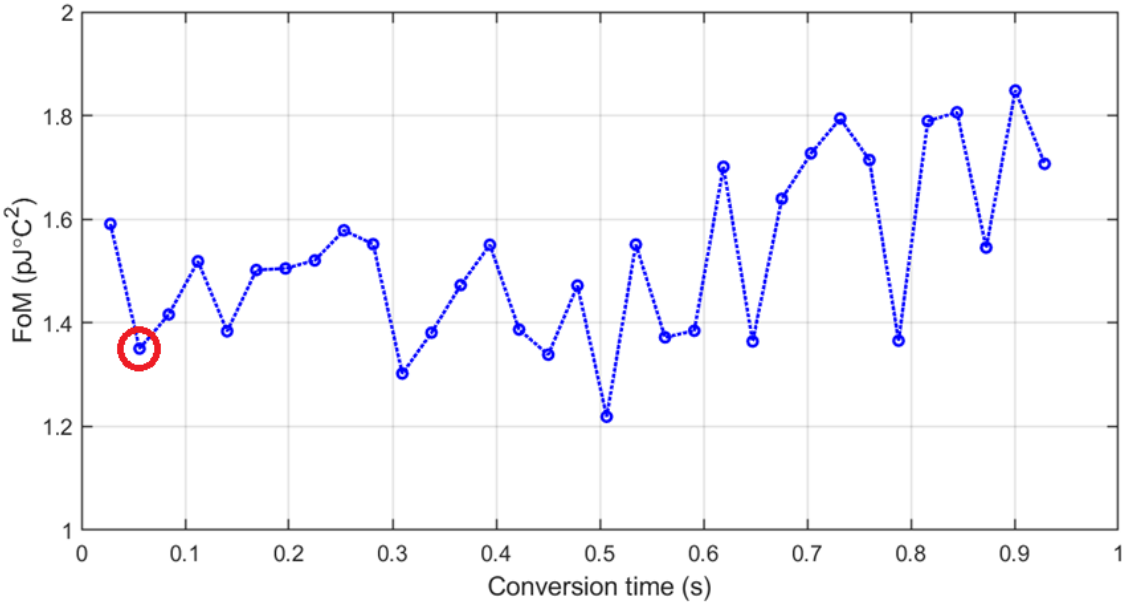


Figure 4.9: *Achieved resolution FoM over conversion time after a sinc^2 filter is applied.*

Figure 4.10 shows the FFT of the sinc^2 decimated bitstream (f_{conv}=17.8Hz). It can be observed that the 1/f noise corner has been reduced to 20mHz, showing the effectiveness of the dynamic techniques at removing flicker noise.

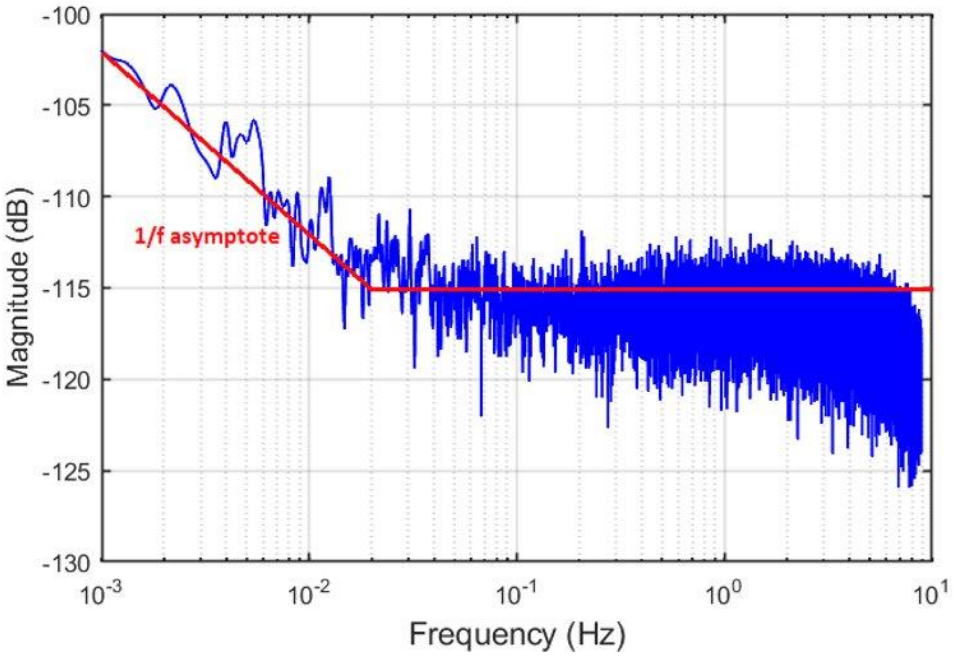


Figure 4.10*: FFT showing the flicker noise corner after dynamic techniques.*

4.3 Power supply sensitivity

The temperature change due to stepping the supply voltage from 1.6V to 2.2V at 27°C and 85°C can be seen in Figure 4.11. It can be observed that the change in temperature error increases as the supply voltage drops. As the supply voltage decreases, the gate voltage of the current mirrors in the front-end, and thus the output of the bias amp decreases. Because of this, the NMOS cascode of the bias amplifier approaches the triode region, which causes the temperature to fluctuate more at lower supply voltages. High temperatures provide the worst case, since currents are largest, meaning that the output voltage of the bias amp is the lowest. Since the power supply sensitivity (PSS) at 1.6V is unacceptably large, a PSS of 50mK/V from 1.7V to 2.2V is reported.

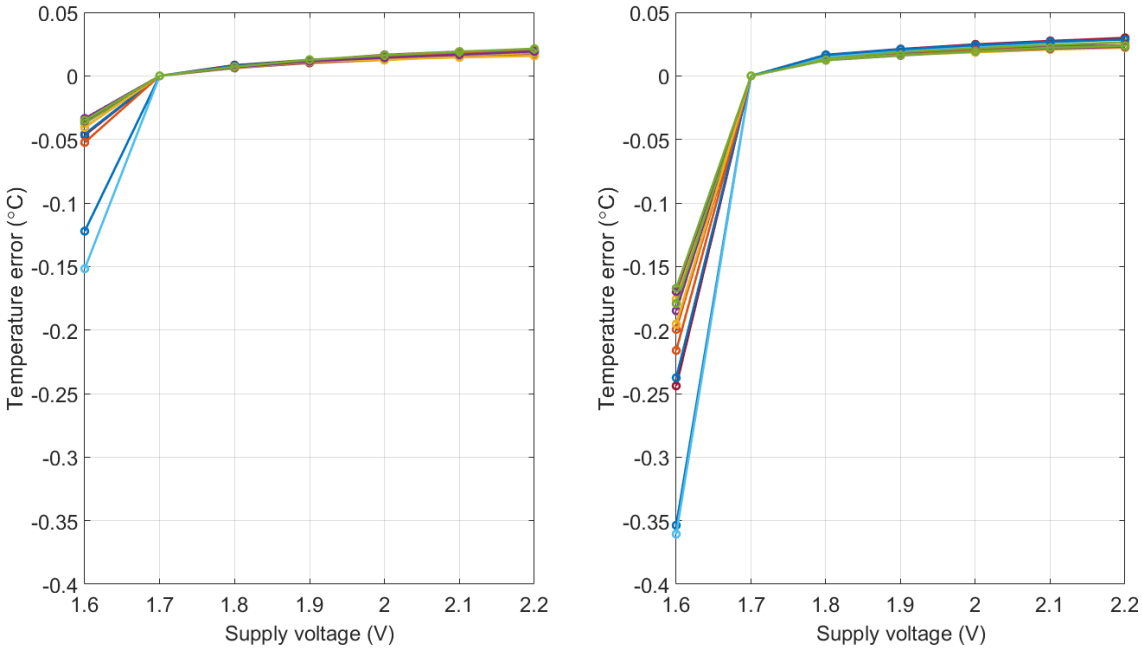


***Figure 4.11**: Power supply sensitivity for 12 sensors at 27°C (left) and 85°C (right).*

4.4 Accuracy

In Figure 4.12 the raw μ data of eighteen chips (36 sensors) has been characterized from –45°C to 85°C. A non-linear behaviour as in Figure 2.4 can be observed, accompanied by a slight offset spread.

The raw data is converted to temperature using equations (2.20)-(2.20), and the parameters used for this batch of chips are α=11.41, A=690.86, B=286.52. Since the residual nonlinearity of the 36 measured sensors after mathematical linearization is below ±10mK, a more complicated high-order (5^{th}) polynomial fit is not required. Figure 4.13 shows the untrimmed temperature spread of 18 chips (36 sensors) after linearization. As expected, the temperature spread is PTAT, due to the spread in V_{BE}. At 85°C a 3σ inaccuracy of ±0.5°C is found.

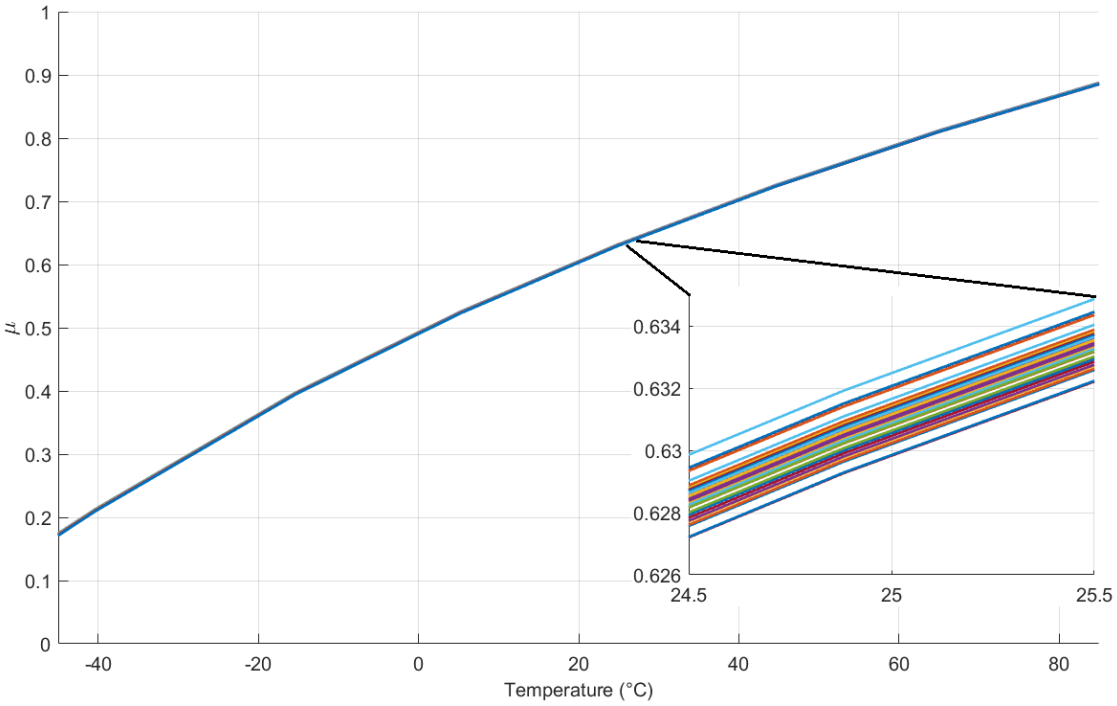


***Figure 4.12**: Raw measured output of the sensors over temperature.*

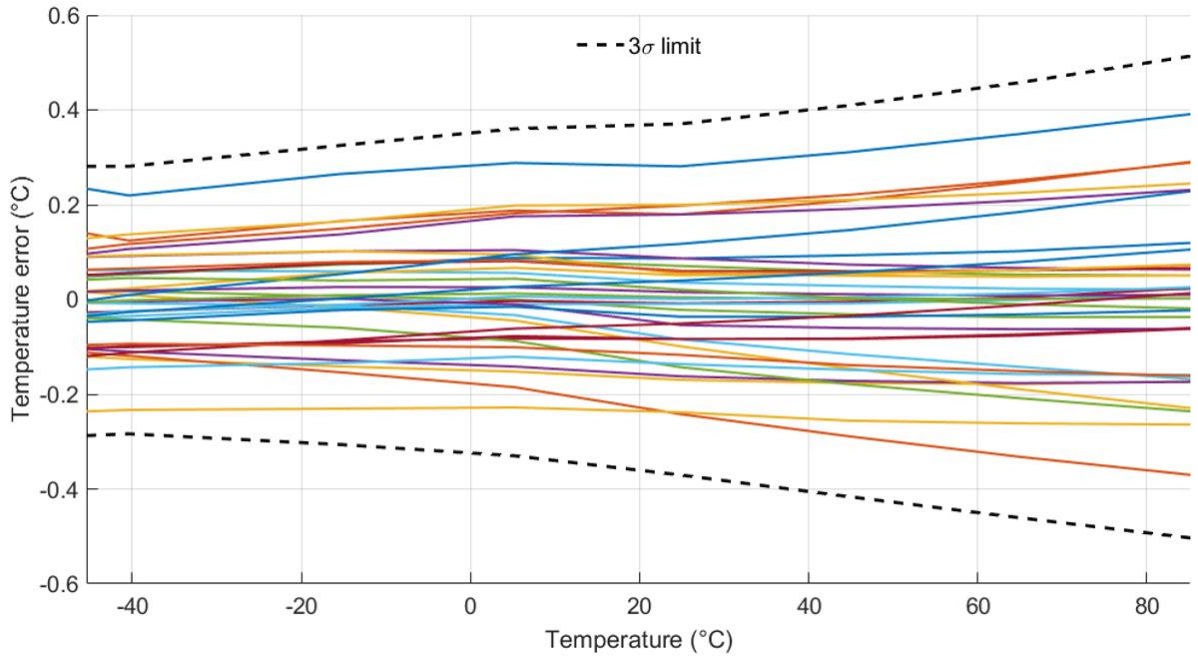


***Figure 4.13**: Untrimmed temperature spread of 36 sensors.*

The most effective way to trim this PTAT spread is to apply an offset trim before linearization [7]. The trim factors are acquired by measuring the output of the sensors at room temperature and calculating their difference to the average μ, after which they are applied to all measurements over the temperature range. Figure 4.14 shows the trimmed temperature spread of the 36 sensors. The 3σ temperature spread from -45°C to 85°C is improved to ±0.13°C (3σ). To take the limited sample size into account, a 0.15°C inaccuracy is reported.

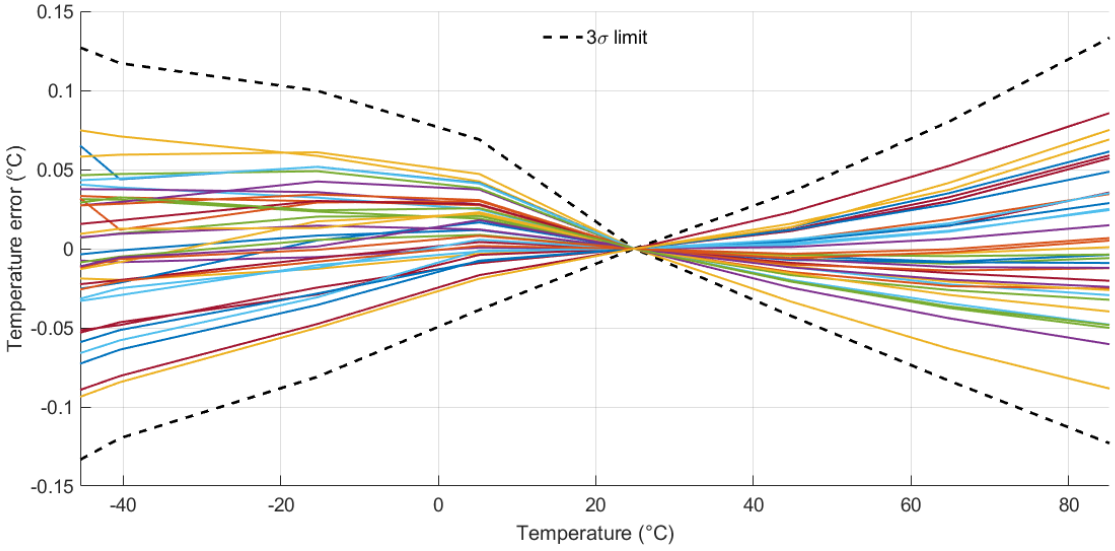


***Figure 4.14**: Trimmed temperature spread of 36 sensors.*

Table 4.1 presents the worst-case temperature spread of the 12 outlier sensors as the various dynamic techniques are enabled progressively. Since the sample size is small, the maximum error is reported rather than the 3σ values. It can be observed that chopping has the largest impact, as the opamp offset influences both the PTAT and the CTAT signal, instead of just the CTAT signal as in voltage-readout BJT temperature sensors. This is followed by current mirror DEM, which has to realize three different coefficients which all appear in the sensor's output. Lastly, it can be observed that the choice for applying BJT DEM was crucial to achieve this sensor's high accuracy.

Opamp chop	CM DEM	BJT DEM	Untrimmed InAcc. (max)	Trimmed InAcc. (max)
OFF	OFF	OFF	4800mK	2900mK
ON	OFF	OFF	1330mK	820mK
ON	ON	OFF	450mK	230mK
ON	ON	ON	390mK	90mK

***Table 4.1:** Table showing the impact of the error reduction techniques on the worst-case sensor accuracy.*

4.5 Higher clock frequencies

Strictly speaking, the sensor's resolution is not thermal-noise-limited, as it is partially determined by the remaining flicker noise due to the slow DEM. By further increasing the clock frequency, the DEM speed can be increased without added quantization-noise folding. A limitation here is the increase of digital power and the speed at which the FPGA can generate the DEM control signals. Figure 4.15 shows the FoM over integer multiples of a conversion time corresponding to the applied sinc^2 window at various clock frequencies. At f_s=100kHz, the achieved FoM approaches 1pJC^2 within the desired conversion time of 100ms. At this frequency, a full DEM cycle occurs at 142Hz, which is still below the simulated flicker noise corner (~200Hz). Due to an increase in digital power, the total current consumption increases to 9.97µA, meaning that 12% of the total power is now consumed by digital logic. It must also be mentioned that at these clock speeds, errors due to the raised sensitivity to switching transients will increase the temperature spread. However, since increasing the clock

frequency from 20kHz to 50kHz only increases the trimmed temperature spread by 5mK, it can be extrapolated that this effect will not be detrimental to the sensor's inaccuracy.

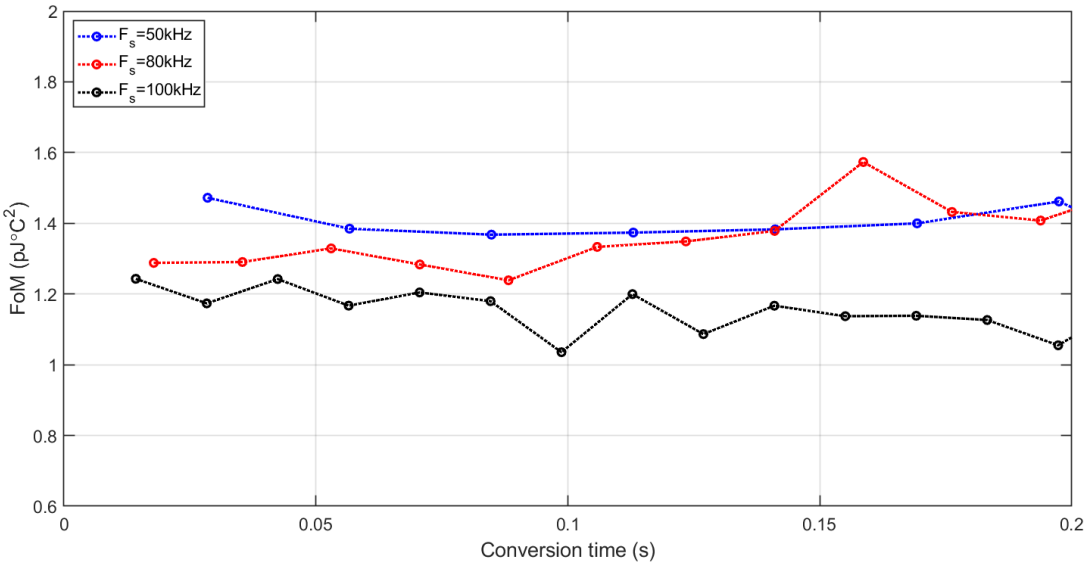


Figure 4.15: *Measured FoM over conversion time for several clock frequencies after a sinc² decimation filter is applied.*

4.6 Extended temperature range

The bitstream average of the sensor changes from 0.16 to 0.88 over the -45°C to 85°C temperature range. It was investigated how the sensor functions when measuring the military temperature range (-55°C to 125°C). Since the DSM clips at 125°C, a -55°C to 115°C range was used, where μ varies from 0.08 to 0.98. As shown in Figure 4.16, the sensor's worst-case spread at 115°C is ±0.2C (3σ), which can still be considered reasonable for a high-accuracy BJT temperature sensor.

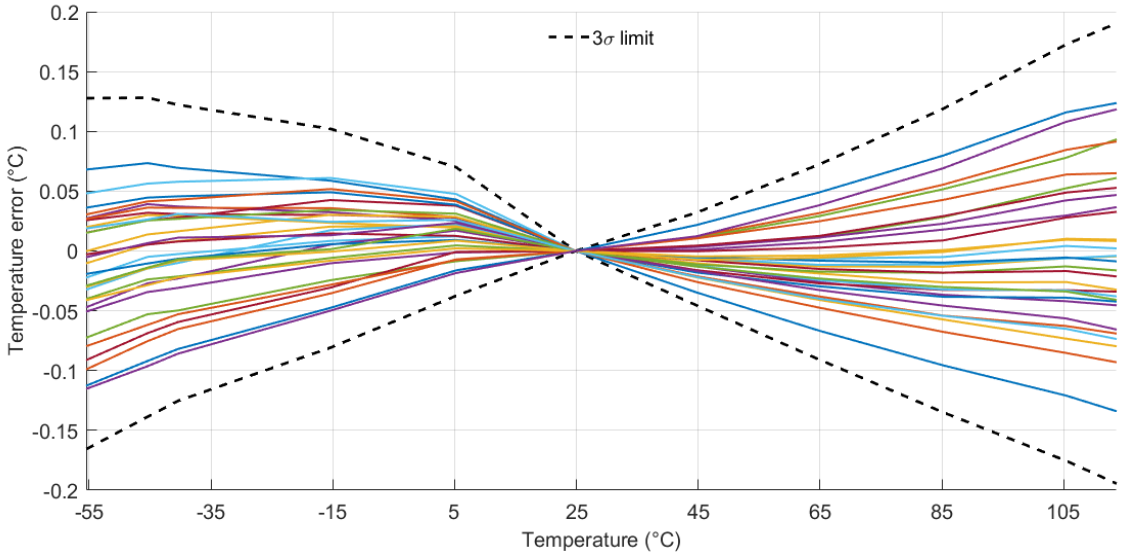


Figure 4.16: *Trimmed temperature spread of 36 sensors over a larger temperature range.*

4.7 Summary

In Table 4.2 the performance of the BJT temperature sensor is summarized and compared to other energy-efficient BJT designs. It can be observed that this sensor achieves the best reported FoM (1.4pJ°C^2) among high-accuracy BJT temperature sensors, while its accuracy (0.15°C (3σ) from -45°C to 85°C) is comparable to that of discrete-time designs.

	JSSC'17 [7]	CICC'21 [18]	ISSCC'14 [14]	ASSCC'19 [9]	ISSCC'20 [17]	**This work**
Sensor type	PNP	PNP	PNP	NPN	NPN	**PNP**
Architecture	DTΔΣM	DTΔΣM	DCM	CTΔΣM	CTΔΣM	**CTΔΣM**
Technology	0.16µm	55nm	0.7µm	0.18µm	0.11µm	**0.18µm**
Chip area [mm^2]	0.16	0.021	0.8	0.35	0.2	**0.12**
Supply current [µA]	4.6	2.2	55	5.5	550	**9.4**
Supply voltage [V]	1.5 to 2	1	2.9 to 5.5	1.6 to 2.2	1.125	**1.7 to 2.2**
Temperature range	-55°C to 125°C	-55°C to 125°C	-45°C to 130°C	-40°C to 125°C	-35°C to 95°C	**-45°C to 85°C**
3σInaccuracy [°C] after a 1-pt trim	±0.06	±0.77	±0.15	±0.13	-	**±0.15**
Resolution [mK]	15	15	3	1.27	0.65	**1.24**
Conversiontime [ms]	5	6.4	2.2	320	0.72	**56.3**
ResolutionFoM [pJ°C^2]	7.8	3.1	3.6	5.4	0.19	**1.4**

***Table 4.2**: Performance summary and comparison to the state-of-the-art*

5 Conclusion and Future work

A continuous-time, energy-efficient BJT-based temperature sensor has been designed which avoids the sampling noise that limits the energy efficiency of switched-capacitor implementations. The main novelty lies in the way the first integrator of the DSM creates the required CTAT current, which avoids introducing additional amplifiers and resistors. Together with the liberal use of dynamic error suppression techniques, the sensor achieves state-of-the-art energy efficiency while still maintaining competitive accuracy compared to earlier BJT temperature sensors. This work paves the way for continuous-time BJT temperature sensors aiming to push the boundaries of energy efficiency while still achieving high accuracy.

5.1 Future work

5.1.1 Higher energy efficiency

The first challenge is further improving the sensor's energy efficiency. A first step could be performing bitstream-controlled DEM [20] at f_s, which would cancel out all remaining current mirror flicker noise, while still avoiding quantization noise folding. With this setup, the chip's resolution will be purely limited by its thermal noise, meaning that the simulated FoM of 590fJ°C^2 could potentially be reached.

Another improvement to energy efficiency could be to experiment with adding a dynamically matched emitter area ratio as in [14]. In this way, a higher current density ratio can be reached using less current, but at the expense BJT and R_{PTAT} area, as well as a complex BJT DEM switching matrix.

5.1.2 Better accuracy

The second challenge is to achieve a high accuracy similar to that of discrete-time BJT temperature sensors, i.e., <0.1°C over the military temperature range (-55°C to 125°C). In this sensor, the main inaccuracy contributor after trimming is the spread of the PTAT/CTAT resistor ratio. One solution is to realize this ratio in the time-domain, i.e., the PTAT current is integrated 'm' times longer than the CTAT current. Since the clock periods are relatively long, a very accurate time ratio can be derived from an external master clock using on-chip frequency dividers. However, the DSM's first integrator needs to be biased at a larger current level to supply the large peak current from the BJT front-end, which increases the sensor's power use and reduces its energy efficiency.

A second method is to estimate the PTAT/CTAT resistor mismatch using 2 measurements and compensate for it digitally. For the first and the second measurement, the positive input of

the first integrator is connected to Q_1 and Q_2, respectively. By subtracting these two measurements the following expression is obtained:

$$\Delta\mu = \left(\frac{n}{n-1} - \frac{R_2}{R_1}\frac{V_{be1}}{k(n-1)\Delta V_{be}}\right) - \left(\frac{n}{n-1} - \frac{R_2}{R_1}\frac{V_{be2}}{k(n-1)\Delta V_{be}}\right) = \frac{R_2}{R_1}\frac{1}{k(n-1)} \tag{5.1}$$

A resistor mismatch compensated μ is then obtained by:

$$\mu_{R-comp} = \frac{\mu_{original} - \frac{n}{n-1}}{k(n-1)\Delta\mu} + \frac{n}{n-1} \tag{5.2}$$

This compensation would be performed before the room temperature trim. The effectiveness of this technique relies on the accuracy of the coefficients 'k' and 'n', which is ensured by DEM. The only required addition to the circuit would be an externally controlled switch that connects either one of the base-emitter voltages in the front-end to the DSM, as can be seen in Figure 5.1. Since temperature is not present in the calibration equation, such measurements can be done at any temperature, as long as it remains the same during both measurements. This property minimizes the added cost.

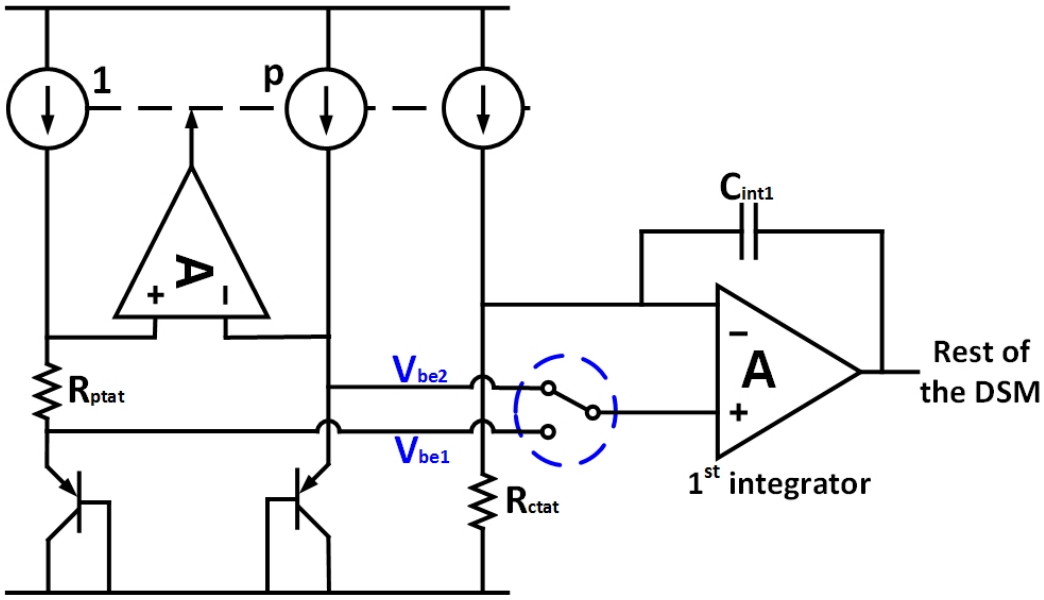


Figure 5.1: *Circuit diagram showing the required switches for resistor mismatch calibration.*

5.1.3 Covering the military temperature range

As discussed in section 4.6, this DSM's output clips at temperatures higher than 115°C. If the sensor must be able to measure over the -55°C to 125°C military temperature range, the coefficients defined in section 2.2 will have to be redesigned. If the BJT collector current ratio remains p=7, then k=1, n=4 and m=6 result in a μ which effectively uses the DSM's dynamic range over the military temperature range, as shown in Figure 5.2.

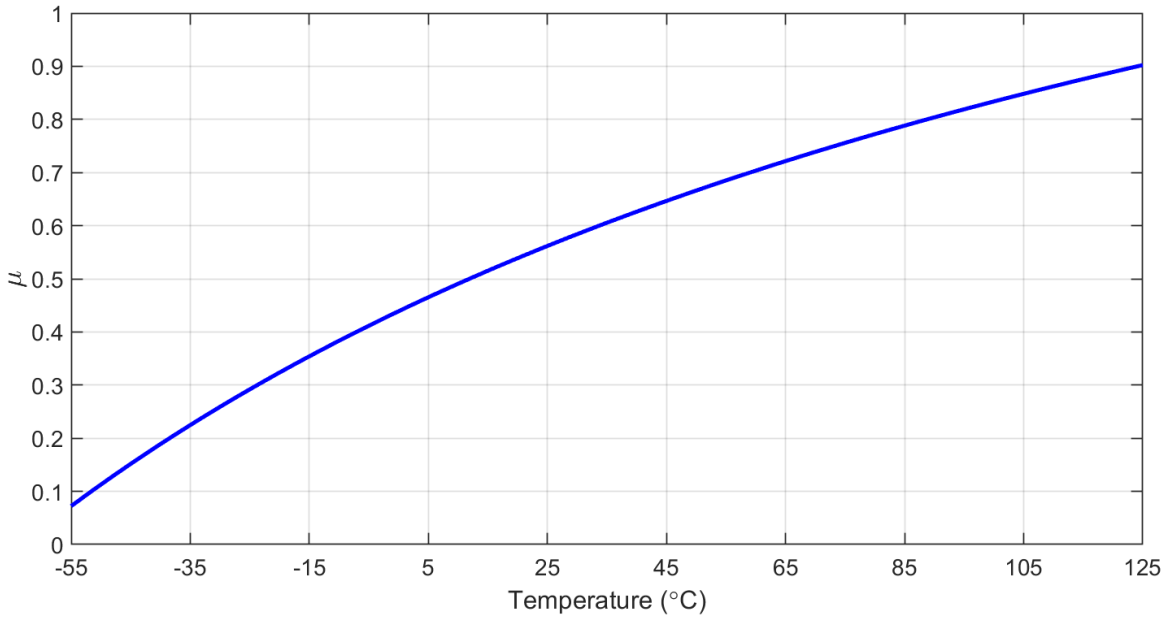


Figure 5.2: *Bitstream average over the military temperature range for p=7, k=1, n=4, m=6.*

Here, μ ranges from 0.08 to 0.90, meaning that the DSM range is used more effectively than for the sensor proposed in this thesis (72%→82%). Because of this, the required oversampling ratio of the DSM to reduce the quantization noise below the thermal noise will be similar, even though the proposed temperature range is larger. An added advantage of these coefficients is that the resistor ratio is reduced from m=8 to m=6, meaning that better matching can be achieved for the same total resistor area. Since the DAC current ratio increased from n=3 to n=4 in this setup, the readout circuit will consume $1 \cdot I_{PTAT}$ more current than in the sensor presented in this thesis, from which a 4% power increase follows.

5.1.4 Conclusion

Since the proposed modifications require only moderate adjustments to the circuit, their implementation can be assumed to be feasible. They theoretically make it possible to achieve a resolution FoM well below $1pJC^2$, while achieving an accuracy towards 0.1°C over the military temperature range, as switched-capacitor BJT sensors are known to achieve.

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