A Doherty-Like Class-G HoC SCPA

With Deep Power Back-Off Efficiency Enhancement

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by

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Introduction

1.1. Motivation

In the world of today, the need for information and connectivity is evergrowing. Communicating through physical media is no longer feasible anymore because of the sheer amount of 'connected' devices. The popular choice of communication nowadays is wireless. These devices can be used for different applications such as: mass data, remote measuring, wearables, automation, and many more. However, they all share two common requirements of low-cost and high power efficiency. In most, if not all, wireless IC designs, the PA is the most power-hungry component. Hence achieving high power efficiency is most effective by improving the overall efficiency of the PA. With the increasing demand for higher data rates, more advanced modulation techniques are required, such as QAM, where two amplitude modulation signals are combined into a single channel. High order QAM improves spectral efficiency at the cost of a larger dynamic range. This leads to a larger peak-to-average power ratio (PAPR) reducing energy efficiency in traditional PAs. Therefore, the average or back-off efficiency is just as important as the peak efficiency in modern modulation techniques.

1.2. Key design specifications for power amplifiers

In this section, a brief concept on the PA will be introduced together with some important FOM and parameters. Understanding the FOM's is required in order to assess and compare the performance, advantages, and disadvantages of different types of PA topologies.

1.2.1. Output power

Output power is one of the FOM and the most important one, else the word power in power amplifier would be meaningless. The supply of a PA is often a fixed voltage, making the current the only design parameter to set the required output power.

Where the current can be set by the load that is presented to the PA. The output power is then given as:

$$P_{OUT} = \frac{\left(\frac{V_{pk-pk}}{2}\right)^2}{2\ R_L} \tag{1.1}$$

In RF applications, the power level is often defined in dBm. A decibel value referenced to 1 mW or 0 dBm. The advantage of the power unit compared to the voltage unit is that it is independent of the media. An RF signal with a power of 0 dBm terminated by a matched 50 Ω load will have a peak-to-peak voltage swing of 0.632 V. However, if the termination or medium is not 50 Ω, the voltage swing would change. Even though the power is the same.

1.2.2. Efficiency

With the increasing demand for portable devices, battery life is an important factor and is closely related to the efficiency of the PA. Since PA operation requires high current consumption any power wasted as heat reduces the battery life significantly. Thus, the efficiency is critical to wireless applications. However, even for non-battery-powered devices the heat generated by low efficiency devices may cause design limitations or reduced reliability. In literature two definitions of efficiency are commonly used [1]:

$$\eta = \frac{P_L}{P_{DC}} \tag{1.2}$$

Drain efficiency or collector efficiency for bipolar implementations is the ratio of the average output power delivered to the load (P_L) to the average power drawn from the supply voltage (P_{DC}).

$$PAE = \frac{P_L - P_{IN}}{P_{DC}} \tag{1.3}$$

Power Added Efficiency also takes into account the input power of the PA. In some cases where the PA has a low gain, this can be significant compared to the output power.

1.2.3. Linearity

The linearity of a PA is defined as how the quality of an input signal is maintained at the output of the PA after amplification. A popular way of encoding information in a wireless signal is to modulate both the amplitude and the phase of the signal. Such signals exhibit high bandwidth efficiency, which is the frequency bandwidth required to support a certain data rate. However, this also poses strict requirements on the the PA as good linearity is needed to maintain the amplitude variation of the original input signal [2]. However, since conventional linear PAs are less efficient than non-linear PAs, methods to improve the linearity of PAs have gained much interest [3]. Such methods use fixed amplitude signals in which the information is only encoded into phase variation. The advantage of this is that the non-linearity

of the PA has negligible effect on the signal degradation.

There are many ways that a PA can distort a signal, and the linearity of a PA is therefore not characterized by a single definition. As this work focuses on the digital PA, two important definitions will be discussed here; AM-AM and AM-PM.

AM-AM distortion represents the input-output relation of a PA excited by a sinusoidal input, or in the case for a digital PA by the input code, over the entire operational power range. As AM-AM directly relates the input to the output, it holds a lot of information, such as the 1 dB compression point or the gain fluctuations. Similarly, AM-PM distortion represents the phase variation throughout the entire operational power range. Together the AM-AM and AM-PM describe the ability of the PA to accurately reproduce the amplitude and phase of the input signal. Distortion in the amplitude and/or phase of a signal have a detrimental effect on identifying the right constellation points.

1.3. Background study of state-of-the-art transmitters

For I/Q transmitters (TXs), the (back-off) efficiency can be improved by quadrature IQ sharing [4] or reducing the phase difference between the I and Q vectors [5]. Other techniques that have been successfully implemented are, outphasing [6], Doherty [7, 8, 9], dynamic impedance modulation [10], supply modulation [11], switched-capacitor class-G [7, 9, 12, 13] or HoC switched-capacitor power amplifier [14]. Class-G efficiency enhancement technique is based on switching behavior, making it an attractive option for standard CMOS processes and is quickly adopted in more advanced smaller technology nodes. However, most implementations exploit two external supplies, effectively moving the complexity off-chip and increasing the bill of materials (BOM). However, in [13] and [14] two different techniques were used that take advantage of class-G switching while only using a single supply. In chapter 2, these techniques will be elaborated, and our proposed TX topology that combines both of them will be presented. Improving deep PBO efficiency even further while still only using a single supply.

1.4. Thesis objective and target specifications

Based on the explanations in section 1.1 and section 1.3, the objective of this thesis is to implement a TX with an innovative deep PBO enhancement technique improving the PBO efficiency by extending the efficiency peaking beyond 6 dB PBO. The proposed TX should be complaint with the two cellular IoT standards based on Long Term Evolution (LTE): Cat-M1 [subtype of enahnced machine type communication (eMTC)] [15] and Cat-NB1 [subtype of narrow band (NB)-IoT] [16]. Which was introduced by the 3rd Generation Partnership Project (3GPP). The TX power control as defined by 3GPP ranges from 23 dBm down to −40 dBm. The Cat-M1 and Cat-NB1 signals can have a high PAPR vlaues (>0 dB), further supporting the goal of

achieving efficiency peaking beyond 6 dB PBO. To be competitive with current state-of-the-art TXs the efficiency at peak power should be at least 30 %. A summary of the target design specifications are provided in Table 1.1.

Table 1.1: Design target specifications of the proposed TX.

Specification	Value	Remark
Supply voltage	2.0 V to 2.2 V	also 1.0 V to 1.1 V supply needed for digital
Efficiency peak	6 dB and 6 dB PBO	-
Frequency range	700 MHz to 900 MHz	optional support for 1800 MHz
Peak output power	26 dBm	23 dBm plus 3 dB margin
PAE@peak	>30 %	-

1.5. Thesis outline

In chapter 2, the concept of the deep power back-off enhancement technique is discussed. In this context, two efficiency enhancement techniques are combined creating three efficiency peaks at peak power, 6 dB PBO and 12 dB PBO. Using only a single supply. In chapter 3, the concept of chapter 2 is converted into a TX prototype. A full explanation is giving on the operating principle of a single PA-cell. This PA-cell forms the building block for the final PA design. In chapter 4, the complete PA design will be discussed. Design choices such as increasing the PA amplitude resolution or further improving energy efficiency by employing a Doherty-like switching scheme are explained. In chapter 5, the digital design which controls the PA is briefly addressed. Finally, in chapter 6, the PA measurement results are shown.

2

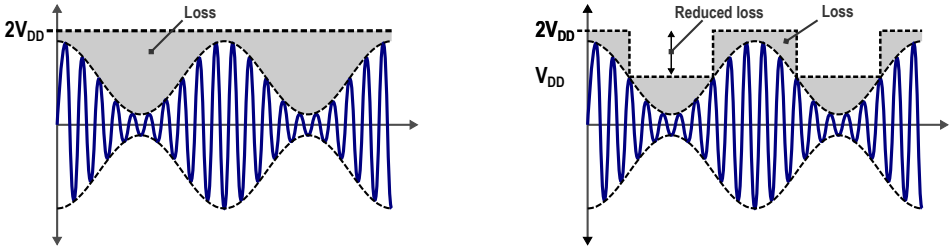
Concept creation

In this chapter, the conceptual design process that led to the final design will be described. First, the main objective of the concept is given in section 2.1. Fulfilling this objective is done by combining two already proven designs, as will be discussed in section 2.2. The fundamental principle of operation of the concept will be introduced in section 2.3.

2.1. Main concept objective

The PA's primary task is to boost the RF power level of the input signal efficiently. The efficiency requirement becomes even more important in the world of IoT and portable devices. Often these devices are battery-powered and require a long operation time. With the PA being the dominant energy dissipator, increasing its efficiency can have a considerate effect on the battery lifetime. Non-constant envelope modulation is nowadays the norm for high spectral efficiency in modern communication standards. The drawback for this non-constant evelope modulation is the increasing PAPR. In a linear PA, the output voltage varies over time while the supply voltage remains constant as ilustrated in Figure 2.1(a). The voltage difference is wasted power and hence as the output voltage is low the efficiency is low. The increased PAPR in modern communication makes matters worse as the probability for signals with lower output power increases.

A solution to regain efficiency for low output power is to also reduce the supply voltage, effectively reducing the voltage difference between the output and supply, as is demonstrated in Figure 2.1(b). In recent years this technique (class-G Supply switching) has been implemented successfully [7, 11, 12, 17]. The drawback, however, is that the complexity is shifted off-chip to the power management circuits on the PCB. A second power circuit is needed to provide the second supply voltage. The target should be to 'generate' the extra supply voltage(s) that are used in class-G PAs without the need of external circuitry, solving the problem in the chip itself.



(a) Power loss mechanism for a conventional PA without PBO enhancements with non-constant amplitude modulation.

(b) Power loss mechanism for a class-G PA with PBO enhancement with non-constant amplitude modulation.

Figure 2.1: The power loss for a conventional and class-G PA, showing the reduced loss when reducing the supply voltage in the class-G PA.

2.2. Proposed approach

For digital power amplifiers the switched-capacitor topology is a popular topology for its superior linearity [18]. A simplified SCPA topology is shown in Figure 2.2. The output amplitude of such an SCPA is defined by the ratio of capacitors that are switching between V_{DD} and V_{GND} to the total number of capacitors. The charge of the switching capacitors is redistributed over the total capacitance. This enables precise generation of any voltage level between V_{DD} and V_{GND}. Consider a capacitor bank of four capacitors equal in size in an SCPA as depicted in Figure 2.2. If three of the four capacitors have their bottom plates connected to V_{GND} while the fourth capacitor's bottom plate is switching between V_{DD} and V_{GND}, the voltage on the top plate changes by $V_{DD}/4$ due to the charge distribution. This, however, does not solve the efficiency problem as the efficiency is proportional to the effective capacitance in the SC array that is switched [18].

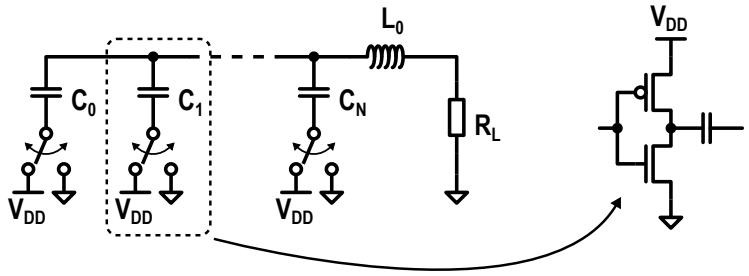


Figure 2.2: A conventional SCPA with output capacitor array C_0 to C_N where each capacitor can be statically driven low (inactive) or driven by an LO signal injecting energy to the load (R_L) by switching between two different voltage potentials (V_{DD} and V_{GND}).

The energy efficiency can be improved by realizing class-G functionality by adding a second power supply voltage, as illustrated in Figure 2.3. This class-G functionality is easily achieved in the SCPA topology as it requires only an additional bottom plate switch for each capacitor in the array. The additional supply voltage makes it possible to keep the ratio of switching capacitors to static capacitors high and, therefore, higher efficiency. However, as mentioned above, it does require a second external voltage supply which is unwanted.

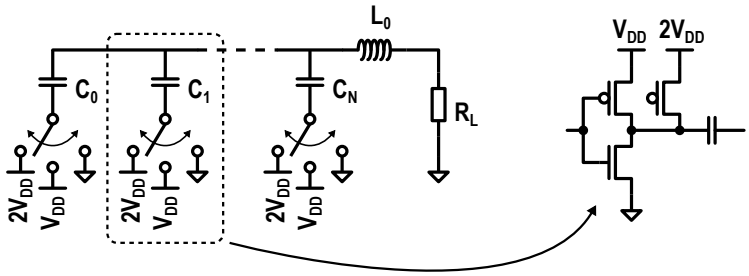


Figure 2.3: A class-G SCPA with output capacitor array C_0 to C_N where each capacitor can be statically driven low (inactive) or driven by an LO signal injecting energy to the load (R_L) by switching between two different voltage potentials. For maximum added power, the switch drives the capacitor between $2V_{DD}$ and V_{GND}, for 6 dB PBO between V_{DD} and V_{GND}.

The next goal is to generate the second supply voltage on-chip. Generating a different supply voltage from the main supply is very common in the world of power conversion. In [14], a technique that found its way from the power converters was used to implement the extra supply voltage needed in the PA for the efficiency enhancement in PBO operation. By implementing PA cells as flying domain switched-capacitor DC-DC converter cells, a supply voltage that is half the voltage of the main supply is inherently generated with potentially high efficiency. In Figure 2.4, the flying capacitor C_{fly} will perform charge sharing with the stacked capacitors C_{SH} and C_{SL} effectively becoming a $2:1$ switched-capacitor DC-DC converter. By strategically closing the switches in the HoC, structure each capacitor in the SC array can be switched between $2V_{DD}$, V_{DD} and V_{GND}, as will be discussed in detail in chapter 3.

In [13], a different technique was used to generate the half supply voltage. To facilitate this technique, the simplified topology has to be changed in a differential structure, as shown in Figure 2.5. During the first phase of the LO signal, the left plate of C_p is connected to $2V_{DD}$ and the left plate of C_n is connected to V_{GND}. In the second phase of the LO signal the left plate of C_p and C_n are shorted together. This short-circuit path provides a current path for the resonating current through the balun and the capcitors, it also causes the left plates which are now the same node to settle to V_{DD}. This arrangement effectively generates the required half supply voltage.

The objective of this work is to increase the PA's efficiency while operating at

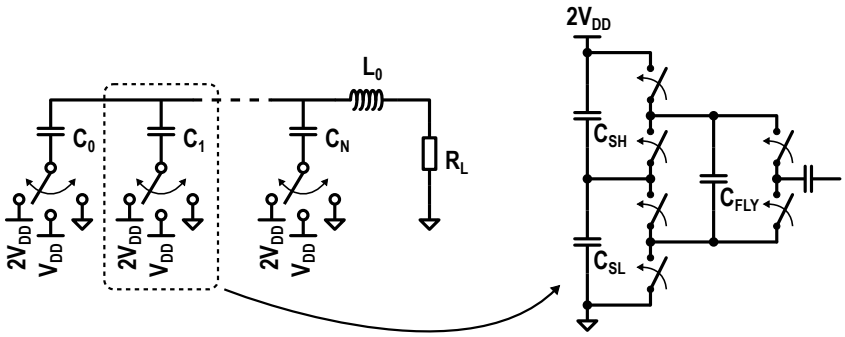


Figure 2.4: A class-G single supply HOC SCPA with output capacitor array C_0 to C_N where each capacitor can be statically driven low (inactive) or driven by an LO signal injecting energy to the load (R_L) by switching between two different voltage potentials. For maximum added power, the switch drives the capacitor between $2V_{DD}$ and V_{GND}, for 6 dB PBO between V_{DD} and V_{GND}.

even deeper PBO. This would require not only an efficiency peak at -6 dB but also at -12 dB. The previously mentioned techniques both add an efficiency peak at 6 dB PBO by generating a half supply voltage from the main supply. The main idea of this work is to combine the highlighted works to not only generate a half supply voltage from the main supply, but also a quarter supply voltage. In theory, one technique would provide an efficiency peak at -6 dB PBO and the other technique a peak at -12 dB PBO. Figure 2.6 shows this proposed combined topology of both using the House-of-Cards and output shorting topologies.

2.3. The four PBO modes

The proposed concept of this work uses the two existing designs to enhance the efficiency at not only 6 dB PBO but also 12 dB PBO. This means that there are four distinct operating modes the PA can operate in; full power or 0 dB PBO, -6 dB, -12 dB and off. In this section, the principle of operation for each of these PBO modes will be discussed.

At full power, the HoC structure is used to switch the array capacitors between $2V_{DD}$ and V_{GND}. The output-short switch is open during both phases of the LO signal. When the output power is reduced to -6 dB, the half supply node of the HoC structure is used such that the array capacitors are switching between either $2V_{DD}$ and V_{DD} or V_{DD} and V_{GND}. In chapter 3, a more detailed explanation is given and explained why both these swings are needed to prevent charge imbalance. Again, the output-short switch is open during both phases of the LO signal. If the power is reduced even further to -12 dB, the operation is the same as in the 6 dB PBO mode during the first phase of the LO signal. The positive side capacitor switches to $2V_{DD}$ or V_{DD} and the negative side capacitor switches to V_{DD} or V_{GND} respectively. However, during the second phase of the LO signal, the output-short switch closes,

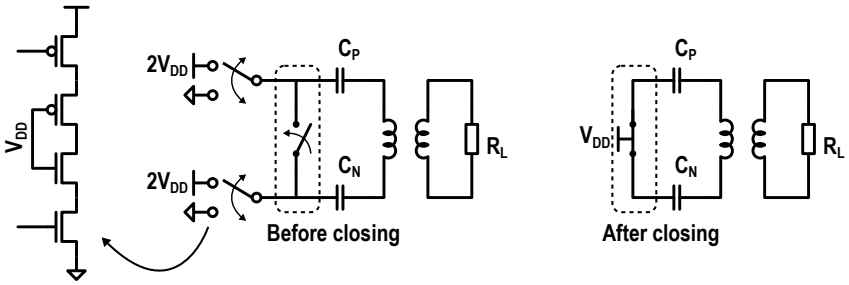


Figure 2.5: A class-G single supply SCPA where maximum output power operation is achieved by switching between two different voltage potentials $2V_{DD}$ and V_{GND}. The 6 dB PBO is achieved by only switching during the first phase of the LO and shorting the bottom plates of the capacitor during the second phase of the LO. This node then settles to V_{DD} creating the half supply swing from a single supply voltage. The capacitors can be implemented as a capacitor array with capacitors C_0 to C_N.

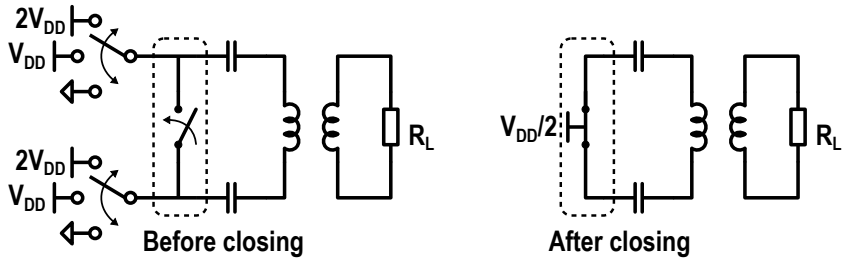


Figure 2.6: The proposed combined class-G single supply HOC SCPA with deep PBO enhancement technique. Achieving 6 dB PBO and 12 dB PBO efficiency peaking by creating voltage swing of $2V_{DD}$, V_{DD} and $\frac{1}{2}V_{DD}$ from a single supply.

shorting the positive and negative capacitor together. The voltage settles to $3/2V_{DD}$ or $1/2V_{DD}$. The last mode is where the PA-cell is off and contributing no power. The array capacitor is shorted to ground through the HoC structure.

3

Core HOC PA cell design

In chapter 2, the concept for the main PA cells was presented. In this chapter, the implementation will be discussed.
In section 3.1, an overview of the implementation will be given as well as the naming convention that will be used in the coming sections.
In section 3.2, the implementation of the HoC PA cell is discussed in detail for the four operating modes. However, from concept to implementation a problem arises, preventing the HoC structure from generating the inherent half supply through switching. Charge sharing with multiple PA cells will be introduced in section 3.3 to keep the generated half supply voltage stable.
In section 3.4, the ideal switches will be replaced by real transistor implementation. As described in section 2.3, the HOC has to be configured in a certain way for each PBO mode. section 3.5 will describe how the PBO signals generated from the AM-code will be decoded to configure the gate drivers which drives the actual inverter stages in the HOC structure. In section 3.6, the transistor implementation of the output-short switch is given.
Finally, the design trade-offs that were made with respect to the performance of the HoC structure are given in section 3.7.

3.1. HOC Implementation & Structure Overview

As discussed in chapter 2, the objective is to extend the high-efficiency operation of the PA to even further PBO. This should be done without adding more complexity to the external power circuitry. A proposal was made to combine two already proven designs to take advantage of both efficiency enhancement techniques; the House-of-Cards and single-supply class-G SCPA [14][13]. Figure 3.1 shows the implementation of the concept for a single PA cell.

From Figure 3.1, three functional circuit blocks can be distinguished. The first block is the HoC structure which from now on will go by the name HoC-cell. Furthermore, as the actual implementation is differential, the positive HoC-cell will be

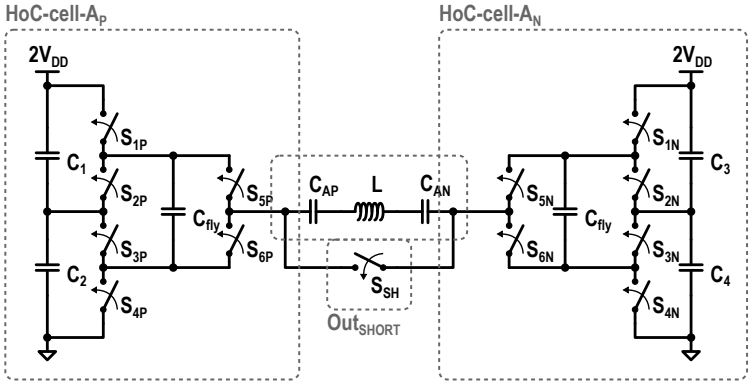


Figure 3.1: The proposed circuit concept of single HoC cell, combining the single supply HoC SCPA technique and the class-G single supply SCPA technique.

referred to as *HoC-cell-A_p*. In the same way, the negative side will be referred to as *HoC-cell-A_n*. The use of *'A'* will become more apparent in section 3.3. The second block is the switch that shorts the output of the *HoC-cell-A_p* and *HoC-cell-A_n*. The last block is the output balun in combination with the output capacitors, which forms the band-pass-filter.

3.2. HOC PBO modes operating principle

3.2.1. 0dB PBO (full-power mode)

For full output power, the left plate of capacitor C_{AP} should be switching between $2V_{DD}$ and V_{GND}. At the same time, the right plate of capacitor C_{AN} should also be switching between $2V_{DD}$ and V_{GND}, however, with a phase difference of 180°. Assuming that the inductor (L) and the capacitors (C_{AP}, C_{AN}) resonate at the LO frequency, a sinusoidal current will flow through the inductor. During the first phase of the LO (ϕ_1) the node V_{op} should be pulled to the supply voltage $2V_{DD}$, and the node V_{on} should be pulled to V_{GND}. This will result in a positive current flow through the inductor. To connect V_{op} to the supply voltage, it is clear that the switches S_{1p} and S_{5p} of HoC-cell-A$_p$ should be closed. In the same way, for V_{on}, closing the switches S_{6n} and S_{4n} of HoC-cell-A$_n$ connects this node to V_{GND}. A complete current path is established from the supply through switches S_{1p} and S_{5p}, the output capacitor C_{AP}, the inductor of the balun, the capacitor C_{AN}, the switches S_{6n} and S_{4n} and finally, to ground, as shown in Figure 3.2.

In the second phase of the LO (ϕ_2), the current flow through the inductor should be negative. To achieve this, node V_{on} should now connect to the supply and node V_{op} to ground. This is done by closing switches S_{1n} and S_{5n} for HoC-cell-A$_n$ and closing switches S_{6p} and S_{4p} for HoC-cell-A$_p$. The resulting current flow is shown in Figure 3.3.

Figure 3.4 shows the voltages of the output node V_{op} and V_{on} versus time. Both

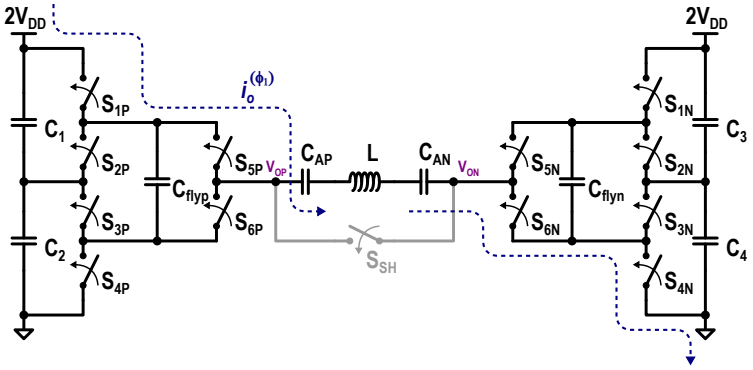


Figure 3.2: The current flow in a single PA cell for the first half period of the LO when operating in the 0dB PBO mode.

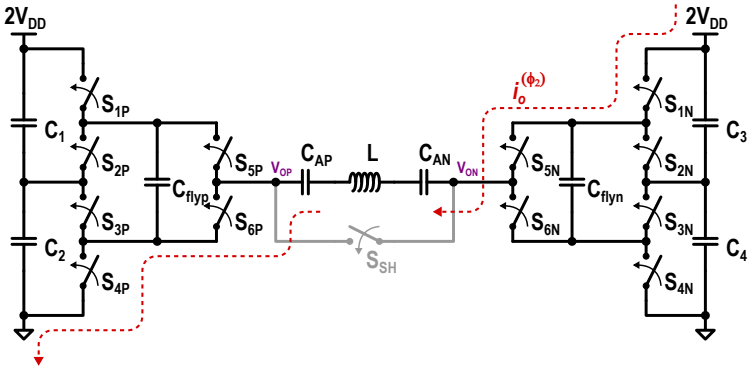


Figure 3.3: The current flow in a single PA cell for the second half period of the LO when operating in the 0dB PBO mode.

the voltages have a swing of $2V_{DD}$ and are opposite in phase due to their push-pull operation.

During the switching process, care has to be taken not to exceed the breakdown voltages of the switches S_5 and S_6. For this reason, when V_{op} is connected to the supply by means of closing the switches S_{1p} and S_{5p}, switch S_{3p} is also closed. This will enforce the mid-rail 'supply' (V_{int}) voltage to the source of S_{6p}. Ensuring that over the switches S_5 and S_6 not more than V_{DD} is applied. The capacitor C_{fly} helps to store this voltage (V_{DD}) also during the transition period.

3.2.2. 6dB PBO mode (half-power mode)

In the 6 dB PBO operation, the output power should be reduced to a quarter of the output power in the full power or 0 dB PBO operation. This requires the output

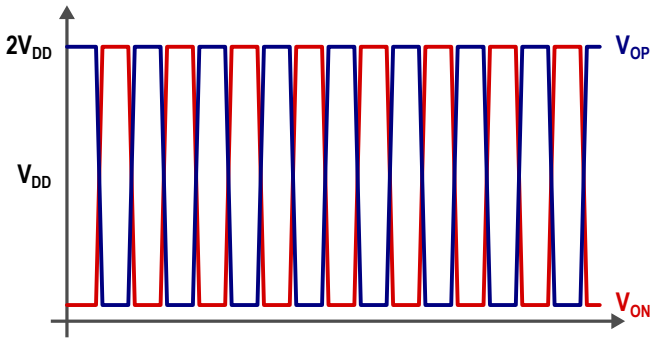


Figure 3.4: A conceptual drawing of the voltage waveforms for the output signals Vop and Von for a single PA cell operating in the 0dB PBO mode.

voltage swing at V_{op} and V_{on} to be half the voltage swing of its full power operation. The HoC-PA-cell is powered by an external supply that provides a voltage of $2V_{DD}$. However, the HoC structure can generate a half supply of V_{DD} as it behaves as a switched-capacitor DC-DC converter. This means that the voltage swing of V_{DD} can be created in two ways. Either by switching both the output nodes V_{op} and V_{on} between $2V_{DD}$ and V_{DD} (*High Voltage domain*) or between V_{DD} and ground (*Low Voltage domain*).

The HoC-cell-A_p can be configured in the HV-domain by keeping the the switches S_{1p} and S_{3p} in the closed position in both phases of the LO such that the top plate of C_{fly_p} is connected to $2V_{DD}$ and the bottom plate to V_{DD}. The same can be done for HoC-cell-A_n. Keeping the switches S_{1n} and S_{3n} closed in both ϕ_1 and ϕ_2 the top plate of C_{fly_n} has a potential of $2V_{DD}$ and the bottom plate a potential of V_{DD}. The V_{DD} voltage swing for V_{op} can easily be satisfied by alternately closing switch S_{5p} and S_{6p} in ϕ_1 and ϕ_2, respectively. This same principle holds for V_{on} where closing switch S_{6n} and S_{5n} in ϕ_1 and ϕ_2 respectively establishes the required voltage swing with a 180° phase difference compared to V_{op}. The resulting current flow in both ϕ_1 and ϕ_2 are shown in Figure 3.5.

Figure 3.6 clearly shows the HV-domain operation. In both phases of the LO the voltage at either V_{op} or V_{on} only switches between $2V_{DD}$ and V_{DD}.

The V_{DD} voltage swing required for -6 dB output power can also be achieved by putting the HoC-cell-A_p and HoC-cell-A_n in the LV-domain. To configure the HoC-cells in this LV-domain the switches S_{2x} and S_{4x} should be kept in a closed position in both ϕ_1 and ϕ_2, where x can be either p or n. This arrangement facilitates V_{DD} or V_{GND} connection to V_{ox}. By closing switch S_{5x}, V_{ox} will be connected to V_{DD} and closing switch S_{6x} will connect V_{ox} to V_{GND}. By closing the switches S_{5x} and S_{6x} in the right sequence, the same current flow through the output balun can be generated, Figure 3.7.

Figure 3.8 clearly shows the LV-domain operation. In both phases of the LO the voltage at V_{op} and V_{on} only switches between V_{DD} and V_{GND}.

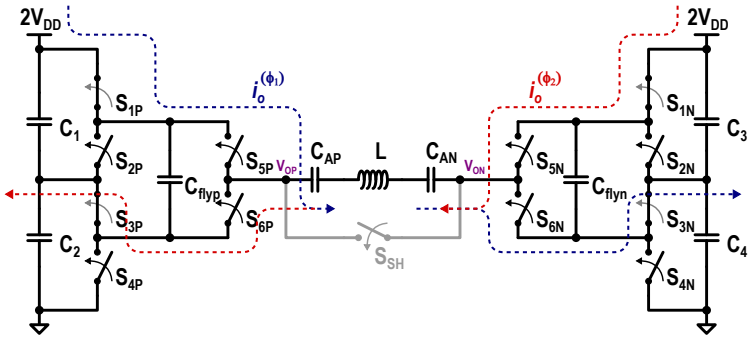


Figure 3.5: The current flow in a single PA cell operating in the 6dB PBO mode and HV-domain, for the first half period of the LO (blue) and the second half period of the LO (red).

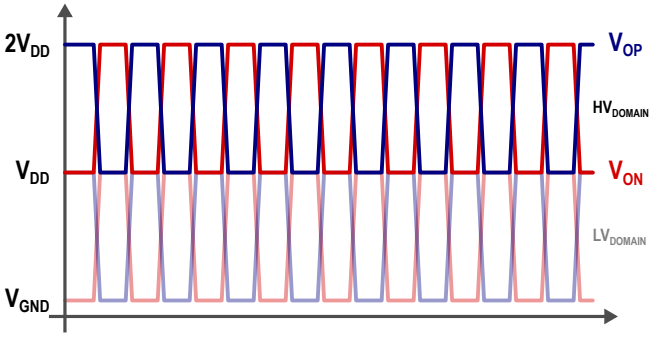


Figure 3.6: A conceptual drawing of the voltage waveforms for the output signals Vop and Von for a single PA cell operating in the 6dB PBO mode in the HV-domain.

Configuring the HoC-cell-A_p and HoC-cell-A_n in either the HV-domain or the LV-domain disrupts the switched capacitor DC-DC conversion operation, which is needed to stabilize the half supply voltage. In section 3.3, a solution will be proposed such that the HoC-cell-A_p and HoC-cell-A_n can still be configured in the HV or LV-domain, which will be called *static-mode* operation from now on.

3.2.3. 12dB PBO mode (quarter-power mode)

For the third efficiency peak at the 12 dB PBO point, again, the output voltage swing at V_{op} and V_{on} needs to be halved with respect to 6 dB PBO. The only supply voltages that are available are $2V_{DD}$ coming from the main external supply and the inherently generated V_{DD} supply. However in order to create the $1/2V_{DD}$ output voltage swing the principle as in the 6 dB PBO operation can not be applied. The second efficiency enhancement technique, as explained in chapter 2, will be used

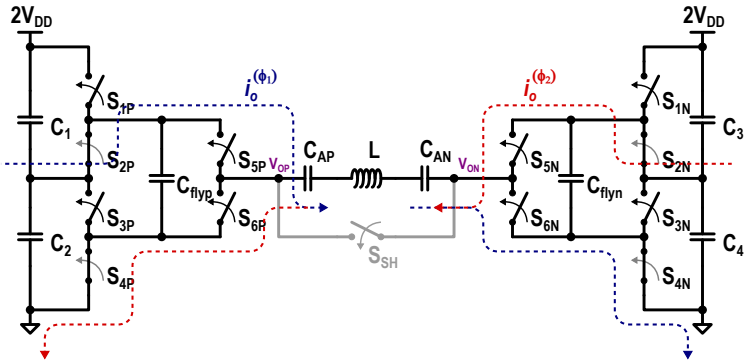


Figure 3.7: The current flow in a single PA cell operating in the 6dB PBO mode and LV-domain, for the first half period of the LO (blue) and the second half period of the LO (red).

to generate the required $^1/_2V_{DD}$ voltage swing.

In the same way as the 6 dB PBO operation the HoC-cell will be configured in the static-mode. This is done by keeping the switches S_{1x} and S_{3x} in the closed position for the HV-domain and switches S_{2x} and S_{4x} for the LV-domain. In ϕ_1 V_{op} is pulled to $2V_{DD}$ by closing switch S_{5p} while at the same time V_{on} is connected to V_{DD} by closing switch S_{6n}. This results in the same current flow as in the first phase of the LO in the 6 dB PBO operation mode, Figure 3.5. In the case of the LV-domain the same switches (S_{5p} and S_{6n}) connects V_{op} to V_{DD} and V_{on} to V_{GND} with the same current flow as in the 6 dB PBO operattion mode, Figure 3.7.

During the second phase of the LO the switches S_{5p}, S_{6p}, S_{5n} and S_{6n} are opened to disconnect the output capacitors C_{op} and C_{on} from the HoC-cell-A_p and HoC-cell-A_n respectively. At the same time, the output-short switch S_{sh} is closed shorting V_{op} and V_{on} together. This will cause V_{op} and V_{on} to settle to the same voltage potential. The final value is the average of the final voltage the nodes V_{op} and V_{on} had right before being shorted. In the case the PA-cell operates in the HV-domain this would be $^3/_2V_{DD}$. When operated in the LV-domain the settling voltage would be $^1/_2V_{DD}$. In both the HV and LV-domains, the resulting voltage swing of V_{op} and V_{on} is equal to $^1/_2V_{DD}$ as shown in Figure 3.9.

Not only does shorting the nodes V_{op} and V_{on} create the necessary voltage swing, it also creates a current path during this second phase of the LO. This current path is needed to keep the resonating RF current that is formed in the output filter network consisting of the output capacitors and the balun. The current path during the second phase of the LO in shown in Figure 3.10.

3.2.4. Off-state

It comes to no surprise that in the off-state, there should be no voltage swing at V_{op} and V_{on}. Leaving V_{ox} floating by opening both switches S_{5x} and S_{6x} is not an option even though no output voltage will be generated. This is due to the fact that

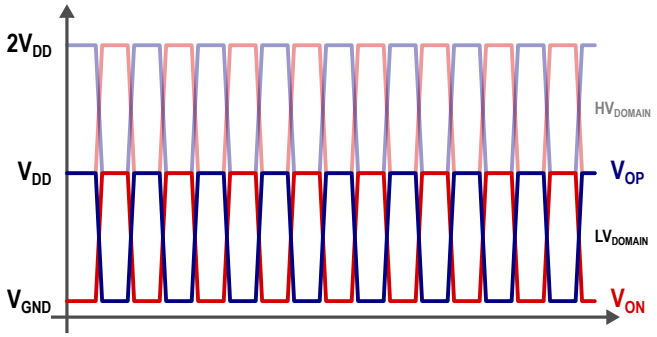


Figure 3.8: A conceptual drawing of the voltage waveforms for the output signals Vop and Von for a single PA cell operating in the 6dB PBO mode in the LV-domain.

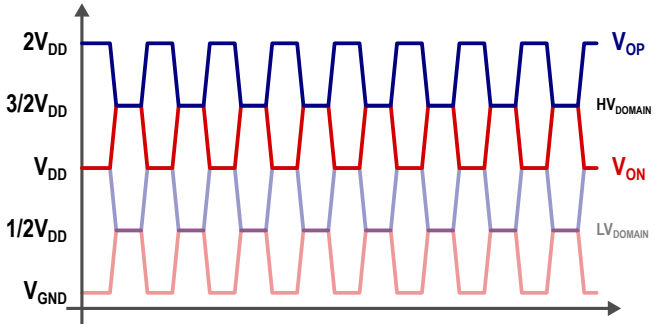


Figure 3.9: A conceptual drawing of the voltage waveforms for the output signals Vop and Von for a single PA cell operating in the 12dB PBO mode in the HV-domain (and LV-domain).

the same capacitance needs to be presented/connected to the primary of the balun as the total capacitance connected to the balun defines the resonance frequency of the output filter. Therefore, in the off-state the V_{ox} node needs to be connected to a steady DC voltage. This gives two options, the $2V_{DD}$ supply or V_{GND}. V_{GND} is the most stable node and therefore more desirable. To tie V_{ox} to V_{GND} the HoC-cell is configured in the static-mode, and both switches S_{4x} and S_{6x} are closed in both ϕ_1 and ϕ_2.

3.3. HoC current sharing and current re-use

When the HoC-cell is operating in the static-mode, charge sharing between C_{fly} and the two C_{int} capacitors stops. This charge sharing is required to stabilize the half supply node V_{int} which should automatically balance to half the supply voltage.

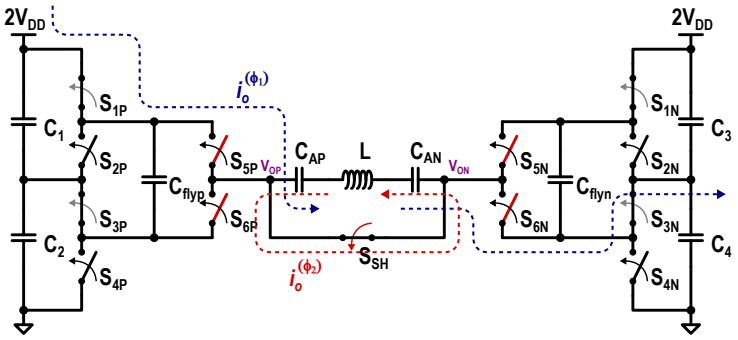


Figure 3.10: The current flow in a single PA cell operating in the 12dB PBO mode and HV-domain for the first half period of the LO (blue) and the second half period of the LO (red).

In the 6 dB PBO mode, the HoC-cell is configured in the static-mode and can be either put in the HV-domain or the LV-domain. Being configured in the HV-domain the total output current i_o will be drawn from the main supply ($2V_{DD}$) and flow through the output balun and enter HoC-cell-A_n, Figure 3.5. However, instead of directing the current i_o to ground, it flows into the half supply node to create the V_{DD} output voltage swing in 6 dB PBO mode. This half supply node is, however, not able to continuously source or sink current as it is effectively a capacitor with limited capacity.

Configuring the HoC-cell in the LV-domain would result in the same problem. Instead of sourcing the output current i_o from the main supply ($2V_{DD}$), it would have to be supplied from the half supply node V_{int} (V_{DD}). This node has a limited capacitance and can store only a limited amount of energy. Configuring the HoC-cell in the static-mode LV-domain would completely drain the energy in this node. As a result the half supply (V_{DD}) would collapse and output power will drop. The static-mode would prevent the half-supply node from being resupplied of energy, which in the normal operation would occur due to the switching behavior of the flying capacitor.

By placing a second HoC-PA-cell (consisting of a HoC-cell-B_p and HoC-cell-B_n) in parallel with HoC-cell-A_n and HoC-cell-A_p and connecting their half supply nodes together, it is possible to re-ues the current that is sinked into the half supply node of HoC-cell-A_n.
The HoC-cell-A_n if configured in the HV-domain would be sinking the output current i_o. The new HoC-cell-B_p configured in the LV-domain would be sourcing the same output current i_o, Figure 3.11. Connecting two HoC-PA-cells in parallel operating in different voltage domains is only possible by the DC blocking effect of the output capacitors that form the output filter with the balun. This DC blocking function makes it possible to generate two voltage swings at a different common-mode voltage.

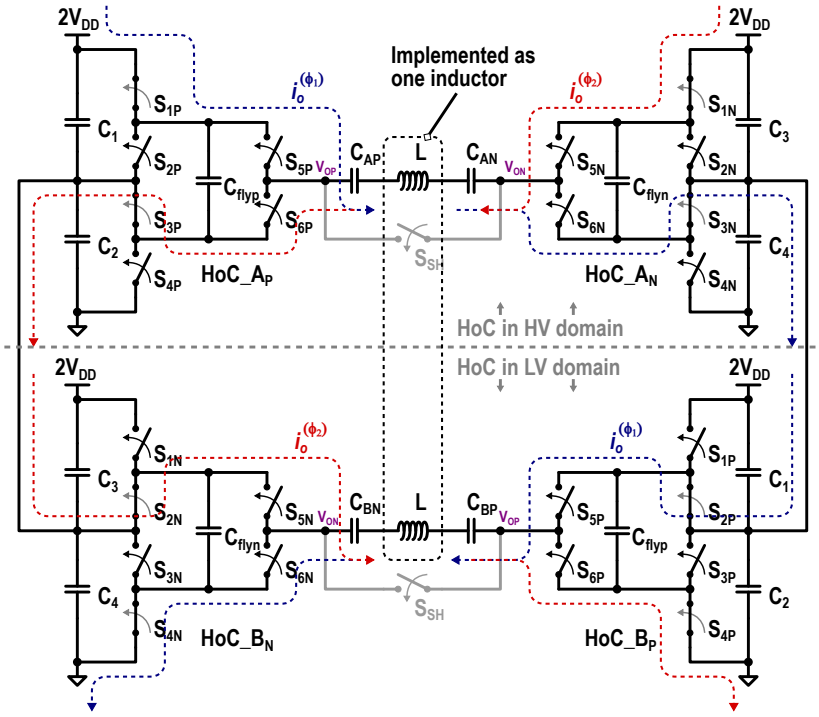


Figure 3.11: Current flow and charge sharing behavior for two HoC cells operating in the static-mode for the first half period of the LO (blue) and the second half period of the LO (red). The top HoC cell is configured in the HV-domain and the bottom HoC cell configured in the LV-domain.

3.4. Transistor Implementation HoC

To achieve the efficiency peaking at 0 dB, 6 dB, and 12 dB, the HoC-PA-cell operates differently in each of these modes. This requires different voltages on the gates of the transistors in the HoC-cell. Not only with respect to the transistors them self but also between the different operating modes. In one mode, the transistors should be switching at the LO frequency, while in the other, they should be static. The two voltage domains add another complexity as, at some point, a conversion must be done to level-shift the input signals for the HoC-cell to the higher voltage domain. This section will discuss what voltages need to be applied when and where. But also how this is done.

In the previous sections of this chapter, the switches in the HoC-cells were considered ideal switches. In the actual implementation, however, they have to be replaced with transistors. In Figure 3.12, this implementation with transistors is given. Furthermore, the naming convention for the gates of the transistors is presented.

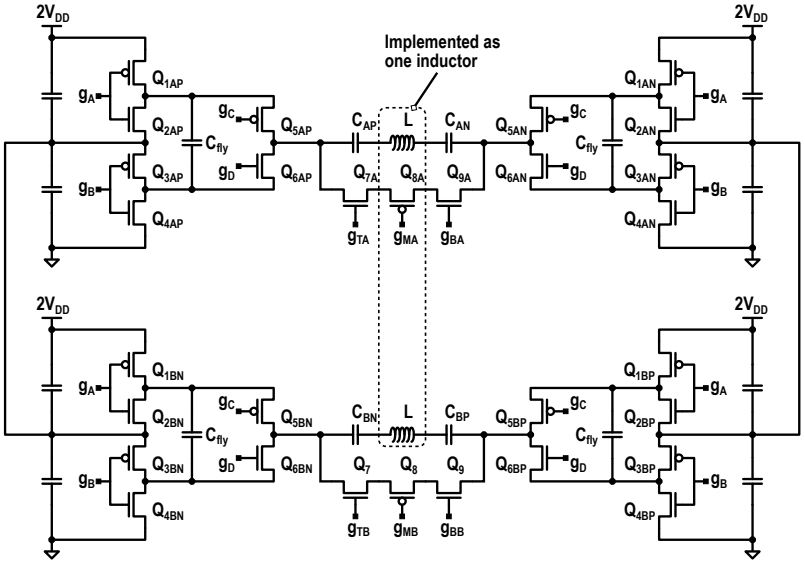


Figure 3.12: The proposed transistor circuit implementation of a single PA cell, combining the single supply HoC SCPA and the class-G single supply SCPA.

The HoC-cell has four distinct gates; g_A, g_B, g_C and g_D. g_A is the input for the first stage inverter in the HV-domain, which is made of Q_1 and Q_2. In the same way g_B is the input for the second first-stage inverter in the LV-domain, consisting of the transistors Q_3 and Q_4. The second stage inverter consisting of Q_5 and Q_6 has individually driven gates; g_C and g_D.

In section 3.2, the operation principle of the four states of the HoC structure is explained, such as which switch should close or open and when. However, practically driving the corresponding transistor switch implementation is not that trivial. In the HoC-PA-cell, there are four HoC-cells; HoC-cell-A_p, HoC-cell-A_n, HoC-cell-B_p, and HoC-cell-B_n. The transistors in these four HoC-cells have to be driven differently to steer the current through the HoC-cell correctly, as explained in section 3.2.

For every HoC-cell, the gate voltage will be presented for each operating mode in Table 3.1, Table 3.2, Table 3.3, and Table 3.4 for the HoC-cells A_p, A_n, B_p and B_n respectively.

3.4.1. HoC-cell-Ap

In the full power mode, V_{op} should be switching between $2V_{DD}$ to V_{GND}. As explained in section 3.2, this means that during the first phase of the LO, the transistors Q_1 and Q_5 should be conducting. Also, transistor Q_3 should be conducting to force a V_{DS} voltage of V_{DD} on the transistors Q_5 and Q_6 to keep them in their safe operating

voltage. To turn transistor Q_1 on a voltage of V_{DD} needs to be applied to g_A. To turn transistor Q_3 on, gate g_B needs to be tied to V_{GND}. As Q_1 and Q_3 are conducting it puts the second stage inverter (Q_5 and Q_6) momentarily in the HV-domain during this first phase of the LO signal. Therefore to turn transistor Q_5 on its gate (g_C) needs to be pulled to V_{DD}. In this regard, Q_6 needs to be off which is done by applying the same voltage of V_{DD} to its gate (g_D). During the second phase of the LO V_{op} should be tied to V_{GND}. This is done by closing transistors Q_4 and Q_6. To turn on Q_4, its gate and therefore the gate of Q_3, should be pulled to V_{DD}. Just as in ϕ_1, the voltage across the transistors Q_5 and Q_6 should not exceed the design voltage of V_{DD}. Applying a voltage of $2V_{DD}$ to g_A turns off Q_1 and turns on Q_2. This, in turn, connects the top plate of C_{fly} to V_{DD} and the voltage condition for Q_5 and Q_6 is satisfied. To turn Q_5 off and turn Q_6 on, g_C and g_D should both be pulled to V_{DD}.

In the 6 dB PBO operating mode, the HoC-cell-A_p is configured in the HV-domain. This effectively means that the second stage inverter consisting of Q_5 and Q_6 should have a top supply of $2V_{DD}$ and a bottom supply of V_{DD} for both phases of the LO. This is done by turning on Q_1 and Q_3 and turning off Q_2 and Q_4. Having g_A and g_B at a fixed voltage of V_{DD} and V_{GND}, respectively during both phases of the LO establishes this and configures HoC-cell-A_p in the HV-domain. Switching V_{op} between $2V_{DD}$ and V_{DD} is simply done by alternatey turning on and off transistors Q_5 and Q_6. To be exact, a positive swing should be applied during ϕ_1 and therefore Q_5 should turn on and Q_6 off. As a result g_C and g_D have a potential of V_{DD} in ϕ_1 and a potential of $2V_{DD}$ during ϕ_2.

At 12 dB PBO, the HoC-cell-A_p is also configured in the HV-domain. The gates of $Q_1 - Q_4$ have the same potential as in the 6 dB PBO operating mode. This is also true for the gates g_C and g_D during ϕ_1. The difference comes, however, in ϕ_2 as the HoC-cell-A_p should be disconnected from the output filter network by turning off both transistors Q_5 and Q_6. This is done by pulling the gate of Q_5 to $2V_{DD}$ and the gate of Q_6 to V_{DD}.

A summary of the voltages that are applied to the gates $g_A - g_D$ is given in Table 3.1. In each cell, first, the voltage potential during ϕ_1 is applied and the second voltage potential is drived during ϕ_2. If only one potential is given it means that it is the same for both phases of the LO.

Table 3.1: The gate voltages for the HoC-Ap cell for both first (ϕ_1) and second (ϕ_2) half periods of the LO and all operating modes.

$\phi_1 - \phi_2$	gA	gB	gC	gD
0dB	V_{DD} - $2V_{DD}$	V_{GND} - V_{DD}	V_{DD}	V_{DD}
-6dB	V_{DD}	V_{GND}	V_{DD} - $2V_{DD}$	V_{DD} - $2V_{DD}$
-12dB	V_{DD}	V_{GND}	V_{DD} - $2V_{DD}$	V_{DD}
OFF				

3.4.2. Hoc-cell-An

As the name suggests, the HoC-cell-A_n is the complementary cell of the HoC-cell-A_p. In full power mode (0 dB), the voltage swing should be the same as the HoC-cell-A_p. The only difference is the phase which is 180° of that of the HoC-cell-A_p. When g_A of HoC-cell-A_p is $2V_{DD}$, g_A of HoC-cell-A_n should be V_{DD}. The same holds for g_B. As both g_C and g_D have a potential of V_{DD} for both phases of the LO there is no difference between HoC-cell-A_p and HoC-cell-A_n.

In the 6 dB PBO operating mode, the HoC-cell-A_n is similar to the HoC-cell-A_p configured in the HV-domain. Therefore, g_A and g_B are the same as for the HoC-cell-A_p. The 180° phase difference between HoC-cell-A_p and HoC-cell-A_n also holds in the 6 dB PBO operating mode, and therefore the gates g_C and g_D are operating at this phase difference.

For the 12 dB PBO operating mode, the HoC-cell-A_n is again configured in the HV-domain, which is also true for the HoC-cell-A_p. There is, however, a difference for the second inverter stage. In the first phase of the LO V_{op} is connected to $2V_{DD}$ by the HoC-cell-A_p. In order to create the correct voltage swing as discussed in subsection 3.2.3, V_{on} should be connected to V_{DD}. This is done by turning off Q_5 and turning on Q_6 by applying a gate voltage of $2V_{DD}$ to both gates g_C and g_D. In the second phase of the LO, the HoC-cell-A_n should be disconnected from the output filter network by turning off transistor Q_6 and applying a gate voltage of V_{DD} to its gate.

The complete overview summary of the gate voltages for the oC-cell-A_n is given in Table 3.2.

Table 3.2: The gate voltages for the HoC-An cell for both first (ϕ_1) and second (ϕ_2) half periods of the LO and all operating modes.

$\phi_1 - \phi_2$	gA	gB	gC	gD
0dB	$2V_{DD}$ - V_{DD}	V_{DD} - V_{GND}	V_{DD}	V_{DD}
6dB	V_{DD}	V_{GND}	$2V_{DD}$ - V_{DD}	$2V_{DD}$ - V_{DD}
12dB	V_{DD}	V_{GND}	$2V_{DD}$	$2V_{DD}$ - V_{DD}
OFF				

3.4.3. HoC-cell-Bp and HoC-cell-Bn

In the full power mode, the HoC-cell-B_p behaves identically to the HoC-cell-A_p. In the 6 dB PBO operating mode, however, the HoC-cell-B_p is configurate in the LV-domain. As mentioned in section 3.3 the current that was used by the HoC-cell-A_p and HoC-cell-A_n will be re-used by the HoC-cell-B_p and HoC-cell-B_n. Therefore the required swing of V_{DD} for V_{op} is created by switching between V_{DD} and V_{GND} and alternately turning on and off Q_5 and Q_6. In the 12 dB PBO mode, the HoC-cell-B_p is still configured in the LV-domain. The principle of operation is the same as for HoC-cell-A_p. However, because of the LV-domain operation, the voltages on g_C and g_D are shifted down by V_{DD}.

Table 3.3 shows the similarity between the HoC-cell-A_p and HoC-cell-B_p.

Table 3.3: The gate voltages for the HoC-Bp cell for both first (ϕ_1) and second (ϕ_2) half periods of the LO and all operating modes.

$\phi_1 - \phi_2$	gA	gB	gC	gD
0dB	V_{DD} - $2V_{DD}$	V_{GND} - V_{DD}	V_{DD}	V_{DD}
-6dB	$2V_{DD}$	V_{DD}	V_{GND} - V_{DD}	V_{GND} - V_{DD}
-12dB	$2V_{DD}$	V_{DD}	V_{GND} - V_{DD}	V_{GND}
OFF				

It would come as no surprise that the operation of HoC-cell-B_n is almost the same as HoC-cell-A_n, where the only difference is the voltage domain in the 6 dB and 12 dB PBO operating mode.

Table 3.4 shows the similarity between the HoC-cell-A_n and HoC-cell-B_n.

Table 3.4: The gate voltages for the HoC-Bn cell for both first (ϕ_1) and second (ϕ_2) half periods of the LO and all operating modes.

$\phi_1 - \phi_2$	gA	gB	gC	gD
0dB	$2V_{DD}$ - V_{DD}	V_{DD} - V_{GND}	V_{DD}	V_{DD}
6dB	$2V_{DD}$	V_{DD}	V_{DD} - V_{GND}	V_{DD} - V_{GND}
12dB	$2V_{DD}$	V_{DD}	V_{DD}	V_{DD} - V_{GND}
OFF				

3.5. Decoding logic and gate drivers

The reason for this exercise, of finding the voltages required to drive the HoC-cells, is to find in which voltage domains the gates are being operated. The digital core of the full PA chip will be powered by V_{DD}, and therefore, level-shifters are needed. However, these required level-shifters can be reduced to a minimum if the level-shifting action can take place before the drive logic for the HoC-cell.

For each gate in the HoC-cell (g_A, g_B, g_C, and g_D) and for each HoC-cell (HoC-cell-A_p, HoC-cell-A_n, HoC-cell-B_p, and HoC-cell-B_n) the voltage domain can be determined by looking at the columns in Table 3.1, Table 3.2, Table 3.3, and Table 3.4. For g_A in the HoC-cell-A_p, it is clear that the only voltage potentials required in all the four operating modes is either V_{DD} or $2V_{DD}$. This means the drive logic for this gate and HoC-cell can be powered in the HV-domain. Doing this for all the gates of the HoC-cells gives an overview of the required domains for the driving logic as shown in Table 3.5.

From the tables in the previous section, an observation can be made that for the gates, there are three possible driving modes; switching-at-LO (EN_{LO}), static-high (EN_H), or static-low ($\overline{EN_L}$). The gate driver circuit should be able to drive the gates of the HoC-cells with these characteristics. The LO should be able to be passed through, but if needed, a static voltage of either V_{LOW} or V_{HIGH} should be applied to the gate, and thus, the LO signal should be blocked. Here V_{LOW} and V_{HIGH} depends on the voltage domain the gate driver operates. The gate driver is

Table 3.5: The required voltage domain for the HoC gate drivers for each HoC cell in a PA cell.

$\phi_1 - \phi_2$	gA	gB	gC	gD
HoC-cell-A_p	HV	LV	HV	HV
HoC-cell-A_n	HV	LV	HV	HV
HoC-cell-B_p	HV	LV	LV	LV
HoC-cell-B_n	HV	LV	LV	LV

shown in Figure 3.13. The first stage is an inverter with enable switches in both the top branch at the lower branch. Two enable switches are needed not to load the static-low or static-high switch. In the second stage of the gate driver there is a pull-up switch for the static-low and a pull-down switch for the static-high. Note that the last stage is the actual output driver implemented as an inverter, and therefore, inverts the pull-up and pull-down that are used for the static mode.

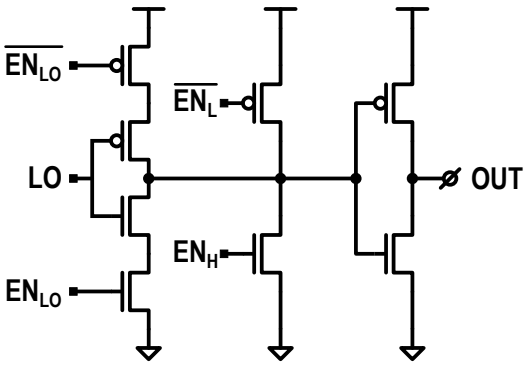


Figure 3.13: HoC Gate driver transistor implementation.

In each HoC-cell four gates need to be driven, hence, four gate lines are needed. Not only that, but there are also three control signals for each gate to put the HoC-cell in switching-at-LO, static-high, or static-low. These control lines depend on the operating modes that the HoC-cell can be configured in. To minimize the area needed for routing these control lines, the operating modes are encoded in two control lines; PBO_0 and PBO_1. These encoded signals are then local to the HoC-cells, decoded, and thereafter passed to the gate drivers to drive the four gates. The operating modes are reflected binary coded. Thus, if the signals P_0 and P_1 have the value representing 0, the HoC-cell should be configured in the full power mode. The complete coding is shown in Table 3.6 here below.

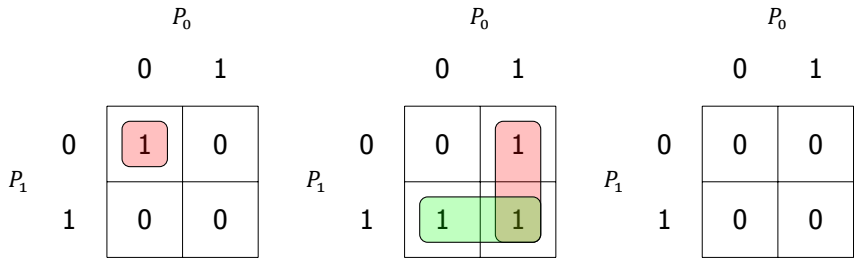
The design of the decoding logic is done with the use of Karnaugh maps. Consequently, for each gate in the HoC-cells, three Karnaugh maps can be defined for the switching-at-LO, static-high, or $\overline{EN_L}$ signals. Take, for instance g_A in HoC-cell-A_p,

Table 3.6: PA PBO modes encoding mapping on the two PBO mode signals. For example for 0db PBO mode the two signals P_0 and P_1 should both be zero.

P_0P_1	00	01	11	10
PBO mode	0dB	6dB	12dB	OFF

Table 3.1. In the full power mode, the gate g_A is switching at the LO frequency. In the first Karnaugh map in Table 3.7, a 1 should be put in the cell where both P_0 and P_1 are 0. In the other operating modes, the voltage applied to g_A is equal to V_{DD}. Remember, however, that g_A is the input of the first stage upper inverter in the HoC-cell-A_p and is always operating in the HV-domain. Therefore, V_{DD} is equal to a $\overline{EN_L}$ signal. For the second Karnaugh map, all the cells except the one where both P_0 and P_1 are 0 should be filled with a 1.

Table 3.7: Karnaugh map for g_A and g_B of the HoC-cell-A_p. On the left, the Karnaugh map for the LO. In the middle is the result for the static-low and on the right for the static-high.



From Table 3.7 the decoding logic can be generated. The result of the Karnaugh map for the EN_{LO} signal is given as

$$\begin{aligned} Y &= \overline{P_0} \circ \overline{P_1} \\ Y &= \overline{P_0 + P_1} \end{aligned} \tag{3.1}$$

The results of the Karnaugh maps are always converted to either a NOR-gate or a NAND-gate if possible as is also done for Equation 3.1. For the $\overline{EN_L}$ signal the result of the Karnaugh map is given as

$$\begin{aligned} \overline{Y} &= P_0 + P_1 \\ Y &= \overline{P_0 + P_1} \end{aligned} \tag{3.2}$$

The static-low is implemented by a pull-up in the gate driver circuit, and therefore, is active low, Figure 3.13. This is why the result is inverted and also, in this

case, equal to the EN_{LO} signal. Of course, the output signal from the decoding logic for the EN_{LO} signal can also be used for the $\overline{EN_L}$ signal as its result is the same. For g_A in the HoC-cell-A_p there is never a case where it is static-high as is easily checked in the corresponding Karnaugh map. The Karnaugh maps are independent of the voltage domain, and because the operation for g_B is effectively the same as for g_A, with the only difference the voltage domain the decoding logic is operating in, the same logic powered in the LV-domain can be used for g_B. The situation for g_C, however, is different. The Karnaugh maps are shown in Table 3.8.

Table 3.8: Karnaugh map for g_C of the HoC-cell-A_p. On the left, the Karnaugh map for the LO. In the middle is the result for the static-low and on the right for the static-high.

P_1 \ P_0	0	1
0	0	0
1	1	1

P_1 \ P_0	0	1
0	1	1
1	0	0

P_1 \ P_0	0	1
0	0	0
1	0	0

The result of the Karnaugh map for the EN_{LO} signal is given as

$$Y = P_1 \tag{3.3}$$

Because again the g_C will never be set to static-high and the $\overline{EN_L}$ is inverted, the same result can be used for $\overline{EN_L}$.

Finally the Karnaugh maps for g_D are defined, Table 3.9.

The result of the Karnaugh map for the EN_{LO} signal is given as

$$\begin{aligned} Y &= \overline{P_0} \circ P_1 \\ Y &= \overline{P_0 + \overline{P_1}} \end{aligned} \tag{3.4}$$

The result of the Karnaugh map for $\overline{EN_L}$ is given as

$$\begin{aligned} \overline{Y} &= P_0 + \overline{P_1} \\ Y &= \overline{P_0 + \overline{P_1}} \end{aligned} \tag{3.5}$$

In the actual layout design, there is almost an inevitable delay mismatch between the P_0 and P_1 signals. Therefore, the signals after the decoding are latched at the LO and buffered to drive the gate drivers. An example for g_A is shown in Figure 3.14.

Table 3.9: Karnaugh map for g_D of the HoC-cell-A_p. On the left, the Karnaugh map for the LO. In the middle is the result for the static-low and on the right for the static-high.

P_1 \ P_0	0	1
0	0	0
1	1	0

P_1 \ P_0	0	1
0	1	1
1	0	1

P_1 \ P_0	0	1
0	0	0
1	0	0

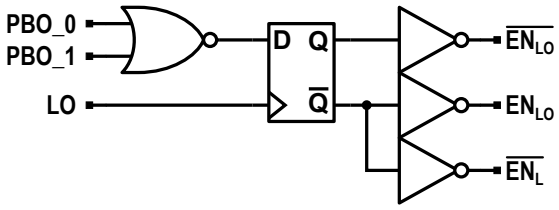


Figure 3.14: PBO mode signal decoding logic. Each HoC PA cell has these locally that convert the two-mode selection signals to the correct gate driving signals. Reducing top-level routing complexity.

The same principle holds for the HoC-cell-A_n, HoC-cell-B_p, and HoC-cell-B_n. However, the actual results will not be further discussed as it is a straightforward procedure. In the end, there are four HoC-cells with four gate drivers, which is controlled by the decoding logic, as shown in Figure 3.15.

3.6. Transistor implementation output short switch

The last block that needs to be discussed is the switch that shorts the output capacitors when operating in the 12 dB PBO mode. The function of this switch is straightforward. The implementation, however, isn't. In the 0 dB and 6 dB PBO operation mode, the short-switch should not conduct regardless of the voltage potential on both V_{op} and V_{on}. This means that the short-switch implementation should be able to handle not only a voltage of $2V_{DD}$ and V_{DD}, but also $-2V_{DD}$ and $-V_{DD}$. Here the polarity is referenced as V_{op} being the positive and V_{on} the negative node.

The short is implemented with a stack of three transistors to cope with the $2V_{DD}$ voltage drop in the 0 dB PBO operation. The stack consist, of either a, NMOS-PMOS-NMOS in the case for the LV-domain and a stack of PMOS-NMOS-PMOS in the HV-domain as shown in Figure 3.16.

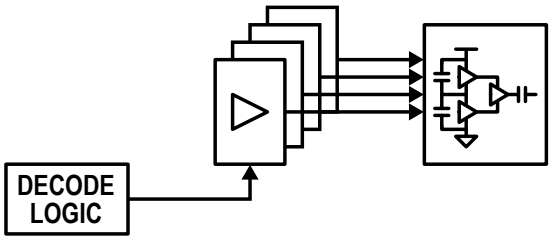


Figure 3.15: Each HoC PA cell has a decoding logic circuit and four gate drivers, one for each gate in the HoC structure.

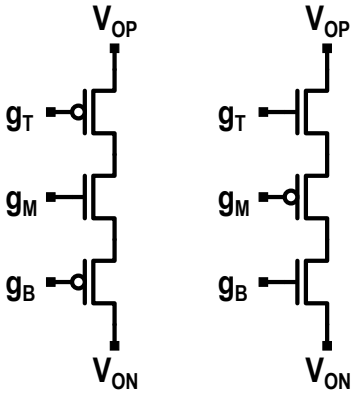
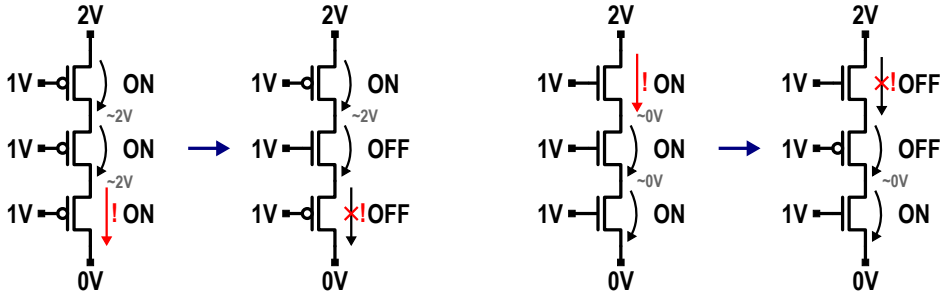


Figure 3.16: Transistor implementation of the 12dB PBO mode output short switches for HV-domain and LV-domain.

As discussed in section 3.3, the HoC-cell-A_p and HoC-cell-A_n operate in the HV-domain. In the 12 dB PBO operating mode, the output switches between $2V_{DD}$ and $3/2V_{DD}$ for V_{op} and between V_{DD} and $3/2V_{DD}$ for V_{on}. This means that the headroom available for the V_{GS} above the settling voltage is only $1/2V_{DD}$. The preferred devices for the short-switches are, therefore, PMOS as V_{GS} could be made equal to V_{DD} by setting it to $1/2V_{DD}$. The same principle holds for the short switch in the LV-domain where the settling potential is $1/2V_{DD}$. The voltage headroom for driving PMOS devices is only $1/2V_{DD}$ in contrast to the available V_{DD} for driving NMOS devices. The preferred devices in the LV-domain are, therefore, NMOS.

A problem arises when a stack of three transistors of either all PMOS or all NMOS is used. In the HV-domain, three PMOS transistors are preferred. In the -12 dB PBO mode, the gate voltage to turn the transistors on should be $1/2V_{DD}$. This $1/2V_{DD}$ lies in the LV-domain, and the gate drivers for the three transistors should thus be powered in the LV-domain to prevent the gates drivers from becoming unnecessarily complex. The only available voltages that can be used for driving the

gates lie between V_{DD} and V_{GND}. In the 0 dB and 6 dB PBO mode, the transistors should be turned off in both phases of the LO. The problem is already visible in the first phase of the LO in the 0 dB PBO mode, where the voltage across the three PMOS transistors is equal to $2V_{DD}$. With only V_{DD} to drive the gates, the transistors would never turn off, as shown in Figure 3.17(a). For this reason, the middle transistor is replaced with its complement. By driving the gate of the middle transistor, which is now NMOS with V_{DD}, the direct short is broken, as shown in Figure 3.17(a). Because the stack is symmetrical, the stack is also off in the second phase of the LO. The downside is, however, that the NMOS transistor only has a V_{GS} of $1/2V_{DD}$ when it is supposed to be turned on. To mitigate the performance drop, the size of the NMOS is increased as well, and implemented as an *elvt* device.



(a) PNP output-short switch needed to turn fully off in 0dB PBO mode.

(b) NPN output-short switch needed to turn fully off in 0dB PBO mode.

Figure 3.17: The output short switches turn off problem if all transistors in the switch would all be PPP or NNN.

In the LV-domain, where the three transistors are preferred to be NMOS devices, the same phenomenon occurs. In the -12 dB PBO mode, the gate voltage to turn the transistors on should be $3/2V_{DD}$ which lies in the HV-domain. Therefore the gate drivers for the three transistors should be powered in the HV-domain. Again the three transistors cannot turn off in the 0 dB PBO mode and 6 dB PBO mode, Figure 3.17(b). By replacing the middle NMOS transistor with its complement, the direct short can be prevented. Of course, the same drawback exists as with the PMOS-NMOS-PMOS stack in the HV-domain. Still, this solution comes with a drawback in the -12 dB PBO mode by the limited V_{GS} for the middle transistors. In the 0 dB and 6 dB PBO mode, it has the benefit that the gates of the three transistors can be kept at a constant voltage reducing the power needed to drive these gates.

3.7. HOC design and optimization

So far in this chapter, the implementation of the concept has been thoroughly discussed. In this section, the performance optimization of the HoC-cell will be discussed.

In the PA two factors determine overall efficiency. One is the conduction losses of the ON-resistance of the swithes (P_{rout}). The second key factor comes from the charging and discharging of the parasitic capacitance of these switches (P_{cap_sw}) every RF cycle, and the parasitics of the top and bottom plates of the output capacitor (P_{cap_cout}). The total PA loss is therefore given as:

$$P_{loss} = P_{rout} + P_{cap\_sw} + P_{cap\_cout} \tag{3.6}$$

In order to reduce the PA loss, one might increase the transistor sizes such to reduce the ON-resistance of these switches. However, because of the increase in size, the parasitic capacitance of these switches increases and in return increases the losses associated with the parasitic capacitance. By the inverse relationship of the losses between the ON-resistance loss and the parasitic loss of the power switches an optimal point is to be expected. Figure 3.18 shows the ON-resistance loss and the parasitic loss of the power switches over normalized switch size at 0 dB. The loss with small switch size is dominated by the loss due to the ON-resistance, whereas the for large switch size the parasitic loss becomes the dominant factor. The optimal point of the sum of the ON-resistance and parasitic loss is achieved with a normalized switch size of 0.7.

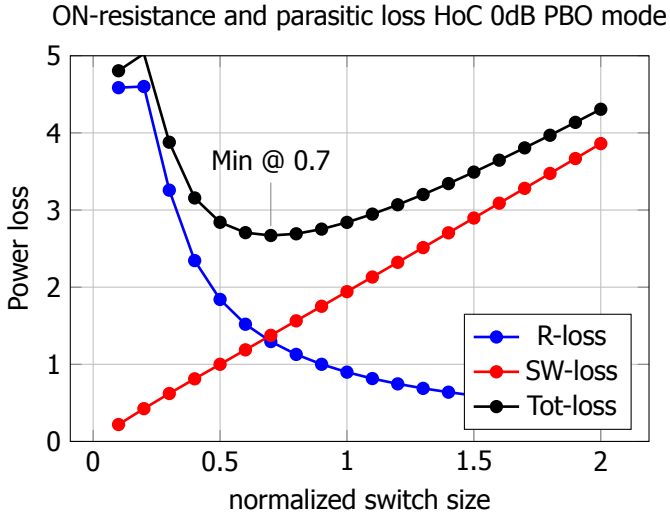


Figure 3.18: Switch optimization for HoC cell in the 0dB PBO mode. Showing ON-resistance losses in (blue) and switching losses in (red). Clearly an optimum can be achieved in the 0dB PBO mode.

In the -6 dB PBO operation, the voltage swing at the output of the HoC-cell is reduced, which in turn, also reduces the current through the switches. This, of course, also reduces the loss that is associated with the ON-resistance of the switches. What, however, is not obvious is how the reduced loss due to the ON-resistance relates to the reduced loss due to the parasitics. As the voltage swing

reduces, the energy needed to charge and discharge the parasitic capacitances reduces. Inside the HoC-cell, the voltage swings are the same as in the 0 dB PBO operation since the inverter stages are kept in the V_{DD} voltage domain. This would mean the same loss due to the parasitics as in the 0 dB PBO operation. However, in the -6 dB PBO operation, the HoC-cell is configured in the static-mode, where the first stage inverters are not switching. This reduces the loss associated with the switches in the inverters that is caused by the parasitic capacitance. Figure 3.19 shows the ON-resistance loss and the parasitic loss of the power switches over normalized switch size in the -6 dB PBO operation. In the 0 dB PBO operation, the optimal normalized switch size is equal to 0.7, while in the -6 dB PBO operation, it reduces slightly to a normalized size of 0.5. The loss with a switch size of 0.7 is negligibly increased.

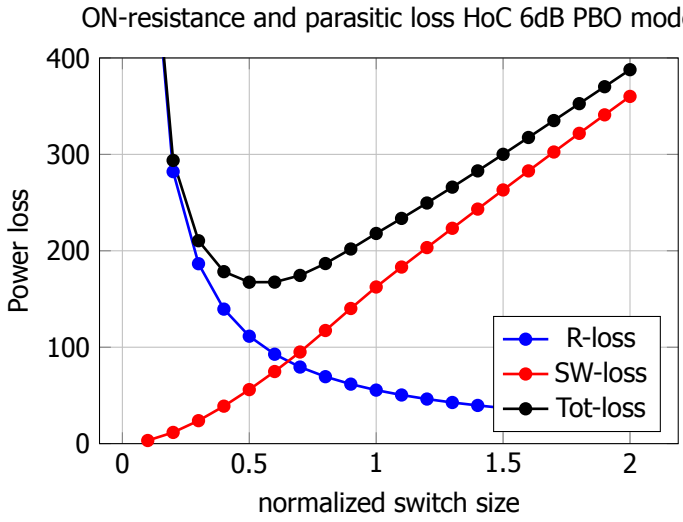


Figure 3.19: Switch optimization for HoC cell in the 6dB PBO mode. Showing ON-resistance losses in (blue) and switching losses in (red). Clearly an optimum can be achieved in the 6dB PBO mode. This optimum is achieved with different transistor sizing compared to the 0dB PBO mode.

In the -12 dB PBO operation, the voltage swing is further reduced, and therefore, also the current through the switches in the HoC-cell. In this mode, the HoC-cell is again configured in the static-mode, reducing the parasitic losses. However, in the second phase of the LO, the switches that short the output of the HoC-cell-A_x and HoC-cell-B_x are turned off. This increases the losses due to the charging and discharging of the parasitics associated with the switches in the output short. In Figure 3.20, the increase in parasitic loss is visible as it becomes dominant for smaller normalized switch sizes, with the optimal for normalized switch size of 0.3.

The different optimal switch size in the -12 dB PBO operation mode compared to the other PBO operation modes necessitate to either deliver up efficiency in the high output power region in order to increase the efficiency at low output power,

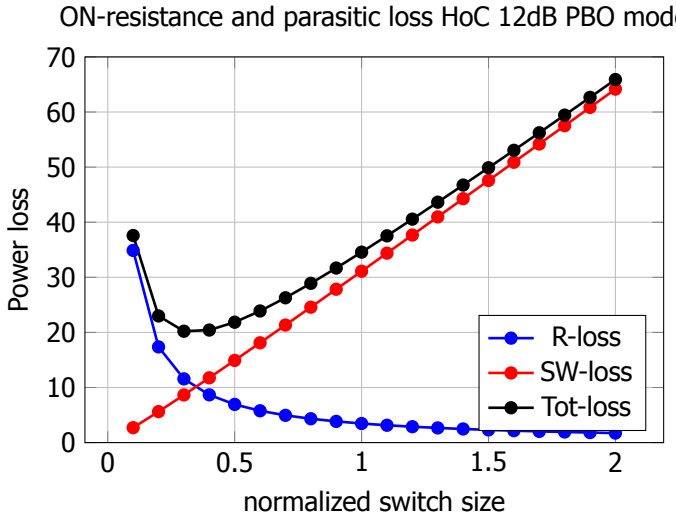


Figure 3.20: Switch optimization for HoC cell in the 12dB PBO mode. Showing ON-resistance losses in (blue) and switching losses in (red). Clearly an optimum can be achieved in the 12dB PBO mode. This optimum is achieved with different transistor sizing compared to the 0dB and 6dB PBO mode.

or the opposite where the efficiency for high output power can be increased at the expense of efficiency for low output powers.

In Figure 3.18, Figure 3.19, and Figure 3.20 the size of all switches inside the HoC-cell was changed simultaneously. This, however, is not necessarily the best method of sizing the transistors in the HoC-cell. Take, for instance, the 0 dB PBO operation mode, where the majority of the current flows through the 'outer' transistors Q_1, Q_5, Q_6 and Q_4 as defined in Figure 3.12. The transistors Q_2 and Q_3 are mainly used for charge distribution between the capacitors C_{int} and C_{fly}. Therefore, a higher ON-resistance can be tolerated for these transistors by reducing their sizes and consequently reducing the parasitic capacitances. This increases the efficiency in the 0 dB PBO operation mode, as shown in Figure 3.21. Figure 3.21 also shows that in the 6 dB and 12 dB PBO operation mode, the efficiency increases with increasing sizes for the transistors Q_2 and Q_3. In these PBO modes, the current is either sinked or sourced from the half supply voltage V_{DD}. Meaning that now the majority of the current, albeit not as large as in the 0 dB PBO mode, is flowing through the transistors Q_2 and Q_3. The ON-resistance becomes more dominant compared to the 0 dB PBO operating mode. For the transistors Q_2 and Q_3 a trade-off must be made between high efficiency at high output power at the cost of efficiency at lower output power or vice versa.

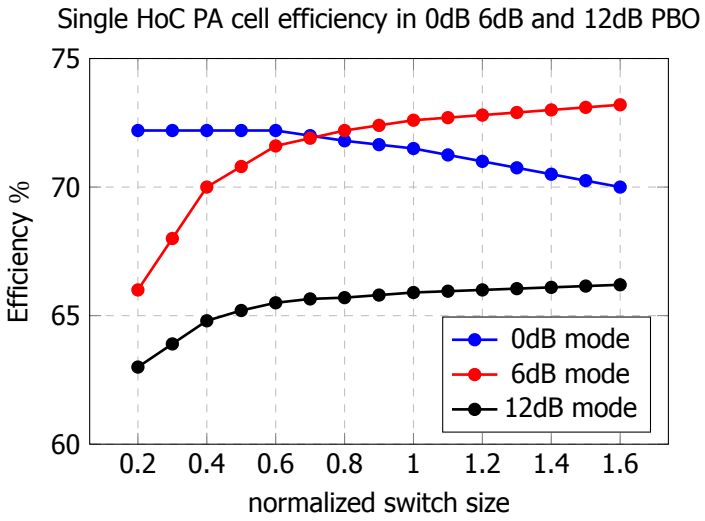


Figure 3.21: Switch optimization for Q_2 and Q_3 HoC cell in the 0dB, 6dB and 12dB PBO mode.

4

Main PA system design

In chapter 2, the concept of the deep efficiency enhancement technique was discussed. In chapter 3, the concept was turned into an actual implementation for a single PA-cell. In this chapter, the complete PA design will be discussed using the PA-cell from chapter 3 as the main building block.

4.1. Increasing PA amplitude resolution

In chapter 3, the design of the HoC PA cell was thoroughly discussed. One such HoC PA cell provides an amplitude resolution of four levels, or 2-bit. These are the four operating modes; 0 dB PBO, 6 dB PBO, 12 dB PBO and OFF.

For the target application LTE NB-IOT a much higher amplitude resolution is required as to generate higher-order QAM signals. Based on a previous design [13], an amplitude resolution of at least 13-bit is chosen. For an amplitude resolution of 13-bit the PA would need to have 8192 amplitude steps in total. Implementing these with unary PA cells would be almost impossible to layout. It would also degrade the efficiency as the switching losses of the PA cell would swamp the output power each cell could produce. Therefor, the PA is divided into three banks comprising binary weighted and thermometer coded sub-banks. The PA is first split into two, resulting in a PA_1 part and a PA_2 part. This is discussed in more detail in section 4.3. This leaves for both PA_1 and PA_2 a resolution of 4096 amplitude steps or 12-bit. The 12-bit resolution is then further divided in binary fashion over the HoC PA cell bank, a small PA cell bank, and an extra small PA cell bank. These arrangements will be called HoC-bank, S-bank and XS-bank, respectively. The XS-bank has 15 unary PA cells, each with a relative weight of $1/128$ or 1 LSB. The S-bank also has 15 unary PA cells, but they are scaled by 16 with respect to the XS-bank cells, giving them a relative weight of $1/8$ or 16 LSB. Due to the layout optimization, which will be discussed in section 4.5, the HoC-bank has 14 unary HoC PA cells, scaled by 8 with respect to the S-bank PA cells. But, as there are two HoC PA cells that are in parallel, the actual relative weighting with respect to the S-bank PA cells is also

16, resulting in 256 LSB. In Figure 4.1, the differential structure of PA_1 is shown, comprising the two parallel HoC PA cells in the HoC-banks, the PA cells in the S-bank, and the PA cells in the XS-bank. Also, the output coupling capacitors with their weight are shown. Having only 14 unary weighted HoC PA cells together with the S and XS-banks results in a total of 7423 amplitude steps for both PA_1 and PA_2, providing at least 13-bit resolution.

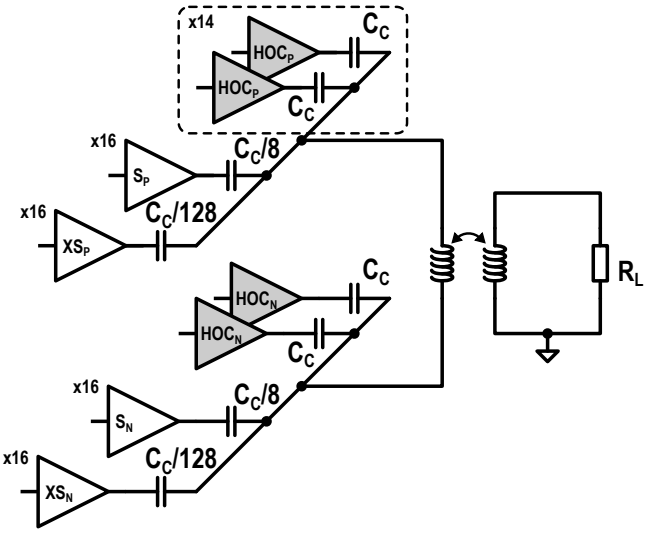


Figure 4.1: First half of the full PA architecture. Implementing the HoC PA cells for high output power and high efficiency PBO operation, smaller PA cells (S-bank and XS-bank) for increased amplitude resolution.

In chapter 3, significant effort has been made to balance the loading on the HV and LV supply domains exploiting charge sharing and current re-use. The PA cells in the S-bank and XS-bank are considerately smaller than the HoC PA cells as their output power contributions are also considerately smaller. Because the PA cells in the S-bank and XS-bank are implemented as single inverter they can only be supplied by V_{DD}. This would pose a problem if both banks would only be supplied by either the HV or LV domain supply as this would offset the charge balance that is needed in the HoC PA cells. To mitigate this problem, the PA cells from the S-bank and the XS-bank are distributed between the HV supply domain and the LV supply domain, turning on alternately between HV and LV domain maintaining equal loading on the two supply domains as much as possible.

4.2. Doherty Like Operation

In classical SCPA, the output amplitude is controlled by the number of actively switching PA slices. This effectively resembles a controllable capacitive voltage divider that is driven by a constant envelope square wave, as shown in Figure 4.2.

The output voltage is then given as:

$$V_{OUT} = \frac{2}{\pi}\left(\frac{n}{N}\right)V_{DD} \tag{4.1}$$

The output power is quadratically related to the output voltage and given as:

$$P_{OUT} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{DD}^2}{R_{OPT}} \tag{4.2}$$

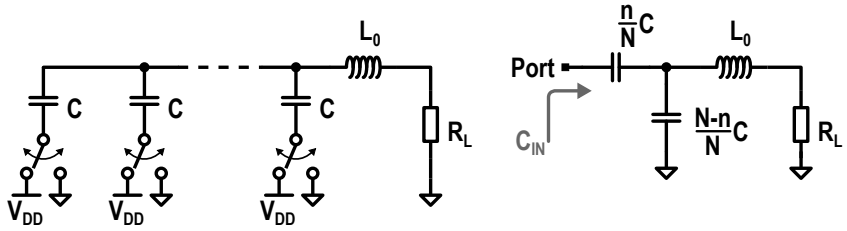


Figure 4.2: The operating principle of a conventional SCPA.

For an ideal SCPA, its efficiency is 100 %. For a real SCPA, however, this is not achievable due to various losses such as switching losses and parasitic losses. Even neglecting these losses, there is a factor that still limits the efficiency, which is the dynamic power required to charge the switch capacitance array. This dynamic power becomes dominant at lower output power levels. As shown in Figure 4.2, the series combination of the capacitor array defines the dynamic power as:

$$P_{SC} = C_{in}V_{DD}^2 f = \frac{n(N-n)}{N^2}CV_{DD}^2 f \tag{4.3}$$

Finally, the overall SCPA efficiency is defined as:

$$Eff = \frac{P_{OUT}}{P_{OUT} + P_{SC}} \tag{4.4}$$

Figure 4.3 shows the output power, dynamic power, and efficiency for a simplified 4-bit conventional SCPA. At full output power, the efficiency is equal to 100 % in this ideal example. Reducing the AM input code reduces the output power as more and more PA cells are inactive. While at the same time, the dynamic power increases as the inactive PA cells form a load on the full system or PA. At half AM input code, the dynamic power consumption is maximum and starts to fall off for output powers lower than half output power.

In classical class-G SCPA designs, the efficiency experiences two efficiency peaks if two voltage supplies are used. These peaks occur when all PA cells switch, contributing to the total output power. One peak when all PA cells switch between $2V_{DD}$ and V_{GND} while the other peak occurs when all PA cells switch between V_{DD}

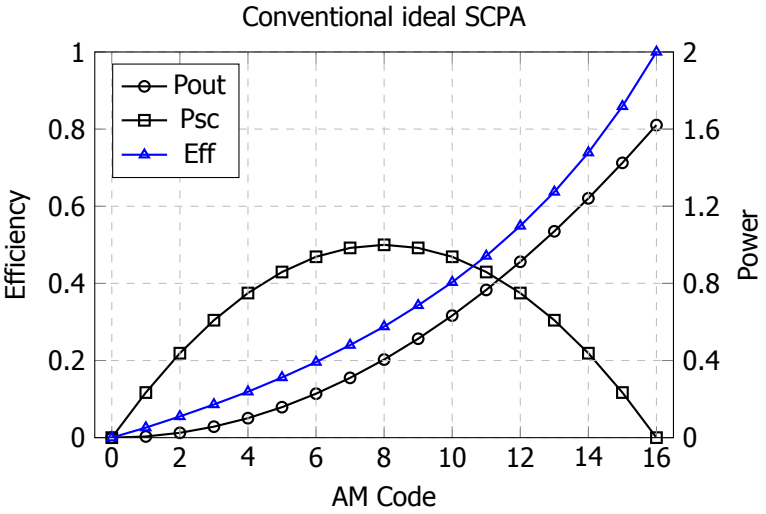


Figure 4.3: The efficiency performance of a conventional SCPA over its full output power range.

and V_{GND}. Figure 4.4 shows the output power, dynamic power, and efficiency for a simplified 4-bit conventional class-G SCPA. The efficiency curve is discontinuous at 6 dB PBO where all the PA cells switch between V_{DD} and V_{GND} at the mid code, with half of the PA cells switching between $2V_{DD}$ and V_{GND} at the next code. During the second half of the AM code, the efficiency shows no improvement compared to the conventional SCPA with only one supply.

To improve the efficiency of a class-G SCPA between the 6 dB PBO and full output power, the number of static or inactive PA cells should be reduced. This is achieved by changing the switching sequence of the SCPA and taking advantage of the DC-blocking nature of switched capacitor circuits, which was first noted in [12]. Instead of having all PA cells switching between $2V_{DD}$ and V_{GND} at full output power and increasing number of PA cells being turned off for lower output powers. Lower output power could be achieved by reducing the voltage swing instead of turning the PA cells off. When reducing the output power, the PA cells first change their voltage swing from $2V_{DD}$ by switching between $2V_{DD}$ and V_{GND}, to V_{DD} by switching between $2V_{DD}$ and V_{DD}. For lower output power more and more PA cells would lower their voltage swing until 6 dB PBO is reached and all PA cells switch between $2V_{DD}$ and V_{DD}. Only when the output power is reduced to below 6 dB are PA cells turned off and their bottom plates of the array capacitors tied to V_{GND}. Figure 4.5 shows the output power, dynamic power, and efficiency for a simplified 4-bit Doherty-like Class-G SCPA.

For the Class-G SCPA of this work, the same Doherty-like switching sequence is implemented. However, where the other works stop at 6 dB PBO, this work has a third efficiency peak at 12 dB PBO. The Doherty-like switching sequence reduces

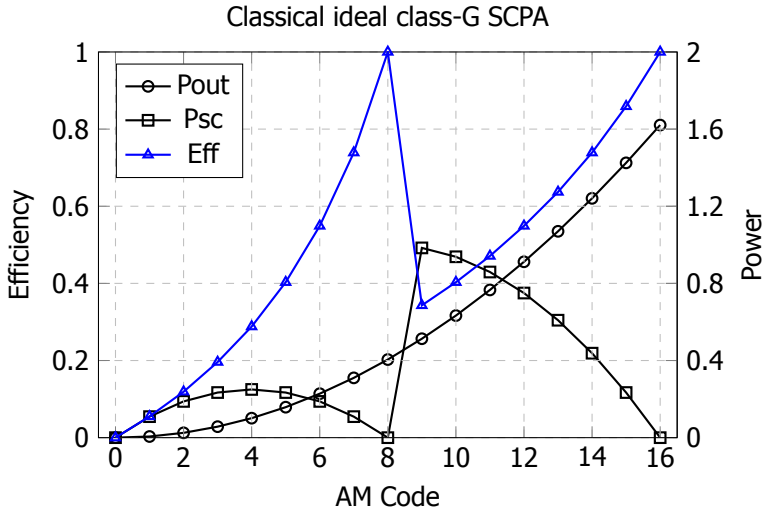


Figure 4.4: The efficiency performance of a Class-G SCPA over its full output power range.

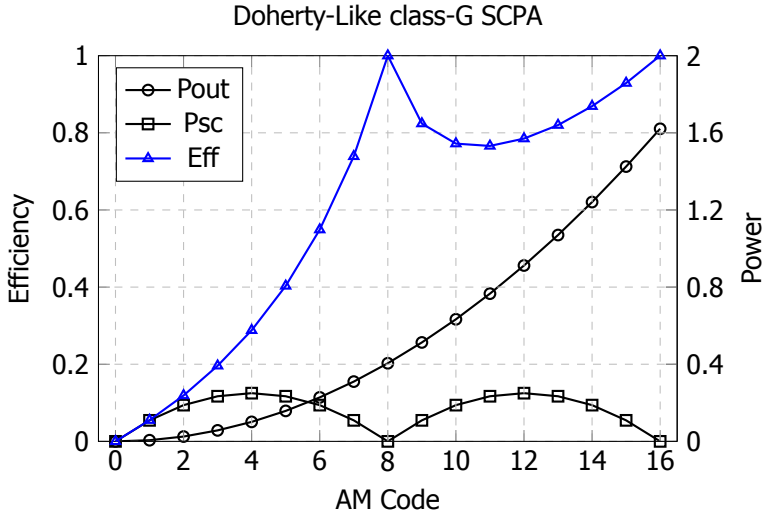


Figure 4.5: The efficiency performance of a Doherty-like Class-G SCPA over its full output power range.

the dynamic power consumption also between the 12 dB PBO and 6 dB PBO peaks. Just as the Doherty-like Class-G SCPA, all PA cells start by switching between $2V_{DD}$ and V_{GND} at full output power. Reducing the output power until the 6 dB PBO or half output power is reached, do PA cells change their output voltage swing, by

switching between $2V_{DD}$ and V_{GND} to switching between $2V_{DD}$ and V_{DD}. At half the output power, all PA cells are switching between $2V_{DD}$ and V_{DD}. Reducing the output power even further, the PA cells are switching between $2V_{DD}$ and V_{DD} or V_{DD} and $0.5V_{DD}$. At 12 dB PBO or a quarter of the output power all PA cells are switching between V_{DD} and $0.5V_{DD}$. Finally, reducing the output power until the PA is not providing any output power anymore, the PA cells are switching between V_{DD} and $0.5V_{DD}$, and the other PA cells are turned off and the bottom plates of the array capacitors tied to V_{GND}. Figure 4.6 shows the output power, dynamic power, and efficiency for a simplified 4-bit Doherty-like Class-G HoC SCPA.

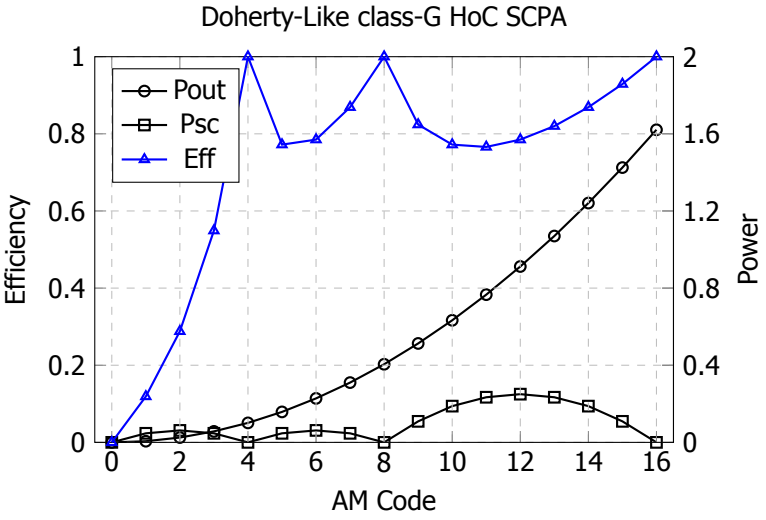


Figure 4.6: The efficiency performance of a Doherty-like Class-G HoC SCPA over its full output power range.

An efficiency comparison between the four SCPA topologies discussed is shown in Figure 4.7.

4.3. Splitting the PA

In section 4.1, it was mentioned that the PA consists of two cores: PA_1 core and PA_2 core. Further improving the efficiency at low output power is the main reason for splitting the PA into two. In section 4.2, the most efficient way of switching the PA cells is discussed. A similar idea is used on a global level for PA_1 core and PA_2 core. When sweeping the output power from zero to maximum, the PA starts with all PA cells in both PA_1 core and PA_2 core "OFF". Then, when the output power of the PA starts to increase, the PA cells change their operating mode from "OFF" to the 12 dB PBO mode. There are now two choices; alternately change the operating modes of the PA cells in PA_1 core and PA_2 core, or first change all the operating modes of the PA cells in the PA_1 core. In the second situation, the PA_2 core can be fully disabled, saving power consumption of the LO buffers of that core. The

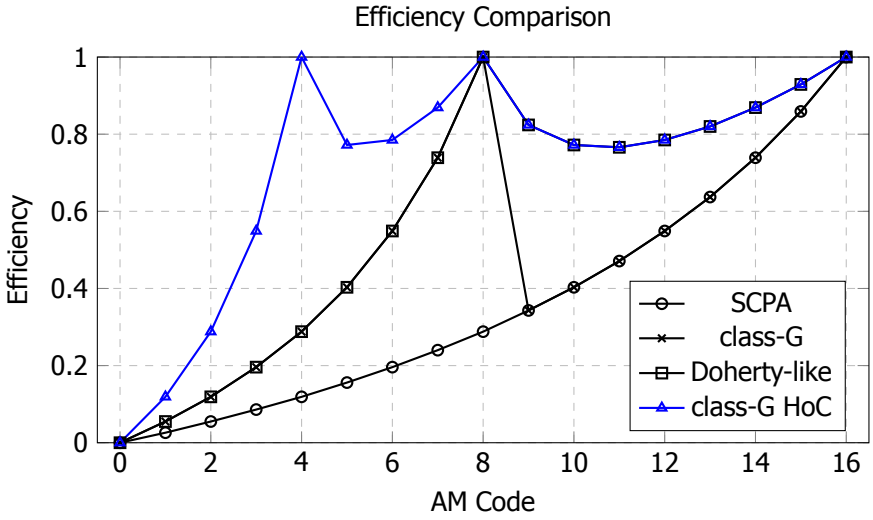


Figure 4.7: The efficiency performance comparison of a conventional SCPA, Class-G SCPA, Doherty-like Class-G SCPA and Doherty-like Class-G HoC SCPA over their full output power range.

other mode is where both the PA_1 core and PA_2 core are active while alternately changing the operating modes of the PA cells in the PA_1 core and PA_2 core, reducing the impact of the gain mismatch between the two cores, improving the linearity.

The PA with its two PA_1 core and PA_2 core is shown in Figure 4.8. What becomes obvious is that the S-bank and XS-bank PA cells are not used in the second PA_2 core. The S-bank and XS-bank PA were added to increase the overall PA resolution of which only one is needed. Furthermore adding or distributing the S-bank and XS-bank over the PA cores would undo the benefit of being able to turn on a complete core as the S-bank and XS-bank are needed from zero to full output power. As they are intermediate steps between the levels provided by the HoC PA cells.

4.4. Output capacitance mismatch

The output amplitude of an SCPA is directly related to the number of capacitors being switched among the total number of capacitors in the array. In previous section 4.3, the two PA cores were introduced. By implementing the two PA cores where the PA_1 core also includes the additional S-bank and XS-bank PA cells, mismatched capacitance is introduced between the two PA cores. The total capacitance of the array in PA_1 core as shown in Figure 4.8 is:

$$C_{in}(PA_1) = \frac{(14 \cdot 2 \cdot C) + \left(15 \cdot \frac{C}{8}\right) + \left(16 \cdot \frac{C}{128}\right)}{2} = 15C \tag{4.5}$$

While the total capacitance of the array in PA_2 core is:

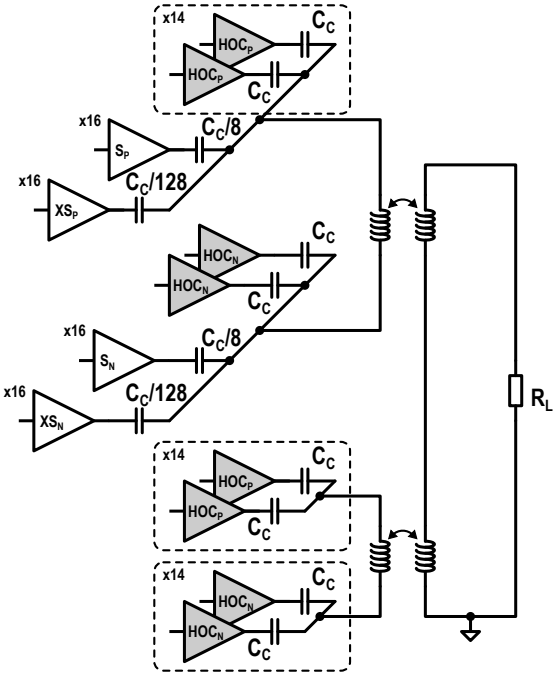


Figure 4.8: Two halves (PA1 and PA2) of the full PA architecture. PA1 implementation entails the HoC PA cells for high output power and high efficiency PBO operation, smaller PA cells (S-bank and XS-bank) for increased amplitude resolution. PA2 implementation entails only the HoC PA cells for high efficiency PBO operation.

$$C_{in}(PA_1) = \frac{(14 \cdot 2 \cdot C)}{2} = 14C \tag{4.6}$$

Due to this capacitance mismatch, PA1 core delivers slightly different power than the PA cells in PA_2, degrading the linearity of the PA. An illustration is shown in Figure 4.9 where the output powers of two PA cores are depicted, one with a total equivalent array capacitance of $15C$ and one with a total equivalent array capacitance of $14C$.

In the PA mode where the PA cells are alternately activated in PA_1 core and PA_2 core, the DNL would suffer as each *odd* code that actives a cell in PA_1 has an amplitude step that is slightly different than the *even* am code which actives a cell in PA_2, as shown in Figure 4.10. In the other PA mode where first all PA cells in PA_1 are activated until the maximum am code for that PA core is reached and then the PA cells in PA_2 are activated, the INL degrades as a relatively large slope change occurs when the second PA core is activated and sweeps from zero to max output

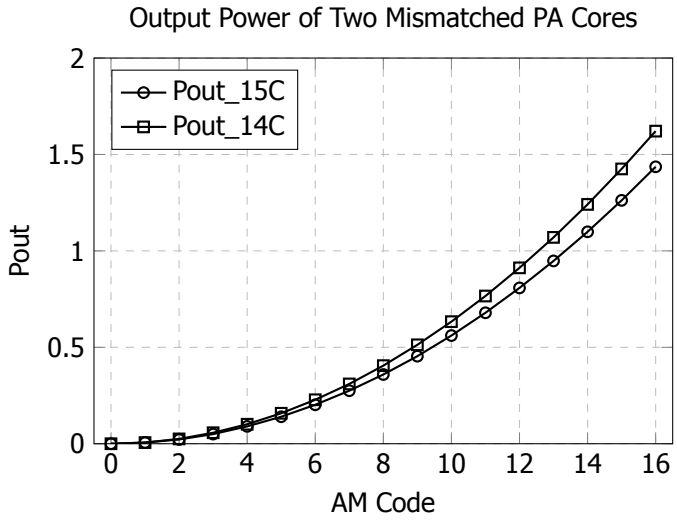


Figure 4.9: Individual output power of the two PA-cores where only one of the two PA-core is active while the other PA-core is inactive. It shows output power mismatch due to the output capacitance mismatch between the two PA-cores.

power.

To solve this linearity issue the total equivalent array capacitance in both the PA_1 core and PA_2 core must be equal. Reducing the array capacitance in the PA_1 core is not an option as it is needed to increase the resolution of the PA. That leaves adding extra capacitance in the PA_2 core. Figure 4.11 shows the added switchable capacitor bank with a size equal to the combined size of the S-bank and XS-bank in the PA_1 core, split into 5-bit, additionally allowing calibration of the two PA cores.

4.5. PA Top Level Floorplan

In this section, the floorplan of the chip will be introduced, providing a clearer picture for the upcoming sections. In chapter 3, the HoC PA cell structure was presented, providing the 12 dB PBO efficiency peaking increasing the efficiency at reduced output power. These HoC PA cells are put in parallel together with additional smaller PA cells increasing the total PA resolution, as discussed in section 4.1. In section 4.3, the PA is split into two PA cores; PA_1 core and PA_2 core. This could improve the efficiency even further at low output power by disabling half of the PA, and therefore, also the LO buffers driving the PA cells. From here, the current PA floorplan is drawn as shown in Figure 4.12, where the two PA cores have a 3x5 grid, of which 14 are HoC PA cells and the PA_1 core has the additional smaller PA cells in the form of a S-bank and XS-bank. The PA_2 core instead has the tunable capacitor bank.

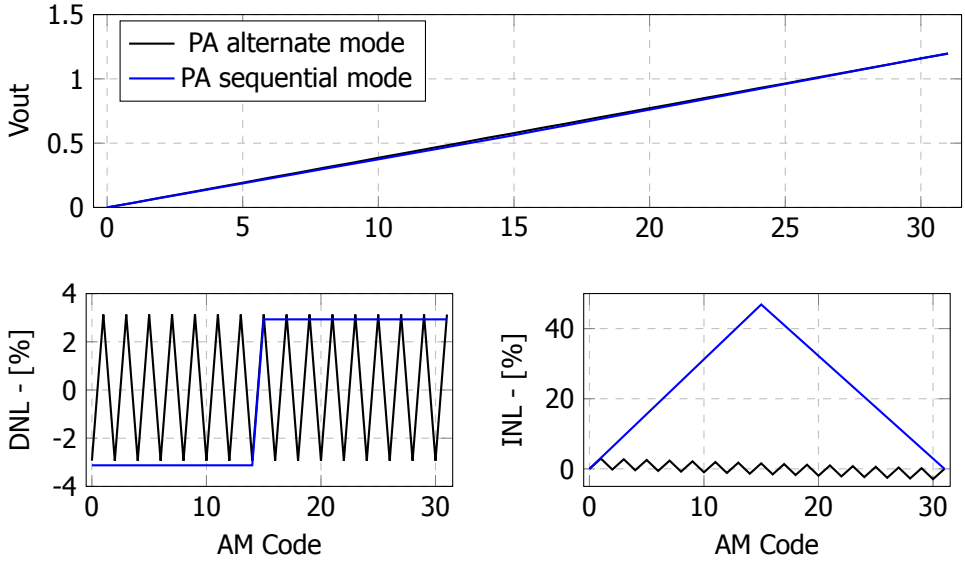


Figure 4.10: Two possible drive modes using both PA-cores. The sequential mode uses first all PA-cells in PA1 and, when saturated, switches to PA2. Toggling mode activates alternatingly PA-cells from PA1 and PA2 until both PA-cores are saturated.

4.6. LO column drive distribution

The principle of reducing the power consumption of the LO drivers by disabling LO drivers - of the PA core that is not active - can be extended to the HoC PA cells within the PA cores. At low output power, not all HoC PA cells will be active. The LO drivers of these HoC PA cells could be turned off to reduce the power consumption. A trade-off between layout complexity and efficiency gain needs to be evaluated. Giving each HoC cell in the PA cores its own LO driver would increase the layout/design complexity while the efficiency improvement would be marginal. Therefor, the HoC PA cells are driven column-wise, simplifying the layout while maintaining the efficiency improvement, as shown in Figure 4.12.

When sweeping the output power from zeros to maximum, the PA cells that first need to be turned on are the XS-bank PA cells and S-bank PA cells. With increasing power the HoC PA cells also need to be enabled one by one. For optimal efficiency the turn-on sequence of the HoC PA cells needs to match with the column LO drivers. The 14 HoC PA cells in the PA core, as shown in Figure 4.12, are turned on in the sequence: HoC_0, HoC_1, ..., HoC_{13}. Initially, the LO driver LO_DRV_0 is turned on, supplying the LO signal to the XS-bank and S-bank PA cells, as well as the two HoC PA cells (HoC_0 and HoC_1) in that same column (Col_0). The two HoC PA cells start in the 12 dB PBO mode. Two options are available for even higher output power; the two HoC PA cells first could cycle through their operating modes

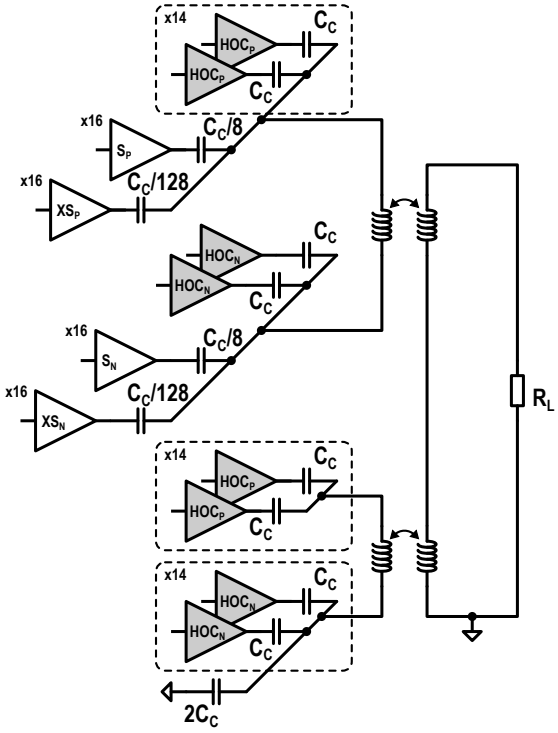


Figure 4.11: Two halves (PA1 and PA2) of the full PA architecture. PA1 implementation entails the HoC PA cells for high output power and high-efficiency PBO operation, smaller PA cells (S-bank and XS-bank) for increased amplitude resolution. PA2 implementation entails only the HoC PA cells for high-efficiency PBO operation with added loading capacitance to match the total output capacitance of PA1 and PA2.

before the next column is activated, or the next column could be activated. The first option has improved efficiency, while the second option reduces the stress by back driving of the inactive HoC PA cells.

4.7. Global PBO signal decoding logic

In section 3.5, the local decoding logic for the HoC PA cells was discussed. The four operating modes of the HoC PA cell, off, 12 dB PBO, 6 dB PBO, and 0 dB PBO require different gate voltages on the switches in the four PA unit cells. To simplify the routing, the four modes are encoded onto a 2-wire interface. The decoding and gate voltages are then generated locally in the HoC PA cells. Each HoC PA cell in the PA cores, therefore, needs four signals to set their operating mode. Two signals carry the operating mode information in the LV-domain and another two signals for the HV-domain. The signals for the HV-domain are level shifted on the left and

right side of the PA_1 core and PA_2 core, respectively, as shown in Figure 4.12. The four signals are then routed horizontally to each individual HoC PA cell.

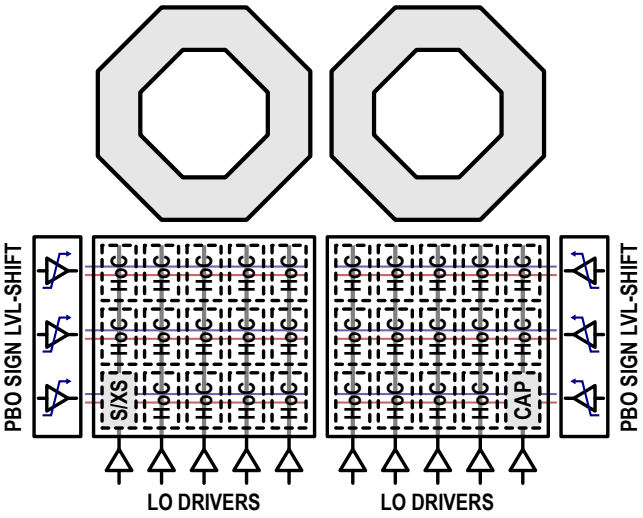
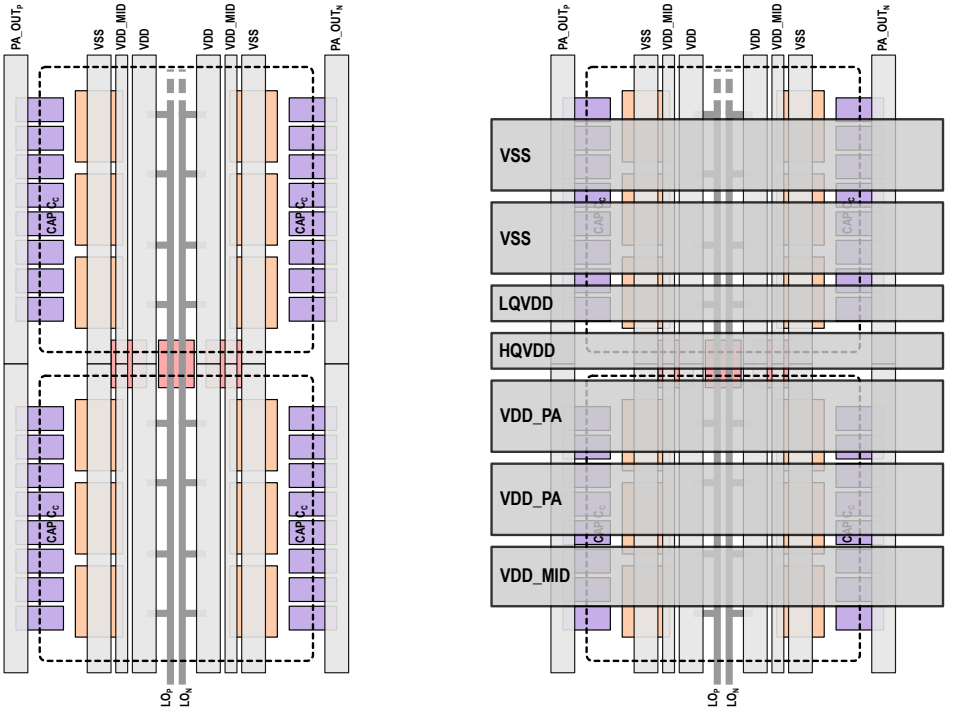


Figure 4.12: Conceptual floorplan of the complete PA chip. Power combiner at the top. The Two PA-cores (PA1 left, PA2 right). Control signal level shifters at the outer edges and LO drivers on the bottom, one for each column.

4.8. Power distribution and routing

The final step in the chip layout floorplan is the power routing. This includes the power domains that are used in the HoC PA cells as well as the output power connections collecting the output power of the HoC PA cells. Because the HoC PA cells have five power supply levels; $2V_{DD}$, $\frac{3}{2}V_{DD}$, V_{DD}, $\frac{1}{2}V_{DD}$ and V_{GND}, as well as, two output power connections, the power routing is not trivial. For the power routing, two metal layers are used; thick copper metal 8 layer (M8) and an ultra-thick aluminum layer (AP). The M8 layer connects the supplies $2V_{DD}$, V_{DD}, and V_{GND} and the output power connections P_{OUT_P}, P_{OUT_N} to all PA cells vertically. With the AP layer, the power supplies $2V_{DD}$, $\frac{3}{2}V_{DD}$, V_{DD}, $\frac{1}{2}V_{DD}$, and V_{GND} are connected horizontally, forming a power grid supplying all necessary supplies to the HoC PA cells. Over each HoC PA cell row, the AP layer consists of V_{GND}, $\frac{1}{2}V_{DD}$, $\frac{3}{2}V_{DD}$, $2V_{DD}$, $2V_{DD}$, V_{DD}, and V_{GND}. This is repeated vertically three times, covering all three rows spanning over the two PA cores, as shown in Figure 4.13(a).

Over each HoC PA cell column, the M8 layer consists of V_{GND}, V_{DD}, $2V_{DD}$, $2V_{DD}$ V_{DD}, and V_{GND}. As with the AP layer, this is repeated for each column in the two PA cores, as shown in Figure 4.13(b).



(a) Floorplan and vertical power routing of the HoC PA cell.

(b) Horizontal power distribution principle for HoC PA cell and PA cores.

Figure 4.13: Vertical or column-wise power routing principle for HoC PA cells and horizontal or row power routing.

5

Digital system design

In this chapter the digital design will briefly be discussed. The digital implementation was performed by the digital team of IMEC and a large part of this digital design was taken from the previous PA [13]. This means that only the small changes that were made will be discussed. In section 5.1, the 14-bit wide binary AM-data input bus is split for the different PA cores and PA banks. In section 5.2, the AM amplitude compression is introduced. Finally, two dithering techniques were implemented. The first one is introduced in section 5.3 where the AM code for the PA_1 core and PA_2 core could be swapped periodically. And the second one is unveiled in section 5.4 where the PA cells in the S bank can be swapped between the HV and LV domain, reinforcing the charge sharing between the two voltage domains.

5.1. AM code splitting and distribution

In section 4.1, the resolution of the PA was briefly discussed. The PA was split into two parts PA_1 and PA_2 as well as extra small PA cells were added to further increase the total PA resolution. Each PA bank (XS-bank, S-bank, and HoC-bank) is implemented with unary-sized PA cells. The banks with respect to each other are, however, binary sized. This requires the 14-bit wide binary AM-data input bus of the chip to be split for each PA bank and converted to unary coding.

The 14-bit AM-data input is first split into two 4-bit data streams for the XS-bank and S-bank PA cells. The LSBs of the AM-data input (AM-data[3:0]) are used for the 15 PA cells in the XS-bank. The next LSBs of the AM-data input (AM-data[7:4]) are used for the 15 PA cells in the S-bank. Both the AM-data[3:0] and AM-data[7:4] are directly converted to unary coding. The resulting 6-bits (AM-data[13:8]) are partially used for the HoC-banks in PA_1 and PA_2.

As discussed in section 4.1, the number of HoC PA cells in both PA_1 and PA_2 is 14. Because the HoC PA cells can operate in different modes, the effective resolution is doubled for each HoC PA cell. This gives an effective resolution of 28 for both PA_1 and PA_2. A total of 56, where there are 64 (6-bit) available. In section 5.2 the

reason for having only double the resolution and not triple the resolution as would be expected is discussed in more detail. The 5-bit data stream for the HoC PA cells in PA_1 are set by the LSBs of AM-data[13:8] capped at a maximum of 28 which is the maximum resolution of the HoC-bank. Above 28, the resulting bits are put in the 5-bit data stream for the HoC PA cells in PA_2. Again capped at a maximum of 28. Finally, all AM-data streams are converted to unary coding and outputted to the AFE. The final effective resolution of the PA is given as:

$$PA_{RES} = 15 \cdot (1LSB) + 15 \cdot (16LSB) + 2 \cdot 14 \cdot (256LSB) = d'14846 \quad (5.1)$$

5.2. AM code to PBO signals encoding

The HoC PA cells have four operating modes as is discussed in section 3.2. With four operating modes a HoC PA cell is able to generate three different voltage levels as well as an off state. This gives the HoC PA cell an output resolution of 2-bits. In section 5.1, however, the total resolution of PA_1 and PA_2 is only double the amount of HoC PA cells. This is due to PA amplitude compression that is needed to keep the output of the PA linear.

To explain the need for this PA amplitude compression, we first consider the case where the full resolution of the HoC PA cells is used. As an example, a PA with eight HoC PA cells is used. When the output power of this PA is increased from zero to maximum, the HoC PA cells first switch to the 12 dB PBO operating mode. This produces a voltage swing of $\frac{1}{2}V_{DD}$ when all HoC PA cells are operating in the 12 dB PBO operating mode they switch to the 6 dB PBO operating mode producing double the voltage swing of V_{DD}. Finally, when again all HoC PA cells operate in 6 dB PBO the cells switch to the maximum output power mode or 0 dB PBO mode. In this mode, the output voltage swing is again doubled to $2V_{DD}$. However, the amplitude step is also doubled compared to changing from the 12 dB PBO operating mode to the 6 dB PBO operating mode. This produces a non-linear output, as shown in Figure 5.1. When the input code switches from 16 to 17, meaning all HoC PA cells were operating in the 6 dB PBO mode, and one HoC PA cell is switched to the 0 dB PBO operating mode, the amplitude step difference is clearly visible.

To fix the non-linear behavior, each step of the AM input code should result in the same amplitude voltage step. When a single HoC PA cell switches from the 0 dB PBO operating mode to the 6 dB PBO operating mode, the voltage step is equal to V_{DD} as the swing reduces from $2V_{DD}$ to V_{DD}. However, when a single HoC PA cell switches from the 6 dB PBO operating mode to the 12 dB PBO operating mode, the voltage step is $\frac{1}{2}V_{DD}$ as the swing reduces from V_{DD} to $\frac{1}{2}V_{DD}$. The same is true when switching from 12 dB PBO operating mode to OFF state as the swing reduces from $\frac{1}{2}V_{DD}$ to 0. Therefor, one HoC PA cell switches from the 0 dB PBO operating mode to 6 dB PBO operating mode. Two HoC PA cells should switch from 6 dB PBO operating mode to 12 dB PBO operating mode or 12 dB PBO operating mode to OFF state, which in this report is called AM amplitude compression. An example of the AM amplitude compression is shown in Figure 5.2.

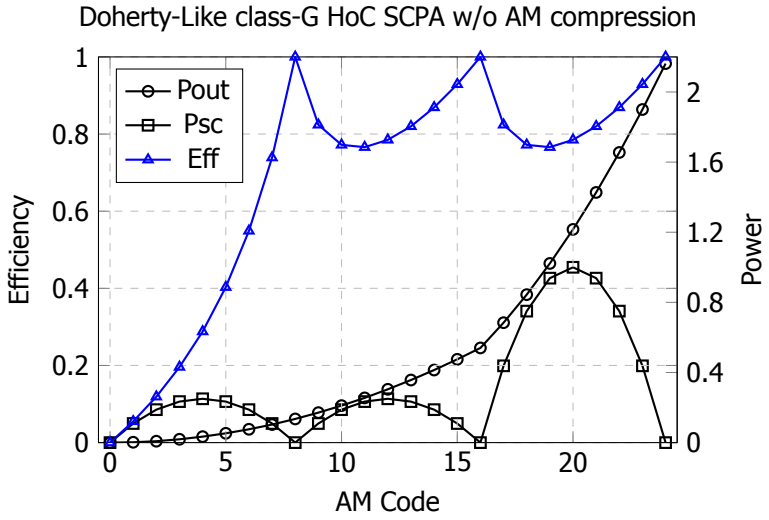


Figure 5.1: Efficiency performance of a doherty-like class-G HoC SCPA over its full output power range. The switching scheme without AM amplitude compression.

The switching sequence for both with compressed amplitude switching and without compressed amplitude switching is shown in Figure 5.3. One block represents a HoC PA cell that can operate in either the 12 dB PBO, 6 dB PBO or 0 dB PBO operating mode. The height represents the amplitude. Again the non-linear output of the non-compressed amplitude switching is clearly visible, which is solved by switching two PA cells in the 12 dB PBO and 6 dB PBO mode.

5.3. PA1 and PA2 AM code dithering

In section 4.3, the most efficient activation of the PA_1 core and PA_2 core was briefly discussed. The options providing either better efficiency by activating first the complete PA_1 core and only when PA_1 core is saturated, activating PA_2 core. Or the other option with better linearity when for each amplitude step a HoC PA cell alternately is activated in the PA_1 core and PA_2 core. This can be even further expanded by allowing the codes that drive PA_1 core and PA_2 core to be switched at the same rate as the LO. This mitigates the non-linearity that is introduced by splitting the PA into two cores. Any mismatch between the PA_1 core and PA_2 core is averaged out by this code dithering, improving the linearity. Also, in this situation no efficiency can be gained as both PA cores have to be active all the time even for low output powers.

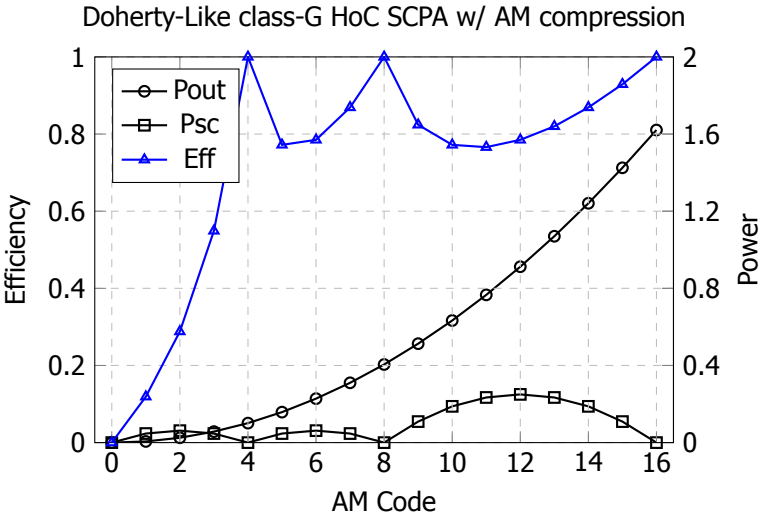
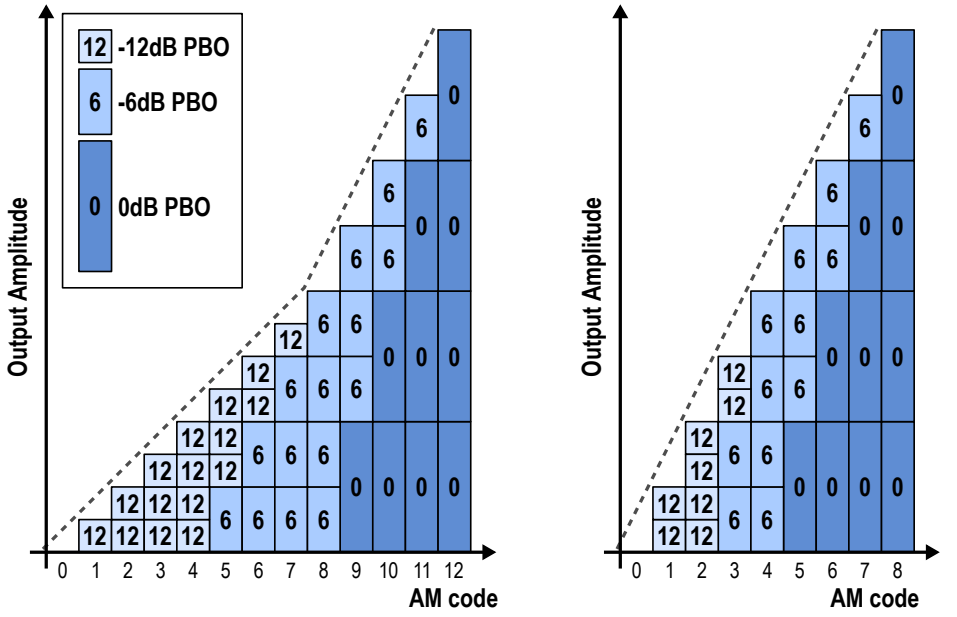


Figure 5.2: Efficiency performance of a doherty-like class-G HoC SCPA over its full output power range. The switching scheme includes AM amplitude compression reducing effective amplitude resolution.

5.4. S PA cells HV and LV dithering

In section 4.1, and section 4.4, the XS-bank and S-bank PA cells were introduced to increase the total PA resolution. These PA cells in these banks are implemented as simple inverters, and therefor, supplied by only V_{DD}. In section 4.1 it was mentioned that these PA cells in both the XS-bank and the S-bank are distributed between the HV and LV-domain. However, as the number of PA cells in both banks is uneven a mismatch is introduced on the power draw between the HV and LV power domain. Even though the PA cells in the XS-bank and the S-bank require significantly less power than the HoC PA cells and the middle supply rail is stabilized by an LDO. Another mechanism is put into place to reduce the charge imbalance as much as possible. In the same way as in section 5.3 also the code for the XS-bank and S-bank is swapped at the rate of the LO, averaging the power draw for the HV and LV supply domains.



(a) Switching scheme without amplitude compression.

(b) Switching scheme with amplitude compression.

Figure 5.3: Comparison of the two switching schemes. With and without amplitude compression showing non-linear output for the non-amplitude compression scheme.

6

Results

In this chapter the measurement results of the proposed TX will be addressed. In section 6.1 the measurement setup will be briefly explained. Showing the unpackaged chip cavity mounted on the manufactured PCB and the method of controlling the chip. section 6.3 demonstrates the performance of the chip under continuous-wave operation and compare the measured results with simulated data. Finally in section 6.4 the proposed TX will be bench marked against state-of-the-art TXs that likewise focus on improving PA/TX efficiency by utilizing deep PBO efficiency enhancement techniques. The proposed Doherty-like class-G HoC SCPA is implemented in a TSMC 40 nm CMOS process. Figure 6.1 depicts the chip top layout as well as the PA HoC cell. The chip occupies an area including the padring of 1900 µm x 2100 µm = 3.99 mm^2, with an active area of 1180 µm x 700 µm = 0.826 mm^2, before shrink.

6.1. Measurement Setup

The chip requires seven different supply voltages to operate, V_{DD_PA} = 2.0 ... 2.2V which is the main high power supply for the PA, V_{DD_PAMID} = 1.0 ... 1.1V to stabilize the self-generated half supply voltage, V_{DD_PAHQ} = 1.5 .. 1.65V three quarter supply voltage used to drive the output short switch, V_{DD_PALQ} = 0.5 .. 0.55V one quarter supply voltage used to drive the output-short switch, V_{DD_LO} for the input LO buffers, V_{DD_DIG} = 1.0 ... 1.1V for the SPI interface and digital control[1], V_{DD_IO} = 1.2 V for the I/O pad ring. The supply voltages are generated on the PCB employing on-board regulators. TPS7A8101DRBR from Texas Instruments, for the main high power PA supply V_{DD_PA} = 2.0 ... 2.2V. Three LM8272 from Texas Instruments take care of the other PA supply domains as they require less power. Three LT3021-1.8 LDOs are used to supply the V_{DD_LO}, V_{DD_DIG}, and V_{DD_IO} supply domains. On-board potentiometers are employed to precisely set the required voltage as well as being able to adjust the voltage slightly over a small range. At the output of each regulator

[1]Special thanks to the digital design team for designing and synthesizing the SPI interface.

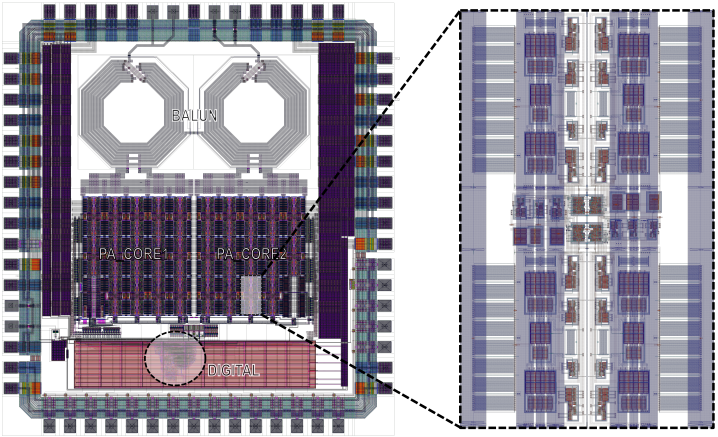


Figure 6.1: IC-TOP layout of the proposed Doherty-like class-G HoC SCPA TX (left). The layout of a single HoC PA cell (right).

and thus for each supply domain, a jumper is placed as a potential tap-off point for current measurements. An on-board balun is used to convert a single ended input clock to a differential clock as required by the chips input clock interface. Due to the on-chip output balun, the differential PA output is easily converted to a single-ended signal. Finally, the SPI interface of the chip is connected to a Teensy, which handles the communication from UART to the SPI interface of the chip.

6.2. Simulation Results

From the post-layout simulation, a maximum efficiency of 42.3 % and peak output power of 27.7 dBm can be expected, as shown in Figure 6.2. This occurs at maximum input code. Furthermore, six efficiency peaks can be distinguished corresponding to the three operating modes: −12 dB, −6 dB, and 0 dB PBO for each PA core. The efficiency for the full PAs −12 dB (Input Code = 14k), −6 dB (Input Code = 7k), and 0 dB (Input Code = 3.5k) PBO points are respectively 42.3 %, 30.9 % and 27.3 %. The targeted operating frequency range of the proposed TX is 700 MHz to 900 MHz. Figure 6.2 shows the expected output power and efficiency performance for this frequency range. Based on the post-layout simulation, the peak efficiency is 42.3 % at 840 MHz. While the maximum peak output power of 27.7 dBm at 900 MHz is to be expected. The last graph in Figure 6.2 shows the simulated efficiency where only the first PA core (PA1) is active at 780 MHz. The reason will be discussed in section 6.3.

6.3. Measurement Results

In the previous section (section 6.2), simulations showed that a peak efficiency of 42.3 % can be expected, and a peak output power of 27.7 dBm at a frequency of

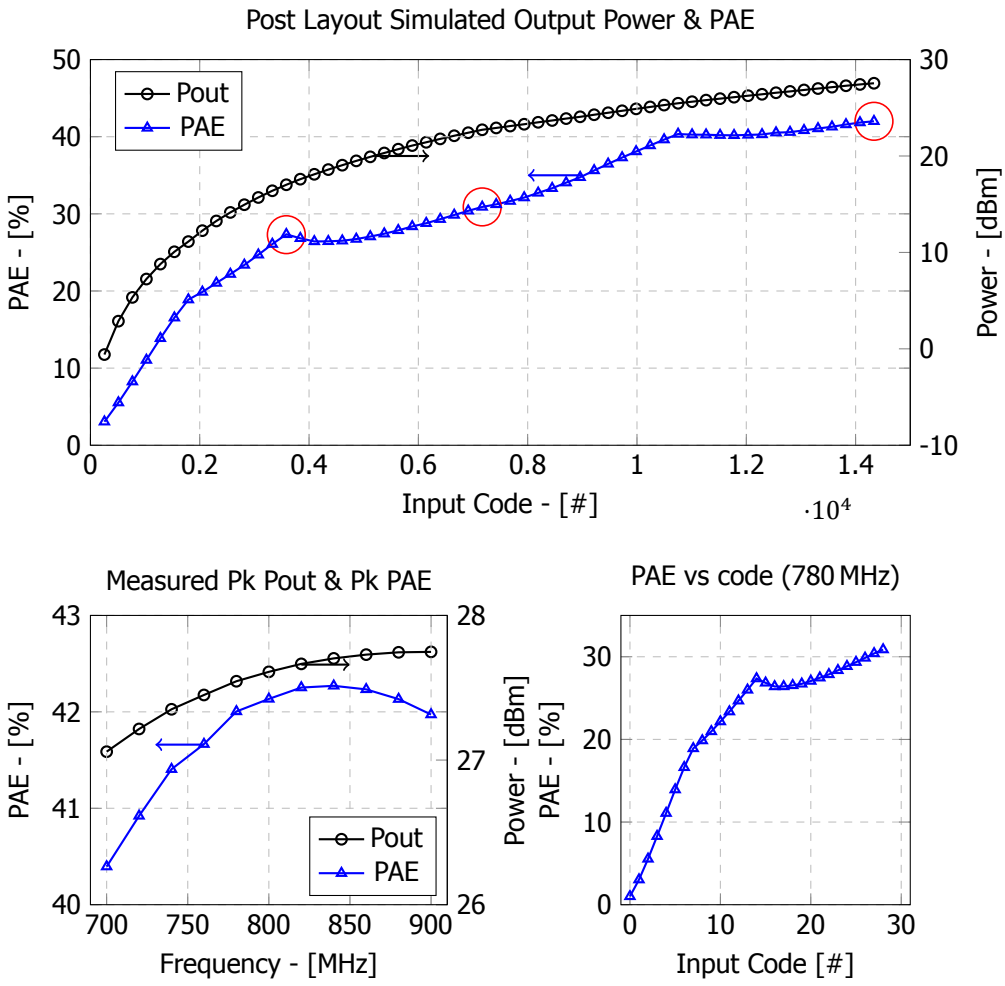


Figure 6.2: Post layout simulation results. Top, full input code sweep for Pout and PAE. Bottom left, frequency sweep from 700 MHz to 900 MHz for Pout and PAE. Bottom right, input code sweep for PA1 core only showing PAE.

820 MHz. Upon first measurements, the peak output power only reached about 18 dBm, which is far from the simulated 27 dBm. After numerous attempts, the measured peak output power could not be improved. Only after manually verifying the layout, a problem was identified. The output balun was incorrectly connected to one of the PA cores. This meant that the PA cores are operating 180° out of phase of each other, causing destructive power combining. As a result, only one PA core can be active at a time. This also has an impact on the overall efficiency of the PA as the unused PA core is still loading the other PA core, even though it is not active. All measurements results in this section are therefore performed with only PA1 core active and PA2 core disabled, unless specified otherwise. The top graph

in Figure 6.3 shows the measured peak output power and efficiency performance over the frequency range of 700 MHz to 900 MHz in steps of 10 MHz. The maximum measured efficiency is 21.7 % at 830 MHz. The maximum measured peak output power is 22.1 dBm at 780 MHz. A noticeable dip in peak output power of almost 1 dB occurs at 750, 760, and 770 MHz. The bottom left graph in Figure 6.3 shows an output power sweep at 780 MHz. The PA is linear throughout the −12 dB PBO mode operation (first seven codes, or 14 active PA cells). However, in the −6 dB and 0 dB PBO mode, severe non-linearity occurs. This can also be seen in the bottom right graph in Figure 6.3, which shows the efficiency for the same code sweep.

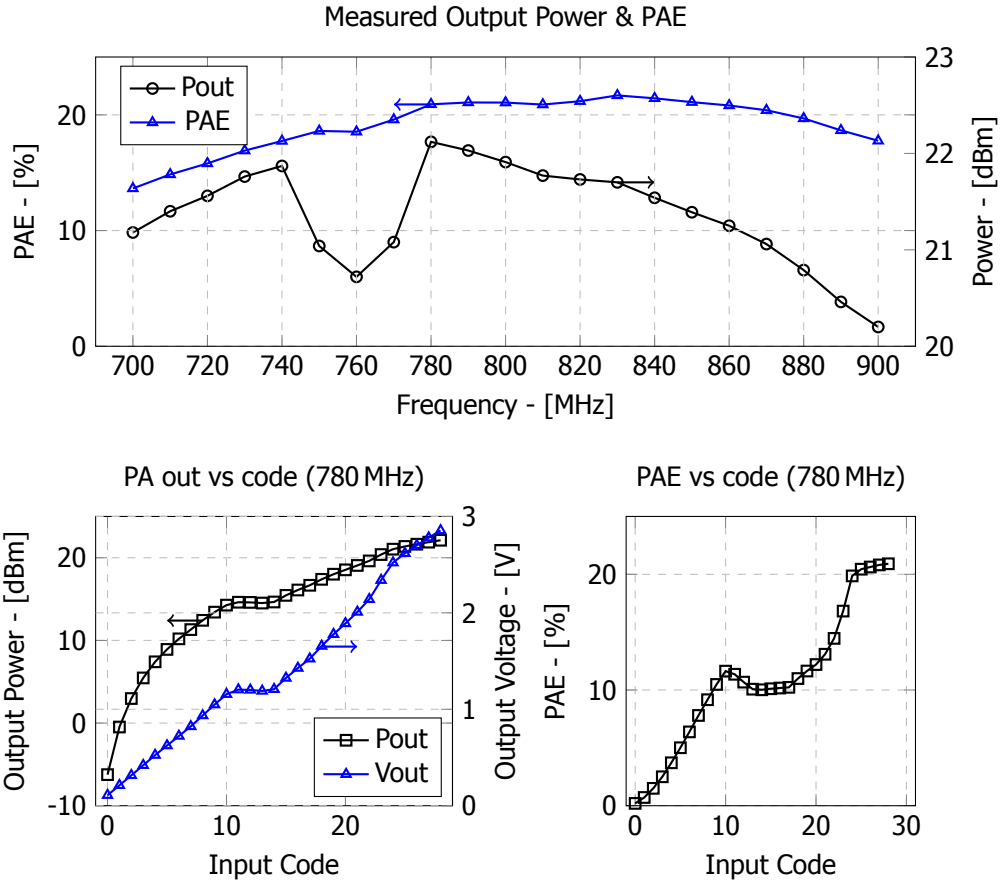


Figure 6.3: Measurement results. Top, frequency sweep from 700 MHz to 900 MHz for Pout and PAE. Bottom left, input code sweep for PA1 core only for Pout and Vout. Bottom right, input code sweep for PA1 core only showing PAE.

Figure 6.4 compares the post-layout simulation results with the measured results for the same conditions. Clearly, the mistake in the balun layout connection has made a severe impact on the overall performance of the PA. Not only because half of the PA cannot be used, but also the incorrect operation in the −6 dB PBO mode

with high nonlinearity.

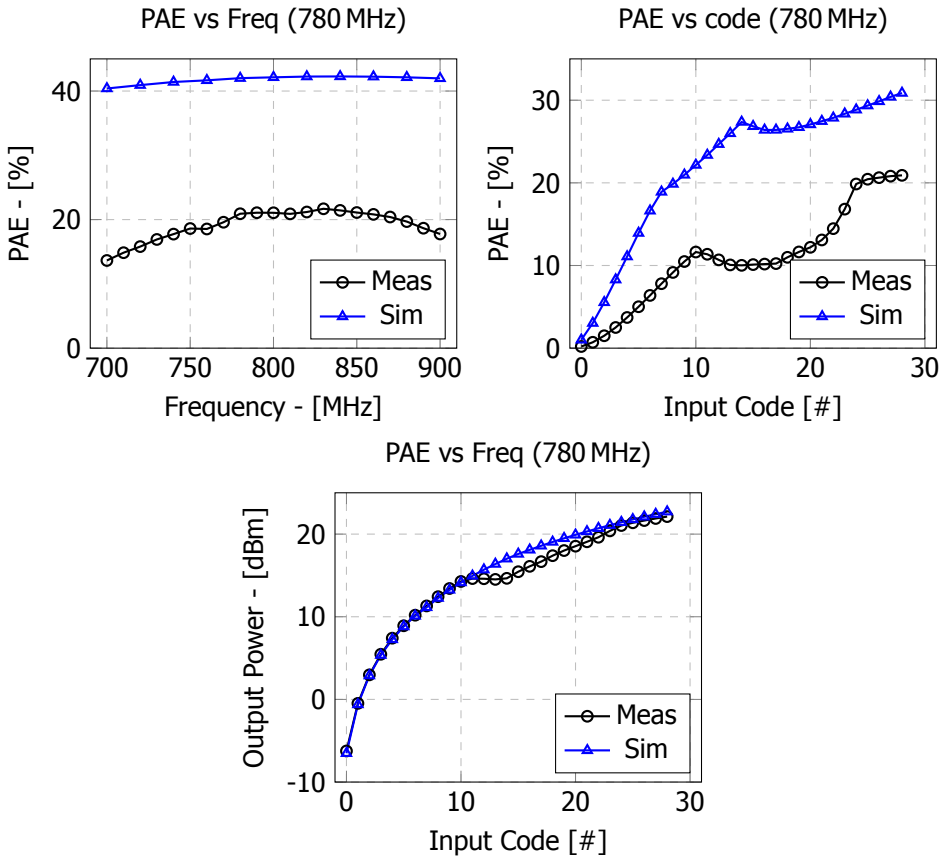


Figure 6.4: Post layout simulation results compared with measurement results. Frequency sweep from 700 MHz to 900 MHz of PAE (top left). Input code sweep for PA1 core only showing PAE (top right). Input code sweep for PA1 core only showing Pout (bottom).

6.4. State-of-the-art comparison

Table 6.1 summarizes the performance of the proposed Doherty-like Class-G HoC PA and compares it with other state-of-the-art PAs with deep PBO enhancement techniques. Note that for this work, both the simulation as well as the measured performance is provided.

Table 6.1: Comparison summary of proposed Doherty-like Class-G HoC PA.

Parameter	**Unit**	**This work** Sim	Meas	[13]	[8]	[19]	[6]	[7]	[18]
Technology		40nm		40nm	55nm	65nm	45nm	65nm	65nm
Area	mm^2	3.99/1.44 (PA)		5.0/1.8 (PA)	1.11	1.62	1.21	3.2	1.68
Freq. range	MHz	700-900		699-915	850/1700	750-1015	900/2400	±2900-4800	±1900-2120
Incl. on-PCB loss		Y		Y	N/A	Y	N	N	Y
Integrated balun		Y		Y	N	N	N	Y	N
PBO technique		HoC Class-G		Ssup Class-G	Doherty	VM-Doherty	Outphasing	Class-G Doherty	Class-G
Supply	V	2-2.2		2.2	1.2/2.4	1.2/2.4	1.2/1.7	1.65/3.0	1.4/2.8
Freq.	MHz	840	780	807	±850	900	900	3710	2150
Peak Pout	dBm	27.7	22.1	27.1	28.9	24.0	24.4	26.7	24.3
PAE @0 dBm	%	42.3	20.9	33.3	36.8	45	55	40.2*	43.5
PAE @−6 dBm	%	30.9	10.0	22.5	29.9	34	32	37.0*	36.5
PAE @−12 dBm	%	27.3	7.8	14.4	±15	±17	11	26.2*	±18

* drain efficiency not PAE

7

Conclusion

In this thesis, a detailed report of the concept, design, and implementation of a Doherty-like Class-G HoC PA is provided. In this final chapter, the outcome of this work will be discussed and reiterates on the achievements that were made. Furthermore, the shortcomings and possible improvements of this work will be briefly discussed.

In most, if not all, wireless IC designs, the PA is the most power-hungry component. Hence achieving high power efficiency is most effective by improving the overall efficiency of the PA. With the increasing demand for higher data rates, more advanced modulation techniques are required, such as QAM, where two amplitude modulation signals are combined into a single channel. High-order QAM improves spectral efficiency at the cost of a larger dynamic range. This leads to a larger peak-to-average power ratio (PAPR), reducing energy efficiency in traditional PA's. Therefore, the average or back-off efficiency is just as important as the peak efficiency in modern modulation techniques. Based on this, the objective of this thesis is to implement a TX with an innovative deep PBO enhancement technique improving the PBO efficiency by extending the efficiency peaking beyond 6 dB PBO. To achieve this goal, a new concept was conceived by combining two already proven architectures, a single supply class-G SCPA [13] and a recursive house-of-cards SCPA [14]. A detailed explanation of the concept was provided, and the implementation was, step by step, introduced and discussed. Finally, the proposed Doherty-like Class-G HoC PA was measured. Unfortunately, the PA could only partially be measured due to a catastrophic layout issue, where one of the PA cores was connected 180° out of phase. While simulation results show promising performance, the measured results, however, were discouraging. This work measured a maximum output power of 22.1 dBm with efficiency peaks of 20.9 %, 10.0 %, and 7.8 % for respectively 0 dB, -6 dB, and -12 dB power back-off. The expected simulation results demonstrates respectively 42.3 %, 30.9 % and 27.3 %.

The promising numbers of post layout-simulation encourage us for a future retape-out to not only fix the balun connection mistake but also further improve

the performance. The three transistor stack output short switches significantly reduce the efficiency for the $-12\,\mathrm{dB}$ and $-6\,\mathrm{dB}$ power back-off. Moreover, the control of these switches relies on two additional supply voltages. Future investigation should address these shortcomings by possibly replacing the output-short switch with a thick oxide transistor simplifying the control and potentially decreasing the R_{ON} resistance of the output-short switch. Giving the opportunity to reduce the transistor size, therefore lowering capacitive loading in the $0\,\mathrm{dB}$ and $-6\,\mathrm{dB}$ power back-off modes.

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