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High Efficiency UV Photodiodes on p-type Substrate

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Electronic Instrumentation Laboratory

Outline

1. Introduction
    - UV Domains and Challenges
    - Prior Art: pure-B on n-type Si
    - Why p-type UV Photodiodes?
2. p-type UV Photodiode
    - Process Development
    - Layout
3. Results
    - Dark Leakage Current
    - Sensitivity
    - Stability
4. Summary & Conclusion

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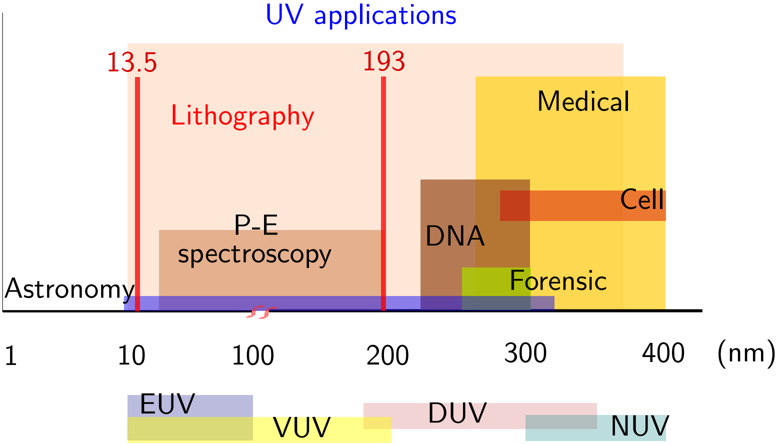
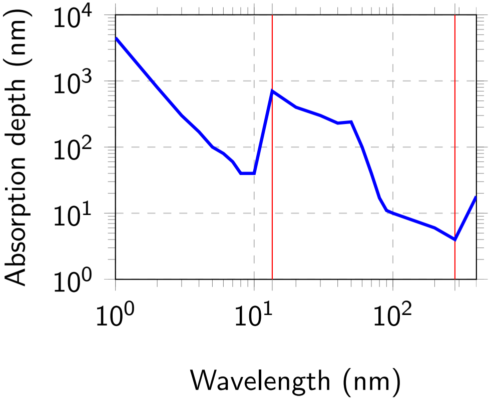
Introduction - UV Domains & Challenges (1/3)



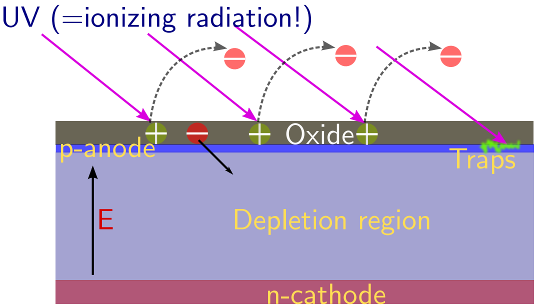
- Application spans a wide range of domains (EUV to NUV)
- A broad-band detector simplifies system design & economical

Introduction - UV Domains & Challenges (2/3)



- Silicon based detector preferred due to CMOS compatibility
- Very shallow absorption depth (a few nm) in DUV/VUV

Introduction - UV Domains & Challenges (3/3)



- UV radiation charges oxide with positive charge, and introduces additional interface traps
- This phenomenon affects spectral stability and can increase dark leakage current via surface electric field modification

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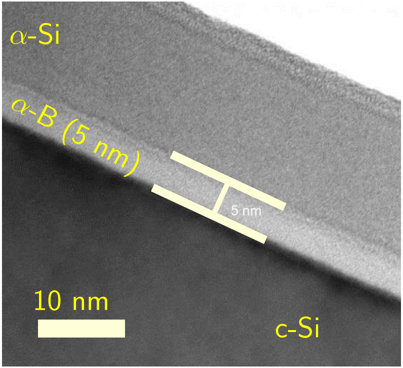
Introduction - Prior Art: pure-B on n-type Si (1/2)

- Oxide free n-type silicon surface exposed to B_2H_6, using commercial Si/SiGe epitaxial AP/LPCVD reactor at DIMES (TUDelft), at 500 °C – 700 °C
- Creates a thin (few nm) of pure-B on Si surface, and a few nm of in-diffusion into Si:
  - acts as a passivation layer for surface interface traps
  - creates a electric field for enhanced photo-charge collection
  - acts as a capping (semi-metal) layer and improves stability
- Excellent results obtained:
  - excellent responsivity in DUV (> 0.1 A/W)
  - excellent responsivity close to theoretical maximum in EUV
  - excellent stability

Introduction - Prior Art: pure-B on n-type Si (2/2)



- HRTEM image of the cross-section of a pure-B diode showing the different regions (α-Si layer deposited for contrast)

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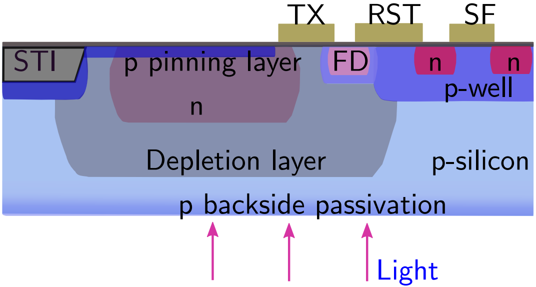
Introduction - Why p-type UV Photodiodes? (1/1)



- Standard CMOS foundry compatibility ⇒ mass production
- Representative of CMOS Image Sensor (CIS) Pixels
  - in particular backside-illumination (BSI)
  - large area diode can be implemented as a test-device to characterize performance
  - lends itself as photo diodes in CMOS pixels

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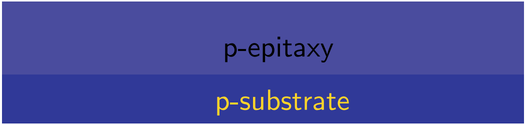
p-type - Process Development (1/11)

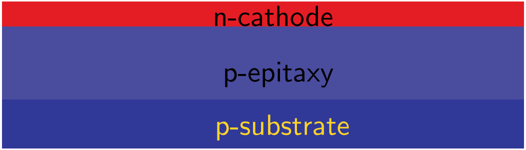
- Highly doped p-substrate starting material ($\approx$ 800 μm, 1×10^{19} at/cm^3)

p-type - Process Development (2/11)



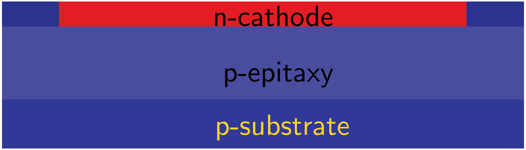
- p-epitaxy(2.5 μm, 1×10^{17} at/cm^3) is grown on the substrate to create a high-quality material for further processing

p-type - Process Development (3/11)



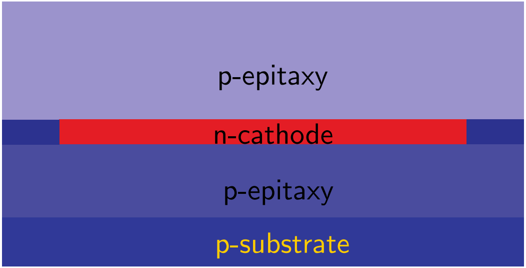
- Buried n-cathode(1 μm, 1×10^{16} at/cm^3) is grown on the p-epi. The depletion should not interact with the low-quality substrate

p-type - Process Development (4/11)



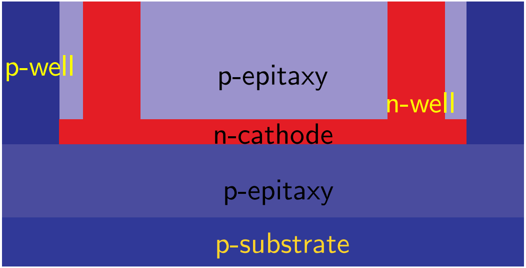
- p-type boron sidewall cutting implants ensure no p-n junctions are formed at the edges. The deep p-implant mask is reused

p-type - Process Development (5/11)



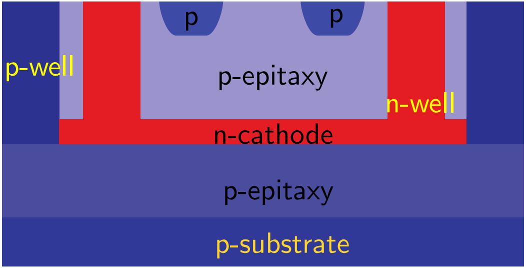
- High resisitivity p-epitaxy (1.5 μm, $\approx 1 \times 10^{14}$ at/cm^3) is grown on the n-cathode. This is fully-depleted at operational voltage

p-type - Process Development (6/11)



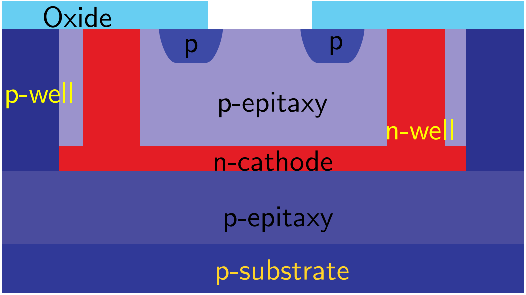
- Deep p-and n-well (implant energy = 500 keV) are used to connect to the p-type layer and the n-buried cathode respectively

p-type - Process Development (7/11)



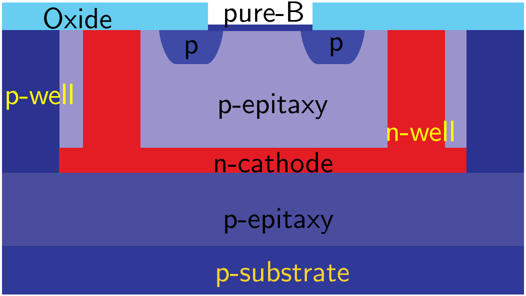
- p^+ anode contact implant is made. At this stage, 30 min anneal at 950 °C is done to activate the implants

p-type - Process Development (8/11)



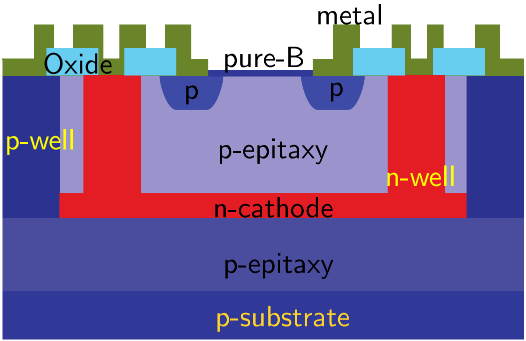
- 375 nm oxide (TEOS) is formed by LPCVD, and patterned to define pure-boron region

p-type - Process Development (9/11)



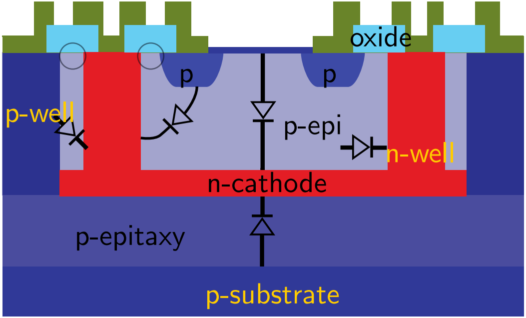
- 3 nm pure-B is formed by CVD. The oxide serves as a mask for the pure-B deposition as boron does not form on oxide

p-type - Process Development (10/11)



- Finally, contact regions are defined, and metal contacts made on the implants to form cathode and anode/ground contacts

p-type - Process Development (11/11)



- Parasitic diode leakage currents (n-well – p-epi, n-well – p-well, n-well – p-anode) & surface leakage ⇒ perimeter component

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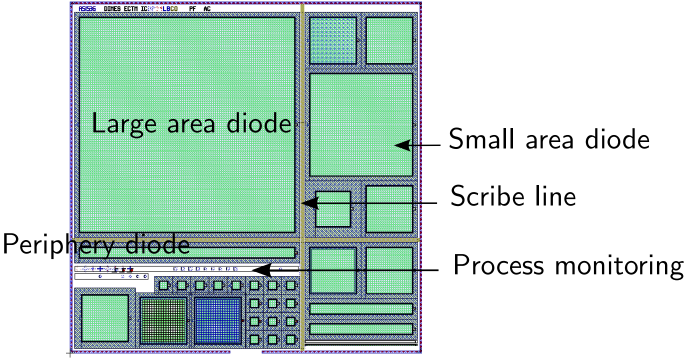
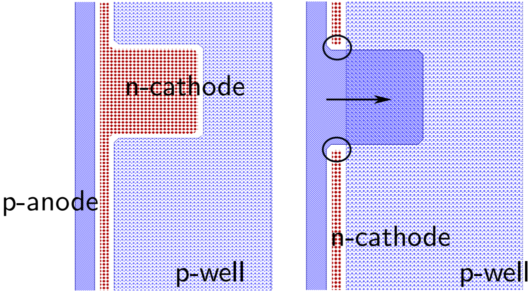
p-type - Layout(1/2)



- Top-cell layout view. The large area diode (10 mm × 10 mm), small area diodes (half and quarter size), periphery diode, process monitoring, and some additional test-diodes can be seen

p-type - Layout (2/2)



- Left: the highly doped regions are separated by 6 μm
- Right: the n-cathode ring is cut to allow the p-anode implant to physically connect with the p-well

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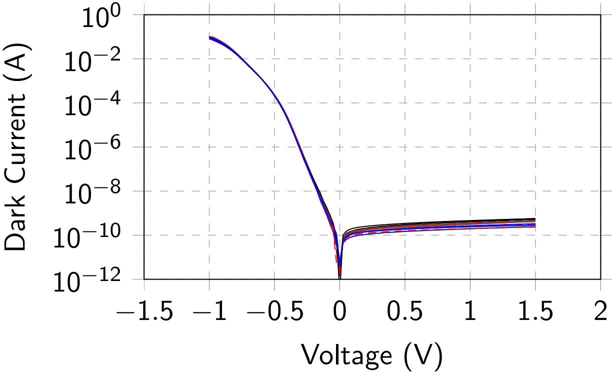
Results - Dark Leakage Current (1/1)



- Dark current is 260 pA at 0.5 V reverse bias (RT)
- Contribution from periphery < 5 % $\Rightarrow$ 25 μm^2 diode: 70 aA

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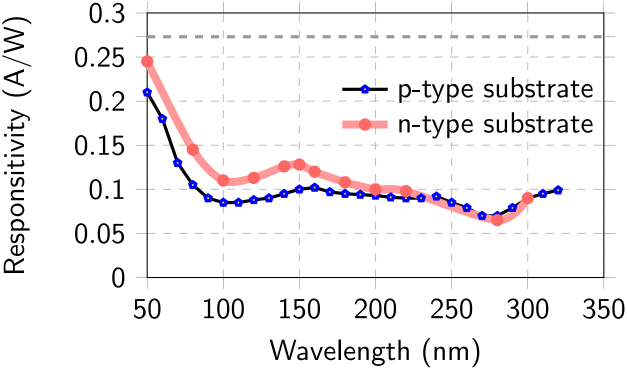
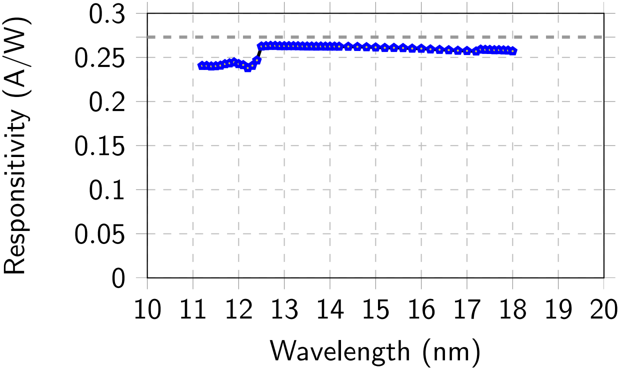
Results - Sensitivity (1/2)



- Good responsivity in entire DUV; minimum at 280 nm: 0.07 A/W
- Quantum efficiency (280 nm) = 26 %

Results - Sensitivity (2/2)



- Good responsivity in entire EUV; close to theoretical maximum at 13.5 nm

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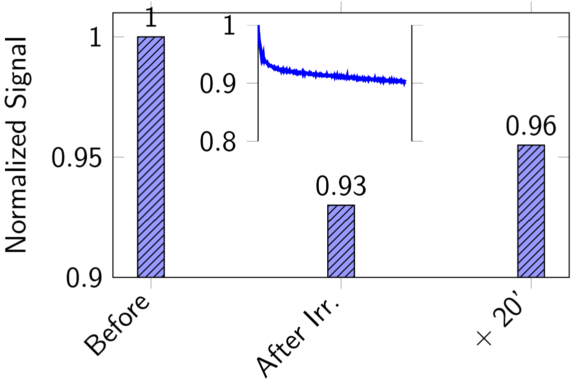
Results - Stability (1/1)



- Responsivity degradation due to irradiation at 121 nm (179 nW, 40 min), and subsequent recovery. Inset: logarithmic behaviour of the signal as a function of irradiation time (t= 0 to 2400 s)

Summary & Conclusion

- Pure-B technology has been successfully ported into p-type substrate:
  - the pure-B diodes show extremely good broadband sensitivity in the EUV and DUV wavelengths
  - the pure-B diodes exhibit very good stability under harsh conditions
- **Conclusion: The technology that has been developed can be used as a post-processing step for the passivation of photo-detectors, including BSI image sensors (both CMOS and CCD) in the whole UV range**