# Fabrication of bifacial poly-Si solar cells with copper-plating metallization

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# Fabrication of bifacial poly-Si solar cells with copper-plating metallization

by

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# Abstract

Carrier-selective passivating contacts (CSPC) have been proven to be effective in suppressing recombination losses at metal-silicon interface in high-efficiency crystalline silicon solar cells. The poly-Si-based CSPCs consisting of $SiO_X$/poly-Si stacks are used in this thesis due to their compatibility with high thermal budgets. CSPCs with thin poly-Si layers are preferred since thicker poly-Si layers induce significant parasitic absorption at device level. The bifacial solar cell design could provide a higher energy yield than monofacial solar cells and largely reduce the consumption of metals such as silver, indium due to the contribution of reflected light. The objective of this thesis is to fabricate double-side textured copper (Cu)-plated bifacial poly-Si solar cells. It is achieved by developing thin poly-Si contacts, addressing the TCO sputtering-induced passivation damage, and optimizing the Cu-plating processes.

Firstly, the passivation of the poly-Si symmetric samples and solar cells was optimized. 16 nm-thick $n^+$ poly-Si and 16 nm-thick $p^+$ poly-Si symmetric samples with intrinsic layer grown through PECVD demonstrated good passivation quality indicated by their $iV_{OC}$ of 713 mV and 665 mV respectively. To further improve the passivation quality of the $p^+$ poly-Si, the layer thickness and the doping gas flow ratios were varied. Best passivation was achieved for a solar cell precursor with 42 nm-thick $p^+$ poly-Si layers. The optimum doping gas flow ratio was found to be $SiH_4$-$B_2H_6$=20/15 sccm. The highest $iV_{OC}$ achieved was 692 mV.

TCO sputtering caused a severe passivation drop of ~90 mV in solar cell precursors. Post-deposition annealing treatments and 2-step TCO sputtering techniques were used to reduce such a passivation loss. However, it was challenging to reproducibly obtain solar cell precursors with good passivation quality before metallization step. The initial solar cell with double side TCO use showed cell parameters were: $V_{OC}$ 398 mV, *FF* 56.22%, $J_{SC}$ 30.55 mA/cm$^2$ and $\eta$ 6.85% (from *n*-side illumination).

To maintain a good passivation quality of the solar cell precursor, an 8 nm-thick $MoO_X$ buffer layer was introduced on top of the $p^+$ poly-Si layer. This approach effectively reduced the passivation drop from 91 mV to 12 mV. However, the $MoO_X$ layer was observed to strongly react with the solution which was used for silver seed layer removal in Cu-plating metallization procedure. Different approaches were tested to obtain a well-plated $p^+$ poly-Si side. As for the $n^+$ poly-Si side, a TCO-free design was deployed. To ensure a good adhesion of the plated Cu fingers, a Ti/Ag (8 nm/192 nm) seed layer was employed before Cu-plating step. Moreover, an additional $SiO_X$ layer, which acts as the anti-reflection coating, was deposited on the *n*-side of a complete solar cell. With these adjustments, the solar cell performance was improved to: $V_{OC}$ 610 mV, *FF* 64.98%, $J_{SC}$ 36.95 mA/cm$^2$ and $\eta$ 14.64% (from *n*-side illumination).

Furthermore, with reducing the Ti thickness in the metal seed layer to 2 nm. The solar cell performance was further improved to $V_{OC}$ 611 mV, *FF* 69.58%, $J_{SC}$ 36.16 mA/cm$^2$ and $\eta$ 15.38% (from *n*-side illumination). The bifaciality factor is 89%.

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# Nomenclature

| | |
|---|---|
| µm | Micrometre |
| A | Ampere |
| Ag | Silver |
| ALD | Atomic Layer Deposition |
| $AlO_X$ | Aluminium oxide |
| Ar | Argon |
| ARC | Anti-reflection coating |
| a-Si | Amorphous silicon |
| a-Si:H | Hydrogenated Amorphous Silicon |
| $B_2H_6$ | Diborane |
| BHF | Buffered Oxide Etch |
| $cm^2$ | Square centimetre |
| c-Si | Crystalline Silicon |
| CSPC | Carrier Selective Passivating Contacts |
| Cu | Copper |
| DI | Deionized |
| $E_C$ | The highest energy of the conduction band |
| ECV | Electro-chemical capacitance-voltage |
| $E_G$ | Bandgap energy |
| $E_{ph}$ | Photon energy |
| *eV* | Electron volt |
| $E_V$ | The lowest energy of the valence band |
| fA | Femto-ampere |
| FBC | Front Back Contact |
| *FF* | Fill factor |
| FGA | Forming Gas Annealing |
| FZ | Float zone |

| | |
|---|---|
| $H_2$ | Hydrogen |
| $H_2O$ | Water |
| $H_2O_2$ | Hydrogen Peroxide |
| HF | Hydrofluoric Acid |
| $HNO_3$ | Nitric Acid |
| i-a-Si:H | Intrinsic hydrogenated amorphous silicon |
| ITO | Indium Tin Oxide |
| $iV_{OC}$ | Implied open circuit voltage |
| $J_0$ | Recombination current density |
| $J_{SC}$ | Short circuit current density |
| LPCVD | Low-Pressure Chemical Vapour Deposition |
| mA | Milli-ampere |
| $MoO_X$ | Molybdenum oxide |
| ms | Milli-second |
| mV | Milli-volt |
| $N_2$ | Nitrogen |
| NAOS | Nitric Acid Oxidation of Silicon |
| $NH_3$ | Ammonia |
| $NH_4OH$ | Ammonium hydroxide |
| nm | Nanometre |
| Pa | Pascal |
| PDA | Post-deposition annealing |
| PECVD | Plasma Enhanced Chemical Vapour Deposition |
| $PH_3$ | Phosphine |
| POLO | Poly-silicon on Oxide |
| Poly-Si | Poly-crystalline Silicon |
| PR | Photoresist |
| PV | Photovoltaic |
| rpm | Rotations per minute |
| RTP | Rapid Thermal Processing |
| sccm | Standard cubic centimetre per minute |

| | |
|---|---|
| SE | Spectroscopic Ellipsometry |
| SEM | Scanning Electron Microscope |
| SHJ | Silicon Heterojunction |
| Si | Silicon |
| $SiH_4$ | Silane |
| $SiN_X$ | Silicon Nitride |
| $SiO_2$ | Silicon dioxide |
| $SiO_X$ | Silicon Oxide/Tunnel Oxide layer |
| SLM | Standard litre per minute |
| SRH | Shockley-Read-Hall |
| TCO | Transparent Conductive Oxide |
| Ti | Titanium |
| TMA | Trimethylaluminium |
| TMAH | Trimethyl ammonium hydroxide |
| TOPCON | Tunnel Oxide Passivating Contact |
| TOPCoRE | Tunnel Oxide Passivating Contact Rear Emitter |
| V | Voltage |
| $V_{OC}$ | Open circuit voltage |
| $\eta$ | Photoconversion efficiency |
| $\rho_c$ | Contact resistivity |
| $\tau_{eff}$ | Minority carrier lifetime |

# 1 Introduction

The major challenge faced by the current generation is the ever-growing energy demand due to the rapid increase in consumption. This is a result of the rise in the global population. US Energy Information Agency (EIA) predicts that the world energy consumption would have a 50% increase by the year 2050 [1]. The currently used fossil fuels for energy production are being constantly depleted and also negatively impact the environment [2]. Almost a billion people are living without access to electricity [3],[4],[5]. This generation of humankind is on the cusp of an energy crisis if the same situation prevails longer. A major shift from the usage of conventional fuel sources to renewable energy sources for energy production is needed.

There has been a 56% increase in renewable energy use over the past two decades. The generation of energy through renewables contributes approximately 25% of the total energy generation. It is driven mainly by hydroelectric energy, wind energy and increasingly solar PV. The share of solar PV contributes to almost one-third of the growth of renewables in the last three years[5],[6],[7].

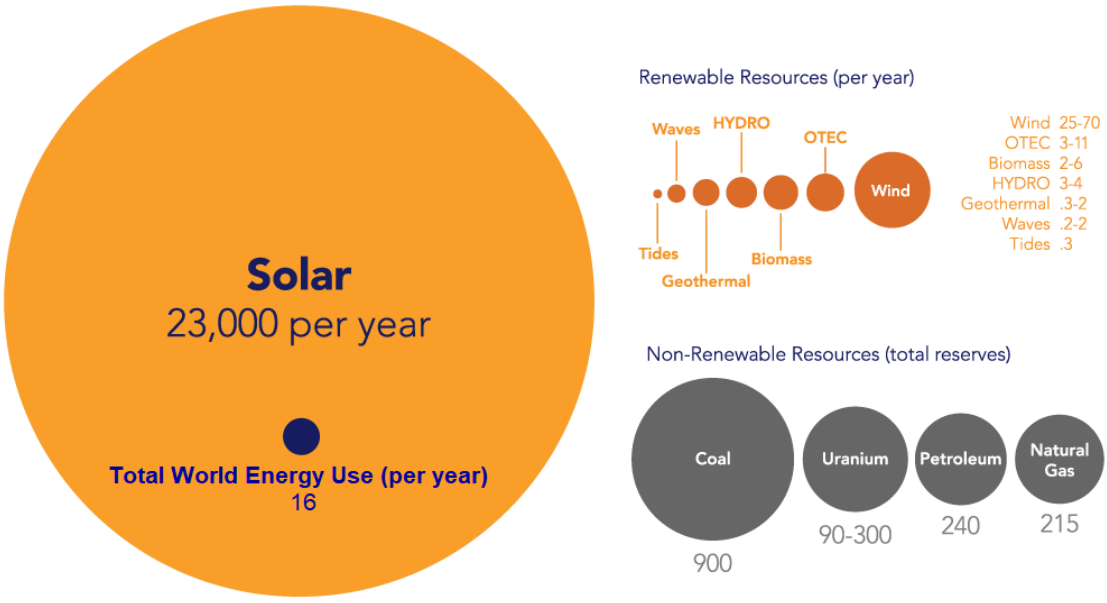


**Figure 1.1** Comparison of conventional and renewable energy reserves available in Terra Watts [7]

Sun is an abundant source of energy. Hence, the solar PV is capable of producing 10000 times more energy than the current global energy demand [8]. Investing in this energy source is the ideal solution to fulfill the ever-growing global energy demand and also leave a positive impact on the environment.

The current trends in solar PV production show that silicon-based PV production is the dominant technology, especially mono-crystalline silicon. As seen from **Figure *1.2***, crystalline silicon has the largest share of almost 95% of the total production [9]. The advantages of this technology are the abundant availability of silicon on the earth's crust and its low cost. Silicon is non-toxic compared to other solar PV technologies like Cadmium Telluride (CdTe) technology [10].

Silicon has a bandgap of 1.12 *eV* at a light absorption cut-off wavelength of 1107 nm [11]. This is an optimal bandgap for solar energy conversion to electrical energy. Mono-crystalline silicon yields higher efficiency than multi-crystalline silicon technology (mono-crystalline 26.7% and multi-crystalline 22.3% [12]). But mono-crystalline silicon requires a more expensive process for industrial

production [13]. Hence, multi-crystalline silicon is preferred over mono-crystalline silicon for mass production due to its lower cost [14].

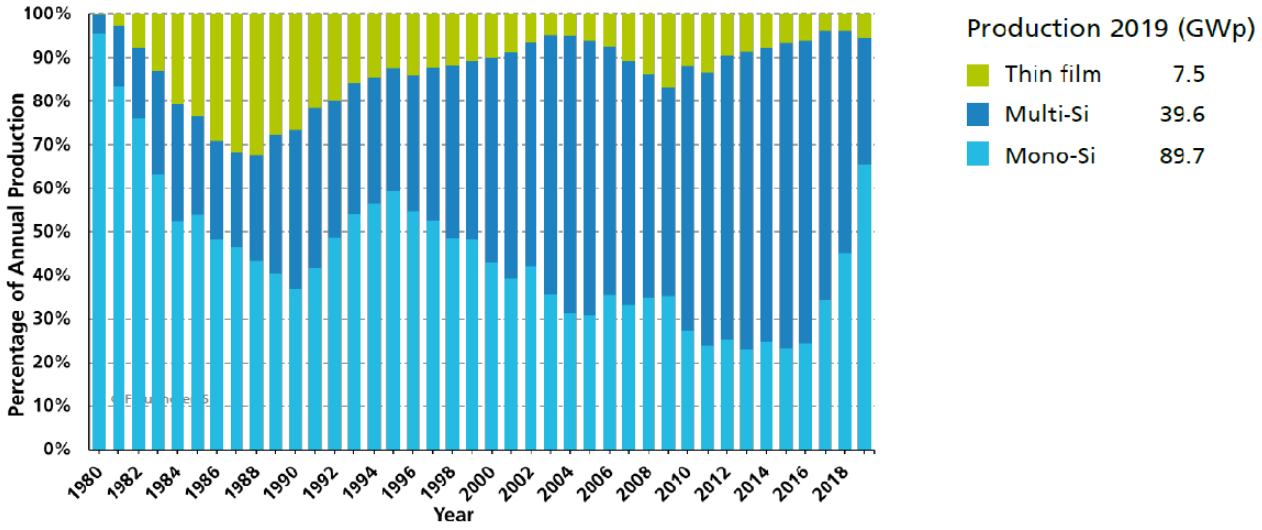


**Figure 1.2** PV production by technology- Percentage of global annual production [9]

## 1.1 Solar Cell working principle and loss mechanisms

A solar cell is a device that converts incident sunlight into electrical energy. The fundamental working principle of a solar cell is the photovoltaic effect. This photovoltaic effect creates a potential difference at the junction of two different materials as a response to the incident radiation. When connected to an external circuit, it can be used to supply power to the connected loads. The primary processes involved in the working of a solar cell are Generation, Separation and Collection of the charge carriers.

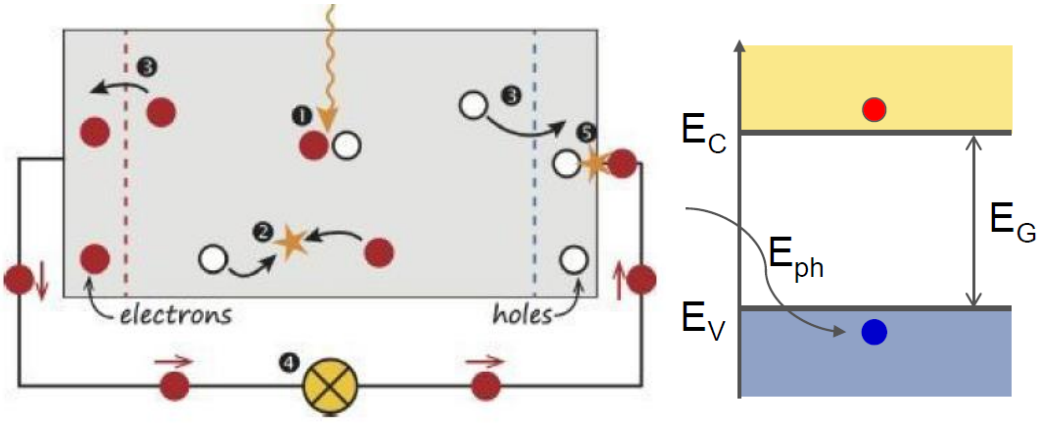


**Figure 1.3** Left: Schematic representation of the steps in the photovoltaic process [16] Right: Band diagram showing generation of the charge carriers hole (blue) and electrons (red) [16]

**Figure *1.3*** shows a basic model of a solar cell. (1) Absorption of the incident light leads to the generation of electron-hole pairs. (2) Generally, the electrons and holes recombine. The energy of the electron-hole pairs is released as heat or transferred to other charge carriers when they recombine [16]. (3) To make use of the energy in the electron-hole pairs, the electrons and holes are separated. It is done using p-type and n-type doped semi-permeable membranes. (4) The separated electrons are collected through the external circuit after performing work. (5) After the electrons have passed through the external circuit, they recombine with the holes at the absorber/metal interface.

Recombination of the charged carriers after absorption is to be avoided for the proper functioning of the solar cell [17].

Generation of charge carriers occurs when the incident photon of a specific energy $E_{ph}$ is absorbed on the semiconductor material. As a result, an electron is excited from the valence band to the conduction band, leaving behind a hole in the valence band. Thus, electron-hole pairs are created within the material. The difference between the valence band energy $E_V$ and the conduction band energy $E_C$ of the material is known as the bandgap $E_G$. In principle, photons with higher energy than the bandgap of the absorber material generates electron-hole pairs [16].

The next step is the separation of the generated charge carriers to prevent them from recombination. This is done by Boron and Phosphorous doped silicon layers to construct an electric field. It separates the holes on the Boron doped side (p-type) and the electrons on the Phosphorous doped side (n-type).

Collection of charge carriers occurs at the electrical contacts of the semiconductor device. The electrons travel through the external circuit for the energy to be used for supplying the load. After it has passed through the circuit, the electron recombines with the hole.

### Loss mechanisms

The spectral mismatch is one of the prominent optical loss mechanisms found in solar cells. Other forms of optical losses that occur in the solar cell are parasitic absorption, reflection, and shading losses.

**Thermalization and Non-absorption:** Photons with energy higher than the material band gap can produce an electron-hole pair. The excess energy of the photons will be lost and released as heat in the semiconductor material. This is known as Thermalization. On the other hand, the absorption for photons with energy lower than the semiconductor band gap will not be possible. This is called non-absorption. Due to this unsuccessful absorption, these photons do not produce electron-hole pairs and will pass through the semiconductor.

**Reflection losses:** The incident photons can be reflected before reaching the absorber layer. These losses can be minimized by introducing an anti-reflection coating layer or by using a transparent conducting oxide layer. To achieve better light absorption in the cell, surface texturing is carried out.

**Parasitic absorption:** The semiconductor material will absorb photons with energy equal to the semiconductor material band gap energy. There are possibilities that these photons can be absorbed in the anti-reflection coating layers and transparent conducting oxide layers which do not contribute to charge carrier generation. The absorption of photons in layers other than the absorber is called parasitic absorption.

**Shading losses:** These losses are mainly due to the metal fingers at the solar cell front side. It blocks the incident light on the surface reducing the short circuit current. Therefore, the dimensions of the metal contacts should be optimized for reducing the shading losses.

### Recombination

The recombination of the electrons and holes after being collected results in the reduction of the collected charge carriers thus affecting the solar cell performance. This is detrimental to the performance of high-efficiency solar cells because it significantly lowers the carrier transport and the carrier lifetime [15]. The recombination can be divided into bulk recombination and surface

recombination. Bulk recombination can be categorized into Radiative recombination, Auger recombination and Shockley-Read-Hall (SRH) recombination.

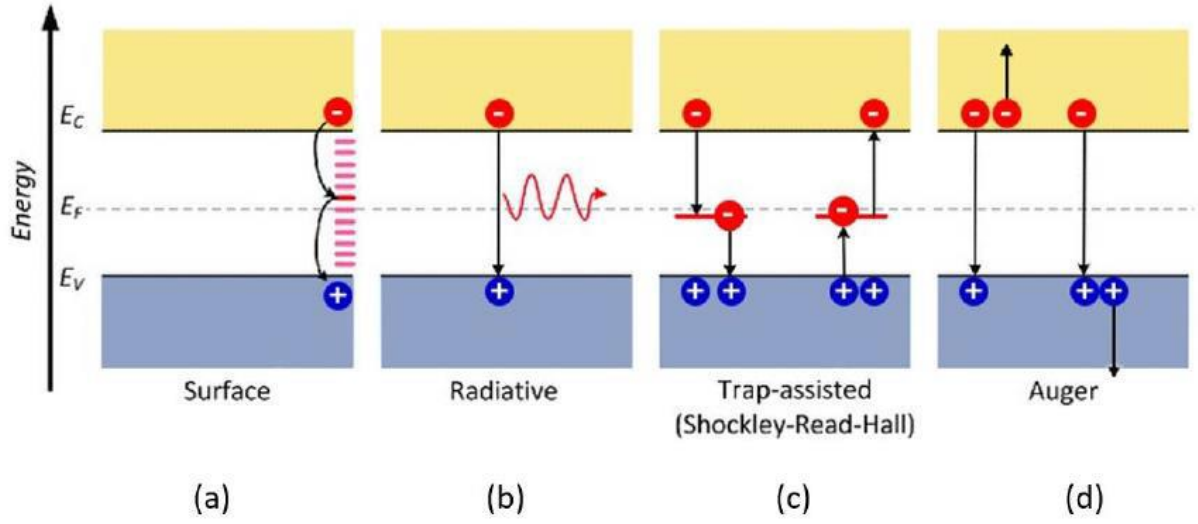


**Figure 1.4** Schematic representation of different recombination mechanisms [16]

Radiative recombination is the opposite of photon absorption. The excited photon is dropped back to the original energy state. The energy emitted is equal to the energy of the bandgap of the material. This recombination mechanism is prevalent in the direct bandgap materials and does not play a role in crystalline silicon materials.

In Shockley-Read-Hall recombination, the electron-hole recombination does not take place directly between bandgaps but at an intermediate energy level called trap state. It is induced by the impurity atoms or lattice defects [16]. This recombination is dominant in semiconductors at most operational conditions but it is less likely than radiative recombination.

Auger recombination is a recombination mechanism that involves three particles. It is prevalent in indirect bandgap semiconductors whose energy and momentum are not matched. The excess energy is transferred to the third particle(hole/electron). This third particle is excited to deeper levels of the valence/ conduction band. It relaxes back to the semiconductor edge by transferring its energy in the form of heat.

Surface recombination occurs mainly due to the dangling bonds on the semiconductor surface. They act as recombination centres and induce trap states. These dangling bonds capture the charge carriers which increases the SRH recombination rate. Surface recombination can be minimized in two ways. By reducing the number of dangling bonds, the probability of electron-hole recombination is reduced. The other way is to increase the doping concentration at the surface. This creates a barrier that prevents minority charge carriers from being transmitted to the material surface.

### Surface Passivation

The surface recombination can be reduced by two methods: Chemical passivation (suppressing surface defects) and Field effect passivation (reduction of surface carrier concentration by an induced electric field).

Chemical passivation is done by introducing ultra-thin layers of silicon oxide ($SiO_X$), hydrogenated amorphous silicon (a-Si:H) films and hydrogenated amorphous silicon nitride (a-$SiN_X$:H). By growing

these thin layers, the dangling bonds at the c-Si surface can be saturated due to the formation of Si-O or Si-H bonds. Generally, these layers are deposited by Chemical Vapour Deposition methods. Precursor gases are introduced to react with the c-Si substrate to form thin layers which passivate the surface defects. Nitric acid can also be used to grow $SiO_X$ films on the substrate and it is known as wet chemical passivation. The silicon nitride layer is a hydrogen-rich material used to saturate the dangling bonds and it also acts as an anti-reflection coating material [18].

Field-effect passivation is achieved by reducing the concentration of one type of carrier by introducing a highly doped layer of the other. The electric field repels the minority carrier from the highly doped region. This highly doped region can be formed by ion implantation or chemical vapour deposition. Applying a dielectric layer with high charges can induce an internal electric field and this carrier selectivity is also one type of field-effect passivation[15].

## 1.2 poly-Si based Carrier Selective Passivating contacts

In a solar cell, the charge carriers are generated due to the photon incident on the surface. They are collected at the metal electrodes separately through carrier selectivity. In a conventional solar cell structure with an aluminium back surface field, the recombination at the metal-semiconductor junction is the major cause of loss in efficiency. It is due to the high interface defect density [19]. To reduce these recombination losses, passivating contacts also known as Carrier Selective Passivated Contacts have been introduced. They are characterized by their high-quality passivation with low contact resistance. Solar cells with these passivating contacts have reduced recombination losses at the metal-silicon interface because of the passivation layer in between them.

The passivating contacts mainly use the silicon oxide ($SiO_X$), hydrogenated amorphous silicon (a-Si:H) films as the thin passivation layer. Passivating contacts based on the a-Si are referred to as silicon heterojunction (SHJ) or heterojunction with thin intrinsic layer (HIT) solar cells. A schematic representation of a double-side textured front-back contacted (FBC) heterojunction solar cell is shown in **Figure *1.5***. Recently, a record efficiency of 26.3% was attained in a heterojunction solar cell with FBC structure [20]. But, the heterojunction solar cells have limitations in the process temperature used for manufacture [19].

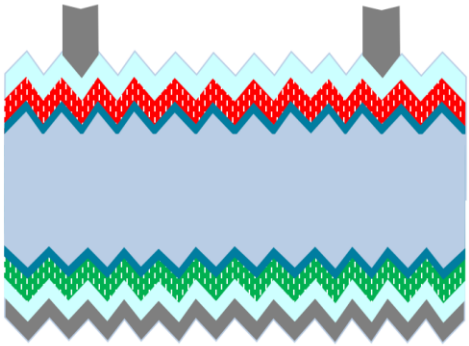

**Figure 1.5** Schematic representation of a front-back contacted Silicon heterojunction solar cell [21]

In contrast, poly-Si/$SiO_X$ contacts exhibit good compatibility with processes involving high thermal budgets. They are also compatible with mainstream PV processing technology [22]. These poly-Si/$SiO_X$ stacks are commonly known as Tunnel Oxide Passivating Contacts (TOPCON) or poly-silicon on oxide (POLO) contacts. The silicon oxide interfacial layer helps in the majority carrier transport through tunnelling as shown in the left of **Figure *1.6***. This tunnel oxide thickness is generally below 1.5nm. If it is too thin, the passivation quality is low and if it is too thick, majority carrier transport is hindered [23].

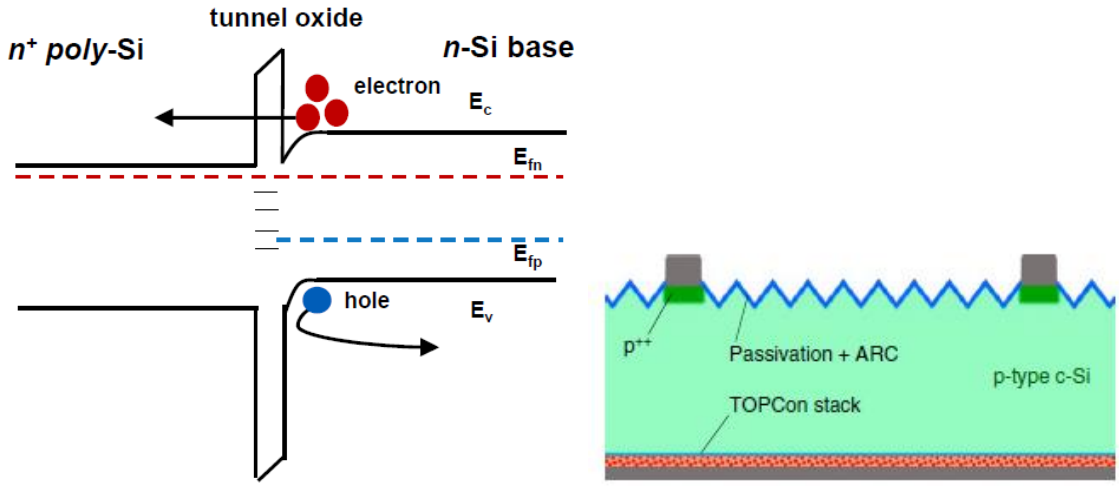


**Figure 1.6** Schematic representation of the band diagram TOPCon [24] and schematic representation of TOPCon rear emitter structure-based solar cell [25]

An ideal passivating contact must combine the functions of a passivation layer and a contact. It must minimize the charge carrier recombination within the surface and contact structure. It should also help in charge extraction from the semiconductor. The quality of a passivating contact in a solar cell is characterized by very low carrier recombination current density $J_0$ and the contact resistivity $\rho_c$ [26][27]. To obtain excellent surface passivation, high-temperature annealing in a $N_2$ atmosphere at 800-900°C followed by a hydrogenation step is usually required. This enhanced surface passivation is also attributed to the combined effects of chemical passivation by tunnel oxide and field-effect passivation by doped poly-Si [28][29]–[32]

Until now, the highest efficiency achieved in a lab-scale back-junction (BJ) solar cell using TOPCon is 26% as shown in **Figure *1.7***. It was achieved for a TOPCon Rear Emitter (TOPCoRE) structure with $Al_2O_3$ passivation at the front surface. Highly doped $p^{++}$ regions were present underneath the front metal contacts [25] as shown in the right of **Figure *1.6***.

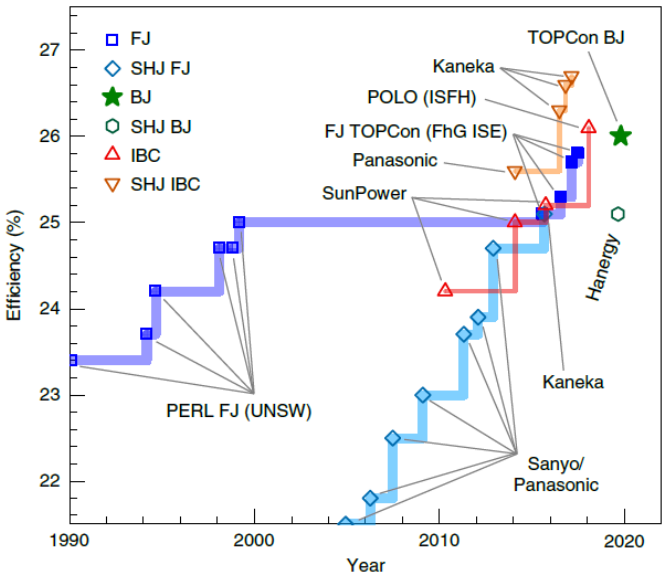


**Figure 1.7** Evolution of efficiencies for different cell architectures [25]

## 1.3 Copper-plated bifacial poly-Silicon solar cells

With common monofacial PV modules, only the light illuminated on the front side of the module can be converted into electrical energy. Bifacial technology also utilizes the reflected light. It gives a higher energy yield with the same area occupied as the monofacial modules. In the absence of rear aluminium metallization, the infrared absorption is reduced. Due to this, the working temperature of the solar cell is reduced. This also results in obtaining a better power output from the solar cell [33].

Some of the advantages of bifacial solar cells over monofacial solar cells are increased power density, increase in maximum power output, reduced area-related costs and decrease in cell working temperature [33].

The bifacial technology replaces the full area rear metal contact with grid metallization [33]. According to the International Technology Roadmap for Photovoltaics (ITRPV), the worldwide share of the bifacial c-Si modules will be significantly close to 80 % by 2031 [34]. This result is a consequence of the higher energy yield [35] and reduced metal consumption [36].

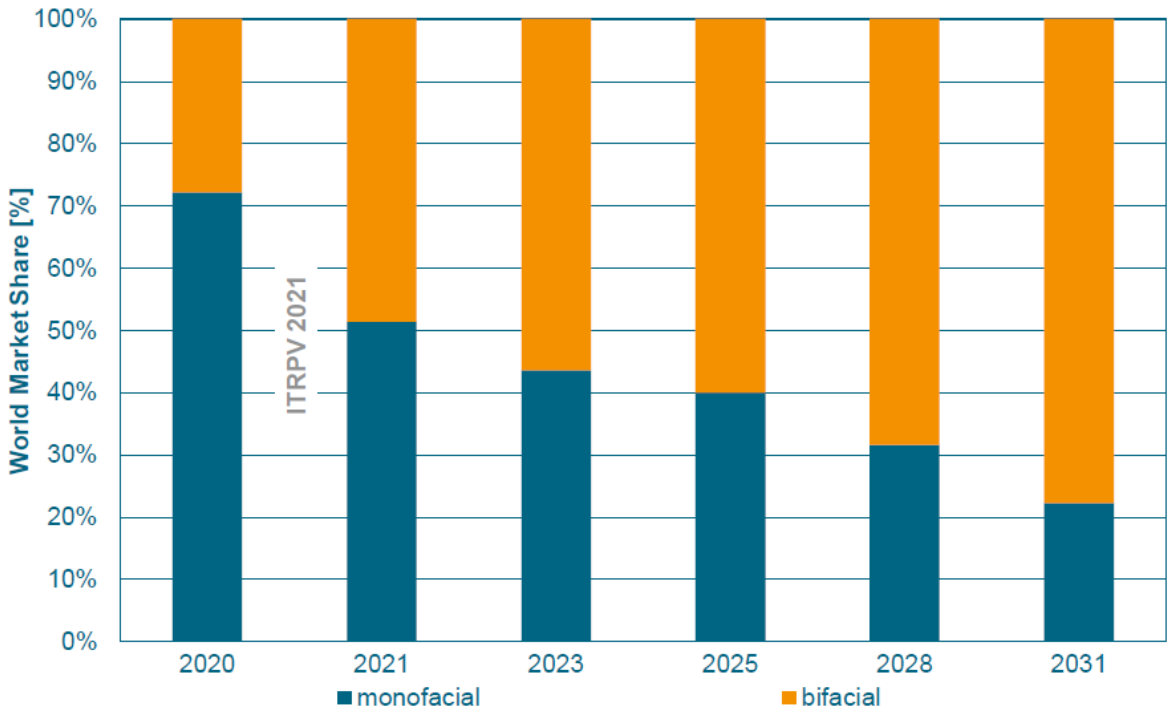


**Figure 1.8** Market share of bifacial c-Si solar cell technology predicted by ITRPV [34]

Poly-Si material suffers from high free carrier absorption. Thicker poly-Si induce parasitic absorption at device level which affects the light trapping and decreases the short circuit density [37]. Hence, it is essential to decrease the thickness of the poly-Si layers to lessen the losses in the generation of current [38]. The latest developments indicate that the parasitic absorption induced by thicker poly-Si layers can be suppressed by reducing the layer thickness to 10-40 nm range[15],[39].

Thus, thin poly-Si passivating contacts are applied in the double-side textured bifacial structure in this thesis. The $SiO_X$ tunnel oxide layer is grown through the wet chemical oxidation method of NAOS (Nitric Acid Oxidation of Silicon) in this thesis.

The metallization to form metal contacts in solar cells is mostly done by screen printing using silver (Ag) paste in the PV industry. The raw material that is used for this metallization is silver, because of

its high conductivity. The downside however is that the silver is also quite expensive. To improve the efficiency, there needs to be a reduction in the Ag consumption and the costs involved. Hence, alternative methods to silver screen printing need to be considered in c-Si solar cells.

Silver screen printing severely affects the performance of thin poly-Si layers. The penetration of Ag paste into poly-Si etches part of the doping into the poly-Si layer. This lowers the field-effect passivation [40]. If the poly-Si layer is very thin, then the Ag paste might completely etch it. This introduces high contact recombination [40]. Screen printing of silver paste also results in a lower aspect ratio.

One of these possible solutions is using copper-plating. Copper is almost as conductive as silver and is also relatively cheaper. The fine grid metallization does not affect the passivation and has a high aspect ratio. The copper-plating process does not require the curing step as required in the screen-printing [41]. By switching to copper-plating, the consumption of silver is suppressed and the process can be performed at room-temperature [42].

According to ITRPV, c-Si solar cells with copper-plated contacts will have 30 % of the market share within 2027 [43]. This increase is due to a potential higher aspect ratio than screen-printed silver contacts. Therefore, a higher short-circuit density due to less optical shading is also achieved [40]. The solar cells with copper-plated contacts have comparable contact resistivity to screen-printed silver contacts [40].

## 1.4 Thesis Objectives

The objective of this thesis project is to fabricate double-side textured copper-plated bifacial poly-Si solar cells. Emphasis is mainly on developing double-side textured solar cell precursors with high passivation quality. The tunnel oxide layer is grown through wet chemical oxidation process. The fabrication process consists of a number of processes which include optimization of the poly-Si carrier selective passivating contacts, annealing conditions, hydrogenation techniques. The complete solar cell to be fabricated is an amalgamation of these processes.

The main research objectives of this thesis are as follows:

- Develop an ultra-thin poly-Si passivating contact by optimizing intrinsic layer deposition, high-temperature annealing condition, doped layer thickness, and doping gas flow ratio.
  Identify the suitable hydrogenation approach for fabricating the solar cell precursor.
- Address the TCO sputtering-induced passivation damage using different passivation recovery techniques.
- Fabricate a double side textured copper-plated bifacial poly-Si solar cell by optimizing the copper-plating processes.

## 1.5 Thesis Outline

This thesis report consists of 5 chapters. The benefits of using solar energy and the current trends in the manufacture of solar cells are discussed in the introduction chapter. The working principle of a solar cell and the loss mechanisms are presented. Next, the motivation behind using poly-Si passivating contacts in the bifacial solar cell architecture is explained. It is followed by the research objectives of this thesis project.

Chapter 2 discusses the fabrication processes of the symmetric samples and the solar cell precursors. It is followed by the various process equipment and characterization techniques used in this thesis.

Chapter 3 will discuss the optimization of the passivation quality of poly-Si symmetric samples and solar cell precursors. Firstly, the optimization of the intrinsic and doped layers is discussed. To further improve the passivation quality in the $p^+$ poly symmetric samples, the layer thickness and the doping gas flow ratios of $SiH_4/B_2H_6$ are varied. A comparison of different hydrogenation approaches to enhance the passivation quality is also explained in this chapter.

In Chapter 4, the fabrication of a double-side textured copper-plated bifacial poly-Si solar cell is discussed. The effects of the passivation damage due to the TCO sputtering and the methods used to recover the passivation loss are presented. The modifications made on the solar cell for improving the performance are also explained in this chapter.

Finally, the report is concluded with a summary of the results found and recommendations for future work in chapter 5.

# 2 Experimental methods

This chapter deals with the fabrication process and the characterization techniques used in this thesis. First, the steps involved in the fabrication process of symmetric samples and solar cell precursors are presented in *Section 2.1*. The process equipment used for the fabrication is discussed in *Section 2.2*. Finally, the characterization techniques used for the analysis of the fabricated samples are discussed in *Section 2.3*.

## 2.1 Fabrication process flow

The various manufacturing processes involved in the fabrication of the symmetric samples and solar cells are presented in this section. The fabrication of the symmetric samples is important in analyzing the passivation quality.

### 2.1.1 Fabrication process flow of symmetric samples

A pictorial flow-chart of the fabrication process of the textured $n^+$ poly-Si symmetric and $p^+$ poly-Si symmetric samples can be seen in **Figure 2.1** and **Figure 2.2** respectively. The fabrication of the $p^+$ poly-Si samples is similar to the $n^+$ poly-Si samples. The only change is the type of the doped layers. Phosphorous doped a-Si:H for n-type and Boron doped a-Si:H for p-type.

- The *n*-type float zone (FZ) c-Si double side polished wafers with a thickness of 280 µm and <100> orientation are used in this thesis. The texturing is performed by immersing the double side polished wafers in an alkaline solution bath. The solution contains tetramethyl ammonium hydroxide (TMAH) and water in the ratio of 1:4, with 120 ml of an additive solution ALKA-TEX. The temperature of the bath is maintained at 80 °C for 15 minutes. The result obtained is wafers with small pyramids.
- Post the texturing process, the wafers are cleaned using Deionized water (DI water) and dried using a spin dryer. The edges of the small rough pyramids formed on the wafers during the texturing process are smoothened by performing poly-Si etch for 2 minutes.
- After the poly-Si etching, the wafers are made to undergo a round of standard cleaning and drying. This is done to remove the organic and inorganic contaminants. Following the standard cleaning, the native oxide layer is removed by the Marangoni cleaning and drying process. This is followed by the chemical oxide growth.
- The tunnel oxide layer, silicon oxide ($SiO_X$) is grown through a wet chemical oxidation process called NAOS (Nitric Acid Oxidation of Silicon). A 1.5 nm-thick silicon oxide layer is grown by immersing the wafers in 69.5% $HNO_3$ solution for 60 minutes.
- The intrinsic hydrogenated amorphous silicon ((i)- a-Si:H) layer is deposited on the substrate using PECVD. The different deposition techniques that were tried for the intrinsic layer growth will be discussed in the next chapter.
- The doped a-Si:H layers are deposited using PECVD, following the intrinsic layer deposition. The doping gases used are $B_2H_6$ for *p*-type a-Si:H and $PH_3$ for *n*-type a-Si:H. The pressure and temperature were maintained at 1 mbar and 180 °C during the deposition. The deposition parameters can be seen in **Table *2.2***.
- After the PECVD process, the substrates are made to undergo a high-temperature annealing process. This is done to crystallize the amorphous silicon and activate the dopants. This results in the formation of poly-silicon layers. The substrates are annealed at 850 °C for 15 minutes in a $N_2$ atmosphere.

- The effusion of hydrogen from the c-Si/$SiO_X$ interface during the high-temperature annealing process is mitigated by the hydrogenation step. It also enhances the passivation quality. The hydrogenation step consists of the deposition of hydrogen-rich $SiN_X$ layers using PECVD. It is followed by forming gas annealing (FGA) step. This helps in the diffusion of hydrogen into the c-Si bulk to passivate the defects.
  In this thesis, a $SiN_X$ layer of 75 nm thickness is deposited on both sides of the textured wafers at 400 °C. This is followed by the FGA at 400 °C for 30 minutes. FGA takes place in an atmosphere containing a mixture of 10 % $H_2$ and $N_2$.
- Following the hydrogenation, the $SiN_X$ layer is etched using BHF (Buffered Oxide Etch) and 0.55 % HF solution before TCO layer deposition. The TCO layer used in this thesis is Indium doped Tin Oxide (ITO). It is a mixture of 90 % Indium Oxide ($In_2O_3$) and 10 % Tin Oxide ($SnO_2$). An ITO layer of 75 nm thickness is deposited on the symmetric samples using the sputtering process with an optimized recipe.
  This ITO layer deposition on the symmetric samples is to get an estimation of the passivation loss that will be observed. This will be helpful when fabricating solar cell precursors.
- The implied $V_{OC}$ ($iV_{OC}$) of the samples is measured using the Sinton WC-120 lifetime measurement equipment. Measurements are made at each step starting from the high-temperature annealing. This provides an estimation of the passivation quality of the samples prepared.

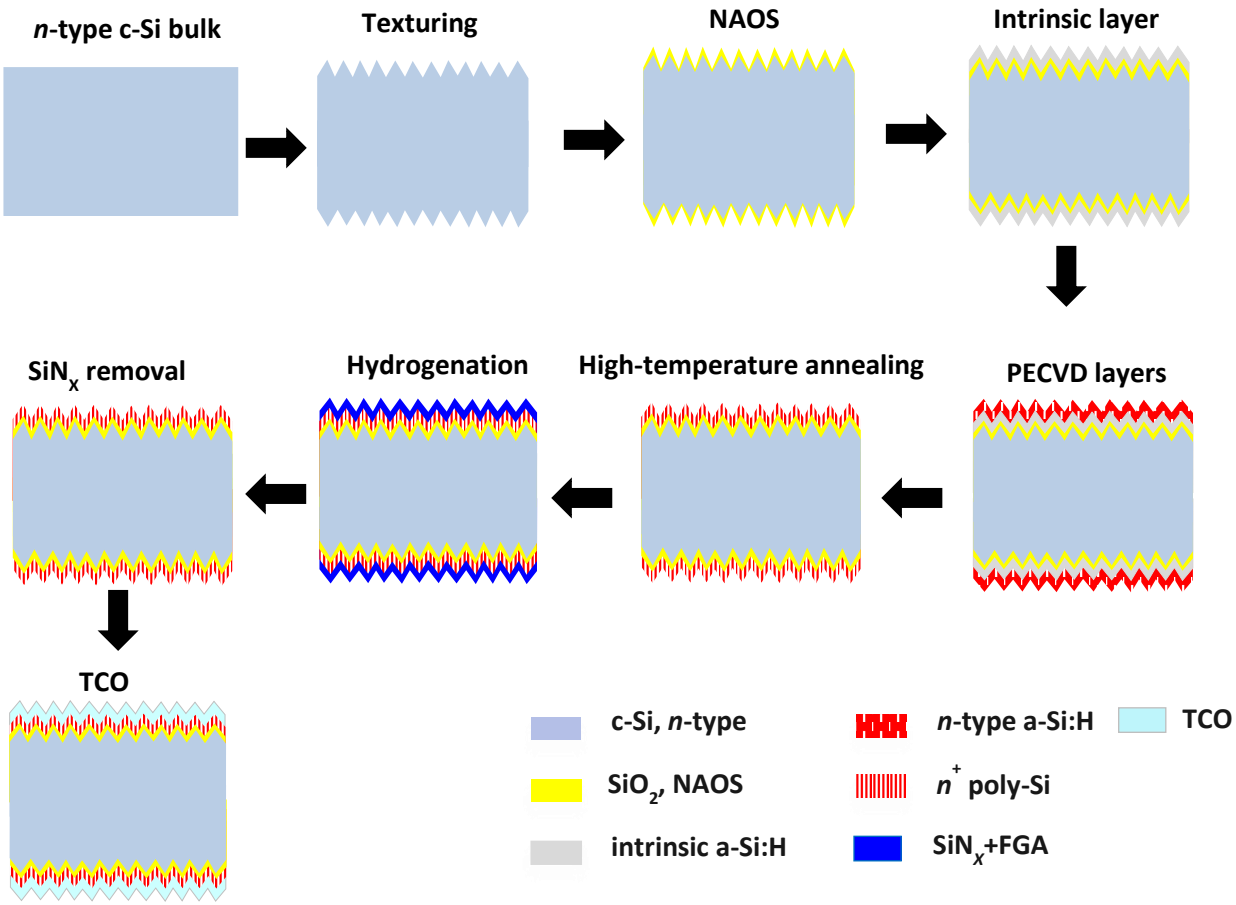


**Figure 2.1** Schematic representation of the fabrication of $n^+$poly-Si symmetric samples

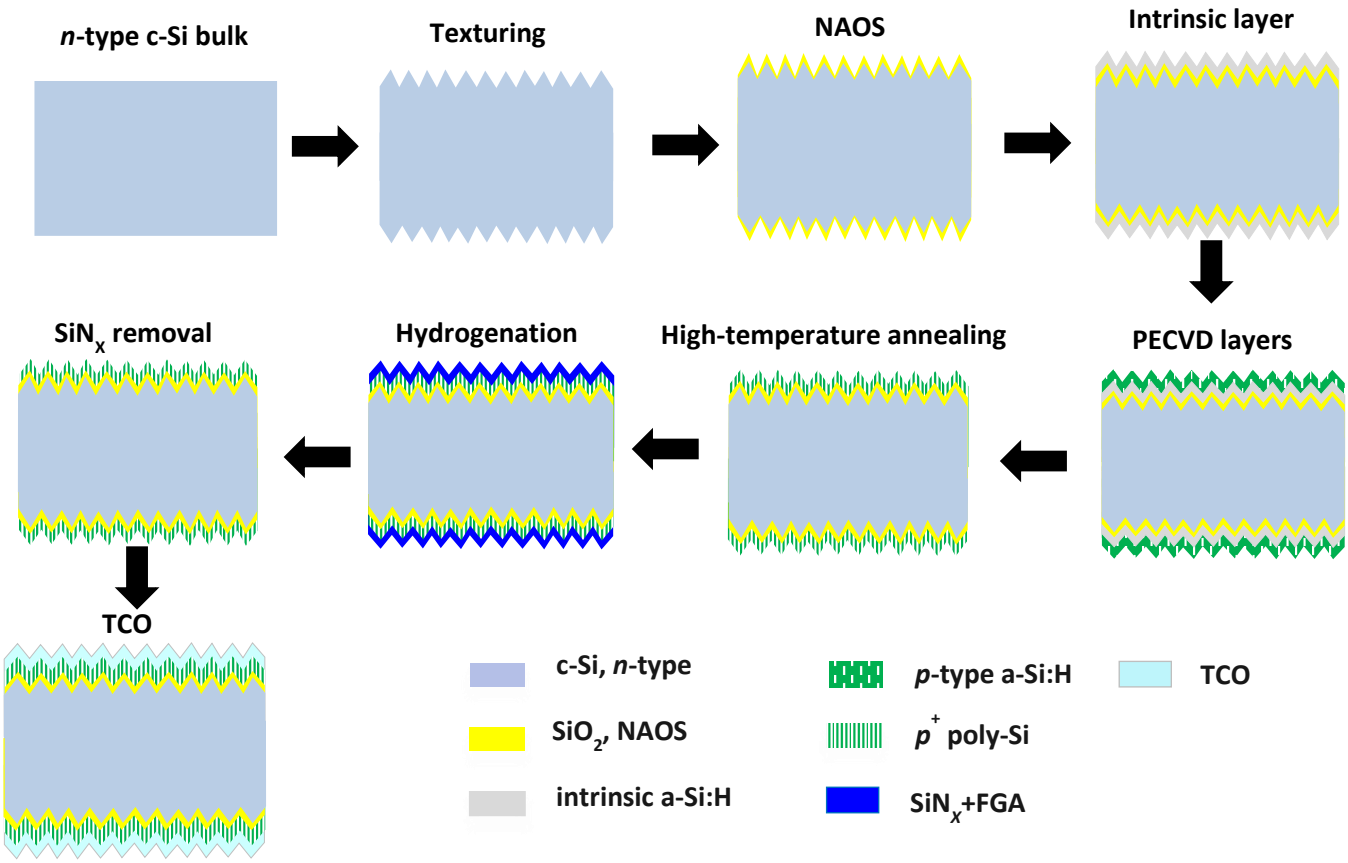


**Figure 2.2** Schematic representation of the fabrication process of $p^+$poly-Si symmetric samples

### 2.1.2 Fabrication process flow of solar cell

After the desired passivation quality is achieved on the *n*-type doped and *p*-type doped symmetric textured samples, they are incorporated in the fabrication of the solar cell. A pictorial representation of the solar cell fabrication process flow is shown in **Figure 2.3**. The sequential steps involved in the fabrication process are as followed:

- Double side polished *n*-type FZ c-Si wafers with thickness 280 µm and <100> orientation are used as the bulk.
- These polished wafers are immersed in a solution bath containing a 1:4 ratio of TMAH and water with 120 ml of an additive ALKA-TEX solution. The temperature of the bath is maintained at 80 °C for 15 minutes to obtain double-side textured wafers. After the texturing process, the wafers are cleaned in DI water and dried using a spin dryer.
- Then, poly-Si etch is performed on the wafers for 2 minutes to smoothen the rough pyramid edges. Following the etching, a standard cleaning and drying process is done on the wafers to remove any organic and inorganic contaminants. After the standard cleaning, the native oxide layer is removed using Marangoni cleaning and drying.
- The silicon oxide layer is grown through the wet chemical oxidation method of NAOS. A 1.5 nm- thick silicon oxide layer is grown by immersing the wafers in 69.5 % $HNO_3$ solution for 60 minutes.
- Intrinsic hydrogenated amorphous silicon ((i)a-Si:H) layer is deposited using PECVD. Following the intrinsic layer deposition, the *n*-type and *p*-type doped a-Si:H layers are deposited. The front side is deposited with Phosphorous doped a-Si:H and the rear side is deposited with Boron doped a-Si:H. The doping gases used are $B_2H_6$ for *p*-type a-Si:H and $PH_3$ for *n*-type a-

Si:H. The pressure and temperature were maintained at 1 mbar and 180 °C during the deposition. The deposition parameters can be seen in **Table *2.2***.

- Post the PECVD process, a high-temperature annealing step is performed at 850 °C for 15 minutes in a $N_2$ atmosphere. This is done to activate the dopants and crystallize the doped a-Si layers into doped poly-Si layers.
- Hydrogenation is the next step in the fabrication of solar cell precursors. $SiN_X$/FGA is the preferred hydrogenation approach in this thesis. 75 nm-thick hydrogen-rich $SiN_X$ layer is deposited on both sides of the substrate using PECVD at 400 °C. This is followed by FGA at 400 °C for 30 minutes. FGA is done in an atmosphere containing a mixture of 10 % $H_2$ and $N_2$.
- Post hydrogenation, the $SiN_X$ layer is etched using the BHF (Buffered Oxide Etch) and 0.55 % HF solution before the ITO layer deposition. 75 nm-thick ITO layer is sputtered on both sides of the cell precursor using an optimized recipe.
- For the copper-plating metallization, a Silver (Ag) seed layer is needed to be deposited before further processing can take place. This Ag seed layer is essential for photolithography. During copper-plating, this seed layer helps in preventing the diffusion of copper into the silicon surface. Thus, a full area Ag seed layer of 200 nm thickness is deposited on the textured samples using the metal evaporation technique.
- In the photolithography process, an organic photo-sensitive material called photoresist (PR) is uniformly coated on the Ag seed layer-deposited samples using a spin-coater. AZ 3027 was the photoresist used in this thesis. An optimized recipe of AZ 3027 ECI 4 µm is used in this thesis.

  12 µm-thick PR layers were coated on each side of the substrate in three rounds of coating. After each round of the coating, the substrates were baked in the oven at 100 °C for 2 minutes, 3 minutes and 5 minutes respectively. This is done to harden the PR layers before exposure.
- The photoresist coated wafers are then exposed to ultra-violet light with a 6-die mask using the contact aligner equipment. A split-exposure approach is used in this thesis. The wafers are exposed through the 6-die mask for 120 seconds. It is split into 40 seconds for each exposure. After the exposure, the wafers are developed for 2 minutes and rinsed with DI water. The developer solution used in this thesis is the MF 322 developer. The exposed PR layer is etched away after development. The wafers are dried and checked under a microscope for the pattern openings.
- The next step in the fabrication process is the copper-plating metallization for forming the metal contacts. An in-built copper-plating equipment is used in this thesis. The wafer is loaded vertically in a bifacial wafer holder with copper plates on both sides. More details on the copper-plating process can be found in *Section 2.2.13*.
- After the copper-plating is performed, the photoresist and metal seed layer need to be removed before measuring the solar cell parameters. This is done by immersing the wafer in acetone to remove the photoresist and then rinsing it with DI water. After that, the wafer is immersed in an aqueous solution of 200 ml DI water, 50 ml of 31 % hydrogen peroxide ($H_2O_2$) and 12.5 ml of 28 % ammonium hydroxide ($NH_4OH$) for the seed layer removal.
- The copper-plated solar cells are rinsed using DI water and dried. The parameters of the fabricated solar cells are measured using the illuminated J-V measurement setup.

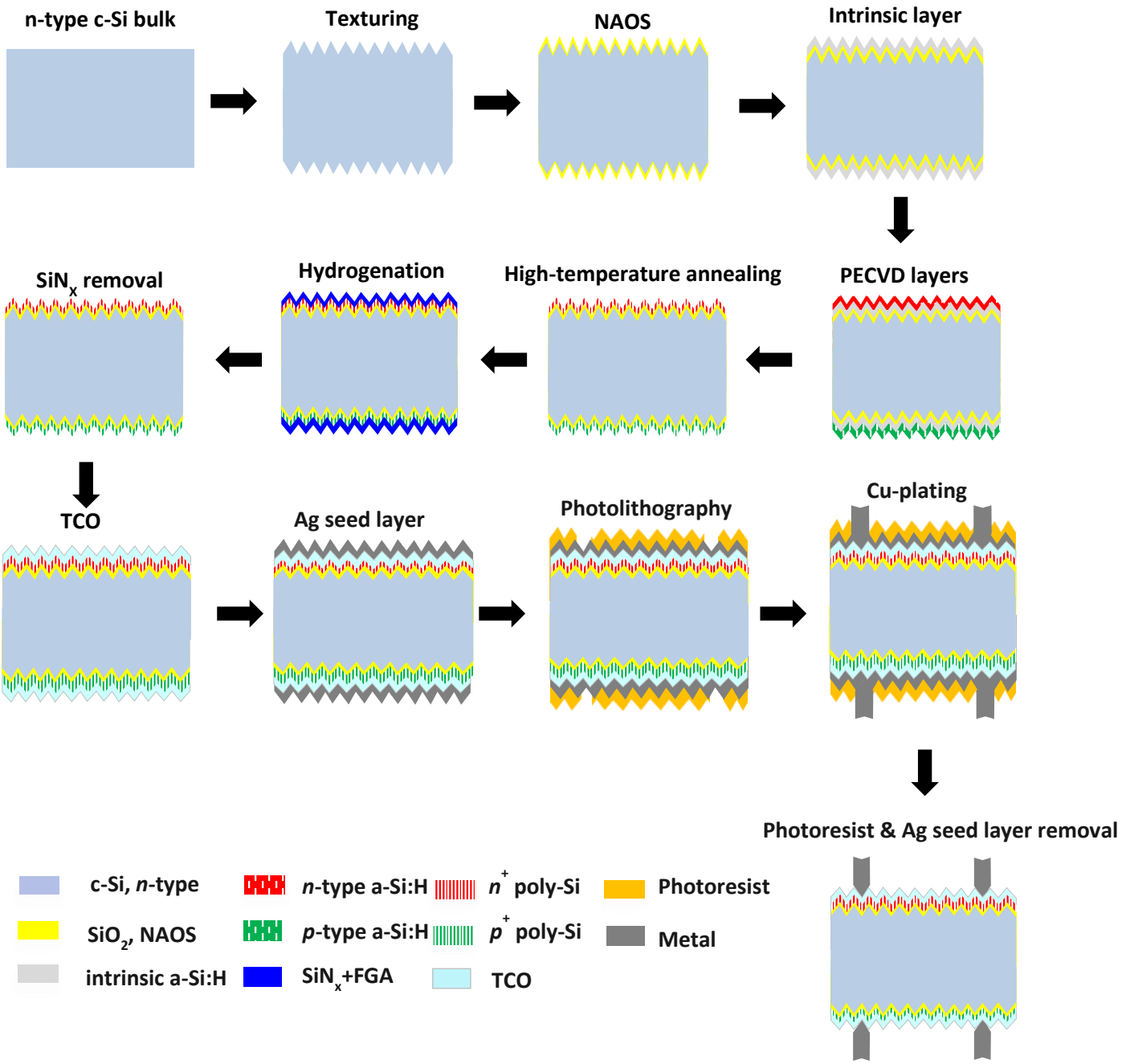


**Figure 2.3** Schematic representation of the fabrication of double side textured copper-plated bifacial poly-Si solar cell

## 2.2 Process equipment

The various processes mentioned in the fabrication process flow are discussed in this section. The process followed from wafer texturing to the metallization step is listed out.

### 2.2.1 Silicon wafer material

The wafers used in the thesis were *n*-type crystalline silicon float zone wafers manufactured by *TOP-SIL*. They were chosen because they are less prone to light-induced degradation effects and show better minority carrier lifetime compared to p-type wafers [44]. The properties of the wafers are shown in **Table 2.1**.

**Table 2.1 :** c-Si wafer parameters

| Parameter | Specification |
|---|---|
| Dopant | *n*-type (Phosphorous doped) |
| Orientation | <100> +/- 1° |
| Diameter | 99.7-100.3 mm |
| Thickness | 260-300 µm (280 µm) |
| Finish | Double side polished |
| Resistivity | 1-5 Ω cm |
| Method | Float zone |

### 2.2.2 Wafer texturing

The texturing process helps in improving the light absorption capacity of the silicon wafers. This is accomplished by etching the wafers in an alkaline solution. There are two orientations of the crystal lattice in the c-Si: <100>(flat) and <111>(textured). The alkaline solution bath contains a mixture of tetramethylammonium hydroxide (TMAH) and water in the ratio of 1:4 with an additional 120 ml solution of ALKA-TEX. The temperature of the bath is maintained at 80 °C for 15 minutes. The solution is constantly kept in circulation at 300 rpm. With this process, the <100> flat oriented wafers are etched to form wafers of <111> orientation with small pyramids. This process is carried out until there is no reflection from the wafer surface. It indicates that the flat wafer has been textured. After the texturing, the wafers are rinsed using DI water and dried.

### 2.2.3 Standard cleaning

The native oxide formed on the wafer surface is etched by immersing the wafers in a 0.55% HF bath for 4 minutes. The sharp tips of the pyramids formed might act as defect states. These textured peaks are smoothened by performing poly-Si etch for 2 minutes. The poly-Si etch solution bath contains a mixture of $HNO_3$ and 40% HF. The wafers are rinsed using DI water and dried before the standard cleaning is performed.

The standard wafer cleaning process is performed to remove any contamination on the wafer surface. First, the wafers are immersed in 99 % $HNO_3$ solution for 10 minutes. This is followed by rinsing them in a bath of deionized water (DI water) for 10 minutes. Then, the wafers are immersed in a bath of 69.5 % $HNO_3$ maintained at 110 °C. After this, the wafers are again rinsed in DI water bath for another 10 minutes. Finally, the wafers are thoroughly rinsed and dried in the Spin Rinse Dryer for 10 minutes. This is the sequence followed in the standard cleaning of the wafers.

### 2.2.4 Removal of native oxide

Even though the wafers are kept in the cleanroom atmosphere, a layer of native oxide is formed on the surface of the wafers after standard cleaning. This native oxide layer is removed by immersing the wafers in 0.55 % HF solution for 4 minutes until the wafer surface is hydrophobic. This hydrophobic nature indicates that the native oxide layer has been removed. Subsequently, the wafers are rinsed with DI water for 4 minutes and an additional 1 minute with isopropyl alcohol for drying the wafers. It is important that this native oxide layer is removed before any further processing on the wafers.

### 2.2.5 Chemical Silicon Oxide growth

The next step in the fabrication is the growth of silicon oxide via wet chemical oxidation. The objective of this step is to achieve an ultra-thin $SiO_X$ layer of thickness 1.5 nm [45][46]. The approach used to grow the silicon oxide layer is called Nitric Acid Oxidation of Silicon (NAOS). The wafers are immersed in a 69.5 % $HNO_3$ solution for 60 minutes at room temperature for developing the ultra-thin $SiO_X$ layer [46]. After that, the wafers are rinsed in DI water for 5 minutes and dried using a single wafer dryer.

The benefits of the wet chemical oxidation approach are that it is done at room temperature and has a uniform thickness [47][48]. It is one of the major advantages since the other thermal oxidation processes require a temperature of 600-700 °C [49]. The insertion of this ultra-thin tunnel oxide layer between the c-Si bulk and the doped poly-Si layer reduces the interface recombination significantly. It prevents epitaxial layer regrowth of as-deposited amorphous-Si layers during the subsequent high-temperature annealing process [50][51]. It also minimizes the dopant diffusion into the c-Si bulk during the high-temperature annealing process. This results in enhanced passivation due to higher band bending at the interface [50].

### 2.2.6 Low-Pressure Chemical Vapour Deposition

Low-Pressure Chemical Vapor Deposition (LPCVD) is one of the methods to deposit amorphous silicon-based layers. Thickness ranging from a few nanometres to micrometres can be deposited using this method. The LPCVD tube furnace manufactured by *Tempress* systems is used in this thesis project. This deposition method was used to deposit intrinsic amorphous silicon layer ((i)-a-Si:H) on the wafer using an optimized recipe.

Before loading in the furnace, the wafers must be dipped in 0.55 % HF solution to avoid the native oxide layer growth. The gas used in the optimized recipe is Silane ($SiH_4$). The gas flow rate is maintained at 45 sccm during the deposition. The temperature and pressure of the system during the deposition are maintained at 580 °C and 20 Pa respectively. The deposition rate of the (i)-a-Si:H layer is around 2nm/min. After the deposition, the recipe includes a post-annealing step at 600 °C for 60 minutes. This post-annealing is to remove any stress developed on the deposited layer.

### 2.2.7 Plasma Enhanced Chemical Vapour Deposition

The other method of deposition of a-Si:H layer is performed using the Plasma Enhanced Chemical Vapour Deposition method. It is one of the most used deposition methods for a vast range of materials in the research of solar cells. Generally, temperatures around 600 °C are required for the breaking up of the precursor gases before the layer deposition. But, the working temperature range of PECVD is around 200-400 °C. This is because of the presence of the plasma. The plasma provides energetic free electrons and ions that can break the chemical bonds of the gases [52].

In PECVD processes, deposition is possible because of the reactant gases being introduced between the parallel electrodes. The plasma is ignited by applying a highly energetic field across the electrodes

on either side of the chamber. The layers formed from PECVD are usually of high quality, possess good layer uniformity and desirable thickness [21]. Hence, PECVD is one of the favoured deposition techniques in the industrial manufacturing of solar cells. The deposition thickness for the textured substrate is reduced by a factor of 1.73 from the estimated thickness on a flat substrate.

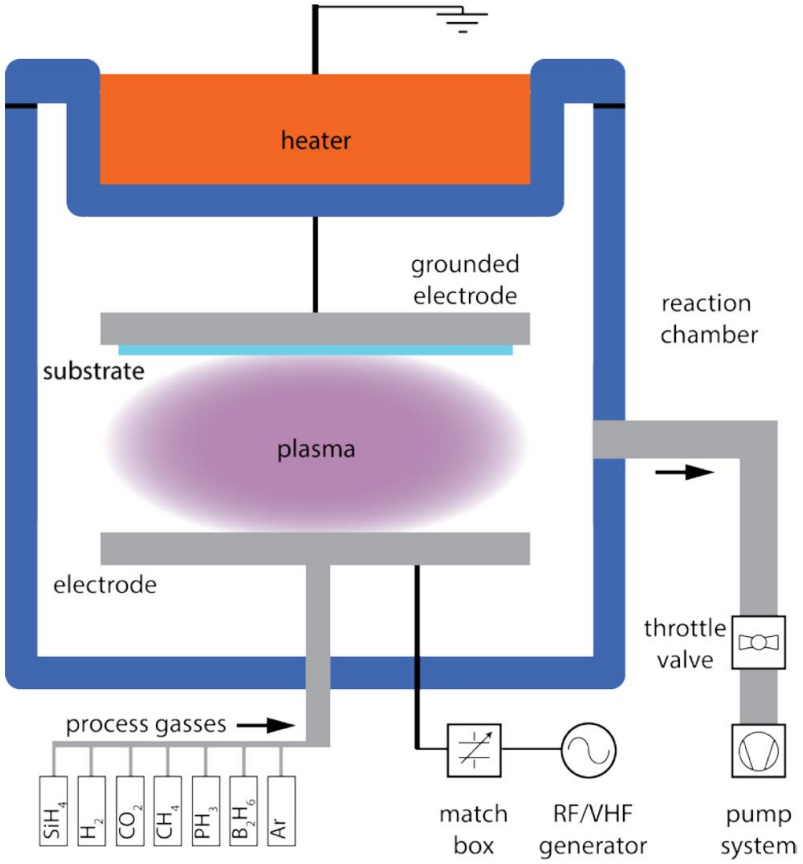


**Figure 2.4** Schematic representation of PECVD and its system components [52]

Two different PECVD machines are used in this thesis project. First, AMOR manufactured by *Elettrorava* is used for the deposition of the intrinsic a-Si:H layer and doped a-Si:H layers on the wafer surface. It consists of 4 dedicated chambers for the deposition of the doped layers. This is to avoid any possible cross-contamination during the deposition. An additional chamber for flipping the wafer is also present so that the deposition can be done on both sides of the substrates.

The recipes used for the deposition of the layers were developed by trying out different doping gas flow ratios. The optimized recipe used for the deposition of the intrinsic and doped a-Si:H layers are given in **Table 2.2.** During the deposition, the pressure and temperature are maintained at 1 mbar and 180 °C. The RF power is kept at 3 W. The tune and load position are maintained at 27 and 50 respectively. The flow rate of the gases is measured in Standard Cubic Centimetre per Minute (sccm).

**Table 2.2 :** Specifications of the layers deposited using PECVD

| Layer | Gases used | Gas flow rate(sccm) |
|---|---|---|
| Intrinsic a-Si:H | $SiH_4$ | 20 |
| | $H_2$ | 20 |
| *p*-type a-Si:H | $SiH_4$ | 20 |
| | $B_2H_6$ | 15 |
| *n*-type a-Si:H | $SiH_4$ | 40 |
| | $PH_3$ | 30 |

The next PECVD machine used is the *Plasmalab80Plus* manufactured by *Oxford Systems*. It is used in the deposition of Silicon Nitride ($SiN_x$) layers during the hydrogenation step. The deposition takes place using an optimized recipe at 400 °C. The deposition rate is maintained at 9.37 nm/min. The gases used in this deposition are Silane ($SiH_4$) and Ammonia ($NH_3$).

### 2.2.8 High-Temperature Annealing

The next step in the fabrication of the solar cell is the high-temperature annealing process. This is performed to activate the dopants in the layer and also crystallize the doped a-Si layers to doped poly-Si layers [53]. Prolonged annealing may increase the boron diffusion which has negative effects on the passivation quality. Extended annealing at temperatures higher than optimum reduces the thickness of the tunnel oxide layer resulting in the formation of pinholes. This deteriorates the carrier selectivity of the TOPCon structure [54]. The wafers are annealed in a *Tempress* furnace using an optimized recipe developed in the PVMD group. It is performed for 15-60 minutes at a temperature of 850 °C in a $N_2$ atmosphere.

### 2.2.9 Hydrogenation

Hydrogenation is one of the chemical passivation techniques used in the thesis. It helps in saturating the surface silicon atoms or dangling bonds with hydrogen atoms. These dangling bonds act as recombination centres and induce trap states as shown in **Figure *2.5***. The effusion of the hydrogen atoms during the high-temperature annealing step can be alleviated by performing this hydrogenation step [55]. Hydrogen passivation is a widely practiced chemical passivation technique. It employs hydrogen-rich dielectric layers to passivate the dangling bonds by creating Si-H bonds. The hydrogenation consists of two steps namely – deposition of hydrogen-rich capping layer ($SiN_x$) and forming gas annealing (FGA).

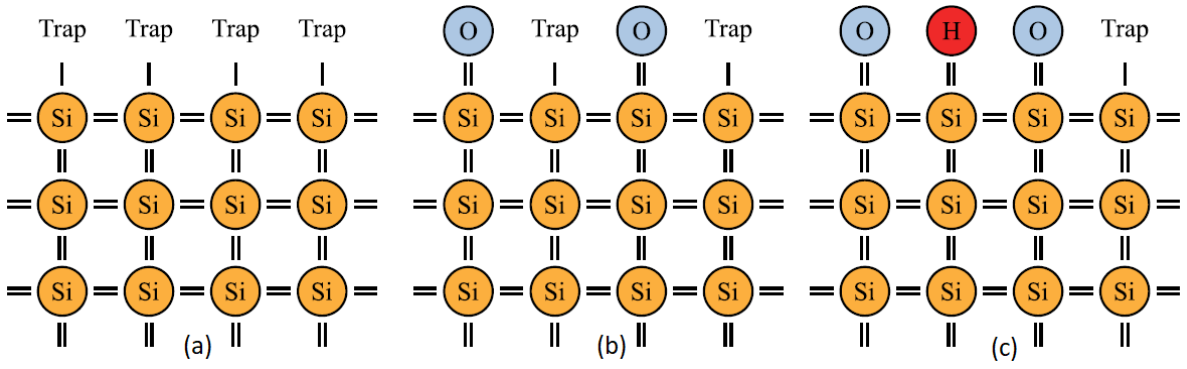


**Figure 2.5** (a) unpaired valence electrons forming dangling bonds at the c-Si surface (b) the dangling bonds being saturated by the oxygen atoms after chemical oxide growth (c) further saturation of the dangling bonds by hydrogenation [56]

The $SiN_X$ layer is deposited using the *Plasmalab80Plus* manufactured by *Oxford Systems*. The gases used in this process are Silane ($SiH_4$) and Ammonia ($NH_3$). An optimized recipe is used with the deposition conditions of temperature 400 °C, a pressure of 87 Pa and gas flow rate is maintained at 200 sccm. 75 nm-thick $SiN_X$ layer is deposited and the deposition rate is maintained at 9.37 nm/min.

The forming gas annealing treatment is carried out to release the hydrogen atoms embedded in the hydrogen-rich $SiN_X$ layer [57]. It also provides additional $H_2$ atoms to diffuse into the c-Si bulk and passivate the defects [58]. The furnace used for this annealing was developed by *Tempress Systems.* The annealing is performed in an atmosphere containing a mixture of 10 % $H_2$ and $N_2$, at a temperature of 400 °C for 30 minutes. The flow rate of the forming gas during FGA is maintained at 4 standard litres per minute (SLM).

### ANA hydrogenation

The Atomic Layer Deposition (ALD) followed by Rapid Thermal Processing (RTP) annealing was another hydrogenation technique used in this thesis. It is used on the symmetric samples for the passivation tests. ALD works on the process of depositing thin films over a number of cycles during which the substrate is exposed to precursor gases. The ALD is used to deposit Aluminium Oxide ($AlO_X$) which also acts as a capping layer. The precursor gases used in this process are water and Trimethylaluminium (TMA).

This ALD process consists of four steps: first, the wafer is coated with the TMA, which adsorbs on the surface. Second, the leftover TMA and the excess by-products are purged. Third, water is fed in to react with the TMA to form the first layer of $AlO_X$. Finally, the excess water is purged out and the cycle is repeated. In this thesis, the number of cycles used is 100 and approximately 7nm-thick $AlO_X$ layer is deposited at the end of the process. This process is carried out in OpAL™ reactor by *Oxford Instruments* at a temperature of 105 °C.

After the $AlO_X$ layer deposition, RTP annealing is performed on the substrates. This takes place at a temperature of 600 °C for 10 minutes in a $N_2$ atmosphere, using an optimized recipe from the PVMD group. This is followed by $SiN_X$ layer deposition and another round of $AlO_X$ layer is deposited using ALD. The samples are then made to undergo FGA at 400 °C for 30 minutes. This hydrogenation approach consisting of $AlO_X$/RTP/ $SiN_X$/ $AlO_X$/FGA is known as ANA hydrogenation.

## 2.2.10 Transparent Conductive Oxide Layer Deposition

Transparent Conductive Oxide (TCO) layers are used for providing the necessary lateral conductivity. These layers are deposited on both sides of the wafer using the magnetron sputtering process. In the sputtering process, Argon (Ar) gas particles are given high energy to bombard the TCO source materials. This bombardment vaporizes the source material, which is then deposited on the wafers as TCO. The generally used TCOs are Fluorine doped Tin Oxide ($SnO_2$:F), Aluminium doped Zinc Oxide (ZnO:Al), Boron doped Zinc Oxide (ZnO:B), Hydrogen doped (hydrogenated) Indium Oxide($In_2O_3$:H) [16], [59].

In this thesis, Indium doped Tin Oxide (ITO) is used as the TCO. It is a mixture of 90 % Indium Oxide ($In_2O_3$) and 10 % Tin Oxide ($SnO_2$). ITO shows promising long-term stability [60]. It also provides an excellent balance of transparency and conductivity [61]. One disadvantage of the sputtering process is the passivation damage it causes on the thin poly-Si layers [38],[62],[63]. The TCO layer also acts as an anti-reflection coating on the illuminated side of the solar cell [64].

The pattern of the deposition is taken care of by hard masks. The ITO deposition is performed using the *Zorro* sputtering machine developed by *Polyteknik*. An optimized recipe developed in the PVMD

group is used for the ITO deposition. The process takes place at room temperature and at a pressure of 3.7 $10^{-2}$ mbar. The Argon flow rate is maintained at 40 sccm. 75 nm-thick ITO layers are sputtered on both sides of the textured wafer.

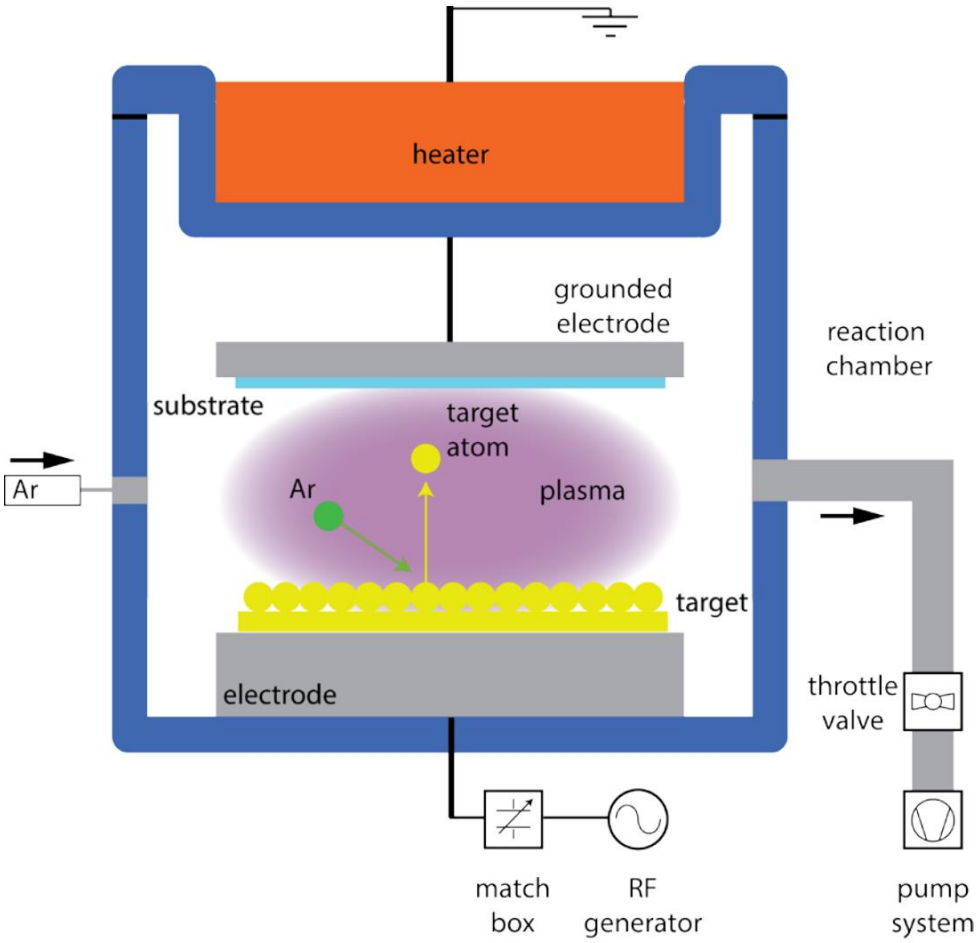


**Figure 2.6** Schematic representation of a RF-magnetron sputtering process and its system components [52]

### 2.2.11 Metal Evaporation

The next step in the fabrication of the solar cell is the deposition of the metal seed layer. The deposition is done using the metal evaporation technique in this thesis. Electron beams or resistive heat source are used to warm the metal to its melting point. This metal would then evaporate and be deposited on the target surface uniformly.

The metal used as a seed layer in this thesis is Silver. It is uniformly deposited on both sides of the wafer. The equipment used for this process is *Provac* evaporation machine in the EKL cleanroom. The full area metal deposition happens in vacuum, at a pressure of $10^{-5}$ mbar. This enables the control of material oxidation and thickness. The desired thickness of the metal seed layer is 200 nm. The thickness for the textured substrate is reduced by a factor of 1.73 from the estimated thickness on a flat substrate.

This metal seed layer is crucial for the photolithography and the copper-plating metallization step. The seed layer prevents the diffusion of copper into the silicon surface. Diffusion of copper into silicon results in the formation of impurities which act as recombination centres [65].

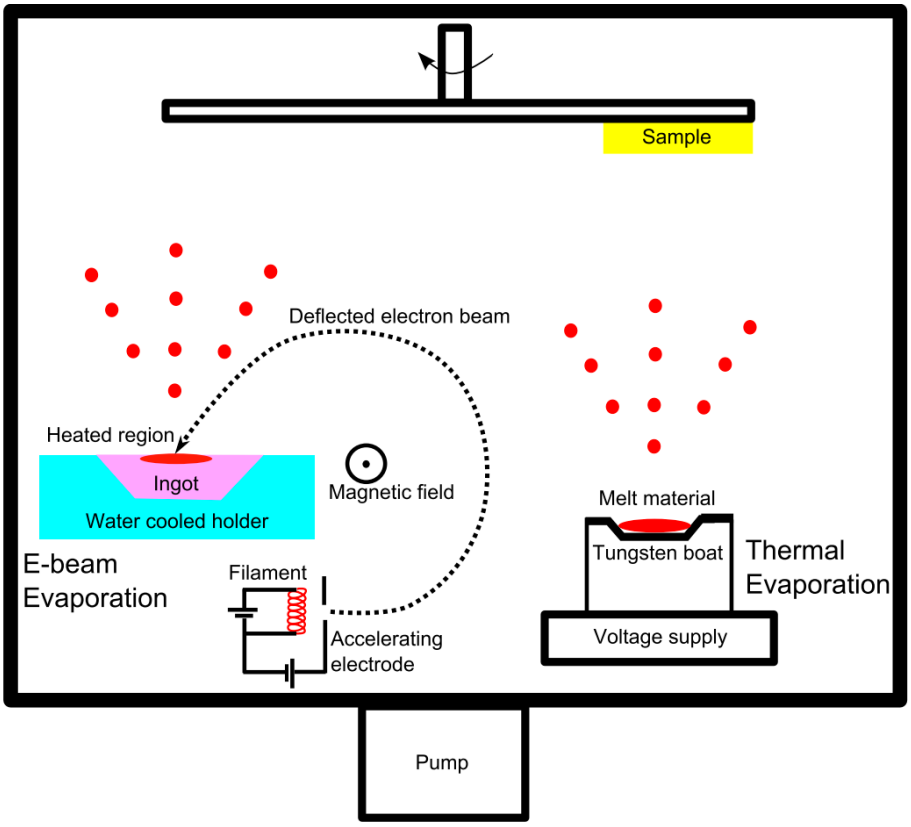


**Figure 2.7** Schematic representation of the metal evaporation process [66]

### 2.2.12 Photolithography

Photolithography is the process used to define the position of the fingers and busbars on the substrates. A photo-sensitive organic material called photoresist (PR) is first coated. The PR coated wafers are then exposed to ultra-violet light through a mask of the desired pattern. The exposed area is then developed to form very precise patterns with feature size less than 1µm [67].

The process begins with a PR layer being coated on the wafer surface using the spin-coater. It helps in having a uniform distribution of the PR by spinning it at various speeds. The deposited PR can be either positive or negative. A positive PR, AZ 3027 is used in this thesis. An optimized recipe of AZ 3027 ECI 4 µm is used for the PR coating. 12 µm-thick PR layers were coated on each side of the substrate in three rounds of coating. After each round of the coating, the substrates are baked in the oven at 100 °C for 2 minutes, 3 minutes and 5 minutes respectively. This is done to harden the PR layers before exposure.

The PR is sensitive to ultra-violet light and will undergo a transition when exposed to it for a specific duration. The duration of exposure depends on the PR layer thickness. By exposing the layer through a mask, the pattern is formed on the wafer. The equipment used for exposure is the *EVG* 420 contact aligner from the EV group. A split-exposure approach is employed in this thesis. The samples are exposed through a 6-die mask for 120 seconds. It is split into 40 seconds for each exposure. After the exposure, the wafer is developed for 2 minutes and rinsed with DI water. The developer solution used in this thesis is the MF 322 developer.

The exposed PR layer is etched away in case of a positive PR. In case of a negative PR, the exposed area is not etched during development whereas, the unexposed PR area is etched away. The developed samples are dried and checked under a microscope for the pattern openings.

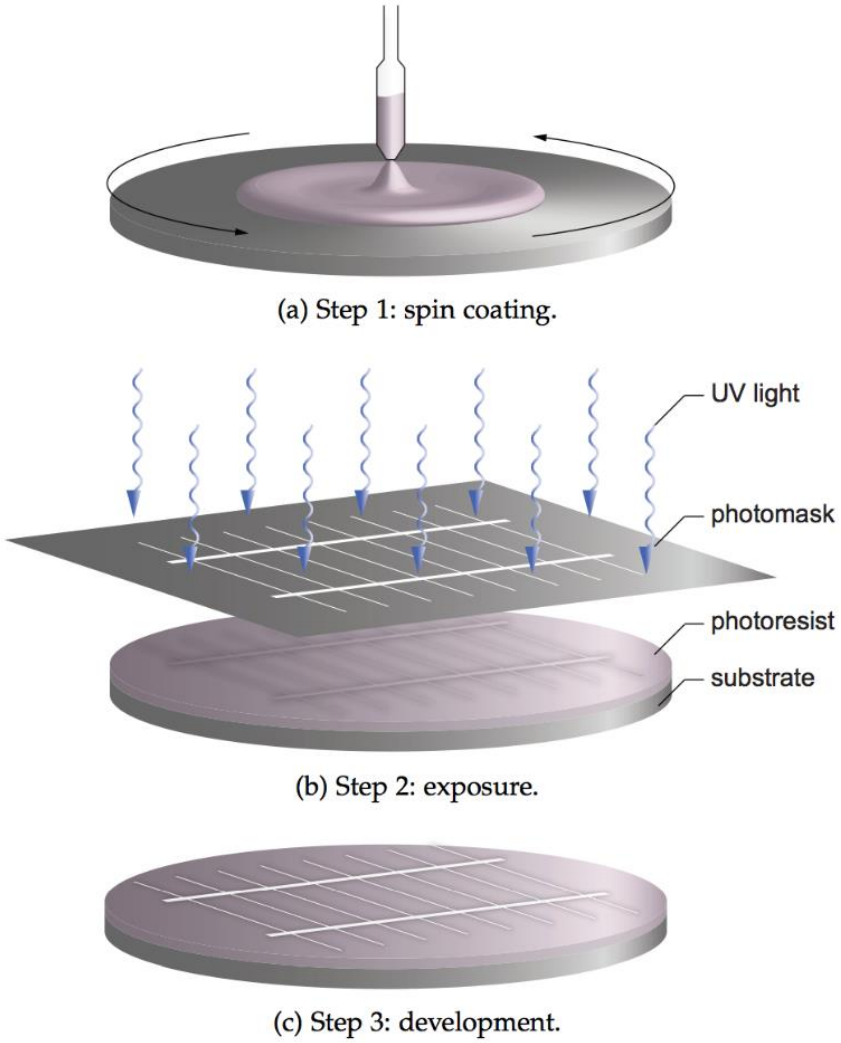


**Figure 2.8** Schematic representation of the working principle of the photolithography with a positive photoresist [68]

### 2.2.13 Copper plating metallization

The final step in the solar cell fabrication process is metallization. It influences both optical and electrical parameters of the solar cell. Optically, the finger width on the cell influences the short circuit current due to the shading effect. Electrically, the metal fingers add to the series resistance of the solar cell which in turn affects the fill factor [16].

The metallization technique used in this thesis is the Copper-electroplating process. Copper-electroplating is an electrochemical (redox) reaction. It involves the transfer of electrons between two electrodes and an electrolyte solution. The working principle is that the wafer is placed at the cathode and the copper plates at the anode. Copper sulphate is the electrolyte solution. When the reaction takes place, the copper at the anode dissolves in the electrolyte and is deposited on the wafer at the cathode. A schematic representation of the process is shown in **Figure *2.9***.

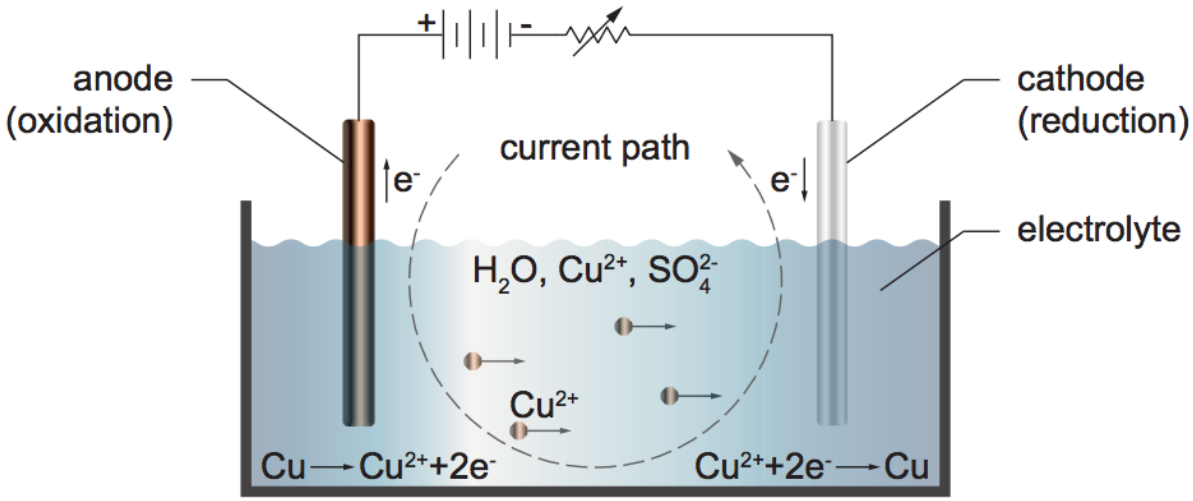


**Figure 2.9** Schematic representation of Copper electroplating process [16][68]

This process is carried out in an in-built copper electroplating machine available in the EKL. The wafer is loaded vertically in a bifacial wafer holder with copper plates on both sides. These copper plates act as counter electrodes. The electrolyte bath is maintained at room temperature. The electrolyte bath is well stirred to avoid any crystallization by pumping it in through a filter.

Both the copper plates have power sources developed by *Metrohm Autolab.* These power sources can act as galvanostat and potentiostat. The galvanostat supplies a constant current during the process and the voltage is varied. The potentiostat supplies a constant voltage during the process and the current is varied. The copper plates are connected to the positive terminal and the wafer is connected to the negative terminal. Hence, a positive current is supplied for the electrochemical reaction to take place. If the connection is done in reverse, a negative current is to be provided.

A two-step copper-plating recipe combining both the potentiostat and galvanostat settings is utilized during this thesis. A voltage of 0.35 V for 30 seconds and a current of 0.4 A for 10 minutes are the settings used in this thesis for bifacial copper-plating. The duration mentioned here is the duration of plating at the specified current and voltage respectively.

This process is very challenging due to the diffusion of copper into the silicon surface. It leads to the formation of impurities that act as recombination centres. These recombination centres cause a decrease in the minority carrier lifetime and affect the performance of the solar cell [16] [65].

After the copper-plating is performed, the photoresist and metal seed layer need to be removed before measuring the solar cell parameters. The photoresist is etched using acetone and the sample is rinsed with DI water. The metal seed layer is removed by immersing the wafer in an aqueous solution of 200 ml DI water, 50 ml of 31 % hydrogen peroxide ($H_2O_2$) and 12.5 ml of 28 % ammonium hydroxide ($NH_4OH$). The samples are then rinsed with DI water and dried using a spin-dryer.

## 2.3 Characterization techniques

The characterization techniques are essential in improving and optimizing the manufacturing processes and solar cell performance. The various characterization techniques used in this thesis are described in this section.

### 2.3.1 Spectroscopic Ellipsometry

While manufacturing the solar cells with thin-film layers, it is critical to have precise control of the layer thickness [21][69][70]. To measure the thickness, Spectroscopic Ellipsometry (SE) was used in this thesis. SE is an optical technique that measures the difference between the incident and the scattered light to determine the thickness. It also provides information on the optical constants of the deposited material using a well-defined optical model [71]. The equipment used in this thesis is the *M-2000DI* manufactured by *J.A Woollam Co.*

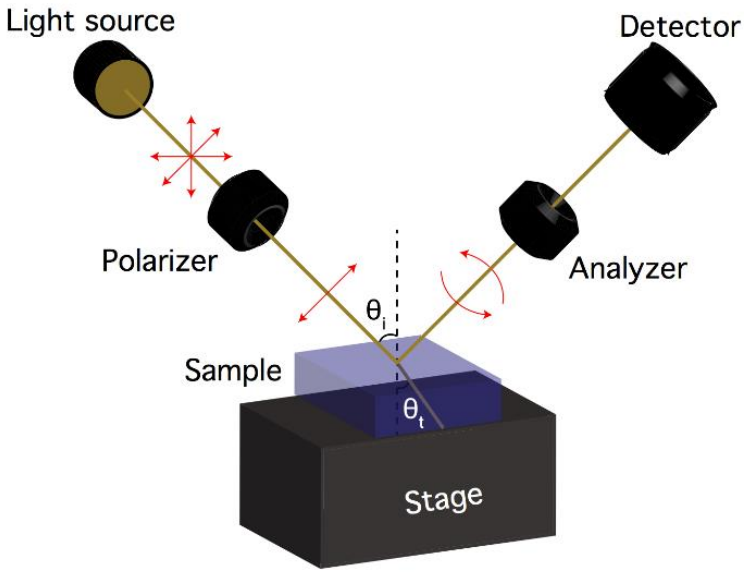


**Figure 2.10** Schematic representation of Spectroscopic Ellipsometry measurement setup [72]

### 2.3.2 Photoconductance Lifetime Measurements

The quality of the passivation of the deposited layers on the wafer surface is determined using photoconductance lifetime measurements. *Sinton WC-120* is the equipment used for lifetime measurements. The samples are exposed to a short flash of light. This induces changes in the photoconductance of the sample caused by the recombination of the excess generated carriers [73]. These changes in the photoconductance are sensed by a coil coupled with the RF bridge. The effective minority carrier lifetime $\tau_{eff}$, the recombination current density $J_0$, and the implied open-circuit voltage $iV_{OC}$ are determined from this measurement setup [73]. The lifetime of a minority carrier $\tau_{eff}$ is defined as the average time that the excess minority carrier requires before it recombines [16].

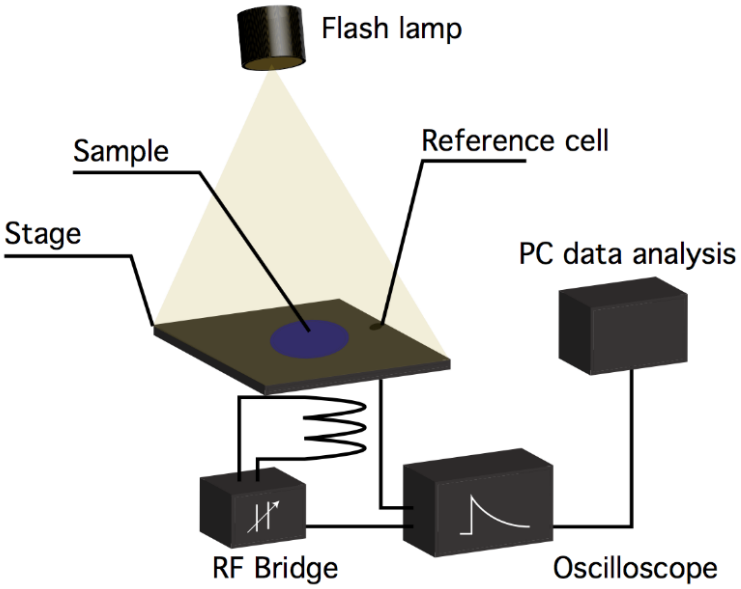


**Figure 2.11** Schematic representation of the Sinton WC-120 measurement setup [72]

### 2.3.3 Profilometer

To obtain solar cells with a uniform thickness of copper on the fingers and busbars, the finger height must be measured after the first deposition. In this thesis, the finger height of the copper-plated wafers is measured using the *Profilometer Dektak 150* manufactured by *Veeco*. A sensitive stylus probe (needle) makes contact with the sample and measures the finger height. The stylus moves in the longitudinal direction on the wafer surface placed on the horizontal plane. The measurement range and the length span of the measurements can be set. The computer software records the movement of the stylus on the wafer surface. It is displayed on the screen as a plot between the height and length. The force applied by the stylus on the wafer surface is very low hence, there will be no damage to the metal layer. This process is used to measure the height and width of the metal contacts.

### 2.3.4 Current-Voltage measurements

The current and voltage characteristics of the fabricated solar cell are measured using the AAA class *Wacom WXS-156S-L2* solar simulator. The test is performed under the standard conditions which are an irradiance of 1000 $W/m^2$, a 1.5 AM spectrum and the solar cell temperature of 25°C [16]. The spectrum is simulated by the combination of a halogen lamp and a Xenon lamp. The current-voltage curve is generated when the solar cell is exposed to the spectrum. A reference solar cell is used for the calibration of the measurement setup.

An example of the *J-V* curve is shown in **Figure *2.13***. $V_{OC}$ is the open-circuit voltage, $J_{SC}$ is the short-circuit current density and MPP denotes the maximum power point. The fill-factor (*FF*) and efficiency ($\eta$) can be further calculated from the obtained open-circuit voltage ($V_{OC}$) and short-circuit current density ($J_{SC}$).

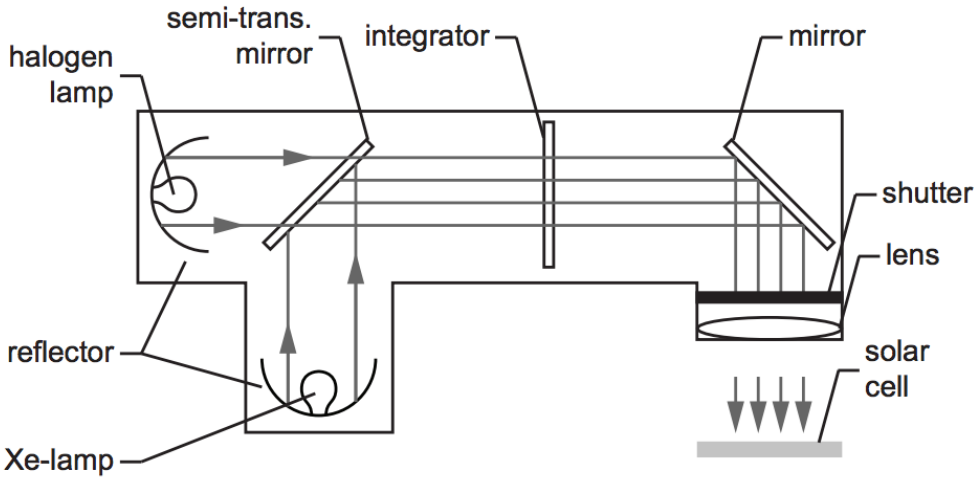


**Figure 2.12** Schematic representation of the Current-Voltage measurement setup [72]

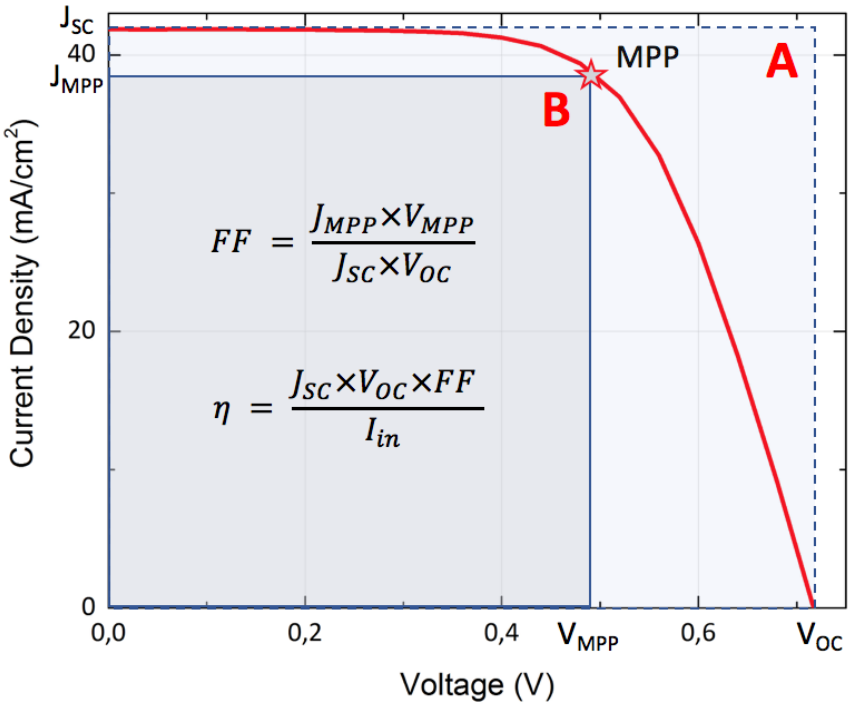


**Figure 2.13** Example of a measured J-V curve with definitions of fill factor and efficiency [16]

# 3 Passivation optimization of poly-Si carrier selective contact

To reduce the recombination at the interface of the metal and the silicon, poly-Si contacts are used. The combination of the ultra-thin silicon oxide ($SiO_X$) and the doped poly-Si layers provide excellent passivation for the c-Si surface. The main objective of this chapter is to optimize the passivation quality of the poly-Si symmetric samples and solar cell precursors. More emphasis is on the optimization of the p-type doped poly-Si layers. *Section 3.1* discusses the experimental results achieved on symmetric passivation test samples for varied intrinsic layers with doped poly-Si layers. *Section 3.2* discusses the influence of the thickness and the doping gas flow ratio of the *p*-type doped poly-Si layers on the passivation quality. The different hydrogenation approaches for the solar cell precursor are compared in *Section 3.3*. The findings of this chapter are summarised in *Section 3.4*.

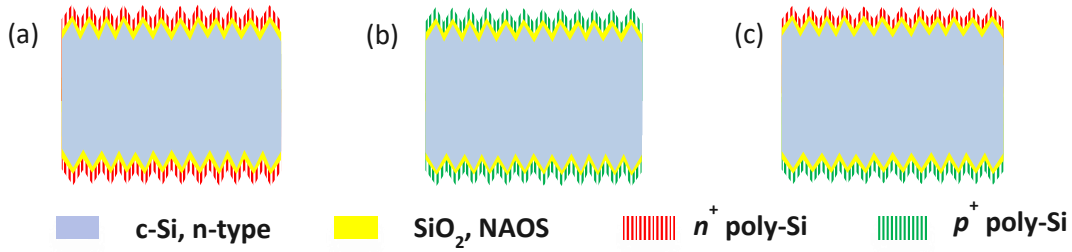


**Figure 3.1** Schematic representation of (a) $n^+$ poly-Si symmetric sample; (b) $p^+$ poly-Si symmetric sample and (c) solar cell precursor

## 3.1 Varied intrinsic layers with doped poly-Si layers

The structure of the poly-Si carrier selective contact consists of an ultra-thin $SiO_X$ layer and a highly doped poly-Si layer. In the fabrication process of the symmetric samples discussed in *Section 2.1.1*, the $SiO_X$ layer is grown using silicon oxide growth through NAOS [45]. On top of the $SiO_X$ layer, the intrinsic hydrogenated a-Si layer ((i)-a-Si:H) is deposited which is followed by the doped a-Si:H layer. In this section, different deposition techniques used for the (i)-a-Si:H layer growth will be studied. The corresponding passivation quality on the final passivation test samples will be compared.

Four variations of the intrinsic layer deposition are tried in this thesis. Symmetric test samples with no intrinsic layer were prepared. The symmetric samples were also subjected to the intrinsic layer growth through LPCVD and PECVD. For the final variation, an intermediate annealing step was performed after the intrinsic layer growth in PECVD.

**Table 3.1 :** Symmetric test samples for (i) a-Si:H layer variation

| Process | Sample-1 | Sample-2 | Sample-3 | Sample-4 |
|---|---|---|---|---|
| $SiO_X$ growth | NAOS | NAOS | NAOS | NAOS |
| (i)-a-Si:H | N/A | LPCVD | PECVD | PECVD + annealing |
| doped a-Si:H | PECVD | PECVD | PECVD | PECVD |
| Annealing | 850 °C 15 minutes | 850 °C 15 minutes | 850 °C 15 minutes | 850 °C 15 minutes |
| Hydrogenation | $SiN_X$+FGA | $SiN_X$+FGA | $SiN_X$+FGA | $SiN_X$+FGA |

This intermediate annealing before the deposition of the doped layers is performed at 600 °C for 60 minutes in $N_2$ atmosphere. The deposition parameters for the intrinsic a-Si:H layer grown through LPCVD can be found in *Section 2.2.6*. *Section 2.2.7* gives information regarding the deposition parameters for the a-Si:H layers grown through PECVD. The total thickness of the *i/n* and *i/p* layers are kept at 16 nm on each side of the symmetric sample. 8 nm-thick (i) a-Si:H layer and 8 nm-thick doped a-Si:H layer is the starting point of the layer thickness since the objective is to keep the poly-Si layers as thin as possible.

For the subsequent high-temperature annealing, samples are made to undergo annealing at 850 °C for 15, 30, 45, and 60 minutes respectively. Both $n^+$ poly-Si and $p^+$ poly-Si symmetric samples observed better passivation for the annealing condition of 15-minute annealing at 850 °C. With this optimal annealing condition, the implied $V_{OC}$ ($iV_{OC}$) of the samples obtained after the $SiN_x$/FGA hydrogenation process are compared for the different intrinsic layer deposition processes. 75nm-thick $SiN_x$ layer is deposited at 400 °C on both sides. The subsequent forming gas annealing was done at 400 °C for 30 minutes.

**Figure *3.2*** shows a comparison of the $iV_{OC}$ values before and after the hydrogenation of $n^+$ poly-Si symmetric samples. The different deposition techniques for the intrinsic layer with n-type doped layer are given on the x-axis.

It is observed that the samples with PECVD intrinsic layer shows better passivation indicated by the higher $iV_{OC}$ values. The samples without the intrinsic layer show a relatively lower $iV_{OC}$ value of 666 mV. Whereas, the sample with PECVD intrinsic layer resulted in an $iV_{OC}$ of 713 mV. This indicates that the intrinsic layer is effective in improving the contact's passivation quality, which is in accordance with the reference [74]. The sample with the intermediate annealing before the doped layer deposition enhanced the passivation quality and resulted in an $iV_{OC}$ of 718 mV. The sample with LPCVD intrinsic layer observed an $iV_{OC}$ of 706 mV.

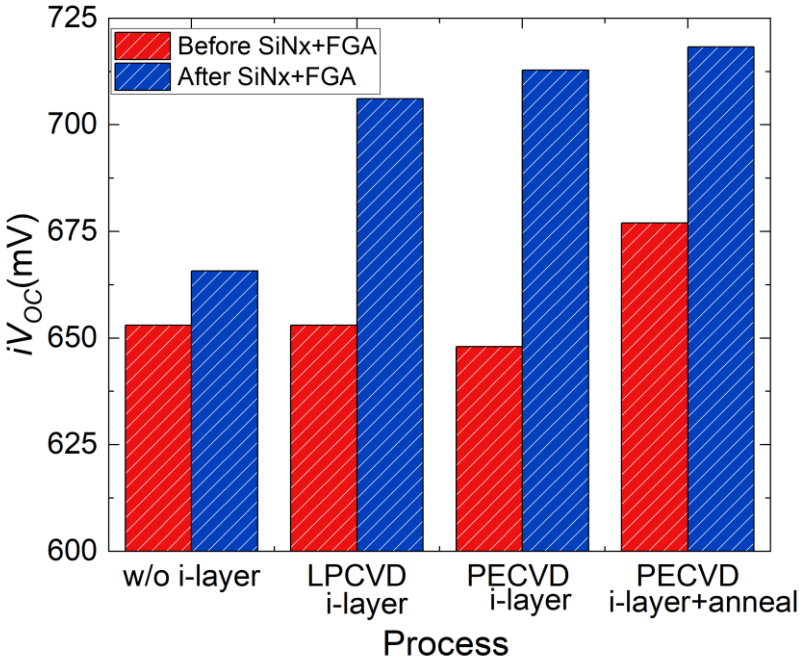


**Figure 3.2** Comparison of $iV_{OC}$ for $n^+$ poly-Si symmetric samples with different deposition techniques for intrinsic layer

A similar approach is also applied for the $p^+$ poly-Si symmetric samples. Different deposition techniques are used for the intrinsic layer growth with a p-type doped layer. The $iV_{OC}$ values obtained before and after the hydrogenation step are shown in **Figure 3.3**.

The sample without an intrinsic layer shows a relatively lower $iV_{OC}$ of 656 mV than the ones with the intrinsic layer. Similar to the $n^+$ poly symmetric samples, the sample with intrinsic layer grown through PECVD shows better passivation results. The highest $iV_{OC}$ of 665 mV is achieved for the PECVD intrinsic layer. The intermediate annealing step resulted in a decrease in the passivation quality, unlike in the $n^+$ poly-Si symmetric sample, where it enhanced the passivation quality. The passivation is also lower for the sample with intrinsic layer grown through LPCVD compared to PECVD.

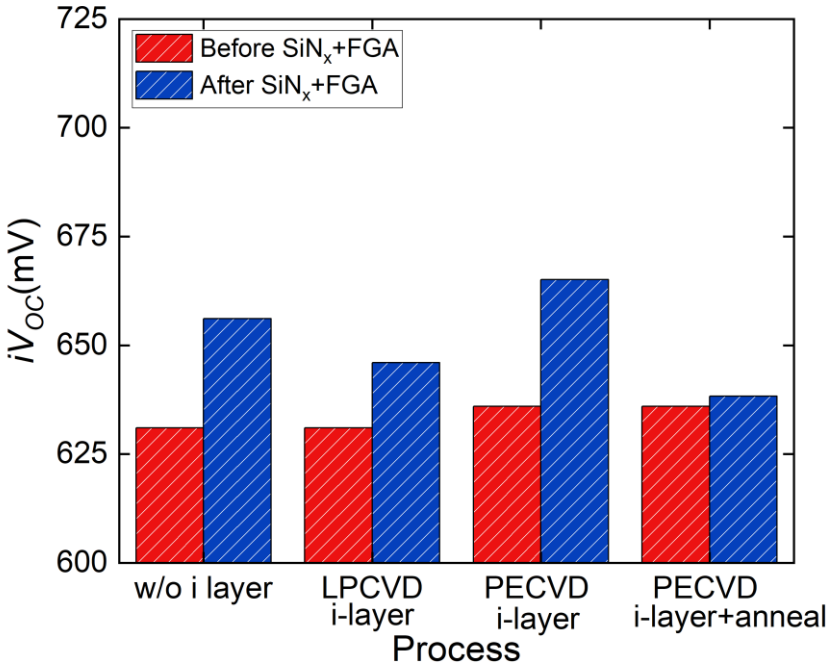


**Figure 3.3** Comparison of $iV_{OC}$ for $p^+$ poly-Si symmetric samples with different deposition techniques for intrinsic layer

Sufficiently high passivation quality is observed for the 16 nm-thick $n^+$ poly-Si symmetric samples but the passivation quality is much lower for the 16 nm-thick $p^+$ poly-Si symmetric samples. Thus, more optimization is required for the *p*-type doped layers to improve the passivation quality. The intermediate annealing step had a negative effect on the passivation quality of $p^+$ poly-Si symmetric samples compared to the $n^+$ poly-Si symmetric samples. Therefore, it was decided that intermediate annealing would not be performed further in this thesis. PECVD would be the preferred deposition technique used for the intrinsic layer deposition. The optimal high-temperature annealing condition to be used in further fabrications is decided to be 15 minutes at 850 °C.

## 3.2 Optimization of *p*-type doped layers

As described in the previous section, the passivation quality of the 16 nm-thick $p^+$ poly-Si Symmetric samples was much lower compared to the 16 nm-thick $n^+$ poly-Si symmetric samples. Obtaining high passivation on $p^+$ poly-Si samples was challenging. Hence, further optimization of the *p*-type doped layers is performed to improve the passivation. In this section, the thickness and the doping gas flow ratio of the *p*-type doped layer are varied to study their influences on the passivation quality.

### 3.2.1 $p^+$ poly-Si layer thickness

The starting point of the thickness of the doped poly-Si layers was 16 nm for both *i/n* and *i/p* symmetric samples. The challenge was to keep the *i/n* and *i/p* layers as thin as possible, while also maintaining sufficient passivation quality. As an adequate level of passivation was achieved for 16 nm-thick $n^+$ poly-Si symmetric samples, the thickness variation is tested on the $p^+$ poly-Si samples. The thickness of the *i/p* layers is increased to check if there is any influence on the passivation quality.

This experiment of thickness variation is carried out on the symmetric samples. The deposition parameters of the doping gas can be found in **Table *2.2*** in *Section 2.2.7*. The high-temperature annealing after the doped layer deposition is performed at 850 °C for 15 minutes. The $SiN_X$/FGA is the hydrogenation approach used in this experiment. 75nm-thick $SiN_X$ layer is deposited at 400 °C on both sides. The subsequent forming gas annealing is done at 400 °C for 30 minutes.

The $iV_{OC}$ values of the symmetric samples with different *i/p* layer thicknesses are seen in **Figure 3.4**. The $iV_{OC}$ values obtained after the $SiN_X$/FGA hydrogenation process are compared for the different *i/p* layer thicknesses of 16 nm, 22 nm, 28 nm, 34 nm, and 40 nm.

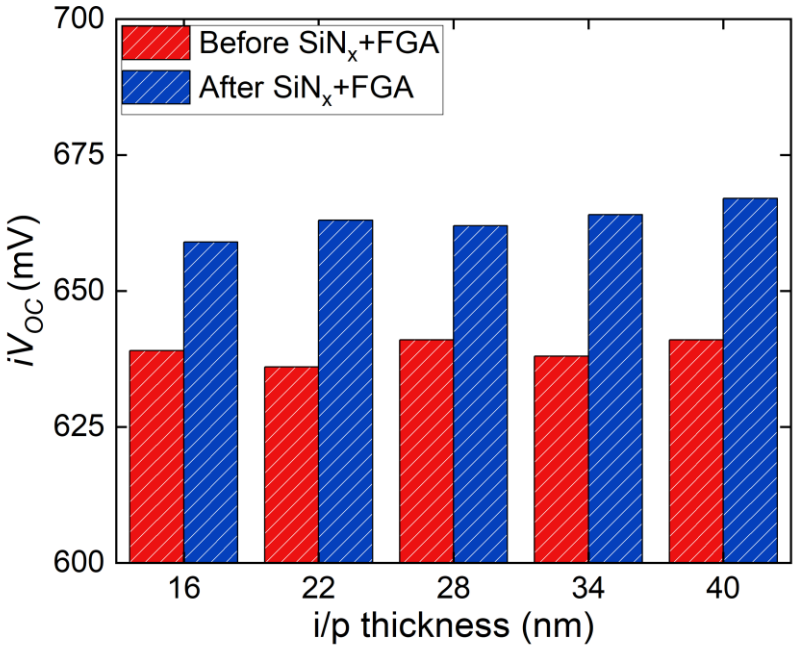


**Figure 3.4** Impact of increasing $p^+$ poly-Si layer thickness on $iV_{OC}$ of $p^+$ poly-Si symmetric samples

It is observed that the variation of thickness did not yield a significant difference in the passivation. Due to significant parasitic absorption at device level, very thick poly-Si layers are not preferred [38],[61]. It is also known that TCO sputtering severely degrades the passivation quality of poly-Si layers below 40 nm [38]. The subsequent processes during the contacting might also be more aggressive on the thin poly-Si layers [75], with values of $J_{0.metal}$ ~ 400 fA/cm$^2$ [76]. The sample with 40 nm-thick i/p layer provides slightly better passivation.

**Solar cell precursor:** The thickness of *i/p* layer is slightly increased to 42 nm, to check for improvements in the passivation quality of the solar cell precursor. The passivation quality of this solar cell precursor was compared to a solar cell precursor with a 40 nm *i/p* layer. Meanwhile, the thickness of the *i/n* layer is maintained at 16 nm. The high-temperature annealing is carried out at the optimum

condition 15 minutes at 850 °C. $SiN_X$ /FGA hydrogenation is performed on the cell precursors. An increase in the $iV_{OC}$ values is observed for the cell precursor with a slightly thicker *i/p* layer. It can be seen from **Figure *3.5***, that the passivation quality indicated by the $iV_{OC}$ is significantly higher for the solar cell precursors with a 42 nm-thick *i/p* layer after hydrogenation. Hence, 42 nm-thick *i/p* layer will be used for further fabrication.

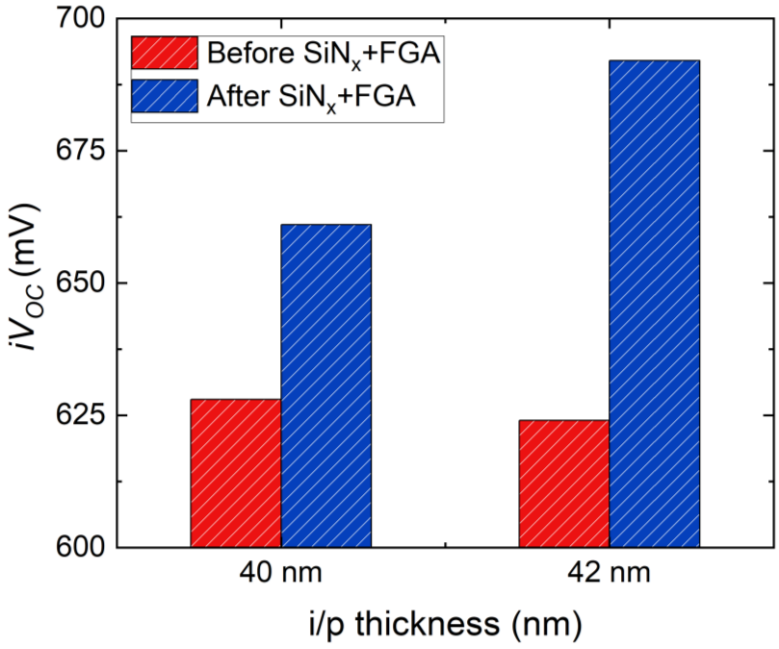


**Figure 3.5** Influence of different *i/p* layer thickness on $iV_{OC}$ of solar cell precursor

The effect of the thickness ratios between (i) a-Si:H and (p)a-Si:H on the passivation quality of the $p^+$ poly-Si, and therefore, that for the solar cell precursor is checked. A thicker doped layer might induce a higher doping level in the poly-Si, which is beneficial for better field-effect surface passivation. Keeping the total thickness of the *i/p* layer constant at 42 nm, the thickness ratio of the intrinsic to the doped layer is varied. Two variations of the *i/p* layer thickness ratios are tested: 12/30 and 21/21. The thickness of the *i/n* layer is maintained at 16 nm. The high-temperature annealing is done for 15 minutes at 850 °C. The $iV_{OC}$ values obtained after $SiN_X$ /FGA hydrogenation are compared and is shown in **Figure *3.6***. Maintaining the same layer thickness for both the intrinsic and the doped layer gives notably better results. A decrease in the $iV_{OC}$ values is observed when the thickness ratio is varied. Hence, it is decided to maintain same thickness for both intrinsic and doped layers.

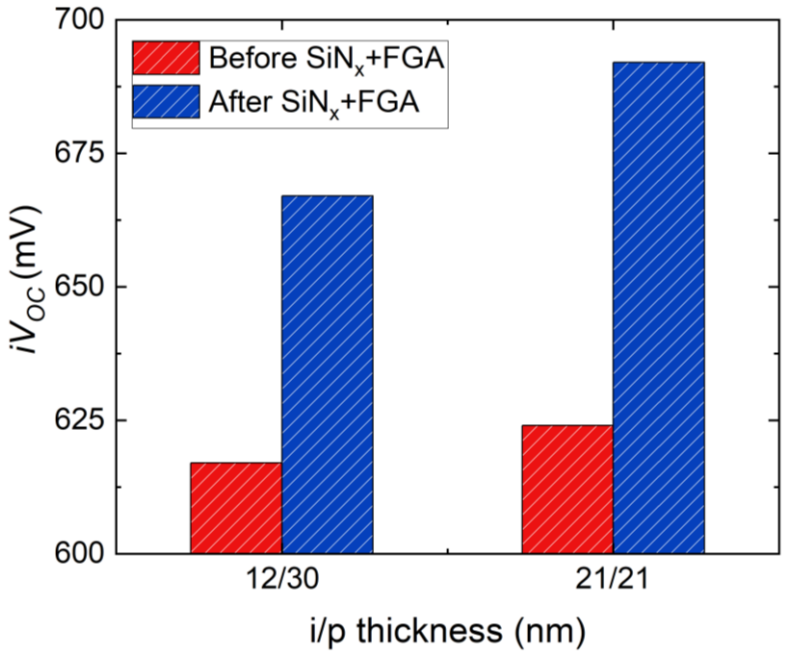


**Figure 3.6** Effect of different *i/p* layer thickness ratio on $iV_{OC}$ of solar cell precursor

### 3.2.2 *p*-type doping gas flow ratio

The previously used doping gas flow rate for the p-type doped layer is $SiH_4$ - 20 sccm and $B_2H_6$ - 15 sccm for the $p^+$ poly-Si preparation shown in the previous sections. In this section, the doping gas flow rates of the *p*-type doped layer are varied to check for its influence on the passivation quality of the $p^+$ poly-Si symmetric samples. Higher doping of poly-Si is beneficial for better surface passivation only if the excessive dopant diffusion through the silicon oxide layer is minimized. Otherwise, it would lead to stronger Auger recombination [77]. The different doping gas flow ratios used for this experiment are shown in **Table 3.2**.

**Table 3.2 :** Variation of the *p*-type doping gas flow ratio

| Layer | Gases used | Gas flow rate(sccm) |
|---|---|---|
| *p*-type a-Si:H | $SiH_4$ -$B_2H_6$ | 31/4 |
| | | 25/10 |
| | | 20/15 |
| | | 15/20 |
| | | 10/25 |

The intrinsic layer and doped layers are deposited using PECVD. The thickness of the *i/p* layer is maintained at 42 nm on the $p^+$ poly-Si symmetric samples. Only the $SiH_4$ -$B_2H_6$ doping gas flow ratios are varied. After the doped layer deposition, the samples are made to undergo high-temperature annealing. This annealing is performed at 850 °C for 15, 30, 45, and 60 minutes in $N_2$ atmosphere. It is followed by the $SiN_x$/FGA hydrogenation. The optimized high-temperature annealing condition is for 15 minutes at 850 °C. Passivation results of the samples at this annealing condition are first compared. The $iV_{OC}$ values obtained after the $SiN_x$/FGA hydrogenation process are compared for the different doping gas flow ratios and is shown in **Figure 3.7**.

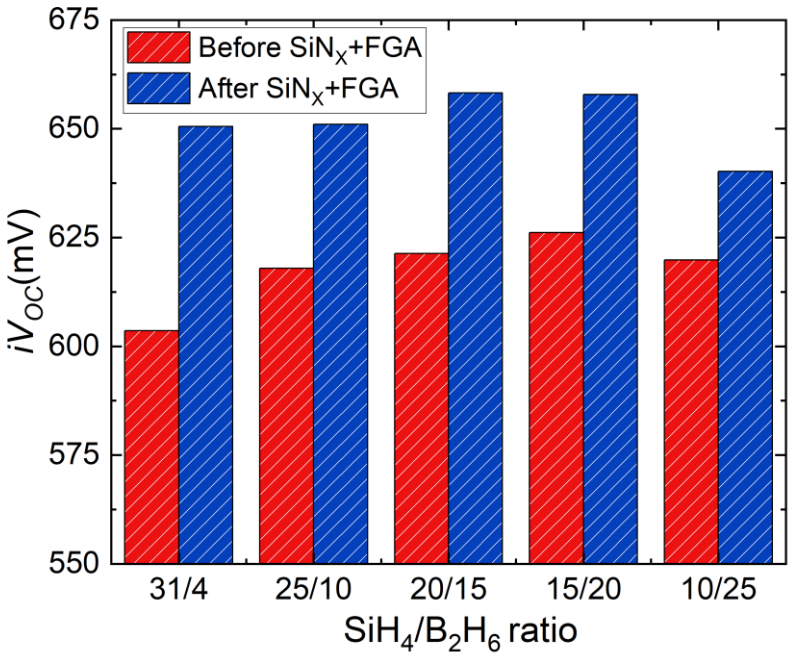


**Figure 3.7** Influence of different doping gas flow ratio on $iV_{OC}$ of $p^+$ poly-Si symmetric samples

The $iV_{OC}$ values for the samples with $SiH_4$ - $B_2H_6$ doping gas ratios 31/4 and 25/10 are similar. The low doping level in these two samples might be the reason for the lower passivation quality observed. For the samples with the doping gas ratio of 10/25, the passivation quality is found to be the lowest among all the samples. This might be due to excessive boron diffusion. The sample with a gas flow ratio of 20/15 shows the best passivation quality. An $iV_{OC}$ value of 658 mV is observed for this sample. From this, it can be concluded that the previously used doping gas flow ratio of 20/15 still provides the best passivation. Further analysis of the doping level will provide insights into the observed difference in passivation quality.

To analyze the doping profiles and the extent of boron diffusion in these samples, Electro-chemical Capacitance Voltage (ECV) measurements are carried out. Three samples with doping gas flow ratios of 31/4, 20/15, and 10/25 are chosen for the ECV measurements. This technique is used to determine the doping profile in semiconductor layers as a function of depth. Controlled etching of the semiconductor material is done using an electrolyte. Subsequent capacitance-voltage measurements across the depth of the semiconductor are performed to obtain the doping profiles [78] [79].

**The influence of doping gas flow ratio: Figure 3.8** shows the measured ECV doping profile of the three selected symmetric $p^+$ poly-Si symmetric samples with different $SiH_4$-$B_2H_6$ doping gas flow ratios. The black curve depicts the doping profile of the doping gas flow ratio $SiH_4$ -$B_2H_6$ = 31/4. The blue curve is the doping profile for the doping gas flow ratio $SiH_4$ -$B_2H_6$ = 10/25. The red curve shows the doping profile for the doping gas flow ratio $SiH_4$ -$B_2H_6$ = 20/15.

There are three regions of interest in **Figure *3.8*** before high-temperature annealing is performed. The in-situ doped poly-Si region of 21 nm, the intrinsic layer region from 21-42 nm, and the c-Si bulk region. The first dotted line at 21 nm represents the interface between the doped and intrinsic region. The second dotted line at 42 nm represents the $SiO_X$ - c-Si interface. The $iV_{OC}$ values obtained after the hydrogenation are also shown in the figure as an indication of the passivation quality.

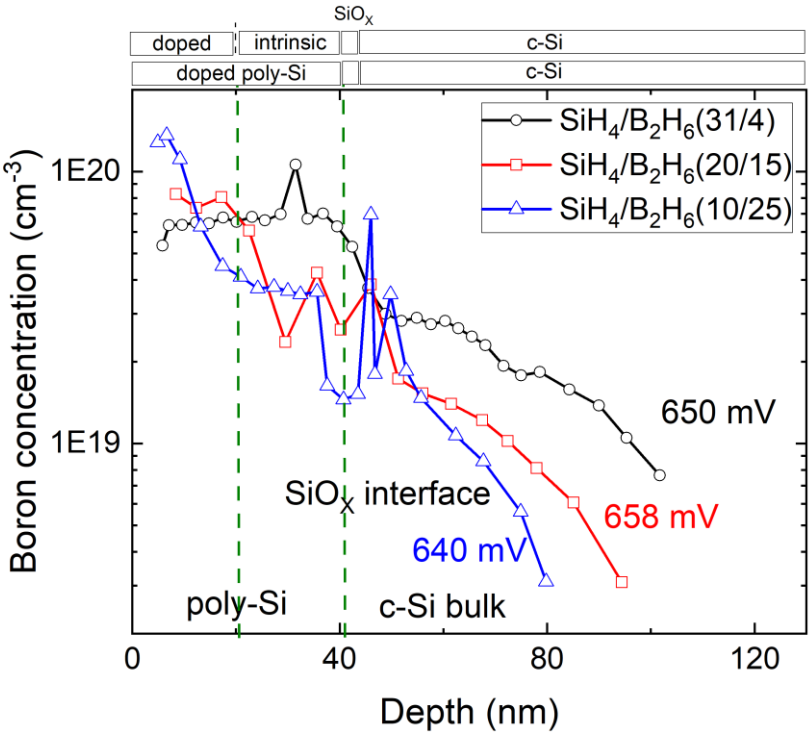


**Figure 3.8** Effect of different doping gas flow ratios on boron diffusion into c-Si bulk

In the in-situ doped poly-Si region, the doping profiles are in accordance with the doping gas flow ratios. As the doping level is increased, the doping concentration of boron is also higher. In the intrinsic region, there seems to be quite a bit of data scattering and the doping profiles have changed positions. This might be due to the ECV measurement equipment but the trend of doping level in the intrinsic region is challenging to reason. Reducing the intrinsic layer thickness can be one of the options to maintain a higher doping level throughout the doped poly-Si region.

Diffusion of the boron atoms into the c-Si bulk is observed for the sample with a doping gas flow ratio $SiH_4$ -$B_2H_6$ = 31/4. As a result, the passivation is lower due to higher Auger recombination. For the sample with the doping gas flow ratio $SiH_4$ -$B_2H_6$ = 10/25, the diffusion of boron into the c-Si bulk is observed to be lower. But the doping concentration is also lower at the $SiO_X$ interface. This results in poor passivation due to a much weaker electric field at the interface. The doping profile achieved for the sample with doping gas flow ratio $SiH_4$ -$B_2H_6$ = 20/15 provides the best passivation compared to the other doping gas flow ratios. This might be because of reduced boron diffusion and reasonably high doping concentration at the $SiO_X$ interface.

**The influence of post-annealing:** The $p^+$ poly-Si symmetric sample with doping gas flow ratio $SiH_4$ -$B_2H_6$ = 20/15 is further analyzed for different annealing times. This is done to investigate the influence of annealing duration on the diffusion of boron into the c-Si bulk. The boron diffusion provides an indication of the passivation quality. If the dopant diffusion is higher, the passivation quality is reduced due to stronger Auger recombination. The $iV_{OC}$ values obtained after the $SiN_X$/FGA hydrogenation for different duration of high-temperature annealing are compared as shown in **Figure 3.9**. The sample with the optimal annealing time of 15 minutes shows slightly better passivation among all the samples, with an $iV_{OC}$ of 658 mV. The sample with the longest annealing time of 60 minutes shows the lowest $iV_{OC}$ value of 645 mV. So, these two samples were taken for the ECV measurements to analyze the doping profiles. The doping profiles for these two samples obtained from the ECV measurements are

shown in **Figure 3.10**. The red curve indicates the doping profile of the sample with 15-minute annealing. The black curve indicates the doping profile of the sample with 60-minute annealing.

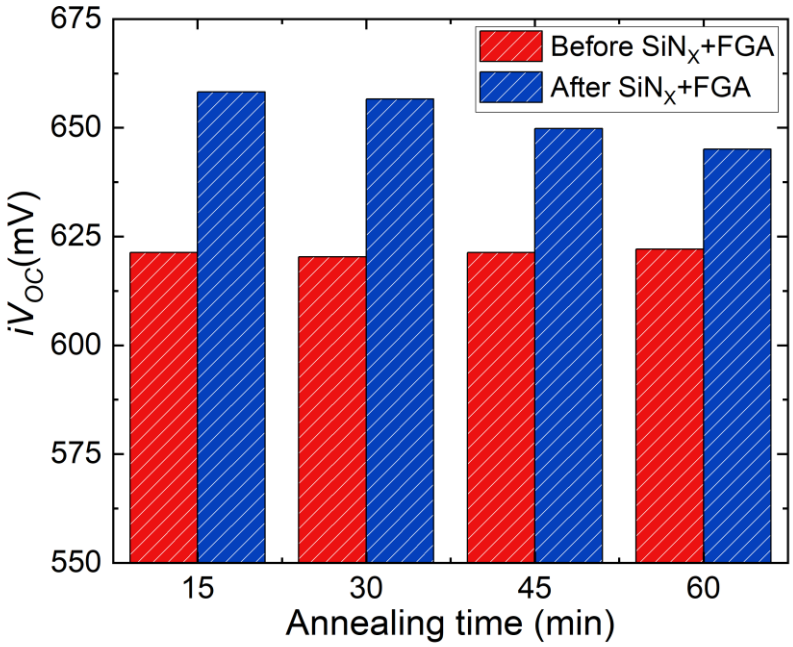


**Figure 3.9** Influence of post-annealing duration on $iV_{OC}$ of the $p^+$ poly-Si symmetric sample with doping gas flow ratio $SiH_4$-$B_2H_6$ = 20/15

There are three regions of interest in **Figure *3.10*** after the high-temperature annealing is performed. The doped poly-Si region up to 42 nm, the $SiO_X$ interface at 42 nm and the c-Si bulk region. The dotted line at 42 nm represents the $SiO_X$ - c-Si interface. The $iV_{OC}$ values obtained after the hydrogenation are also shown in the figure as an indication of the passivation quality.

The doping concentration of the 15-minute annealing sample is higher at the $SiO_X$ interface. The diffusion of boron into the c-Si bulk is also lower. This results in better passivation with an $iV_{OC}$ of 658 mV. With the increase in the duration of annealing, a higher boron diffusion into the c-Si bulk is observed. This explains the lower passivation as a consequence of Auger recombination. Weaker electric field due to much lower doping concentration at the $SiO_X$ interface also contributes to its lower passivation.

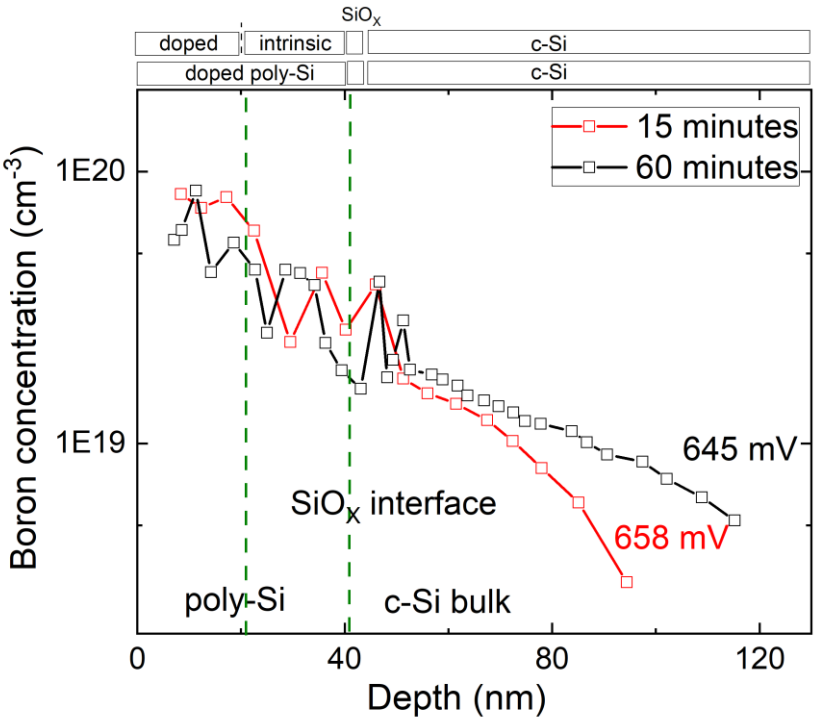


**Figure 3.10** Effect of different post-annealing duration on boron diffusion into c-Si bulk

From this, it is concluded that the optimal doping gas flow ratio for the p-type doped layers is $SiH_4$-$B_2H_6$ = 20/15 sccm. The optimal high-temperature annealing condition of 15 minutes at 850 °C remains unchanged. Thus, optimized thin $n^+$ poly-Si and $p^+$ poly-Si passivating contact are developed and it will be used in the fabrication of solar cell precursors.

## 3.3 Hydrogenation approach comparison for $n^+$ poly-Si and $p^+$ poly-Si contacts

Hydrogenation is performed to further enhance the passivation quality of the poly-Si symmetric samples and solar cell precursors. Different hydrogenation techniques are compared for the already optimized $n^+$ poly-Si and $p^+$ poly-Si symmetric samples. The schematic representation of the hydrogenated $n^+$ poly-Si symmetric sample, $p^+$ poly-Si symmetric sample, and solar cell precursor is shown in **Figure 3.11**.

Samples after the high-temperature annealing for 15 minutes at 850 °C are subjected to the hydrogenation to further enhance the passivation. The different hydrogenation approaches tried in this thesis are (i) $SiN_X$/FGA hydrogenation and (ii) $AlO_X$/RTP/$SiN_X$/$AlO_X$/FGA hydrogenation also known as ANA hydrogenation. Details of the hydrogenation processes can be found in *Section 2.2.9.*

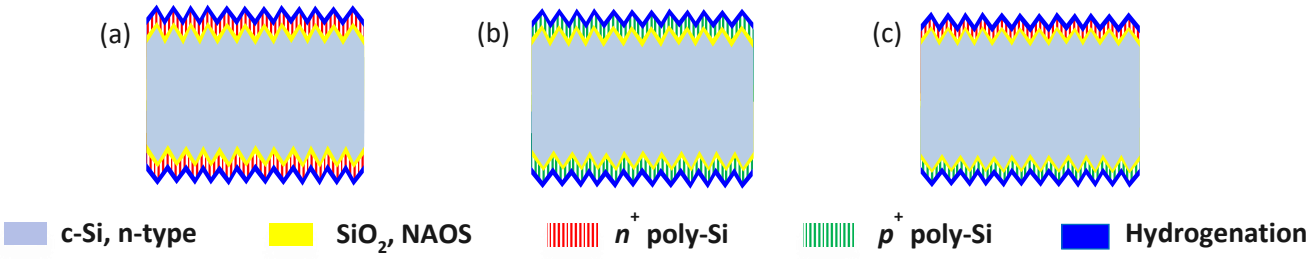


**Figure 3.11** Schematic representation of hydrogenated *(a)* $n^+$ poly-Si symmetric sample; (b*)* $p^+$ poly-Si symmetric sample and (c) solar cell precursor

### 3.3.1 Passivation optimization of symmetric samples

First, the effect of the above-mentioned hydrogenation techniques on the passivation quality of $n^+$ poly-Si and $p^+$ poly-Si symmetric samples are investigated. The $iV_{OC}$ values obtained after the different hydrogenation techniques are compared to check for a better increase in passivation quality.

**Figure 3.12** shows the $iV_{OC}$ values obtained after hydrogenation for two $n^+$ poly-Si symmetric samples. It can be observed that the $SiN_X$/FGA hydrogenation provides a higher increase in the passivation compared to the ANA hydrogenation. An increase of 12 mV in $iV_{OC}$ is observed after $SiN_X$/FGA hydrogenation. The sample with ANA hydrogenation observed a smaller increase in $iV_{OC}$ of 7 mV. Thus, the $n^+$ poly symmetric samples with $SiN_X$/FGA hydrogenation exhibited a higher increase in the passivation quality.

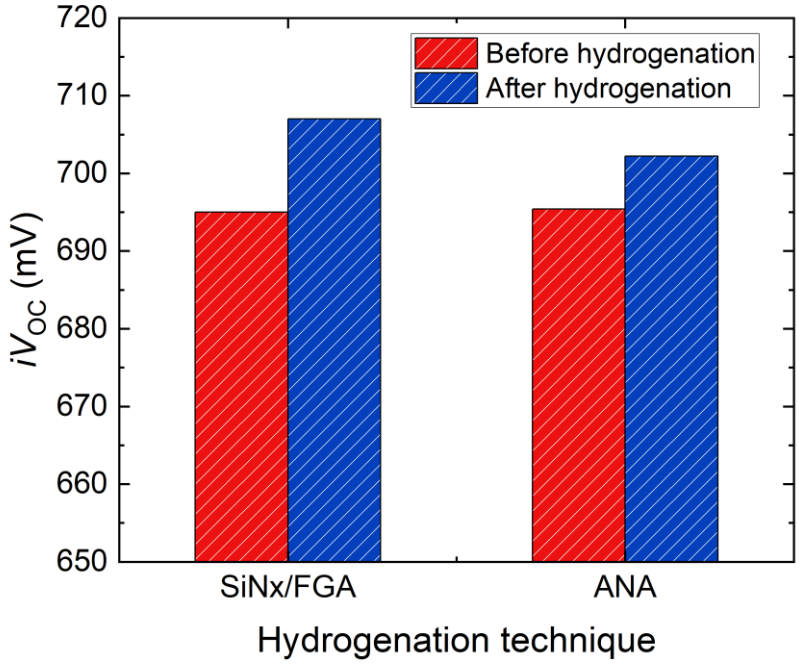


**Figure 3.12** $SiN_X$/FGA hydrogenation technique providing a higher increase *in* $iV_{OC}$ of $n^+$ poly-Si symmetric samples

Similarly, the $iV_{OC}$ values obtained after hydrogenation are compared for two symmetric $p^+$ poly-Si contact samples. The results are shown in **Figure 3.13**. The highest increase in $iV_{OC}$ after the hydrogenation is found to be for the sample with $SiN_X$/FGA hydrogenation ($\Delta\ iV_{OC}$ = 39 mV). ANA hydrogenated sample shows a relatively lower increase ($\Delta\ iV_{OC}$ = 32 mV). The $SiN_X$/FGA hydrogenation approach exhibited a higher increase in $iV_{OC}$ after hydrogenation.

The plots shown here are representative of the trends achieved for a large number of samples tested. This experiment is repeated on more symmetric samples and the same trend is observed. Thus, for both the $n^+$ poly-Si and $p^+$ poly-Si symmetric samples, the $SiN_X$/FGA hydrogenation provides a higher increase in passivation.

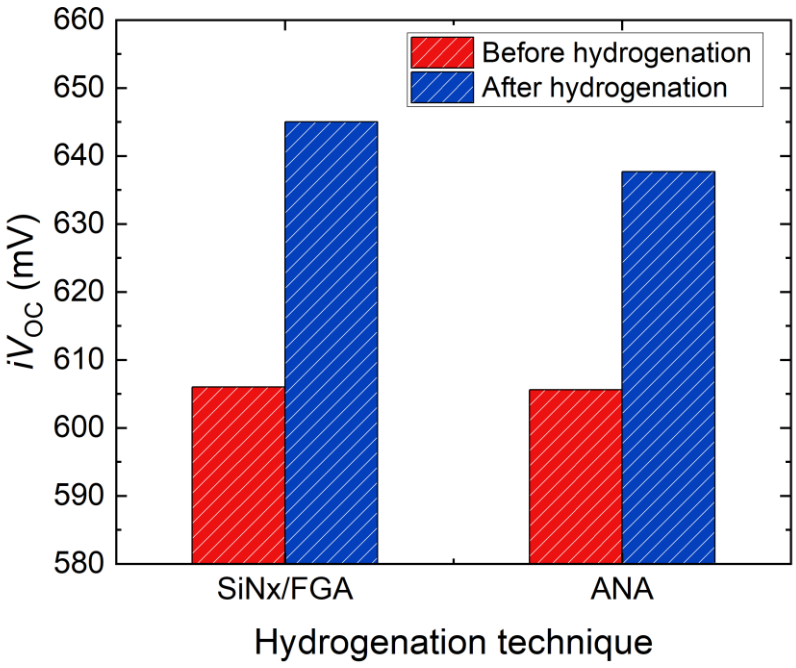


**Figure 3.13** $SiN_X$/FGA hydrogenation technique providing a higher increase in $iV_{OC}$ of $p^+$ poly-Si symmetric samples

### 3.3.2 Passivation optimization of solar cell precursors

The fabrication process of the solar cell precursors can be found in *Section 2.1.2*. Solar cell precursors with a 16 nm-thick *i/n* layer at the front and a 42 nm-thick *i/p* layer at the rear with doping gas flow rates as found in **Table *2.2*** are fabricated. The ensuing high-temperature annealing condition is performed for 15 minutes at 850 °C. Because of the relatively lower passivation quality of the $p^+$ poly-Si, the $iV_{OC}$ values achieved on the solar cell precursors before the hydrogenation are lower than expected. Thus, the hydrogenation step is performed to enhance the passivation quality.

The two hydrogenation approaches - $SiN_X$/FGA hydrogenation and ANA hydrogenation are tested on the fabricated solar cell precursors. This is done to compare their influence on the passivation of the solar cell precursors. **Figure 3.14** shows the $iV_{OC}$ values obtained after hydrogenation for two solar cell precursors. The trend observed in the symmetric samples, (see **Figure *3.12*** and **Figure *3.13***) is maintained for the solar cell precursors as well.

The solar cell precursor with $SiN_X$/FGA hydrogenation shows a higher increase ($\Delta\ iV_{OC}$ = 29 mV) in comparison to the solar cell precursor with the ANA hydrogenation ($\Delta\ iV_{OC}$ =21 mV). This experiment is repeated on more solar cell precursors. Every time, $SiN_X$/FGA hydrogenation provides a pronounced increase in $iV_{OC}$ compared to ANA hydrogenation. Hence, due to the lack of significant improvements in passivation quality and longer processing time, ANA hydrogenation is not considered in further fabrication process. Therefore, $SiN_X$/FGA hydrogenation technique will be used in the solar cell fabrication in this thesis. The best solar cell precursor observed $iV_{OC}$ as high as 692 mV.

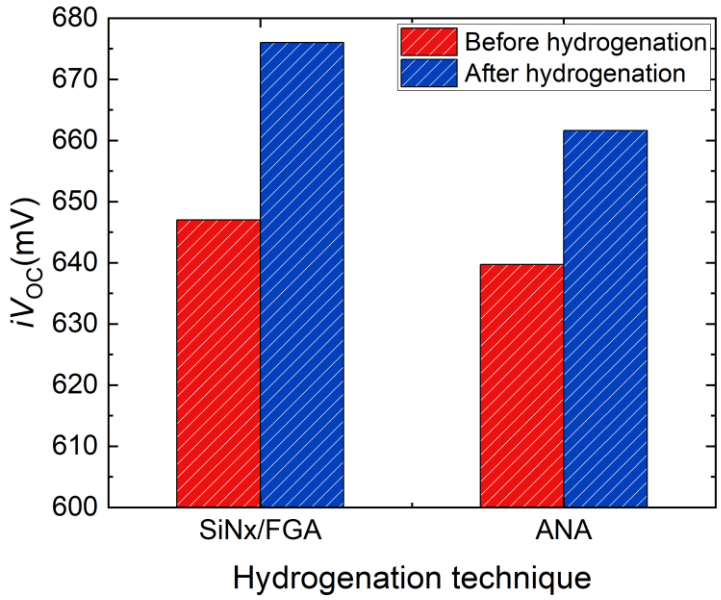


**Figure 3.14** $SiN_X$/FGA hydrogenation technique providing a higher increase in $iV_{OC}$ of solar cell precursors

## 3.4 Summary

This chapter focused on optimizing the passivation quality of the poly-Si passivating symmetric samples and solar cell precursors. The structure of the poly-Si carrier selective contact consists of an ultra-thin $SiO_X$ layer and a highly doped poly-Si layer. The silicon oxide layer was grown through wet chemical oxidation method of NAOS. On top of this $SiO_X$ layer, an intrinsic a-Si:H layer is deposited which is followed by a doped a-Si:H layer. Passivation tests were performed on the symmetric samples and solar cell precursors to optimize the intrinsic a-Si:H layer deposition, poly-Si layer thickness, and doping gas flow ratio of the *p*-type doped layer. The passivation was further enhanced by performing hydrogenation. The high-temperature annealing was done on all the test samples for 15 minutes at 850 °C in a $N_2$ atmosphere. The conclusions drawn from these optimization processes are as follows:

**Passivation quality of $n^+$ poly-Si passivating contacts:**

For the $n^+$ poly-Si symmetric samples, a variation of intrinsic a-Si:H layer deposition with the *n*-type doped a-Si:H layer was carried out. Passivation quality of symmetric test samples with no intrinsic layer and intrinsic layer deposition through PECVD, LPCVD were compared. Additionally, an intermediate annealing after the intrinsic layer deposition was performed on one of the test samples. For 16 nm-thick $n^+$ poly-Si symmetric sample, the intrinsic layer deposited using PECVD provided sufficiently high passivation quality of $iV_{OC}$ 713 mV.

**Passivation quality of $p^+$ poly-Si passivating contacts:**

A similar approach was also applied for the $p^+$ poly-Si symmetric samples. Symmetric passivation test samples were used for determining the optimal intrinsic layer deposition with *p*-type doped layers. Samples with intrinsic layer deposited through PECVD provided the best passivation results with $iV_{OC}$ 665 mV. But the passivation quality of the 16 nm-thick $p^+$ poly-Si symmetric samples was observed to be lower. To further improve the passivation quality, the thickness of $p^+$ poly-Si and the doping gas flow ratios of the p-type doped a-Si:H layers were varied.

(i) **Thickness variation:**

The influence of the thickness of the $p^+$ poly-Si symmetric samples was studied by varying the thickness of the *i/p* layers from 16 nm to 42 nm. Thicker poly-Si layers were not preferred since they induce significant parasitic absorption at device level. The subsequent TCO sputtering is known to severely damage the passivation quality of thin poly-Si layers below 40 nm. Best passivation of the solar cell precursor was achieved with 42 nm-thick $p^+$ poly-Si layers.

(ii) **Doping gas flow variation with ECV:**

The previously used doping gas flow ratio for the deposition of the p-type doped a-Si:H layers was $SiH_4$-$B_2H_6$ = 20/15. This was varied from 31/4 to 10/25, to study its influence on the passivation quality. ECV measurements were carried out for these different doping gas flow ratios to investigate the doping profiles. Lower doping level resulted in lower passivation quality due to reduced field-effect surface passivation. Higher doping resulted in increased boron diffusion into the c-Si bulk, thus resulting in low passivation quality. It was observed that the previously used doping gas flow ratio of 20/15 provided the highest $iV_{OC}$ of 658 mV.

(iii) **Influence of post-annealing time:**

The symmetric samples with the optimum doping gas flow ratio $SiH_4$-$B_2H_6$ = 20/15 were further analyzed for the different post-annealing duration. This was done to study the influence of annealing time on the diffusion of boron which indicates the passivation quality. ECV measurements were carried out on the samples annealed for different duration. It was observed that with a longer annealing time, the passivation quality reduced due to increased boron diffusion. Hence, the duration of high-temperature annealing was maintained at 15 minutes.

**Passivation quality enhancement by hydrogenation:**

The passivation quality of the $n^+$ poly-Si symmetric samples and the $p^+$ poly-Si symmetric samples were further enhanced by performing hydrogenation. Two hydrogenation techniques - $SiN_X$/FGA hydrogenation and ANA hydrogenation were compared to check for better increase in passivation quality. $SiN_X$/FGA hydrogenation involved deposition of a 75 nm-thick $SiN_X$ layer at 400 °C using PECVD followed by forming gas annealing for 30 minutes at 400 °C. ANA hydrogenation involves deposition of a triple capping layer of $AlO_X$/$SiN_X$/$AlO_X$ followed by RTP-FGA. $AlO_X$ layers were deposited using ALD at 105 °C. The RTP annealing was done at 600 °C for 10 minutes. The hydrogenation tests were performed on symmetric samples. A higher increase in passivation quality of $n^+$ poly-Si symmetric samples and $p^+$ poly-Si symmetric samples was observed from $SiN_X$/FGA hydrogenation. The experiment was repeated on more symmetric samples and the trend observed was similar.

**Passivation quality of the solar cell precursor:**

With the optimized results, solar cell precursors were fabricated with 16 nm-thick $n^+$ poly-Si layer at the front and 42 nm-thick $p^+$ poly-Si layer at the rear. The high-temperature annealing condition performed was 15 minutes at 850 °C in $N_2$ atmosphere. Similar to the trend observed in the symmetric samples, $SiN_X$/FGA hydrogenation provided a higher increase in the passivation quality of the solar cell precursor. The trend was maintained when hydrogenation was performed on a large number of solar cell precursors. Due to the lack of significant improvements in the passivation quality and longer processing time, ANA hydrogenation was not considered in the fabrication of solar cell precursors. The best solar cell precursor with the ultra-thin poly-Si passivating contacts observed an $iV_{OC}$ of 692 mV.

# 4 Copper-plated bifacial poly-Si solar cells

This chapter discusses the fabrication process and results of double-side textured bifacial copper-plated poly-Si solar cells. Transparent conducting oxide (TCO) layers are deposited on the hydrogenated cell precursors through sputtering. This sputtering process is known to degrade the passivation quality of the thin poly-Si contacts. *Section 4.1* discusses the methods used to recover the passivation quality after TCO sputtering. Subsequently, the copper-plating metallization process is carried out. *Section 4.2* shows the results of the bifacial copper-plated poly-Si solar cells. *Section 4.3* looks into the different approaches that are employed to improve solar cell performance. Lastly, the findings from this chapter are summarized in *Section 4.4*.

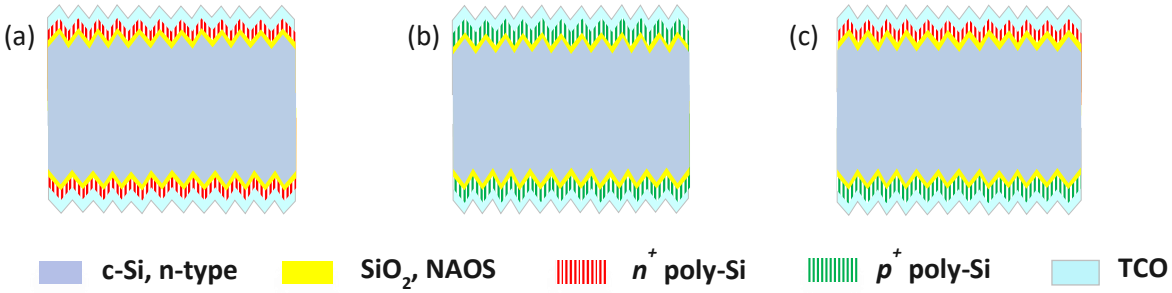


**Figure 4.1** Schematic representation of ITO sputtered (a) $n^+$ poly-Si symmetric samples; (b) $p^+$ poly-Si symmetric samples and (c) solar cell precursor

## 4.1 Post-annealing treatment tests after TCO sputtering

Thin poly-Si layers are deposited to avoid significant parasitic absorption. But it is not enough to provide sufficient lateral carrier transport to the metal grids [38], [62]. Therefore, TCO layers are deposited to provide the necessary lateral conductivity of charge carriers. It also acts as anti-reflection coatings [64]. The sputtering process for the TCO layers is explained in *Section 2.2.10*.

Sputtering is a highly scalable and well-established technique in the manufacturing of solar cells. One of the drawbacks of this technique has been its degrading effect on the passivation quality of thin poly-Si based solar cell precursors. The poly-Si contacts are stable at high temperatures. Curing at temperatures around ~350 °C after the TCO sputtering is reported to recover the passivation quality[38], [62].

It was reported by Han et.al in [62] that post-deposition annealing treatment (PDA) at 400 °C for 60 minutes in a $H_2$ atmosphere, can effectively help in recovering the passivation damage induced during TCO deposition. Therefore, post-annealing treatments are tried to recover the TCO sputtering damage.

ITO layers are used as TCO in this thesis. Before directly depositing the ITO layers on the solar cell precursors, ITO layers are applied on the symmetric samples with $n^+$ poly-Si and $p^+$ poly-Si layers as shown in **Figure 4.1 (a)** and **Figure 4.1 (b)**. This is done to get an estimate of passivation loss. Previously optimized $n^+$ poly-Si and $p^+$ poly-Si symmetric samples with $SiN_X$/FGA hydrogenation are used for this test. As mentioned in *Section 2.1.2*, a BHF and 0.55% HF etch is performed on the samples before the ITO layer is deposited. This is done to remove the $SiN_X$ layer deposited during hydrogenation. The $iV_{OC}$ is measured using the Sinton WC-120 equipment before the ITO deposition as a reference for the passivation.

They are deposited at room-temperature using RF magnetron sputtering. 75 nm-thick ITO layers are deposited on both sides of the symmetric samples. After the deposition, the $iV_{OC}$ is measured to examine the passivation damage. Post-deposition annealing treatment in a $H_2$ atmosphere at 400 °C for 60 minutes is performed on the samples to check for recovery in passivation.

**Figure *4.2*** shows the $iV_{OC}$ values obtained on a $n^+$ poly-Si symmetric sample. The x-axis shows the different stages at which the $iV_{OC}$ measurements are made. Passivation of the sample without ITO, with ITO and the passivation recovery after post-deposition annealing, are shown. The drop in the passivation is indicated by the double-sided arrows for each step. A big drop in $iV_{OC}$ of 75 mV is observed after ITO deposition. When post-annealing treatment is performed on the sample, a recovery in $iV_{OC}$ of 23 mV is observed but the passivation loss is 52 mV.

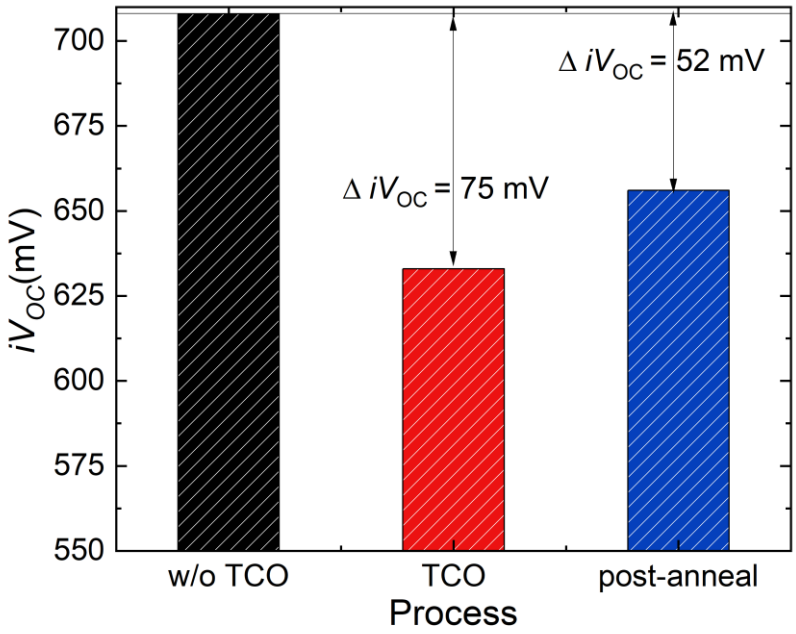


**Figure 4.2** $iV_{OC}$ drop due to standard ITO sputtering on $n^+$ poly-Si symmetric samples

When the test is performed on a $p^+$ poly-Si symmetric sample, the passivation loss is significant and is shown in **Figure *4.3***. The $p^+$ poly-Si layer seems to be more sensitive to the sputtering process. A massive drop in $iV_{OC}$ of 90 mV is observed after the ITO deposition. There is no notable recovery of the passivation after the post-deposition annealing at 400 °C for 60 minutes in a $H_2$ atmosphere.

When ITO layer is deposited on both sides of a solar cell precursor to check for the passivation loss, a big drop in $iV_{OC}$ of 91 mV is observed after the ITO deposition as shown in **Figure *4.4***. After the post-annealing treatment, there is a recovery in $iV_{OC}$ of 12 mV for the solar cell precursor. However, the passivation damage is still 79 mV. Thus, a different approach to reduce the passivation loss needs to be explored.

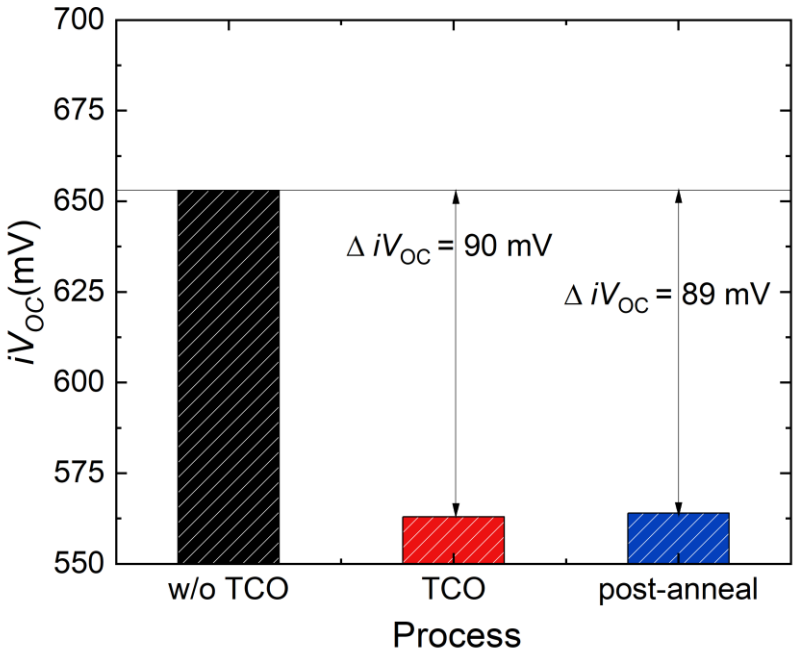


**Figure 4.3** Severe drop in $iV_{OC}$ due to standard ITO sputtering on $p^+$ poly-Si symmetric samples

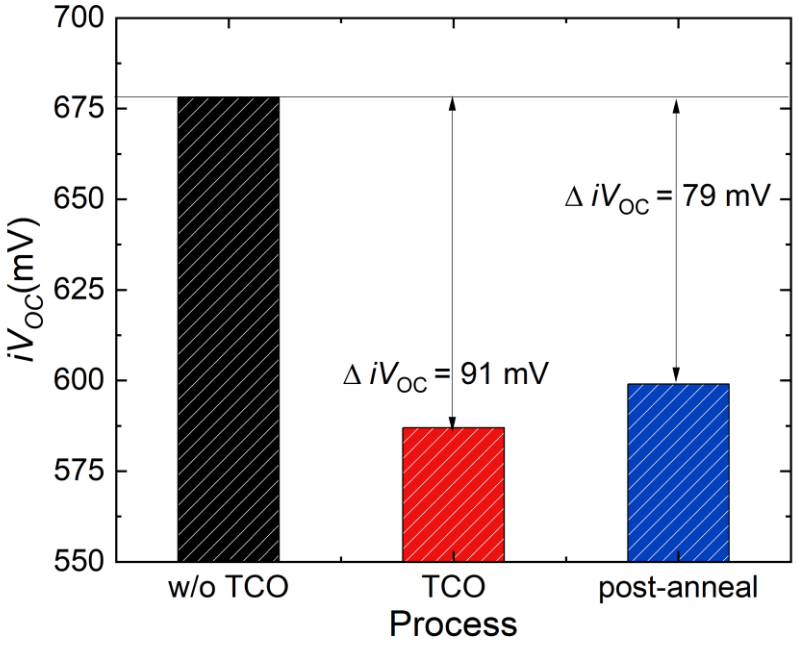


**Figure 4.4** Severe drop in $iV_{OC}$ due to standard ITO sputtering on solar cell precursor

The bombardment of particles during the sputtering might be a cause for the severe drop in passivation. It was reported in [38] and [61] that by changing the power density of the sputtering process, the bombardment could be reduced.

This Is done by employing a 2-step ITO sputtering process for depositing the 75 nm-thick ITO layer. This is achieved by reducing the power density of the sputtering process by 70% for the initial deposition of 20 nm-thick of ITO growth. It is followed by the standard sputtering recipe for deposition of the remaining 55 nm. If the power density is further reduced, the deposition rate is very low. The initial layer deposited at a lower power density is meant for protecting the poly-Si layer from the particle bombardment during the standard sputtering.

**Figure *4.5*** shows the passivation recovery of a solar cell precursor with ITO deposition using a 2-step ITO sputtering process. The drop in $iV_{OC}$ for the sample with soft ITO sputtering is lower than the drop observed for the sample with the standard ITO sputtering. With post-deposition annealing at 400 °C in $H_2$ atmosphere for 60 minutes, the passivation loss is further reduced to 39 mV. This recovery is better compared to the recovery with the standard ITO sputtering shown in **Figure *4.4***. It is worth noting that the $iV_{OC}$ value before the ITO deposition for the solar cell precursor used here (643 mV) is much lower compared to the solar cell precursor used for the standard ITO sputtering (678 mV).

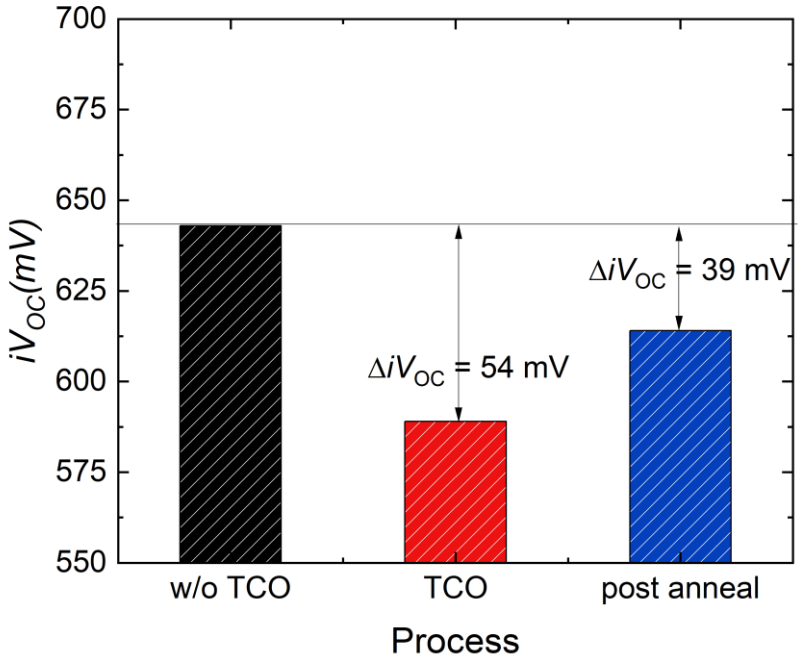


**Figure 4.5** Reduced $iV_{OC}$ drop after 2-step ITO sputtering on solar cell precursor

Hence, the passivation recovery is expected to be better when this 2-step ITO sputtering is performed on samples with better passivation quality. But due to reproducibility issues, the steep loss in passivation could not be recovered consistently. **Figure *4.6*** shows the passivation loss when the 2-step ITO sputtering is used on a different solar cell precursor with better passivation quality. A big drop in $iV_{OC}$ of 91 mV is observed. After the post-deposition annealing, the recovery is not significant. The passivation drop is still 72 mV.

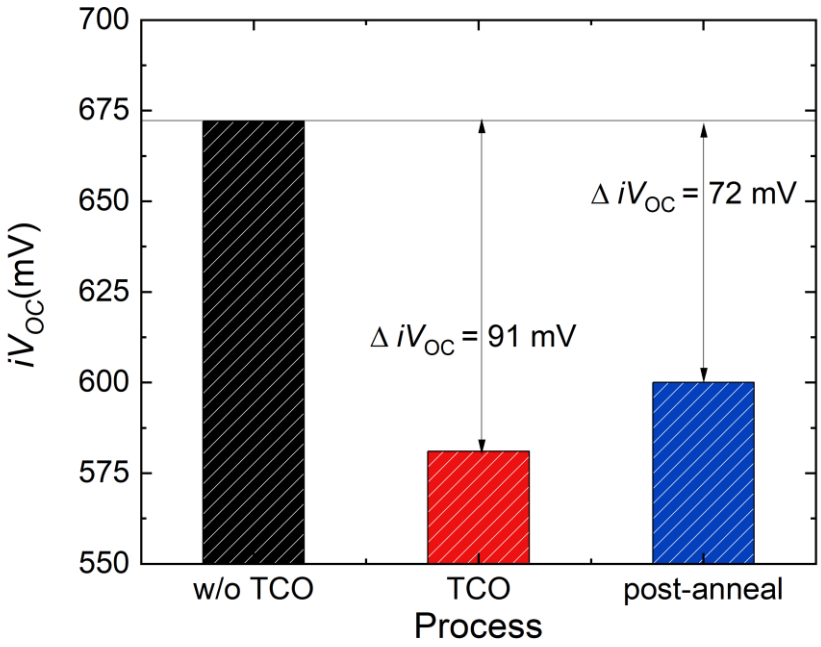


**Figure 4.6** Inconsistent $iV_{OC}$ recovery after 2-step ITO sputtering on a solar cell precursor with higher passivation quality

2-step ITO sputtering is used in the further fabrication of solar cells. But it is difficult to reproducibly recover such high passivation loss. To get an estimate of the solar cell parameters with this design of ITO layers on both sides, metallization was performed on the solar cell precursors to obtain a complete solar cell.

## 4.2 Bifacial copper-plating

Once the ITO layers are deposited on both sides, the next step in the fabrication process is metallization. Copper-plating is the metallization technique used in this thesis. It suppresses the consumption of silver and also enables to perform the metallization process at room temperature[42].

The fabrication process of the copper-plated bifacial poly-Si solar cells can be found in *Section 2.1.2*. A silver seed layer of 200 nm thickness is deposited through metal evaporation on both sides of the solar cell precursors with ITO. This process is followed by photoresist coating, exposure, and development as explained in *Section 2.2.12*. A 6-die pattern is obtained on the solar cell precursors. The copper-plating is then performed on these solar cell precursors. The copper-plating process is explained in *Section 2.2.13*. A two-step copper-plating recipe is utilized during this thesis.

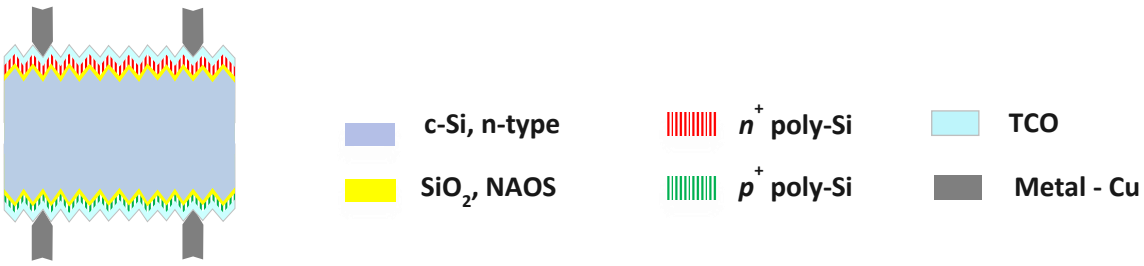


**Figure 4.7** Schematic representation of bifacial copper-plated solar cell with ITO on both sides

Before performing copper-plating on the solar cell precursors, it was done on test wafers with metal seed layers to estimate the height of the copper fingers grown. The *Dektak-150* profilometer is used to measure the height of the copper fingers. If the finger height is either too small or extremely high, the current-voltage and duration settings during copper-plating are changed. This is done to obtain the desired finger heights ranging from 15-20 µm. These finger heights are obtained for the settings of 0.35 V for 30 seconds and 0.4 A for 10 minutes during the copper-plating process. It is the optimum settings used in this thesis for bifacial copper-plating on the solar cell precursors. **Figure 4.7** shows a schematic representation of a bifacial copper-plated solar cell after the removal of the photoresist and the metal seed layer.

**Table 4.1 :** Solar cell parameters of the initial poly-Si solar cell (from *n*-side illumination)

| $iV_{OC}$ before ITO | $iV_{OC}$ after ITO | $V_{OC}$ (mV) | $J_{SC}$ (mA/cm$^2$) | *FF* (%) | $\eta$ (%) |
|---|---|---|---|---|---|
| 678 | 599 | 398 | 30.55 | 56.22 | 6.85 |

**Table *4.1*** shows the results of the solar cell with ITO on both sides. The performance of the solar cell is very low, especially the $V_{OC}$ and *FF*. The poor cell performance can be mainly attributed to the severe passivation loss caused by the ITO sputtering process, as well as a problematic selective carrier transport issue. As it can be seen, the $iV_{OC}$ before ITO layer deposition is much higher and the passivation drop experienced after the ITO deposition is 79 mV. Similar results were obtained on other solar cells with ITO on both sides.

This massive drop in passivation has resulted in very low solar cell parameters. In the following section, the solar cell performance is aimed to be improved by utilizing strategies that could stably minimize the sputtering damage from ITO deposition.

## 4.3 Solar cell performance improvement

To reduce the ITO sputtering damage, two strategies are developed. (1) Introduction of buffer layers on the $p^+$ poly-Si side to reduce the passivation damage. (2) Fabricating TCO-free $n^+$ poly-Si side to avoid the passivation damage. These two modifications are tested on the solar cell precursors to check for improvement in the solar cell performance.

### 4.3.1 $p^+$ poly-Si side with MoO*x* buffer layer

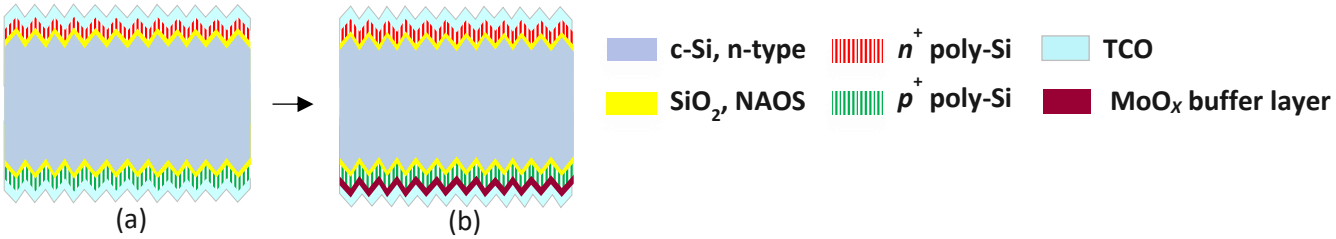


**Figure 4.8** Schematic representation of solar cell precursor (a)With ITO on both sides; (b) With $MoO_X$ buffer layer on $p^+$ poly-Si side

The molybdenum oxide ($MoO_X$) buffer layer has normally been utilized as a hole-selective contact due to its high work function [80],[81]. It has been reported as an effective buffer layer to reduce the ITO sputtering-induced passivation damage in perovskite solar cells [61]. This layer is deposited on the $p^+$ poly-Si side before the ITO layer. Metal evaporation technique is employed for this buffer layer

deposition. It helped in maintaining better passivation quality of the solar cell precursors after ITO sputtering. To determine the optimal thickness of the $MoO_X$ buffer layer, tests are done on solar cell precursors by depositing different thicknesses of the $MoO_X$ layer. The $n^+$ poly-Si side of the solar cell precursor had a 75 nm-thick ITO layer and no other changes are made on the $n^+$ poly-Si side.

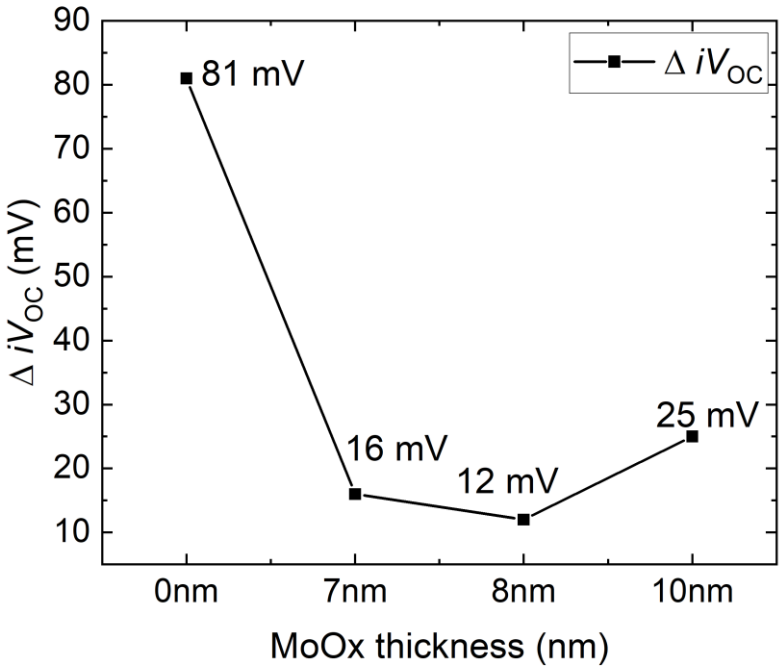


**Figure 4.9** $MoO_X$ buffer layer reducing the ITO sputtering-induced $iV_{OC}$ drop

**Figure *4.9*** shows the passivation recovery by the introduction of the $MoO_X$ buffer layer. The difference in $iV_{OC}$ values before ITO sputtering and after ITO sputtering are compared. Three cell precursors with different $MoO_X$ buffer layer thicknesses 7 nm, 8 nm, 10 nm are used. One cell precursor without the buffer layer is kept for reference.

For the cell precursor without the $MoO_X$ buffer layer, a high loss in passivation of 81 mV is observed. With the introduction of this buffer layer, the drop $iV_{OC}$ after ITO deposition is significantly reduced to 25 mV. It also slightly improved the minority carrier lifetime and recombination current density of the solar cell precursors. The lowest passivation drop of 12 mV is was observed for the solar cell precursor with an 8 nm-thick $MoO_X$ buffer layer.

With this $MoO_X$ buffer layer, the passivation loss after ITO sputtering was reduced from 91 mV (as observed in **Figure *4.6***) to 12 mV without any post-deposition annealing treatments. This result of obtaining a low passivation drop with an 8 nm-thick $MoO_X$ buffer layer is reproducible in other cell precursors. Therefore, a $MoO_X$ buffer layer of 8 nm thickness will be deposited on the $p^+$ poly-Si side in further fabrication.

After the deposition of this buffer layer, the ITO layers are deposited using the 2-step sputtering process. No post-deposition annealing treatments are performed. The other processes followed in the fabrication of a complete solar cell - metal seed layer deposition, photolithography, and copper-plating remain the same.

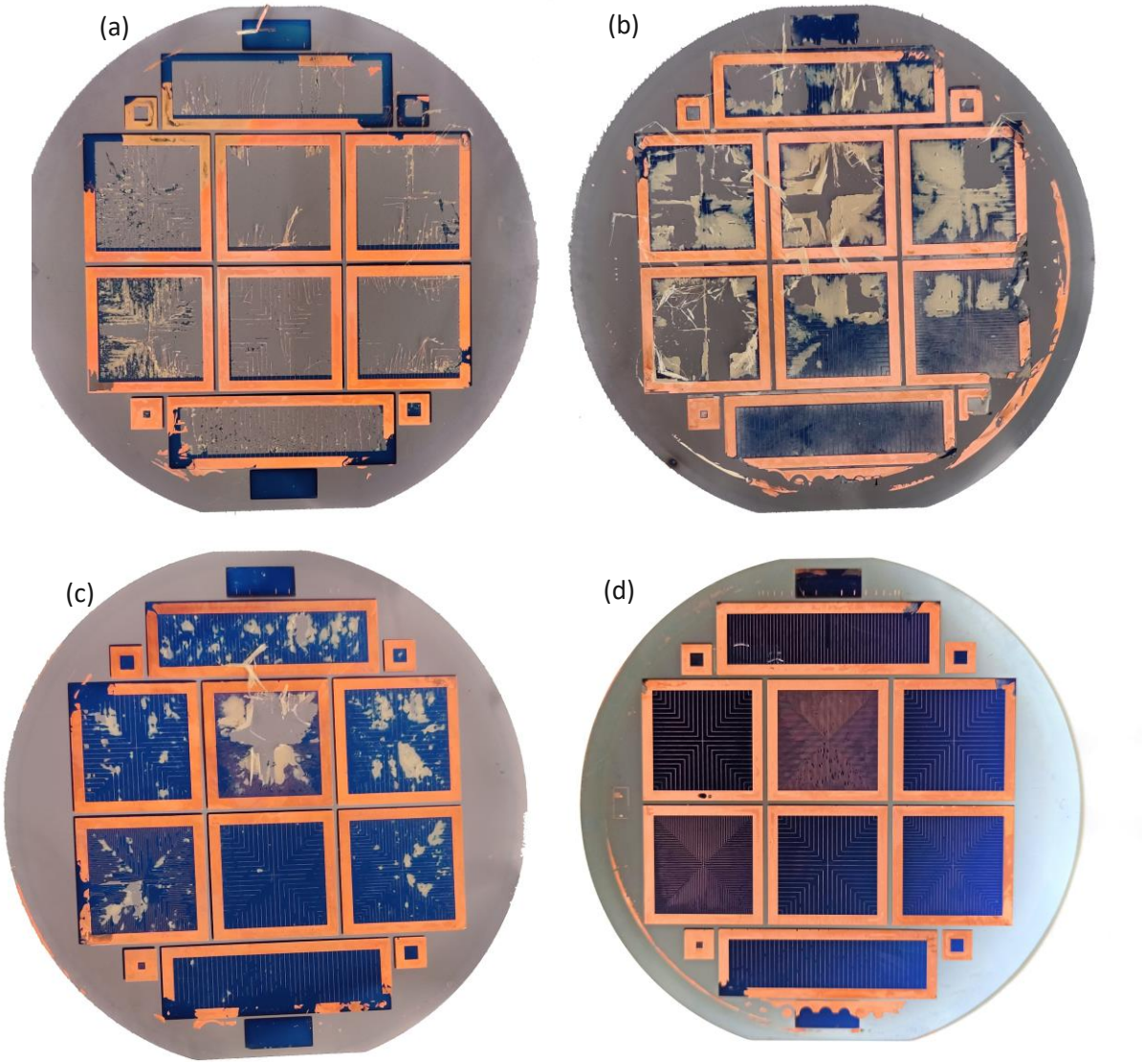


**Figure 4.10** $MoO_X$ reacting with seed layer removal solution. Step-by-step changes made in solution and approach to obtain well-plated $p^+$ poly-Si side of the solar cell

While removing the metal seed layer, it is observed that the $MoO_X$ reacts with the solution for seed layer removal. The standard seed layer removal solution consists of 200 ml DI water, 50 ml of 31 % hydrogen peroxide ($H_2O_2$), and 12.5 ml of 28 % ammonium hydroxide ($NH_4OH$). From **Figure 4.10 (a)**, it is seen that the copper fingers along with the ITO and $MoO_X$ layers are etched away.

Air-annealing treatment on the cell precursors after the ITO layer deposition is carried out at 180 °C for 10 minutes to reduce the strong reactions with the solution for seed layer removal. But it resulted in the formation of flake-like particles as shown in **Figure *4.10* (b)**. The volume of the solution used for seed layer removal is altered. Broken copper-plated test samples are used in this process. Diluting the seed layer removal solution reduced the flake-like particles. An aqueous solution of 300 ml DI water, 50 ml of 31 % hydrogen peroxide ($H_2O_2$), and 12.5 ml of 28 % ammonium hydroxide ($NH_4OH$) is used for the seed layer removal. As seen in **Figure *4.10* (c)**, the etching of copper-fingers and the ITO layer is reduced. But the formation of flakes could not be fully prevented. This meant that the solar cell is still not usable.

Every time during seed layer removal, the solar cell is completely immersed in the seed layer removal solution. To avoid the flake-like particles, a new step-by-step approach is introduced. The broken copper-plated test samples are immersed in the solution for a short time (maximum 3 seconds) and immediately rinsed with DI water. This step-by-step approach is then tested on the copper-plated solar cells. With the additional air-annealing treatment and step-by-step approach for removing the seed layer, a well-plated $p^+$ poly-Si side of the cell is obtained similar to the cell shown in **Figure *4.10* (d)**. This approach produced well-plated $p^+$ poly-Si side on other solar cells as well.

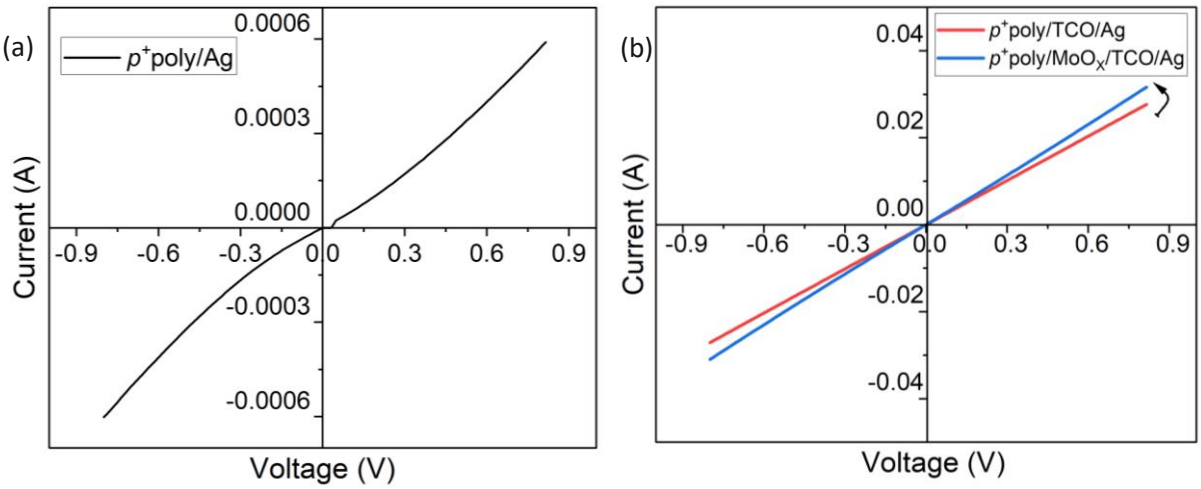


**Figure 4.11** I-V measurements of *p* contact side; (a) $p^+$ poly-Si sample with only silver seed layer and (b) Influence of TCO and $MoO_X$ buffer layer on the $p^+$ poly-Si sample

Additionally, vertical I-V measurements are performed on the symmetric samples based on the p-type wafer. This is done to understand the contact behaviour on the *p* contact side. The silver seed layer is deposited directly on the $p^+$ poly-Si layer using a hard mask to obtain the desired pattern. Measurements are taken on this sample with $p^+$ poly-Si/Ag. A non-ohmic contact feature is observed on the sample with metal directly contacting the $p^+$ poly-Si layer, as shown in **Figure *4.11* (a)**. When the ITO layer is deposited on the $p^+$ poly layer and measurements are taken on this sample with $p^+$ poly-Si/ITO/Ag, an ohmic contact feature was observed. Upon introducing the 8 nm-thick $MoO_X$ buffer layer between the $p^+$ poly-Si layer and TCO, the ohmic contact feature is observed. Also, the contact resistance measured is lower for the sample with $MoO_X$ buffer layer, as shown in **Figure *4.11* (b)**. Thus, the introduction of the $MoO_X$ buffer layer maintains ohmic contact in addition to reducing the passivation damage.

### 4.3.2 $n^+$ poly-Si side with Ti/Ag seed layer for copper-plating

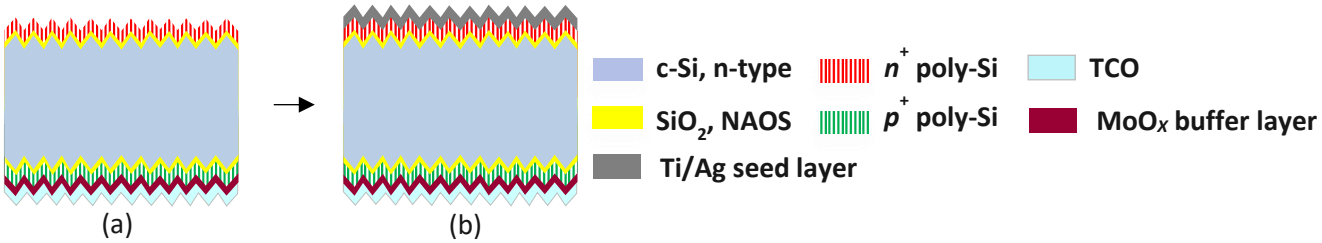


**Figure 4.12** Schematic representation of solar cell precursor (a)With TCO-free $n^+$ poly-Si side; (b) Addition of titanium to the silver seed layer to improve the adhesion

The TCO layers mainly contribute to the lateral conduction of charge carriers. For the $n^+$ poly-Si contact, a large portion of the lateral charge carrier transport to the front metal contacts can be

accomplished by the n-type c-Si bulk [25]. To avoid the sputtering-induced passivation damage on $n^+$ poly-Si layers, TCO-free $n^+$ poly-Si side is fabricated. The $p^+$ poly-Si side of the solar cell precursor consists of the additional 8 nm thick $MoO_X$ buffer layer. The other processes followed in obtaining a complete solar cell - metal seed layer deposition, photolithography, and copper-plating remain the same.

While removing the seed layer, it is observed that the copper fingers and busbars are peeling off from the $n^+$ poly-Si side of the solar cell. This is shown in the left of **Figure *4.13***. The adhesion of copper can be improved by adding a thin layer of titanium with the silver seed layer. A thin layer is preferred since the resistivity of titanium is higher than that of silver [82]. Titanium has been reported to have better adhesion and contacting properties [40]. Due to its availability and ease of incorporating into the existing fabrication process, it is deposited along with silver as the metal seed layer.

An arbitrary 8 nm-thick titanium layer was deposited through electron-beam evaporation. To maintain the overall seed layer thickness of 200 nm, the thickness of the silver seed layer to be deposited is reduced to 192 nm. When Ti/Ag seed layer is deposited on the TCO-free $n^+$ poly-Si side, a well-plated $n^+$ poly-Si side is obtained. This can be seen in the right of **Figure *4.13***. The previously used diluted seed layer removal solution also helps in removing the thin titanium seed layer along with silver.

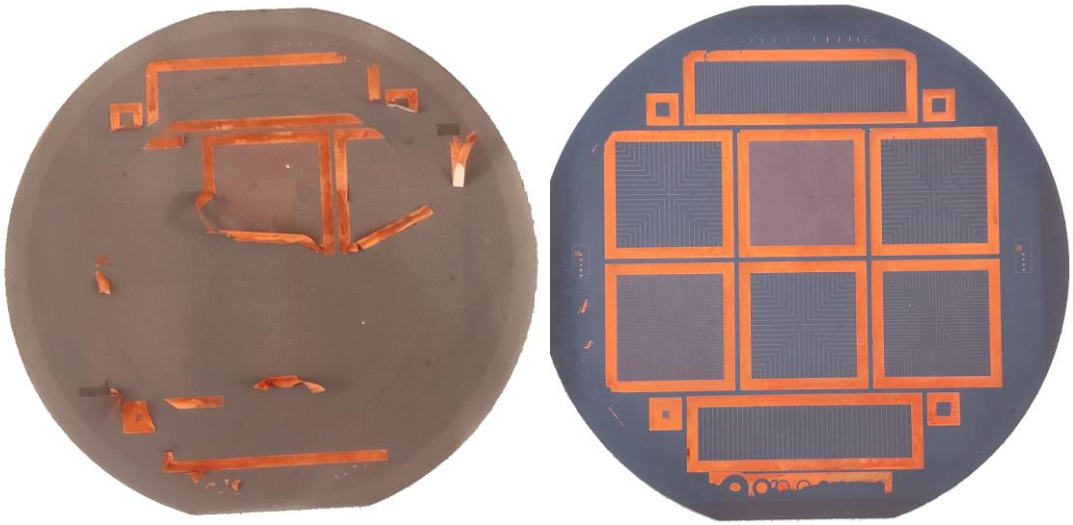

**Figure 4.13** Left: Poor adhesion of copper. Right: Better adhesion by introducing titanium with silver for the metal seed layer

Similar to the *p* contact side, vertical I-V measurements are performed on symmetric samples based on the n-type wafer, to understand the contact behaviour on the *n* contact side. The results are shown in **Figure *4.14***. Firstly, measurements are carried out on the sample with only the silver seed layer deposited on $n^+$ poly-Si layers. For the sample with metal directly contacting the $n^+$ poly-Si layers ($n^+$ poly-Si/Ag) indicated by the black curve, a non-ohmic contact feature is observed from the measurements. In another sample, an 8 nm-thick titanium layer is deposited with 192 nm-thick silver seed layer on the $n^+$ poly-Si layers. When measurements are taken for this sample with $n^+$ poly-Si/Ti/Ag, the contact feature observed is ohmic indicated by the red curve. This also validates that in addition to improving the adhesion, a thin layer of titanium is sufficient to improve the contact.

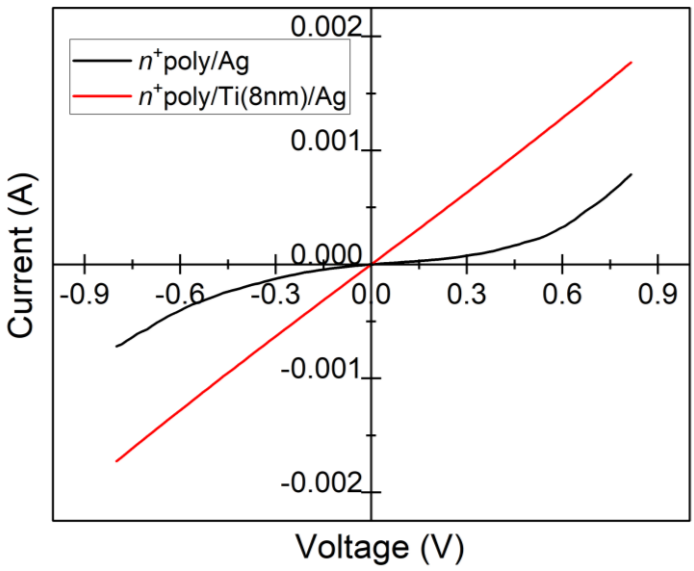


**Figure 4.14** Influence of titanium on I-V measurements of the *n* contact

Thus, improvements were made on both the $p^+$ poly-Si side and $n^+$ poly-Si side to reduce the ITO sputtering damage on the passivation quality of the solar cell precursors. The next step is to fabricate complete solar cells with these modifications.

### 4.3.3 Solar cell results

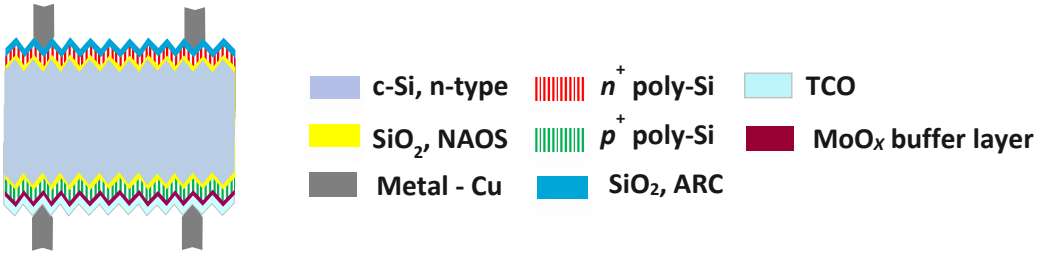


**Figure 4.15** Schematic representation of a double side textured copper-plated bifacial poly-Si solar cell after the modifications

With the improvements made on the $p^+$ poly-Si side and $n^+$ poly-Si side as mentioned in *Section 4.3*, complete solar cells are fabricated. As previously stated in *Section 2.2.10*, TCO layers also act as anti-reflection coatings (ARC). It helps in better light trapping on the illuminated side of the solar cell. Since both sides are illuminated in a bifacial cell, an anti-reflection coating is required on the TCO-free $n^+$ poly-Si side of the fabricated solar cell.

$SiO_2$ thin films deposited using electron-beam evaporation act as anti-reflection coatings [83]. 100 nm-thick $SiO_2$ ARC is deposited through e-beam evaporation on the $n^+$ poly-Si side. High purity $SiO_2$ granules are used as the source material. An already optimized recipe in the PVMD group is used for the ARC deposition. A steel mask is used to ensure that the ARC is deposited only on the active area of the solar cell. This is to avoid deposition on busbars which might cause contacting issues during J-V measurements. The complete copper-plated bifacial poly-Si solar cell obtained after the ARC deposition are shown in **Figure *4.16***.

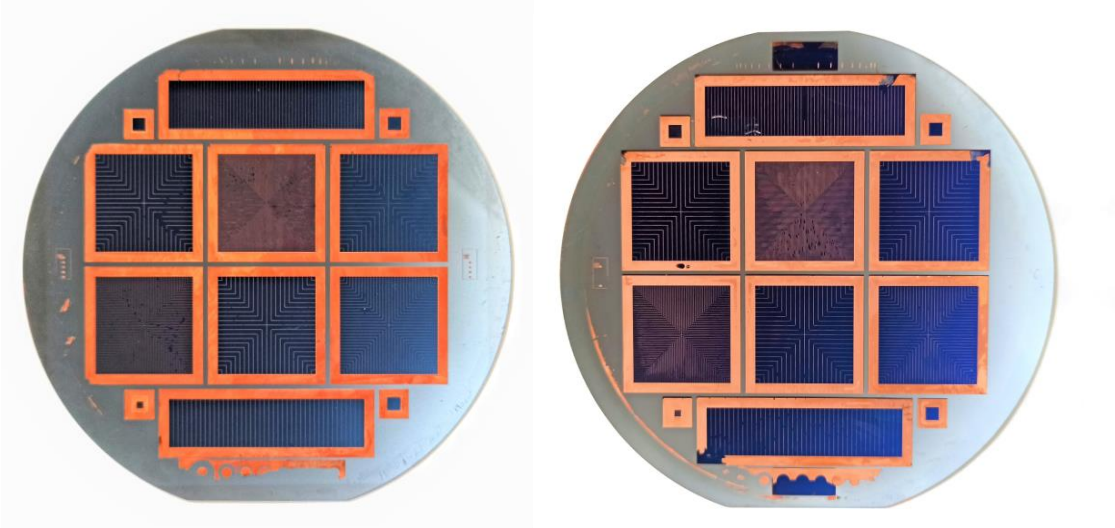

**Figure 4.16** Complete copper-plated bifacial poly-Si solar cell after the modifications. Left: TCO-free $n^+$ poly-Si side with anti-reflection coating. Right: $p^+$ poly-Si side with ITO

**Table 4.2 :** Improved solar cell results

| $iV_{OC}$ before ITO | $iV_{OC}$ after ITO | Illuminated side | $V_{OC}$ (mV) | $J_{SC}$ (mA/cm$^2$) | *FF* (%) | $\eta$ (%) |
|---|---|---|---|---|---|---|
| 671 | 654 | n | 610 | 36.95 | 64.98 | 14.64 |
| | | p | 607 | 35.27 | 64.57 | 13.83 |

**Table *4.2*** shows the results of the complete bifacial solar cell. The modified $n^+$ poly-Si side is TCO-free and consists of an 8 nm-thick titanium layer. The modified $p^+$ poly side consists of an 8 nm-thick $MoO_X$ buffer layer and a 75 nm-thick ITO layer.

The passivation loss after ITO sputtering is only 17 mV because of the introduction of the $MoO_X$ buffer layer. All the solar cell parameters have a significant increase with this improved contacting scheme. Higher $V_{OC}$ and *FF* values are observed, which in turn leads to better efficiency. This can be attributed to the better passivation quality after the ITO deposition. The J-V curves obtained by illuminating both the n-side and p-side of the solar cell are shown in **Figure *4.17***. A final efficiency of 14.64% and 13.83% is achieved on the n-side and p-side respectively.

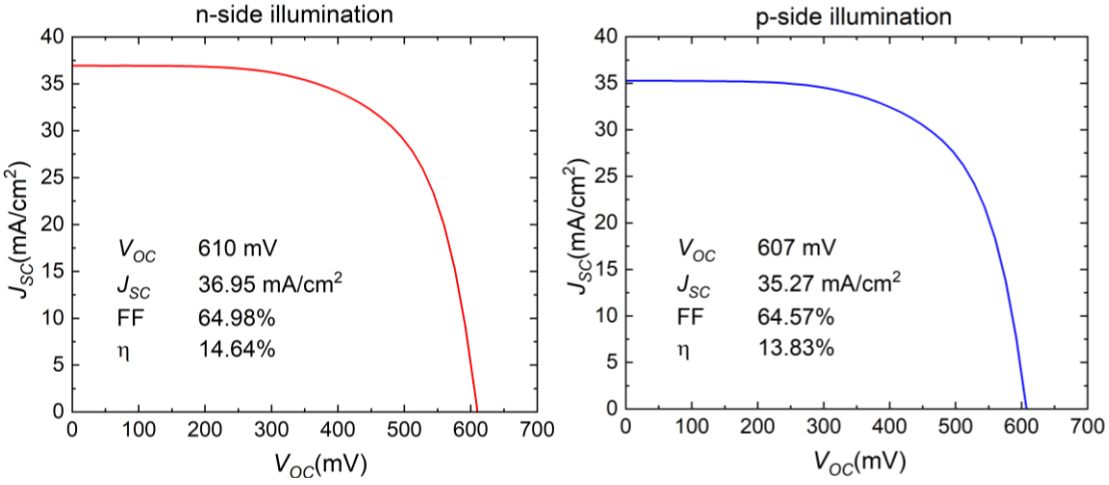


**Figure 4.17** Improved solar cell results with the introduction of titanium on the $n^+$ poly-Si side and $MoO_X$ on the $p^+$ poly-Si side

Since the resistivity of titanium is higher, thinner layers might be sufficient to provide the contact improvements. Thus, the thickness of the titanium layer is reduced and a thin layer of 2 nm is deposited. Improvements in the solar cell performance and contacting are checked. To maintain the overall metal seed layer thickness at 200 nm, the silver seed layer of 198 nm thickness is deposited. The rest of the fabrication process of the solar cell remain the same. A complete solar cell is fabricated with a 2 nm-thick titanium layer.

**Table 4.3 :** Comparison of solar cell parameters for different titanium layer thickness when illuminated on *n*-side

| Ti layer thickness | Illuminated side | $V_{OC}$ (mV) | $J_{SC}$ (mA/cm$^2$) | *FF* (%) | $\eta$ (%) |
|---|---|---|---|---|---|
| 8 nm | n | 610 | 36.95 | 64.98 | 14.64 |
| 2 nm | n | 611 | 36.16 | 69.58 | 15.38 |

**Table *4.3*** shows the comparison of the solar cell results obtained when different titanium layer thicknesses are used. Since the modification is done on the *n*-side of the solar cell, only the illuminated *n*-side results are shown. The reduction in titanium thickness provides an absolute 4.6 % gain in *FF*. As a result, there is an absolute 0.74% gain in efficiency. The efficiency achieved is 15.38%. The bifaciality factor is calculated to be 89%.

To understand the reason behind the increase in *FF*, vertical resistance measurements between the metal layers and silicon bulk are performed. Two symmetric $n^+$ poly-Si contact samples with Ti/Ag seed layers are taken for the measurements. The thickness of titanium layers are 8 nm and 2 nm respectively. The curves obtained from the current-voltage measurements for both the samples are shown in **Figure *4.18***. The ohmic contact feature is observed for both samples.

The inverse of the slope of the curves indicates the resistance values. For the sample with an 8 nm-thick titanium layer indicated by the red curve, the slope is small, resulting in higher resistance. For the sample with the 2 nm-thick titanium layer shown by the blue curve, the slope is higher hence lower resistance. This reduced resistance observed from the contacting behaviour tests is the reason for the improvements in FF. Hence, better efficiency is achieved in the sample with the 2 nm-thick titanium layer.

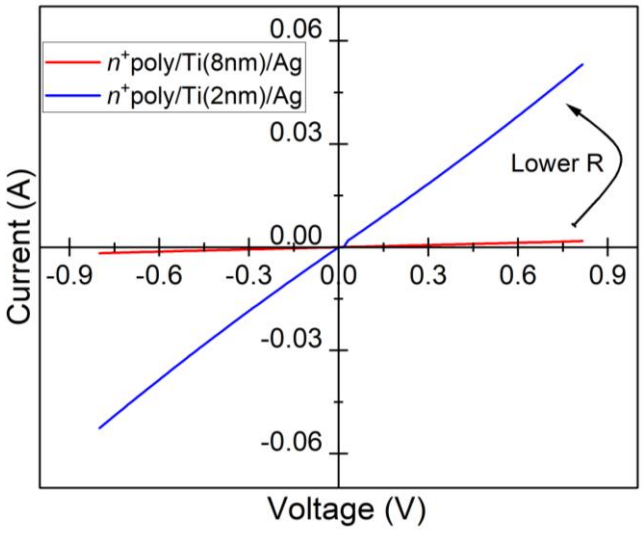


**Figure 4.18** Influence of reduced titanium thickness on I-V measurements of *n* contact side

## 4.4 Summary

This chapter discussed the fabrication of double-side textured bifacial copper-plated poly-Si solar cells by addressing the TCO sputtering-induced passivation damage and optimizing the copper-plating process. Symmetric samples and solar cell precursors were subjected to post-deposition annealing treatments at 400 °C for 60 minutes after the ITO sputtering. But severe passivation loss was noticed on both the $n^+$ poly-Si side and the $p^+$ poly-Si side. A 2-step ITO sputtering was developed and used on the cell precursors. But such high passivation loss was difficult to reproducibly recover. A bifacial copper-plated solar cell with ITO on both sides was fabricated. The initial solar cell parameters were: $V_{OC}$ 398 mV, *FF* 56.22 %, $J_{SC}$ 30.55 mA/cm$^2$ and $\eta$ 6.85 % (from *n*-side illumination).

Strategies on improving the solar cell performance were devised individually for the $n^+$ poly-Si side and the $p^+$ poly-Si side. 8 nm-thick $MoO_X$ buffer layer was introduced on top of the $p^+$ poly-Si layer to maintain a better passivation quality after ITO sputtering. It helped in reducing the drop in $iV_{OC}$ after ITO deposition from 91 mV to 12 mV. Strong reactions of the $MoO_X$ buffer layer with the solution for seed layer removal etched the copper fingers and formed flake-like particles. The solution for seed layer removal was diluted and a step-by-step approach while removing the seed layer resulted in a well-plated $p^+$ poly-Si side.

Regarding the $n^+$ poly-Si side, it was decided to fabricate TCO-free $n^+$ poly-Si contact to avoid the passivation damage due to sputtering. An additional 8 nm-thick titanium seed layer was used in combination with silver to maintain better adhesion of copper on the $n^+$ poly-Si side.

These modifications contributed to improving the performance of solar cells. Adequate passivation quality was maintained and also the solar cell performance was enhanced significantly. The solar cell results were improved to be: $V_{OC}$ 610 mV, *FF* 64.98 %, $J_{SC}$ 36.95 mA/cm$^2$ and $\eta$ 14.64 % (from *n*-side illumination).

Further reduction in titanium layer thickness was performed since thinner Titanium layers were sufficient to improve the contacting. It boosted the *FF* by 4.6 %, as a consequence of lower resistance obtained during the contacting behaviour tests. The best performing solar cell was achieved with the 2 nm-thick titanium layer. The solar cell performance is: $V_{OC}$ 611 mV, *FF* 69.58 %, $J_{SC}$ 36.16 mA/cm$^2$ and $\eta$ 15.38 % (from *n*-side illumination). The bifaciality factor was calculated to be 89 %.

# 5 Conclusions and Recommendations

This thesis project discussed the fabrication of double-side textured copper-plated bifacial poly-Si solar cells by developing ultra-thin poly-Si passivating contacts, addressing the TCO sputtering induced passivation damage and optimizing the copper-plating process. *Section 5.1* of this chapter summarizes the major findings from the experiments performed to achieve the thesis objectives. *Section 5.2* discusses some of the recommendations for future work.

## 5.1 Conclusions

The fabrication process of the double-side textured copper-plated bifacial poly-Si solar cell involved developing an ultra-thin poly-Si passivating contact, addressing the TCO sputtering induced passivation damage, and optimizing the copper-plating process. The structure of the poly-Si carrier selective contact consists of an ultra-thin $SiO_X$ layer and a highly doped poly-Si layer. The wet chemical oxidation method of NAOS was preferred for the growth of tunnel oxide layer. Intrinsic a-Si:H layers are deposited on top of the $SiO_X$ followed by the doped a-Si:H layers. High-temperature annealing was performed to crystallize the a-Si:H layers to poly-Si. Hydrogenation was performed to enhance the passivation quality of the poly-Si contacts. The conclusions are as follows:

**Ultra-thin poly-Si passivating contact optimization**

The main objective of this thesis project was to develop ultra-thin poly-Si passivating contacts. Passivation tests were carried out on textured symmetric samples with different deposition techniques for intrinsic a-Si:H layer growth with n-type doped layers. The deposition of the intrinsic a-Si:H layer was optimized. It was found that intrinsic a-Si:H layers deposited through PECVD provided the best passivation results. The high-temperature annealing condition was also optimized for the $n^+$ poly-Si contacts and the optimal annealing duration was 15 minutes at 850 °C. Thus, thin $n^+$ poly-Si contacts were developed. High passivation quality was achieved for the 16 nm-thick $n^+$ poly-Si symmetric samples with $iV_{OC}$ of 713 mV.

A similar process was followed for optimizing the deposition of intrinsic a-Si:H layer for developing thin $p^+$ poly-Si contacts. Intrinsic a-Si:H layers deposited through PECVD gave the best passivation results. The optimized high-temperature annealing condition for the $p^+$ poly-Si contacts was 15 minutes at 850 °C and it resulted in the highest $iV_{OC}$ of 665 mV. But the passivation quality of the 16 nm-thick $p^+$ poly-Si symmetric samples was significantly lower when compared to the passivation quality observed in $n^+$ poly-Si symmetric samples. This was due to boron diffusion, which is approved by doping profile measurement. Thus, further optimization of the $p^+$ poly-Si symmetric samples was carried out by varying the layer thickness and doping gas flow ratios.

The thickness of the $p^+$ poly-Si layer was optimized and it was found that sufficiently high passivation quality was achieved for the solar cell precursor with a 42 nm-thick $p^+$ poly-Si layer. With this optimum thickness, the doping gas flow ratio of the *p*-type doped layer on symmetric samples was optimized. ECV measurements were carried out to analyze the doping profiles for different doping gas flow rates. It was concluded that the sample with a doping gas flow ratio of $SiH_4$-$B_2H_6$ = 20/15 sccm provided the best passivation.

The hydrogenation approach was optimized to maximize the passivation quality of the poly-Si passivating contacts. For both the symmetrical passivation test samples and the solar cell precursors, two different hydrogenation approaches - $SiN_X$/FGA hydrogenation and ANA hydrogenation were tested. The symmetric samples were used to compare the passivation enhancement from the

different hydrogenation approaches. It was observed from the tests that $SiN_X$/FGA hydrogenation gave a higher increase in $iV_{OC}$. The same increasing trend in $iV_{OC}$ from $SiN_X$/FGA hydrogenation was also observed on the fabricated solar cell precursors.

Thus, implementing the $SiN_X$/FGA hydrogenation technique on the double side textured solar cell precursor resulted in excellent passivation quality indicated by the $iV_{OC}$. The best solar cell precursor with the ultra-thin poly-Si passivation contacts showed a high $iV_{OC}$ of 692 mV.

### Recovery of the TCO induced passivation damage

The second objective of this thesis project focused on addressing the passivation damage induced due to the TCO sputtering process. ITO was chosen as the TCO to be used due to an excellent trade-off between transparency and conductivity. Before depositing ITO on the fabricated solar cell precursors, ITO deposition was done on the textured symmetric samples with $n^+$ poly-Si and $p^+$ poly-Si layers. This was done to get an estimate of the drop in passivation indicated by the $iV_{OC}$.

A massive drop in passivation was observed for $n^+$ poly-Si and $p^+$ poly-Si symmetric samples. The $n^+$ poly-Si samples suffered a drop of 79 mV in $iV_{OC}$ and the $p^+$ poly-Si samples suffered a drop of 90 mV in $iV_{OC}$. To recover the passivation damage, post-deposition annealing treatment was performed. It was done for 60 minutes at 400 °C in a $H_2$ atmosphere. But the passivation loss after the post-annealing treatment was 52 mV for $n^+$ poly-Si samples and 89 mV for $p^+$ poly-Si samples. When ITO layers were deposited on solar cell precursors, the drop in passivation was 91 mV and the post-annealing treatments could not recover more than 12 mV.

To reduce the bombardment of the particles during ITO sputtering, a 2-step sputtering approach was considered for ITO deposition on solar cell precursors. This 2-step sputtering uses a 70 % lower power density for the 20 nm-thick initial ITO deposition followed by the 55 nm-thick bulk ITO layer with the standard sputtering process. This resulted in better recovery of the passivation loss after the post-deposition annealing.

### Working double-side textured bifacial copper-plated poly-Si solar cell

The third objective of this thesis project was to demonstrate a working double-side textured copper-plated bifacial poly-Si solar cell. Ag metal seed layer was deposited on the solar cell precursor to avoid the diffusion of copper into the silicon surface during copper-plating. The desired cell pattern was formed on the solar cell precursor using the photolithography process. Bifacial copper-plating was performed on solar cell precursors using an in-built copper-plating equipment. An optimized recipe was utilized for copper-plating with current-voltage setting of 0.35 V for 30 seconds and 0.4 A for 10 minutes. Finger heights in the range of 15-20 µm were obtained.

The initial solar cell parameters were: $V_{OC}$ 398 mV, *FF* 56.22 %, $J_{SC}$ 30.55 mA/cm$^2$ and $\eta$ 6.85 % (from *n*-side illumination). These low results were mainly due to severe passivation loss induced by the ITO sputtering. Due to the very low performance of the solar cell with ITO on both sides of the cell, modifications were made to improve the solar cell performance.

To reduce the severe passivation damage caused during the ITO sputtering process on the $p^+$ poly-Si side, a $MoO_X$ buffer layer was introduced. From suffering a massive drop in $iV_{OC}$ of 91 mV after ITO deposition, the $iV_{OC}$ drop was greatly reduced to 12 mV on solar cell precursors with an 8 nm-thick $MoO_X$ buffer layer on $p^+$ poly-Si side. It also helps in maintaining an ohmic contact in addition to reducing the ITO deposition-induced drop in passivation.

By applying this 8 nm-thick $MoO_X$ buffer layer on the $p^+$ poly-Si side before ITO deposition, complete solar cells were obtained after copper-plating. To prevent the strong reactions of the $MoO_X$ buffer layer with the standard solution for seed layer removal, air-annealing at 180 °C for 10 minutes after ITO deposition was performed. The flake-like particles formed was reduced by diluting the seed layer removal solution and a step-by-step seed layer removal approach was carried out to obtain well plated $p^+$ poly side of the solar cell.

To avoid the passivation damage due to ITO sputtering on the $n^+$ poly-Si side, TCO-free $n^+$ poly-Si side was fabricated. With the 8 nm-thick $MoO_X$ buffer layer on the $p^+$ poly-Si side before ITO deposition and TCO-free $n^+$ poly-Si side, complete solar cells were obtained after copper-plating. The poor adhesion of copper noticed after seed layer removal was solved by using an 8 nm-thick titanium in the metal seed layer. The desired ohmic contact feature was observed after adding titanium to the metal seed layer. It was found that by adding 8 nm-thick titanium layer, a well-plated $n^+$ poly-Si side of the solar cell was achieved.

With these modifications, the results of the solar cell were significantly improved. Illuminating from the *n*-side, the solar cell showed $V_{OC}$ 610 mV, *FF* 64.98 % $J_{SC}$ 36.95 mA/cm$^2$ and $\eta$ 14.64 %. Illuminating from the *p*-side, the solar cell showed $V_{OC}$ 607 mV, *FF* 64.57 %, $J_{SC}$ 35.27 mA/cm$^2$ and $\eta$ 13.83 %.

Since the resistivity of titanium is higher than silver, its thickness was reduced to 2 nm. A solar cell with a 2 nm-thick titanium layer was fabricated. It was observed that by reducing the thickness of titanium to 2 nm boosted the *FF* by 4.6 %. The best performing double-side textured copper-plated bifacial poly-Si solar cell was obtained with the 2 nm-thick titanium buffer layer. The solar results are: $V_{OC}$ 611 mV, *FF* 69.58 %, $J_{SC}$ 36.16 mA/cm$^2$ and $\eta$ 15.38 % (from *n*-side illumination). The bifaciality factor was calculated to be 89 %.

## 5.2 Recommendations

### On passivation quality improvement

To improve the performance of the solar cells, especially the $V_{OC}$, the passivation quality of the $p^+$ poly-Si layers could still be improved. Detailed material characterization of the doped poly-Si layers can be carried out. The deposition thickness of the p-type doped layer can be accurately measured using spectroscopic ellipsometry. Fourier Transform Infra-Red Spectroscopy (FTIR) measurements can be performed to analyze the microstructure of the deposited a-Si:H layers. By altering the microstructure of the deposited layers, the chemical passivation can be improved [74].

The TCO-induced sputtering damage severely degrades passivation especially for thin poly-Si layers on double side textured samples. Further investigation into the TCO sputtering process can be undertaken by testing different TCO materials and different TCO layer thicknesses to reduce the passivation damage.

### On alignment during exposure

For bifacial solar cells, it is necessary for the exposed patterns to be aligned on both sides of the solar cell precursor during the photolithography process. Currently, the alignment of the pattern on the solar cell precursors are done by manually creating markers before the metal seed layer deposition. This approach is time-consuming and manual marking is also not accurate. There are chances of pattern misalignment and this inconsistency in the alignment of the front and rear side patterns might affect the performance of bifacial solar cell. It will be difficult to analyse the solar cell parameters when corresponding dies in both sides of the cell are mismatched. Dedicated masks for aligning both sides accurately could help improve the fabrication process by minimizing the lithography process time.

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