A Short Range, Low Data Rate, 7.2 GHz-7.7 GHz FM-UWB Receiver Front-End

Yi Zhao, *Student Member, IEEE*, Yunzhi Dong, *Student Member, IEEE*, John F. M. Gerrits, *Senior Member, IEEE*, Gerrit van Veenendaal, John R. Long, *Member, IEEE*, and John R. Farserotu, *Senior Member, IEEE*

***Abstract*—A 9 mW FM-UWB receiver front-end for low data rate (<50 kbps), short range (<10 m) applications operating in the ultra-wideband (UWB) band centered at 7.45 GHz is described in this paper. A single-ended-to-differential preamplifier with 30 dB voltage gain, a 1 GHz bandwidth FM demodulator, and a combined (preamp/demodulator) receiver front-end were fabricated in 0.25 μm SiGe:C BiCMOS and characterized. Measured receiver sensitivity is −85.8 dBm while consuming 9 mW from a 1.8 V supply, and −83 dBm consuming 6 mW at 1.5 V. 15-20 m range line-of-sight in an indoor environment is realized, justifying FM-UWB as a robust radio technology for short range, low data rate applications. Multi-user and interference capabilities are also evaluated.**

***Index Terms*—FM-UWB, frequency modulation (FM), IEEE standardization, multi-user capacity, ultra-wideband (UWB) RF receiver front-end, voltage RF preamplifier, wideband FM demodulator.**

I. Introduction

ULTRA-WIDEBAND (UWB) technologies are poised to enable short-range wireless applications such as remote health and environmental monitoring, inventory control, and home/office/factory automation [1]. UWB systems have demonstrated greater robustness than traditional narrowband schemes to frequency-selective multipath and other types of interference caused by varying propagation conditions. The low transmit power permitted by regulatory authorities for unlicensed use extends battery life and eases coexistence with existing wireless communication systems. In addition, cost and size constraints envisioned for short-range applications require low-complexity RF interfaces, which can be provided by a UWB transceiver employing frequency modulation such as FM-UWB [2].

This paper describes a prototype FM-UWB receiver front-end (i.e., preamplifier and wideband FM demodulator) operating in the 7.2 GHz to 7.7 GHz (unlicensed) band that is available worldwide [3]. The principles underlying FM-UWB, and specifications used for subsequent development of the prototype receiver front-end are presented in Section II. Design and implementation of RF preamplifier, wideband FM demodulator and receiver front-end prototype are then detailed in Section III. Measurement results for the stand-alone blocks and complete FM-UWB receiver front-end are presented in Section IV. Concluding comments and areas identified for future work are outlined in Section V.

Manuscript received November 25, 2008; revised March 10, 2009. Current version published June 24, 2009. This work was supported in part by the European Sixth Framework project My Personal Adaptive Global NET (IST-507-102, "MAGNET Beyond").

Y. Zhao and J. R. Long are with Delft University of Technology, Delft, The Netherlands (e-mail: j.r.long @tudelft.nl).

Y. Dong is with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada.

J. F. M. Gerrits is with Delft University of Technology, Delft, The Netherlands, and also with the CSEM, Neuchâtel, Switzerland.

G. van Veenendaal is with the IC Lab, NXP Semiconductors, Eindhoven, The Netherlands.

J. R. Farserotu is with the CSEM, Neuchâtel, Switzerland.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2009.2020225

II. Constant-Envelope FM-UWB

Various UWB approaches are either in-use today or are being studied, addressing applications such as position localization [4], high data rate transmission, or robust communication [5]. New wireless applications such as health monitoring and body-area networks (BAN) require tetherless connectivity at data rates below 50 kbps, a range less than 10 m, and operational lifetime from a single battery charge for weeks or months. FM-UWB targets this level of performance, using a low-complexity implementation based upon wideband analog FM. The IEEE802.15 Task Group 6 (IEEE802.15.6) is currently developing a communication standard for body-area networks [6], where FM-UWB is a candidate for low data rate, medical BAN applications operating in the 7.2 GHz-9.5 GHz band. The full (PHY-MAC) proposal combines FM-UWB radio with an energy efficient, high availability protocol called WiseMAC [7].

A block diagram of the proposed FM-UWB transceiver is shown in Fig. 1. Transmit data is modulated using binary FSK with modulation index β_{SUB} onto a low-frequency sub-carrier, $\mathrm{m(t)}$ to create the constant-envelope FM-UWB transmit signal. Multiple users may share the same RF carrier, but distinguish themselves via different sub-carrier frequencies (FDMA) or other multiple access techniques (e.g., TDMA). The sub-carrier modulates the RF transmit oscillator directly (RF-VCO in Fig. 1), yielding an FCC-compliant constant-envelope UWB signal. A flat power spectral density and steep spectral roll-off is obtained when a triangular sub-carrier waveform is employed (as illustrated in Fig. 2 for $\mathrm{f_m} = \mathrm{f_{SUB}} = 1$ MHz and $\Delta \mathrm{f} = 250$ MHz).

The FM-UWB signal is demodulated without mixing, as shown in Fig. 1. The low complexity FM-UWB receiver consists of a high gain RF preamplifier, wideband FM demodulator, low-frequency downconversion and sub-carrier signal processing blocks (e.g., sub-carrier filtering, amplification, and FSK demodulation). Carrier synchronization is not required, and receiver synchronization is only limited by the bit synchronization time. Multiple users are demodulated by the sub-carrier processor, yielding multiple baseband data streams.

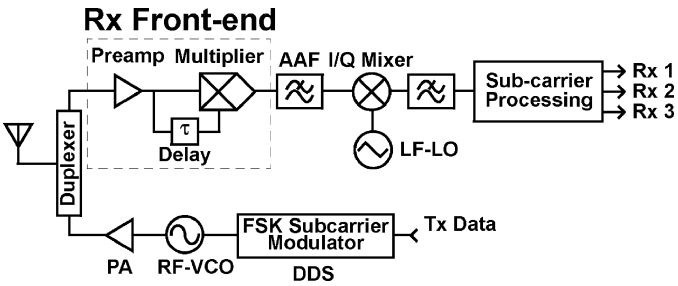


Fig. 1. FM-UWB radio transceiver architecture. (This work is highlighted by the dashed rectangle).

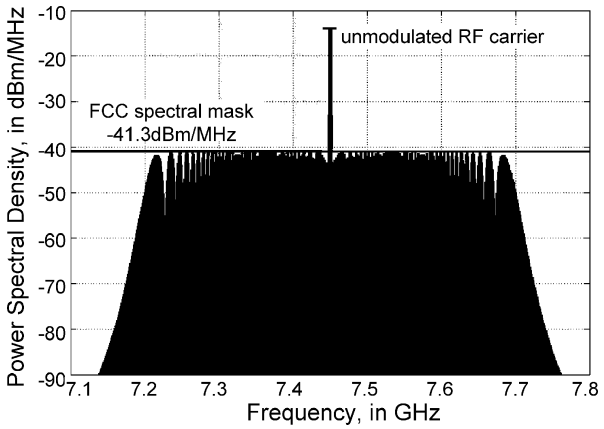


Fig. 2. Spectral density of the unmodulated carrier at 7.45 GHz and the FM-UWB signal obtained with $f_{SUB} = 1$ MHz and $\beta = 250$.

For example, ECG, EEG and SpO_2 data streams in a health monitoring application [8] would be demodulated as Rx 1, Rx 2, and Rx 3 in Fig. 1.

A. FM-UWB Receiver Front-End System Analysis and Prototype Specification

The FM-UWB radio demonstrator targets bit rate on the order of 50 kbps and a link span of 10 meters under free-space propagation conditions. For a 500 MHz wide FM-UWB signal limited to -41.3 dBm/MHz (as dictated by the FCC), the transmit power P_{TX} is -14.3 dBm. Assuming a free space propagation range of 10 m and 0 dBi gain antennas, the link loss is 70 dB at 7.45 GHz. For 500 MHz receiver front-end bandwidth, the thermal noise power at the receiver input is -87 dBm, with the difference between received signal and 50 Ω noise floor yielding 3 dB SNR. The minimum required SNR to obtain a bit error rate of 1×10^{-6} is -9 dB [2], implying an overall receiver noise figure better than 10 dB with 2 dB of margin for a prefilter and antenna switch. A wideband FM demodulator reported previously [9], demonstrated -46 dBm sensitivity (1.1 mV_{RMS}) in a 50 Ω system and 1.8 GHz bandwidth. We target 10 dB improvement in demodulator sensitivity for this work, thus an RF preamplifier with 25 dB-30 dB voltage gain and 5 dB noise figure is required.

Interference from other FM-UWB users must also be considered. Assuming that the worst-case interference scenario is another user 50 cm away, the interference level will be -58 dBm at the receiver in our proposed FM-UWB link. Simulations have shown that a 1 dB compression point (P_{1dB}) for the receiver front-end of -50 dBm is adequate given this level of interference and 30 dB voltage gain in the preamp. Given a 10 dB difference between gain compression and third-order intercept (IIP_3) points, an IIP_3 better than -40 dBm would avoid blocking of the desired signal at the receiver.

Target power consumption of the FM-UWB receiver front-end demonstrator is 10 mW from a 1.8 V supply. Low current consumption and high gain motivated the selection of a 0.25 μm SiGe:C-BiCMOS technology (NXP Semiconductors' QUBiC4X) for fabrication of the prototype [10].

III. Circuit Design

Design and implementation of the RF preamplifier and wideband FM demodulator, which comprise the prototype FM-UWB receiver front-end, are described in this section.

A. RF Preamplifier

We use the term preamplifier (or preamp) rather than low-noise amplifier for the receiver input stage, as gain at a given power consumption is emphasized more than low noise performance in the FM-UWB application. The RF preamplifier should realize 25–30 dB gain and 5 dB noise figure, assuming a minimum wideband demodulator sensitivity of -56 dBm (as specified in Section II-A). Target power consumption is 4 mW (or less) from a total budget of 10 mW for the receiver front-end when operating from a 1.8 V supply [11].

A single-ended input with better than 10 dB return loss when packaged is required for connecting to a 50 Ω single-ended antenna or preselect filter. Gain control via an AGC function with approximately 10 dB control range is also desired.

The active balun input stage (see Fig. 3) consists of common-base (CB) and common-emitter (CE) stages with paralleled inputs [12]. The inverting common-emitter (CE, Q_2) and non-inverting common-base (CB, Q_1) amplifiers produce an almost pure differential output signal (within ± 0.1 dB amplitude and $\pm 0.5^0$ phase imbalance) when operated at 7.5 GHz, which is well below the transistor f_T of 45 GHz (emitter area of 0.4×10.3 μm^2 and 1 mA bias). The collector shot noise contributed by Q_1 is cancelled in the differential output when the voltage gains in each path (i.e., input to CB output and input to CE output) are equal in magnitude (noise canceling). That is, the product $g_{m1}R_{L1}$ is set equal to $g_{m2}R_{L2}$, where g_{m1} and R_{L1} are the transconductance and collector load resistance of Q_1, respectively, and g_{m2}, R_{L2} are the parameters for transistor Q_2 [13].

When the collector shot noise of Q_1 is cancelled at the balun outputs, noise figure for the input stage is limited by the CE stage because the source impedance (R_S) must be set equal to the input impedance of the CB stage (approximately $1/g_{m1}$) for impedance matching. A PTAT biasing circuit (not shown in Fig. 3) maintains g_{m1} constant with changes in temperature. The noise figure of a 0.4×10.3 μm^2 CE stage in QUBiC4X SiGe technology at 1 mA bias current ($R_S = 1/g_{m1} = 25\ \Omega$) is approximately 4 dB over the 7.2 GHz to 7.7 GHz operating band. This exceeds the target of 5 dB. Note that the noise canceling condition is satisfied when the preamp is impedance matched to the source.

A second differential CE stage (Q_3 and Q_4) is cascaded with the input to realize 30 dB gain. The Miller effect is neutralized by feedback capacitors implemented using transistors Q_5-Q_8,

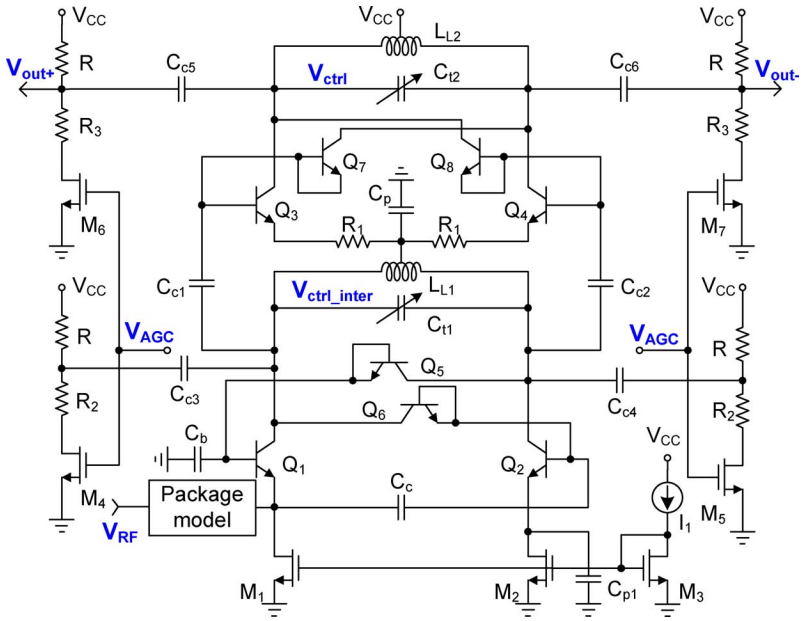


Fig. 3. Schematic of the preamplifier with active balun (bias not shown).

which track the base-collector (i.e., Miller) capacitance in each stage despite of process, bias and temperature variations.

Bias current in the second stage is re-used by the first stage to lower power consumption when operating from a (fixed) 1.8 V supply. Parallel resonant circuit $\mathrm{L_{L1}}$ and $\mathrm{C_{t1}}$ in Fig. 3 provides a high impedance AC load for the first stage, while $\mathrm{L_{L1}}$ conducts bias current from $\mathrm{Q_3}$, $\mathrm{Q_4}$ to input transistors $\mathrm{Q_1}$, $\mathrm{Q_2}$. RF is coupled to the second stage ($\mathrm{Q_3}$ and $\mathrm{Q_4}$) by capacitors $\mathrm{C_{c1}}$ and $\mathrm{C_{c2}}$. As a result, the RF signal is amplified by two stages, while the same DC current biases both stages.

Staggered tuning is applied to each LC tank, so that gain and bandwidth may be varied. Minimum in-band gain variation is guaranteed by controlling the resonant frequency of the two LC tanks. One tank resonates close to 7.2 GHz while the other resonates close to 7.7 GHz, allowing 500 MHz bandwidth to be realized. Simulations predict that this approach accommodates the processing variations anticipated for the BiCMOS technology. Wider bandwidth and gain flatness are accompanied by reduced in-band gain when the separation between the two resonant frequencies increases. Varactors $\mathrm{C_{t1}}$ and $\mathrm{C_{t2}}$ tune bandwidth and gain of each tank, while the differential topology ensures that decoupling capacitor $\mathrm{C_p}$ has no effect on the resonant frequency. The biasing conditions and load impedance of each stage are insensitive to the limited varactor tuning range. While gain control is realized by varying the tank center frequency, tank bandwidth is controlled via variable MOS resistors $\mathrm{M_4}$-$\mathrm{M_7}$.

The 25 Ω input resistance of $\mathrm{Q_1}$ (biased at 1 mA) is transformed by a passive network consisting of a bondwire, package lead (16 pin HVQFN package: very-thin quad flat-pack, no-leads, with exposed paddle) and circuit board trace to impedance match the 50 Ω antenna or preselect filter. An electrical model for the package was developed using Ansoft's Q3D Extractor® tool [14]. The package parasitics are dominated by the series inductance of the bondwire and package lead combination, which has a total self inductance ranging from 0.96 nH to 1.22 nH with mutual coupling coefficient between adjacent leads of approximately 0.2. The input bondpad and ESD protection network are modelled by a 150 fF capacitor in parallel with the input. Bondwire deformation caused by the flow of epoxy encapsulant during injection molding (i.e., wire sweep) is accounted in the model. A fraction of the capacitance needed at the input of the matching network is adjustable on the PCB, either as a discrete component or shorted transmission line stub for trimming. Better than 10 dB input return loss over the 7.2 GHz–7.7 GHz band is predicted (worst case) from simulation.

B. *Wideband FM Demodulator*

In order to avoid the FM capture effect, the received RF signal is not hardlimited prior to demodulation. The capture effect causes suppression of multiple FM signals, which is undesirable in a multi-user sub-carrier FDMA scenario [15]. By avoiding hardlimiting, simultaneous demodulation of multiple FM-UWB input signals with different sub-carrier frequencies occupying the same RF band is possible. The FM-UWB demodulator circuit should be able to process multiple signals simultaneously, where each FM-UWB signal may have a negative SNR. Not all FM demodulators operate effectively under these conditions. For example, a phase-locked loop demodulator will not capture a signal reliably when the input SNR is less than 0 dB (i.e., SNR must be positive), nor can it demodulate multiple RF signals. Thus, a circuit topology and design best suited to the FM-UWB context is required.

The fixed-time-delay FM demodulator developed in this work is shown in Fig. 4. It relies upon FM-to-PM conversion, which yields superior receiver performance overall [16]. The FM signal (V_{RF}) is transformed into a phase-modulated (PM) signal by cascading allpass (APF) and bandpass filter (BPF) stages. The delayed signal is then fed to one input of a simplified Gilbert multiplier, where it is multiplied with the (non-delayed)

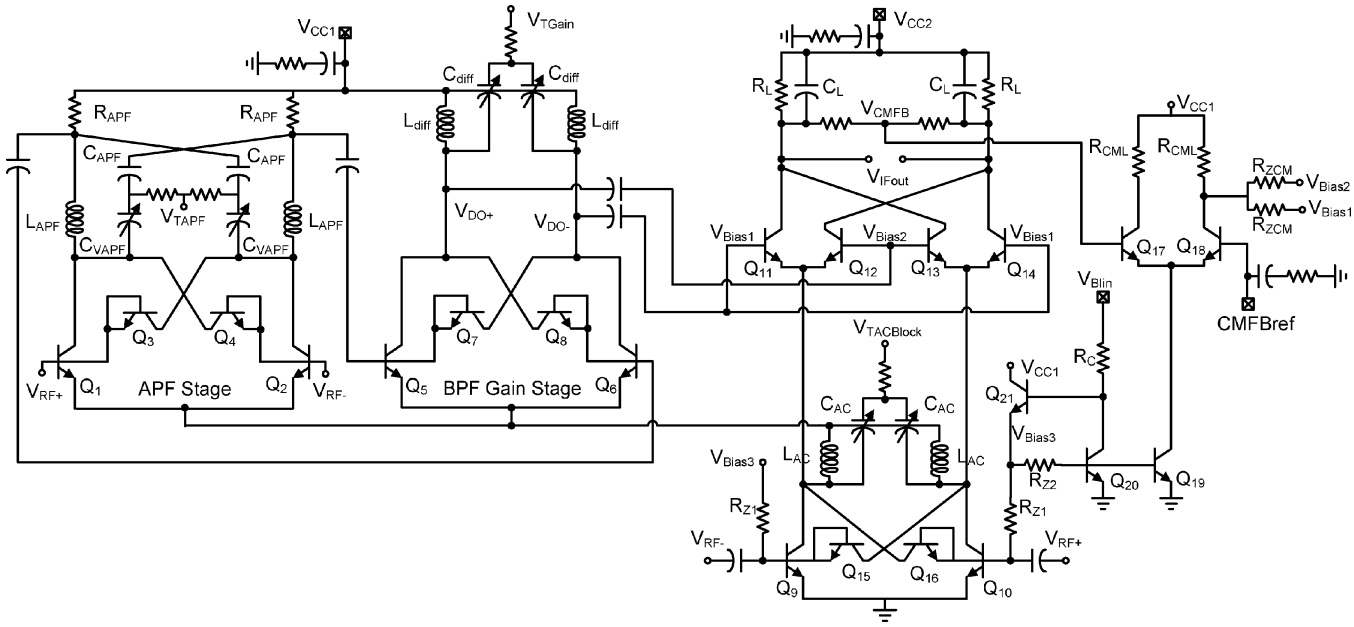


Fig. 4. Schematic of the demodulator.

RF input, yielding the low-frequency, demodulated signal (V_{DEMOD}) at the output.

V_{DEMOD} is maximized when the delay time (τ) is an odd multiple of a quarter-period ($\mathrm{T}/4$) of the FM signal center frequency (i.e., $\tau = NT/4 = N\pi/(2\omega_c)$, where order N is an odd integer). The phase shift at the center frequency is $N\pi/2$.

Assuming a multiplication gain K_D and equal amplitudes (A_I) at the multiplier inputs, the demodulator output signal as a function of frequency is (ideally)

$$V_{\mathrm{DEMOD}}(f) = \frac{K_D A_I^2}{2}\sin\left(N\frac{\pi}{2}\frac{f-f_c}{f_c}\right) = \frac{K_D A_I^2}{2}\sin\left(\pi\frac{f-f_c}{B_{\mathrm{DEMOD}}}\right). \quad (1)$$

Increasing N (i.e., increasing the delay time τ), which increases $V_{\mathrm{DEMOD}}(f)$ for a given frequency difference ($\mathrm{f} - \mathrm{f}_c$), yields higher demodulator sensitivity. B_{DEMOD} represents the useful bandwidth of the demodulator ($2f_c/N$), where N is chosen by trading off the design complexity of the APF and BPF stages with the sensitivity of the demodulator. In this design, the bandwidth is chosen equal to twice the bandwidth of the FM-UWB signal (i.e., $\mathrm{B}_{\mathrm{DEMOD}} = 1$ GHz), requiring $N = 15$. This allows the system to be insensitive to an offset of ± 100 MHz between the demodulator center frequency and the center frequency of the received FM-UWB signal.

1) APF and BPF Delay Stage Design: The group delay (τ_{G}) in the delay path determines the useful frequency range of the demodulator as previously described. A 1 GHz demodulator bandwidth requires a group delay of 504 ps ($N = 15$, $\mathrm{f}_c = 7.45$ GHz). A phase shift of 90° and a portion of the delay are realized with the allpass filter and the second BPF gain stage contributes the remainder. LC tanks are used as loads for both filters so that phase shift across the 2 stages remains close to 90° despite component variations, with varactors $\mathrm{C}_{\mathrm{VAPF}}$ adding capability for trimming.

The current-driven, tunable allpass lattice filter (APF) in Fig. 4 has a transfer function of the form

$$\frac{V_{\mathrm{OUT}}}{I_{\mathrm{IN}}} = -2R_{\mathrm{APF}}\frac{s^2-\omega_0^2}{s^2+\frac{4\omega_0}{Q}s+\omega_0^2} \quad (2)$$

where $\omega_0 = 1/\sqrt{L_{\mathrm{APF}}\left(C_{\mathrm{APF}} \| C_{\mathrm{VAPF}}\right)}$, $Q = \omega_0 L_{\mathrm{APF}}/R_{\mathrm{APF}}$, and $\tau_{\mathrm{G}} = Q/2\omega_0 = L_{\mathrm{APF}}/2R_{\mathrm{APF}}$. The phase shift ($\varphi$) at resonance ($\omega_0$) from (2) is $-90°$, as required for FM demodulation. The input impedance of the APF at ω_0 should be kept low so that the filter is effectively current driven by transistors Q_1 and Q_2 from Fig. 4. Given the chip area required to implement on-chip inductors, $\mathrm{L}_{\mathrm{APF}}$ of 2.5 nH and $\mathrm{R}_{\mathrm{APF}}$ of 12 Ω are selected, resulting in an allpass filter Q-factor of 10 and 6 dB gain. However, the resulting APF group delay τ_{APF}, is 110 ps, which is insufficient to realize the 504 ps delay time required.

Thus, a second gain stage (Q_5 and Q_6) with tunable resonant tank load (see BPF gain stage Fig. 4) is added to realize the total delay time. The 20 dB BPF gain stage also suppresses noise from the following multiplier quad. Q factor of the LC tank is set at approximately 15, yielding a peak group delay of 600 ps at 7.45 GHz in the BPF. The average group delay in the demodulator is approximately 500 ps across the 7.2 GHz–7.7 GHz operating band (note that group delay varies with frequency and average delay is determined from simulation). A 500 ps group delay is equivalent to 15th order ($N = 15$) and bandwidth of 1 GHz for the demodulator (since $\tau = N\pi/(2\omega_c)$), as desired.

2) Gilbert Multiplier: A simplified Gilbert multiplier (i.e., without predistortion stage as in Fig. 4) is used in the demodulator. Sensitivity is improved by optimizing transistor quad (Q_{11}–Q_{14}) so that its noise contribution is minimized without affecting the multiplier gain. Base resistance and its associated thermal noise are minimized by proper selection of transistor emitter area. A bias current of 80 μA for each (0.4×3.0 $\mu\mathrm{m}^2$

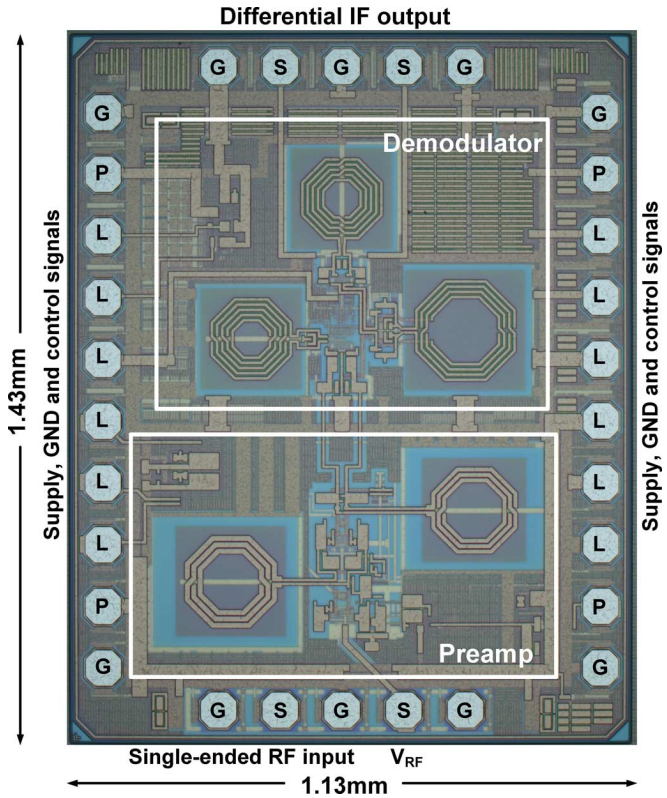


Fig. 5. Die photo of the receiver front-end test chip.

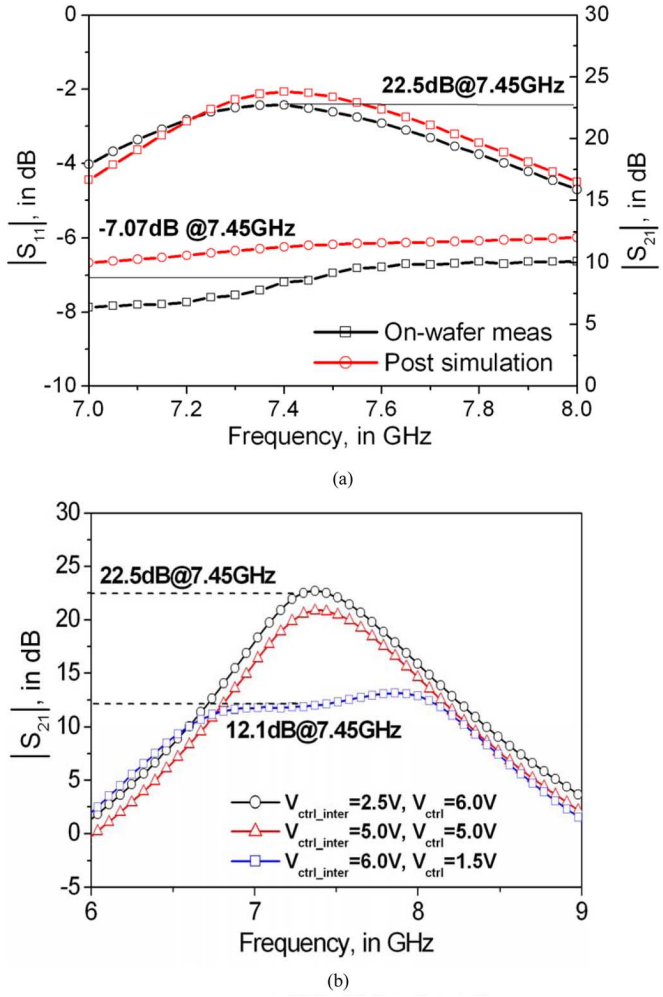


Fig. 6. On-wafer measured performance of the preamplifier. (a) Measured and post-layout simulated S-parameters. (b) Measured gain control capability by staggered tuning technique.

area) transistor in the quad gives an acceptable compromise between multiplier gain and noise performance.

Multiplication gain is determined primarily by the total transconductance preceding the quad. In order to preserve gain while controlling noise generation (thereby maximizing sensitivity), bias currents in the quad and transconductance stages are set independently. Bias current from the input filter and gain stages is also used to bias transconductor Q_9, Q_{10} via inductor L_{AC} (see Fig. 4), so that the overall current consumption is limited to 3.1 mA from a 1.8 V supply. Resonant tuning of L_{AC} using varactors C_{AC} isolates the small-signal and bias paths in the multiplier. Neutralization of feedback currents via the Miller capacitances of Q_3/Q_4, Q_7/Q_8, and Q_{15}/Q_{16} compensates gain roll-off in the delay and input transconductance stages at high frequency. A common-mode feedback loop (Q_{17} and Q_{18}) stabilizes the output DC voltage and controls the bias current flowing through Q_{11}–Q_{14}. Voltage V_{BIin} controls the total bias current via base bias V_{Bias3}, while DC current biasing the quad is adjusted via reference voltage CMFBref. Base bias for the quad transistors (i.e., V_{Bias1} and V_{Bias2}) is sourced via high-ohmic poly resistors R_{ZCM}. The supplies for the delay and multiplier stages are separated so that their bias currents can be monitored during testing (V_{CC1} and V_{CC2} in Fig. 4, respectively).

IV. Measurement Results

The receiver front-end prototype and stand-alone version of the RF preamplifier and demodulator were fabricated in 0.25 μm SiGe:C-BiCMOS [10]. The active areas of the preamp, demodulator, and receiver front-end IC (excluding bondpads) are 0.41 mm^2, 0.50 mm^2, and 0.88 mm^2, respectively. A photomicrograph of the integrated front-end test chip is shown in Fig. 5.

A. RF Preamplifier

Emitter followers were added to the stand-alone version of the preamp in order to drive 50 Ω test equipment. The S-parameters measured on-wafer at 1.8 V supply and 2 mA operating current agree well with post-layout simulations, as seen in Fig. 6(a). Peak S_{21} is 22.5 dB at 7.45 GHz, which corresponds to a voltage gain of 31.5 dB delivered to a (differential) load impedance of 100 Ω. The measured isolation (S_{12}) is better than -50 dB, and the output return loss is better than 10 dB from 1 GHz to 15 GHz. Complete functionality and 25 dB voltage gain for the preamplifier was verified for supply voltage as low as 1.4 V.

The control range realized from the staggered tuning technique is approximately 10 dB, with a measured bandwidth of 1.7 GHz at low gain settings as shown in Fig. 6(b). An overall attenuation from input to output can be obtained via the additional gain control provided by resistors M_4-M_7 (e.g., 2.5 dB attenuation at $V_{ctrl} = 1.5$ V, $V_{ctrl\_inter} = 6.0$ V, and $V_{AGC} = 0.6$ V).

TABLE I
PREAMPLIFIER PERFORMANCE SUMMARY AND COMPARISON

Source	Target spec	Preamp	[17]	[18]	[19]	[20]	[21]
Technology	0.25μm SiGe:C-BiCMOS (this work)		0.18μm SiGe BiCMOS	0.18μm SiGe BiCMOS	0.25μm SiGe BiCMOS	0.13μm CMOS	90nm CMOS
Active Area (mm^2)	—	0.41	—	0.25**	0.92	0.13**	0.2
BW (MHz)	500	650	17,000	500	400	2000	1500
Power (mW)	3.6@1.8V	3.6@1.8V	3.65@2.7V	5@1.8V	14.4@1.8V	45@1.5V	8
S_{21}/A_v (dB)	21/30	22.4/31.4	16.1/22.1	15/21	22/28	25.8/31.8	10.6/19
NF (dB)	5	5.7*	5.65	3.0	1.6	4.0	4.0-5.4
IIP_3 (dBm)	-20	-17	—	-7	—	-13	-8
OIP_3 (dBm)	1	5.4	—	8	—	12.8	2.6
P_{1dB} (dBm)	-30	-27.5	-16.8	—	-17.7	-22.7	—

*NF measured with mismatched RF input **active area estimated from published die micrograph

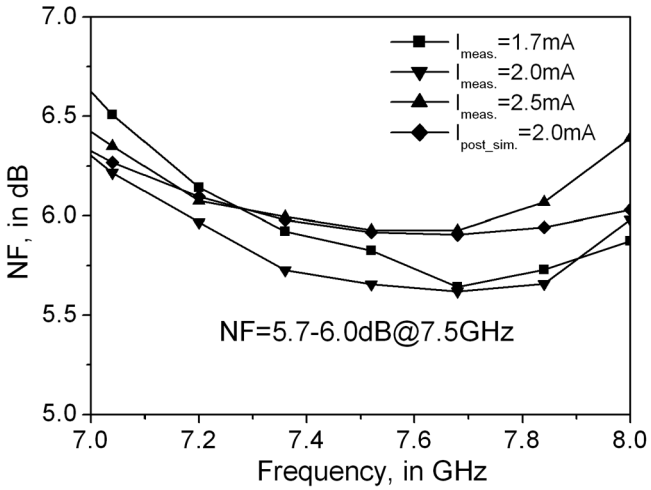


Fig. 7. Measured NF at different bias levels in comparison with the post-layout simulated NF at 2.0 mA.

The measured IIP_3 and P_{1dB} are -17 dBm and -27.5 dBm, respectively, which is 1 dB better than predicted from simulation, and well-above the minimum required IIP_3 of -40 dBm (from Section II-A).

The noise figure measured on-wafer at different bias currents is compared to post-layout simulation in Fig. 7. Measured and simulated 50 Ω noise figure agree within ± 0.25 dB for the same bias settings, unmatched (i.e., $S_{11} = -7$ dB seen in Fig. 6(a)). The package and circuit board parasitics assumed for the preamp design are not present when on-wafer testing, so the measured noise figure (5.7 dB at 7.5 GHz) is 1.2 dB higher than the 4.5 dB predicted from simulation when the RF input is matched to the source.

The preamplifier performance is compared to the target specifications and wideband amplifiers selected from the recent literature in Table I. Voltage gain for the variable-gain preamp designed in this work is higher than 30 dB across the 7.2 GHz–7.7 GHz band, while drawing 2 mA from a 1.8 V supply. The 0.13 μm CMOS amplifier [20] achieves approximately 0.5 dB higher voltage gain but consumes 10 times more power. Higher gain with less power consumption is achieved by the preamp designed in this work compared to the design reported in [17], but at the expense of bandwidth (650 MHz vs. 17 GHz). The noise figure attained by the FM-UWB preamp is comparable to other designs which use a CB input stage [17], or employ the similar active balun and noise canceling [21]. The designs reported in [18], [19] achieve lower noise figure, but higher power is consumed. Larger chip area is required by [19]. When linearity is compared (i.e., OIP_3, which is independent of gain), the preamp designed in this work compares very favorably with the other examples listed in the table given its low dc power consumption.

B. Wideband FM Demodulator

Measured sub-carrier SNR versus input RF power for the stand-alone version of the demodulator at different supply and bias settings is shown in Fig. 8. Post-layout simulation results are included for comparison. The gain stage (26 dB gain) suppresses multiplier noise, yielding an input sensitivity of -68.6 dBm at nominal bias. However, gain saturation begins to appear for signal level greater than -55 dBm due to the high amplification. Reduced gain at low-power biasing (i.e., $V_{CC} = 1.5$ V) results in poorer sensitivity for the demodulator. Sensitivity degrades by approximately 7 dB when power consumption is reduced from 5.8 mW to 3.45 mW as V_{CC} is lowered from 1.8 V to 1.5 V. This illustrates the trade-off

TABLE II
MEASUREMENT SUMMARY FOR THE PROTOTYPE DEMODULATORS

Parameter	Target	Demodulator1		[9]
		Standard	Low Power	Standard
Sensitivity (dBm)	-55	-68.6	-61.8	-46
BW (GHz)	1	1	1	1.8
RF carrier(GHz)	7.45	7.45	7.45	4
Power (mW)	6	5.8	2.8	10
Supply (V)	1.8	1.8	1.2	2.5
Active Area (mm^2)	-	0.5	0.5	0.3*

*active area estimated from published die micrograph

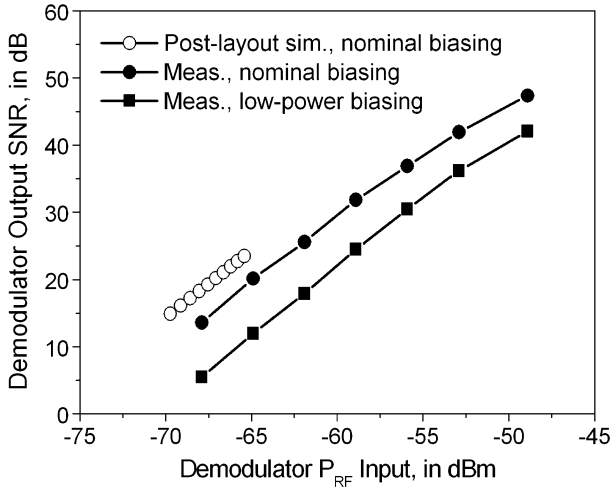


Fig. 8. Post-layout simulated and measured sub-carrier SNR vs. RF input power for the demodulator prototype at different biasing conditions (Nominal biasing: $V_{\rm cc} = 1.8$ V, $\rm I_{bias} = 3.2$ mA; Low-power biasing: $V_{\rm cc} = 1.5$ V, $\rm I_{bias} = 2.3$ mA).

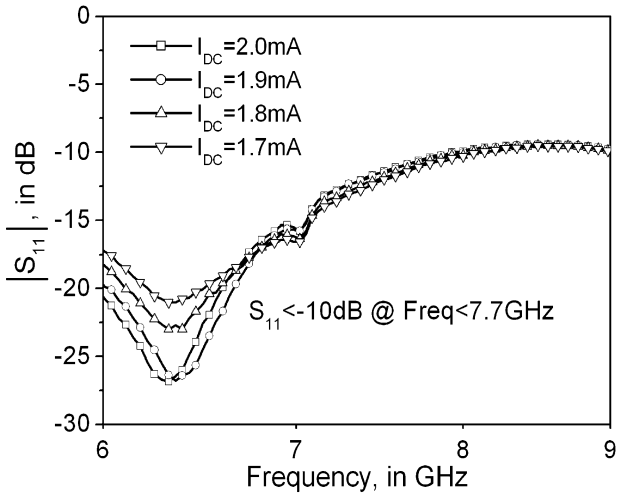


Fig. 9. Measured $\rm S_{11}$ for the receiver front-end.

between RF performance and power consumption. The measured variation in SNR versus RF input power at nominal bias tracks post-layout simulations, but the measured SNR is consistently 5 dB poorer than that predicted from simulation. Potential sources of error in simulation are model inaccuracy (e.g., varactor, inductor and transistor models), inaccurate post-layout parasitic extraction, while improper calibration or measurement inaccuracy could affect the experimental data.

Performance of the demodulator is summarized and compared with the target specifications in Table II. About 14 dB better sensitivity than required is achieved at nominal bias, and the circuit continues to perform well as $V_{\rm CC}$ is reduced from 1.8 V to 1.5 V. A 41% saving in power can be realized with only 7 dB degradation in sensitivity, indicating that further trade-offs between RF performance and power consumption can be made in the FM-UWB receiver design. Few wideband demodulator examples could be found in the recent literature, but more than 20 dB greater sensitivity with 40% less power is achieved for the demodulator design in this work compared to the circuit reported in [9] (see Table II).

C. FM-UWB Receiver Front-End

Measurement of the complete receiver front-end (i.e., combined preamp and demodulator) described in this section was performed on packaged devices mounted on a custom-designed PCB fabricated from Rogers 4350 material. Preamp loading is minimized by the relatively high input impedance of the demodulator, so the emitter followers used in the stand-alone version of the preamp are not required. The preamp supply is shared with $V_{\rm CC1}$ of the demodulator (see Fig. 4), while $V_{\rm CC2}$ of the demodulator is adjusted separately to control biasing of the multiplier stage. Parasitics at the RF input packaged in the 32 pin HVQFN used for testing are identical to those assumed for the 16 pin package used for the preamp design. The measured return loss is better than 10 dB from 7.2 GHz to 7.7 GHz (see Fig. 9). The total input inductance is approximately 0.3 nH larger than expected, causing a shift in the minimum return loss to 6.5 GHz.

The front-end sensitivity was measured using a 500 MHz wide FM-UWB RF input signal centered at 7.45 GHz, and then evaluating the sub-carrier SNR (500 kHz sub-carrier) in a 200 kHz bandwidth (100 kbps FSK with $\beta_{\rm SUB} = 1$). Measurements show that the developed prototype handles data rates up to 100 kbps. Fig. 10 illustrates the measured sub-carrier SNR as a function of RF input power for the receiver front-end at two different bias settings, and the simulated performance at 1.8 V supply (i.e., nominal biasing). The nominal bias settings

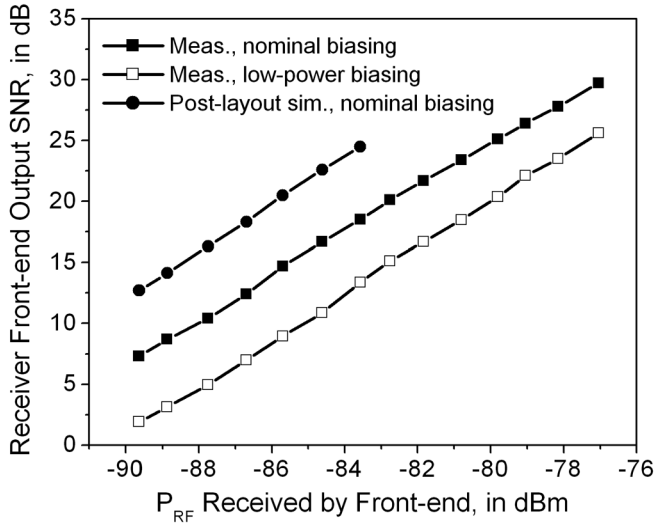


Fig. 10. Post-layout simulated and measured sub-carrier SNR vs. RF input power at different biasings for receiver front-end (Nominal biasing: $V_{\rm cc} = 1.8$ V, $\rm I_{bias} = 5.1$ mA; Low-power biasing: $V_{\rm cc} = 1.5$ V, $\rm I_{bias} = 4$ mA).

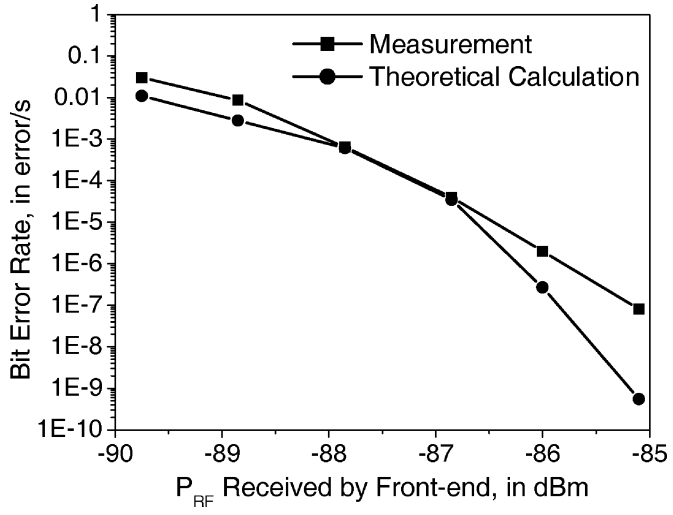


Fig. 11. Front-end BER measurement results with 50 kbps data rate and 1 MHz subcarrier.

are 2 mA and 3.1 mA for the preamp and demodulator, respectively, at a 1.8 V supply. In the low-power setting, the supply voltage is reduced to 1.5 V and preamp and demodulator bias currents are reduced to 1.7 mA and 2.3 mA, respectively. The measured receiver sensitivity is −85.8 dBm under nominal biasing conditions for $\rm SNR_{SUB} = 14$ dB. In low-power bias mode, sensitivity drops to −83 dBm. The 3 dB reduction in sensitivity is caused by a combination of lower preamp gain and poorer demodulator sensitivity at the lower bias settings. The 6 dB difference in SNR between measurement and simulation is consistent with the 5 dB SNR difference observed between measurement and simulation for the demodulator (see Fig. 8). Loading of the preamp by the demodulator input stage, and other sources of experimental error could account for the additional 1 dB difference.

The bit-error rate (BER) was measured for a complete receiver board at 50 kbps date rate, where the RF front-end is followed by sub-carrier processing blocks and a digital FSK subcarrier demodulator. Fig. 11 shows the measured BER under nominal biasing conditions, compared to the theoretical BER for FM-UWB system[1] [2]. A BER of 1×10^{-6} is observed at −85.8 dBm input power. The difference between measurement and theory at higher received powers is likely due to inadequate supply decoupling and imperfections in the baseband FSK demodulator.

1) Measurement With 2 FM-UWB Users: Tests were also carried out on the receiver front-end to validate multi-user performance using sub-carrier FDMA, where different users share the same RF bandwidth but distinguish themselves via different sub-carrier frequencies.

Two cases are modeled and evaluated; the first, where two FM-UWB users are received at the same RF input power level, and a second where the received power levels differ by 10 dB. In this scenario, one user may be viewed as a source of interference for the other, and vice-versa. The signal output from the wideband demodulator is buffered by a 46 dB gain amplifier for measurement. Fig. 12(a) shows the measured output for two users with equal RF powers (−70 dBm) and operating at sub-carrier frequencies of 1.25 MHz and 1.50 MHz. As expected, equal amplitude FSK signals are observed after demodulation. Fig. 12(b) shows the wideband demodulator output signal when the interferer has a power level 10 dB stronger than the desired RF signal (i.e., user1 is −60 dBm at 1.25 MHz vs. user2 at 1.5 MHz and −70 dBm). The amplitude of the interfering sub-carrier increases by 20 dB compared to the level shown in Fig. 12(a), due to the quadratic transfer characteristic of the FM demodulator (see (1)). The noise floor rises by 4 dB (compared to Fig. 12(a)) due to multiple-access interference. The measured BER drops to 1×10^{-3} when the signal-to-interference ratio (SIR) is −14 dB (i.e., interferer 14 dB stronger than the desired signal).

These results show that the performance is limited by the multi-access interference when subcarrier FDMA is employed [2], [22]. Robustness to multi-access interference can be improved by increasing the receiver processing gain through widening the bandwidth of the transmit signal (e.g., 1 GHz), or adopting a different multiple access techniques to multiplex different users onto the RF carrier (e.g., TDMA in the transmitter baseband, or frequency multiplexing FM-UWB signals at RF, i.e., RF FDMA). However, for a multi-sensor BAN application, 14 dB SIR is sufficient to cope with variations in distance and shadowing. We have experimentally determined that in the multi-sensor BAN application, the combination of TDMA and sub-carrier FDMA yields adequate performance.

2) Measurement With Narrowband Interferer: The FM-UWB receiver front-end performance was also evaluated in the presence of narrowband interference, both in-band at 7.5 GHz and out-of-band at 6.0 GHz. Fig. 13 illustrates the measured front-end sensitivity versus received power level for a single interfering tone. The FM-UWB receiver can detect RF inputs down to −85.8 dBm, even though a 25 dB stronger narrowband interferer is present (i.e., −60 dBm interference). Sensitivity degrades by more than 3 dB as the interference increases above −55 dBm in-band, and above −38 dBm out-of-band. The measured power difference of 17 dB between

[1]Theoretical BER for FM-UWB system is expressed as

$$\mathrm{BER} = 0.5 \times erfc\left[\frac{0.5 \times B_{\rm RF}\mathrm{SNR}_{\rm RF}^2}{B_{\rm SUB}\left(1+4\mathrm{SNR}_{\rm RF}\right)}\right]$$

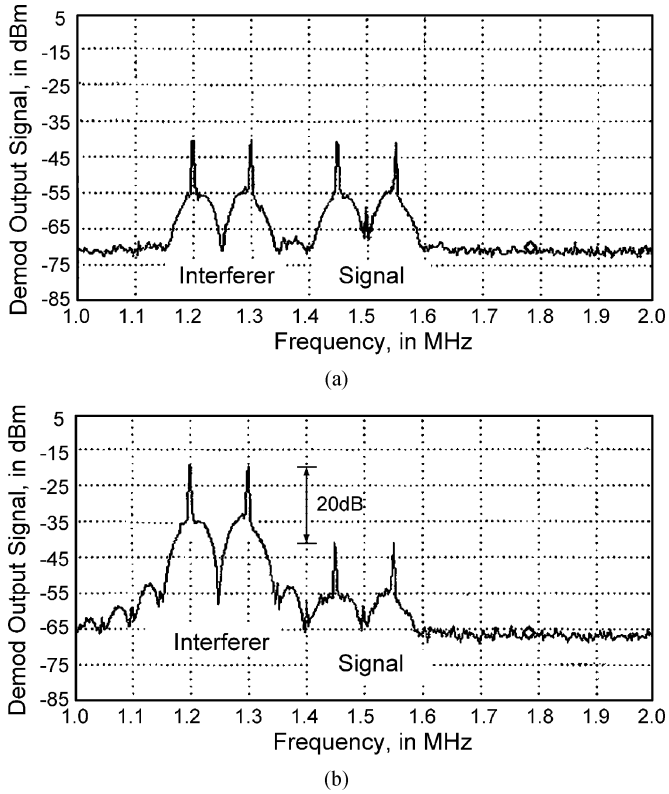


Fig. 12. FM-UWB receiver front-end measured signal at the demodulator output with 50 kbps data rate and two users. (a) Wideband demodulator output for two users of equal strength. (b) Wideband demodulator output for two users with 10 dB power difference at RF.

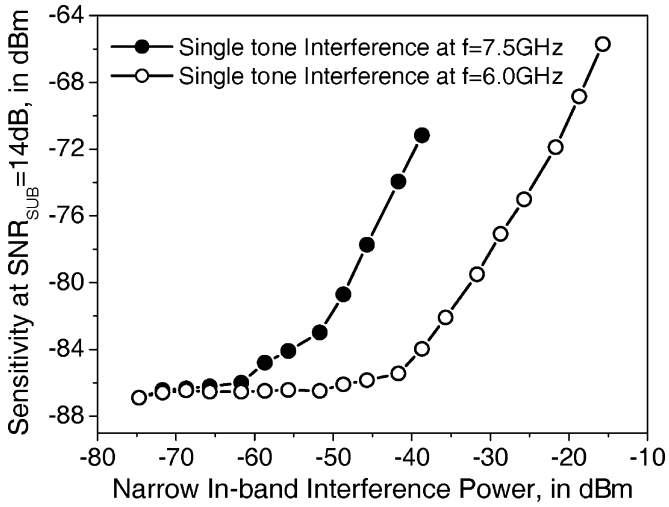


Fig. 13. Sensitivity of front-end test chip with narrowband interference.

these two cases is due to the additional out-of-band interference suppression from the bandpass responses of the preamplifier and FM demodulator gain stages. Out-of-band interference suppression could be further improved by adding a preselect filter at the RF input (e.g., up to 45 dB additional rejection), or using a frequency-selective antenna (e.g., with band-reject notches in the frequency characteristic).

3) Measured Performance Comparison: The receiver front-end prototype performance is compared to the target specifications and state-of-the-art SiGe and CMOS circuits selected from the recent literature in Table III. The receiver front-end developed in this work realizes −88.0 dBm measured sensitivity at a BER of 1×10^{-3} and 9.1 mW power consumption (see Fig. 11). The Zigbee and UWB receiver front-ends reported in [23], [24] achieve about 10 dB better sensitivity, but consumes 3 to 4 times more power and require more chip area in their implementations. Comparable sensitivity at the same BER is realized by the Bluetooth front-end from [25] at a higher data rate, however, higher power is again consumed. The FSK narrowband receiver design reported in [26] realizes 20 dB better sensitivity operating in the ISM band around 0.9 GHz, where gain is easier to realize at low current consumption. However, this implementation may be susceptible to interference from nearby commercial cellular bands and other appliances operating in the same (unlicensed) ISM band at 900 MHz. The sensitivity of a FM-UWB receiver at 50 kbps and BER of 1×10^{-3} is about 20 dB poorer than an ideal narrowband FSK receiver [2]. However, robustness against interference and multipath is greater for FM-UWB compared to narrowband FSK.

V. Summary and Suggestions for Future Work

An FM-UWB receiver front-end for low-complexity, robust short-range communication has been demonstrated in a production 0.25 μm SiGe BiCMOS technology. The RF preamplifier realizes 30 dB voltage gain across the 7.2 GHz–7.7 GHz band, with a 50 Ω noise figure of 5.7 dB (unmatched) and drawing 2 mA from a 1.8 V supply. The bandwidth and gain of the preamp is controlled via a staggered tuning and variable-load AGC method. An overall gain control range of 25 dB was demonstrated. The wideband FM demodulator integrates a differential allpass filter and bandpass gain stage on chip, rather than a conventional passive delay line. Measured RF input sensitivity is −68.6 dBm at 3.1 mA bias current from a 1.8 V supply. Operating at a data rate of 50 kbps, measured sensitivity for the prototype receiver front-end is −85.8 dBm (1×10^{-6} BER) consuming 9 mW from a 1.8 V supply, and −83 dBm consuming 6 mW from a 1.5 V supply in the low-power mode. Over the air experiments have demonstrated 15 to 20 meter spans in a typical indoor office environment with line of sight propagation.

The demodulator gain affects the tradeoff between dynamic range and power consumption of the receiver. In the case where noise from preamp begins to dominate the front-end sensitivity, the demodulator gain can be decreased in order to reduce power consumption and maximize the dynamic range.

The results of this study validate FM-UWB as a low-complexity, robust wireless radio technology. Further development of FM-UWB could enable new applications requiring low data rate radios with power consumption on the order of a few mW. A fully-integrated FM-UWB transceiver requires sub-carrier processing and FSK demodulator circuits, a PLL for center frequency calibration and a direct digital synthesizer for multi-user sub-carrier modulation. Implementation of a complete FM-UWB system with multi-user capability, improved large-signal performance for greater robustness, and mW power consumption in BiCMOS/CMOS technology are goals for future research and development work.

TABLE III
MEASUREMENT RESULTS FOR RECEIVER FRONT-END

Parameter	This work			[23] Zigbee	[24] UWB	[25] Bluetooth	[26] SRD (FSK)
	Target	Standard	Low power				
Technology	0.25μm SiGe:C BiCMOS			0.18μm CMOS	90nm CMOS	0.25μm BiCMOS	0.18μm CMOS
Sensitivity (dBm)	-84	-85.8/-88	-83	-101	-99	-91	-108
BER	$1x10^{-6}$	$1x10^{-6}$/$1x10^{-3}$	$1x10^{-6}$	$1x10^{-2}$	$1x10^{-3}$	$1x10^{-3}$	$1x10^{-3}$
RF band (GHz)	7.2-7.7	7.2-7.7	7.2-7.7	2.4 (ISM)	4.4 (UWB)	2.4 (ISM)	0.868 (SRD)
Data rate (kbps)	<50	50	50	250	100	-	25
Power/current Consumption	10mW	9.1mW	6mW	14.7mA	35.8mW	33.5mW	2.1mA
Power Supply (V)	1.8	1.8	1.5	1.8-3.6	0.65	2.5	1.0-1.6
Active Area (mm^2)	-	0.88	0.88	-	1.0*	1.7*	1.2*

*active area estimated from published die micrograph

ACKNOWLEDGMENT

Prototypes were designed and implemented at the IC Lab of NXP Semiconductors in collaboration with Delft University of Technology. The authors would like to thank M. Collados for measurement support and H. Bonakdar and J. Bergervoet of NXP Semiconductors for many fruitful discussions on circuit design.

REFERENCES

[1] J. R. Long, W. Wu, Y. Dong, Y. Zhao, M. A. T. Sanduleanu, J. F. M. Gerrits, and G. van Veenendaal, "Energy-efficient wireless front-end concepts for ultra lower power radio," in *Proc. IEEE CICC*, San Jose, CA, 2008, pp. 587–590.

[2] J. F. M. Gerrits, M. H. L. Kouwenhoven, P. R. van der Meer, J. R. Farserotu, and J. R. Long, "Principles and limitations of UWBFM communications systems," *EURASIP J. Appl. Signal Process.*, vol. 2005, no. 3, pp. 382–396.

[3] Y. Dong, Y. Zhao, J. F. M. Gerrits, G. van Veenendaal, and J. R. Long, "A 9 mW high band FM-UWB receiver front-end," in *Proc. ESSCIRC*, Sep. 2008, pp. 302–305.

[4] Sapphire DART, Ultra Wideband Real-Time Location System Datasheet. [Online]. Available: http://www.multispectral.com/pdf/Sapphire_DART.pdf

[5] G. Heidari, *WiMedia UWB: Technology of Choice for Wireless USB and Bluetooth*. New York: Wiley, 2008.

[6] *Body Area Networks (BAN)*, IEEE 802.15 WPAN™ Task Group 6 [Online]. Available: http://www.ieee802.org/15/pub/TG6.html

[7] A. El-Hoiydi and J.-D. Decotignie, "WiseMAC: An ultra low power MAC protocol for multi-hop wireless sensor network," in *Proc. 1st Int. Workshop on Algorithmic Aspects of Wireless Sensor Networks (ALGOSENSORS 2004)*, Jul. 2004, vol. LNCS 3121, Lecture Notes in Computer Science, pp. 18–31.

[8] S. Brebels, S. Sanders, C. Winters, T. Webers, K. Vaesen, G. Carchon, B. Gyselinckx, and W. de Raedt, "3D SoP integration of a BAN sensor node," in *Proc. ECTC*, Jun. 2005, pp. 1602–1606.

[9] J. F. M. Gerrits, J. R. Farserotu, and J. R. Long, "A wideband FM demodulator for a low-complexity FM-UWB receiver," in *Proc. ECWT*, 2006, pp. 99–102.

[10] P. Deixler, A. Rodriguez, W. de Boer, H. Sun, R. Colclaser, D. Bower, N. Bell, A. Yao, R. Brock, Y. Bouttement, G. A. M. Hurkx, L. F. Tiemeijer, J. C. J. Paasschens, H. G. A. Huizing, D. M. H. Hartskeerl, P. Agarwal, P. H. C. Magnee, E. Aksen, and J. W. Slotboom, "QUBiC4X: An $f_T/f_{max} = 130/140$ GHz SiGe:C-BiCMOS manufacturing technology with elite passives for emerging microwave applications," in *Proc. BCTM*, Sep. 2004, pp. 233–236.

[11] Y. Zhao, G. van Veenendaal, H. Bonakdar, J. F. M. Gerrits, and J. R. Long, "3.6 mW, 30 dB gain preamplifiers for an FM-UWB receiver," in *Proc. BCTM*, Oct. 2008, pp. 216–219.

[12] B. Nauta, "Single-to-differential converter," U.S. Patent 5,404,050, Apr. 4, 1995.

[13] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[14] Q3D EXTRACTOR®, A 2D/3D Parasitic Extraction Tool for Electronic Design. [Online]. Available: http://www.ansoft.com/products/si/q3d_extractor/

[15] K. Leentvaar and J. H. Flint, "The capture effect in FM receivers," *IEEE Trans. Commun.*, pp. 531–539, May 1976.

[16] M. H. L. Kouwenhoven, *High-Performance Frequency-Demodulation Systems*. Delft, The Netherlands: Delft Univ. Press, 1998.

[17] K. Bhatia, S. Hyvonen, and E. Rosenbaum, "A compact, ESD-protected, SiGe BiCMOS LNA for ultra-wideband applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1121–1130, May 2007.

[18] P. Roux, Y. Baeyens, J. Weiner, and Y. K. Chen, "Ultra-low-power X-band SiGe HBT low-noise amplifiers," in *Proc. IEEE Microwave Symp.*, Jun. 2007, pp. 1787–1790.

[19] G. Gramegna, A. Magliarisi, and M. Paparo, "An 8.2-GHz, 14.4 mW, 1.6 dB NF SiGe bipolar LNA with DC current reuse," in *Proc. BCTM*, Sep. 2003, pp. 49–52.

[20] R. Salerno, M. Tiebout, H. Paule, M. Streibl, C. Sandner, and K. Kropf, "ESD-protected CMOS 3–5 GHz wideband LNA+PGA design for UWB," in *Proc. ESSCIRC*, Sep. 2005, pp. 219–222.

[21] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A wideband noise-canceling CMOS LNA exploiting a transformer," in *Proc. IEEE RFIC Symp.*, San Francisco, CA, Jun. 2006.

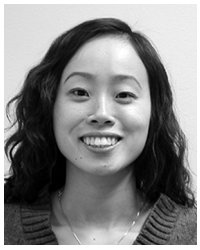
[22] J. F. M. Gerrits, J. R. Farserotu, and J. R. Long, "Multi-user capabilities of UWBFM communications systems," in *Proc. Ultra-Wideband*, Sep. 2005, pp. 684–689.

[23] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, and D. Eggert, "A fully integrated 2.4-GHz IEEE 802.15.4-compliant transceiver for Zigbee™ applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2767–2775, Dec. 2006.

[24] F. S. Lee and A. P. Chandrakasan, "A 2.5 nJ/b 0.65 V 3-to-5 GHz subbanded UWB receiver in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 116–590.

[25] A. A. Emira, A. Valdes-Garcia, B. Xia, A. N. Mohieldin, A. Valero-Lopez, A. T. Moon, X. Chunyu, and E. Sanchez-Sinencio, "A dual-mode 802.11b/Bluetooth receiver in 0.25 μm BiCMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 270–527.

[26] V. Peiris, C. Arm, S. Bories, S. Cserveny, F. Giroud, P. Graber, S. Gyger, E. Le Roux, T. Melly, M. Moser, O. Nys, F. Pengg, P. D. Pfister, N. Raemy, A. Ribordy, P. F. Ruedi, D. Ruffieux, L. Sumanen, S. Todeschin, and P. Volet, "A 1 V 433/868 MHz 25 kb/s-FSK 2 kb/s-OOK RF transceiver SoC in standard digital 0.18 μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2005, vol. 1, pp. 258–259.



Yi Zhao (S'08) received the B.Sc. degree in electrical engineering from the Fudan University, Shanghai, China, in 2005 and the M.Sc. degree in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2008.

She worked for NXP Semiconductors in The Netherlands on ultra-wideband RF circuit design in 2008. She is currently pursuing the Ph.D. degree in microelectronics at the Delft University of Technology. Her current research interests include integrated transceiver circuit for wireless and high-speed communication applications in RF and mm-wave domain.

Yunzhi Dong (S'09) received the B.Sc. degree (with honors) from the Department of Microelectronics, Fudan University, Shanghai, China, in 2005, and the M.Sc. degree (with distinction) from the Department of Electrical and Computer Engineering, Delft University of Technology (TU Delft), Delft, The Netherlands, in 2008. Currently, he is working towards the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada.

From March 2006 to August 2006, he was a student IC design intern within the Analog Division, Flash Product group, Intel, Shanghai, China. From May 2007 to February 2008, he was a student IC design intern within IC Lab, NXP Semiconductors, Eindhoven, The Netherlands, working on low-power UWB RFIC designs. From March to June 2008, he was employed by the same division at NXP Semiconductors as an analog IC designer. His research interests include high-speed analog circuits and RFIC circuits.

John F. M. Gerrits (M'91–SM'07) was born in 1963 in Leiden, The Netherlands. He received the M.Sc.E.E. degree from Delft University of Technology, Delft, The Netherlands, in 1987. His final thesis was on the design of integrated high-performance harmonic oscillator circuits.

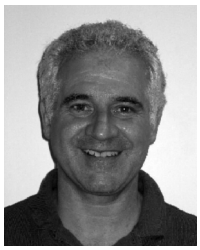
In 1988, he joined the Philips T&M division in Enschede, The Netherlands, where he designed integrated oscillator and data-acquisition systems for oscilloscope applications. In 1991, he joined CSEM in Neuchâtel, Switzerland, where he has been involved in both system and circuit design of a single-chip low-power VHF radio receiver for hearing aid applications and of a single-chip ISM UHF transceiver. His current work involves system and circuit design of UWB radio systems, RF sensing and measurement methodology. He is currently working towards the Ph.D. degree on the fundamental aspects and practical realizations of FM-UWB communication systems at Delft University of Technology. He is editor and co-author of the book *Low-Power Design Techniques and CAD Tools for Analog and RF Integrated Circuits* (Kluwer, 2001). He holds three European and five U.S. patents. He is the winner of the 2006 European Conference on Wireless Technologies Prize.

Gerrit van Veenendaal was born in Arnhem, on March 10, 1956. He joined Philips Research Laboratories Eindhoven, The Netherlands, in 1979. From 1979 to 1989, he was a research assistant, working on optical communication, data transmission and integrated transceivers. In 1989, he moved to Philips Semiconductors Product Concept and Application Laboratory as a Senior Designer active in AM/FM radio, satellite and terrestrial integrated TV systems. In 1996, at Philips Semiconductors System Laboratory Eindhoven, he was working on and involved in Paging, Bluetooth and program management. Since 2004, he has been New Business Development Manager at Philips Consumer Electronics IC Laboratory and is also responsible for EU and National subsidy projects at ICLab. ICLab moved to NXP Semiconductors Innovation and Technology office in 2006.

John R. Long (S'77–A'78–M'83) received the B.Sc. degree in electrical engineering from the University of Calgary, Canada, in 1984, and the M.Eng. and Ph.D. degrees in electronics from Carleton University, Ottawa, Canada, in 1992 and 1996, respectively.

He was employed for 10 years by Bell-Northern Research, Ottawa (now Nortel Networks R&D), involved in the design of ASICs for Gbit/s fiber-optic transmission systems, and from 1996 to 2001 as an Assistant and then Associate Professor at the University of Toronto, Canada. Since January 2002, he has been chair of the Electronics Research Laboratory at the Delft University of Technology, The Netherlands. His current research interests include transceiver circuits for integrated wireless and high-speed wireline data communications systems.

Prof. Long is a former Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and is currently a Distinguished Lecturer for the Solid-State Circuits Society. He received the NSERC Doctoral Prize and Douglas R. Colton and Governor General's Medals for research excellence, and is a co-recipient of Best Paper Awards from the International Solid-State Circuits Conference (ISSCC) in 2000 and 2007, the RFIC and European Wireless Symposia in 2006, and IEEE-BCTM in 2003. He was general chair and local organizer for the 2006 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), held in Maastricht, NL. He chairs the RF circuits subcommittee for ISSCC 2010, and is a member of the technical program committees for the European Solid-State Circuits (ESSCIRC) and European Microwave IC (EuMIC) conferences.



John R. Farserotu (S'81–M'82–SM'07) received the B.S.E.E. degree from the University of Maryland, College Park, MD, in 1982 and the M.S.E.E. degree in communications engineering from George Washington University, Washington DC, in 1986. In 1998, he received the Ph.D. degree in electrical engineering from the Telecommunication and Traffic Control Systems Group, Delft University of Technology, Delft, The Netherlands.

He is currently the Head of the Information Communication Technology (ICT) Programme at CSEM. His research interests include wireless systems, ultra wideband (UWB), modulation and coding, HAP/satellite communication and networking. He has authored or co-authored over 50 publications in major journals and conferences. He is co-author of a book on Mobile Satellite over IP/ATM Networks, published in English and Chinese, and he currently teaches a course on this subject at the Ecole Polytechnique Federale de Lausanne (EPFL).

Dr. Farserotu is the Vice-Chair and Research Co-ordinator of the HERMES Partnership, a network of major European R&D centers in the field of wireless and mobile communication bringing together over 1000 engineers and scientists. He was the Deputy Co-ordinator of the FP6 MAGNET IP. He is also a member of the Editorial Board of Wireless Personal Communications, a leading international journal on wireless communication and has served on technical programme committees, steering and organizing committees of major international conferences in the domain of wireless and mobile communication.

Previously, Dr. Farserotu was a Principal Scientist in the Satellite Communications Branch, of the NC3A, The Hague, where he was a member of the SATCOM Post-2000 team evaluating SATCOM requirements, options and technologies for the future, as well as, the ATM project team, examining ATM over SATCOM, networking and performance analysis and characterisation. From 1985 to 1990, he was a Senior Engineer and Task Leader at Stanford Telecommunications, Inc., Reston, VA, where he led a team of engineers performing design and analysis of communication waveforms and systems.