Charge-Transfer CMOS Image Sensors: Device and Radiation Aspects

Charge-Transfer CMOS Image Sensors: Device and Radiation Aspects

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To Gayathri, Sudarshan, amd my Family

ഗായത്രിക്കും സുദർശനും സുകുടുംബത്തിനും

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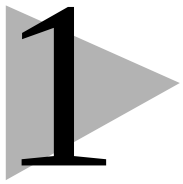


The Universe has always been a fascination to humans through the ages. One of the ancient Rig Vedic hymn relating to the creation of the Universe reads thus: “There was not what is not, and there was not what is, then” [1.1]. Time has changed much since this most celebrated philosophical statement, wherein the author portrays his dilemma as rhetoric [1.2]. Yet, Man has only started to objectively understand the intricacy of this Universe at the macroscopic as well as the microscopic level. It is not far-fetched to argue that both of these have been possible, to a large extent, due to the ability of Man to see the farthest and the smallest. The photon, which carries information in the form of energy (colour) and amplitude (brightness), travels with an incredible speed of 3×10^8 m/s. By “freezing” these photons, it is not only possible to bring back old memories, but also study events more carefully for many scientific applications. Aesthetics is a complex topic; at least when it comes to photography (the art of freezing photons in a pleasing manner). This thesis attempts to study device physics aspects of solid-state detectors used in scientific applications: radiation effects on CMOS image sensors and a CCD (Charge-Coupled Device) like image sensor in

standard CMOS technology (aimed at medical applications)—leaving the problem of aesthetics to seasoned artists!

1.1 History of photography

1.1.1 Development of the camera—The early period

Camera Obscura (literally "dark-room") utilized a pin-hole to project an image onto a wall (inside the dark room) and has been prevalent for at least four centuries now [1.3]. The first mention of the concept of a pin-hole camera can be traced back to Mozi, a Chinese philosopher who lived circa 400 BC. An accurate description of camera obscura, however, has been credited to the Persian scientist, Ibn al-Haitham. Down the time line, Aristotle also seems to have known the principles of the optics of camera obscura. Leonardo Da Vinci mentions it in his work *Codex Atlanticus* and is speculated to have even used one of them. The Dutch masters like Johannes Vermeer Van Delft (17^{th} century), who painted such intricate details may have used such a system, though the idea is regarded highly controversial [1.4]. The first "portable" version of camera obscura was built by Johann Zahn in 1685 [1.5].

The name "photography" was coined by John Herschel in the year 1839. This came at a time when the technique of the *Daguerreotype*—an early camera based on the camera obscura and a plate coated with silver salts—was made "public" by the French Government. This was the culmination of efforts undertaken by many people who studied the effect of light on certain chemicals (e.g., silver chloride). A major hurdle was the requirement for large exposure times to form an image; sometimes for hours together. The issue of sensitivity of the silver chemicals was tackled by using gallic acid as a sensitiser which resulted in the *Talbotype*; another photographic technique on paper. Many photographic processes were to ensue—like the *colloidal* method as well as advancements in photographic glass plates through the 19^{th} century.

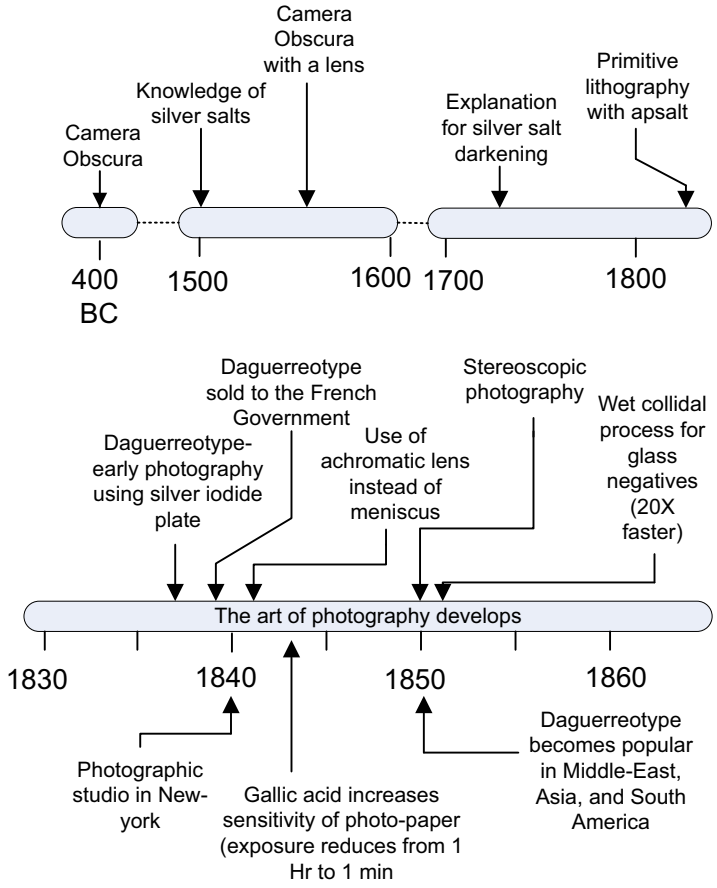


Fig. 1-1 *Milestones in the development of photography: the early period (~ 400 BC-1860) [1.3].*

In 1851, the invention of the collodion process greatly improved the time required for exposure on glass plates—from several minutes to a few seconds. Of the different competing types of photographic processes, the Talbotype is considered to be the cul-de-sac of early photography, culminating to the modern film based cameras.

The major milestones in the development of photography in the early period (~ 400 BC-1860) is shown in Figure 1-1.

Fig. 1-2 *Willard S. Boyle (left) and George E. Smith, inventors of the charged-coupled device (CCD), demonstrating the imaging capabilities of their patented CCD camera in 1974 [1.6]. Reprinted with permission.*

1.1.2 Development of the camera—The early modern and modern periods

During the end of the 19th century, the photographic film was developed by George Eastman for his Kodak camera, and became the basis for the modern film based photographic system [1.8]. This camera became very popular among the public, and no wonder the slogan for the Kodak system was: "You press the button, We do the rest"!

The first mass marketed film camera, the *Brownie*, hit the market in the year 1900. A major breakthrough came with the

introduction of the *Kodachrome* film in 1935, resulting in the first color camera. From here on, the film camera gained immense popularity, with consumers having a variety of choices to make with respect to size, cost and features.

The first viable light-to-digital conversion using a CCD was developed by Willard S. Boyle and George E. Smith in the year 1969. The CCD camera was patented by its inventors in the year 1974 (Figure 1-2).

But the first viable color digital camera had to wait until the year 1981, when Sony's *Sony Mavica* was released. This was marked a major step towards popularising digital photography among the masses. The first Megapixel camera was already conceived in 1987 through Kodak's *Videk*. The Megapixel race in the CCD world was soon gaining momentum. Between 1973 and 1994, the quality of CCD in terms of sensitivity, noise and pixel density became comparable to that of the film.

On the other hand, a thin but visible track of CMOS image sensors started to emerge in the 1990s. The key figure behind the development of a low power and radiation tolerant sensor (thus rendering it suitable for outer-space applications) was Eric Fossum of JPL (Jet Propulsion Lab). Though developed for scientific applications, it soon became popular in the consumer circle, due to its lower costs and power requirements.

The first commercial camera which used a CMOS image sensor was the 1.8 Megapixel *CMOS-PRO* digital camera introduced in 1990. Starting with such a humble beginning, CMOS image sensors quickly joined the megapixel race. In early 2008, Samsung announced a 14.6 Megapixel CMOS image sensor for the DSLR camera GX-20. As of this writing, Sony already has plans for a 24.8 Megapixel sensor for their DSLR! For many scientific applications, even higher resolution sensors are required. Currently only CCDs can satisfy this requirement. For example, DALSA has released a 100+ Megapixel CCD sensor (to be accurate—111 Megapixel) for astronomical purposes. It will not be long before CMOS image sensors catch up with CCDs in the ultra-high resolution arena.

The timeline of major milestones in the early modern and modern periods of photography is graphically represented in Figure 1-3.

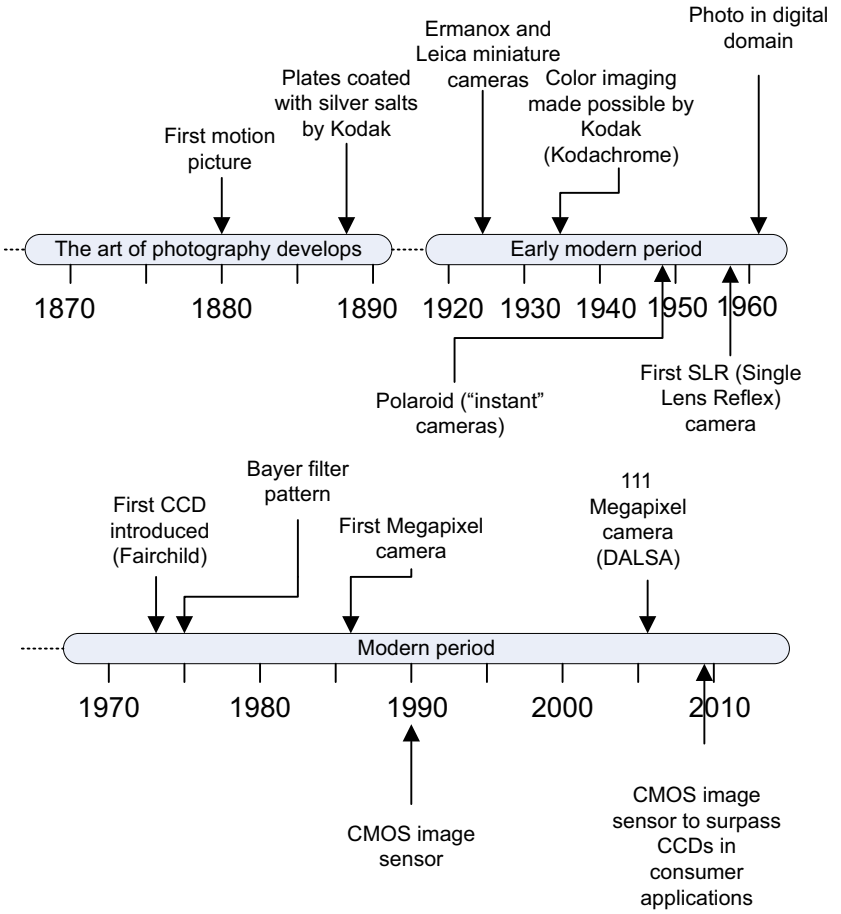


Fig. 1-3 *Development of the camera: early modern and modern periods [1.3].*

1.1.3 Development of the digital camera—Scientific applications

Though the CCD (Charge-Coupled Device) was invented in 1969, its development and acceptance in scientific imaging was slow. The major competitor for the digital image sensor in scientific applications was the photographic film itself. Film technology was well established, mature and standardised. It had its own merits over the then digital sensors. For example, the film corresponds to the resolution of a 100+ Megapixel sensor—a feat that could not be contested by the early-era digital sensors. This huge resolution is particularly important for astronomical applications, like mapping a huge portion of the sky. Moreover, film is sensitive to X-rays (thus making it suitable for medical applications) and ultraviolet (e.g., spectroscopy). Thus the digital sensor had to gain grounds through exotic applications like outer-space and the military.

There arose the need for very small, durable and low-power sensors to replace the vidicon tubes for space applications like the LST (Large Space Telescope—later called as the Hubble), and other activities of JPL [1.9]. One of the major drawbacks of film based technology for space applications was the “fogging” of the film due to high energy cosmic particles, i.e., film was not radiation hard. The vidicon tubes, on the other hand, were slow in operation, and their lifetime was questionable.

Bell Labs introduced the CCD to the LST team in 1972. It was a 100×100 pixel sensor, with a very poor charge transfer efficiency. It was received by the team because of its large time-frame of operation, low power consumption, linearity and ability to output data in the digital domain. Moreover, it exhibited good radiation tolerance (compared to films). Soon, many groups including JPL, Fairchild, RCA, Texas Instruments etc were busy refining and optimizing the CCD. Its first success in conventional applications was in the field of astronomy; as a sensor in telescopes. Soon, CCDs gained a place in almost every branch of applied sciences.

Performance of early CMOS image sensors did not match up well with the then mature CCDs due to its high dark current and read-out noise.

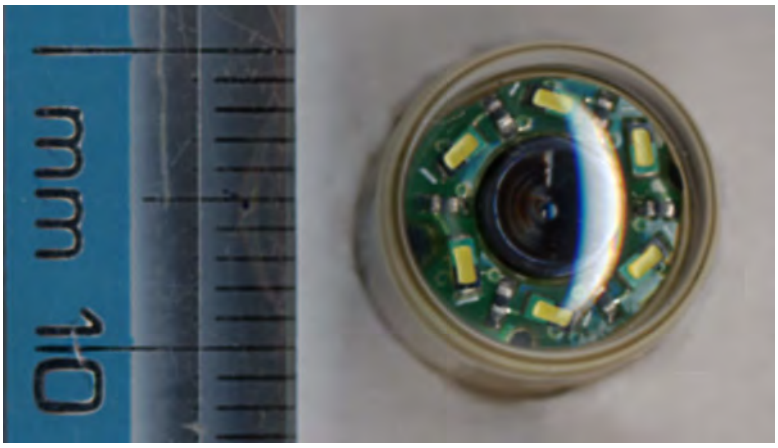


Fig. 1-4 *A capsule endoscope. The patient swallows this "imaging pill" that captures and transmits high resolution images for gastro-intestinal study. Requirements such as compact size, low power operation and SOC (System on Chip) are met through the use of a CMOS image sensor. From Wikipedia.*

Thus initial CMOS image sensor systems were limited to low-cost cameras and very specific applications including machine vision. In the late 1990s, however, the use of pinned photodiodes, charge transfer gates, microlenses etc, which were originally CCD concepts, helped revolutionise CMOS image sensors. As a result, they became more acceptable in both consumer as well as precision scientific applications.

CMOS image sensors can be realized as an SOC (System on Chip), thus rendering it useful for many customised applications. Moreover, compact size, low power/voltage requirements and standardised production meant it could meet many scientific requirements. These include low-light imaging, high-speed and high-dynamic range applications, three-dimensional range finding, target tracking, etc. Application fields include, but not limited to: bio-technology, medicine and medical sciences, information and communication technologies, astronomy and outer-space, spectroscopy, microscopy etc [1.7].

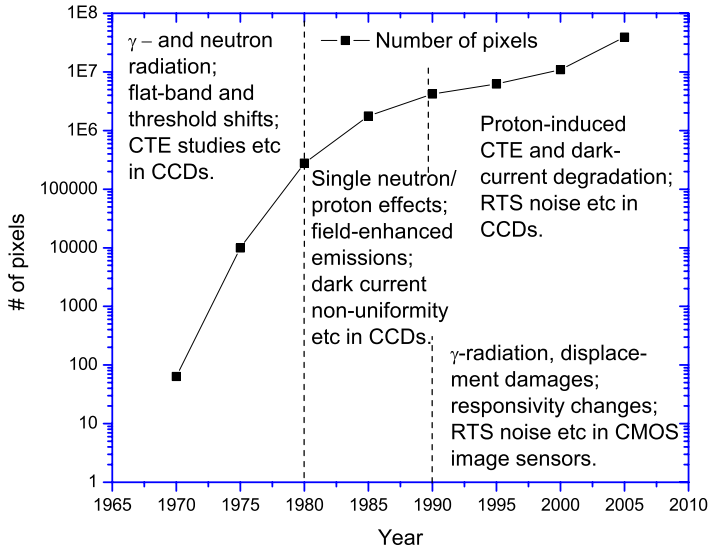


Fig. 1-5 *Development of solid-state sensor (judged by the pixel count) and the important radiation study undertaken during that period [1.9].*

One particular application that summarises the advantages of CMOS image sensors in a "nutshell" is *capsule endoscopy* (Figure 1-4).

In the following sections, the history of digital image sensors relevant to the topic of this thesis—study of radiation effects as well sensors for medical applications—will be discussed in detail.

Radiation effects on solid-state imagers

The research on the radiation tolerance of solid-state digital sensors was soon to follow their introduction, as they were to be deployed in radiation-harsh environments. Figure 1-5 traces the development of the image sensor (judged by the sensors pixel count) and the important radiation studies undertaken during that period.

In the 1970s, the investigation of radiation tolerance focused on neutron and γ-ray damage on the sensor. Parameters that were

observed include CTI (Charge Transfer Inefficiency), flatband shifts as well as dark current after irradiation. Some of the early attempts for a radiation tolerant CCD design have been covered in the excellent article by J. M. Killiany [1.10]. The important steps that the early investigators took to achieve a radiation tolerant image sensor include: n-buried channel devices, planar isolation techniques to minimize CTI and doped polysilicon for inter-electrode isolation.

With the invention of the MPP (Multi-Phased Pinned) CCDs in the 80s, surface traps could be filled with holes, leading to better dark current suppression and significant hardening towards ionizing damage [1.11].

With the increasing resolutions (800 × 800 pixels for the Hubble telescope), cosmetic quality assumed importance. In mid 1980s, single neutron and proton effects were studied. It was also discovered that elastic collisions in the high electric field regions in the CCD resulted in high dark current spikes of several orders of magnitude [1.12], [1.13], [1.14]. Researchers concluded that field-enhanced emissions were responsible for such drastic dark current spikes that were observed after irradiation. A decrease in the thermal activation energy was also observed which corroborated the findings.

In recent years, work has been done on radiation damage characterization of CCD sensors used in space telescopes like the Chandra, XMM Newton, the Hubble etc especially on the proton induced CTE degradation. Similar work has also been undertaken in the case of CMOS image sensors. Dark current and dark current non-uniformity, fixed pattern noise, and spectral response are the key degradation observed in CMOS image sensors. Flatband voltage shifts were found to be small due to the thin gate oxides employed in current CMOS technology [1.15].

Solid-state imagers for medical applications

The first use of digital imagers for medical purposes started in the late 1980s [1.16]. The first device for dental imaging, for example, was the *Trophy radiology system* introduced in 1987 in France [1.17]. The first version of the dental sensor was very thick and had an active area of only 19 × 28 mm. This was capable of producing the image of a single molar tooth.

In 1979, [1.18] developed a CCD system for direct detection of single X-ray photons. The pixels were 30 μm in size and had a resolution of 100 × 100. It used a buried channel, front-illuminated sensor. A video rate X-ray imager was conceived by [1.19] in 1987. This also used direct detection especially for soft X-rays. The researchers also recommend in their paper the use of phosphor plates to reduce blooming effects and improving radiation tolerance.

In 1990, [1.20] presented the first results of a X-ray imaging with scintillating glass and optical fibre coupling. The scintillating plate was coated with cerium activated glass (GSI). It was observed that the plate had a high radiation tolerance (up to 10^8 rads) due to the strong electron affinity of cerium which inhibits the formation of color-centres. The authors of [1.20] also envision in their report, an immediate use of their invention in medical imaging.

Following the steps of [1.20], [1.21] reported an X-ray area imager sensor consisting of an intensified CCD camera which utilizes a terbium-doped glass plate as the scintillator. Optical fibres were used for photon coupling and to reduce optical cross-talk. Soon the field caught on with many reports on improved scintillators, cross-talk and even portability [1.22].

To study a large area with a digital imaging system for bio-medical applications, large area pixels are required. This reduces the resolution of the sensor. To circumvent this problem, multiple-CCDs arrays which are small in size are generally employed for reducing costs. Similarly, since many solid-state imaging solutions utilize a less-than-ideal scintillation screen to convert the incoming X-rays to visible light, sensitivity of the sensor is paramount.

The most important drawback of the CCD based detectors is CTE (Charge Transfer Efficiency) degradation due to some of the high energy radiation that happens to be incident on them. Radiation damage also leads to defective pixels and inoperative columns. Another problem of CCD based system is blooming effects due to the thick absorption regions present in the CCD, which absorbs part of the direct X-rays [1.17].

An alternate CMOS based X-ray detector was reported by Fossum et al. [1.24] and later by Abdalla et al. [1.17]. The latter concluded that the detector must be at least 20 × 30 mm^2 and that the pixel size need

not be more than $50 \times 50\ \mu m^2$ for X-ray imaging in medical (dental) applications, based on the following facts:

- The scintillator on top of the image sensor as well as the distance between the object and the sensor determines the maximum resolution obtainable by the detection system. This sets the minimum size of the pixel.

- On the other hand, the intensity of light emitted by the scintillator decides how big the pixel should be. A larger pixel size is required when the emitted photons are scant.

1.2 Thesis objectives

The objective of this thesis is to study the radiation and device physics aspects of CMOS image sensors fabricated in the 0.18-μm technology. Aggressive sub-micron technologies are not optimized for imaging applications. The technological drive behind the IC fabrication industry is the need for high density integration of digital circuits. While semiconductor fabrication technology progresses (judged by the minimum feature size) according to the Moore's law (Figure 1-6), several phenomenons hitherto unknown begin to appear for imaging applications. This thesis aims to study the two main points given below, in the context of deep sub-micron technology as applicable to image sensor. The main aims of this thesis are:

- Investigating the effect of γ-ray radiation on 4-T CMOS image sensors.

- The possibility of realizing a CCD like sensor in standard 0.18-μm CMOS technology.

The first point is also a precursor to a project presently being perused at TUDelft: a sun-sensor for attitude determination, and parallel to other projects on radiation hardness.

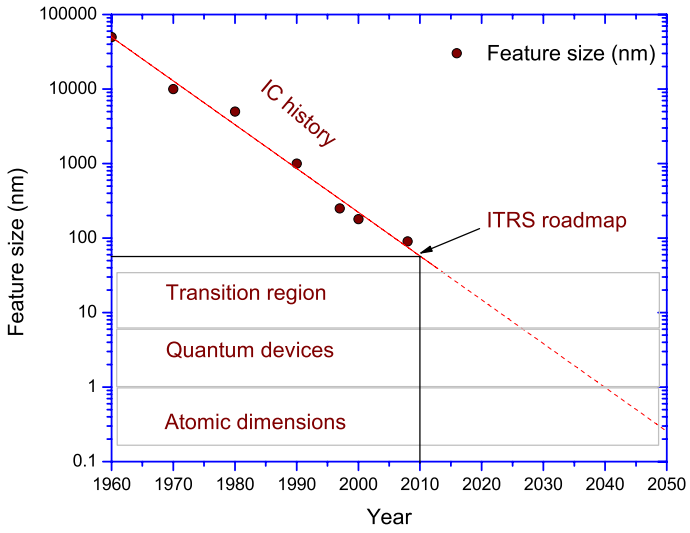


Fig. 1-6 *Evolution of CMOS process technology as a function of year. The ITRS (International Technology Road map for Semiconductors) road map is represented by the straight line [1.23].*

The second aim of this thesis, i.e., a CCD like sensor in standard 0.18-µm CMOS technology is self-contained. However, many semiconductor fundamentals and models used in the study of radiation effects are carried over to this study. Moreover, a study of the radiation characteristics of CMOS technology, particularly to high-energy photons, will be both logical and supplementary while dealing with sensors for medical imaging.

Radiation effects in CMOS image sensors

This part of the thesis is devoted to studying the effect of radiation on the electrical as well as optical performance of 4-T CMOS image sensors. These sensors are state-of-the-art. This investigation is carried out from the view point of device physics. Only γ-ray radiation effects have been studied and transient effects have not been considered. The choice of γ-ray is due the fact that the results

obtained can also be used to predict the radiation effects due to X-rays used in medical applications (since both are high-energy photons). This helps in designing a novel sensor discussed as the next objective of this thesis. The results also help to understand the weak points of the sensor that lead to its degradation, and ideas to improve the sensor for applications pertaining to harsh environments.

Though there have been many studies on radiation tolerance of image sensors in the past, the work presented here is a pioneering effort undertaken to study radiation tolerance of 4-T CMOS image sensors in the 0.18-μm technology. In addition, it also bridges many knowledge gaps existing in the other works. For example, a quantitative analysis of the radiation induced bulk/surface degradation has not been done yet. The fundamental aspects of the degradation are studied in this work using a very simple structure called as the gated-diode. Similarly, the effect of radiation on some of the oxides used in the fabrication process has been analyzed and studied using models that were developed. The measurements for the optical degradation are carried out using FTIR (Fourier Transform of Infrared) as well as ellipsometry.

Similarly, the spectral response of pinned-photodiodes has been analyzed and an analytic model has been derived. The derived model will help to understand not only the operation of the image sensor, but also the mechanism of its degradation due to radiation.

CCD like image sensor in standard CMOS technology

This part of the thesis investigates the possibility of utilizing the 0.18-μm standard CMOS technology for fabricating a CCD targeted at medical applications. The major hurdles faced by current solid-state image sensors for medical applications include the issues with dynamic range, resolution and radiation hardness. Dynamic range in radiography is important because of the high contrast between the dark (flesh and tissue) and the light (bones etc) part of the image. Similarly, there is a trade-off between the resolution and the dynamic range. A larger pixel implies a lower resolution and vice-versa. In our approach, we utilize split-gates to perform clever operations inside the pixel. This is possible due to the very small gaps that can be formed between polysilicon gates in current

semiconductor technologies. This helps the surface potentials under the gates to merge, and allow charge transfer. By carefully choosing the mode of operation, both dynamic range as well as resolution of the pixel can be enhanced.

There have been some efforts carried out in this direction in the past. But the efforts were not fully fruitful due to the lack of technology as well as incomplete analysis. This thesis hopes to generate interest and spearhead the fusion of CCD and CMOS technologies so that the advantages of both of these can be harnessed. Needless to say, this study also comes at a time when several groups have started to realize the advantages and are working towards this goal (for e.g. see [1.25]).

Since the conversion efficiency of the scintillator layer in front of the sensor is not 100%, there is still high-energy radiation incident on the sensor that could affect its performance. Therefore, the results obtained in the previous discussion on radiation tolerance can be utilized effectively in the present part.

1.3 Organization of the Thesis

Chapters 2 to Chapter 4 concern mainly with the theory and experiments carried out in the topic of radiation hardness. It is advisable to read them in that order. Chapter 5 is more or less a self contained work, though some background information will be found in the first two chapters. All chapters contain a brief summary of the important concepts presented in that particular chapter.

Chapter 2 introduces the gated-diode (GD). Concepts such as generation lifetime and surface recombination velocity are presented and experimental results obtained through the GD are discussed. Further, thermal and diffusion leakage currents are presented together with the Arrhenius plots. Other important semiconductor concepts useful later in the thesis are also presented in this chapter.

Chapter 3 deals with the fundamentals of the 4-T CMOS image sensor. The basic structure as well as the working principle of the sensor is presented. An analytic model of the spectral characteristics of pinned photodiode is derived and the sensitivity of the sensor to

various variables is studied. This model is used in chapter 4 for a better understanding of the degradation of spectral characteristics of the sensor due to irradiation. The fundamentals of dark current leakage mechanisms in the sensor are introduced in this chapter. This exposes the reader to the necessary mathematical as well as theoretical background required to read ensuing chapters. This chapter is concluded with some background information on electric fields in advanced image sensors, and its effect on sensor performance.

Chapter 4 discusses the experiments carried out on the gated-diodes as well as the 4-T CMOS image sensors. Experimental results on both the electrical as well as optical degradation of the image sensor due to radiation is presented. The effect of various STI (Shallow Trench Isolation) parameters on the radiation damage is investigated. FTIR and ellipsometry are used to identify the degradation in oxides. The chapter is concluded with a short description of the role of electric fields on enhanced emission and its likelihood of increasing the sensitivity of the sensor towards radiation effects. The results are corroborated with the theory presented in previous chapters.

Chapter 5 is a study on the feasibility of a CCD like structure in standard CMOS technology. As mentioned earlier, such a fusion would enable a sensor to acquire the merits of both these technologies. First, the basic concepts as well as some simulation studies will be presented. The design of the pixel structure and other details follows this. Experimental results are then discussed and the concept is proven. Finally conclusions are drawn based on the results.

Chapter 6 summarises the thesis, and presents some possible future work in the direction of the study presented in this thesis.

1.4 References

[1.1] http://www.pacitti.org/books_00199102.htm

[1.2] J. F. Staal, “Negation and the Law of Contradiction in Indian Thought: A Comparative Study”, Bull. Sch. Orient. Afr. Stud., Univ. of London, Vol. 25, No. 1/3, pp. 52-71, 1962.

[1.3] http://www.videopreservation.stanford.edu/library/brief_history_of_imaging_technology_v10.pdf

[1.4] W. Lefevre, “Exposing the Seventeenth Century Optical Camera Obscura”, Endeavour, Vol. 31, No. 2, pp. 54-58, 2007.

[1.5] http://en.wikipedia.org/wiki/Johann_Zahn

[1.6] http://www.digicamhistory.com/Boyle%20and%20Smith.html

[1.7] J. Ohta, “Smart CMOS Image Sensors and Applications”, pp. 1-9, CRC Press, 2008.

[1.8] http://www.kodak.com/US/en/corp/kodakHistory/index.shtml

[1.9] J. C. Pickel et al., “Radiation Effects on Photonic Imagers - A Historical Perspective”, IEEE Trans. Nucl. Sci., Vol. 50, No. 3, pp. 671-688, 2003.

[1.10] J. M. Killiany, “Radiation Effects on Silicon Charge-Coupled Devices”, IEEE Trans. Comp. Hyb. Manuf. Tech., Vol. CHMT-1, No. 4, pp. 353-365, 1978.

[1.11] J. R. Janesick, “Scientific Charge-Coupled Devices”, SPIE Press, pp. 50, 232, 2001.

[1.12] P. W. Marshall et al., “Displacement Damage Extremes in Silicon Depletion Regions”, IEEE Trans. Nucl. Sci., Vol. 36, No. 6, pp. 1831-1839, 1989.

[1.13] J. R. Srour and R. A Hartmann, “Enhanced Displacement Damage Effectiveness in Irradiated Silicon Devices”, IEEE Trans. Nucl. Sci., Vol. 36, No. 6, pp. 1825-1830, 1989.

[1.14] G. R. Hopkinson and Ch. Chlebek, “Proton Damage Effects in an EEV CCD Imager”, IEEE Trans. Nucl. Sci., Vol. 36, No. 6, pp. 1865-1871, 1989.

[1.15] W. J. Snoeys, T. A. Palacios Gutierrez, and G. Anelli, “A New NMOS Layout Structure for Radiation Tolerance”, IEEE Trans. Nuc. Sci., Vol. 49, No. 4, pp. 1829-1833, 2002.

[1.16] M. Hoheisel “Review of Medical Imaging with Emphasis on X-ray Detectors”, Nuc. Instr. Meth. Phys. Res. A, Vol. 563, No. 1, pp. 215-224, 2006.

[1.17] M. A. Abdalla, C. Frojdh, and C. S. Petresson, “A CMOS APS for Dental X-ray Imaging using Scintillating Sensors”, Nuc. Instr. Meth. Phys. Res. A, Vol. 460, No. 1, pp. 197-203, 2001.

[1.18] R. C. Catura and R. C. Smithson, “Single Photon X-ray Detection with a CCD Image Sensor”, Rev. Sci. Instr., Vol. 50, No. 2, pp. 219-220, 1979.

[1.19] A. Benetello et al., “A Position Sensitive Detector Using an Interline Transfer Imaging CCD at Standard TV Rate and Room Temperature”, Nuc. Instr. Meth. Phys. Res. A, Vol. 258, No. 2, pp. 235-241, 1987.

[1.20] G. Zanella and R. Zannoni, “X-ray Imaging with Scintillating Glass Optical Fibres”, Nuc. Instr. Meth. Phys. Res. A, Vol. 287, No. 3, pp. 619-627, 1990.

[1.21] P. Ottonello et al.,”An X-ray Area Detector with Scintillating Glass Fiber Optics”, Nuc. Instr. Meth. Phys. Res. A, Vol. 323, No. 1-2, pp. 485-488, 1992.

[1.22] B. D. Sawicka, P. Reynolds, and K. Sonnenburg, “Portable Digital Electronic Radiography System with a Solid-State-imaging Detector”, Nuc. Instr. Meth. Phys. Res. A, Vol. 428, No. 2-3, pp. 608-615, 1999.

[1.23] J. D. Plummer and P. B. Griffin, “Material and Process Limits in Silicon VLSI Technology”, IEEE Proc., Vol. 89, No. 3, pp. 240-258, 2001.

[1.24] E. R. Fossum, R. H. Nixon, and D. Schick, “A 37×28 mm^2 600-k Pixel CMOS APS Dental X-ray Camera-on-a-chip with Self-Triggered Readout”, ISSCC, pp. 172-173, 1998.

[1.25] K. Fife, A. El. Gamal, and H.-S.P Wong, “A 0.5 μm Pixel-Frame Transfer CCD Image Sensor in 110 nm CMOS”, IEDM, pp. 1003-1006, 2007.

Device physics—Basics

This chapter introduces the basics of semiconductor physics that will serve as a background for ensuing chapters. A simple device structure for semiconductor characterization—the gated-diode (GD)—will be presented and some experimental results which compliment the theory will be discussed. Further, the concept of Arrhenius plots will be explained. The Arrhenius plot helps to determine the thermal activation energy of the semiconductor device under study. The presence of traps—both in the bulk as well as in the interface—increases the thermal generation and hence the leakage current of silicon sensors. A mathematical treatment of the leakage current process will help in understanding the different variables involved. Further, a simple method to profile the energy dependent traps at the Si-SiO_2 interface using the GD will be introduced. This technique, called as the sub-band photonic GD method, uses infrared (IR) to excite the traps in the interface. The resulting trap-induced leakage current is used to extract the energy dependent profile of surface traps.

2.1 Semiconductor device physics—Components of an image sensor

Image sensors in a CMOS technology, or CCD for that matter, consists of either a *photodiode* or a *photogate* as its primary photo-sensing element [2.1]. A photodiode is formed by using one or more doped semiconductor layers, usually an n- over a p-region. In CMOS technology, the p-type region is the *epi-layer* region that is formed on top of a much higher doped *substrate* region (which is also a p-type). The sandwich of contrasting layers (n- and p-regions) creates a "depletion" region in their interface, where the semiconductor is free of carriers (electrons and holes) and consists only of immobile ions. This region is also called as the *space charge region* (SCR). If a reverse bias is applied across this diode, the thickness of the depletion width will increase as the square root of the applied voltage. It is important to note that the electric field due to the applied reverse bias would be contained within this depleted region. The carriers that are generated in this region due to the incoming photons would be immediately separated (collected) by the electric field due to the "drift" process. This implies that the electrons would move towards the n-region (highest potential) and the holes, to the p-type region (lowest potential). The carriers that are generated at the neutral regions (n and p) due to impinging photons would "diffuse" to the depletion region, and separate due to the electric field. The drift process is more effective and fast compared to the diffusion process [2.1], [2.2].

A photogate on the other hand, consists of a MOS (Metal-Oxide-Semiconductor) capacitor. The metal region is formed using a highly-doped polysilicon material, usually an n-type. When a suitable positive potential is applied at the gate with respect to the substrate (p-type), a depletion region is formed underneath the gate region in the semiconductor. The polysilicon gate region is very thin (~150 nm), so that photons can penetrate through it—albeit suffering some absorption in this process. The incoming photons generate electron/hole pairs according to the process outlined above. Thus the fundamental units of a CMOS image sensor pixel are the diode and the gate.

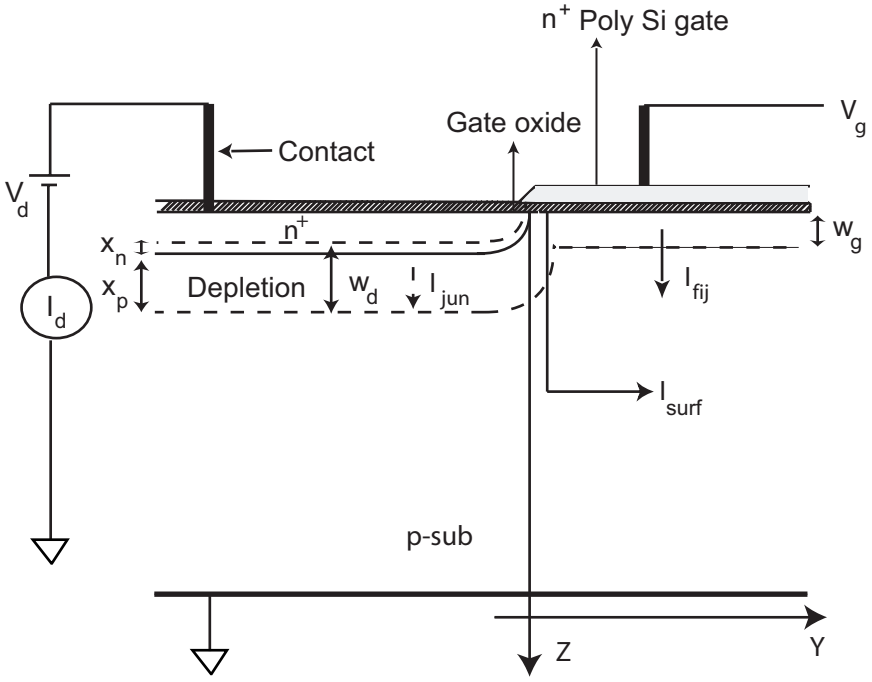


Fig. 2-1 *The gated-diode schematic and the different leakage components in the device.*

A simple device that contains these two elements is the *gated-diode* or the *gate-controlled diode* (Figure 2-1). Many device physics aspects of an image sensor pixel can be comprehended by the use of this structure. The rest of the thesis deals with the different techniques that can be employed using the GD for semiconductor parameter extraction. Along with this, explanation will also be provided for various semiconductor variables that are to appear later in this thesis.

2.2 The gated-diode

Gated-diodes (GD) or gate-controlled diodes are an important tool in the characterization of semiconductor bulk as well as the surface. The gated-diode measurements date back to the earliest of the semiconductor industry and have been discussed in the literatures for quite some time. It was first proposed by A. S. Groove and D. J. Fitzgerald in the year 1966 and since then it has been used to characterize the surface as well as the bulk properties of silicon devices [2.3]. Of importance are the bulk and the gate leakage currents, the surface related leakage mechanisms characterized by the surface recombination velocity, the mapping of the interface as well as the bulk defects, hot-carrier effects, short-channel effects, and radiation effects to mention a few.

The GD technique evolved as an extension to the MOS capacitor studies in silicon devices that were used to characterize the surface effects. But while the pulsed capacitance method is a non-steady state phenomenon and its interpretation is difficult, results obtained through gated diode measurements are straightforward and the current components can be evaluated more easily [2.4], [2.5].

The gated-diode (GD) is a simple structure that consists of a p-n diode region and a gate region which overlaps the diode, as shown in Figure 2-1. The diode is reverse biased with a very small voltage V_d, creating a depletion region (w_d) around the junction. A very small reverse current (I_{jun}), flows through the diode as a result of excess carrier generation in the depletion region (I_{dp}^{jun}) and in the neutral-bulk (I_{diff}) region. At room temperatures, however, the diffusion component can be neglected. The application of a reverse bias V_d on the diode lowers the *quasi-Fermi level* for electrons, and thus modulating the gate voltage V_g required to induce an inversion [2.10]. In this non-equilibrium case and the simplifying assumption that potential variation in a direction parallel to the surface (Y axis) is negligible, sweeping the voltage of the overlapping gate V_g of the GD through the regimes of *accumulation*, *depletion* and *strong inversion* while monitoring the reverse current I_{jun}, helps resolve the surface leakage component I_{surf} as well as the bulk (field-induced) leakage component I_{fij}.

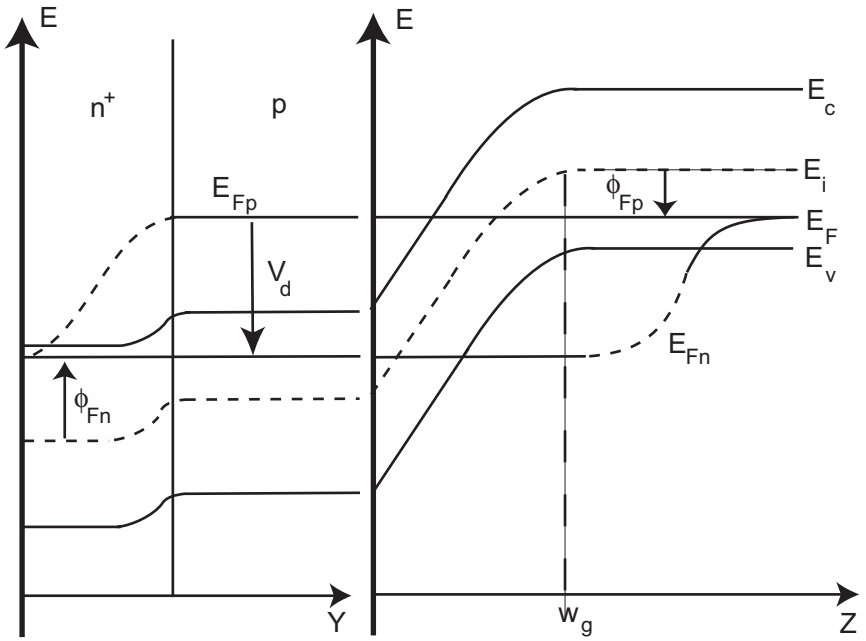


Fig. 2-2 *The energy band diagram in a GD in both Y (Z = 0) and Z (Y = gate location) directions under inversion condition [2.12].*

These leakage components help establish two important device parameters, s_0—the *surface recombination velocity* and τ_0—the *generation lifetime* of minority carriers. They are temperature-dependent parameters, whose temperature dependence is determined by the energy position of the dominant generation centre and temperature dependencies of the centre capture cross sections [2.6]. The energy band diagram along the length (Y axis) and the depth (Z axis) for a GD in strong inversion is shown in Figure 2-2 [2.12]. In the figure, E_C *i*s the conduction band, E_V, the valence, E_i is the intrinsic level, E_F the Fermi level, E_{Fn} and E_{Fp} the quasi-Fermi levels for electrons and holes respectively, ϕ_{Fn} and ϕ_{Fp} the quasi-Fermi potentials of electrons and holes respectively.

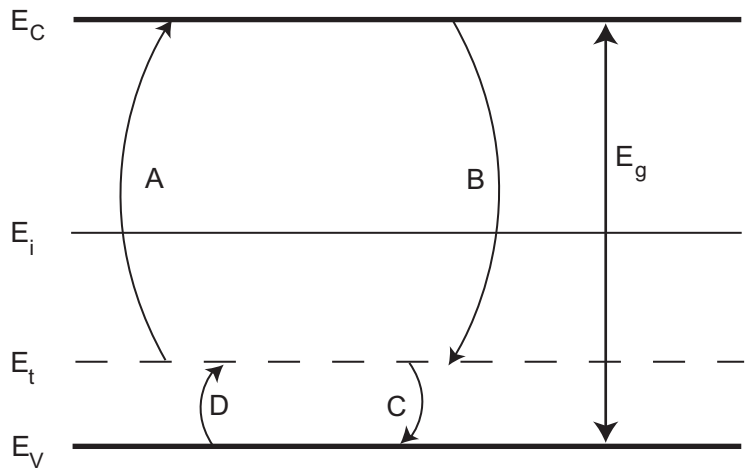


Fig. 2-3 *Possible electron transitions via a recombination centre at energy* E_t.

2.2.1 Generation/recombination phenomenon—Basics

Though semiconductor materials are of the highest quality, they are not perfect. They might have crystal defects such as interstitials (excess semiconductor atoms in the crystal lattice), vacancies (missing semiconductor atoms in the crystal lattice), dislocations (crystal structure imperfections), as well as traces of impurity atoms [2.2]. These defects and impurities create additional energy levels in the energy bandgap. Consider a level, E_t, in the bandgap (Figure 2-3). This permitted level can lose an electron to the conduction band (A) called as *electron generation*; gain an electron from the conduction band (B) called as *electron recombination*; loose a hole to the valence band (C) called as *hole recombination*; or gain a hole from the valence band (D) called as *hole generation*. These permitted levels could be either acceptor levels (negative when empty) or donor levels (neutral when empty). These addition levels are also known as *generation-recombination centres* or in short, *recombination centres*. The recombination events are called as SHR (Shockley-Read-Hall) recombination events. An analytic expression for the recombination rate for electrons and holes—U_n and U_p can

be written when there are recombination centres in the bandgap as [2.2]:

$$U = \frac{pn - n_i^2}{\tau_p\left(n + n_i e^{\left[\frac{E_t - E_i}{kT}\right]}\right) + \tau_n\left(p + n_i e^{\left[\frac{E_t - E_i}{kT}\right]}\right)} \tag{2-1}$$

with τ_n and τ_p defined as:

$$\tau_n = \frac{1}{N_t v_{th} \sigma_n} \text{ and } \tau_p = \frac{1}{N_t v_{th} \sigma_p} \tag{2-2}$$

where τ_n and τ_p are the *lifetimes* of electrons and holes in steady state conditions respectively, σ_n and σ_p the *capture cross section areas* of electrons and holes respectively, N_t the volume density of traps, p and n are the electron and hole concentrations, n_i the intrinsic carrier concentration, E_i the mid gap energy level, E_t the trap energy level, v_{th} the thermal velocity of electrons or holes, k the Boltzmann constant, and T the absolute temperature. From (2-1), we find that the recombination rate is directly proportional to $pn - n_i^2$. U can be regarded as a force that tends to bring the pn product back to its equilibrium value; n_i^2. The three conditions that U exhibits are [2.2], [2.7]:

- $U = 0$ if $pn = n_i^2$ (equilibrium)
- $U > 0$ if $pn > n_i^2$ (recombination)
- $U < 0$ if $pn < n_i^2$ (generation)

It should be noted that the recombination rate is highest when the energy level of the recombination centre E_t is very near to mid gap ($E_t \approx E_i$). The condition $pn \to 0$ is approximated at the SCR, signifying a generation process [2.7].
The electron or hole capture cross section area (cm^2) is a measure of how close the electron or hole must be to a centre in order to be

captured by it. Assuming that the electron and hole capture cross sections are equal ($\sigma_n = \sigma_p = \sigma_0$), the recombination rate takes the following form [2.2], [2.3]:

$$U = \frac{pn - n_i^2}{\tau_0\left(p + n + 2n_i \cosh\left[\frac{E_t - E_i}{kT}\right]\right)} \tag{2-3}$$

where $\tau_0 = \frac{1}{N_t v_{th} \sigma_0}$

The recombination rate of excess carriers occurs not only within the bulk of the semiconductor crystal, but also at the surface of the crystal. This is because of the interrupted periodicity at the surface of the crystal. An expression very similar to (2-1) can be derived for the surface recombination rate (S). With the assumption that the capture cross sections are equal, it can be written as [2.2], [2.3]:

$$S = \frac{\sigma_0 v_{th} N_{st} (p_s n_s - n_i^2)}{p_s + n_s + 2n_i \cosh\left[\frac{E_{st} - E_i}{kT}\right]} \tag{2-4}$$

where p_s and n_s are the electron and hole concentrations at the surface respectively, N_{st} is the concentration of surface recombination centres, and E_{st} is the their energy.

The surface recombination velocity, s, can be related to S as:

$$S_n = s_n(n - n_0) \text{ and } S_p = s_p(p - p_0) \tag{2-5}$$

where n_0 and p_0 are the equilibrium electron and hole concentrations, and s_n and s_p are the surface recombination velocities of electrons and holes respectively.

The surface generation is maximum for a depleted surface—where n_s and p_s are small. The surface recombination velocity at the depleted interface is usually represented as s_0.

2.2.2 Surface and bulk leakage currents under the GD gate region

The ideal GD curve representing the contribution of the different leakages to its response is shown in Figure 2-4. A mathematical treatment of these leakage components is carried out below.

Surface leakage current

The diode surface leakage current is the leakage current that is generated in the region where the depletion region touches the surface, and can be mathematically stated as [2.8], [2.9]:

$$I_{surf} = qn_i A_{SD'} s_0 \tag{2-6}$$

where $A_{SD'}$ is the depleted surface area and s_0 is the surface recombination velocity. The recombination at the surface is usually described by considering it as a plane sink, with a gradient of carrier concentration close to it. For cases where the gate length is larger than the gate-diode overlap region given by A_{SD}, $A_{SD'} = A_{SD} + A_{gate} \approx A_{gate}$.

Field-induced leakage current in the bulk

The current I_{fij} is due to the generation via the G-R (Generation-Recombination) centres in the depletion region of the field-induced junction close to the surface under the gate and hence provides information about the carrier lifetimes in this region of interest [2.11], [2.12]. This current can be expressed as [2.3], [2.9]:

$$I_{fij} = \frac{qn_i A_{gate} w_g}{\tau_0} \tag{2-7}$$

where w_g is the width of the depletion region under the gate region and τ_0 is the generation life time of minority carriers in the depletion region in the bulk under the gate-region. The surface analogue of a minority carrier lifetime in the bulk, s_0 provides a conveniently homogeneous boundary condition for the excess minority carrier con-

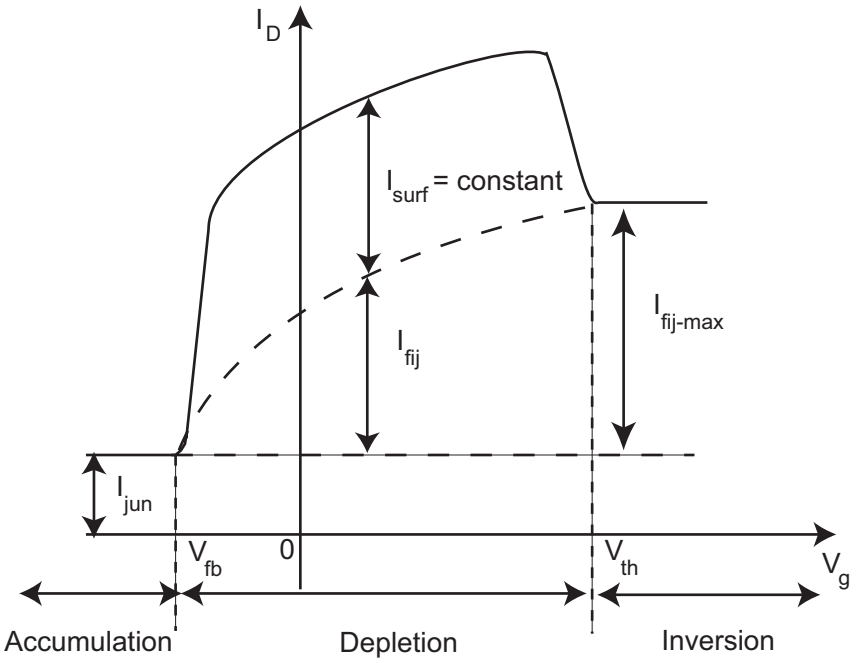


Fig. 2-4 *The ideal GD curve and its leakage currents components.*

centration. Both s_0 as well as τ_0 can be related to the trap density D_{it} (in the interface) or D_t (in the bulk) by [2.3]:

$$s_0 \text{ as well as } \frac{1}{\tau_0} = \sigma v_{th} \pi k_B T D_{it \text{ or } t} \tag{2-8}$$

where σ is the effective capture cross-section of traps in the surface interface or in the bulk ($\sigma = \frac{1}{2}\sqrt{\sigma_n \sigma_p}$, where σ_n and σ_p are the capture cross sections for electrons and hole traps respectively), v_{th} is the thermal velocity (10^7 cm/s), D_{it} is the trap density in the interface and D_t the trap density in the bulk ($cm^{-2}\,eV^{-1}$), and k is the Boltzmann constant.

Leakage current in the diode depletion region

When the gate is held in the accumulation regime, the leakage current generated is from the depletion region of the reverse biased diode. This leakage current can be expressed as:

$$I_{dp}^{jun} = \frac{qn_i w_d \times A_{diode}}{\tau_0} \tag{2-9}$$

where q is the electronic charge, n_i is the intrinsic carrier concentration at a temperature T, w_d the width of the depletion layer ($w_d = x_n + x_p$), A_{diode} is the diode area and τ_0 is the generation life time.

2.2.3 GD design and experiment

Figure 2-5 shows the actual structure of the GD that was fabricated. Since the leakage currents obtained will be quite small, it is important to fabricate devices with very large areas so that appreciable leakage currents could be obtained through the structure. Thus devices were fabricated with an area of at least 300 × 300 μm^2. Similarly, from the values obtained through the literature, it was realized that s_0 could vary from a few cm/s to 1000 cm/s, while τ_0 could vary from a few μs to many ms. Keeping these in mind and solving the fundamental GD equations discussed above, it was decided that to obtain an appreciable "step" in the GD response, the gate as well as the diode areas need to be "comparable". In the design, the areas were chosen to be equal. The GDs are fabricated in the form of finger gates called *finger gated-diodes* (FGDs). The diodes and gates are connected in series. The gate and the diode length were chosen to be 1 μm. The finger gates thus preserve the required gate (diode) area to gate (diode) length to extract the necessary semiconductor parameters. For the present study, FGD structures were fabricated in the Philips' 0.18-μm CMOS technology. The gate oxide thickness of the GDs for the present study was 4 nm.

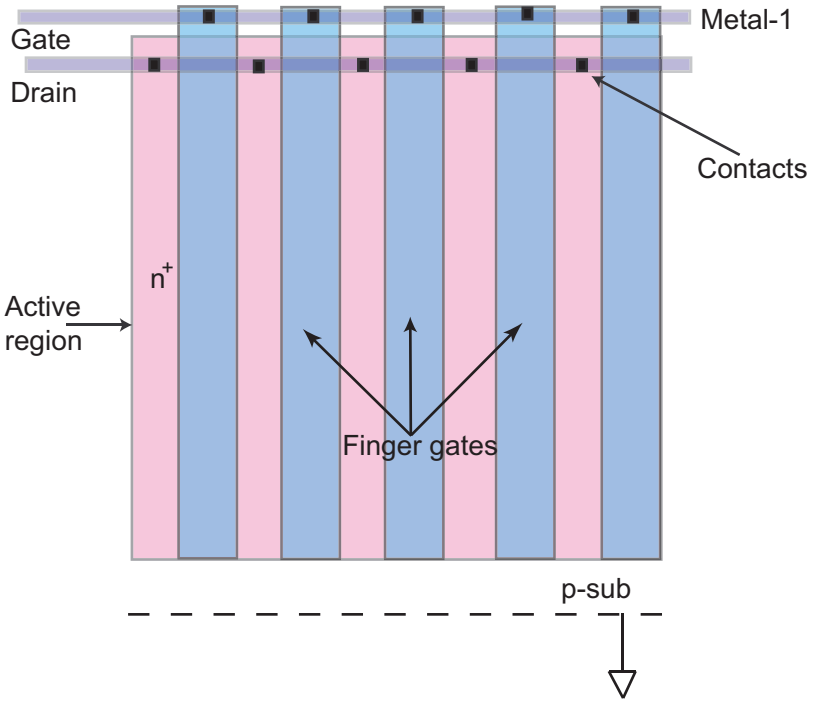


Fig. 2-5 *The finger gated-diode (FGD) layout.*

The n^+ diodes and the overlapping poly-Si gates were fabricated on a p-epi layer ($N_A \sim 10^{15}$ cm^{-3}) and STI (Shallow Trench Isolation) technique was used to isolate individual devices in the wafer.

Figure 2-6 shows the experimental setup used for the FGD experiment. The measurements were carried out on wafer-level in the dark, utilizing a probe station. Since the leakage currents are very low, special precautions were taken during the measurements. An *Agilent 4156C* parameter analyzer in conjunction with SMUs (Source Monitoring Units) was used for generating, sweeping and recording the FGD signals. An Attoguard^{TM} system was used for adequate isolation of the DUT (Device Under Test) from external interferences.

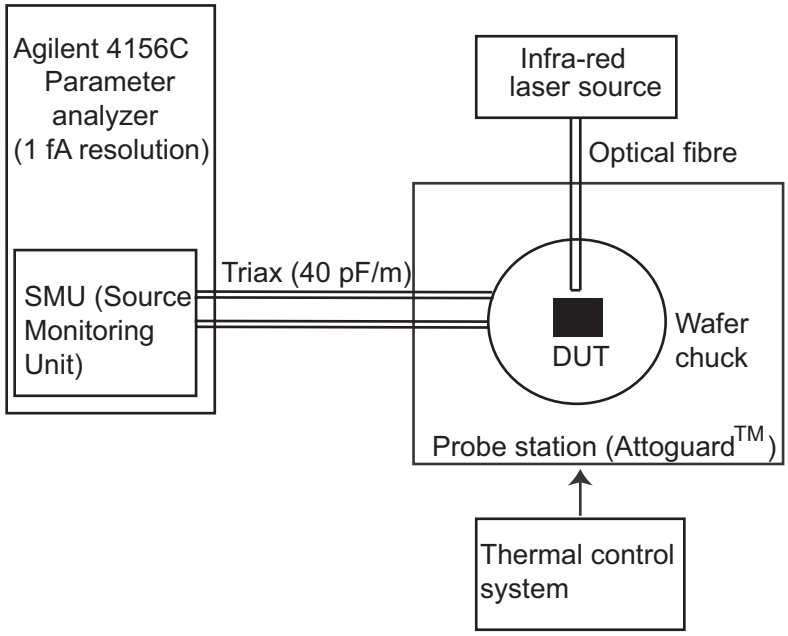


Fig. 2-6 *The setup for characterizing the FGD structures.*

A temperature control unit was used to control the ambient temperature inside the wafer enclosure. The gate voltage sweep was carried out in steps, ensuring a DC condition at each gate voltage. This was to avoid any high-frequency effects. The measurements were recorded at each gate voltage after adequate averaging to minimize noise. For measurements involving the infra-red laser, a fibre optic cable was introduced into the probe station, after ensuring there was no external light leakage present.

Figure 2-7 shows the I-V characteristics of the FGD. When the gate is sufficiently negative, the region under the gates is in strong accumulation. The holes that accumulate passivate the surface interface traps. The leakage current obtained from the FGD under this circumstance is limited to the diode leakage current. On increasing the gate voltage towards the flatband voltage (V_{fb}), the fast-centres at

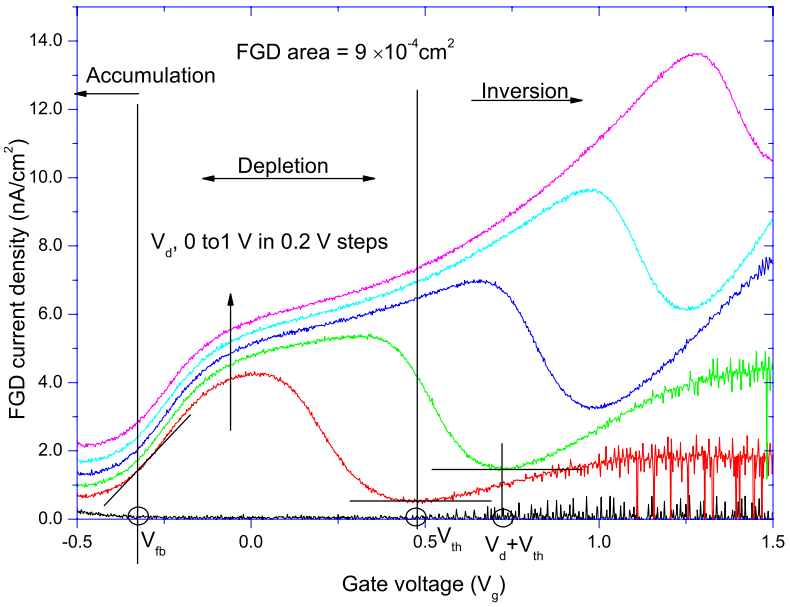


Fig. 2-7 *The FGD I-V curves obtained via the experiment.*

the Si-SiO_2 interface and in the field-induced region under the gate contribute to the increase in the leakage current until threshold ($V_{th} = V_d + V_{fb} + 2\phi_B - Q_{sd}/C_{ox}$) where ϕ_B is the bulk Fermi potential, Q_{sd} is the "depletion charges" [2.2]. At threshold however, the inverted surface under the gate again passivates the traps. The signal obtained in this case is the leakage currents from the diode and the field-induced region under the gates. These three regimes can be used to resolve the leakage currents from the three different regions of the structure namely, the diode, the surface as well as the bulk region under the gates. More importantly, using (2-6) and (2-7), we can resolve both s_0 as well as τ_0. The different parameters extracted using the FGD and their relationship to fundamental parameters is highlighted in Table 2-2.

It should be noted that a small depleted region underneath the gates will interact with the STI located at the periphery of the FGD structure. The area of the interaction is estimated to be ~ 0.06% of the

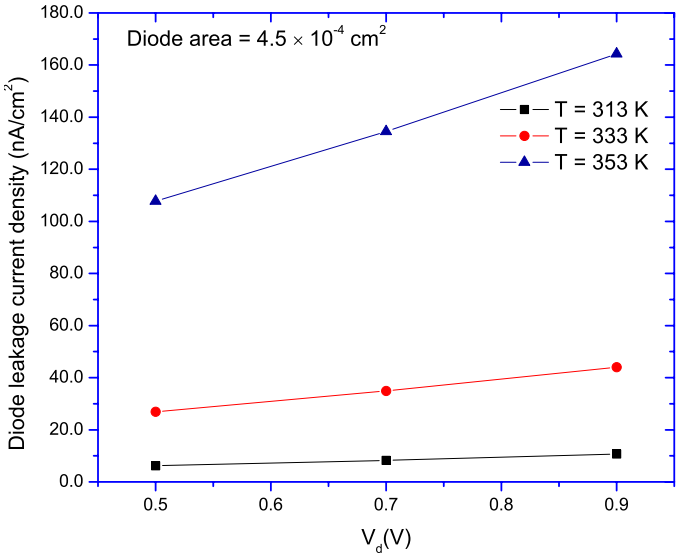


Fig. 2-8 *The I-V curve of the diode in a FGD (keeping the gate in accumulation) at three different temperatures.*

total gate area. The contribution from the STI is thus coupled with I_{fij}, and the extent of this contribution is decided by the STI properties. If the STI surface is "heavily" damaged, the contribution from the STIs can be significant. Using the current FGD structures, it is not possible to separate the STI leakage component from I_{fij}. The STI will be treated in more detail in Chapter 3. The influence of radiation on both the STI as well as the FGD structures will be discussed in detail in Chapter 4.

2.2.4 Diode leakage currents in the FGD

The diode leakage currents can be studied by keeping the gate area in accumulation. In this way, the diode region is isolated from the gate region. The leakage from the diode I_{jun}, can be expressed as the sum of the diffusion (I_{diff}) as well as thermal generated (I_{jun}^{dp}) given as [2.13]:

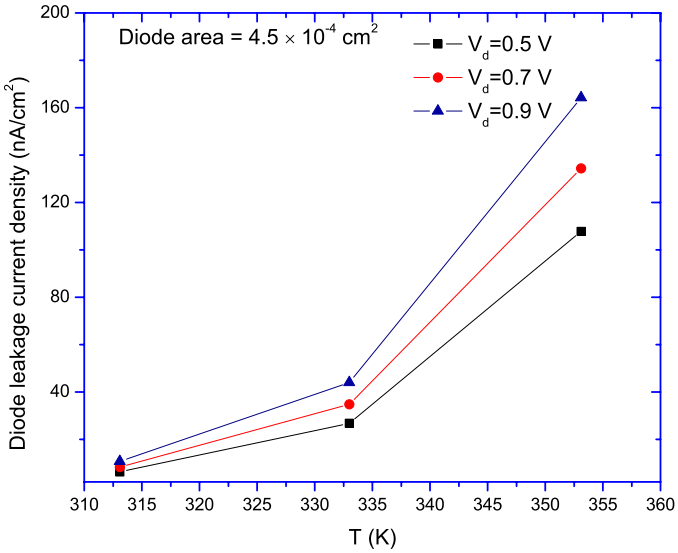


Fig. 2-9 *The leakage current of the FGD diode region (keeping the gate in accumulation) as a function of temperature.*

$$I_{jun} = I_{diff} + I_{jun}^{dp} \tag{2-10}$$

As stated above, at room temperatures the diffusion component can usually be neglected. However, at higher temperatures, there is a non-negligible contribution due to diffusion from the neutral p- and n-regions of the diode.

Figure 2-8 shows the leakage current as a function of reverse bias applied on the diode while Figure 2-9; the temperature behaviour of the diode leakage current.

The leakage current density as a function of reverse bias can be expressed as [2.13], [2.2]:

$$J_{jun} \cong q\left(\frac{D_n}{H}\right)\frac{n_i^2}{N_A} + q\frac{n_i}{\tau_0}w_d \tag{2-11}$$

where D_n is the electron diffusion constant (in the p-layer), H is the thickness of the neutral p-layer, N_A is the acceptor concentration, and w_d is the depletion width (ref: Figure 2-1). The first part of the equation is the diffusion part, and the second, the thermal generation.

Since the doping concentration of the n^+ region is very high, the diffusion contribution from this region is very small and hence can be neglected.

The depletion width can be expressed as [2.2], [2.14]:

$$w_d = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} + V_d)} \tag{2-12}$$

where ε_{si} is the permittivity of silicon, V_{bi} is the built-in (junction) potential, N_A and N_D are the acceptor and donor concentrations respectively, k is the Boltzmann constant and T is the temperature in Kelvin and where the built-in potential is given by [2.2], [2.7]:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2-13}$$

It can be readily seen from (2-11) and (2-12) that the leakage current due to thermal generation increases as the square root of applied voltage.

The intrinsic carrier concentration, on the other hand, can be expressed as:

$$n_i \propto T^{\frac{3}{2}} e^{\left(-\frac{E_g}{2kT}\right)} \tag{2-14}$$

where E_g is the silicon energy bandgap (1.12 eV).

Thus we see that the leakage current is highly sensitive to temperature in an almost exponential relationship. Moreover, the diffusion and the thermal generation are dependent on two different mechanisms; the former on n_i^2 and the latter on n_i.

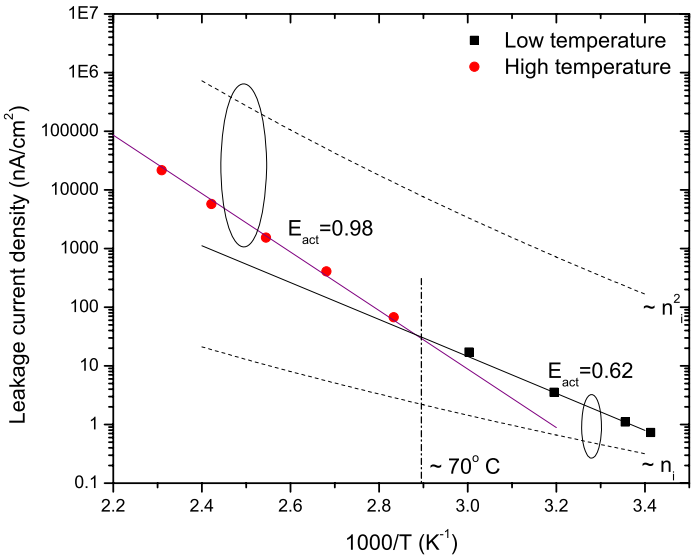


Fig. 2-10 *The Arrhenius plot of the diode in the FGD (keeping the gate in accumulation).*

These two mechanisms can be distinguished by an Arrhenius plot, which is a plot between the inverse of temperature ($1/T$) and the diode leakage current (J_d), in log scale. The Arrhenius equation is of the form [2.15]:

$$R = Ae^{-\left(\frac{E_{act}}{kT}\right)} \tag{2-15}$$

where R is the observed process (leakage current in this case) and E_{act} is the "activation" energy of the process. As explained earlier, the leakage current can have two dependencies; E_g corresponding to n_i^2 at high temperatures and $E_g/2$, corresponding to n_i at low temperatures. However, the careful reader can also notice from (2-14) that this is only an approximation, since n_i has also a $T^{1.5}$ dependence. Recent experiments have shown that a value of 1.7 may

be a better approximation for the exponent. More interesting reading can be done here [2.16].

For the present work, however, the approximation is taken for granted. The Arrhenius plot of the diode in the FGD is shown in Figure 2-10. It can be seen clearly that for low temperatures (below ~ 70^{o} C) the thermal generation mechanism dominates the leakage current. An activation energy of 0.62 eV (~ $E_g/2$) was extracted from the Arrhenius plot for this temperature range. At higher temperatures, the activation energy is seen to be dominated by the diffusion process.

	I_{surf}	I_{jun}^{dp}	I_{diff}
Thermal generation	$\frac{1}{2}E_g$	$\frac{1}{2}E_g$	E_g
Reverse bias	$\neq f(V_d)$	$\sqrt{V_d}$	$\neq f(V_d)$
Geometry	Area	Volume	Volume

Table 2-1. *The dependence of the leakage components on temperature, voltage and geometry.*

An activation energy of 0.98 eV (~ E_g) was extracted from the Arrhenius plot for this temperature range.

The different leakage currents and their dependence on the applied voltage, temperature and geometry are listed in Table 2-1.

2.2.5 Energy-dependent profiling of interface states

Infrared (IR) has an energy that is sub-band gap in the case of silicon. This means that the energy of IR photons is less than sufficient for optical excitation of electrons from the valence band to the conduction band ($E_{ph}<E_g$). Interestingly, devices may show a response to IR radiation due to excitation of electrons from traps in the bandgap to the conduction band; a process which requires lesser energy. Thus this phenomenon can be useful to determine the properties of traps. In this section, the energy-dependent profiling of surface interface traps is studied using this effect.

For the experimentation, a fibre optic cable was coupled to a laser source ($\lambda = 1310\ nm$). Two sets of measurements were carried

out; one in the dark, and one under IR illumination. The interface trap induced leakage current, I_{it} can thus be written as [2.17]:

$$I_{it} = I_{opt(IR)} - I_{dark} = A_g \sum_{\Delta E} J_{it} \tag{2-16}$$

where $I_{opt(IR)}$ is the FGD current due to IR radiation and I_{dark} is the FGD leakage current in the dark.

The surface trap induced leakage current density can then be written as:

$$J_{it} = qn_i s_0 = qn_i \left(\frac{\sigma_s v_{th} N_{it}}{2} \right) \tag{2-17}$$

which leads to:

$$\Delta J_{it} = qn_i \left(\frac{\sigma_s v_{th} \Delta N_{it}}{2} \right) \tag{2-18}$$

The surface potential under the gate (ϕ_s) can be modulated by the gate voltage (V_g). The relationship between gate voltage and surface potential for a MOS system (without any interface or oxide trapped charges) in deep-depletion can be expressed as [2.1], [2.21]:

$$V_g = \frac{qN_A w_g^2}{2\varepsilon_{si}} + \frac{t_{ox}}{\varepsilon_{ox}} (qN_A w_d) + V_{fb} \tag{2-19}$$

$$\text{where, } \phi_s = \frac{qN_A w_g^2}{2\varepsilon_{si}} . \tag{2-20}$$

Here, V_g is the gate voltage, q is the fundamental electronic charge, w_g is the depletion width under the gate, ε_{si} and ε_{ox} are the permittivity of silicon and silicon-dioxide respectively and V_{fb} is the flatband voltage. Using this information, the energy dependent interface state density D_{it} can be obtained as:

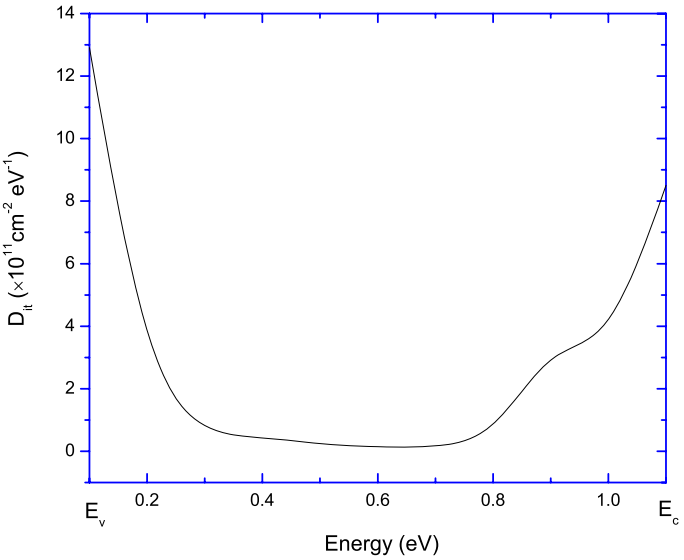


Fig. 2-11 *The extracted interface trap density as a function of its energy with* σ_s *assumed to be* 10^{-16} cm^{-2}.

$$D_{it} = \frac{1}{q}\frac{\partial \Delta N_{it}}{\partial V_g}\frac{\partial V_g}{\partial \phi_s} = \frac{2}{A_g q^2 n_i \sigma_s v_{th}}\left(\frac{\partial \Delta I_{it}}{\partial V_g}\frac{\partial V_g}{\partial \phi_s}\right) \qquad (2\text{-}21)$$

where ϕ_s is the surface potential underneath the gate, σ_s is the capture cross section area of surface interface traps (cm^2), and D_{it} is the interface trap density (cm^{-2} eV^{-1}).

The value of σ_s is in the order of roughly the size of an atom. Many studies using charge pumping methods have indicated the surface traps to be around 10^{-16} cm^{-2}. More details on this can be found in these references: [2.18], [2.19], [2.20]. The extracted D_{it} with the assumption of σ_s of 10^{-16} is shown in Figure 2-11. Note that the shape of D_{it} has a minimum near the mid-gap and sharply increases towards either band edge. This is typical for interface trap in the Si-SiO_2 system [2.22]. The interface trap density is continuous throughout the Si forbidden energy gap, with a "U" shape with

monotonically increasing energies towards the band edges [2.7]. The levels in the middle are the most important for the operation of the device and is heavily influenced by the processing [2.23]. The value at the mid bandgap is around 0.5×10^{11} cm^{-2} $eV^{-1}$from the figure. The values of σ_s and D_{it} also make perfect sense when substituted in (2-8), which yields a s_0 value of 4 cm/s at T=300 K, which is in the range of the expected value.

Parameter	Relationship/ Reference	Value
ϕ_{ms} (Metal semiconductor work function)	[2.7]	-1.08 V
v_{th} (Thermal Velocity)	[2.2]	10^7 cm/s
t_{ox} (Gate-oxide thickness)	Process manual	~ 4 nm
C_{ox} (Gate-oxide capacitance)	$\frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$	8.3×10^{-7} F/cm^2
V_{fb} (Flatband voltage)	FGD Measurement data	-410 mV
V_{th} (Threshold voltage)	FGD Measurement data	350 mV
J_{jun} (V_d = 0.5 V, T = 298 K)	FGD Measurement data	~ 1 nA/cm^2
N_A (Acceptor concentration epi-layer)	Process manual	~ 1×10^{15} cm^{-3}
ϕ_B (Bulk potential)	$\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$	0.288 V
w_g (max) (Maximum depletion width under the gate, ($V_d = 0$)	$\sqrt{\frac{4\varepsilon_{si}\phi_B}{qN_A}}$	0.24 µm

Table 2-2. *Values for different semiconductor parameters obtained from manuals and through the FGD.*

Parameter	Relationship/ Reference	Value
Q_{sd} (max) (Maximum space charge density in the depletion region, $V_d = 0$)	$(-q)N_A w_g$ (max)	-3.8×10^{-9} C cm^{-2}
s_0 (Surface recombination velocity)	$\frac{I_{surf}}{qn_i A_{gate}}$	2.78 cm s^{-1}
τ_0 (Generation lifetime)	$\frac{qn_i A_{gate} w_g}{I_{fij}}$	3.47 μs
σ_s (Capture cross section area in the surface interface)	[2.18]	1×10^{-16}cm^{-2}
D_{it} (Interface trap density) at mid bandgap	Sub-band photonic gated-diode method	~ 0.5×10^{11} eV^{-1}cm^{-2}

Table 2-2. *Values for different semiconductor parameters obtained from manuals and through the FGD.*

Very careful processing have resulted in D_{it} as low as 10^{10} cm^{-2} eV^{-1} [2.22]. Depending on the oxidation conditions and the substrate crystal orientation, these states can be either donor-like (positively charged when empty) or acceptor-like (neutral when empty). Therefore these traps give rise to surface charges called as interface-trapped charges (Q_{it}).

When the silicon surface layer is converted to SiO_2 by the oxidation process, a thin interfacial layer (~ 50 A^o) of oxide of the form SiO_x ($0 < x < 2$) is formed [2.23]. This results in a sheet of immobile positive charge which is bias independent. More problematic are the mobile ions due to alkali metal ions that create reliability problems in MOS structures. When the device is subject to radiation, extra charges may be trapped in the oxide called as oxide trapped charges (Q'_{ss}). These issues will be dealt with in more detail in Chapter 4.

2.3 Summary

In this chapter, fundamental semiconductor physics has been introduced. A very simple yet effective device for semiconductor parameter extraction, the gated-diode (GD), has been introduced and its operation presented. The gated-diodes have been fabricated in finger-like structures—the finger gated-diode (FGD), to preserve the GD geometries. Several device physics parameters were extracted using the FGD. Of these, the generation life time (τ_0) and the surface recombination velocity (s_0) have been given prominence. They establish the basic leakage currents in CMOS devices. The degradation of these parameters due to γ-irradiation will be presented in Chapter 4.

The concept of Arrhenius plot has also been introduced. The two major temperature-dependent leakage mechanisms—the thermal generation as well as the diffusion have been studied using the diode present in the FGD (keeping the gate in accumulation). The Arrhenius plot allows us to extract the activation energy of these mechanisms; viz $E_g/2$ for thermal generation and E_g, for diffusion.

The FGD also hides some tricks up its sleeves. By using an infrared source, the interface trap density was extracted through the sub-band gap induced leakage current. A "U" shaped distribution was obtained using the photonic sub-band gap technique. Assuming an equal capture cross-section areas for holes and electrons ($\sigma_n = \sigma_p = 10^{-16}$ cm^{-2}), the value of D_{it} at the mid-gap obtained through the sub-band photonic method is around 0.5×10^{11} ev^{-1} cm^{-1}.

This chapter also introduces several variables and key concepts which are imperative in understanding ensuing chapters.

2.4 References

[2.1] A. J. P. Theuwissen, "Solid-State Imaging with Charge-Coupled Devices", Kluwer Academic Publishers, pp. 1, 27-35, 18-23, 1995.

[2.2] J. P. Colinge, and C. A. Colinge, “Physics of Semiconductor Devices”, pp. 98-105, 82-89, Springer, 2002.

[2.3] A.S. Grove, and D.J. Fitzgerald, “Surface Effects on p-n Junctions: Characteristics of Surface Space-Charge Regions under Non-equilibrium Conditions”, Solid. St. Elec., Vol. 9, pp. 783-806, 1966.

[2.4] G. Vanstraelen et al., “Generation Lifetime Monitoring on High Resistive Silicon Using Gated Diodes”, Nucl. Inst. Meth. Phys. Res., Vol. 288, No. 1, pp. 48-53, 1990.

[2.5] K. S. Rabbani and D. R. Lamb, “Direct Correlation of Generation Lifetimes from Pulsed MOS Capacitance and Gated-diode Measurements”, Sol. St. Elec., Vol. 26, No. 2, pp. 161-168, 1983.

[2.6] T. Rudenko, V. Kilchytska, V. Dessard, and D. Flandre, “A Revised Reverse Gated-diode Technique for Determining Generation Parameters in Thin-film Silicon-on-insulator Devices and its Application at High Temperatures”, J. App. Phy., Vol. 97, No. 9, pp. 093718.1-093718.9, 2005.

[2.7] D. K. Shroder, “Semiconductor Material and Device Characterization”, Wiley-Interscience Publication, pp. 61, 271, 1990.

[2.8] G. Verzellesi et al., “Extraction of Bulk Generation Lifetime and Surface Generation Velocity in High-resistivity Silicon by means of Gated-diodes”, Nucl. Instr. Meth. Phy. Res., Vol. 477, No. 1-3, pp. 220-225, 2002.

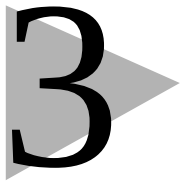
[2.9] G. Verzellesi et al., “On the Accuracy of Generation Lifetime Measurement in High-resistivity Silicon using PN gated-diodes”, IEEE Trans. Elec. Dev., Vol. 46, No. 4, pp. 817-820, 1999.

[2.10] T. P. Chen, D. S. H. Chan, and W. K. Chim, “Determination of Substrate Doping, Substrate Carrier Lifetime and Density of Surface Recombination Centers of MOSFETs by Gate-controlled-diode Measurements”, Semicond. Sci. Technol., Vol. 11, No. 5, pp. 672-678, 1996.

[2.11] P. C. T. Roberts, and J. D. E. Beynon, “An Experimental Determination of the Carrier Lifetime near the Si-SiO_2 Interface”, Solid. St. Elec., Vol. 16, No. 2, pp. 221-227, 1973.

[2.12] J. V. D. Spiegel, and G. J. Declerck, “Theoretical and Practical Investigation of the Thermal Generation in Gate-controlled Diodes”, Solid. St. Elec., Vol. 24, No. 9, pp. 869-877, 1981.
[2.13] N. V. Loukianova et al., “Leakage Current Modeling of Test Structures for Characterization of Dark Current in CMOS Image Sensors”, IEEE Trans. Elec. Dev., Vol. 50, No. 1, pp. 77-83, 2003.
[2.14] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-submicrometer CMOS Circuits”, IEEE Proc., Vol. 91, No. 2, pp. 305-327, 2003.
[2.15] A. Czerwinski, E. Simoen, A. Poyai, and C. Claeys, “Activation Energy Analysis as a Tool for Extraction and Investigation of p–n Junction Leakage Current Components”, J. Appl. Phys., Vol. 94, No. 2, pp. 1218-1221, 2003.
[2.16] A. Poyai, E. Simoen, and C. Clayes, “Improved Extraction of the Activation Energy of the Leakage Current in Silicon p-n Junction Diodes”, App. Phys. Lett., Vol. 78, No. 14, pp. 1997-1999, 2001.
[2.17] S. S. Chi et al., “Photonic Gated-diode Method for Extracting the Energy-dependent and the Spatial Distributions of Interface States in MOSFETs”, Journ. Kor. Phys. Soc., Vol. 43, No. 5, pp. 879-886, 2003.
[2.18] N. S. Saks, “Measurement of a Single Interface Trap Capture Cross Sections with Charge Pumping”, Appl. Phys. Lett., Vol. 50, No. 25, pp. 3380-3382, 1997.
[2.19] S. M. Sze, and K. K. Ng, “Physics of Semiconductor Devices”, Wiley-Interscience, pp. 221, 2006.
[2.20] S. O. Kasap, and P. Capper, “Springer Handbook of Electronic and Photonic Materials”, Springer, pp. 436, 2006.
[2.21] D. F. Barbe, “Imaging Devices Using the Charge-Coupled Concept”, IEEE Proc., Vol. 63, No. 1, pp. 38-67, 1975.
[2.22] N. Dasgupta, and A. Dasgupta, “Semiconductor Devices: Modelling and Technology”, PHI Learning Pvt. Ltd, pp. 248, 2004.
[2.23] T. P. Ma, and P. V. Dressendorfer, “Ionizing Radiation Effects in MOS Devices and Circuits”, Wiley-IEEE, 1989.

Electrical and optical aspects of 4-T image sensors



Before CMOS image sensors (CIS) and CCDs, there were MOS sensors. The 1960s was an experimental era where many research groups toyed with PMOS, NMOS and bipolar devices [3.1]. Some sensors that were developed during this era were: the computational sensor, which determines the position of a light spot (1963), the scanistor based on n-p-n junctions (1964), p-n junction in photon-flux integration mode later called as the reticon (1968), as well as CdS/ CdSe TFTs (1967), etc [3.2], [3.3]. These developments were followed by the introduction of buried channel photodiodes for extremely small dark currents (1968), source follower for in-pixel buffering, and the technology for FPN (Fixed Pattern Noise) reduction. CCDs were the focus of attention for the next few decades, after being introduced in 1970. In the 1990s however, there was a renewed interested in CMOS image sensors; the main motivation being the possibility of utilizing “standard” CMOS technology, where cost rather than quality was the driving force. Very soon, with several independent research groups actively perusing the CMOS technology, CIS became a major challenge to CCDs. The main attraction of CIS was its low power consumption (few tens of mW), sensors tailored

for custom applications, as well as harnessing the vertical integration and the exponential growth of CMOS technology [3.4].

Section 3.1 discusses the basics of CIS, especially the choice of the day: the 4-T CIS (4-Transistor CMOS Image Sensor); Section 3.2 on the spectral characteristics of the image sensor and Section 3.3, on the dark current aspects. Section 3.4 reviews the major aspects covered in this chapter.

3.1 4-T CIS: Basics

A pixel with an active amplifier inside it is called as an active pixel sensor (APS). Earlier in its progress, device mismatch of this amplifier was a major source for FPN [3.3]. Techniques like CDS (Correlated Double Sampling) have been used to reduce FPN significantly.

A 4-T pixel has four transistors inside the pixel and is schematically illustrated in Figure 3-1. A part of the device simulated in a process simulator is shown in Figure 3-2. Darker colours indicate a higher doping concentration. 4-T sensors employ what is called as a “pinned” photodiode structure [3.5]. This is achieved by the formation of a heavily doped p^+ layer on top of a n-p type photodiode. This isolates the depleted regions of the photodiode from interacting with the surface and hence reduces surface leakage currents. The doping levels are chosen such that the photodiode is completely depleted (fully-depleted photodiode). In essence, the diode is pinned at a fixed voltage called as the “pinning” voltage [3.6]. This has an added advantage in that the structure suffers much less from the problem of “reset” noise and image lag. Reset noise occurs when the photodiode is reset to a different level each time the reset operation of a photodiode is carried out. Since the diode is fully depleted, uncertainty in reset levels from this region can be eliminated. CDS is usually employed at a later stage to reduce the reset noise that originates from the FD node.

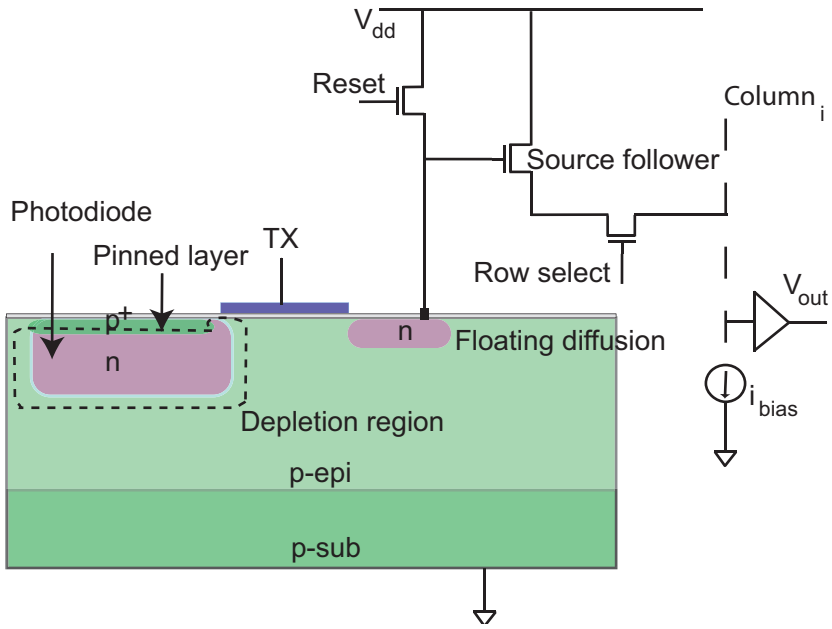


Fig. 3-1 *Schematic of a 4-T CMOS image sensor.*

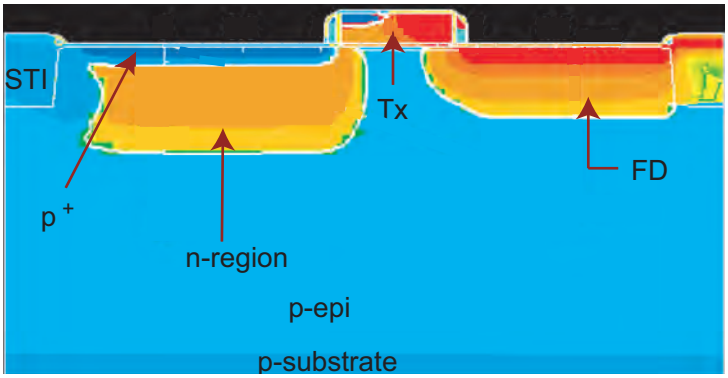


Fig. 3-2 *A part of the 4-T CMOS sensor simulated in a process simulator. Darker colours indicate higher doping concentrations.*

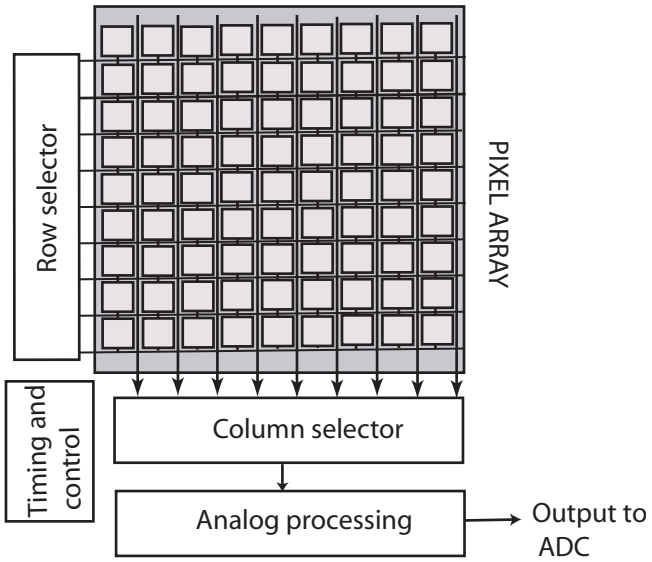


Fig. 3-3 *The basic sections of a complete CMOS image sensor.*

The heavily doped p^+ layer contributes to the sensitivity of the photodiode to the blue/green regions of the visible spectrum as will be explained in Section 3.2.1. But since the reset potential is fixed, these sensors suffer from low well capacity.

The integration of charges takes place in the pinned photodiode, and the charges are moved towards the floating diffusion node (FD) by switching "ON" the transfer gate (TX). The FD node is usually reset just before the actual transfer operation to minimize dark current. This reset value is read-out via a source follower (SF) and stored in a capacitor in the column bus. The reset potential "falls" after the charges from the photodiode are transferred due to the discharge of the FD node capacitance [3.5].

Figure 3-3 shows the sensor schematic. The main sections of the sensor include a column and a row selector, a timing and control circuit, an analog processing block as well as ADCs (Analog to Digital Converters). In a typical rolling shutter mode, each row is selected sequentially, and read-out through the column. The column contains important analog blocks like the CDS circuitry (Figure 3-4).

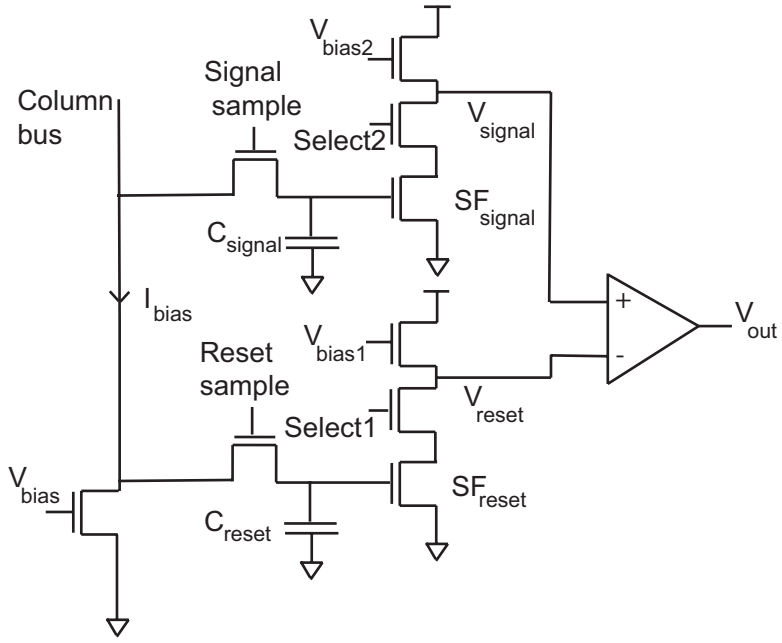


Fig. 3-4 *A correlated double sampling (CDS) circuit.*

CDS operation is basically used to cancel pixel offsets and reset noise (especially from the FD node). The operation includes storing the reset value (by enabling “Reset sample”) and the signal value (by enabling “Signal sample”) on capacitors C_{reset} and C_{signal} which are in the column bus. These two values are sampled within a very short interval, for efficient noise reduction. The sampled values are buffered through the source followers “SF_{reset}”, “SF_{signal}” and enabled for read-out by the “Select” switches. The sampled value are either subtracted in a differential amplifier or fed as differential inputs to an ADC. The operation helps in effectively cancelling the pixel reset noise, pixel FPN as well as flicker noise [3.7].

Due to the rapid development in the field of CMOS image sensors, there have been different flavours of the sensor aimed at specific applications. For instance, ADCs have been included in each

column and even inside each pixel [3.8]. Improvements have also been made on the power consumption of the sensors by tuning the performance of ADCs as well as the analog blocks. Efforts have also been undertaken to perform more operations inside the pixel, so that post-processing can be reduced for higher speed of operation of the sensor.

With the reducing pixel dimensions, modern CMOS sensors have very small FD geometries and hence a very high conversion gain ($\mu V/e^-$). This is especially true for the 4-T image sensor, where a separate FD node is used for charge conversion rather than the large area photodiode used in other APS like the 3-T.

3.2 Spectral characteristics of the 4-T pixel sensor

The quantum efficiency of any photodetector is the fraction of photon flux (F_0) that contributes to photocurrent as a function of wavelength λ.The quantum efficiency (QE) establishes a very accurate relationship between the number of photo-charges generated by a photon incident on the photodetector [3.9]. Quantum efficiency can be divided into two parts:

- *The internal quantum efficiency*: Refers to the number of photo-electrons generated inside the semiconductor material per incident photon.

- *The external quantum efficiency*: Refers to the number of photo-electrons generated per incident photon taking into account the transmission loss at the surface (including reflection and absorption). A detailed knowledge of the optical stack that forms on top of the silicon substrate is necessary to establish the external QE.

In the following section, an analytic model of a pinned photodiode is developed to predict the internal QE of the sensor.

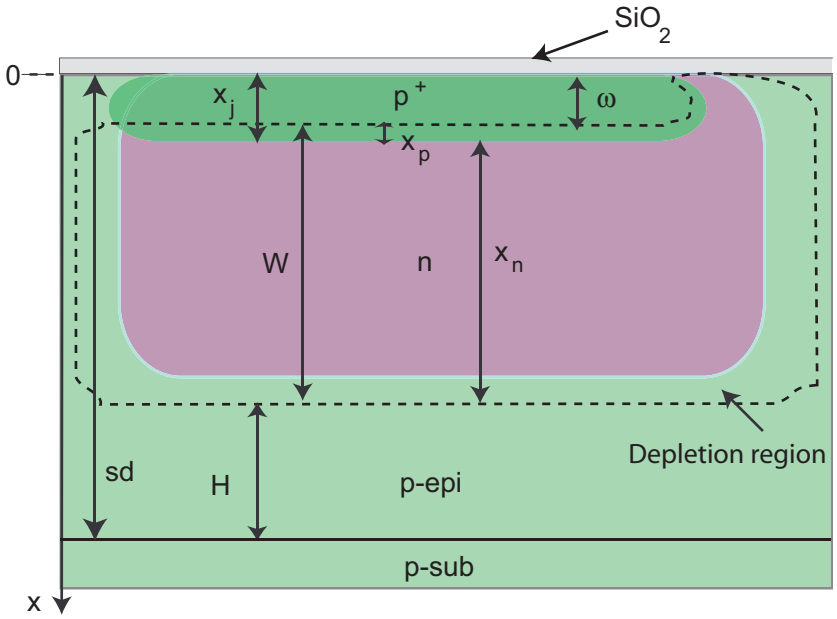


Fig. 3-5 *The p^+/n/p-epi/p-sub structure formed in the 4-T pixel and the various geometrical parameters used.*

A representative case of the influence of the optical stack on the QE will be introduced following this.

3.2.1 Internal QE

An analytic model for the internal QE of a pinned photodiode shown in Figure 3-5 is derived by solving the continuity equation of a usual p^+/n photodiode, by using an equivalent diode reverse voltage V_{dp}, which represents the depleted diode. The contribution from the p-type epitaxial region as well as the p-type substrate is included for the contribution from carriers collected through diffusion. Since the penetration of the depletion region into the highly doped pinning region is negligible, this solution is a very good approximation to the spectral response of the pinned photodiode. The p^+ region is considered to have a Gaussian profile for the solution.

The diffusion length, L_A, of the p^+ layer may be considered to be small compared to the minority carrier (electron) diffusion length which is given by:

$$L_n = \sqrt{D_n \tau_n} \tag{3-1}$$

where D_n is the electron diffusion constant, and τ_n is the minority carrier lifetime in the p^+ region. This results in a simplified continuity equation [3.10]:

$$\frac{\partial^2 \Delta n}{\partial r^2} - r\frac{\partial \Delta n}{\partial r} - \Delta n = -\frac{F_0 \alpha}{D_n} 2L_A{}^2 e^{-\sqrt{2}\alpha L_A} \tag{3-2}$$

where Δn is the excess electrons in the p^+ region, F_0 is the photon flux incident on the front surface of the photodiode where reflection is assumed to be zero, α is the absorption coefficient of silicon, and r is given by:

$$r = \frac{x_p}{\sqrt{2}L_A} \tag{3-3}$$

where x_p is the penetration of the depletion region into the p^+ region. This penetration depth can be determined by the doping concentration as well as the total depletion width W which is given by:

$$W = \sqrt{\frac{2\varepsilon_{si}}{q}(v_{dp} + \phi_n + \phi_p) \times \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{3-4}$$

where ε_{si} is the silicon permittivity, V_{dp} is the reverse bias voltage, ϕ_n, ϕ_p are the bulk potentials of the n and p^+ regions and N_A and N_D are the acceptor and donor concentrations.

The depth of penetration into the p^+ region is then given by:

$$x_p = \frac{W}{1 + \frac{1}{k}} \tag{3-5}$$

where $k = \frac{N_A}{N_D}$. The depth of penetration into the n region is given by:

$$x_n = x_p \times \frac{1}{k} \tag{3-6}$$

The minority carriers lost in the front surface interface ($x = 0$) is governed by the relationship:

$$s\Delta n\big|_{x=0} = D_n \frac{\partial \Delta n}{\partial n}\bigg|_{x=0} + \mu_n E \Delta n\big|_{x=0} \tag{3-7}$$

where s is the surface recombination velocity (SRV) at the front surface. The concentration of excess carriers at the boundary of the depletion region ($x = \omega$) with a reverse bias V_{dp}, can be determined by the diode equation:

$$\Delta n\big|_{x=\omega} = \frac{n_i^2}{N_A}\left(e^{\frac{qV_{dp}}{kT}} - 1 \right) \tag{3-8}$$

where n_i is the intrinsic carrier concentration, and N_A is the acceptor concentration. An analytic solution based on a power series can be a used to solve (3-2) applying the boundary conditions (3-7, 3-8) to yield the photo-current density from the p^+ region (J_{p+}) [3.10].

The photo-generation at the depletion or the space charge region (SCR) is given by:

$$J_{sc} = qF_0(e^{-\alpha(x_j - x_p)} - e^{-\alpha(x_j + x_n)}) \tag{3-9}$$

Recombination in the space charge region is not considered. The contribution from the epitaxial region can be given as [3.13]:

$$J_{epi} = \frac{qF_0\alpha L'_n}{(\alpha^2 L'^2_n - 1)} e^{-(x_j + x_n)} \times \left(\alpha L'_n - \frac{\cosh\left(\frac{H}{L'_n}\right) - e^{-\alpha H}}{\sinh\left(\frac{H}{L'_n}\right)} \right) \quad (3\text{-}10)$$

Here x_j is the metallurgical junction depth of the p^+-n diode, x_n is the depletion width into the n-region and H is the thickness of the neutral p-region. L'_n is the electron diffusion length in the p-epi region.

Finally, the contribution from the substrate can be given as [3.15]:

$$J_{sub} = qF_0\alpha \left(e^{-\frac{H}{L_{op}}} \right) \times L_{op} \times L_s \times \left(\frac{L_{sn} - L_{op}}{L_{sn}^2 - L_{op}^2} \right) \quad (3\text{-}11)$$

where H is the width of the neutral p-epi region, L_{op} is given by $\frac{1}{\alpha}$, and L_{sn} is the electron diffusion length in the substrate region.

The total current density (J_{tot}) is the sum of the contribution from the heavily doped p^+ region, the SCR, the neutral epi-region as well as the substrate. The quantum efficiency can be calculated by the ratio of the total current to the total photon input which is:

$$QE = \frac{J_{tot}}{qF_0} \quad (3\text{-}12)$$

A internal QE (%) simulation of the various photocurrent components obtained by the derived model and utilizing the parameters listed in Table 3-1 is shown in Figure 3-6.

The p^+ region is seen to be contributing in the window from 350-500 nm, with a peak around 400 nm. Thus, the p^+ region can be considered to be a high-pass filter. Some reserach has also proved that the pinned-photodiodes have better blue response than other detector types [3.16]. Thus, this layer should be tailored for optimal performance of the sensor towards the blue spectrum.

Parameter	Value	Remarks
F_0	4×10^{12} (~ 10 Lux at $\lambda = 555$ nm)	Photon flux (photons/cm^{2}s)
D_n	2 [3.11]	Electron diffusion constant in p^+ (cm^2/s)
D'_n	34.8 [3.11]	Electron diffusion constant in epi- layer (cm^2/s)
L_A	0.119×10^{-4} Process simulation	Impurity diffusion length of p^+ (cm)
sd	3.5×10^{-4} [3.15]	Epi-region depth (cm)
T	300	Temperature (K)
Doping (epi)	1×10^{15} [3.14]	cm^{-3}
Doping (p+)	1×10^{20} [3.17]	cm^{-3}
V_{dp}	$1\rightarrow2$ [3.6]	Equivalent depletion voltage (V)
J_d	0.25×10^{-4} [3.19]	p^+ junction depth (cm)
s	$1\times10^5\rightarrow1\times10^6$ [3.18]	Surface recombination velocity (cm/s)
τ_n	1×10^{-9} [3.12]	Lifetime (electron) in p^+ (s)

Table 3-1. *Device parameters used in the simulation.*

Parameter	Value	Remarks
τ'_n	100×10^{-6} [3.12]	Lifetime (electron) p-epi (s)
L_{sn}	4×10^{-4} [3.15]	Diffusion length (electrons) in substrate (cm)

Table 3-1. *Device parameters used in the simulation.*

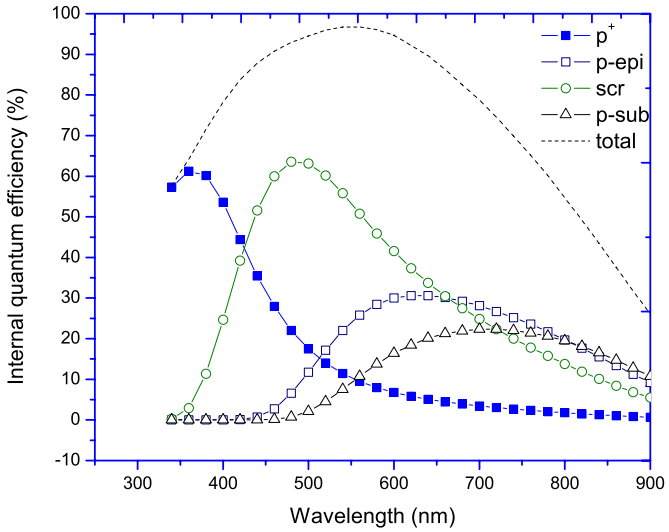


Fig. 3-6 *The contribution of the individual spectral components to the total quantum efficiency.*

The depleted region (space charge region) is seen to respond to a wide bandwidth from ~ 400-700 nm, with a peak at around 500 nm. This peak represents the green region of the visible spectrum. Thus, the SCR plays a major role in detecting the green and also some of the red regions of the spectrum. The SCR can be conveniently thought of as band pass filter, reacting to the green and red portion of the visible spectrum.

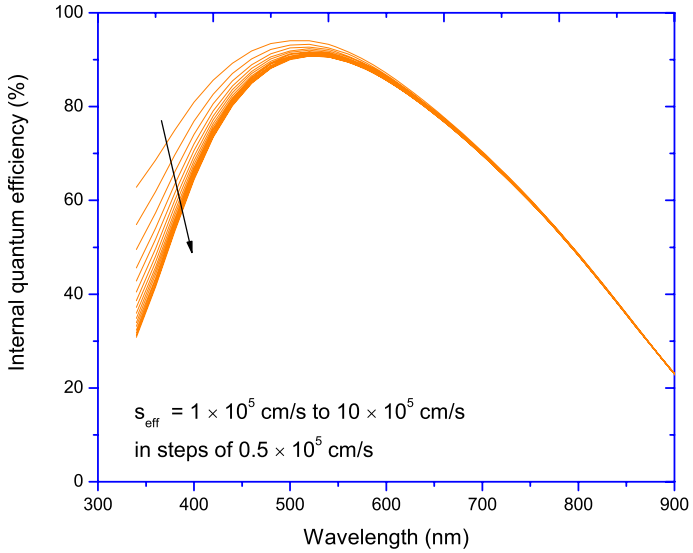


Fig. 3-7 *Effect of surface recombination velocity (s) on the internal QE.*

The epi-region (3-4 μm) is seen to contribute towards the higher wavelengths (~ 550-900 nm) of the visible spectrum. Thus it forms a low-pass filter with much less peak efficiency than the SCR region, owing to its limited thickness.

The red-photons require much deeper penetration depths for it to be collected effectively. Thus the thickness of the epi-region/substrate plays an important role in deciding the sensors performance at this part of the spectrum. Modern CMOS technologies are built over thin epi-layers, to minimize noise coupling. This can be a major disadvantage in imaging applications, since the efficiency towards the red/deep-red regions is reduced. But on the other hand, pixel cross talk is reduced due to the thin epi-layer.

The epi-layer/substrate junction can be thought of as a carrier sink. Most of the charge carriers at this junction or near to it in the substrate are forced towards the epi-region. But since the substrate is heavily doped, carrier mobility in the substrate region is rather limited. As can be seen from the simulation, the contribution from the substrate is the smallest. The very little contribution it offers is in the

red portion of the visible spectrum. On the other hand, it is an advantage in disguise since cross-talk between pixels due to charges generated deep in the silicon bulk can be minimized.

The surface recombination velocity (SRV) included in the model is varied from 10^5 cm/s to 10^6 cm/s in the simulation (Figure 3-7). It can be seen that the SRV affects the response of the sensor to shorter wavelengths [3.20].

The SRV depends on the quality of the interface. The larger the number of interface traps, the higher the value of SRV. Since high energy photons like blue up to green are absorbed very close to the interface, they are affected more than the other photons. The curves are seen to saturate at ~ 5×10^5 cm/s.

The depletion width varies as the square root of the applied (pinning) voltage. Figure 3-8 shows the variation of the spectral response as a function of the reverse voltage (V_{dp}), where V_{dp} is varied from 1 to 2 V. A very small change is noticed in the mid-section of the spectral response (the green photons).

The thickness of the epi-regions effects the larger wavelengths as was explained before. This is because they have lesser energy, and require larger depth for effective collection. Figure 3-9 shows the simulation in which the epi-layer depth is varied from 10 μm to 200 μm. As expected, the efficiency increases dramatically with the epi-layer thickness. The curves saturate for epi-thickness > 80 μm.

As explained before, limiting the collection of carriers generated deep in the semiconductor bulk also limits cross-talk at the price of a lower QE.

The model derived in this section is used to fit the experimental QE curves to be discussed in Chapter 4. The change in the fit parameters is used to analyse radiation induced damage mechanism in the 4-T CMOS image sensor.

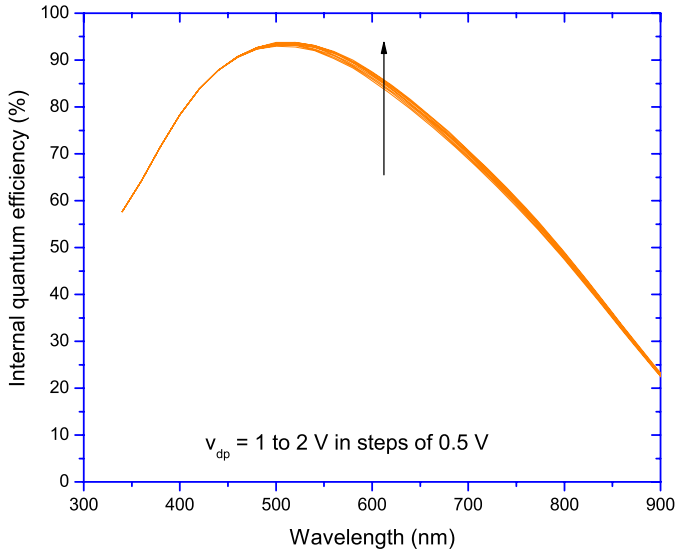


Fig. 3-8 *The effect of reverse bias voltage on the internal QE.*

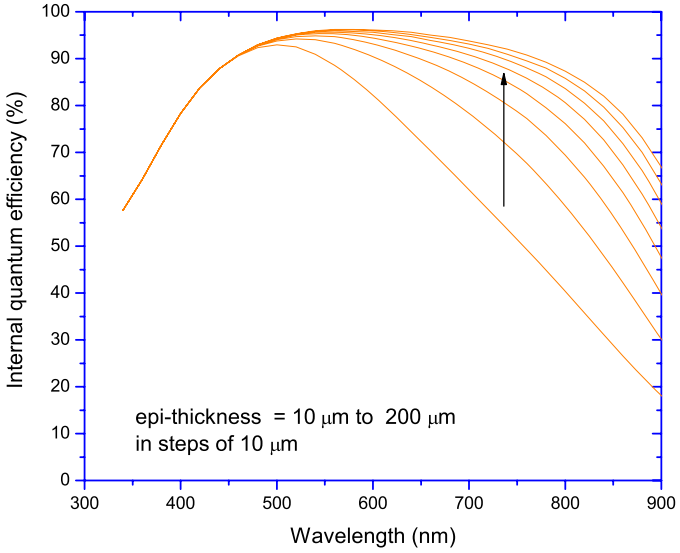


Fig. 3-9 *The effect of epi-thickness on the internal QE.*

3.2.2 External QE

Modern CMOS processes involve multiple inter-dielectric layers on top of the silicon, mainly for isolating individual metal layers. They usually comprise of different kinds of oxides and organic materials. A final passivation of the entire chip is also carried out usually by silicon nitride (Si_3N_4). These layers have different optical constants (refractive indices, absorption coefficients etc). The light that passes through this stack of materials undergo multiple reflections and thus exhibit interference effects. Due to the reflection and absorption, the transmission through the stack will not be 100%. This loss determines the external quantum efficiency of the photodetector. For the very simple case of an air/oxide/silicon structure, the wavelength dependent reflection from the top surface of the stack is given by the equation [3.15], [3.20]:

$$R(\lambda) = \frac{n_{SiO_2}^2 (n_{air} - n_{si})^2 \cos^2\left(\frac{2\pi p}{\lambda}\right) + \left(n_{air} n_{Si} - n_{SiO_2}^2\right) \sin^2\left(\frac{2\pi p}{\lambda}\right)}{n_{SiO_2}^2 (n_{air} + n_{si})^2 \cos^2\left(\frac{2\pi p}{\lambda}\right) + \left(n_{air} n_{Si} + n_{SiO_2}^2\right) \sin^2\left(\frac{2\pi p}{\lambda}\right)} \quad (3\text{-}13)$$

Here, n_{SiO_2} is the refractive index of silicon dioxide; n_{air} that of air; and n_{Si} that of silicon. p is the optical path difference given by:

$$p = n_{SiO_2} t_{ox} \cos(\theta) \quad (3\text{-}14)$$

where t_{ox} is the oxide thickness and θ is the angle of incidence. When the optical path difference is an odd multiple of $\lambda/4$, the value of $R(\lambda)$ is minimized leading to the simplified equation [3.15]:

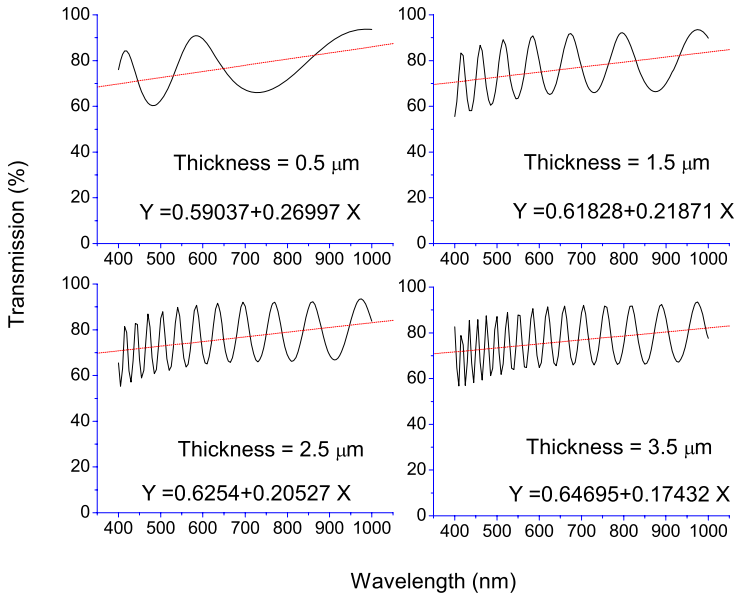


Fig. 3-10 *The transmission (%) vs. wavelength for various silicon dioxide thicknesses. The curve trend is indicated by the linear fit and expressed in the standard form Y=mx+C.*

$$R = \frac{\left(n_{air}n_{Si} - n_{SiO_2}^2\right)^2}{\left(n_{air}n_{Si} + n_{SiO_2}^2\right)^2} \tag{3-15}$$

Modern CMOS processes utilize several oxides or nitride layers of varying thicknesses. Thus it is difficult to emulate a real structure. But it many cases, for example in comparative study, an approximation can be done on the stack, the material and its thickness. Many intuitive insights can also be obtained though the study of simple stacks.

Figure 3-10 shows the transmission curves (%) for a simple air/ oxide/silicon structure. The refractive index of the oxide is chosen to

be a constant; 1.46 throughout the spectrum, and no absorption is considered in the oxide layer. Though this is a simplification, this helps to understand the concept. The spectrum is seen to be cyclically varying with the wavelength. When this transmission (or $1-R$, where R is the reflectance) is multiplied with the internal QE, we get the external QE.

The thickness of the oxide layer is varied from 0.5 μm to 3.5 μm in 1 μm steps in Figure 3-10. It can be seen that the number of peaks increases with the thickness of the oxide layer. The average transmission is also seen to increase slightly with the thickness of the oxide in the spectral range considered. Needless to say, the refractive index, surface properties, absorption in the layers, etc complicate the analysis to the extent that only a simplified, empirical approach would be feasible for a model.

3.2.3 Spectral response: experimental method

To measure the spectral response of the image sensor, a setup consisting of a monochromator, filter and grating set, focusing optics and a camera board interfaced to a PC are used. Figure 3-11 shows the scheme of the setup. A halogen light source (LS) is used to produce a highly intense, polychromatic beam of light. A band-pass filter wheel (F1) is used to select a band of wavelengths falling in the blue, green or red portion of the spectrum. This beam is then directed by a mirror (M1) into a grating (GR-1) that separates it into individual color components. After a final mirror that deflects the wavelength of interest, the beam travels further through a slit. The gratings and mirrors are controlled using a digital interface.

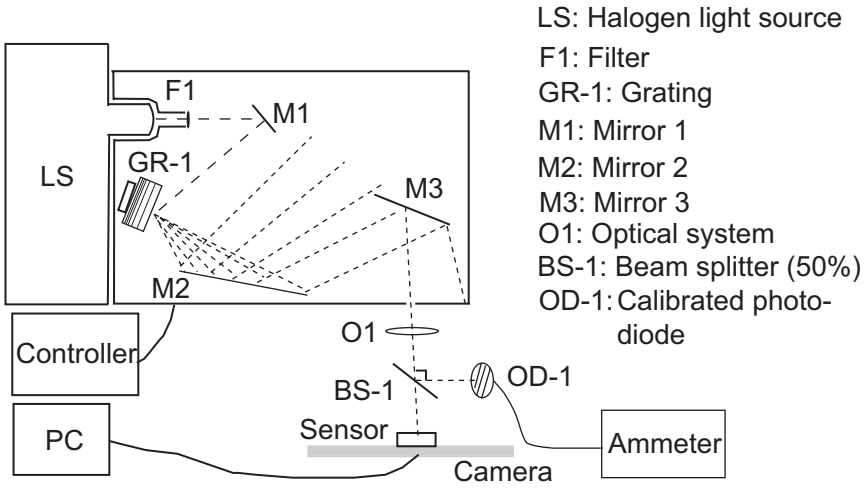


Fig. 3-11 *The setup for the spectral response measurement.*

A 50/50 beam splitter (BS-1) splits the beam into two. One part falls directly on the sensor, and the other one, on a pre-calibrated photodiode (OD-1). The calibrated photodiode is used to determine the power incident on the sensor. For this reason, it is ensured that the path length from the beam splitter to either the calibrated photodiode or the sensor is fixed.

To calculate the number of incident photons from the input power the following expression can be used:

$$\frac{Number\ of\ photons}{s} = \frac{Power}{Energy} = \frac{P}{h\nu} \tag{3-16}$$

where h is the Plancks constant and ν is the frequency of the photon. The number of photons responsible for generating the sensor current is given by:

$$\frac{Number\ of\ photons\ generating\ carriers}{s} = \frac{Sensor\ current}{q} = \frac{I_{sensor}}{q} \tag{3-17}$$

The quantum efficiency is given by:

$$QE = \frac{Number\ of\ photons\ generating\ carriers}{Number\ of\ photons} \tag{3-18}$$

The number of photons incident on the sensor can be estimated using (3-16). At the same time, the output of the sensor is measured utilizing the camera board. The QE can then be determined by (3-18). In reality, the beam splitter may also have a wavelength dependent behaviour, and should be considered during the experimentation. The experimental results and the fit through the model derived in Section 3.2.1 are further discussed in Chapter 4. In that chapter, the model has been used to quantify the effects of radiation on the spectral response of the image sensor.

3.3 Dark current of the 4-T pixel sensor

As with any other semiconductor device, the 4-T pixel sensor too suffers from leakage currents. The basic leakage current mechanisms such as thermal generation as well as diffusion have been treated fairly well in Chapter 2. The 4-T pixel achieves a very low dark current by isolating the photodiode from the surface by using a heavily doped p^+ pinning layer, thus minimizing the surface leakage component. We have seen earlier that the p^+ pinning layer on top of the photodiode also contributes to the spectral response of the sensor in the blue/green regions.

The other major sources of dark current in the pinned 4-T pixel are the STI (Shallow Trench Isolation) region and the transfer-gate region. As the pixel size reduces, the total dark current is influenced by the perimeter leakage than the area. The perimeter leakage in a pixel is due to the generation from the sidewalls of the STI. The Poole-Frenkel effect is an electric field induced lowering of potential barrier for the thermal emission of a carrier from a level in the bandgap. Reduced dimensions contribute to increased electric fields and thus an enhanced dark current via the Poole-Frenkel effect. Each of these issues will be discussed in this section.

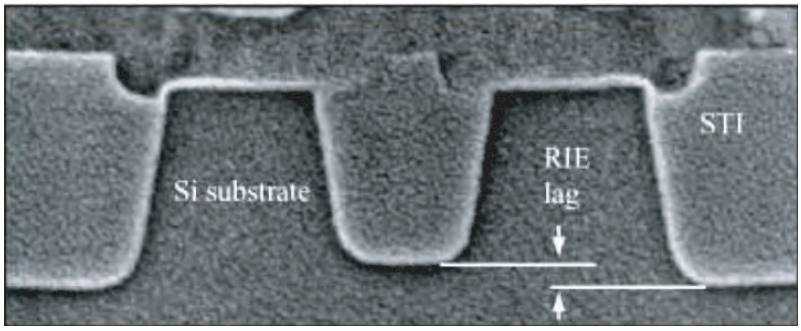


Fig. 3-12 *Cross sectional SEM image of the STIs in 0.18 μm node. The STI/silicon interface is notorious for defects and hence leakage currents [3.26]. Typical STI depths are ~ 0.3-0.5 μm. © 2002 by IBM Corporation.*

3.3.1 STI induced dark current

The isolation regions are usually formed of local oxidation of silicon (LOCOS) or in sub 0.25-μm processes; the STI [3.21]. A cross sectional SEM image of the STI in 0.18-μm process is shown in Figure 3-12. The dislocations at these structures, as well as the stress upon the photodiodes due to the STIs are primarily responsible for dark current observed in these sensors [3.22], [3.23]. They are also prone to degradation in harsh environments [3.27]. The side walls as well as edges of the STI play an important role in the dark current generation. Some research has been carried out to estimate the surface recombination velocity as well as the bulk generation lifetime of STIs [3.24]. The study revealed a high surface recombination velocity of around 2570 cm/s at the STI interface. The study also indicated that etch damage removal process when employed, reduced the surface roughness leading to leakage current improvements. Recent DLTS (Deep-Level Transient Spectroscopy) measurements reveal mid-gap traps of energies $|E_t - E_i| \sim 0.05$ eV and $|E_t - E_i| \sim 0.02$ eV of capture cross sections, 1.02×10^{-13} and 6.06×10^{-16} cm^{-2} respectively [3.23]. The study by the group of H. I. Kwon et al. ([3.23]) contribute the defects to the RIE (Reactive Ion Etching) process for the STI manufacturing process which results in

mechanical stress-induced lattice damage, stacking fault as well as dislocation. They also attribute the quantized dark currents in their studies to the STI.

The leakage current from a diode surrounded by STI can be given as:

$$I_{total}[A] = A_{diode} \times I_{area} + P_{diode} \times I_{perimeter} + I_{stress} \tag{3-19}$$

where A_{diode} is the area, and P_{diode} is the perimeter of the diode. I_{area}, $I_{perimeter}$, I_{stress} are the leakage current components from the area, perimeter and the stress respectively. In fact for very small diodes, another factor will add to the total leakage current: the corner effect (I_c) which is proportional to the number of corners.

The area leakage can be written as the sum of the area diffusion and area thermal generation currents as:

$$I_{area} = I_{diff}^{A} + \frac{qn_i w_d A_{diode}}{\tau_0} \tag{3-20}$$

where I_{diff}^{A} is the area diffusion component, w_d is the width of the depletion region, A_{diode} is the area and τ_0 is the generation lifetime. The second term of (3-20) represents the area thermal generation component.

The perimeter current component, on the other hand, is composed of a perimeter diffusion current and perimeter generation current similar to the area leakage. In addition, it also contains the surface recombination current characterized by the surface recombination velocity at the Si-SiO_2 interface.

The surface leakage current can be written as:

$$I_{surf} = qn_i A_s \left(\frac{\pi}{2}\right) \sigma_s v_{th} (kTD_{it}) \tag{3-21}$$

where A_s is the depleted surface area, D_{it} is the interface state density, and σ_s is the capture cross section area of the traps.

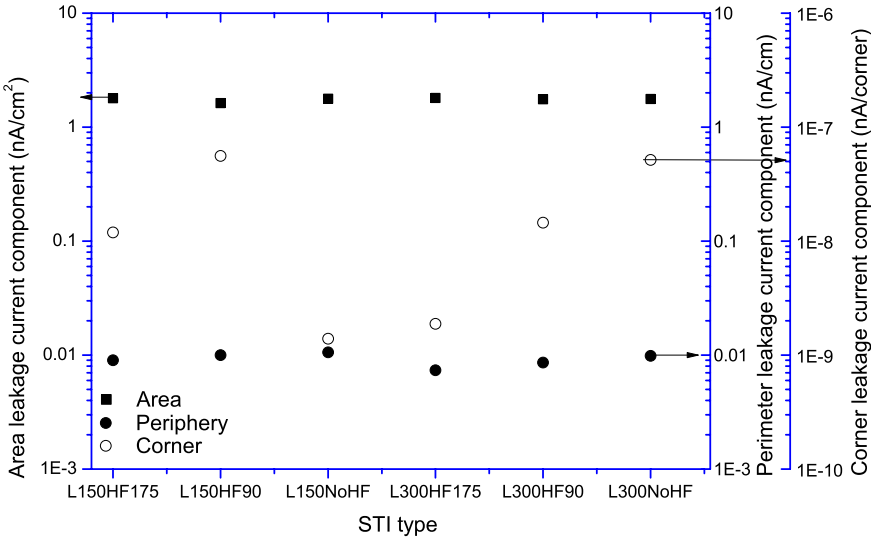


Fig. 3-13 *Area, periphery and corner leakage components extracted using various STI test structures using data from [3.30]. The depth of STI was 3000 A^o.*

Two methods to improve STI quality are by reducing sidewall damages and corner rounding. The former is achieved by a thermal 'liner' oxidation and the latter by "undercutting" of pad oxide [3.25].

Figure 3-13 shows the extracted leakage components introduced by the STI using diode test structures consisting of various geometries (area, periphery or corner intensive) [3.30]. The STI includes: liner oxidations (*L*) of 150 A^o and 200 A^o, and liner undercuts (*H*) of 90 A^o, 175 A^o, as well as no undercuts. The labels used in the X axis in Figure 3-13 for different STI schemes are of the form: "L liner value H undercut value". Undercut etches the pad oxide under the nitride mask along the corner sidewall and induces the corner shape to change [3.31].

As typical STI structures are perimeter intensive devices, the perimeter leakage component will be many times the area component. As can be seen from Figure 3-13, the corner leakage components are indeed very small and negligible.

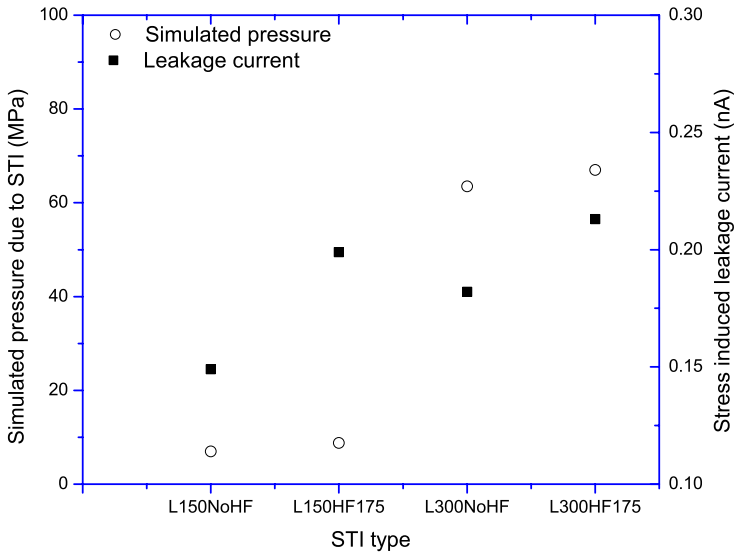


Fig. 3-14 *Simulated STI stress and resulting leakage for different STI types obtained from [3.30].*

Stress due to the STIs also contributes to leakage current. Compressive stress can cause silicon bandgap to narrow. STI as well as LOCOS peripheries exhibit high stress. The intrinsic carrier concentration, n_i is given as:

$$n_i \propto e^{-\frac{E_g}{2kT}} \tag{3-22}$$

where E_g is the bandgap of silicon. Thus, even a small change in the value of E_g can increase the intrinsic carrier concentration dramatically. This leads to increased thermal generation from depletion regions near the areas of the stress.
The anisotropic compressive stress in the diode, due to STI as well as silicides in modern CMOS technologies can reach several MPa [3.28].

Fig. 3-14 shows the results of a Tsuprem4^{TM} stress simulation on some STI types [3.30]. It can be seen that the stress increases for higher liner values as well as undercuts.

One of the "practical" methods prevalent to reduce the dark current from the STIs include the formation of a p-type passivation around the STI as well as tailoring the distance between the STI and the photodiode. The excess holes in the p-well reduce the probability of electrons from reaching the diode region, thus reducing the STI induced leakage current. In Chapter 4, the effect of such passivations on radiation tolerance of 4-T CMOS image sensors will be discussed in detail.

3.3.2 Enhanced generation due to electric fields

Processes like trap-assisted tunneling and field-enhanced emissions have been though to increase the dark current in image sensors. The emission rate from a defect that is located in a high local electric field is believed to increase dramatically [3.29]. The presence of strong electric fields in semiconductors results in higher emission rates from defects via processes like *Poole-Frenkel* effect, *phonon-assisted tunneling* and *direct tunneling*. The Poole-Frenkel effect is an electric field induced lowering of potential barrier for the thermal emission of a carrier from a level in the bandgap. The Poole-Frenkel effect occurs in the case of charged defects while phonon assisted tunneling occurs for defects which are both charged as well as neutral.

The ionization probability due to electric field increases as [3.32]:

$$\frac{e(E)}{e(o)} \propto e^{\left(\frac{\varepsilon_{pf}}{k_B T}\right)} \tag{3-23}$$

where the lowering of the barrier ε_{pf} is given as:

$$\varepsilon_{pf} = 2\sqrt{\frac{Zq^3 E}{\chi}} \tag{3-24}$$

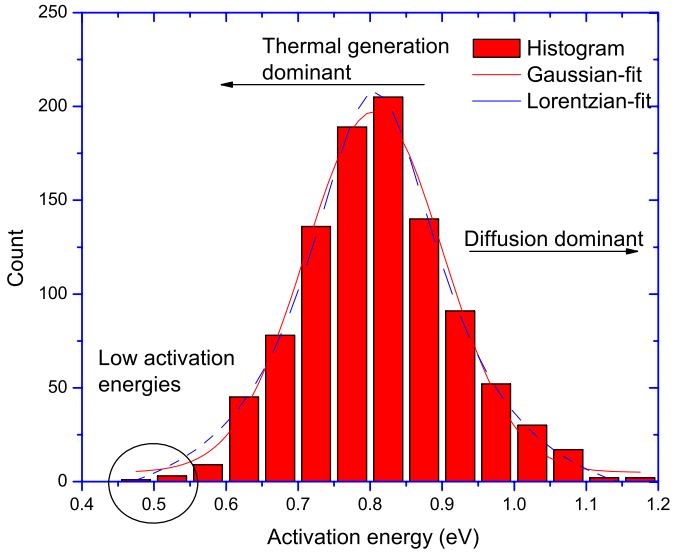


Fig. 3-15 *Histogram of the activation energies of some 1000 pixels in a CMOS image sensor.*

Here Z is the charge of the centre, q is the electronic charge, E is the electric field strength and χ is the dielectric constant. This equation tells us that the emission in an electric field, denoted by $e(E)$, increases exponentially to the square root of the electric field.

The emission rate in the case of phonon-assisted tunnelling is given as [3.32]:

$$\frac{e(E)}{e(0)} = e^{\left(\frac{E^2}{E_c^2}\right)} \tag{3-25}$$

where E_c is the characteristic field strength, given by:

$$E_c = \sqrt{\frac{3m^* h}{q\tau_t^3}} \tag{3-26}$$

where m^* is the effective mass of charge carriers, τ_t is the tunnelling time. We thus find that the emission increases exponentially with the square of the electric field for phonon-assisted tunnelling.
Figure 3-15 shows the histogram of the activation energy of some 1000 pixels of a 4-T CMOS image sensor in 0.18-μm technology. The activation energy histograms has a wide span, which ranges from $E_g/2$ to E_g. A detailed description of activation energies has been covered in Chapter 2. As can be observed from the figure, some pixels reveal an activation energy < 0.56 eV, which is physically not possible. These pixels provide a clue that hints towards an activation energy lowering mechanism in action, as described in the previous section.

It is known that the high electric fields at the photodiode-transfer gate overlap is an important dark current mechanism in CMOS image sensors [3.33]. A 0.2 μm overlap is present between the pinned layer and the TX gate due to self-aligned process. A very strong electric field of 3×10^5 V/cm is present in this region (when the reset voltage of the FD node is ~ 2V) that gives rise to higher leakage current. This amounts to an emission enhancement factor of 18 in a 3-dimensional model [3.34]. Increasing the voltage on the TX gate moves the channel "pinch-off" point towards the photodiode region and results in an even higher electric field. This phenomenon can be expected to be worse for future devices where the dimensions are made smaller and thus leading to higher electric fields. Traps that are located in this high electric field region may exhibit a higher darker current than the traps located outside this local field. This could also lead to a higher RTS (Random Telegraph Signal) noise in the sensor [3.35].

The phenomenons described in this chapter are also revisited in Chapter 4 which deals with radiation effects in CMOS image sensors.

3.4 Chapter summary

In this chapter, a basic introduction to the 4-T CMOS image sensor has been presented. These imagers are state-of-the-art and have excellent qualities that make in at par with CCDs. The pinned

structure minimizes dark current and increases the sensors efficiency in the blue spectrum of visible radiation. Moreover, by applying CDS, very low noise levels can be achieved in these sensors.

The QE of such a sensor has been empirically modelled by solving the continuity equation as well as applying suitable boundary conditions. It was found that the heavily doped pinned region contributes to the sensors sensitivity at the blue spectrum. But since modern CMOS fabrication utilizes a thin epitaxial layer, the sensitivity towards the red photons is hampered. The model derived has been used later in this thesis to quantify the effects of radiation on the spectral response of these sensors.

The STI has a predominant contribution to the leakage mechanism. This is mainly through the high surface recombination velocity at the STI interface. By employing p-well passivation around the STI, the leakage currents from the STI can be substantially reduced. This is also evident later in this thesis, when various test structures with different STI configurations are subjected to irradiation. Those with a p-well protection exhibits a higher tolerance to the radiation process.

Very high electric fields present in modern day silicon devices contribute to a enhanced emission rates. The electric fields play a major role in reducing the activation energy of traps located in its vicinity. This was noticed in the activation energy histogram where pixels with very low activation energies were present. This is possible when there is a activation energy lowering mechanism like the Poole-Frenkel effect or phonon assisted tunnelling.

The discussion and results in this chapter are used as a precursor to comprehend and analyze the radiation effects on the sensor which will be presented in Chapter 4.

3.5 Acknowledgements

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3.6 References

[3.1] A. E. Gamal and H. Eltoukhy, “CMOS Image Sensors”, IEEE Circ. & Dev. Mag., pp. 6-20, 2005.

[3.2] J. R. Janesick, “Scientific Charge-Coupled Devices”, SPIE Publication, pp. 3-7, 2001.

[3.3] E. R. Fossum, “CMOS Image Sensors: Electronic Camera-On-A-Chip”, IEEE Trans. Elec. Dev., Vol 44, No. 10, pp. 1689-1698, 1997.

[3.4] M. Bigas, E. Cabruja, J. Forest, and J. Salvi, “Review of CMOS Image Sensors”, Micr. Elec. Journ., Vol. 37, No. 5, pp. 433-451, 2006.

[3.5] A. J. P. Theuwissen, “CMOS Image Sensors: State-of-the art”, Sol.St. Elec., Vol. 52, No. 9, pp. 1401-1406, 2008.

[3.6] B. Mheen, M. Kim, Y. J. Song, and S. Hong, “Operation Principles of 0.18-μm Four-Transistor CMOS Image Pixels With a Non-fully Depleted Pinned Photodiode”, IEEE Trans. Elec. Dev., Vol. 53, No. 11, pp. 2735-2740, 2006.

[3.7] H. Sumi, “Low-Noise Imaging System with CMOS Sensor for High-Quality Imaging”, Proc. IEDM, pp.1-4, 2006.

[3.8] D. X. D. Yang, B. Fowler, and A. E. Gamal, “A Nyquist Rate Pixel-Level ADC for CMOS Image Sensors”, IEEE Journ. Sol. St.Circ., Vol. 34, No. 3, pp. 348-356, 1999.

[3.9] A. Ferrero et al., “New Model for Internal Quantum Efficiency of Photodiodes based on Photocurrent Analysis”, Appl. Opt., Vol. 44, No. 2, pp. 208-216, 2005.

[3.10] A. Sinha, and S. K. Chatopadyaya, “Photocurrent in a Diffused p-n Junction”, Sol. St. Elec., Vol. 19, No. 4, pp. 345-346, 1976.

[3.11] A. Schenk, “Advanced Physical Models for Silicon Device Simulation”, Birkhäuser, pp. 52, 1998.

[3.12] D. K. Schroder, “Semiconductor Material and Device Characterization”, John Wiley and Sons, Inc., pp. 360-365, 1990.

[3.13] X. Zhang, “Investigation of n^+-p Diffused Junction Silicon Solar Cells”, Sol. St. Elec., Vol. 35, No. 11, pp. 1661-1665, 1992.

[3.14] H. Zimmermann, “Silicon Optoelectronic Integrated Circuits”, Springer, pp. 49, 2004.

[3.15] J. S. Lee, and R. I. Hornsey, “Analysis of CMOS Photodiodes - Part 1: Quantum Efficiency”, IEEE Trans. Elec. Dev., Vol. 50, No. 5, 2003.
[3.16] T. Lule et al., “Sensitivity of CMOS Based Imagers and Scaling Perspectives”, IEEE Trans. Elec. Dev., Vol. 47, No. 11, pp. 2110-2122, 2000.
[3.17] R. Doering, and Y. Nishi, “Handbook of Semiconductor Manufacturing Technology”, CRC Press, pp. 1-27, 2008.
[3.18] E. Rosencher, B. Vinter, and P. G. Piva, “Optoelectronics”, Cambridge University Press, pp. 480, 2002.
[3.19] Chipworks, “Inside CMOS Image Sensor Technology”, Elec. prod. rev. online., Ref. 13758, 2005.
[3.20] C. A. Lewis, “Evaluation of the Spectral Response for Thin Epi Back-Illuminated Photodiodes”, Master Thesis, Northeastern University, Boston, 2000.
[3.21] H. Ohyama et al., “Defect Assessment of Irradiated STI Diodes”, Nuc. Inst. Meth. B, Vol. 186, No. 1, pp. 424-428, 2002.
[3.22] C. R. Moon et al., “Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors”, IEEE Elec. Dev. Lett., Vol. 28, No. 2, pp. 114-116, 2007.
[3.23] H. I. Kwon et al., “The Analysis of Dark Signals in the CMOS APS Imagers From the Characterization of Test Structures”, IEEE Trans. Elec. Dev., Vol. 51, No. 2, pp. 178-184, 2004.
[3.24] L. S. Riley, S. Hall and J. Schitz, “Evaluation of Surface Generation Velocity of Sidewall Oxide Interfaces Formed by Dry Etching for Shallow Trench Isolation”, Sol. St. Elec., Vol. 44, No. 11, pp. 2093-2095, 2000.
[3.25] M. Nandakumar et al., “Shallow Trench Isolation for Advanced ULSI CMOS Technologies”, IEDM, pp. 133-136, 1998.
[3.26] P. D. Agnello, “Process Requirements for Continued Scaling of CMOS—The Need and Prospects for Atomic-level Manipulation”, IBM J. Res. Dev., Vol. 46, No. 2/3, pp. 317-338, 2002.

[3.27] P. R. Rao, X. Wang, and A. J. P. Theuwissen, “Degradation of CMOS Image Sensors in Deep-Submicron Technology due to γ-irradiation”, Sol.St. Elec.,Vol. 52, No. 9, pp. 1407-1413 2008.
[3.28] A. Steegen et al., “Silicide and Shallow Trench Isolation Line Width Dependent Stress Induced Junction Leakage”, Symp. VLSI. Tech., pp. 180-181, 2000.
[3.29] J. Bogaerts, “Radiation-Induced Degradation Effects in CMOS Active Pixel Sensors and Design of a Radiation Tolerant Image Sensor”, PhD thesis, pp. 5-15, 37-95, Katholieke Univ. Leuven, 2002.
[3.30] V. P. Gopinath, H. Puchner, and M. Mirabedini, “Impact of Shallow Trench Linear Oxidation Scheme on Junction Leakage”, Proc. ESSDERC, pp. 419-422, 2001.
[3.31] C-H Tung, G. T. T. Sheng, and C-Y Lu, “ULSI Semiconductor Technology Atlas”, pp. 235-240, Wiley-IEEE, 2003.
[3.32] S. D. Ganichev, E. Ziemann, and W. Prettl, “Distinction Between the Poole-Frenkel and Tunneling Models of Electric-Field-Stimulated Carrier Emission From Deep Levels in Semiconductors”, Phys. Rev. B, Vol. 61, No. 15, pp. 10 361-10 365, 2000.
[3.33] X. Wang, P. R. Rao, and A. J.P. Theuwissen, “Fixed-Pattern Noise Induced by Transmission Gate in Pinned 4T CMOS Image Sensor Pixels”, Proc. ESSDERC., pp. 331-334, 2006.
[3.34] J. R. Srour, and R. A. Hartmann, “Enhanced Displacement Damage Effectiveness in Irradiated Silicon Devices”, IEEE Trans. Nuc. Sci., Vol. 36, No. 6, pp. 1825-1830, 1989.
[3.35] Gordon R. Hopkinson, “Radiation Effects in a CMOS Active Pixel Sensor”, IEEE Trans. Nucl. Sci., Vol. 47, No. 6, pp. 2480-2484, 2000.

Radiation effects on CMOS image sensors

CMOS Active Pixel Sensors (APS) rival CCDs (Charge-Coupled Devices) in domains that include low power operation, on-chip integration of analog and digital circuitry as well as cost effectiveness. Since CMOS image sensors are utilized for applications involving the detection of signals as low as a few electrons as well as high energy photons (especially for medical/ outer-space applications), radiation tolerance of such devices is of primary concern [4.1], [4.4], [4.5]. Though many studies have been undertaken on the issue of radiation hardness of image sensors, not much work has been carried out on the state-of-the-art in the imaging world: 4-T (4-Transistor) CMOS image sensors. These sensors utilise a heavily doped p^+ pinning layer to isolate the photodiode from the surface. This reduces the leakage current from the surface and contributes to the performance of the sensor in the blue region of the visible spectrum, as discussed in Chapter 3. But the effect of radiation on image sensors in the presence of the pinning layer has not yet been studied. Similarly, the issue of leakage currents due to STI (Shallow Trench Isolation) structures was highlighted in Chapter 3. How sensitive are these structures to radiation? These are some of the questions that will be discussed in this chapter. The simple tool

introduced in Chapter 2, the gated-diode, is used as a radiation sensitive tool in this study. It is found that these devices are simple yet efficient in resolving radiation induced damages in advanced CMOS processes [4.6].

4.1 Radiation effects: Basics

All possible radiation effects are usually grouped into three basic types: transient effects, ionization damage and displacement damages [4.5]. Transient effects have not been included here since the scope of this study is to evaluate long-lived degradation. Ionization damage as well as displacement damages will be dealt in the following sections.

4.1.1 Ionization damage

Ionization damage is the dominant mechanism when energetic photons (γ and X-rays) interact with solid-state matter. This damage causes charge-trapping at Si-SiO_2 interfaces (in the gate region as well as the STIs) and trap build-up at these locations. Ionizing rays can interact with the atom under consideration in three different ways [4.2]:

Photoelectric effect: When ionizing radiations pass through a semiconductor material, the energetic photons ionize the target atom and generate electron-hole pairs (photoelectric effect). The photon is completely absorbed in this process. The vacancy thus introduced in the electron orbit may be filled by an electron in the outermost orbit of the atom, resulting in a low energy photo-electron to be released.

Compton effect: The incoming ionizing radiation is scattered on interacting with the atom, just like visible light is diffused from a rough surface. Here, the energy of the incident radiation is divided among the electron that is released and the scattered photon.

Electron-positron pair creation: The incident photon is completely annihilated. This phenomenon occurs for radiation energies of more

than 1.024 MeV. This energy increases with decreasing atomic mass (Z).

The probability of these interactions with the material under consideration depends on the atomic mass of the target [4.7]. The various effects of interaction as a function of the atomic mass and photon energy are depicted in Figure 4-1. For Silicon, the interaction of γ-rays with energy of about 1.25 MeV is mainly through the Compton effect. The energy of X-rays are lower than γ-rays: in the range of keV, and the interaction is mostly through the photoelectric effect.

Ionization damage affects the interfaces and are more damaging for certain devices (e.g., MOSFET) than displacement damages (whereby a neighbouring interstitial atom or vacancy is created thus modifying carrier lifetimes). MOSFETs are sensitive to interface effects since the conduction channel is very close to the surface and does not extend into the bulk.

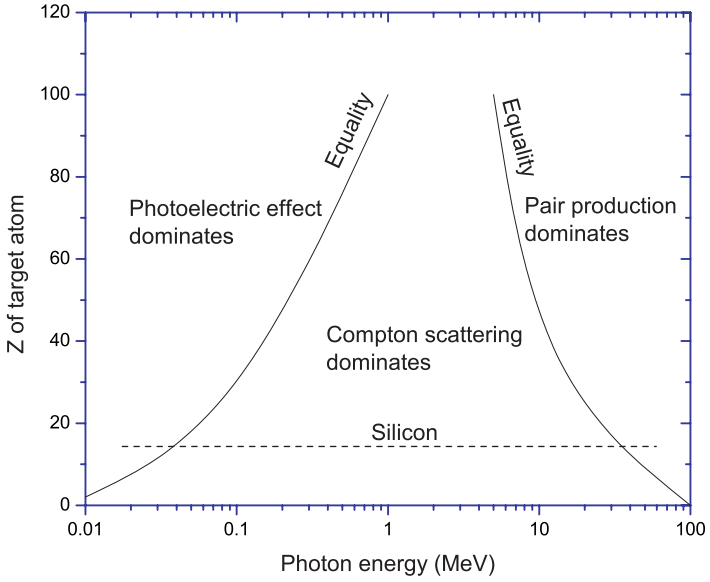

Fig. 4-1 *Interaction effects as a function of photon energy and atomic mass [4.7].*

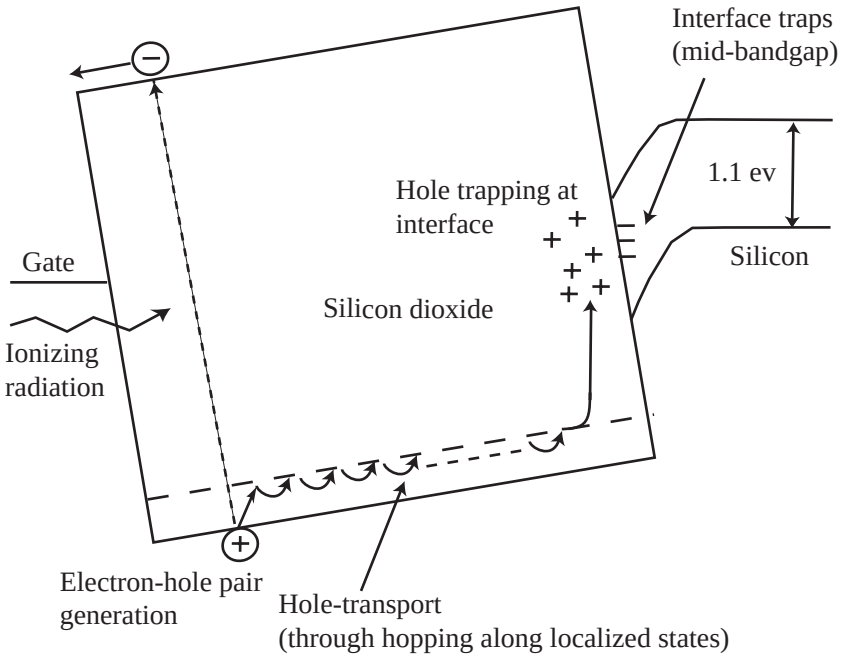

Fig. 4-2 *Depiction of various radiation effects in a positively biased MOS structure [4.3].*

For devices that rely on the semiconductor bulk, for e.g., long-length photodiodes, displacement damages can also start to play a role.

When ionizing rays strike a MOSFET, electron-hole pairs are formed due to photoelectric effect. Most of the generated electron-hole pairs in the doped polysilicon gate and in the semiconductor bulk recombine and disappear rapidly as these regions are highly conductive. In the oxide, a fraction of the generated charges recombine and the rest are separated by the electric field across the oxide. When a positive bias is applied on the gate, the electrons move rapidly (~ few pico seconds) towards the gate while the holes move slowly towards the Si-SiO_2 interface. This is because in the oxide region, electrons and holes have different mobilities which can differ by as much as twelve orders of magnitude. The movement of holes towards the interface is through a characteristic

transport phenomenon which is dispersive in time. Near the interface (but in the oxide), the trapped charges give rise to a net positive charge that can shift the threshold/flatband voltages. These events are summarised in Figure 4-2. The generation/movement/trapping of the charges is elaborated in Section 4.1.1.1. In addition to the above, charge trapping and interface traps generation will be explained in Section 4.1.1.2 and Section 4.1.1.3 respectively.

4.1.1.1 Charge generation and movement in the oxide

The amount of charge that is generated in the matter depends on the total amount of energy deposited by the particles. This amount is related to their LET (Linear Energy Transfer), which is the linear transfer of energy to the material by the particles. This factor depends on the nature of the incident particle and on the density of the material under consideration [4.7], [4.8]. Once the value of LET is known, the number of charges generated can be deduced from the fact that the generation of a single electron-hole pair in the oxide requires 17±1eV.

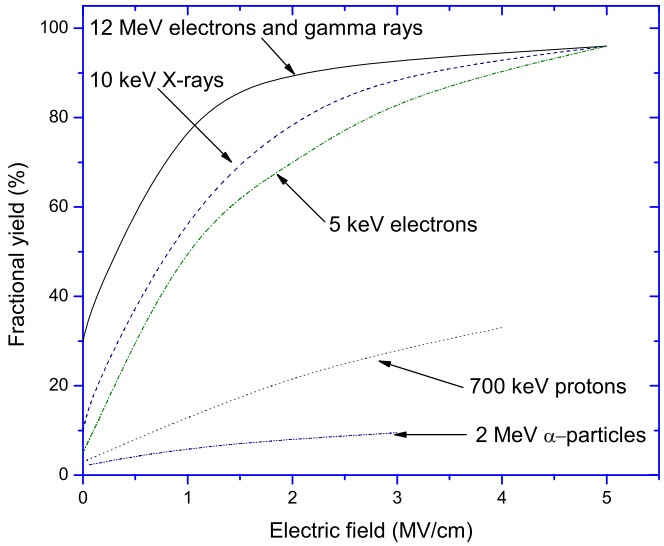

Fig. 4-3 *Fractional yield in SiO_2 as a function of the electric field for various particles [4.7].*

After a pico second of its generation, a partial recombination of the charge pairs occur. The percentage of the recombined pairs is a function of the LET as well as the gate-bias. For instance, the fractional yield due to γ-rays obtained through a Co^{60} source in silicon dioxide for zero gate-bias is 30%. For X-rays, this value is 10%. Increasing the electric field makes this value even higher. For electric fields above 5 MeV, the fractional yield is almost 100% [4.7]. The fractional yield in SiO_2 as a function of electric field for various particles is shown in Figure 4-3.

The charge mobility of electrons in an oxide is much higher than for holes as discussed in the previous section. E.g., the mobility for electrons at room temperature in the oxide is about 20 $cm^2V^{-1}s^{-1}$. For an electric field of 10^5 V/cm and an oxide thickness of 4 nm, the electrons that do not recombine transit in about 0.2 ps. The hole mobility in the oxide is much lower, varying from 10^{-4} to 10^{-11} $cm^2V^{-1}s^{-1}$ [4.3]. Thus hole trapping in the oxide is of much concern in ionization damage rather than electron trapping. As mentioned earlier, the transport of holes in the oxide is dispersive in time. The study of this phenomenon in silicon dioxide can be described by a model that is based on a concept known as *small polaron hopping* [4.9]. This mechanism is related to the strong interaction between the hole and the lattice. The presence of a hole polarizes (distorts the lattice) its immediate vicinity inside the medium, and the medium in turn reacts to this charge. If these interactions are strong enough, the carrier becomes localised at a particular site thereby increasing the effective mass of the carrier. The carrier which in principle is “self trapped” is called as a *small polaron*. When the hole moves through the insulator, it carries with it the potential well that arises from the distortion of the lattice. The motion is facilitated through thermal fluctuation of the system which permits tunnelling. This motion can be mathematically described by a model called as *CTRW* (Continuous Time Random Walk) which has been developed to study dispersive phenomenon in a disordered solid [4.7]. This model provides good time-scale response of the motion of holes as a function of the temperature, electric field in the oxide and oxide thickness.

To conclude this section, a simple relationship connecting the characteristic time-scale of hole transport process in the oxide (t_s) of

thickness (t_{ox}), the electric field (E_{ox}) at a temperature (T) can be given as [4.7]:

$$t_s = t_s^0 \left(\frac{t_{ox}}{a}\right)^{\frac{1}{\alpha}} \exp\left(\frac{\Delta_0 - 0.5qAE_{ox}}{kT}\right) \quad (4\text{-}1)$$

where a is the average hopping distance in the electric field direction, Δ_0 and t_s^0 are constants, and α is the principle parameter of the CTRW model linked to disorder in the solid and determined by detailed microscopic transport processes. In case of holes in silicon dioxide, α = 0.25. It can be seen that the characteristic time scale of the hole transport process in silicon dioxide varies with the fourth power of oxide thickness and decreases exponentially with the electric field and temperature. Thus, devices and technology that employ thin gate oxides can be considered to be less prone to radiation effects than those which employ thicker oxides.

4.1.1.2 Charge trapping in silicon dioxide

After the transport of the charges across the oxides, there is a possibility of holes being trapped very close (a few nanometers) to the Si-SiO_2 interface. This region is under mechanical stress and oxygen deficient. When the generated holes encounter this interface region, the strained bonds break and relax into an E' centre [4.3]. The model for the hole trapping and formation of an E' centre is depicted in Figure 4-4.

The trapping of holes at the Si-SiO_2 interface leads to negative threshold shifts represented by the term $\Delta V_{th(Q'_{ot})}$. This residual change can remain for a time period of a few milliseconds to several years. The amount of charges trapped is directly proportional to the number of defects in the interface and insensitive to the surface potential. The hole that reaches the interface is trapped according to the mean hole trap density (N_{ht}) and the field dependent capture cross section given by $\sigma_{ht}(E_{ox})$. The fraction f_T of trapped holes on which $\Delta V_{th(Q'_{ot})}$ depends can be given as [4.10]:

$$f_T = N_{ht}\sigma_{ht}(E_{ox})\Delta X \quad (4\text{-}2)$$

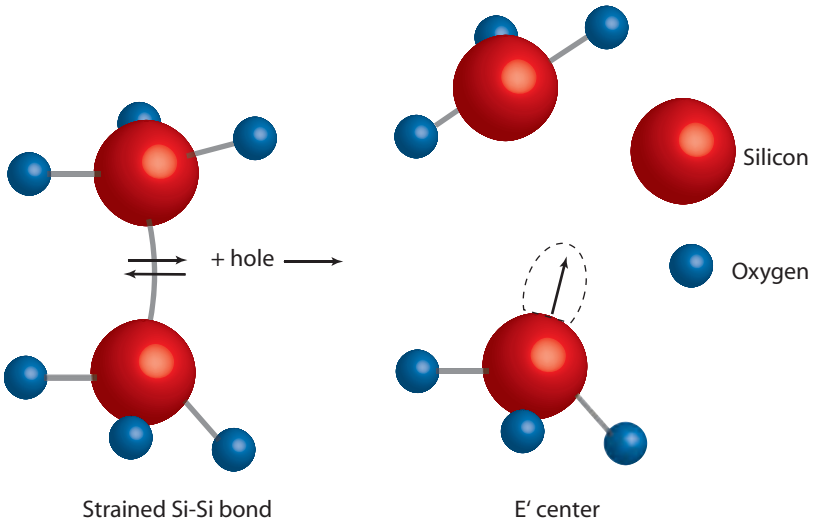

Fig. 4-4 *Model for hole trapping in SiO_2* [4.28].

where ΔX is the width of the trap distribution. Typical values for the parameters are, N_{ht} : 10^{18}-10^{19} cm^{-3}, $\sigma_{ht}(E_{ox})$: 10^{-14}-10^{-13} cm^2 [4.7].

This means that based on the quality of the oxide, the percentage of trapped holes can vary between 1% and 100%. The holes that are not trapped reach the Si-SiO_2 interface and recombine with the electrons mainly through three phenomenons:

- Recombination at the Si-SiO_2 interface.
- *Tunnel-based annealing effect* where a hole tunnels from the oxide into the silicon substrate and recombines with an electron.
- Recombination with an electron generated in the vicinity of the trapped hole, depending on the local density of the trapped hole (N_{ht}) and the electric field dependent capture cross-section area ($\sigma_{ht}(E_{ox})$). This phenomenon increases with radiation dose and contributes to the saturation $\Delta V_{th(Q'_{ot})}$ at high irradiation dose levels.

- Recombination of holes with thermally generated electrons in the oxide (thermal annealing).

The *probability of tunnelling* depends exponentially on the distance from the trap to the Si-SiO_2 interface and can be expressed as [4.7]:

$$P_{tun} = \alpha_f e^{-\beta x} \tag{4-3}$$

where α_f is the "attempt" to escape frequency, and β is a parameter related to the height of the potential barrier. Since electric fields reduce the barrier height for tunnelling to occur, this type of annealing is more effective at higher electric fields.

Thermal annealing can be explained as the thermal emission of radiation-induced holes from the traps in the oxide to the valence band in the oxide, where it conducts/hops to the substrate. The emission probability P_{em} of a hole from the oxide hole trap to the valence-band can be expressed as [4.7]:

$$P_{em} = AT^2 e^{-\left(\frac{q\phi_{vt}}{kT}\right)} \tag{4-4}$$

where A is a constant depending on trap cross-section and other parameters, and ϕ_{vt} is the difference between the trap and the valence band energies. From the equation, we see that the emission rate is decided by the temperature and is independent of the spacial distribution of the traps. Thus, this kind of annealing depends mainly on the energy distribution of the traps in the oxide. The tunnel annealing, on the other hand, depends on the spatial distribution of the traps in the oxide.

4.1.1.3 Radiation induced traps at the Si-SiO_2 interface

An important consequence of irradiation is the increase of radiation induced traps at the Si-SiO_2 interface. There are many competing hypotheses to explain this phenomenon, based on models that take into account electric fields, temperature and total dose. The radiation induced traps introduce energy levels in the bandgap (between the

valence and the conduction bands). Majority of the traps above the mid-bandgap are believed to be acceptors and those below; donors. An accurate analysis of the phenomenon requires a detailed knowledge of distribution of the traps rendering the analysis quite complicated. The three major hypotheses to explain the phenomenon are [4.7]:

- Direct creation of traps by radiation.
- Generation of traps due to hole trapping near to the surface.
- Traps due to secondary phenomenon.

Experiments carried out with UV radiation on thin metallic MOS gates confirm that traps were being generated at the interface despite the fact that UV radiation gets absorbed in the first few layers of the oxide [4.12]. Thus the experiments rule out a direct generation of interface traps due to radiation. Similarly, experiments also rule out the generation of traps due to hole trapping near the surface, as the interface build-up with respect to dose was found to evolve slower than the hole transport in oxide. The model by Winokur and McLean [4.13] proposes a two stage mechanism for the interface trap generation.

Upon irradiation, hydrogen ions (from the hydrogen and other impurities usually present due to the fabrication process) are set free from the oxides through the generated holes. These ions move towards the Si-SiO_2 interface upon the application of a positive gate-bias and form new states which act as traps. In this case, only the ions that are generated very close the interface give rise to interface traps. This model successfully explains the temperature dependency and time-evolution of the traps. Since the movement of ions is very slow, the time-evolution of traps is smaller than the hole transport in the oxide. At low temperatures, these ions “freeze” and give rise to relatively lower trap densities and hence the temperature dependency. But it fails to explain the electric field dependency of radiation-induced traps. One would assume, based on this model, that at higher electric fields holes are capable of setting out more hydrogen ions leading to a higher trap-generation. In reality, the

trap-generation has been verified to be inversely proportional to the square root of the electric field. This inconsistency was resolved through yet another model known as the $(HT)^2$ (*hole-trapping/ hydrogen-transport*) [4.14]. In this model, the holes drift towards the Si-SiO_2 interface and get trapped very near to it. They then release the hydrogen ions which in turn get trapped in the interface leading to the generation of traps. In this model, the hole capture cross-section area determines the electric field dependency, but the time-evolution is still determined by the motion of the ion. Hence it satisfies the experimental results entirely. One of the assumptions of the hypothesis is the generation of hydrogen ions in the entire oxide volume. Thus experimental results should reveal an interface trap-generation dependency based on the thickness of the oxide. This has been verified by some recent experiments (e.g., [4.15]).

The models that have been discussed are also able to explain the reason as to the larger trap formation in wet-grown oxides compared to dry-grown ones.

4.1.1.4 Radiation effects on electrical and optical parameters

Radiation induced voltage shifts

Radiation can shift the flatband/threshold voltages of MOS structures by introducing:

- Trapped charges in the oxide region.
- Charge introduced by the interface traps.

The flatband voltage shift, ΔV_{fb}, of an ideal MOS device (having no oxide charges or interface traps) due to irradiation can be given as [4.17]:

$$\Delta V_{fb} = -\frac{Q'_{ot} + Q'_{it}}{C_{ox}} \tag{4-5}$$

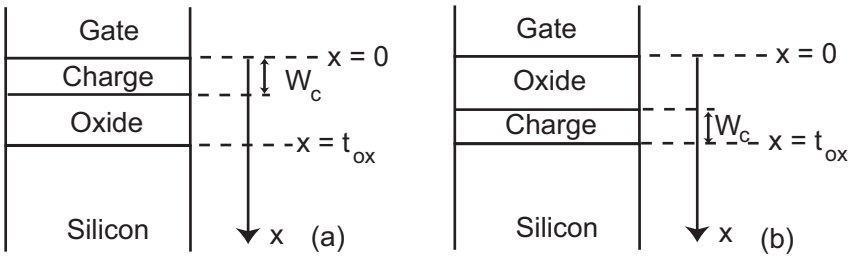

Fig. 4-5 *Charge accumulation at a) the upper part of oxide and b)lower part of oxide.*

where Q'_{ot} is the equivalent charge trapped per unit area in the oxide close to the Si-SiO_2 interface, Q'_{it} is the charge per unit area due to interface states, and C_{ox} is the oxide capacitance per unit area. The value of Q'_{ot} can be expressed as the integral of all charges in the oxide volume and given as:

$$Q'_{ot} = \frac{1}{t_{ox}} \int_0^{t_{ox}} x\rho(x)dx \tag{4-6}$$

where t_{ox} is the oxide thickness, x is the distance from the gate oxide interface and $\rho(x)$ is the distribution of charge density. It can be deduced from equations (4-5) and (4-6) that:

- The flatband shift is negative when Q'_{ot} is positive (lower gate voltage required for flatband condition) and
- The closer the charges are to the interface, the higher the shift.

The second statement can be understood better in this manner: Consider the situation where a uniform charge of charge density A is situated in the upper part of the oxide as shown in Figure 4-5 (a). In this case, we can formulate the boundary condition as $\rho(x < W_c) = A$ and zero everywhere else. The shift in the flatband voltage due to the presence of trapped charges can then be given as:

$$\Delta V_{fb(Q'_{ot})} = -\frac{AW_c^2}{2\varepsilon_{ox}} \tag{4-7}$$

where ε_{ox} is the SiO_2 permittivity. In case that the charges are present near the interface, (Figure 4-5 (b)), $\rho(t_{ox}-W_c<x<t_{ox}) = A$ and ($\rho(0<x<t_{ox}-W_c) = 0$, the shift in the flatband can be represented as:

$$\Delta V_{fb(Q'_{ot})} = -\frac{AW_c^2}{2\varepsilon_{ox}}\left(\frac{2t_{ox}}{W}-1\right) \tag{4-8}$$

We note that there is an additional multiplication factor in (4-8) compared to (4-7), being $2t_{ox}/W_c$. Since $t_{ox}>W_c$, a larger flatband shift can be noticed in this case. Moreover, another interesting observation can be made using (4-8). When t_{ox} is reduced retaining W_c a constant, the shift in the flatband is also reduced proportionally. Thus the thinner the gate-oxide, the more radiation tolerant the device would be especially in terms of variations due to charge-trapping.

The change due to the presence of charges at the interface can be simply equated as:

$$\Delta V_{fb(Q'_{it})} = -\frac{Q'_{it}}{C_{ox}} \tag{4-9}$$

where Q'_{it} is the amount of charges (per unit area) at the interface. The interface state build up is considered to be slower than the charge trapping phenomenon in the oxide.

The analysis for the threshold shift can be deduced in a similar fashion as:

$$\Delta V_{th} = -\frac{Q'_{ot}+Q''_{it}}{C_{ox}} \tag{4-10}$$

where Q''_{it} is the amount of charges trapped at the interface during the condition of inversion. It should be noted that the charge density at the interface (Q_{it}) is a function of the surface potential, and hence is different during flatband ($Q_{it} = Q'_{it}$) and inversion ($Q_{it} = Q''_{it}$) conditions.

Radiation induced leakage current

Ionizing radiations can cause increased generation primarily through the creation of addition interface states in the oxide/silicon interfaces. Assuming a uniform interface trap density across the bandgap, the generation rate can be expressed by integrating the contribution from all interface traps in the bandgap and is given as [4.28], [4.18]:

$$G = \frac{1}{2}\sqrt{(\sigma_n \sigma_p)} v_{th} D_{it} \pi k T n_i \tag{4-11}$$

This equation reveals that the contribution of traps from the energy window of πkT around E_i is of importance, and generation through traps located further away from mid-gap is negligible. Using (4-11), generation current density through the surface can be conveniently written as:

$$J_{surf} = q s_0 n_i \tag{4-12}$$

where s_0 is the surface recombination velocity in cm/s. Thus, an increase in interface traps result in a proportional increase in s_0.

Radiation induced optical changes (top layer material stack)

Radiation affects optical materials in three different ways:

- The darkening of these materials when exposed to ionizing radiation. This effect is supposed to be due to the introduction of new energy levels (color centres) within the bandgap of the material under consideration, and also the trapping of electrons/holes in these defect sites.

- Changes in the reflection from the surface through a change in the material properties like refractive index.

- Changes in surface properties like increased surface roughness and "pit" formation.

The darkening is usually modelled as [4.16]:

$$T(\lambda,D,x) = T_o e^{-\alpha_D x_{opt}} \tag{4-13}$$

where T is the transmittance at wavelength λ, through an optical path x_{opt}, after a total dose of D, T_0 is the initial transmission and α_D; the absorption coefficient after irradiation. Here α_D can be written as:

$$\alpha_D = \alpha_{sat}(1-e^{-\beta_a D}) + KD \tag{4-14}$$

α_{sat}, β_a and K are independent of dose, but depend on material and wavelength. The term with α_{sat} and β_a denote absorption due to inherent defect sites.

For doses which are < $1/\beta_a$, K can be neglected and (4-14) expanded to a first order approximation as:

$$\alpha_D \approx \alpha_{sat}\beta_a D \tag{4-15}$$

Thus, for small doses, the modified absorption coefficient can be considered to be linear with dose.

Ionizing radiations can also bring upon "densification" in oxides (glasses). This, in turn, affects the refractive index of the material and can lead to severe aberrations in optical instruments and detectors. In the case of high energy photon irradiation like γ-rays, densification occurs due to optically active point defects created by the breaking of atom-to-atom chemical bonds in the oxide. The energy of a single γ-ray photon is enough to break a Si-O bond. Dopants as well as intrinsic defects play a significant role in the glass network modification process. Thus, the maximum radiation hardness is observed in "pure" glasses that do not have impurities in them.

Bulk refractive index changes can be estimated by the differentiated Lorentz-Lorentz relation [4.21]:

$$\frac{\Delta n}{n} = \frac{\Delta \rho}{\rho}(1+\Omega)\frac{(n^2-1)(n^2+2)}{6n^2} \tag{4-16}$$

where n is the refractive index, $\Delta\rho/\rho$ is the relative compaction, and Ω is a parameter based upon whether the densification was elastic or inelastic.

4.1.2 Displacement damage

If the energy is high enough, ionizing radiations can also affect both the generation current (by the introduction of additional energy levels in the silicon bandgap), as well as diffusion currents. This phenomenon is usually very small in the case of γ- and X-rays, but nevertheless, not completely absent. Thus, this phenomenon is also discussed for completeness.

The generation rate U due to bulk defect states located at an energy E_t under the assumption that the free carrier concentration of holes and electrons are significantly less than their equilibrium values can be written as [4.18]:

$$U(E_t) = \frac{\sigma_n \sigma_p v_{th} N_T n_i}{\sigma_n \exp\left[\left(\frac{E_T - E_i}{kT}\right)\right] + \sigma_p \exp\left[-\left(\frac{E_T - E_i}{kT}\right)\right]} \tag{4-17}$$

where σ_n and σ_p are the capture cross-section area of electrons and holes respectively, v_{th} is the thermal velocity, N_T is the trap density per unit volume, E_i is the intrinsic Fermi level and k is the Boltzmann constant. Under the assumption, the generation process dominates the recombination process. Radiation-induced dark current density increase, ΔJ_D in the bulk-depletion regions of the sensor can be written as [4.19]:

$$\Delta J_D = \frac{q n_i \phi W}{K_g} \tag{4-18}$$

where ϕ is the particle fluence, W is the depletion width and K_g is the generation lifetime damage coefficient for a particular particle type and energy defined through the relation [4.19]:

$$K_g = \frac{\phi}{\left[\frac{1}{\tau_0} - \frac{1}{\tau'_0}\right]} \tag{4-19}$$

where τ_0 and τ'_0 are pre-and post-irradiated generation lifetimes respectively. Assuming that a single trap of energy level E_T is responsible for the thermal generation process, (4-17) can be conveniently re-written in terms of generation lifetime as:

$$\tau_0 = \tau_p \exp\left[\left(\frac{E_T - E_i}{kT}\right)\right] + \tau_n \exp\left[-\left(\frac{E_T - E_i}{kT}\right)\right] \tag{4-20}$$

where the pre-factors are: $\tau_p = (\sigma_p v_{th} N_g)^{-1}$ and $\tau_n = (\sigma_n v_{th} N_g)^{-1}$. Here, N_g is the generation centre density. This equation is a general relationship between the generation lifetime, capture cross-section of electrons/holes, the generation density as well as the energy of the trap. From this equation, we can arrive at the conclusion that the increased thermal generation through radiation-induced generation centres is the basic mechanism responsible for the increased leakage current in the depletion region [4.19]. The value of K_g for a particular type of radiation particle and energy is usually correlated through experiments.

Displacement damage usually signifies creation of generation centres in the silicon bandgap. This has the effect of decreasing the generation lifetime, τ_0 and thus a higher dark current. K_g is inversely proportional to the generation lifetime. It has been established that impurities in the silicon are not responsible for this effect through various experimental studies. For generation via mid-gap, the generation rate G expressed in (4-17) reduces to:

$$G = \frac{\sigma_n \sigma_p}{\sigma_n + \sigma_p} v_{th} N_T n_i = \sigma v_{th} N_T n_i \tag{4-21}$$

The generation current density is then given by:

$$J_{bulk} = \frac{qn_i W}{\tau_0} \tag{4-22}$$

4.2 Experimental

An important goal of radiation studies is to correlate the effect of radiation on the properties of materials and devices. The unit used to describe the average energy or dose (ionization) that a material receives during an irradiation is termed as *Gray* (1 J/kg). The equivalent quantity for displacement damages is the non-ionization dose which does not have any particular unit. Definition of the basic radiation units started to be developed in the 1950s, with the introduction of linear energy transfer (LET). The special unit of the radiation absorbed dose is the *rad* (100 erg/g). It was observed that many biological phenomenons could be correlated on the basis of the average energy deposited independent of the characteristics of the particular radiation causing it. The launching of satellites in the 1950s and the resulting discovery of the Van Allen belts broadened the interest of the radiation effects community. The radiation response of semiconductor devices became a major area of study during this and the following era.

In this work, radiation effects of γ-rays have been studied. X-rays and γ-rays are the same class of radiations (i.e., photons), with γ-rays having more energy and thus the ability to displace atoms to some extent. The results from the experiments shed light on the performance of semiconductors fabricated in deep sub-micron technology in general, and specifically on CMOS image sensors fabricated in the same technology. The results can be used to model the behaviour of the sensor if it were used for outer-space or for medical applications, including X-ray detection.

Co^{60} γ-source was used to study ionization ray induced damage in CMOS image sensors. The facility of Reactor Institute Delft (RID) was utilized for the study. As long as their energy is above a threshold, the secondary electrons produced by the incident γ-rays are

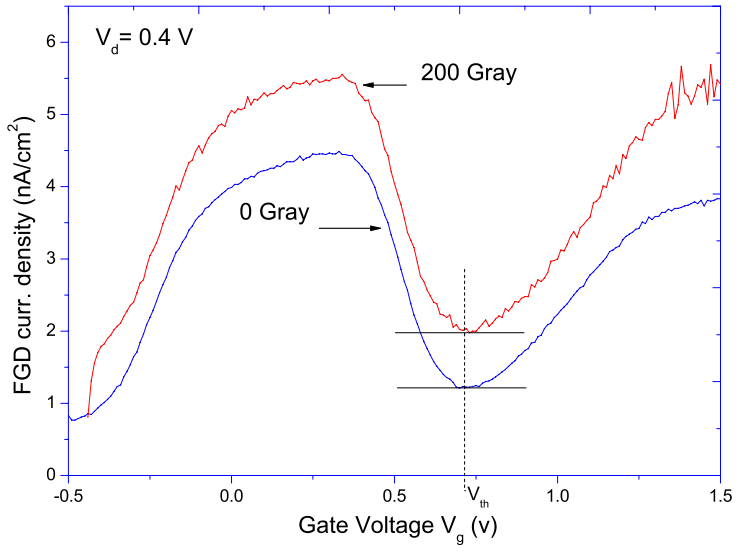

Fig. 4-6 *Radiation response of the FGD to a irradiation dose of 200 Gray.*

capable of displacing atoms to some extent. The γ-ray (1.17 MeV-1.33 MeV) dose used for the experiments was from 0 to 1000 Gray in steps of 200 Gray, with a dose rate of 75.9 Gray/min. The source was calibrated using *Fricke dosimetry* technique. All the test structures for the experiments were fabricated in Philips' 0.18-μm CMOS technology, and was kept unbiased during the irradiation.

4.2.1 Radiation mechanisms resolved by finger gated-diodes

The finger gated-diode (FGD) introduced in Chapter 2 has been used to resolve the radiation damage mechanisms. Figure 4-6 shows the response of the FGD to an irradiation dose of 200 Gray. An obvious increase in the response can be seen after irradiation. The mechanism for this shift is an increase in the number of interface traps in the surface and/or in the bulk that leads to a higher leakage current. The point of inversion of the curves remained unchanged indicating that no charge trapping has occurred in the SiO_2 region that can shift the flatband or threshold voltages concurrent with the earlier discussions.

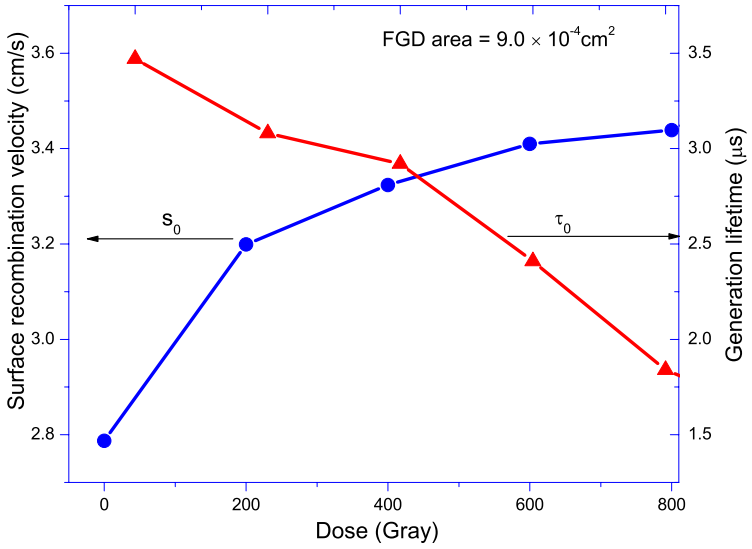

Fig. 4-7 *s_0 and τ_0 resolved using the FGD.*

This is especially encouraging since 4-T CMOS image sensors include in-pixel amplifiers and transistors for its operation. Radiation induced threshold as well as gain variation in these transistors will be minimal.

Figure 4-7 shows the variation of s_0 and τ_0 as a function of radiation dose resolved using the FGD (using (2-6) and (2-7) of Chapter 2 respectively). The surface component increases monotonically and saturates at higher doses. The bulk component, on the other hand, exhibits a rapid change after 400 Gray. The surface recombination velocity, s_0, is related to the fast surface states in the interface, assumed to be uniformly distributed in energy near the centre of the silicon bandgap. Thus an increase in the surface recombination velocity implies a proportional increase in the density of fast surface states located near the middle of the bandgap. The fact that there is a change in the value of s_0 despite its very small initial value of 2.8 cm/s, indicates that the degradation is not related to the initial interface quality [4.12]. This means that degradation is not specific to “defective” devices.

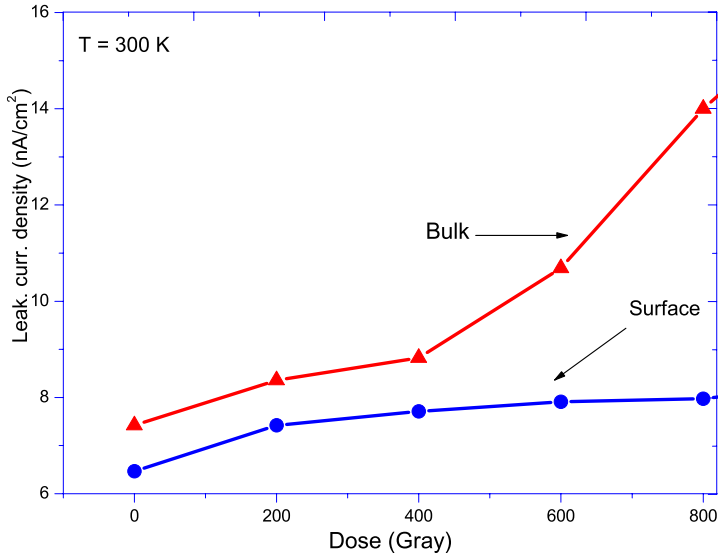

Fig. 4-8 *The reverse-computed current components using the obtained s_0 and τ_0 values.*

The leakage currents reverse-computed from the s_0 and τ_0 parameters are shown in Figure 4-8. A similar knee-point for the the leakage current in the Figure 4-8 was noticed by [4.22]. They contribute it to the fact that radiation-induced defects are divacancy and oxygen-vacancy (O-V) centres which are *amphoteric* (i.e. acts as both generation as well as recombination centres). Radiation-induced electron traps would saturate at high radiation doses, increasing the density of excess electrons reaching the n^+ drain region. In our case, however, it should be kept in mind that the leakage contribution from the STI is coupled with the bulk component as was discussed in Chapter 2 (Section 2.2.3). Because the area of the depletion region which interacts with the STI is very small, the surface recombination velocity of the STIs need to be very high for a significant contribution. Many studies have indeed reported a very high surface recombination velocity as was indicated in Chapter 3, Section 3.3.1. Thus, it is difficult to ascertain the cause of the increase in the bulk

leakage from Figure 4-8. Since displacement damage due to γ- or X-rays is quite limited, the contribution of bulk depletion regions to the leakage increase is doubtful. The degradation of the STI is further investigated in the next section. This helps to come to a clear conclusion regarding the bulk leakage current in the FGDs. However, from the current FGD results, it can be concluded that an increase in the radiation induced leakage current density with a slope in the range of a few pA/cm^2/Gray for both the surface as well as the bulk component occurs. The surface leakage is seen to evolve slowly, and saturate at higher radiation doses. Further, no threshold shift occurs implying that the gate region is highly radiation tolerant.

4.3 Radiation effects on CMOS image sensors

4.3.1 Dark-signal degradation

With the continuing reduction of dimensions in CMOS technology, isolation techniques have gained great prominence. The two important isolation techniques for sub 0.25-μm processes are the STI (Shallow Trench Isolation) as well as PELOX (Polysilicon Encapsulated Local Oxidation) techniques. The increased mechanical stress in both STI as well PELOX contributes to higher leakage currents. Defect analysis through spectroscopic techniques have confirmed that the peripheral leakage current is determined by the isolation technique used, while the area component is due to defects during processing [4.27]. For sub 0.25-μm processes, STI is the only viable scheme of achieving high packing densities [4.23]. The STI is considered to be the prominent mechanism of leakage current in 4-T CMOS image sensors that employ pinned photodiodes [4.24], [4.25]. The generation rate can be characterized through the surface recombination/generation velocity at the interface and also by the generation lifetime in the bulk of the STI, the interface effects being prominent [4.26]. The STI has been treated fairly well in Chapter 3. Protecting the STIs by p-well structures has proved useful against STI induced leakage mechanisms. But not much work has been done to characterize the effect of radiative environments on such structures.

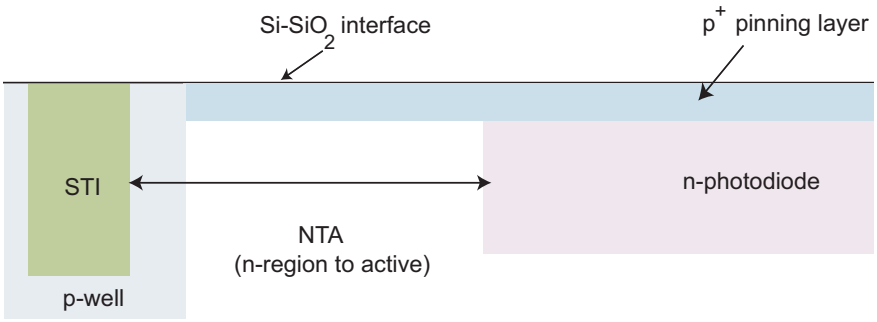

Fig. 4-9 *Layout schematic for the test structures.*

Parameter	Value
Technology	0.18-μm Philips process
Pixel pitch	3.5 μm
Conversion gain	40 μV/e
W/L (source follower)	0.46 μm/0.34 μm
Transfer gate length	0.6 μm
Operating voltage	3.3 V
Integration time for measurements	6.4 ms
Dark current (300 K)	0.3 nA/cm^2
Spectral range	~350-900 nm
Peak external quantum efficiency	37%

Table 4-1. *4-T CMOS image sensor parameters.*

In this study, radiation effects as a function of type of layout (with and without p-well protection) and distance separating the STI from the photodiode, has been carried out. Test structures (Figure 4-9) with and without p-well protection were fabricated for two different "p-well to active region" distances (NTA) to estimate the degradation due to γ-ray irradiation in these configurations. All test structures were fabricated in Philips' 0.18-μm CMOS technology and had properties listed in Table 4-1. The tests were carried out on 36k pixels of each configuration. The histograms of the dark signal (i.e., no of pixels (count) vs. dark signal in digital number (DN)) of the sensors (Figure 4-10 to Figure 4-13) reveal that the radiation-induced degradation mechanism is sensitive to the nature and the location of the STI. The largest degradation is seen in structures that have unprotected STIs. Further, structures that have the STI closer (NTA = 0.2 μm) to the photodiode is seen to degrade faster than the structures that have the STI further apart (NTA = 0.3 μm). The results are summarized in Figure 4-14. A larger value of NTA results in higher immunity to radiation damage, but this value should be optimised so the sensitivity and saturation level of the sensor is not overly sacrificed.

Since the doping density of the p-well region is relatively higher than that of n-type region of the photodiode, the STI is isolated from the depletion region during integration for structures with p-well protection [4.25]. This explains the slower degradation of these structures to irradiation.

From Figure 4-14, it can also be observed that the diode structures that are "completely" isolated from the STI (case NTA = 0.3 μm, p-well protected), the dark signal evolution is negligible. As the diode has a large depletion region, this points to the fact that displacement damages due to γ- or X-rays is negligible. This should also be true for the FGD structures, and it can be safely concluded that degradation of the STI region is primarily responsible for increase in I_{fij} in the FGD structures as well.

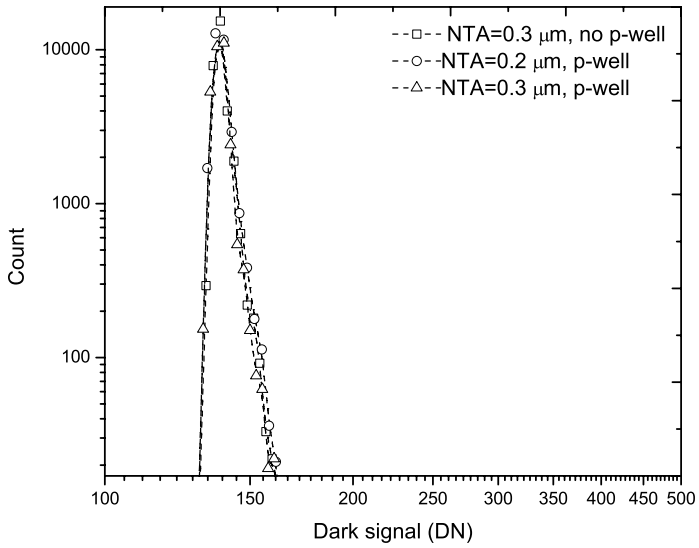

Fig. 4-10 *Dark signal histogram of un-irradiated sensors (T = 300 K).*

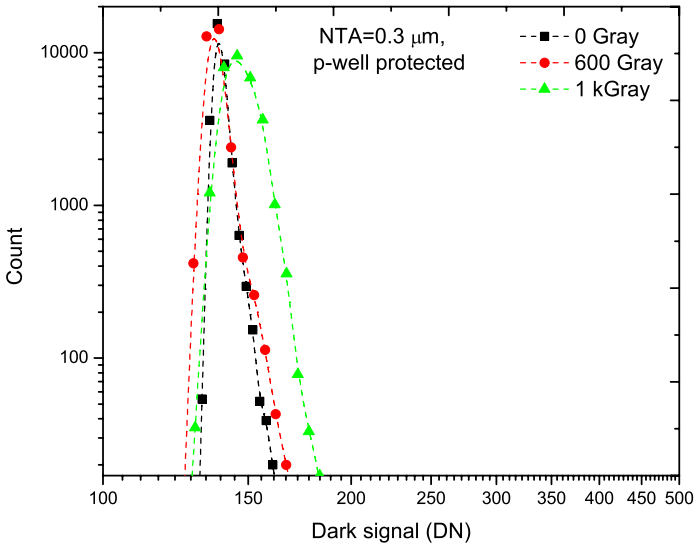

Fig. 4-11 *Dark signal histogram, NTA = 0.3 μm, with p-well (T = 300 K).*

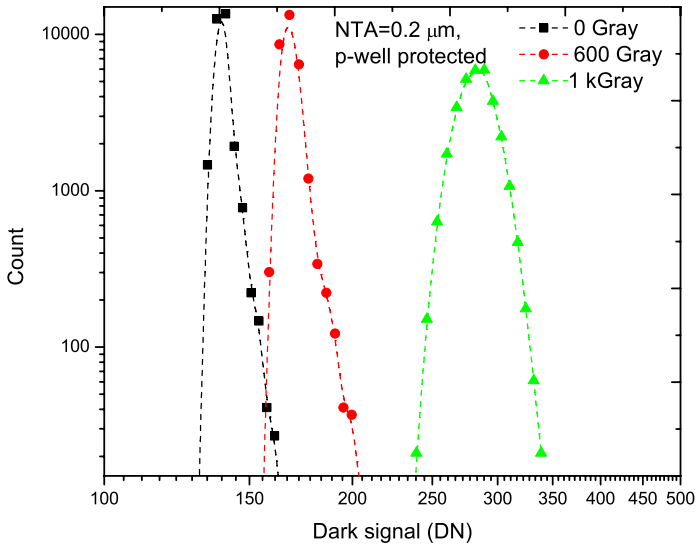

Fig. 4-12 *Dark signal histogram, NTA = 0.2 μm, with p-well (T = 300 K).*

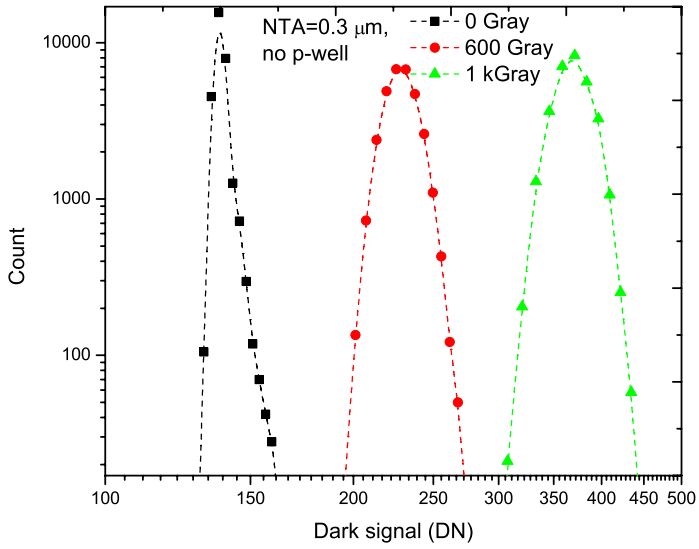

Fig. 4-13 *Dark signal histogram, NTA = 0.3 μm, no p-well (T = 300 K).*

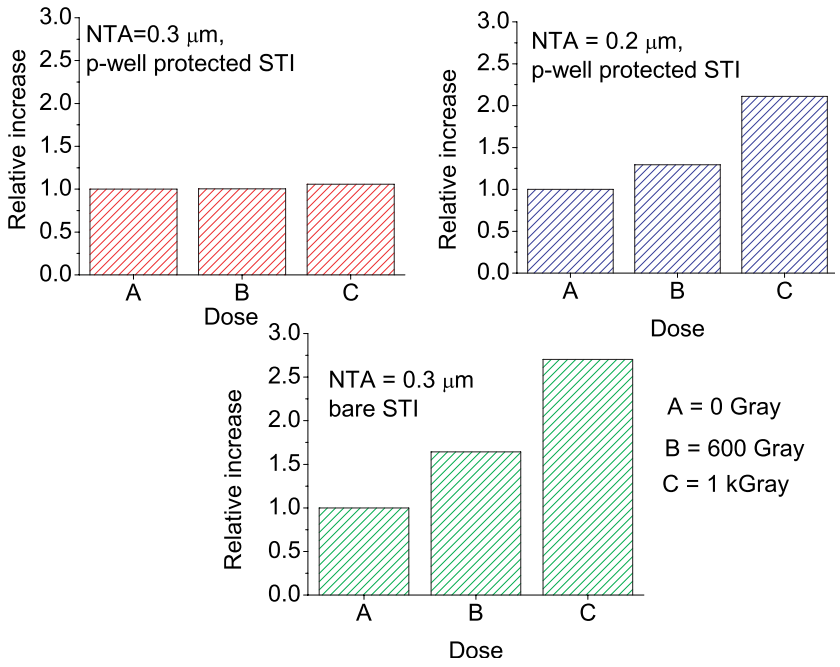

Fig. 4-14 *Relative increase in the mean dark signal w.r.t. dose for the three sensors. All measurements were conducted at T = 300 K.*

The Arrhenius plot of the mean dark current of un-irradiated as well as radiated sensors is shown in Figure 4-15, carried out on the sensor with NTA = 0.3 μm, bare STI. The activation energy of silicon devices such as CMOS image sensors usually lie anywhere between E_g (1.12 eV; characteristic of a diffusion process) and $E_g/2$ (0.56 eV; characteristic of a thermal generation process). Generally, at room temperature, the thermal generation process dominates the diffusion mechanism. However, pixels with a low dark current may also see a diffusion current dependence [4.28]. Upon irradiation of the sensors, it was found that the average activation energy of the sensors was reduced and the slope tends towards the slope of thermal generation. From the above discussions, this appears to be due to the introduction of additional energy states, that enhances thermal generation.

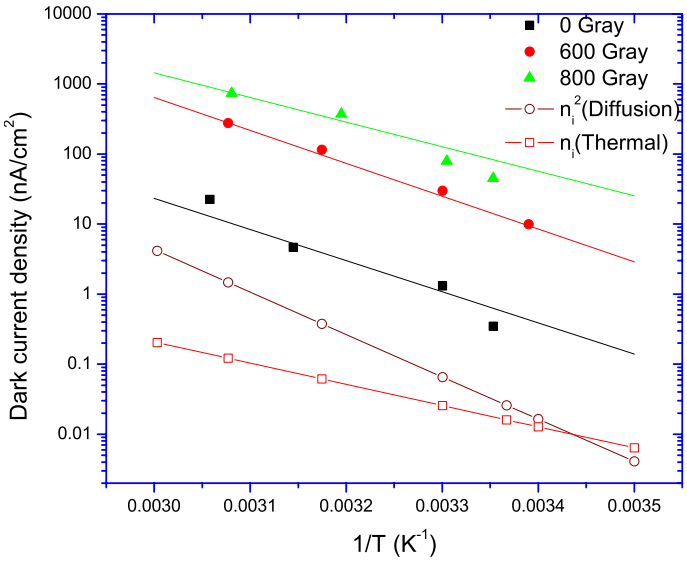

Fig. 4-15 *Arrhenius plot of radiated and un-irradiated sensors. The scaled slopes of n_i and n_i^2 are shown for reference.*

Other processes like trap-assisted tunnelling and field-enhanced emissions can also be thought to play a role in this behaviour (see Chapter 3). The emission rate from a defect that is located in a high local electric field is believed to increase dramatically [4.28], [4.29]. To further investigate this phenomenon, the activation energies of some 1000 pixels (of a radiated sensor) as a function of dark current (Figure 4-16 to Figure 4-18) were extracted. The activation energy of the pixels forms a band from 1.2 eV to 0.56 eV, with most of the pixels being concentrated around the mean activation energy of the sensor. Pixels with lower activation energies were seen to exhibit a higher dark current. It can also be seen that these pixels are very sensitive to temperature (Figure 4-17, Figure 4-18). These findings reveal a field-enhancement mechanism in action [4.5], [4.29] as was explained in detail in Section 3.3.2 of Chapter 3. High electric fields reduce the activation energy for thermal emission. The high electric field at the photodiode-transfer gate overlap is an important dark current mechanism in CMOS image sensors [4.30].

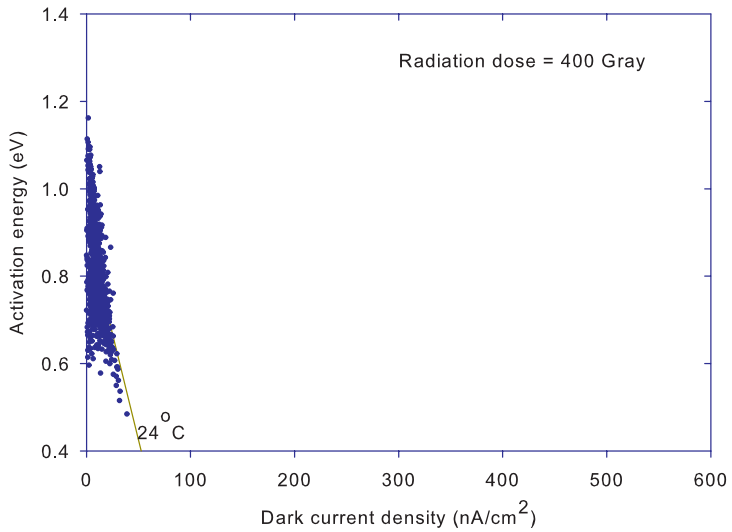

Fig. 4-16 *Leakage current vs. activation energy of 1000 pixels at 24° C.*

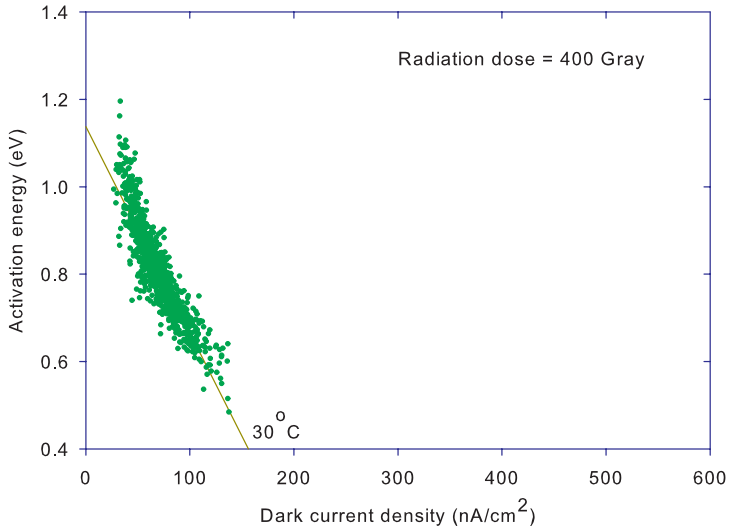

Fig. 4-17 *Leakage current vs. activation energy of 1000 pixels at 30° C.*

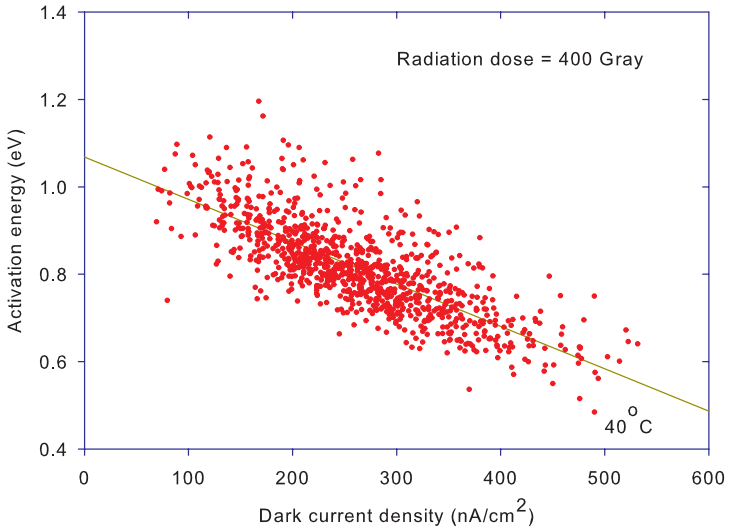

Fig. 4-18 *Leakage current vs. activation energy of 1000 pixels at 40 °C.*

A 0.2 μm overlap is present between the pinned layer and the transfer gate due to self-aligned process. A very strong electric field of ~ 3×10^5 V/cm is present in this region (when the reset voltage of the floating diffusion node is ~ 2V) that gives rise to higher leakage current during charge transfer. This amounts to an emission enhancement factor of 18 in a 3-dimensional model [4.31]. Increasing the voltage on the transfer gate moves the channel “pinch-off” point toward the photodiode region and results in an even higher electric field. This phenomenon can be expected to be worse for future devices where the dimensions are made smaller and thus leading to higher electric fields. Traps that are located in this high electric field region may exhibit a higher darker current than the traps located outside this local field. This could also lead to a higher RTS (Random Telegraph Signal) noise in the sensor [4.29]. Clearly, further studies are necessary in this direction to establish the mechanism by which such electric fields interact with traps introduced through irradiation and the effect of future aggressive technologies where dimensions are continuously being shrunk.

4.3.2 Optical degradation

The spectral response degradation is the result of changes to the top-layer materials that form as part of the fabrication process above the photodiode element, as well as its Si-SiO_2 interface. In this section, the change in the spectral response of a 4-T (4-Transistor) CMOS image sensor due to irradiation is studied. To further investigate the effects, FTIR (Fourier Transform Infrared) as well as ellipsometry is carried out on some commonly used materials that form the top-layer of a standard 0.18-μm CMOS process.

4.3.2.1 Sensor spectral characteristics

A detailed analysis of the 4-T CMOS image sensor as well as its spectral characteristics has been introduced in Chapter 3. The model that was developed is used to resolve the radiation induced degradation mechanisms in the sensor. This has been carried out by fitting the response curve with the variables s (the surface recombination velocity) that affects the photons in the shorter wavelengths, and a correction factor for the mean; ζ_{opt}. Figure 4-19 shows the normalized quantum efficiency of radiated as well as un-irradiated devices.A very good fit for all the curves is obtained by using the correction factor ζ_{opt} as well as the term for surface recombination velocity, $s = s_{eff}$.

From Section 4.2.1 on gated-diodes, it can be seen that there is negligible change in the threshold as well as gain of in-pixel transistors due to irradiation. Thus the parameter ζ_{opt} can be decoupled from such electrical variations and related mainly to the optics. ζ_{opt} reflects the need for a correction factor in the model to fit the irradiated curves through the mean. This arises due to the effect of operating a non-linear change in the internal QE as a function of s on the "wavy" interference pattern produced by the optical stack. In other words, the peaks and valleys of the interference pattern are modulated (pulled up and down in different rates) by the change in the internal QE spectra. Other optical factors, like the presence of color centres if any, will also be reflected in this term.

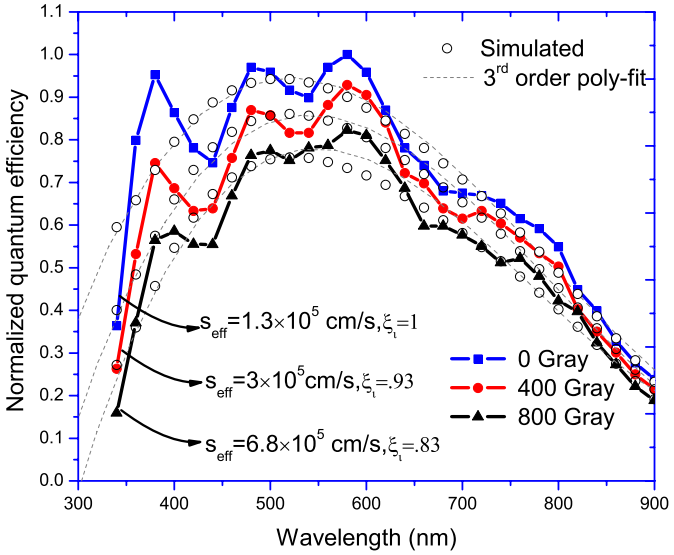

Fig. 4-19 *Normalized quantum efficiency of radiated and un-irradiated sensors and the fit through the model.*

Also, it is worthwhile to note that only an effective surface recombination velocity (s_{eff}) can be determined by this approach since wavelength-depended properties of the optical stack has not been included in the model. Nevertheless, the relative change in this parameter offers insight into the degradation of the Si-SiO_2 interface quality of the photodiode element.

The extracted s_{eff} parameters indicated in Figure 4-19 reveal an increase in the Si/SiO_2 interface traps and thus the surface recombination velocity. As explained in Chapter 3, the blue and green photons are primarily affected by the interface traps resulting in a modified internal QE spectra. Furthermore, the peaks and valleys are also modulated by this change. This in turn affects the mean value of the curves indicated by the need for ζ_{opt}. From Figure 4-19, a smoothening of the sharp peaks found in the un-irradiated devices can be seen on radiated devices. This may be due to a change in the material properties due to irradiation.

High energy rays such as γ-rays can change the material properties of the materials they penetrate and mainly interact through electronic excitation, electronic ionization and limited atomic displacements as has been discussed in 4.1.1.4. As a result, color centres can be introduced in the material [4.35]. Moreover, material densification can also occur. It is not immediately clear how much of these phenomenons play a role in the present result. To further investigate this phenomenon, radiation studies on oxides were conducted and have been presented in Section 4.3.2.2. This also helps us to understand the nature of ζ_{opt}.

The variation of the lifetime in the epi-layer does not have much effect in the present sensor, with a thickness of a few micrometers. Since γ-ray irradiation do not produce significant displacement damages as can be seen from the results of the experiments presented in this chapter, the change in lifetimes due to radiation can be safely neglected.

4.3.2.2 Radiation effects on oxides

Various oxides form the top-layer of conventional CMOS processes as shown in Figure 4-20. In general, as the number of metal layers in the fabrication process increases, so does the stack height due to the oxides. Usually, the designer is not offered any control over the type of oxide that has been used in the fabrication process or its thickness. Hence the study of radiation effects on oxides begs importance. The results will be helpful in modifying the process flow for increased radiation tolerance of CMOS image sensors.

The oxides that are usually used as part of the process flow are BPSG (Borophosphosilicate glass), and TEOS (Tetraethyl Orthosilicate). Another material that may form as a passivating material is Si_3N_4 (silicon nitride). These layers are usually deposited by CVD (Chemical Vapour Deposition) processes [4.33]. There are two major CVD processes used in the fab: LPCVD (Low Pressure CVD process) and PECVD (Plasma Enhanced CVD process). LPCVD is usually performed at temperatures between 550 and 750° C, at pressures from 0.25-2.0 torr. This process ensures better step coverage. PECVD, on the other hand, is a low temperature process. It is preferred for deposition subsequent to the first metal layer since aluminium cannot be heated to more than 450° C.

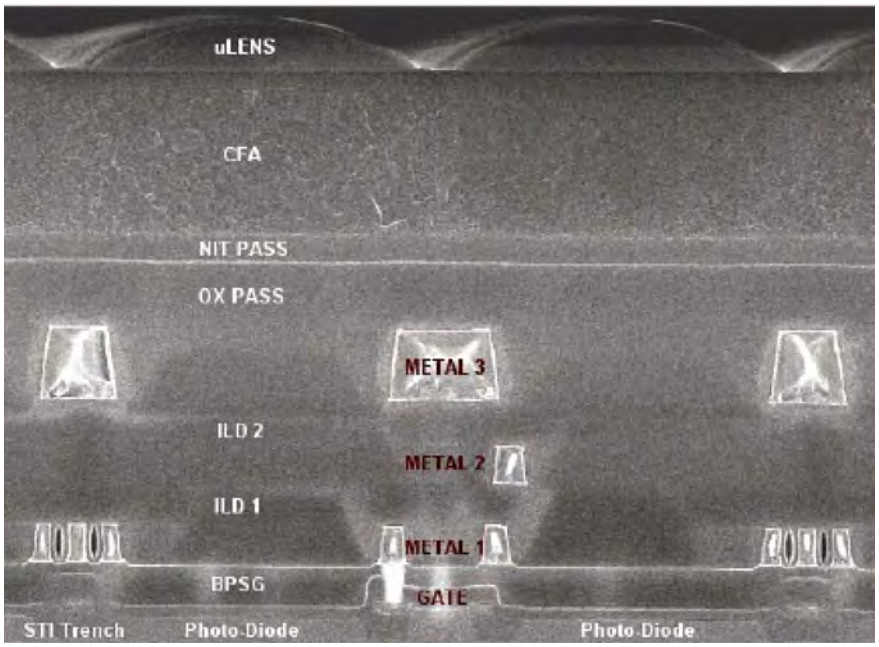

Fig. 4-20 *The cross-section of a CMOS image sensor in 0.18-μm "imaging" process from [4.32]. The micro-lens (μLENS) focuses light into the photodiode. The light passes through a color filter (CFA), a silicon nitride passivation layer (NIT PASS), an oxide passivation layer (OX PASS), inter-dielectric material layers (ILD2, ILD1), and BPSG oxide layer before reaching the photodiode. The image sensor used in the current work does not contain the micro-lens or the color filter. © 2004 EEE.*

The plasma used in the deposition is derived by applying RF fields to a low-pressure gas thereby causing gas-phase disassociation and ionization of reactant gases. This process also has a higher deposition rate that other CVD processes. The various oxides that are deposited by utilizing these two processes are listed below:

BPSG: This is a kind of silicate glass that includes additives of both boron and phosphorous. This is usually used as an insulating material between inter-metal layers in CMOS processes. Since it contains

more “impurities”, this material can be considered to be more prone to optical damage during irradiation.

TEOS: TEOS forms highly conformal films with both LPCVD and PECVD processes. In many cases, TEOS is also used as first-level dielectric. TEOS films are known to be quite porous and absorb moisture.

Si_3N_4: Silicon nitride films are used primarily for two purposes. One is as an oxidation mask, and the other is as a final passivation layer on chips. LOCOS (Local Oxidation of Silicon) occurs using silicon nitride as a mask, since diffusion of oxygen through the film is very slow. These masking layers are deposited by the LPCVD process. As a final passivation layer, silicon nitride is a very good barrier against water and sodium diffusion. It can also be deposited conformally. PECVD is used in this process.

For the experiments, the oxides (thicknesses of 1 μm) were deposited on silicon wafers. The samples were diced into squares and irradiated at the irradiation facility. Care was taken not to damage the surface of the samples.

FTIR measurements

The FTIR (Fourier Transform Infrared) transmission measurements were carried out in the wavelengths from 2.5 μm (wave number = 4000 cm^{-1}) to 25 μm (wave number = 400 cm^{-1}). The silicon bulk itself becomes “transparent” at these wavelengths, and the changes being reflected by the changes in the oxide (glass). Glass in fully transparent to IR wavelengths up to about 2.6 μm ([4.34]). In the higher wavelength region, there is also some absorption depending on the constitution of the glass, including impurities. Thus the oxide can be “probed” using this method. The FTIR measurement results for the different oxides before and after irradiation are shown from Figure 4-21 to Figure 4-26. A radiation dose of 800 Gray was used in all the cases. The BPSG (PECVD) layer, TEOS (PECVD) layer and the thermal oxide show a reduction of up to 3%, 1% and 1% respectively in the transmission spectra.

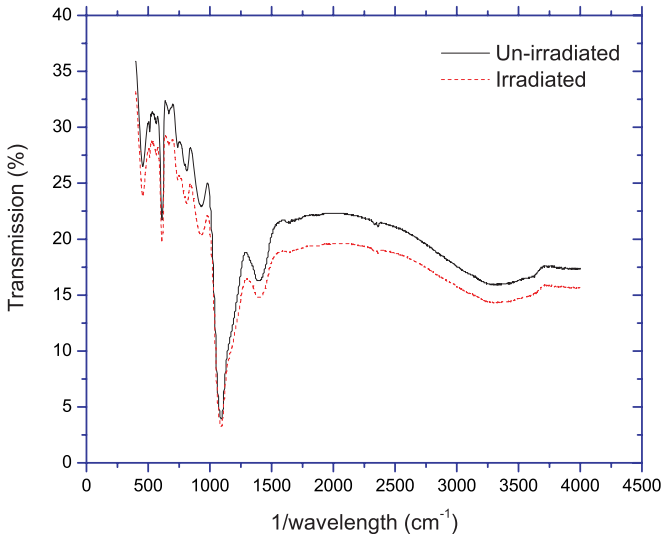

Fig. 4-21 *FTIR on BPSG layer (PECVD).*

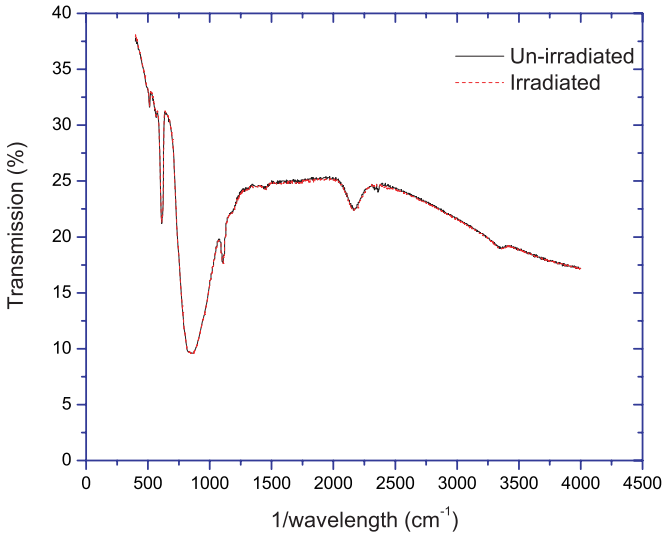

Fig. 4-22 *FTIR on Si_3N_4 layer (PECVD).*

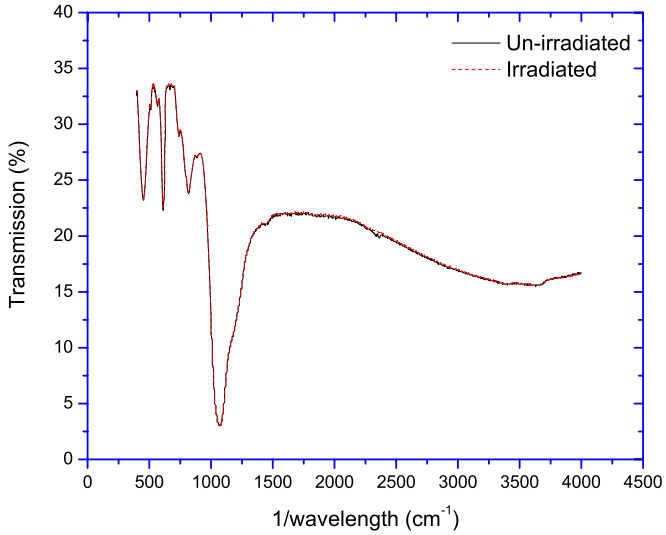

Fig. 4-23 *FTIR on SiO_2 layer (PECVD).*

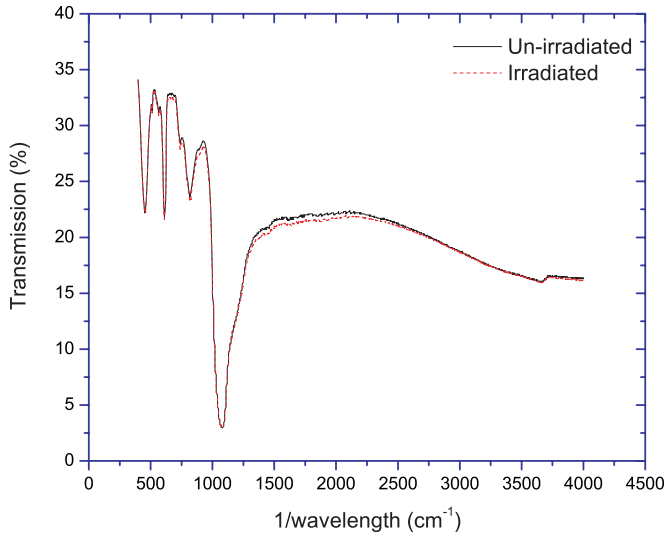

Fig. 4-24 *FTIR on TEOS layer (PECVD).*

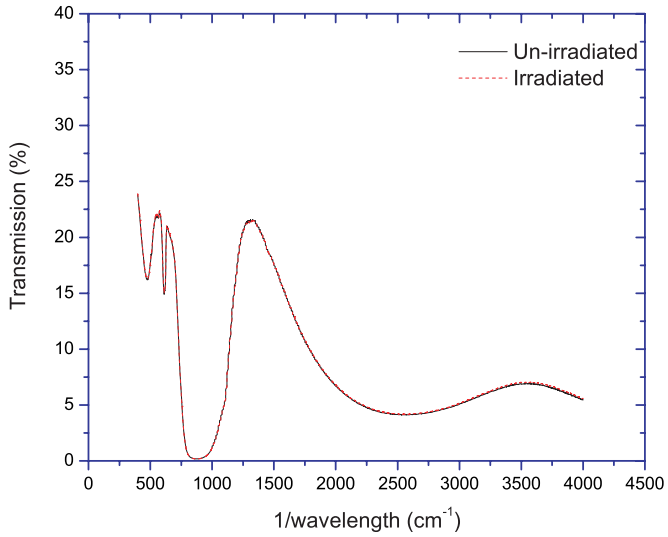

Fig. 4-25 *FTIR on Si_3N_4 layer (LPCVD).*

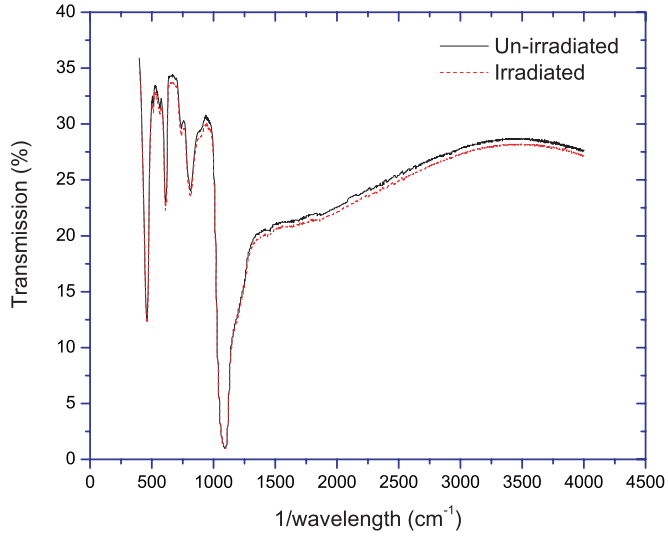

Fig. 4-26 *FTIR on SiO_2 (grown thermal oxide through wet-process).*

It is also observed that no peaks or valleys are introduced in the spectra after irradiation, though the change in the spectra is wavelength dependent. BPSG oxides contain Boron and Phosphorous as impurities that make them vulnerable to degradation. Similarly, TEOS films are quite porous and absorb moisture readily. This could be a contributing cause to their optical degradation. Silicon nitride layer processed in both the PECVD and LPCVD methods did not show any significant changes after irradiation.

The small change in the transmission seen in some of the oxides can be either due to change in the reflectance or due to color centres that may have formed due to irradiation. To study this further, ellipsometry is performed on the oxides to see whether the optical constants change after the irradiation process. So far we have conducted experiments in the IR region. A transmission measurement in the visible region is difficult because that requires a "free-standing" oxide membrane and sophisticated alignment/ measurement procedures. So ellipsometry is performed on the oxides to determine if there are changes to the optical constants after irradiation. This will be explained in the next section.

Ellipsometric measurements

Ellipsometric studies were also performed on the oxides that were subjected to FTIR measurements. This enables to see the effect of radiation in the visible spectrum, and also extract optical parameters like the refractive index (n) and the extinction coefficient (k). Figure 4-27 to Figure 4-33 show the results of the ellipsometry. Concurrent to the FTIR measurements, the BPSG layer (PECVD) and the TEOS layer (PECVD) manifest a small increase (densification) in the refractive index, Δn of ~0.002 after irradiation. The refractive index of BPSG shows the highest change in the range 300-700 nm, while for the TEOS, the change is noticed after 500 nm. The value of k obtained from ellipsometry in the wavelength used in the study was negligible, even after irradiation. This indicates that no color centres are formed due to the irradiation process in the dose range considered in this study.

In the very simple case of radiation reflection from the boundary of two optical media of refractive indexes n_1 and n_2 is given by:

$$R = \left[\frac{n_1 - n_2}{n_1 + n_2}\right]^2 \tag{4-23}$$

The total transmittance T_{total} of m identical plates placed in series is given by [4.36]:

$$T_{total} = \frac{T_0}{m - T_0(m-1)} \tag{4-24}$$

and the radiation transmitted directly, T_{dir} is given by:

$$T_{dir} = (1-R)^{2m} \tag{4-25}$$

Thus from the above equations, we can see that a change in the refractive index will cause a change in the reflectance pattern of the spectra. Further, for a stack of optical layers, the effect of changes in the refractive indices on the transmission is multiplicative.

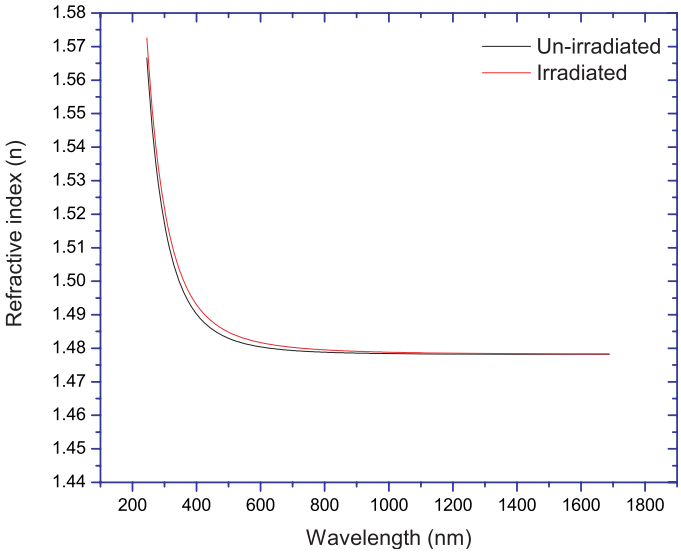

Fig. 4-27 *Ellipsometry on BPSG layer (PECVD).*

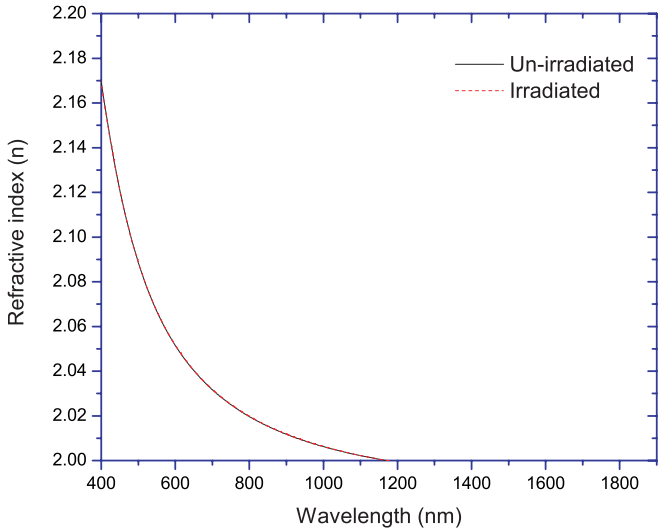

Fig. 4-28 *Ellipsometry on Si_3N_4 layer (PECVD).*

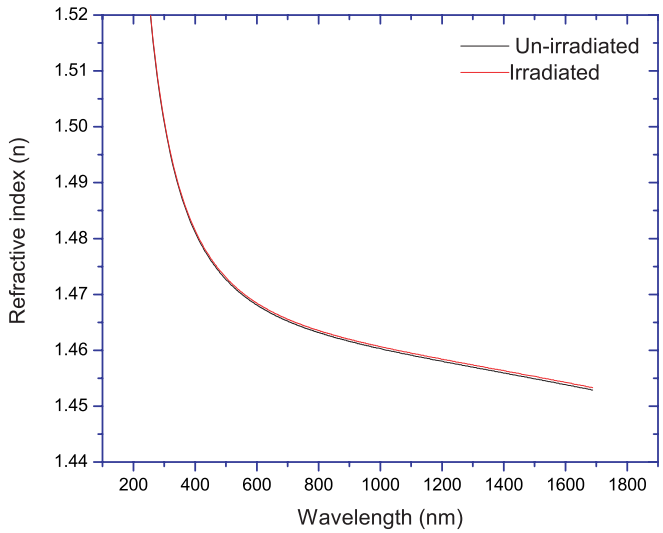

Fig. 4-29 *Ellipsometry on $Si0_2$ layer (PECVD).*

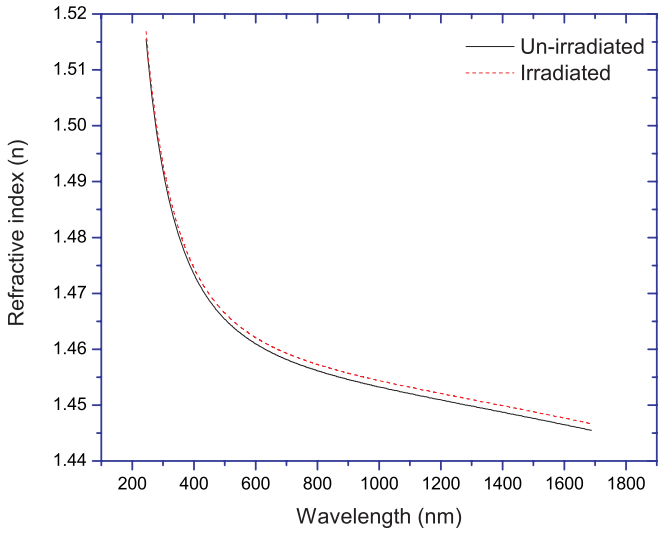

Fig. 4-30 *Ellipsometry on TEOS layer (PECVD).*

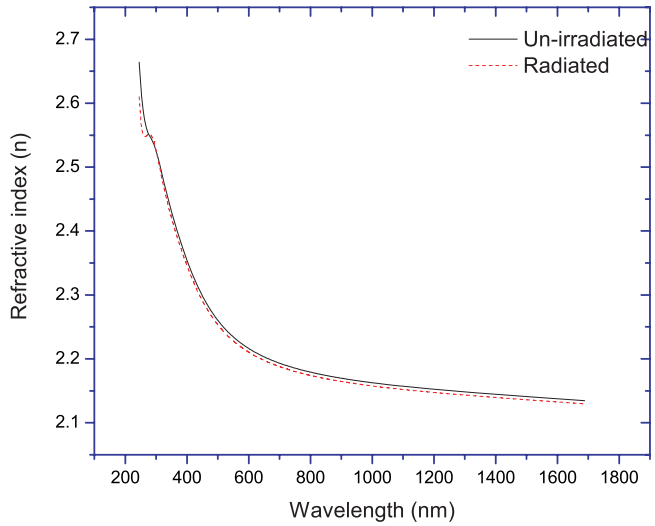

Fig. 4-31 *Ellipsometry on Si_3N_4 layer (LPCVD).*

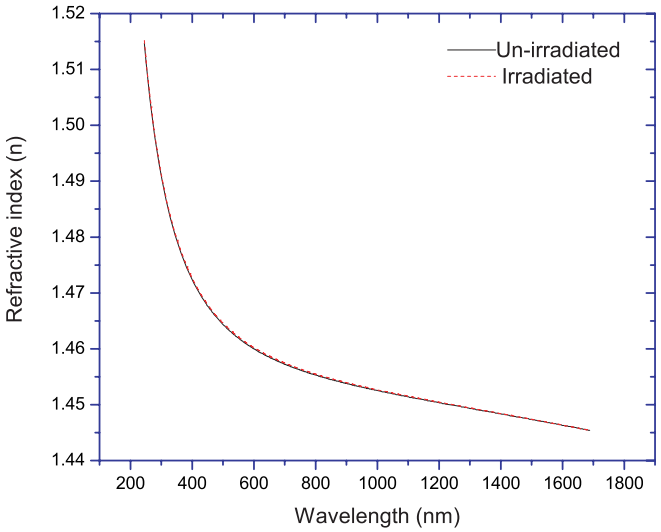

Fig. 4-32 *Ellipsometry on $Si0_2$ layer (thermal oxide via wet-process).*

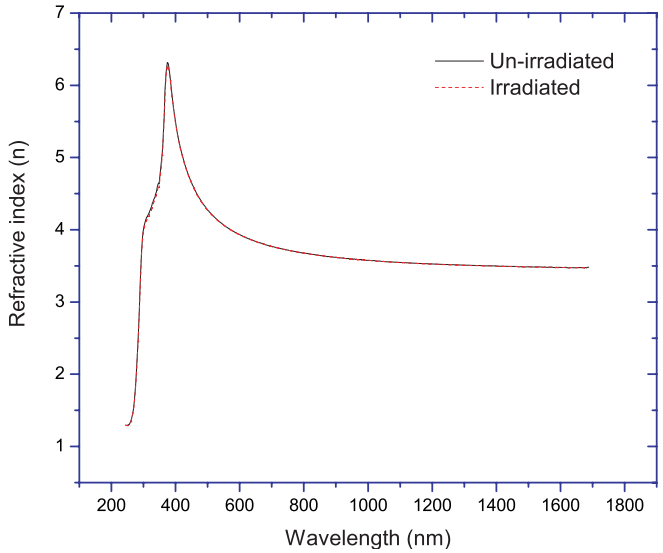

Fig. 4-33 *Ellipsometry on the silicon bulk.*

Oxide type	Surface roughness (A°) Un-irradiated	Surface roughness (A°) Irradiated
BPSG (PECVD)	34	54
Si_3N_4 (PECVD)	47	63
SiO_2 (PECVD)	41	34
Si_3N_4 (LPCVD)	44	71
SiO_2 (LPCVD)	71	65
TEOS (PECVD)	44	59

Table 4-2. *Surface roughness profile of oxides before and after irradiation.*

Surface profilometry

The data obtained through surface profilometry of the oxides is shown in Table 4-2. A dedicated surface profilometer was used for the experiment. The results indicate that no “pits” or roughness was introduced in the surface after irradiation in the dose range concerned. All the values are within the noise range.

4.3.2.3 General discussion on radiation-induced optical effects

From the experiments and the fit through the model (Section 4.3.2.1), it can be understood that the Si/SiO_2 interface degrades after irradiation. The FTIR measurements on the oxides reveal that there is a very small decrease in the transmission spectra of certain oxides like BPSG and TEOS. This is most probably due to the small change in the refractive index of these oxides after irradiation. Further, no peaks or valleys were introduced in the spectral response of the oxides after the irradiation process. Likewise, there was no indication of the introduction of color centres by the irradiation process. No physical modification of the oxide surface was noticed. Thus it is safe to conclude that the post irradiated change in the QE of the 4-T sensor is mainly due to the change in the surface recombination velocity (SRV). The change in the SRV also modulates the interference pattern as mentioned in Section 4.3.2.1. This results in a further change in the average value of the sensor response.

Figure 4-34 shows the simulated QE (normalized) utilizing the refractive indices of un-irradiated and irradiated TEOS shown in Figure 4-30. A single layer of TEOS (thickness = 3.5 μm) above a silicon substrate is assumed for this simulation. The wavelength step was chosen to be 40 nm. The resulting transmission spectra are multiplied by the corresponding internal QE spectra, simulated for two values of surface recombination velocities: 1.3×10^5 cm/s and 6.8×10^5 cm/s, extracted from the experiments (Figure 4-19). To evaluate the effect of change in the refractive indices on the QE, the unmodified transmission spectra is operated on the internal QE response corresponding to modified SRV of 6.8×10^5 cm/s. A 3rd order poly-fit is also shown for all the spectra.

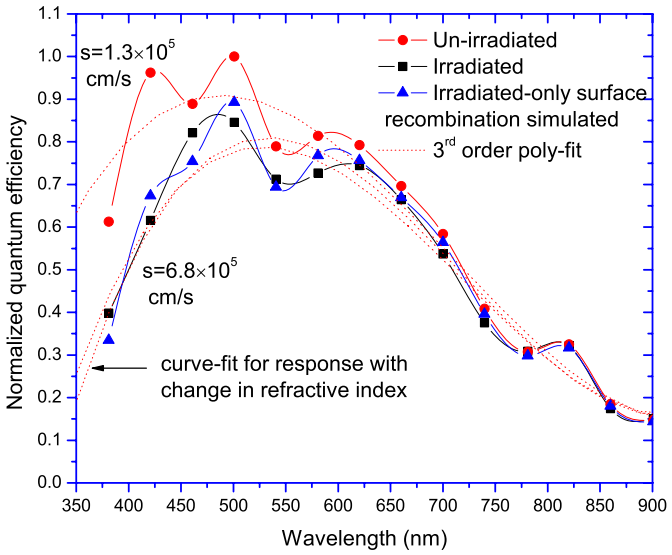

Fig. 4-34 *Simulated QE (normalized) using the ellipsometric data for TEOS before and after irradiation. An oxide thickness of 3.5 μm is assumed in the simulation.*

It can be seen that, similar to the experimental curves shown in Figure 4-19, there is a diminished optical response for a higher SRV value. Further, the change in the refractive index contributes to small shifts and changes to the the peaks, but there is negligible change in the mean value. Thus it can be concluded that the major degradation mechanism in the optical response due to irradiation (in the dose range concerned in this study) is due to a change in the SRV.

Two more predictions can be made from the discussion so far on the optical degradation:

- Sensors that have very small interface defects and are already very sensitive—especially to blue and green photons —will degrade more due to irradiation compared to the less sensitive sensors. This follows the discussions in Chapter 3,

(Section 3.2.1) on the effect of SRV on the internal QE. At high values of SRV, the spectral curves tend to saturate, leading to less noticeable differences.

- The effects of radiation damage on the spectral characteristics will be more noticeable in ultra-shallow junction diode types such as the pinned photodiode, which has a higher response to the blue and green photons. In photodiodes with deeper junctions, the effect of the change in SRV will be less noticeable.

4.4 Chapter summary

In this chapter, effects of γ-ray irradiation on CMOS image sensors fabricated in 0.18-μm CMOS process were studied. Some interesting results were observed during this venture. On the positive side, it was found that the very thin oxides employed in advanced CMOS processes offer an inherent radiation tolerance to sensors fabricated in this technology. The flatband/threshold shift due to charge trapping in the oxides and thus the change in the conversion gain of in-pixel transistors was found to be negligible. The FGDs reveal an increased leakage current after irradiation. It was found that the surface leakage evolution was very small, but the bulk component degraded fast especially above 400 Gray. In the FGD structures, there exists a very small region where the depletion under the gate interacts with the STI at the device periphery. Thus, the STI leakage component is coupled with I_{fij} and cannot be separated with the current FGD structures. The results from the imagers offer more clue to the observations.

By utilizing techniques like p-well passivation and optimizing the value of NTA, dark signal evolution in the imagers were found to be effectively mitigated. This also strongly hints to the fact that displacement damages due to γ-ray irradiation should be negligible. Thus, it is concluded that the STIs are primarily responsible for leakage current increase due to irradiation in the imagers as well as the FGDs.

It was found that an increased dark current generation due to the presence of high electric fields can hamper high-quality imaging in radiation-harsh environments. Radiation induced traps are found to be sensitive to such local electric fields. With the shrinking of geometry, attention should be given to such field effects when utilizing such sensors for medical/outer-space applications.

From the results, lifetime variations in the silicon bulk are predicted to be minimal. This indicates that the spectral response variations due to ionizing radiations will be negligible.

The surface recombination velocity at the Si/SiO_2 interface in the photodiode region is seen to increase after irradiation. This affects the spectral response of the sensor and results in a reduction in the internal QE. The peaks and valleys of the interference pattern produced by the optical stack above the photodiode are also modulated by the change in the internal QE. This results in a modified external QE which manifests as a decreases in the overall sensor response.

Finally, some of the oxides that form on top of the sensor are also found to be affected by irradiation. The major material change due to irradiation in the dose range concerned is a change in the refractive index (densification). Materials like BPSG and TEOS are found to succumb to this degradation. However, the change is very small and does not contribute to drastic changes to the response, and can be neglected. Further, there was no indication of the formation of color centres in the oxides.

The designer usually does not have control over the oxide properties or its physical parameters while designing the sensor. With the evolution of aggressive technologies, the number of metal layers will increase and thus affect the thickness and the choice of material used in the stack by the fabs. Hopefully, fabrication processes aimed for imaging solutions would take into consideration the effects mentioned above as well, to improve the quality of imaging in future technologies. In summarizing, it can be safely concluded that deep-submicron process are the choice of technology when it comes to radiation tolerant designs, if measures are taken in the direction presented in the work.

4.5 References

[4.1] J. R. Srour, and J. M. McGarrity, “Radiation Effects on Microelectronic in Space”, Proc. IEEE, Vol. 76, No. 11, pp. 1443-1469, 1988.

[4.2] L. Rossi, P. Fischer, T. Rohe, and N. Wermes, “Pixel Detectors: From Fundamentals to Applications”, Springer Science & Business, pp. 32-34, 2006.

[4.3] T. P. Ma, and P. V. Dressendorfer, “Ionizing Radiation Effects in MOS Devices and Circuits”, Wiley-IEEE, pp. 162, 147, 171-173, 1989.

[4.4] C. Claeys and E. Simon, “Radiation Effects in Advanced Semiconductor Materials and Devices”, Springer Series in Material Science, pp. 1-5, 2002.

[4.5] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, “Total Dose and Displacement Damage Effects in a Radiation-Hardened CMOS APS”, IEEE Trans. Elec. Dev., Vol. 50, No. 1, pp. 84-90, 2003.

[4.6] P. R. Rao, X. Wang, and A. J. P. Theuwissen, “Degradation of CMOS Image Sensor in Deep-submicron Technology due to γ–irradiation”, Sol. St. Elec., Vol. 52, No. 9, pp. 1407-1413, 2008.

[4.7] G. Anelli, “Design and Characterization of Radiation Tolerant Integrated Circuits in Deep submicron CMOS Technologies for the LHC Experiments”, PhD Thesis, Institut National Polytechnique De Grenoble, pp. 35-62, 2000.

[4.8] R. L. Pease, A. H. Johnston, and J. L. Azarewicz, “Radiation Testing of Semiconductor Devices for Space Electronics”, Proc. IEEE, Vol. 76, No. 11, pp. 1510-1526, 1988.

[4.9] R. C. Hughes, “Time-resolved Hole Transport in a-SiO_2” Phys. Rev. B, Vol. 15, No. 4, pp. 2012-2020, 1977.

[4.10] R. K. Chauhan, and P. Chakrabarti, “Effect of Ionization Radiation on MOS Capacitors”, Micr. Electr. Jour., Vol. 33, No. 3, pp. 197-203, 2002.

[4.11] P. J. McWhorter, S. L. Miller, and W. M. Miller, “Modelling the Anneal of Radiation-induced Trapped Holes in a Varying Thermal Environment”, IEEE Trans. Nucl. Sc., Vol 6, No. 37, pp. 1682-1689, 1990.

[4.12] E. H. Snow, A. S. Grove, and D. J. Fitzgerald, “Effects of Ionization Radiation on Oxidised Silicon Surfaces and Planar Devices”, Proc. IEEE., Vol. 55, No. 7, pp. 1168-1185, 1967.

[4.13] P. S. Winokur, H. E. Boesch, Jr., J. M. McGarrity and F. B. McLean, “Two-stage Process for Buildup of Radiation-induced Interface States”, J. App. Phys., Vol. 50, No. 5, pp. 3492-3494, 1979.

[4.14] D. L. Griscom, “Hydrogen Model for Radiation-induced Interface States in SiO_2-on-Si Structures: A Review of the Evidence”, J. Elec. Mat., Vol. 21, No. 7, pp. 763-767, 1992, and the references therein.

[4.15] M. R. Shaneyfelt et al., “Interface-trap Building Rates in Wet and Dry Oxides”, IEEE Trans. Nucl. Sc., Vol. 39, No. 6, pp. 2244-2251, 1992.

[4.16] R. H. White, and G. R. Wirtenson, “Radiation Induced Darkening of the Optical Elements in the Startracker Camera”, Lawrence Livermore National Laboratory Report, University of California, pp. 1-6, 1993.

[4.17] D. K. Schroder, “Semiconductor Material and Device Characterization”, Wiely-Interscience publication, pp. 244-263, 411-420, 1990.

[4.18] J. P. Colinge, and C. A. Colinge, “Physics of Semiconductor Devices”, Springer, pp.80-90, 2006.

[4.19] J. R. Srour, and D. H. Lo, “Universal Damage Factor for Radiation-induced Dark Current in Silicon Devices”, IEEE. Trans. Nuc. Sci., Vol. 47, No. 6, pp. 2451-2459, 2000.

[4.20] B. Brichard, O. V. Butov, K. M. Golant, and A. F. Fernandez, “Gamma Radiation-induced Refractive Index Change in Ge- and N-doped Silica”, J. App. Phys., Vol. 103, No. 5, pp. 054905-1-4, 2008.

[4.21] R. E. Schenker, and W. G. Oldham, “Ultraviolet-induced Densification in Fused Silica”, J. App. Phys. Vol. 82, No. 3, pp. 1065-1071, 1997.

[4.22] Xian-Ti Meng et al., “Effects of Electron and Gamma-ray Irradiation on CMOS Analog Image Sensors”, Microelectron. Reliab., Vol. 43, No. 7, pp. 1151-1155, 2003.

[4.23] .H. Ohyama et al., “Defect Assessment of Irradiated STI Diodes”, Nuc. Inst. Meth. B, Vol. 186, No. 1, pp. 424-428, 2002.
[4.24] C. R. Moon et al., “Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors”, IEEE Elec. Dev. Lett., Vol. 28, No. 2, pp. 114-116, 2007.
[4.25] H. I. Kwon et al., “The Analysis of Dark Signals in the CMOS APS Imagers from the Characterization of Test Structures”, IEEE Trans. Elec. Dev., Vol. 51, No. 2, pp. 178-184, 2004.
[4.26] L. S. Riley, S. Hall and J. Schitz, “Evaluation of Surface Generation Velocity of Sidewall Oxide Interfaces Formed by Dry Etching for Shallow Trench Isolation”, Sol. St. Elec., Vol. 44, No. 11, pp. 2093-2095, 2000.
[4.27] A. Poyai et al., “Lifetime Study in Advanced Isolation Techniques”, Mat. Sci. Semi. Proc., Vol. 4, No. 1-3, pp. 137-139, 2001.
[4.28] J. Bogaerts, “Radiation-Induced Degradation Effects in CMOS Active Pixel Sensors and Design of a Radiation Tolerant Image Sensor”, PhD thesis, pp. 5-15, 37-95, Katholieke Univ. Leuven, 2002.
[4.29] G. R. Hopkinson, “Radiation Effects in a CMOS Active Pixel Sensor”, IEEE Trans. Nucl. Sci., Vol. 47, No. 6, pp. 2480-2484, 2000.
[4.30] X. Wang, P. R. Rao, and A. J. P. Theuwissen, “Fixed-Pattern Noise Induced by Transmission Gate in Pinned 4T CMOS Image Sensor Pixels”, Proc. ESSDERC, pp. 331-334, 2006.
[4.31] J. R. Srour, and R. A. Hartmann, “Enhanced Displacement Damage Effectiveness in Irradiated Silicon Devices”, IEEE Trans. Nuc. Sci., Vol. 36, No. 6, pp. 1825-1830, 1989.
[4.32] H. Rhodes et al., “CMOS Imager Technology Shrinks and Image Performance”, WMED, pp. 7-18, 2004.
[4.33] H. Veendrick, “Deep-submicron CMOS ICs”, Kluwer Publications, pp. 95-100, 1998.
[4.34] W. Clark, “Photography by Infrared”, Read Books, pp. 411, 2007.

[4.35] K. Arshak, and O. Korostynska, “Gamma Radiation-induced Changes in the Electrical and Optical Properties of Tellurium Dioxide Thin Films”, IEEE Sens. J., Vol. 3, No. 6, pp. 717-721, 2003.
[4.36] Optical Society of America, “Handbook of Optics”, McGraw-Hill Publication, pp. 8-42-8-45, 1978.

CCD in standard CMOS technology — A study

5

A *CCD* (Charge-Coupled Device) is a series connection of capacitors. In simple terms, it is a charge collection, storage and transport device aimed at imaging [5.1]. Each of these capacitors can also be regarded as a photogate. The incoming photons fall on the photogate to produce electron-hole pairs in the silicon bulk. The charges are then collected by potential "pockets" formed by pulsing each of these photogates to deep depletion. Since the charges are confined within each pocket, each of these capacitors can be viewed as individual pixels. The charge transportation occurs by manipulating the potential pocket digitally, so that the charges "flow" from one pixel to another. This continues until the charges are dumped into an output node which converts the charge packets into a corresponding voltage to be read-out. Several charge transportation schemes can be utilized for moving the charges through the CCD, the popular ones being the four-phase and two-phase systems [5.1], [5.2].

CCDs are fabricated in specialized foundries which allow the fabrication of overlapping polysilicon gates and override many constrains imposed by CMOS fabs. While CCD image sensors benefit through high dynamic range, quantum efficiency and noise performance, CMOS image sensors benefit through integration of

electronics, and random access capabilities [5.3]. With these in mind, it would be worthwhile to investigate the possibility of integrating a CCD in the CMOS technology [5.4]. Current deep-submicron technologies allow the fabrication of polysilicon gates very close to each other (~0.24 μm). This study investigates whether this ability could be used to allow surface potentials to overlap between adjacent polysilicon gates and achieve a CCD like structure in standard CMOS technology. The advantages and applications of such an endeavour will be clarified further in this thesis.

5.1 Background

CCDs have conventionally used overlapping (0.5-2.5 μm) polysilicon gates to achieve smooth charge transfer between photogates with a very high CTE (Charge Transfer Efficiency) [5.1]. The advantages of hybridizing a CCD structure with CMOS are:

- At the pixel level, clever strategies like charge addition, sub-pixel resolution, etc are possible.
- At the sensor level, easier integration with electronics and readout circuitry, lower power supply requirements and power consumption.
- At the consumer level, potential lower price, mass production capability and the ability to develop application specific CCD structures.

To verify the feasibility, device simulations were carried out using the software SPECTRA®. This is presented in Section 5.2. Subsequent to the feasibility study, test structures were fabricated in the TSMC 0.18-μm process based on the results obtained through the simulation study. The layout and fabrication details are presented in Section 5.3. The experimental results are discussed in Section 5.4.

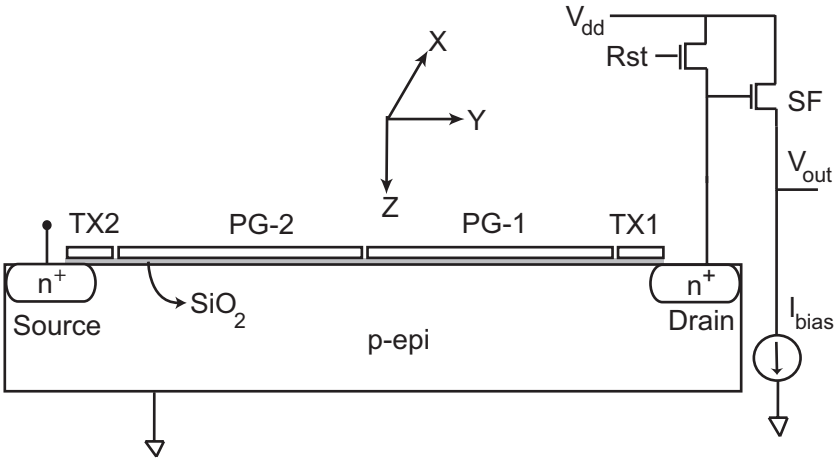

Fig. 5-1 *The simplest form of the intended structure. It consists of at least two photogates (PG-2, PG-1), a transfer gate (TX1), the drain, the reset transistor (Rst) and a source follower (SF). Transfer gate (TX2) and the source are formed as part of the fabrication process. It can be used to test the pixel through charge injection.*

5.2 Simulation and modelling

The simplest form of the intended structure is shown in Figure 5-1. It contains two polysilicon photogates (PG-1 and PG-2) separated by a very small gap. The transfer gate (TX1) is used to transfer charges collected from the photogates into the floating diffusion node (FD). The FD node is also the drain region of the structure.

The reset transistor (Rst) is used to reset the FD node, and the voltage is read-out through a source follower (SF). These two form the basic circuitry in the sensor. A bias current (I_{bias}) is used to bias the SF and is provided off-chip in this study. Additionally, a transfer gate (TX2) formed in the source region is used to “inject” charges under the photogates for electronically characterizing the sensor without the necessity for a light source. The simulations only include PG-2, PG-1, TX1 and the FD node. The length of PG-2 as well as

PG-1 was chosen to be 6 μm for the simulations. The length of TX1 is 1 μm. The fabricated test structures discussed later have up to 5 photogates based on the layout scheme shown in Figure 5-1. The photogate area is kept constant in all cases: this requires the tailoring of the photogate lengths accordingly.

Charge transfer between two gates of a CCD is through the movement of charge carriers along the surface of the CCD. The three driving forces behind charge transfer are [5.1]:

- The thermal diffusion of charge carriers by redistributing its local gradient towards an equilibrium state.
- Self-induced fields that result from the repulsion of carriers of the same type.
- Fringing-fields where the existence of electric fields due to voltage on gates helps drive charges from one location to another. This effect is gate-geometry dependent.

Whereas the first two mechanisms are “slow” and help in the transfer of charges initially, for a near-complete charge transfer to occur fringing-fields are necessary. Thus this effect is detailed in the next section.

5.2.1 Fringing fields

The forcing of transport by electric fields due to voltages on the gates enables high transport efficiency coupled with speed of operation. The surface potential is determined not only by the applied gate voltage, but also by its neighbouring gates. If the surface potentials were “flat” beneath a gate, there would not be any fringing fields. However, in reality, the fields have a certain gradient and this allows the surface potentials under two gates separated by a small gap to “overlap”. The fringing fields are a function of the oxide thickness, substrate doping and geometry [5.1], [5.5].

The relationship between gate voltage and surface potential in deep-depletion is given in Chapter 2; (2-19), (2-20).

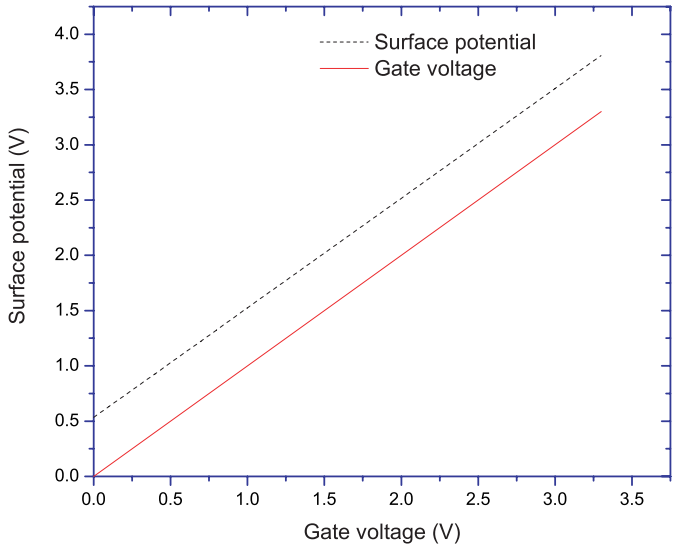

Fig. 5-2 *The surface potential under a gate in deep-depletion for a thin gate-oxide.*

When there are no trapped charges in the oxide or in the interface, the flatband voltage is the work function difference between the gate and the semiconductor. For the highly doped n^+ polysilicon gate used in CMOS technology, the flatband voltage without any charge trapping is -0.55 V. Figure 5-2 shows the surface potential as a function of the gate voltage computed using the gate voltage/surface potential relationship. For the thin gate-oxide value used in this simulation (~4 nm), the relationship between the gate voltage and surface potential is almost linear. We can see from the graph that when the gate voltage is 0 V, the surface potential is ~ 0.52. Likewise, when the gate voltage is 3.0 V, the surface potential is ~ 3.52 V. The gate-oxide thickness as well as the presence of fixed charges in the silicon-dioxide region can influence the surface potential.

Conventional CCDs have typically used overlapping polysilicon gates to achieve high charge transfer efficiencies. However, standard CMOS technologies usually employ single-poly process.

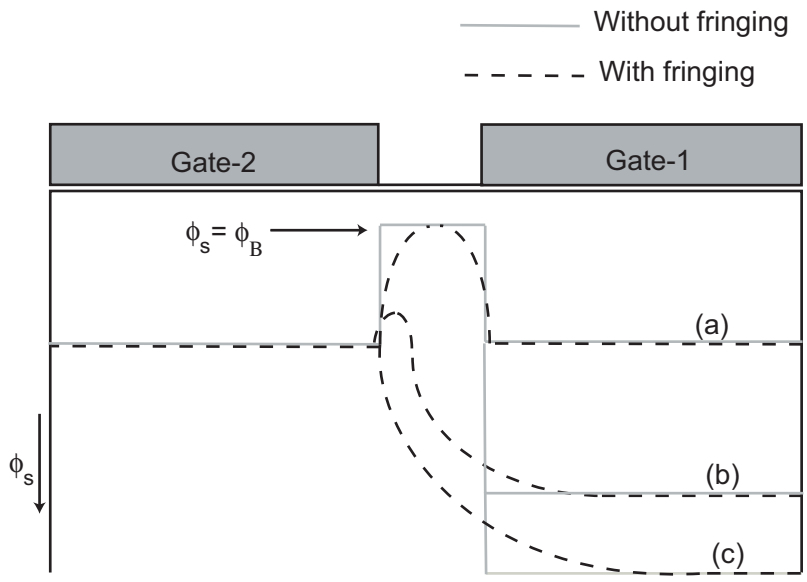

Fig. 5-3 *The conceptual diagram of the surface potential under two gates separated by a small gap. The thick line shows a step-response while the dotted lines show modified surface potential due to fringing fields.*

Overlapping of polysilicon layers is generally not allowed. This stringent requirement is a hindrance to fabricate a CCD in a standard CMOS process. But the merit of modern 0.18-μm CMOS process is the ability to have feature sizes as small as 0.18 μm. When two gates are placed close to each other, with a very small gap in between, the surface potentials overlap. This ability was in fact recognized early on, but the technology was not yet mature enough for a practical device to be fabricated. Some early efforts in this direction can be seen in the work of [5.7]. Figure 5-3, which is a conceptual diagram, further explains the idea. It shows two gates, Gate-2 and Gate-1, placed close to each other. The surface potential ϕ_s is indicated positively down. With no fringing fields, the surface potentials form a "step" curve. Condition (a) represents the situation where equal voltages are applied to the gates. In this situation, if the gap is

sufficiently large, the potential in that region steeps back towards the bulk potential of the semiconductor referred to as ϕ_B. This forms a potential "pocket", inhibiting the smooth transfer of charges between the two gates. If the gap size is reduced, the height of this barrier will also reduce. With fringing fields, the transition in the gap will be smoother as indicated with the dotted line. In condition (b), the gate voltage on Gate-1 is increased to a more positive value. As represented in the figure, a small pocket is still present, which could defer the efficient charge transfer. On further increasing the voltage as represented in condition (c), a very smooth curve can be noticed enabling efficient charge transfer. Thus, the key for efficient charge transfer depends on the gap-size for the voltage range that is planned to be used on the gates. Though there can be a study undertaken towards optimizing the substrate doping, this effort will not be useful in a situation where "standardised" CMOS processes are used.

Figure 5-4 shows the simulation result whereby the gap between PG-2 and PG-1 is varied between 0.8 μm and 0.28 μm, on a substrate doping of $N_A = 1\times10^{15}cm^{-3}$. PG-1 is biased at 3.0 V and PG-2 at 0 V. The surface potential is represented in the Y-axis (positively downwards).

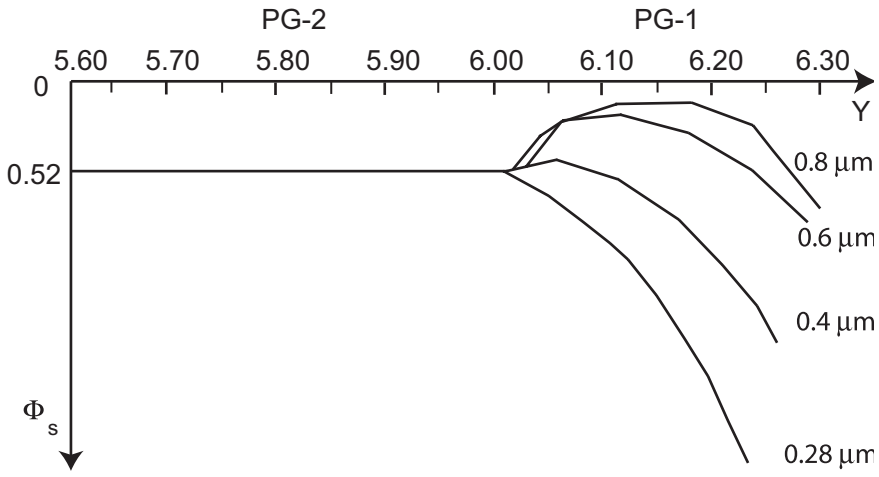

Fig. 5-4 *Surface potential (along Y axis) for different gap sizes. Surface potential under PG-1 is not shown for clarity.*

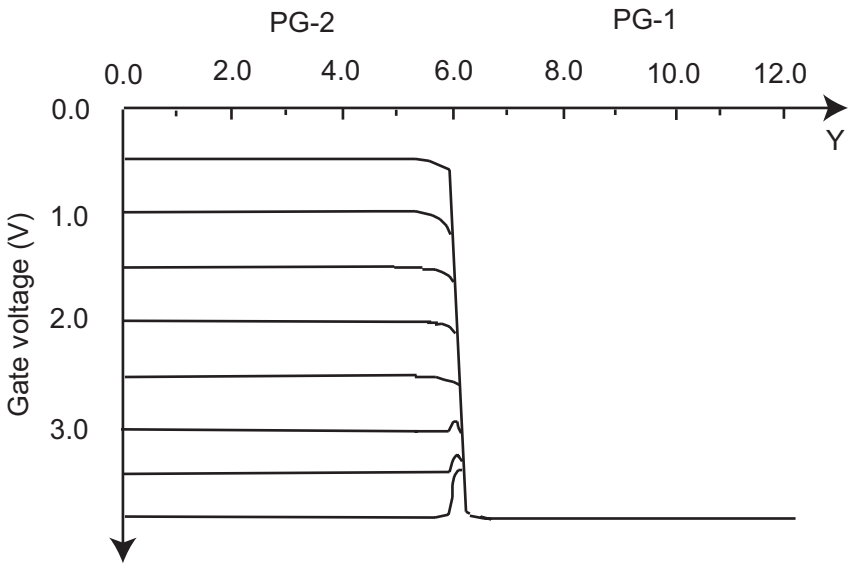

Fig. 5-5 *Surface potential as a function of gate voltage. PG-2 is swept from 0 to 3V keeping PG-1 at 3 V.*

It can be immediately seen that as the gap is increased, the potential bump increases as well. Thus, the smaller the gap-size that can be fabricated, the better. As mentioned earlier, current CMOS technologies such as the 0.18-μm technology can be used to fabricate gap sizes as small as 0.24 μm, which will ensure a monotonous potential formation. Figure 5-5 shows the surface potential simulation wherein PG-1 is kept at 3.0 V and PG-2 is biased from 0 V to 3 V. When both the gates are at equal potentials, a potential pocket can be seen. In fact, this need not be a disadvantage since this allows the two photogates to perform charge integration simultaneously and without the problem of charge mixing. Thus clever schemes like charge addition (for high-dynamic range applications) or sub-pixel resolution within the same pixel becomes a reality. In the latter case, the higher resolution comes with the price of slower device performance and memory requirements due to the multiple read-outs required and information storage.

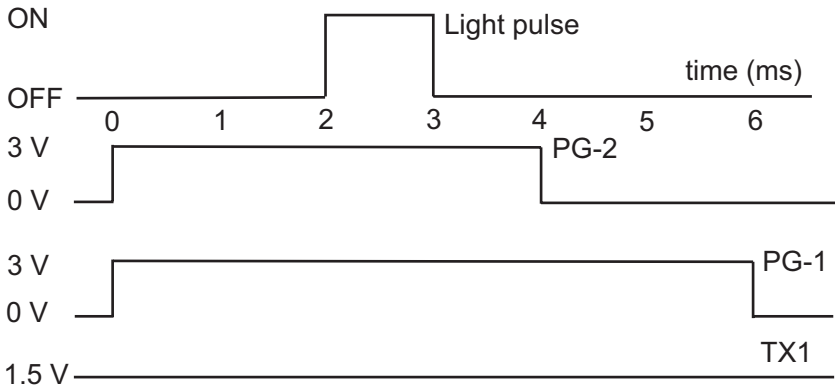

Fig. 5-6 *Timing scheme used for the device simulation.*

5.2.2 Simulation of the device

The timing diagram for operating the device is shown in Figure 5-6. The source region as well as the transfer gate TX2 is assumed to be isolated in this simulation. These are used in the test devices for injecting electrons under the photogates. This helps enable the study of linearity and light leakage tests to be explained later. To apply the initial conditions, a reset potential of 3.0 V is chosen on the floating diffusion node. To apply this condition, the "n-fermi" (quasi-Fermi level of electron) parameter in the simulation environment is chosen. This "fixes" the electron Fermi potential in the FD node, and thus would allow a time varying analysis to be carried out [5.9].

The cycle starts at t = 0 ms, where PG-2 and PG-1 start their integration process. The integration is carried out by switching the photogates to a high potential of 3 V. The surface potentials under the gates would be held at ~ 3.5 V in this condition. A rectangular light pulse (1 mW/ cm^2, E_{ph} = 2.25 eV) with a dimension 0.5 × 3.5 μm^2, is simulated to be incident on the photogates at t = 2 ms for 1 ms. Since the light pulse "ON" condition occurs during the time when both the gates are integrating, equal amounts of photo charges will be collected by each of the photogates. In the simulation, optical effects including reflection are not considered.

During the integration cycle, TX1 is held at a potential of 1.5 V. This isolates the photogates from the floating diffusion node during the integration process. The 2-D electron concentration plot at the end of the integration period is shown in Figure 5-7 (a). The electrons are filled up in the potential "bucket" formed in the substrate as can be seen from the 2-D plot. The concentration amounts to $\sim 3 \times 10^{16}$ electrons/cm^3 as is evident from the 1-D plot (along Y axis) shown in Figure 5-7 (b). The surface potential at this stage is shown in Figure 5-7 (c). As explained earlier, since the gates are held at the same potential, a potential barrier is formed in the gap which isolates the two charge "pockets" and prevents the charges from "mixing".

Subsequently, PG-2 switches to 0 V at 4 ms, thus transferring the charges underneath it to PG-1. The gate voltage switching is not instantaneous but takes some ns to reach 0 V. The condition at the instance of switching is shown in Figure 5-8. The charge pocket under PG-2 has not been completely emptied as can be seen from Figure 5-8 (a). Approximately 99.8% of charges have been transferred as can be seen from Figure 5-8 (b). The surface potential under PG-2 decreases as the gate voltage is reduced (Figure 5-8 (c)).

At 5 ms (Figure 5-9), however, we see that all the charges have been completely transferred from PG-2 to PG-1. The charge "pocket" under PG-2 disappears (Figure 5-9 (a)). In reality, almost all of the charges are transferred within several ns after the switching is complete. This can be simulated using the program with very small time-steps, but will result in a very large computation time. The electron concentration increases under PG-1 (Figure 5-9 (b)) and the surface potential under PG-2 reaches 0.52 V (Figure 5-9 (c)) consistent with a gate voltage of 0 V.

At t = 6 ms, PG-1 switches to 0 V, thereby transferring all the charges underneath it into the FD node. The condition at t = 7 ms is shown in Figure 5-10. The charge "pocket" under PG-1 disappears (Figure 5-10 (a)), and the electron concentration reduces to zero (Figure 5-10 (b)). The surface potential under both the gates are now around 0.52 V (Figure 5-10 (c)). Since the transfer gate has been biased at a constant potential of 1.5 V, electrons flow smoothly from PG-1 to the FD node. It can be noticed that the electron quasi-Fermi level at this stage decreases from the initial value of 3.0 V to 2.76 V.

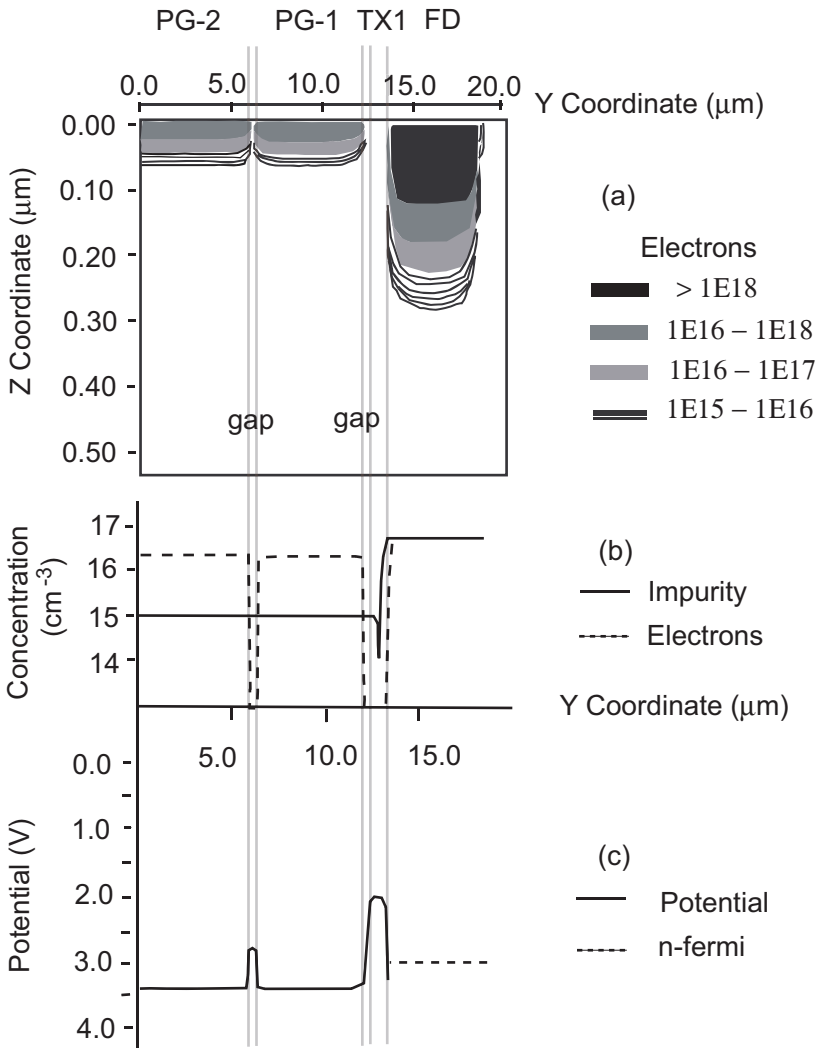

Fig. 5-7 *(a) YZ plot of electron concentration at the end of the integration time (t = 3 ms). (b) Electron and impurity concentration along Y axis (t = 3ms). (c) Surface potential plot (along Y axis) (t = 3 ms).*

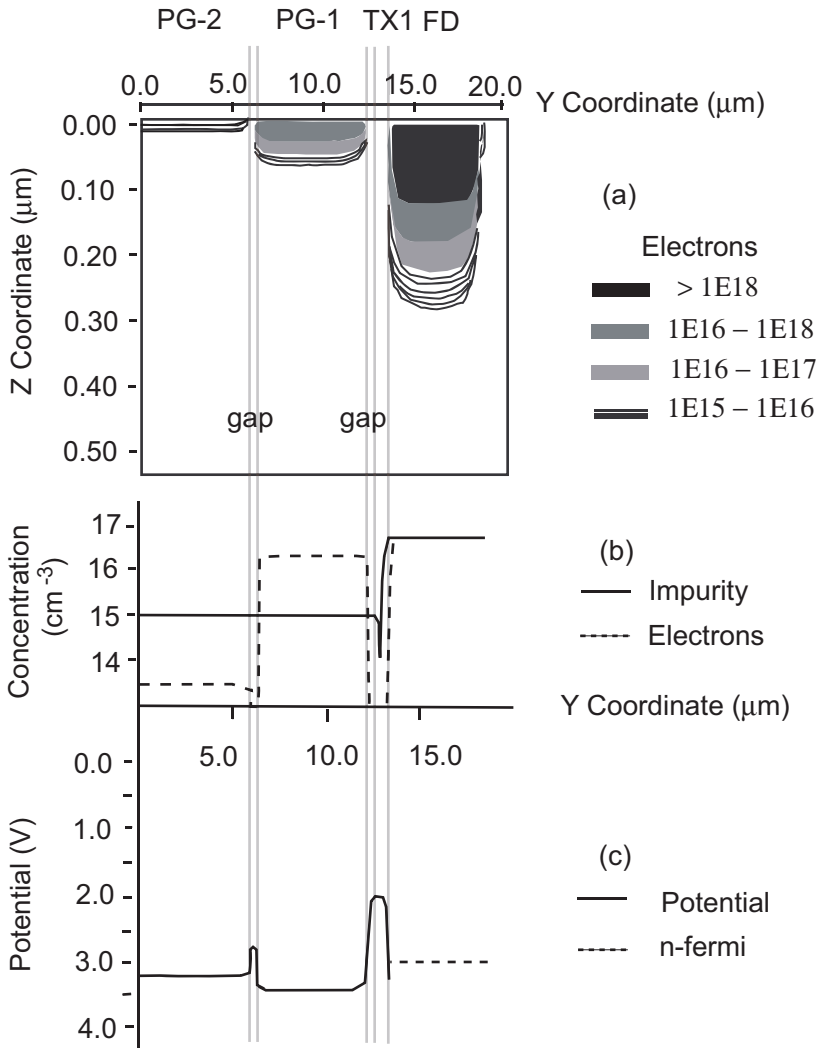

Fig. 5-8 *(a) YZ plot of electron concentration at the first transfer instance (t = 4 ms). (b) Electron and impurity concentration along Y axis (t = 4 ms). (c) Surface potential plot (along Y axis) (t = 4 ms).*

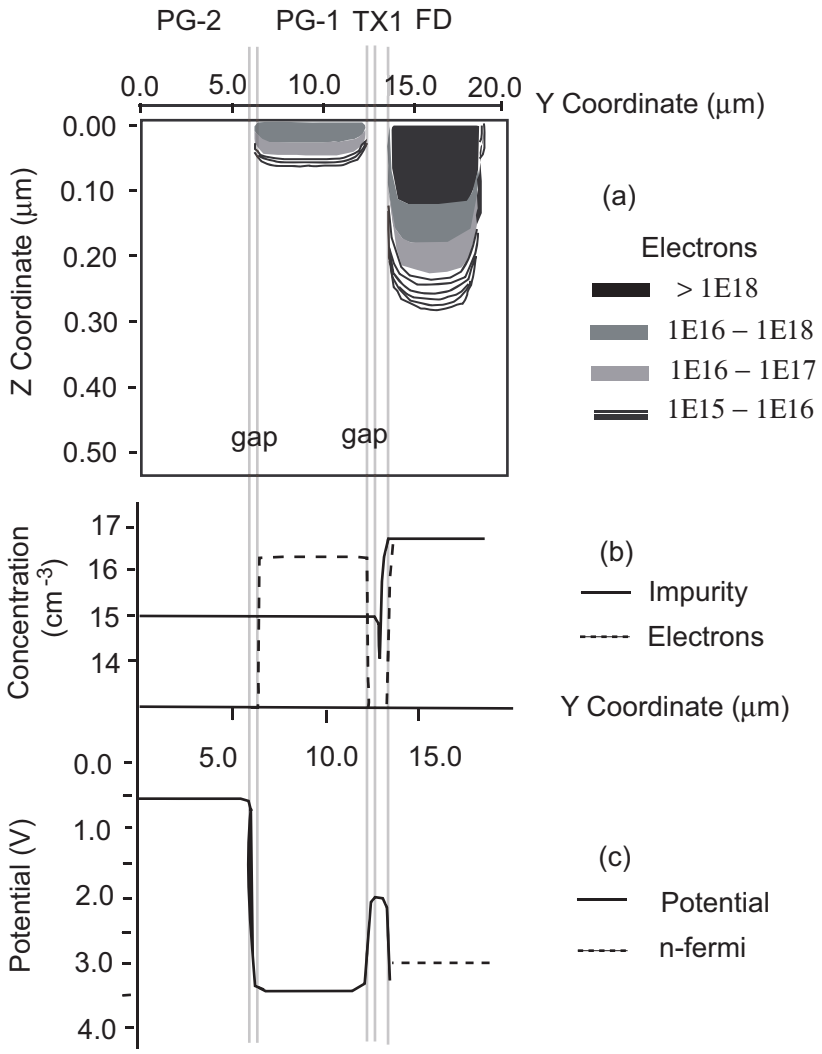

Fig. 5-9 *a) YZ plot of electron concentration after the first transfer (t = 5 ms). (b) Electron and impurity concentration along Y axis (t = 5 ms). (c) Surface potential plot (along Y axis) (t = 5 ms).*

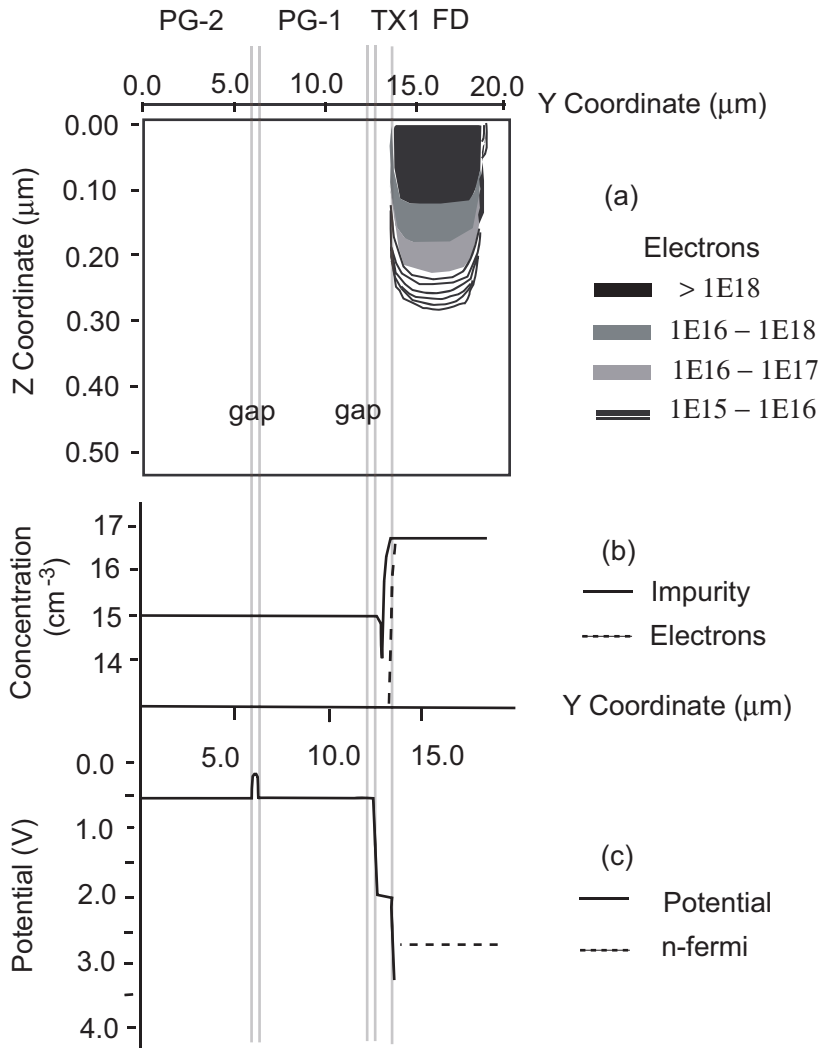

Fig. 5-10 *a) YZ plot of electron concentration after the second transfer (t = 7 ms). (b) Electron and impurity concentration along Y axis (t = 7 ms). (c) Surface potential plot (along Y axis) (t = 7 ms).*

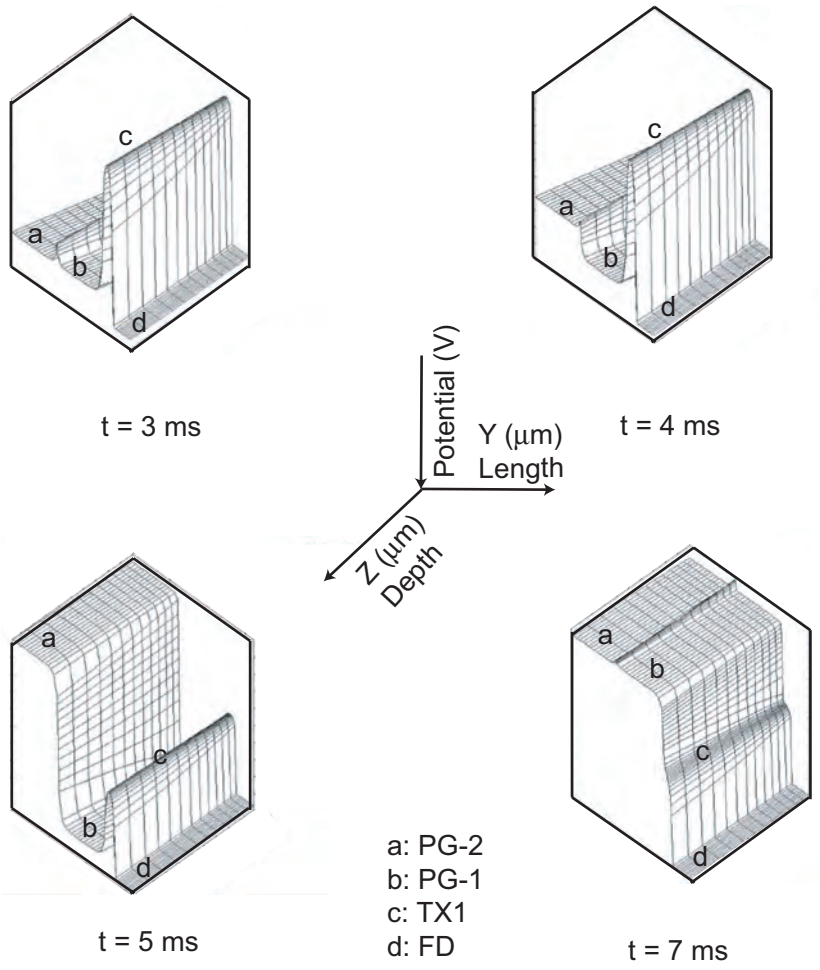

Fig. 5-11 *The 3-D plots of the surface potentials (along the Y axis) at different points in time corresponding to earlier figures. The potential axis is depicted to be positive downwards. The maximum depth into the substrate simulated is 0.1 μm.*

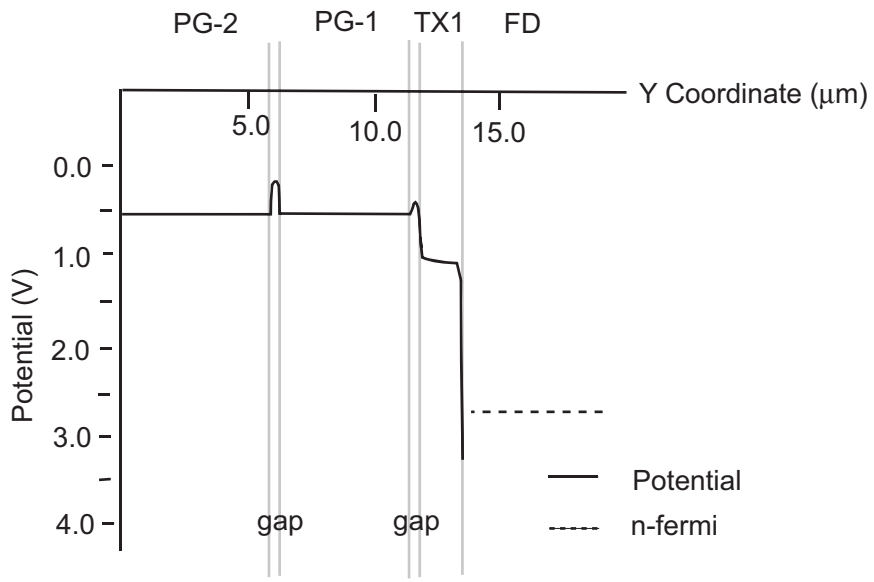

Fig. 5-12 *Surface potential plot after the second transfer (t = 7 ms). The transfer gate in this simulation is biased at 0.5 V instead of 1.5 V. Notice the "hump" at the PG-1/TX1 interface.*

This change in the quasi-Fermi potential is due to the electrons that discharge the floating node capacitance and change the reset potential.

The sequence of operation in 3-D representing the Y-axis (length), the Z-axis (depth) and the surface potential corresponding to the timing sequence described above is shown in Figure 5-11.

Figure 5-12 shows the simulation in which the transfer gate (TX1) is biased at a constant potential of 0.5 V. It can be seen that a potential hill is present between PG-1 and TX1. This would hamper the smooth flow of electrons from the photo-gate into the floating diffusion. As shown earlier in Figure 5-5, the potential hill disappears for gate voltage differences of ~ 1 V. Thus, potential difference of at least 1 V should be maintained between PG-1 and TX1 for ensuring a smooth transfer of charges into the FD node. In order to minimize the

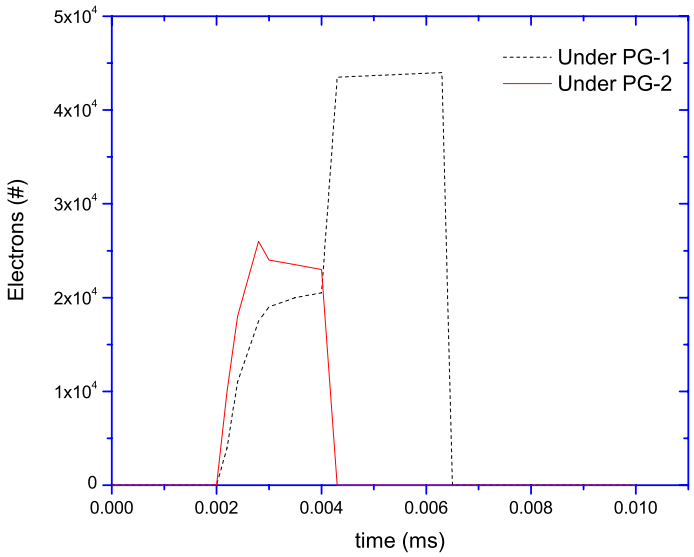

Fig. 5-13 *The number of electrons under PG-1 and PG-2 as a function of time.*

dark current generated from the transfer gate, a pulse of an appropriate voltage can be applied instead of a DC bias. The reset operation can also be carried out immediately before the actual transfer so as to clear any dark current collected by the FD node during the integration period.

To calculate the generated electrons, we can use the formula [5.10]:

$$\#\ e = \frac{P_{in}\left(\frac{W}{cm^2}\right) \times Area(cm^2) \times time(s)}{E(\lambda_{ph})(eV) \times q} \tag{5-1}$$

where P_{in} is the incident power, $E(\lambda_{ph})$ is the energy of incident photon (2.25 eV corresponding to green photons) and q is the fundamental charge constant. Considering 100% quantum efficiency, the generated electrons can be calculated to be 4.86×10^4.

The simulation of the number of electrons beneath each gate as a function of time is shown in Figure 5-13. The simulation predicts the number of electrons to be 4.27×10^4. This implies a QE of 87%. The high QE is unrealistic in real cases due to the absorption of photons in the polysilicon layer (up to 20%), as well as limited epi-layer thickness (~ 3 - 4 μm). The simulation predicts almost equal amounts of photo charges (electrons) being collected under the gates after the integration time. This simulation also points towards the possibility of integrating the charges independently under the gates. Though this simulation is directed towards charge addition (mixing the charge packets under each photogate), multiple charge transfer can be done (starting from PG-1) for sub-pixel resolution.

5.3 Fabrication and layout

From the previous section, we understand that the gap-region is very important for efficient charge transfer. The smaller the gap, the better will the charge transfer efficiency. The presence of dopants or impurities in this region can “distort” the surface potentials and hamper a smooth charge transfer process. Thus, this gap-region should be formed in such a way that it is rendered free of unintentional dopants. Conventional MOSFET processes utilize “self-aligned” processes for device fabrication. This means that it uses the gate region as a mask for the drain and source region formation. During this process, the gate region is also doped, thus reducing the polysilicon resistance and thereby gate-contact resistances. An n-LDD (n^- type) deposition is performed prior to this step especially in deep-submicron processes. This is necessary since as device dimensions reduce, strong electric fields may be created in the gate channel resulting in “hot electron” problems [5.11]. These electrons possess high energies that can cause impact ionization and additional electron-hole pairs by breaking Si-Si bonds. Such carriers may also gain sufficient energy to surmount large energy barriers such as the 3.2 eV barrier between Si conduction band and the SiO_2 conduction band. This results in carriers being injected into gate dielectrics which may get trapped and cause reliability problems.

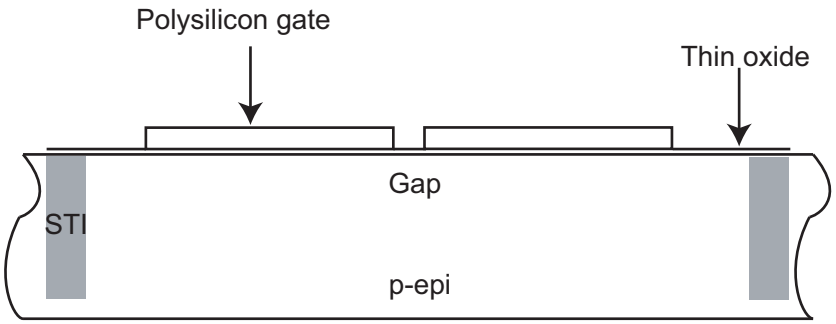

Fig. 5-14 *The deposition of polysilicon gates that act as "natural" masks for drain/source deposition (not to scale).*

The main approach taken in our design is to fabricate "split" or finger gates with a small gap in between the gates. Obviously, it is necessary to circumvent the problem of unintentional doping of the gap regions due to the self aligned process used in CMOS technology. The approach should be such that it is simple (i.e. does not introduce extra masks) and effective. The introduction of a simple n-LDD mask was found to be enough for this purpose. In order to understand how a minor modification can help achieve the goal, the steps involved in the fabrication process are highlighted.

The first step in a CMOS process is the formation of the gate regions that naturally act as masks for the drain and source diffusions as was mentioned earlier (Figure 5-14). Next, the n-LDD regions are deposited. This is a relatively lighter doping compared to the source/drain regions. The lighter doping reduces the electric fields and the problems related to the same. If this is masked, the deposition is not performed (Figure 5-15). The n-LDD deposition is masked by using an n-LDD block layer. Since we do not operate the device as a conventional MOSFET, (in the strong inversion region), but rather in the depletion mode, we do not have to consider hot-carrier and related effects in our design.

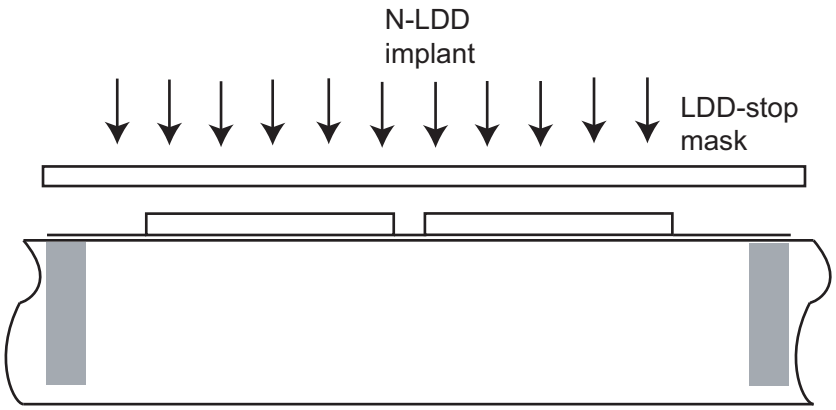

Fig. 5-15 *The n-LDD deposition is masked by using an n-LDD block layer.*

After the n-LDD step, sidewall spacers are formed by LPCVD deposition of conformal spacer dielectric (SiO_2 or Si_3N_4) and anistropic etching, usually a plasma reactive-ion etch (Figure 5-16). These sidewall spacers help in providing a smooth doping-transition from drain/source diffusion regions to the gate. The minimum thickness of this spacer in technology used is around 100 - 120 nm (Figure 5-18). When the gates are placed extremely close (~ 240 nm), these spacers will merge due to their thickness as well as technological constrains.

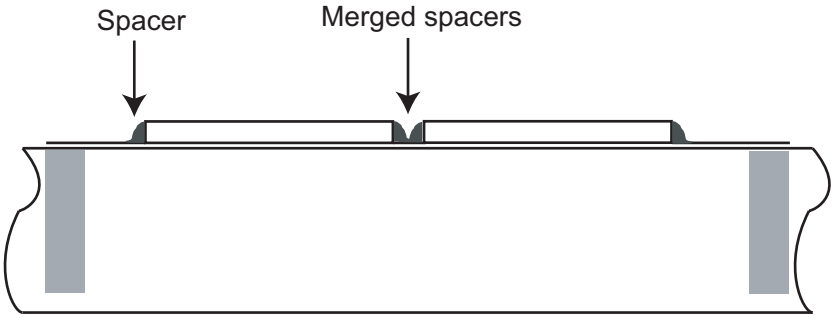

Fig. 5-16 *Due to the very small gap, the spacers merge.*

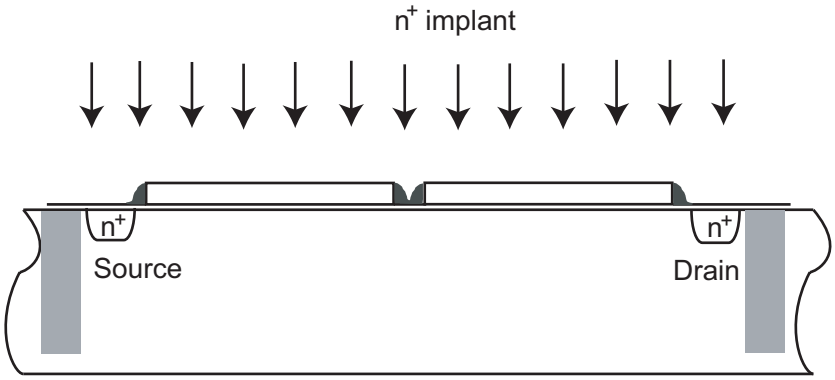

Fig. 5-17 *Finally, the source and drain regions are formed by n^+ doping.*

The merged spacers further act as masks for subsequent source or drain deposition [5.12], [5.13]. This ensures that the gaps are free from all types of dopants. A recent trend in technology is to reduce the thickness of the spacers. Thus care should be taken to preserve the thickness so that the merging can be accomplished by this technique. In addition to these steps, it is also necessary to use a silicide blocking mask. This is to prevent the silicide formation on top of the gates as they could hinder the transmission of light through the polysilicon gates. The high concentration n^+ drain and source regions are formed as the last step (Figure 5-17).

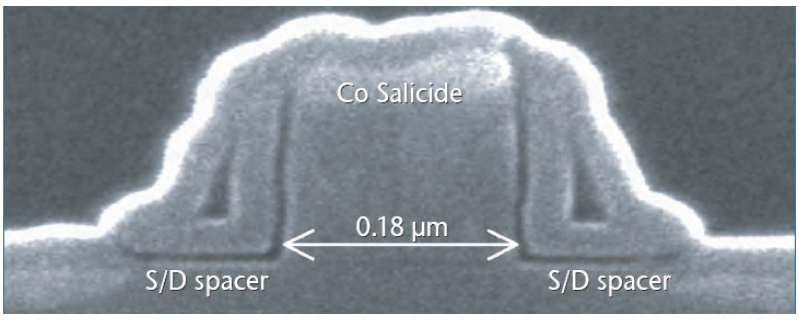

Fig. 5-18 *Cross-section of the source/drain (S/D) spacer in a 0.18-µm process [5.14]. © 2007 X-FAB Semiconductor Foundries AG*

The source region is not really necessary in the formation of the CCD. In our design, it is an added advantage since it can be used to inject electrons underneath the photogates for electrically characterising the sensor. An addition transfer gate (TX2) is necessary to isolate the source from the CCD during normal operation.

The 1st and higher order metal contacts, intermediate dielectrics including organic materials and a final passivation layer are formed subsequently. It should be noted that these fabrication steps do not affect the electrical properties of the CCD though the optical properties would be affected.

Figure 5-19 and Figure 5-20 respectively show the layout of a 1 photogate and a 2 photogate structure that were designed. The photogates, the transfer gates, the source follower, the reset transistor as well as the source/drain regions are indicated in the layout. A metal-2 layer is used to cover the whole of the non-imaging regions. It was kept grounded to avoid shifts in device operation conditions due to the possibility of charge trapping in the metal-dielectric region. The reason to use the metal-2 layer was to keep the routing simple (since metal-1 was used to contact the drain/source regions), but at the same time keep the metal layer as close as possible to the structure. During the experiments, this did present problems as a small light leakage was observed and is explained in the section on experimental results. It is hoped to be prevented in future devices by careful metal-1 routing as well as utilizing higher order metal light shields.

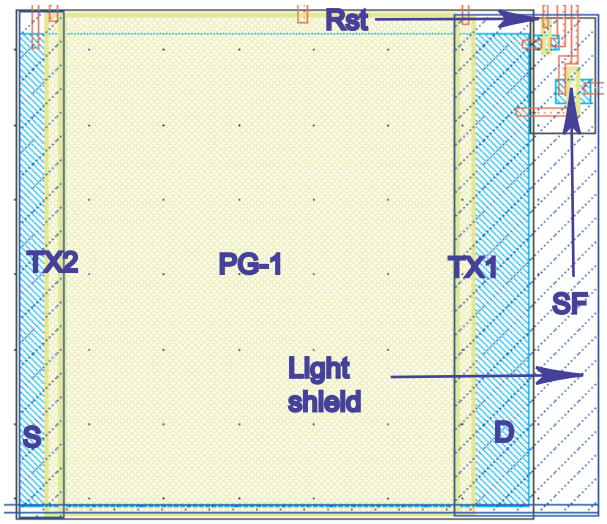

Fig. 5-19 *Layout schematic of the 1 photogate structure.*

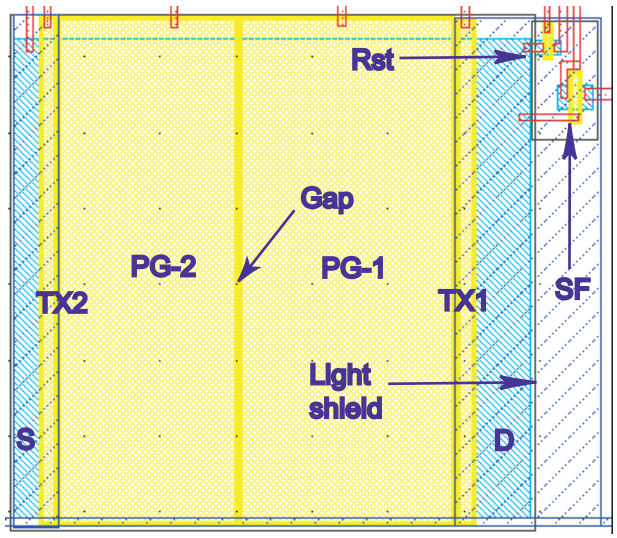

Fig. 5-20 *Layout schematic of the 2 photogate structure.*

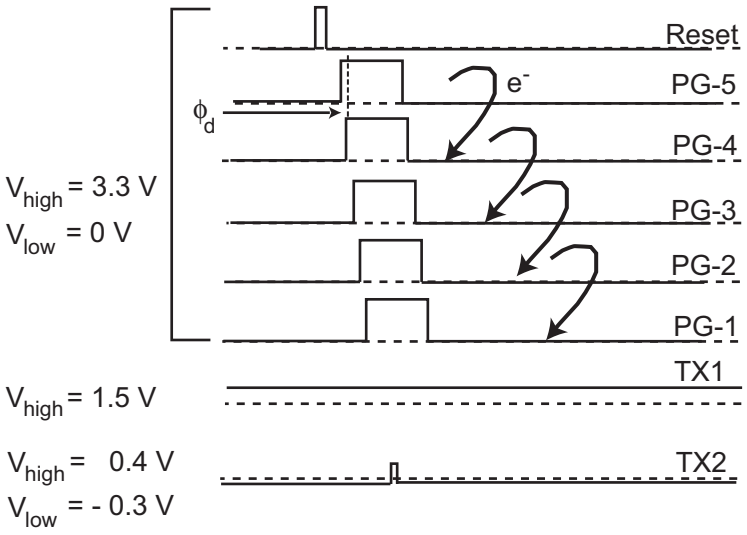

Fig. 5-21 *Timing diagram for the 5 photogate structure.*

Parameter	Value
Photogate dimension	26×31.5 μm^2
Transfer gate length	1 μm
Gap width	0.24 μm
Floating diffusion dimension	3.7×31.5 μm^2
Conversion gain	10 $\mu V/e^-$
Full-well capacity (FD node)	113 ke^-
Dark current	0.6 nA/cm^2 (300 K)
I_{bias}	5 μA

Table 5-1. *Important parameters of the CCD fabricated in standard CMOS technology.*

5.4 Results and discussion

The important parameters of the fabricated CCD are shown in Table 5-1. For the operation of the device, a test-system was developed based on Xilinx FPGA (Field-Programmable Gate Array) and analog components for analog voltage levels. The chip was housed in a light-proof box and has the LED mounted through a tiny hole. Care was taken to seal stray light from entering through the system and all measurements were carried out at room temperature. In the following experiments, use of the 1 and the 5 photogate structures are utilized, and the functioning of the structures compared.

For the confirmation of the operation of the CCD, the pulses were provided as per the scheme represented in Figure 5-21 and measurements were performed in the dark (using charges injected through TX2). The reset transistor gate-voltage (V_{Rst}) was pulsed momentarily to reset the floating node and clear it off from residual charges. The integration of charges was carried out by pulsing the photogates to a high potential.

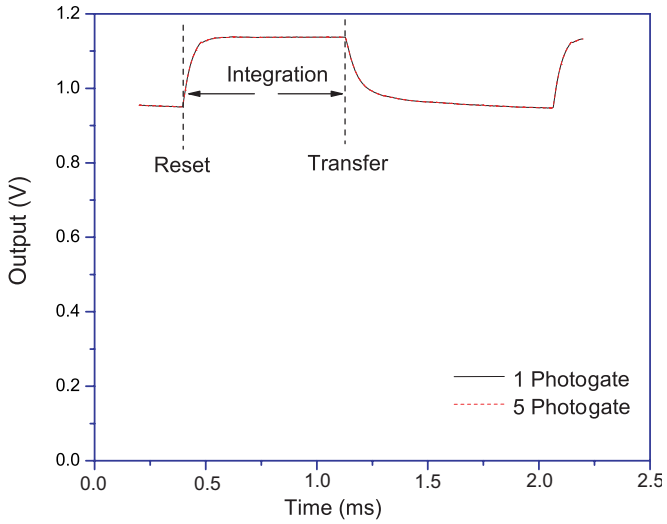

Fig. 5-22 *Output response of the 1 as well as the 5 photogate structure on charge injection from the source by pulsing transfer (TX2) gate.*

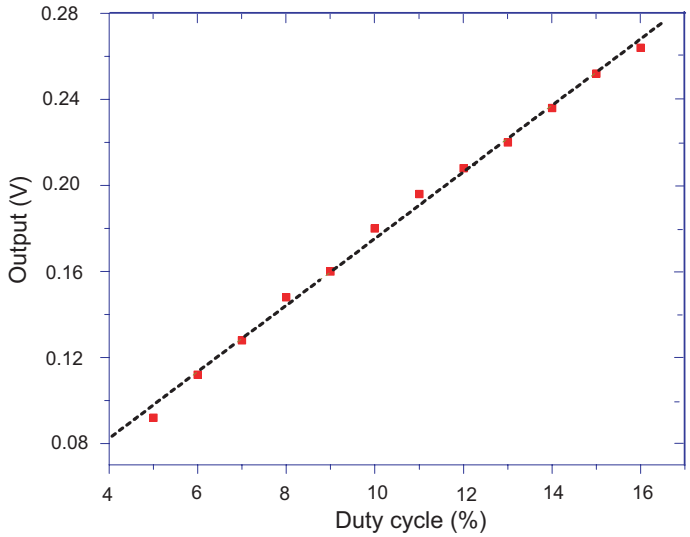

Fig. 5-23 *The linearity check of the photogates after a CDS operation.*

Each of the photogates were driven with a small offset (ϕ_d) of a few µs w.r.t the previous gate. The source region was kept grounded while the transfer gate (TX2) was pulsed momentarily to inject electrons into the FD node. This is done during the period that the photo-gate integration periods overlap. Thus the gates integrate equal amount of charges in this scheme. To drive the charges from the left to the right (into the floating diffusion node), the integration was started with PG-5. The charges that are collected beneath it are transferred and added with charges under PG-4 and so on. The integration time under each of the photogates (t_{int}) was 0.73 ms. The accumulated charges are then transferred to the floating diffusion node via the transfer gate (TX1). In this measurement, the transfer gate was biased with a constant DC voltage of 1.5 V. A bias current of 5 uA was chosen to bias the SF (source follower).

Figure 5-22 shows the FD node voltage as a function of time. The node voltage resets to a high voltage (1.13 V) and holds at this value until the integration (t_{int}) period of 0.73 ms. When the collected charges are transferred to the FD node, a drop in potential is seen.

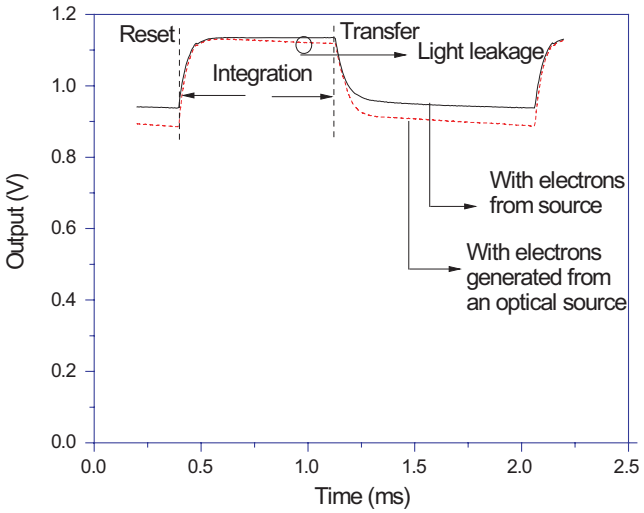

Fig. 5-24 *Output response of the 1 photogate as well as 5 photogate structure on charge injection from the source by pulsing transfer (TX2) gate.*

No appreciable difference was observed in the response of the 1 photogate or the 5 photogate structure. The reset potential dropped from the value of 1.13 V to about 0.98 V after the charge transfer operation in both the structures. The linearity of the CCD was checked by varying the duty cycle of the TX2 signal (Figure 5-23). This was thanks to the fact that the amount of injected carriers in linearly dependent on the width of the TX2 pulse. The output was found to be linear until the saturation value of 1.13 V.

Figure 5-24 shows the response of the CCD to an excitation with a light source obtained through a LED. In this case, the TX2 is held at a small negative potential so that the source region is disconnected from the CCD. As can be seen, there is a small light leakage present in the response of the CCD, both during the integration period as well as the transfer. The slopes of these curves are also parallel to each other, confirming a light-leakage problem. As mentioned earlier, we opted for a metal-2 layer for the light shielding. The photons incident on the CCD can undergo multiple reflections

from between the metal layers to reach the FD node. This is hoped to be prevented in future devices by using multiple metal layers and careful routing. In our present measurements, this can be avoided by adopting the following measures:

- Performing a reset operation prior to charge transfer. This would clear both the dark current collected at the FD node during the integration period, and any stray photons collected by the node.

- Using a pulsed-light excitation rather than a constant light source during the integration period. In this way, the intensity of the source can also be accurately varied by controlling the pulse width of the light source.

CTE (Charge Transfer Efficiency) measurements

The contributing factors to charge transfer inefficiency are [5.15]:

- The nature of the exponential decay of charge during transfer by diffusion and the fringing fields.

- Finite transfer time during the clock period.

- Potential barriers in the gap region.

Usually specialised techniques like X-Ray transfer methods, extended pixel edge response (EPER), pocket pumping etc are used for absolute CTE measurements. This works for large CCD structures which can “amplify” the tiny losses at each stage. The device under consideration does not have many stages that can accurately characterize these inefficiencies. Thus the characterization of absolute CTE is beyond the scope of the present work. However, a simplified experiment is attempted to see if there are serious charge losses due to the presence of pockets in the structure. The technique employed for this is multiple read-outs of the charges to see if there are any charges remaining under the gates or in potential pockets. Figure 5-25 illustrates this idea.

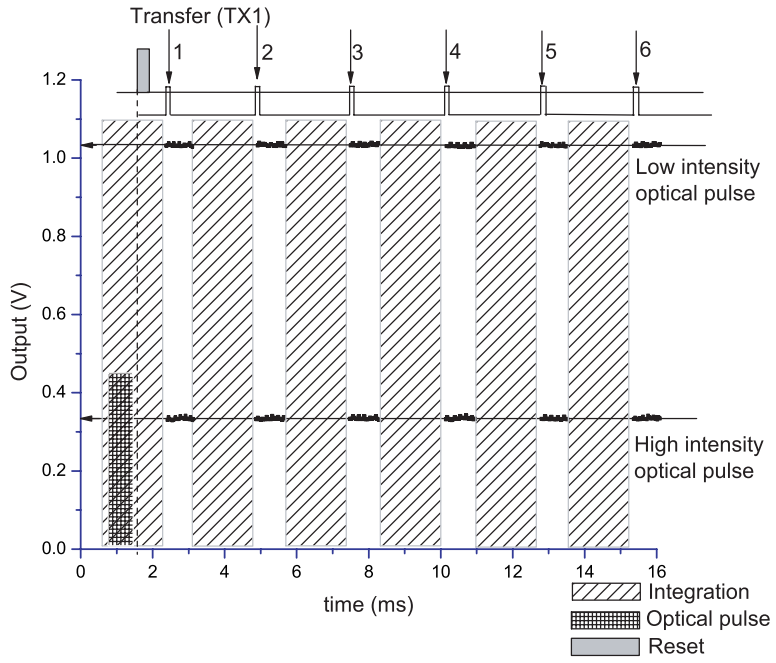

Fig. 5-25 *CTE measurements on the 5 photogate structure.*

The operation begins with the integration process wherein the photons from a short pulse of LED are collected by the photogates. A reset of the FD node is performed to remove any charges collected here. Following this, the photogates are sequentially switched to move the charges towards PG-1 and finally, the transfer gate is pulsed high to transfer charges to the FD node. The collected charges reduce the floating node potential. The second set of integration is performed but this time, without the light pulse and the transfer process repeated. This process is continued several times. If there are serious charge losses, we would see each transfer discharging the FD node until a "stable" and flat region is attained.

The experiment was conducted on the 5 photogate structures at both low and high light levels obtained by varying the "ON" period of

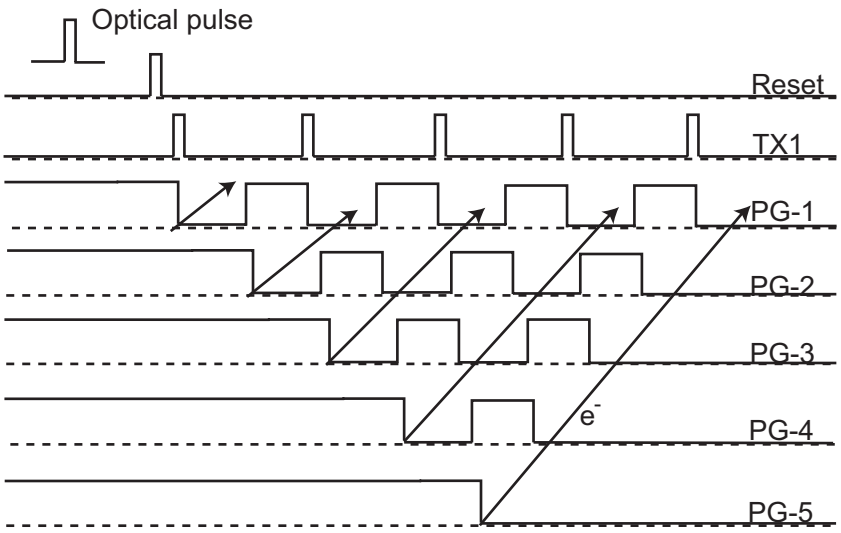

Fig. 5-26 *Timing scheme employed for testing the multi-resolution capability of the sensor.*

the LED. As can be seen from Figure 5-25, no major losses can be observed in the structure. The output is found to be stable at the first transfer process. This indicates that there are no major charge losses in these CCDs. However, exact CTE measurement techniques as mentioned before may help in locating the few hundreds of electrons that may have been lost in potential pockets in these structures.

Multi-resolution capabilities

The device operation until now was based on the charge-addition capabilities of the CCD sensor. This is very useful in low-light conditions where high sensitivity is paramount. It was noticed from the simulations that it is also possible to perform multiple transfers thanks to the surface potential pockets that are formed when the gates are biased at the same potential. This means that it would be possible to collect information from each of the photogates, the downside being a larger memory requirement (for sto-

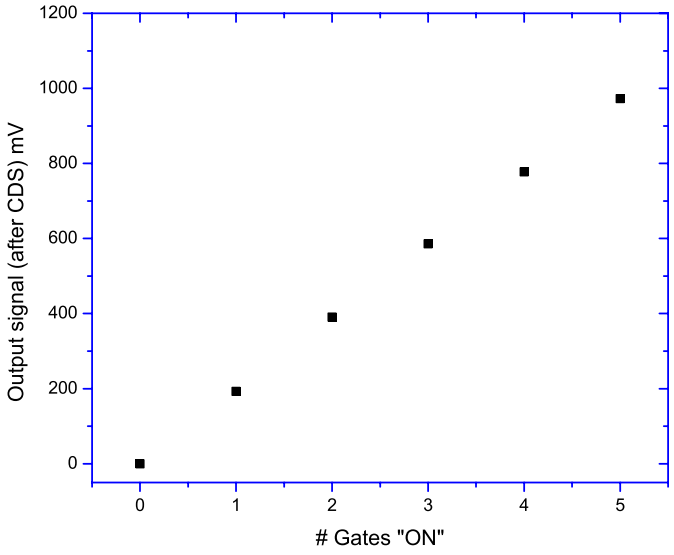

Fig. 5-27 *Contribution from each of the photogate after CDS.*

ring the information on-chip) as well as a larger read-out time. This will also hamper the dynamic range of the sensor. The multiple read-out process would be useful in situations where the image intensity is high enough and read-out speeds/memory requirements are not stringent but where high resolutions are required.

To verify the idea, the scheme shown in Figure 5-26 is used. The charges in each photogate, starting from PG-1, are sequentially dumped into the FD node that has been reset. The output signal after CDS is noted for each transfer. The LED light incident on the CCD can be considered to be uniform across the area of the sensor. The output voltage after the CDS operation is shown in Figure 5-27. It can be seen from the figure that each transfer process contributes 1/5th of the total charge collected from the CCD. This confirms the idea that multi-sampling capabilities can be realised easily with the structure. By incorporating micro-lenses above each of the photogates, photons

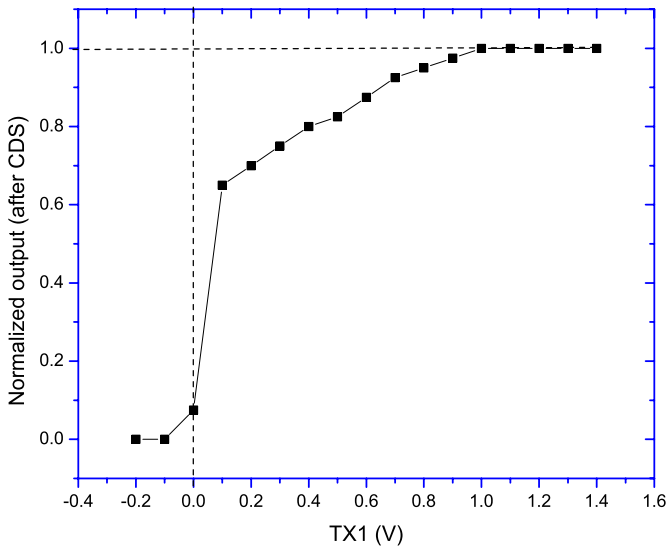

Fig. 5-28 *Normalized output after CDS as a function of transfer gate (TX1) voltage.*

can be focussed onto each of these pixels for higher efficiency and prevent pixel crosstalk. The multi-resolution scheme can be very useful in many medical applications where a small area has to be read-out at high resolution. The dexterity of this CCD structure is in its ability to perform both in the high dynamic range mode by charge addition within the pixels, as well as multi-resolution by independent read-outs. Other clocking schemes can also be employed using this structure for faster read-out as well.

To conclude this section, the effect of transfer gate (TX1) on the output is investigated. Figure 5-28 shows the normalized output after CDS for different transfer gate (TX1) voltages. It can be seen that the output reaches a maximum and saturates at around 1.0 V. This is consistent with the simulations result (Figure 5-5) where a difference between the gate voltages of around 1 V results in the disappearance of the potential hill. By employing the selective transfer gate switching mechanism, dark current introduced through the transfer gate can be effectively curtailed.

5.5 Chapter summary

In this chapter, the feasibility of a CCD like image sensor in standard 0.18-μm CMOS technology has been discussed. It was found that by using the standard processing capabilities, and utilizing the very small feature sizes available in the standard technology, a CCD like structure can be realized. Since the deep-submicron technology is essentially radiation hard, these CCDs can be used for medical/ outer-space applications without the need for further modifications. Moreover, clever techniques can be employed within the structure like charge addition for increased dynamic range or multiple read-out for higher resolution. The latter however comes with the price of higher memory requirements for storing the signal on chip as well as lower read-out speeds. The dynamic range is also affected since the photons under only one gate is effectively read-out. Thus it is highly suitable when high image intensity is available, and where speed requirements are not paramount. Digital X-ray diagnostics is a good example of the application of this sensor. Recently, a CCD like image sensor in CMOS technology has also been reported by [5.16].

With the aggressive development of deep-submicron technologies, there is a trend to also reduce many of the key fabrication steps that are essential for realizing this device, including the sidewall spacer thickness. Additional design considerations have to be taken care under such circumstances. Thus, the progress of submicron technology is a double edged sword: in one hand, the smaller feature sizes help in efficient surface potential manipulations, on the other hand changes in the technology does not allow the easy fabrication of such sensors without much careful revision of the design.

5.6 References

[5.1] A. J. P. Theuwissen, “Solid-State Imaging with Charge-Coupled Devices”, Kluwer Academic Publishers, pp. 25-35, 53-65, 317-348, 1995.

[5.2] J. R. Janesick, “Scientific Charge-Coupled Devices”, SPIE Press, pp. 22-27, 2001.

[5.3] A. J. P. Theuwissen, “CCD or CMOS Image Sensors for Consumer Digital still Photography?”, Int. Symp. VLSI Tech., pp. 168-171, 2001.

[5.4] Padmakumar R. Rao, Xinyang Wang, and Albert J.P. Theuwissen, "CCD Structures Implemented in Standard 0.18-μm CMOS Technology", IEEE Elec. Lett., Vol. 44, No. 8, pp. 548-549, 2008.

[5.5] J. G. C. Bakker, “Simple Analytic Expressions for the Fringing Field and Fringing-Field-Induced Transfer Time in Charge-Coupled Devices”, IEEE Trans. Elec. Dev., Vol. 38, No. 5, pp. 1152-1161, 1991.

[5.6] H. Ohyama et al., “Defect Assessment of Irradiated STI Diodes”, Nuc. Inst. Meth. B, Vol. 186, No. 1, pp. 424-428, 2002.

[5.7] S. Kleinfelder et al., “Novel Integrated CMOS Sensor Circuits”, IEEE Trans. Nuc. Sci., Vol. 51, No. 5, pp. 2328-2336, 2004.

[5.8] D. F. Barbe, “Imaging Devices using the Charge-Coupled Concept”, IEEE Proc., Vol. 63, No. 1, pp. 38-67, 1975.

[5.9] H. Mutoh, “Simulation for 3-D Optical and Electrical Analysis of CCD”, IEEE Trans. Elec. Dev., Vol. 44, No. 10, pp. 1604-1610, 1997.

[5.10] Y. Kraftmakher, “Determination of the Quantum Efficiency of a Light Detector”, Eur. J. Phy., Vol. 29, No. 4, pp. 681-687, 2008.

[5.11] J. Tsai et al., “Hot Carrier Degradation in Deep-Submicron Nitride Spacer Lightly Doped Drain n-Channel Metal-Oxide-Semiconductor Transistors”, Jpn. J. App. Phy., Vol. 41, No 8, pp. 5078-5082, 2002.

[5.12] Sollner et al., “Manufacturing CCDs in a Conventional CMOS Process”, U.S Patents, Pub. No. US 2007/0161148 A1, 2007.

[5.13] M. Duane et al., “Merged Sidewall Spacer formed between Series-connected MOSFETs for Improved Integrated Circuit Operation”, U. S Patents, Pub. No. 6329695, 2001.
[5.14] http://www.xfab.com/fileadmin/X-FAB/Download_Center/Technology/CMOS/XC018_CMOS_Info_sheet.pdf
[5.15] S. M. Sze, and Kwok Kwok Ng, “Physics of semiconductor devices”, John Wiley and Sons, 3rd edition, pp. 709, 2006.
[5.16] K. Fife, A. El. Gamal, and H. S. Philip Wong, “A 0.5 μm Pixel Frame-Transfer CCD Image Sensor in 110 nm CMOS”, IEDM, pp. 1003-1006, 2007.

General conclusions and suggestions for future work

In this chapter, some of the general conclusions derived from the work presented in this thesis is summarised. In addition to the suggestions provided in each of the chapters, some guidelines for possible future work will be highlighted here. It is hoped that this will install the curiosity and enthusiasm necessary for researchers to carry out further research on the present topic.

6.1 Radiation hardness of semiconductors and in particular, CMOS image sensors

In this thesis, fundamental radiation studies were carried out on a simple, yet effective structure called as the finger gated-diode. The results obtained through this structure was helpful in analysis the radiation induced effects on complex devices such as CMOS image sensors. This section presents some conclusions based on the radiation studies on the finger gated-diodes as well as 4-T CMOS image sensors.

6.1.1 Finger gated-diodes (FGDs)

In the first phase of this investigation, radiation hardness of deep sub-micron technology was evaluated using a very simple structure called as the gated-diode (GD). It was found that the GDs are very simple, yet effective structures for semiconductor parameter extraction and non-destructive testing (NDT). The GDs were successfully fabricated in the form of fingers to preserve the geometry required to extract necessary parameters in 0.18-μm technology. The characterization of these finger gated-diodes (FGDs) was successfully accomplished using a specialized test system. The surface recombination velocity (s_0) and the generation lifetime (τ_0) were successfully extracted using the FGD. The values obtained for a virgin FGD were s_0 = 2.78 cm/s and τ_0 = 3.47 μs. Several other parameters were also successfully estimated using the FGDs. An activation energy for the FGD diode leakage current of 0.62 eV in the low temperature range (< 70^o C) was obtained using the Arrhenius plot. This is close to the value of $E_g/2$. The slope of J_{jun} vs 1000/T in this temperature range corresponds to the slope of n_i. For the high temperature range (> 70^o C), an activation energy of 0.98 eV was obtained. This is close to the value of E_g. The slope of J_{jun} vs 1000/T in this temperature range corresponds to the slope of n_i^2.

By using a photonic sub-band technique which utilizes an infra red laser, the density of interface traps at the Si-SiO_2 interface (D_{it}) was successfully mapped. With the assumption of the capture cross section area of 10^{-16} cm^{-2}, a U-shaped distribution of D_{it} was extracted with a mid gap level of ~ 0.5×10^{11} $eV^{-1}cm^{-2}$. This indicates that the surface is of very good quality.

6.1.2 Radiation effects on FGDs

Since the FGD structure enables the characterization of the silicon technology, these devices were further utilized in studying radiation induced damage mechanism. This provides more clues to radiation induced degradation in very complex devices such as CMOS image sensors. Only γ-ray irradiation studies were carried out and transient effects were not included in the study.

The γ-ray (1.17 MeV-1.33 MeV) dose used for the experiments was from 0 to 1000 Gray in steps of 200 Gray, with a dose rate of 75.9

Gray/min. An obvious increase in the FGD response was seen after the irradiation process. Since the gate oxide thickness in deep sub-micron technologies is very small (~ 4 nm), charge trapping and interface trap build-up should be minimal. This was confirmed by observing the point of inversion of the curves, which remained unchanged. This indicates that negligible charge trapping has occurred in the SiO_2 region that can shift the flatband or threshold voltages. This is especially encouraging since 4-T CMOS image sensors include in-pixel amplifiers and transistors for its operation. Radiation induced threshold as well as gain variation in these transistors will be minimal. This is also true for transistors used in the analog/digital modules of the sensor such as the CDS circuitry.

The dark current degradation from the bulk and the surface as a function of irradiation was resolved successfully. The surface leakage current is found to saturate at ~ 400 Gray, which signifies a saturation of the interface traps. There was a knee point for the bulk leakage current at around the point of 400 Gray, after which it increases quickly. In the FGD structures, there exists a very small region where the depletion under the gate interacts with the STI at the device periphery. Thus, the STI leakage component is coupled with I_{fij} and cannot be seperated with the current FGD structures. Since displacement damage due to γ- or X-rays is quite limited, the contribution of bulk depletion regions to the leakage increase is doubtful. However, from the available FGD results, it was concluded that an increase in the radiation induced leakage current density with a slope in the range of a few pA/cm^2/Gray for both the surface as well as the bulk component occurs. The surface leakage is seen to evolve slowly, and saturate at higher radiation doses. Further, no threhsold shift occurs implying that the gate region is highly radiation tolerant.

6.1.3 Radiation effects on CMOS image sensors

Electrical effects

Several test-structures with different STI (Shallow Trench Isolation) configurations were successfully fabricated in deep sub-micron technology. These test structures were subjected to radiation as was with the FGDs. It was found that the p-well passivated STI structures

suffered less leakage current degradation compared to the un-passivated ones. Further, the closer the STI was to the photodiode, the higher was the degradation.

It was observed that the imagers that had the diode structures "completely" isolated from the STI (case NTA = 0.3 μm, p-well protected), had a negligible dark current evolution after irradiation. As the fully-depleted diode has a very large depletion region, this points to the fact that displacement damages due to γ- or X-rays is negligible. This it can be safely concluded that degradation of the STI region is primarily responsible for increase in I_{fij}, also for the FGDs.

In this context, it was suggested that the distance as well as the passivation should be tailored so that other features of the image sensor (like full-well capacity) are not overly sacrificed.

The Arrhenius plots indicate that there is a decrease of the activation energy after irradiation. This could be due to the introduction of additional energy states that enhances thermal generation. It was also concluded that other processes like trap-assisted tunnelling and field-enhanced emissions can also be thought to play a role in this behaviour.

When the activation energy as a function of the pixels leakage current was plotted, it was noticed that pixels with lower activation energies exhibited a higher dark current. This confirms the hypothesis that a field-enhancement phenomenon is in action can lower the energy required for thermal generation. A major candidate for this mechanism is the Poole-Frenkel effect. A 0.2 μm overlap is present between the pinned layer and the transfer gate due to self-aligned process, where high electric fields are present. This region is thought to be a major source for enhanced generation.

Optical effects

As a first step towards characterizing optical effects of radiation, an analytic solution for the internal quantum efficiency of a pinned photodiode was successfully derived. Using this model, the quantum efficiency of radiated as well as un-irradiated sensors was fitted. A post-irradiated QE attenuation in the mean of about 20% was observed at 800 Gray. Two components were resolved through the derived model for the observed change: the effective surface

recombination velocity (s_{eff}) which affected the high frequency photons and a mean correction factor (ξ_{opt}). The value of s_{eff} increased from 1.3×10^5 to 6.8×10^5 cm/s upon an irradiation dose of 800 Gray. ξ_{opt}, on the other hand, changed from 1.0 to 0.83. The high frequency photons generate carriers very close to the surface, and are very sensitive to surface traps. ζ_{opt} turns out to be a correction factor that is needed to fit the curve through the mean value of the irradiated devices. This occurs due to the effect of operating a non-linear change in the internal QE as a function of s on the "wavy" interference pattern produced by the optical stack. In other words, the peaks and valleys of the interference pattern are modulated differently by the change in the internal QE, as a result of the change in surface recombination velocity.

Using FTIR (Fourier Transform Infrared), the oxide was "probed". Since silicon by itself is transparent to far infrared, it gives a good indication of the changes to the oxide. The transmission of certain oxides such as BPSG and TEOS were seen to undergo a reduction of up to 3% and 1% in the infrared region, after irradiation with a dose of 800 Gray. To further study this phenomenon, ellipsometry in the visible spectra was also carried out. It was noticed that the refractive index of some oxides (BPSG, TEOS) undergo a slight increase upon irradiation. This can be attributed to material densification. An increase of the refractive index of ~ 0.001 was observed. Simulations conducted in the visible spectrum conclude that this change would only introduce slight shifts in the curves, and hence can be neglected. For the dose range considered, there was no indication of color centres being formed as well. Further, the average surface roughness of the oxides remain within the noise level after irradiation, thus confirming that there has been no physical modification of the surface. Thus the major reason for the change in the spectral response after irradiation can be attributed to a change in the surface recombination velocity tn the Si/SiO_2 interface of the photodiode region.

With the evolution of aggressive technologies, the number of metal layers will increase and thus affect the thickness and the choice of material used in the stack by the fabs. Hopefully, fabrication processes aimed for imaging solutions would take into consideration

the effects mentioned in this work, to improve the quality of imaging in future technologies.

6.2 CCD like image sensors in deep sub-micron CMOS technology

In this part of the work, feasibility of a CCD like image sensor in standard 0.18-μm CMOS technology was investigated. It was found that by using standard processing capabilities, and utilizing the very small feature sizes available in standard CMOS technology, a CCD like structure can be realized.

As a first step, some software simulations were performed. It was found that the closer the gap between two gates, the "smoother" and monotonic the surface potentials in the gap becomes. This enables a smooth charge transfer between adjacent photogates. For the fabrication, the minimum gap space allowed in the fabrication process—which is 0.24 μm—was chosen.

The fabrication was accomplished in 0.18-μm CMOS technology. The structures had an active photogate area of 26×31.5 μm^2, with a transfer gate length of 1 μm. The floating diffusion was 3.7×31.5 μm^2. Due to the fact that the technology constrains produce merged spacers, all kinds of impurities in between the gaps can be avoided without the requirement for extra masks.

Experiments were successfully conducted with a dedicated setup consisting of an FPGA solution that could provide digital pulses to the DUT. The sensor exhibited a small light leakage problem due to the fact that a higher order metal was employed. By utilizing a pulse sequence that ensures that the light source is present only during the time of integration, and reset is done just before charge transfer, the above mentioned problem was circumvented successfully for both characterization and successful operation of the device. The sensor showed a linear response to the light intensity.

Under this scheme, the dark current density was estimated to be 0.6 nA/cm^2 at 300 K. The sensors conversion gain was determined to be 10 $\mu V/e^-$, rendering a full-well capacity of 113 ke^- at the reset voltage of 1.18 V.

By carrying out multiple charge transfer and read-outs, it was concluded that the device does not have measurable charge transfer inefficiencies at both low- and high- lighting conditions. Further, the multi-resolution capability of the device was confirmed by transferring charges from individual photogates to the floating diffusion node, and carrying out multiple read-outs. The disadvantage of this technique in a camera system is the need for extra memory for storing each of these individual values, as well as slower device operation. It was concluded that while the charge-addition property of the sensor was useful in low-light conditions, the multiple read-out technique could be used when there is sufficient light and higher resolutions are necessary.

An output signal dependency on the transfer gate voltage was noticed. The signal output was seen to increase with the transfer gate voltage up to ~ 1 V, and thereafter saturate. To minimize transfer gate induced dark current, an appropriate pulse of the optimal voltage can be applied just before the actual readout.

6.3 Suggestions for future work

The work done in this thesis is far from complete. There is enough room for further research in the topics described in this thesis. Suggestions for improvements will be described below.

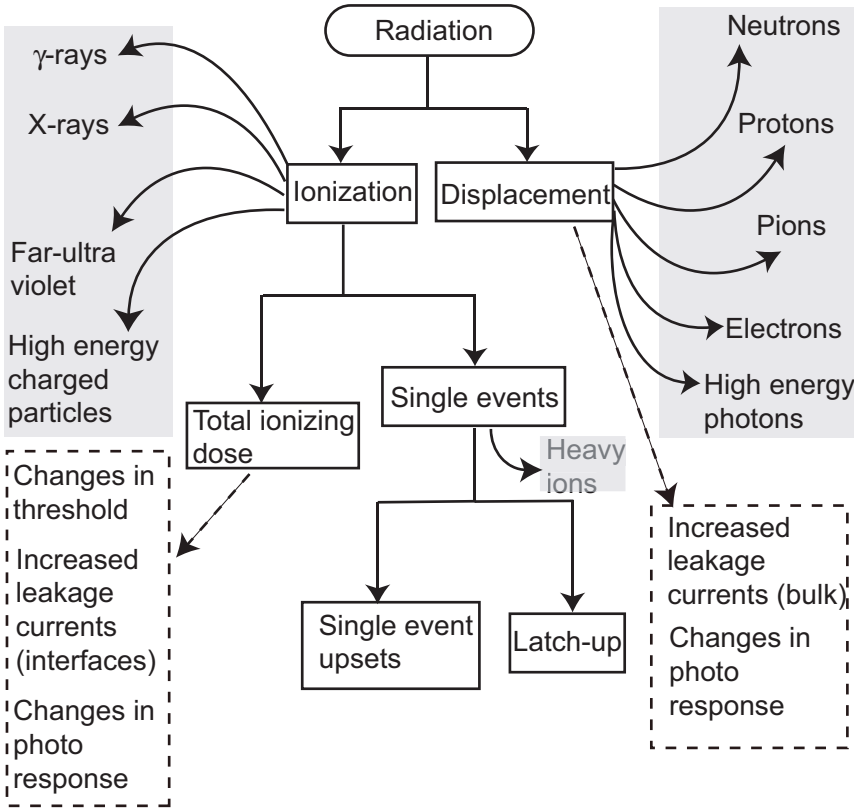

Fig. 6-1 *Different types of radiation and their effects on semiconductor devices [6.1], [6.2], [6.3].*

6.3.1 Radiation hardness studies

In this thesis, gamma-ray effects on semiconductors and in particular, CMOS image sensors have been undertaken. The main reason for choosing gamma-ray is due to the fact that the radiation tolerance of the novel CCD-like structures in standard CMOS technology (for medical applications) could also be predicted. Both gamma-rays as

well as X-rays are high energy photons. In nature, several other radiation types exist.

Figure 6-1 shows the characteristics of each of these radiation types. Unfortunately, there has not been a study that utilizes an efficient device to extract and correlate the effects of these particles on semiconductor materials. Such an effort would also enable the development of a “universal” model that would predict the effect of these particles on sensors in a radiation harsh environment. Moreover, utilizing this model, the effect of radiation damage due to a plurality of particles can be understood. This would enable designing radiation-tolerant sensors—especially for outer-space applications —where multiple types of radiation exist.

As mentioned earlier, the FGDs were successfully utilized to resolve the bulk and surface degradation mechanisms due to gamma-irradiation. Further it was also used to map the energy-dependent interface trap density using the sub-band photonic GD method. The following additional experiments can be done using the FGDs.

- Utilize the FGD to study the degradation mechanism due to plurality of particles (and their processes) referred in Figure 6-1.
- Evaluate the effect of semiconductor processing conditions on radiation tolerance using the FGDs.
- Study and compare the effect of temperature, bias conditions as well as annealing of different radiation types on silicon using the FGDs.
- Correlate the effect of radiation dose rate with natural radiation events.
- Map the energy dependent interface trap density before and after different kinds of irradiation.
- Employ multiple optical techniques on dedicated test structures for evaluation radiation induced optical degradation.

- Use the FGDs to accurately establish the effect of terrestrial cosmic rays.

The last two suggestions require more explanation. In this work, radiation effects on oxides were performed using ellipsometry (visible light) as well as FTIR (IR region). “True” transmission studies can be done using MEMS techniques that can be used to fabricate free standing “membranes” of the oxides which are both sufficiently thick as well as mechanically stable. This obviously involves a lot of additional study. Moreover, experimental techniques have to be explored including the exact alignment of these membranes with both the source as well as the detector.

In relation to the last suggestion, it was discovered by Theuwissen [6.4], [6.5] that CCD image sensors exhibit an aging effect whereby there is an increased “white” spot generation. This effect was observed even on sensors stored on-shelf. It is hypothesized that this effect is due to high-energy terrestrial rays, in particular neutrons. To confirm the hypothesis, the sensors were flown via air and land to different geographical locations. Those that were exposed to high altitudes exhibited a higher white spot generation rate.

The exact mechanism as well as the nature of particles can be effectively deduced by comparing FGDs with different geometries and oxide thicknesses which have been subjected to radiation tests. It is not known at present if the ageing effect is also a matter of concern for CMOS image sensors. Hopefully, more studies will be carried out in this direction.

6.3.2 CCD-like image sensors in standard CMOS technology

The feasibility of a CCD-like structure was presented in this thesis. It was concluded that such a device is indeed possible, and that too, without the requirements for additional masks/fabrication steps. It will indeed be valuable to fabricate a complete image sensor employing the idea. It was mentioned earlier in this thesis that several groups are active at the time of this writing to do exactly the same—albeit utilizing different techniques and improvisations. For example, Fife et al. [6.6] recently demonstrated a CCD in 0.11-μm

CMOS technology. They used a very small pixel pitch of 0.5 μm and the sensor was targeted towards depth mapping applications. As predicted from the simulations in this thesis, the smaller the gap, the better would be the performance. Thus the concept has a real advantage as the technology progresses.

As described in this thesis, the sensor can be applied for a wide spectrum of applications by choosing an appropriate logic due to its ability to perform multiple resolutions as well as charge addition within the same pixel. Some other suggestions are listed below:

- Employ the technique of fabricating CCD in CMOS technology in more aggressive technologies after sufficient optimization. The gap size reduces as technology improves, and this results in better charge transport.

- A complete sensor, if fabricated, can be used for a wide variety of applications, such as: SPECT (Single Photon Emission Computed Tomography); digital X-ray imaging; commercial camera systems; and of course, outer space applications amongst others.

- Instead of the square pixels, these closely spaced gates can also take upon interesting geometries such as a hexagon or octagon. In this scheme, the floating diffusion would occupy the centre of the pixel. This also has the added advantage in that all the charge packets would experience approximately the same amount of force towards the centre, thereby increasing transfer speeds.

6.4 References

[6.1] H. Spieler, “Semiconductor Detector Systems”, Oxford University Press, pp. 277-285, 2005.

[6.2] T. P. Ma, and P. V. Dressendorfer, “Ionizing Radiation Effects in MOS Devices and Circuits”, Wiley-IEEE, pp. 256-265, 1989.

[6.3] J. Bogaerts, “Radiation-Induced Degradation Effects in CMOS Active Pixel Sensors and Design of a Radiation Tolerant Image Sensor”, PhD thesis, Katholieke Univ. Leuven, pp. 5-8, 2002.

[6.4] A. J. P. Theuwissen, “Influence of Terrestrial Cosmic Rays on the Reliability of CCD Image Sensors, Part 2: Experiments at Elevated Temperature”, IEEE Trans. Elect. Dev., Vol. 55, No. 9, pp. 2324-2328, 2008.

[6.5] A. J. P. Theuwissen, “Influence of Terrestrial Cosmic Rays on the Reliability of Solid-State Image Sensors, Part I: Storage at Room Temperature”, IEEE Trans. Elect. Dev., Vol. 54, No. 12, pp. 3260-3266, 2007.

[6.6] K. Fife, A. El. Gamal, and H. S. Philip Wong, “A 0.5 μm Pixel Frame-Transfer CCD Image Sensor in 110 nm CMOS”, IEDM, pp. 1003-1006, 2007.

Summary

The aim of this thesis was twofold: investigating the effect of ionizing radiation on 4-T CMOS image sensors and the possibility of realizing a CCD like sensor in standard 0.18-μm CMOS technology (for medical applications). Both the aims are complementary; borrowing and lending many aspects of radiation and device physics amongst each other.

Chapter 2 introduced the gated-diode (GD). The GD turned out to be a very simple, yet powerful device capable of extracting many device physics parameters. Concepts such as generation lifetime and surface recombination velocity were presented and studied using the GD. Other essential semiconductor concepts necessary for the ensuing chapters were also presented.

Chapter 3 dealt with the fundamentals of 4-T CMOS image sensors. These sensors are state-of-the-art in the imaging world. An analytic model for the spectral response of the pinned photodiode was successfully derived and the sensitivity of the sensor to various variables was studied. The derived model was used later in the thesis to characterize the spectral degradation of the sensor due to

irradiation. The fundamentals of dark current and field-enhanced generation mechanisms were also studied.

Chapter 4 dealt with the radiation experiments that were carried out on the gated-diodes as well as the 4-T CMOS image sensors. On the positive side, it was found that the thin gate oxides used in advanced CMOS technologies provide inherent radiation tolerance. No charge trapping effects or threshold voltage shifts were noticed after irradiation. However, a rapid increase in the bulk-leakage current component was observed after irradiation in the GD and the imagers. It was found to be caused due to the degradation of the STI (Shallow Trench Isolation). By utilizing a p-well passivation around the STI and tailoring its location with respect to the diode, it was possible to curtail the dark current increase.

A decrease in the spectral response of the 4-T CMOS imagers was noticed after irradiation. FTIR and ellipsometry ruled out degradation of the optical stack that forms above the sensor. Using the spectral response model that was previously derived, it was found that an increased surface recombination velocity at the diode surface interface was to be blamed for the spectral response degradation.

In Chapter 5, the feasibility of a CCD like image sensor in standard 0.18-μm CMOS technology was investigated. By carrying out simulations, it was found that the formation of a very small gap between adjacent gates allowed the surface potentials under the gates to “overlap” and provide charge transfer capabilities. For the fabrication, the minimum gap space allowed in the fabrication process—which is 0.24 μm—was chosen. The functioning of the device was verified. Charge addition and multiple readouts schemes were successfully tested. Key sensor parameters were presented.

Chapter 6 highlights the important conclusions derived in this thesis, and offers some suggestions for future work.

Samenvatting

Het doel van deze thesis was tweeledig: het omvatte enerzijds de studie van de invloed van ioniserende straling op 4-T CMOS beeldsensoren en anderzijds de realisatie van een CCD-type sensor voor medische toepassingen, gemaakt in standaard 0.18-µm CMOS technologie. Beide doelstellingen zijn complementair waarbij aspecten als straling en systeemfysica konden worden uitgewisseld.

In hoofdstuk 2 werd de gated-diode voorgesteld. Dit bleek een zeer eenvoudige maar toch krachtige structuur te zijn waarbij veel systeemfysische parameters konden worden afgeleid. Concepten als levensduursbepaling en oppervlakte recombinatie snelheid werden voorgesteld en bestudeerd. Andere essentiële halfgeleider concepten werden eveneens besproken.

Hoofdstuk 3 handelt over de basisprincipes van 4-T CMOS beeldsensoren. In de industrie worden deze sensoren beschouwd als de meest geavanceerde. Er werd succesvol een analytisch model opgesteld waarbij de spectrale respons van de pinned fotodiode kon worden opgemeten en eveneens de gevoeligheid ten aanzien van verschillende variabelen kon worden bestudeerd. Dit model werd

later ook gebruikt voor de karakterisatie van spectrale veroudering door bestraling van de sensor. De basisbeginselen van donkerstroom en veld-verbeterde generatie mechanismen werden eveneens bestudeerd.

Hoofdstuk 4 handelt over de stralingsexperimenten die werden uitgevoerd op zowel de gated-diodes als de 4-T beeldsensoren. Enerzijds werd opgemerkt dat het dunne poort oxide dat gebruikt wordt in geavanceerde CMOS technologie een inherente bescherming geeft tegen straling: er werden geen ladings-trap effecten, noch veranderingen in drempel spanning opgemeten na bestraling. Anderzijds werd wel een snelle toename van bulk-lekstroom opgemeten na bestraling in de GD en beeldsensoren. Dit werd veroorzaakt door veroudering van de STI. Wanneer een p-well passivatie werd aangebracht rond de STI en de afstand tot de diode op maat werd aangepast, was het mogelijk om de toename van de donkerstroom terug te dringen. Voor de 4-T CMOS beeldsensor werd eveneens een vermindering van de spectrale respons opgemerkt na bestraling. FTIR en ellipsometrie toonden aan dat er geen veroudering was opgetreden van de optische lagen boven de sensor. Gebruik makend van het eerder afgeleide spectrale respons model, werd gevonden dat de verhoogde oppervlakte recombinatie snelheid aan het diode oppervlak te wijten is aan de spectrale respons veroudering.

In hoofdstuk 5 werd de mogelijkheid voor het maken van een CCD-type beeldsensor uit 0.18-μm CMOS technologie onderzocht. Door het uitvoeren van simulaties werd gevonden dat bij een zeer smalle afstand tussen naburige poorten de oppervlakte potentialen overlappen wat ladingsoverdracht toelaat. Voor de fabricatie werd de minimaal toegelaten afstand tussen twee poorten, zijnde 0.24 μm, gekozen. Het functioneren van de structuur werd bevestigd. Ladingstoediening en meervoudige readout schema's werden getest. Eveneens werden de voornaamste beeldsensor parameters voorgesteld.

Tenslotte geeft hoofdstuk 6 de belangrijkste conclusies van deze thesis en worden er enkele voorstellen gedaan voor verder onderzoek.

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Publications

Key Publications

[1] **Padmakumar R. Rao**, Xinyang Wang, and Albert J.P. Theuwissen, "Radiation Hardness of Deep-Submicron CMOS Technology Evaluated by Gated-Diode Measurements", Poster at Sense of Contact, April 4th, 2007, Zeist (Netherlands).

[2] **Padmakumar R. Rao**, Xinyang Wang, Adri J. Mierop, and Albert J.P. Theuwissen, "Gamma-Ray Irradiation Effects on CMOS Image Sensors in Deep Sub-Micron Technology", International Image Sensor Workshop, pp.70-73, 2007.

[3] **Padmakumar R. Rao**, Xinyang Wang, and Albert Theuwissen, "Degradation of Spectral Response and Dark Current of CMOS Image Sensors in Deep Sub-micron Technology due to γ-irradiation", ESSDERC, pp. 370-373, 2007.

[4] **Padmakumar R. Rao**, Xinyang Wang, and Albert. J.P. Theuwissen, “Degradation of CMOS Image Sensor in Deep-submicron Technology due to γ–irradiation”, Sol. St. Elec., Vol. 52, No. 9, pp. 1407-1413, 2008.

[5] **Padmakumar R. Rao**, Xinyang Wang, and Albert J.P. Theuwissen, "CCD Structures Implemented in Standard 0.18-μm

CMOS Technology", IEEE Elec. Lett., Vol. 44, No. 8, pp. 548-549, 2008.

Other Publications

[6] Albert J.P. Theuwissen, Martijn F Snoeij, X. Wang, **Padmakumar R. Rao**, and Erik Bodegom, "CMOS Image Sensors for Ambient Intelligence", AmIware Hardware Technology Drivers of Ambient Intelligence, Philips Research Book Series, SpringerLink, Vol. 5, pp. 125-150, 2006.

[7] Xinyang Wang, **Padmakumar R. Rao**, and Albert J.P. Theuwissen, "Noise in Deep Sub-Micron CMOS Image Sensors", Poster at Sense of Contact, April 4th, 2007, Zeist (Netherlands).

[8] Xinyang Wang, **Padmakumar R. Rao**, and Albert J.P. Theuwissen, "Characterization of Buried Channel n-MOST Source Followers in CMOS Image Sensors", International Image Sensor Workshop, pp. 223-225, 2007.

[9] Johan Leijtens, Albert Theuwisen, **Padmakumar R. Rao**, Xinyang Wang, and Ning Xie, "Active Pixel Sensors: The Sensor of Choice for Future Space Applications", SPIE Europe Remote Sensing Conf., pp. 2007.

[10] Xinyang Wang, Martin F Snoeij, **Padmakumar R. Rao**, Adri Mierop, and Albert J.P. Theuwissen, "A CMOS Image Sensor with a Buried-Channel Source Follower", ISSCC, pp. 62-63, 2008.

[11] Xinyang Wang, **Padmakumar R. Rao**, Adri Mierop, and Albert J.P. Theuwissen: "Random Telegraph Signal in CMOS Image Sensor Pixels", IEDM, pp. 115-118, 2006.

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