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A Highly Linear Receiver Using Parallel Preselect Filter for 5G Microcell Base Station Applications

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Abstract—By introducing three different techniques, this article, for the first time, presents a wideband highly linear receiver (RX) capable of handling blocking scenarios in fifth-generation (5G) microcell base station applications. First, a parallel preselect filter is introduced to satisfy the base station co-location blocking requirements. Next, a combination of third-order RF and baseband (BB) filters is adopted to attenuate close-in blockers by a -120 dB/dec roll-off. Finally, a translational feedback network is proposed to reduce the in-band gain ripple to below 0.5 dB and provide better than -19 dB input matching. Fabricated in the 40-nm CMOS technology, the proposed RX occupies a core area of 0.8 mm^2 and consumes 108–176 mW from a 1.3 V supply over the RX's 0.5–3-GHz operating frequency. It achieves a 3-dB bandwidth of 150 MHz and a noise figure (NF) of 2.6–3.9 dB over the RX frequency range. Activating the parallel preselect filter degrades the NF by as little as 1.2 dB in the worst case. The RX shows a $\geq 97.5\%$ throughput when receiving a 100-MS/s quadrature phase shift keying (QPSK) signal with 7.5-dB SNR and achieves a -9.7 dB error vector magnitude (EVM) while facing a -15 dBm continuous-wave (CW) blocker only 20 MHz away from the desired 100-MS/s QPSK signal with 12.3-dB SNR, thus satisfying the 3rd generation partnership project (3GPP) requirements with sufficient margin.

Index Terms—Blocker-tolerant, current-mode receiver (RX), fifth-generation (5G), harmonic rejection (HR), high-order band-pass filter, preselect filter, software-defined radio, wideband RX.

I. INTRODUCTION

FIFTH-GENERATION (5G) mobile communication has recently been introduced for sub-6 GHz radios to satisfy the relentless customer demands for higher data rates. However, it imposes stringent design requirements on the base station receivers (RXs). First, the RF bandwidth (BW_{RF}) can be as high as 200 MHz, demanding higher power consumption for the baseband (BB) amplifiers. Second, an out-of-band close-in blocker with -15 dBm power can appear at only 20-MHz offset frequency from the bandwidth edge, thus

requiring sharp filtering. Third, a sub-3-dB noise figure (NF) is essential to achieve a high link budget and spectral efficiency. Fourth, an $+8$ dBm far-out out-of-band blocker can also be present in co-location applications, demanding high out-of-band linearity at far-out offset frequencies [1].

Mixer-first RXs are one of the candidates that can achieve high out-of-band linearity, which makes them suitable for co-location applications [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. However, they typically suffer from poor NF and in-band linearity performance. A noise-canceling architecture can be adopted in mixer-first RXs to achieve high BW_{RF} , good in-band linearity, and decent NF [10]. However, the reported blocker 1-dB compression point ($B_{1\text{dB}}$) and filtering order [10] do not satisfy the requirements of the co-location applications. Although third-order filtering and high out-of-band linearity have been achieved in [11], [12], and [13], their NF is poor, limiting the RX sensitivity.

Alternatively, a low-noise transconductance amplifier (LNTA) can be used at the RX input to improve the noise performance [15]. To improve the out-of-band linearity of the LNTA-based RXs, an N -path notch filter can also be placed in LNTA's feedback [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. In this way, the N -path notch filter creates a feedforward path from the LNTA's input to its output, providing an unlimited rejection at the LNTA's output for far-out blockers if $G_{M1}R_{ON} = 1$, where G_{M1} is the LNTA's transconductance, and R_{ON} is the ON-resistance of switches. However, satisfying this condition over process, voltage, and temperature (PVT) variations is not feasible. Moreover, the filtering order at the RX input is only first-order, making this structure prone to the close-in blockers of the 5G applications. To solve this issue, two zeros around the LNTA's transfer function have been added to meet the specifications of the user equipment applications [26]. Nevertheless, its reported out-of-band linearity and $B_{1\text{dB}}$ are still not good enough for the base station applications.

A band-select filter can further improve the out-of-band linearity of the LNTA-based RXs. For example, to achieve sharp filtering and high out-of-band linearity, Song and Hashemi [27] proposed a band-select filter based on implementing transmission zeros in a passive network. Although the transmission zeros can be tuned, the operating frequency is limited to below 1 GHz. Alternatively, Darvishi et al. [28] proposed an active N -path filter to realize a wideband third-order band-select

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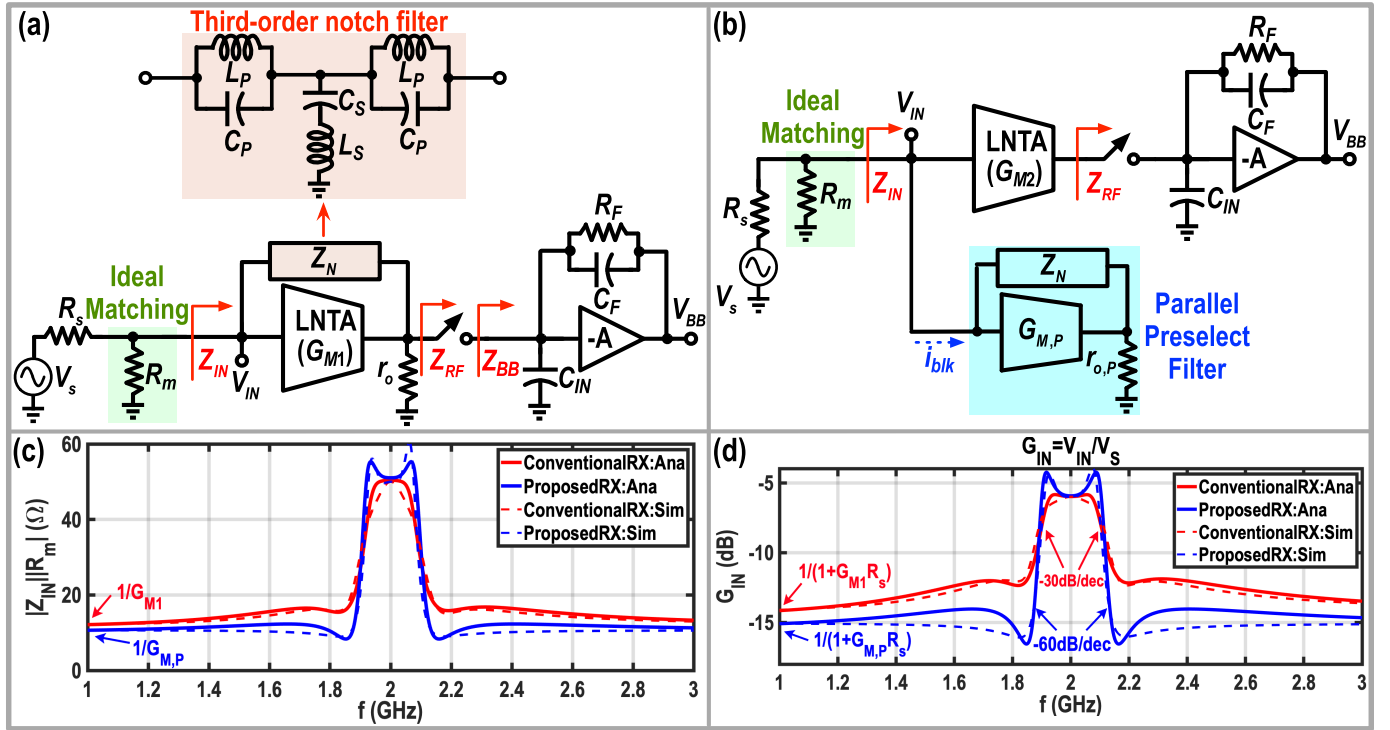


Fig. 1. (a) Conventional LNTA-based structure to achieve RF selectivity [17], [18], [19], [20], [21], [22], [23], [24]. (b) Proposed RX with a parallel preselect filter. Comparison between the analytical and simulation results of (c) $Z_{IN} \parallel R_m$ and (d) G_{IN} of the conventional and proposed RX when Z_N is an LC-based third-order notch filter.

filter. Due to its active implementation, the voltage gain of the band-select filter is around 25 dB, and the voltage gain only drops by 5 dB at the 20-MHz offset frequency. Hence, the close-in blocker will be amplified by 20 dB, making the situation worse for the subsequent RX. Moreover, the band-select filters mentioned above degrade the NF of the RX lineup by at least 2.8 dB.

To solve these issues, as has been briefly presented [29], we propose an LNTA-based RX prototype that shows similar out-of-band linearity as prior art mixer-first RXs without sacrificing NF. First, a parallel preselect filter is placed at the input of the RX to improve the RF selectivity and achieve $B_{1\text{dB}}$ better than +5 dBm. Second, we propose a third-order RF and BB filtering to achieve -120 dB/dec selectivity. Finally, a translational feedback network is introduced to reduce the in-band gain fluctuations below 0.5 dB. The rest of this article is organized as follows. Section II discusses the proposed RX structure with a parallel preselect filter. Section III describes the feedback network and the theory behind it. Circuit implementation is elaborated in Section IV. The measurement results are shown in Section V, and Section VI concludes the article.

II. PROPOSED RX STRUCTURE

Fig. 1(a) shows a simplified block diagram of a conventional current-mode RX in which the LNTA converts the RF input voltage into an RF current. Passive mixers down-convert the LNTA's RF current, and the transimpedance amplifier (TIA) eventually converts it into a BB voltage. For simplicity, as shown in Fig. 1(a), the input matching is provided by an ideal 50 Ω shunt resistor (R_m) at the RX input. Moreover, a notch filter is placed in the feedback of the LNTA to provide

RF selectivity in conventional LNTA-based RXs [17], [18], [19], [20], [21], [22], [23], [24]. Through the Miller theorem, the RX's input impedance can be calculated by

$$Z_{IN} = \frac{1}{G_{M1}} + \frac{Z_N}{1 + G_{M1}Z_L}, \quad Z_L = r_{o1} \parallel Z_{RF} \quad (1)$$

where Z_N is the equivalent impedance of the notch filter. Furthermore, G_{M1} and r_{o1} denote the transconductance and output resistance of the LNTA, respectively, and Z_{RF} is the impedance seen from the input port of the passive mixers [see Fig. 1(a)]. Transparency of the passive mixers up-converts the TIA's low-pass input impedance to a bandpass impedance at RF frequencies. Based on the method presented [30], the up-converted BB impedance can be approximated as

$$Z_{RF} \approx R_{ON} + \frac{Z_{BB}(\omega - \omega_{LO})}{M} \quad (2)$$

where Z_{BB} is the input impedance of the TIA, ω_{LO} is the LO frequency, and M is the number of nonoverlapping LO phases. In current-mode RXs, Z_{RF} usually has a small value to sink the RF current of the LNTA (i.e., $Z_{RF} \ll r_{o1}$). Hence, the LNTA's voltage gain can be approximated by $G_M Z_{RF}$. In other words, TIA's low input impedance loads LNTA, thus reducing the voltage swing at the LNTA's output which improves the in-band linearity of the RX.

Note that the second term in (1) is frequency-dependent and defines the transition slope from the in-band frequencies to the out-of-band frequencies. Around the operating frequency, the notch filter is open; thus, the LNTA current is absorbed by the TIA. However, the notch filter shorts the LNTA's input and output ports at high offset frequencies, improving the RX's

out-of-band linearity. Hence, the filtering order of the notch filter is directly seen at the input impedance of the RX.

As mentioned earlier, sharp filtering is required to attenuate the -15 dBm close-in blocker in the base station applications. To improve the RF selectivity, one can increase the notch-filter order. However, when Z_N is replaced with an ideal LC-based third-order notch filter [see Fig. 1(a)], the simulated transfer functions of the input voltage gain G_{IN} and $Z_{IN} \parallel R_m$ are not optimal, as their roll-offs are smaller than the ideal -60 dB/dec, as can be gathered from Fig. 1(c) and (d). The reason behind this degradation can be intuitively explained as follows. The load of the LNTA, Z_{RF} , has a bandpass shape, and the LNTA's voltage gain drops with a -20 dB/dec slope. Hence, the effective filtering shape and slope at the RX's input are corrupted by the notch filter interaction with the LNTA's voltage gain at out-of-band frequencies. To solve this issue, we need to exempt the LNTA from RF filtering at the RX input by removing the notch filter from its feedback at the cost of lower far-out blocker rejection at the LNTA's output. Then, RF filtering should be achieved using another technique.

A. Parallel Preselect Filter

A preselect filter can be adopted to improve the RF selectivity of the LNTA-based RXs. The preselect filter can be placed in series [27], [28], or parallel [31] with the RX input. The series implementation degrades the NF of the entire receive chain. Unlike series preselect filters [27], [28], the parallel preselect filter can be turned off to reduce the power consumption and improve the NF in the absence of blockers. An N -path filter can serve as a parallel preselect filter [31]. However, the filtering order of the N -path filter is only first-order [31], and the amount of attenuation for the close-in blockers of the base station application is negligible. High-order mixer-first RXs [12], [13], [14] can also be used in parallel with the RX input to provide RF filtering. However, mixer-first RXs require a large input capacitor at the TIAs' inputs to sink the blocker current and improve the out-of-band linearity, thus substantially increasing the chip area. Moreover, at far-out offset frequencies, the input impedance of the RX is related to R_{ON} of the switches. Hence, large switches are required to provide enough filtering for the large blockers of the co-location applications, demanding high dynamic power consumption.

To solve the issues mentioned above, we propose adding a high-order parallel preselect filter at the RX input. As depicted in Fig. 1(b), the parallel preselect filter comprises a transconductance stage and a notch filter. Now, the RX's input impedance can be rewritten as

$$Z_{IN} = \frac{1}{G_{M,P}} + \frac{Z_N}{1 + G_{M,P}r_{o,P}} \quad (3)$$

where $G_{M,P}$ and $r_{o,P}$ are, respectively, the transconductance and the output resistance of the parallel preselect filter. As can be deduced from (3), the voltage gain of the parallel preselect filter is constant over frequency, and the frequency-dependent part of the RX's input impedance is only related to Z_N . Hence, if one replaces Z_N with the same LC-based third-order notch filter, the RF selectivity at the RX's input will be

third-order [see the simulation results in Fig. 1(c) and (d)]. The parallel preselect filter plays two roles in the proposed RX structure. First, it provides sharp filtering at the RX input to attenuate close-in blockers. At far-out frequencies, since the notch filter is short, the input impedance of the RX becomes $1/G_{M,P}$. Hence, its second task is to sink the blocker current at far-out offset frequencies, thus relaxing the LNTA linearity requirements [see Fig. 1(b)]. Compared with the case of using high-order mixer-first RXs [12], [13], [14] as the parallel preselect filter, the far-out input impedance of the proposed RX is reduced by raising the dc power consumption of the transconductance stage (i.e., via increasing $G_{M,P}$) instead of consuming more dynamic power in LO buffers to drive enormous low- R_{ON} switches. Moreover, the proposed structure does not need any BB TIAs. Consequently, depending on the technology node, for the same amount of far-out input impedance and filtering order, the proposed parallel preselect filter would be more power-efficient, especially at higher operating frequencies and bandwidths.

It is instructive to compare the performance of the conventional RX in Fig. 1(a) and the proposed RX in Fig. 1(b) when they consume the same power in the front-end components (i.e., $G_{M1} = 2G_M$, $G_{M2} = G_M$, and $G_{M,P} = G_M$) and exhibit the same in-band gain and linearity. The conventional RX would offer a lower NF since the front-end noise factor increases from $1/(2G_MR_s)$ to $1/(G_MR_s)$ for the proposed structure, as quantified in Appendix A. The conventional RX would also show a higher out-of-band linearity for far-out blockers, since its input impedance would be $2\times$ lower at far-out frequencies, as can be gathered from the first terms in (1) and (3). However, the values of mixers' ON-resistance and TIA feedback resistor, R_F , in the conventional RX must be $2\times$ lower to show the same in-band gain and linearity compared with the proposed RX. This demands $2\times$ more power consumption for driving the main mixers and occupying a $2\times$ larger area for implementing TIA's feedback capacitance, C_F , to keep the RX bandwidth the same. More importantly, as discussed in the previous paragraph and can be gathered from Fig. 1(c) and (d), the proposed RX maintains the filtering shape and slope and offers much better out-of-band linearity for the close-in blockers, making it more suitable for our application.

B. Implementation of the Parallel Preselect Filter

The next step is to realize Z_N with a tunable third-order notch filter. We propose to use a third-order high-pass filter and translate its impedance to RF frequency using the transparency of the passive mixers, as shown in Fig. 2(a). The third-order high-pass filter mainly comprises two series capacitors (C_H) and one shunt inductor (L_H).

When the switches of one of the high-pass filter branches are on, a current proportional to the out-of-band blockers flows through the corresponding inductor. However, when the switches are turned off, the inductor current cannot abruptly go to zero; thus, a parallel capacitance, C_P , is intentionally added to provide a return path for the inductor current. To solve this problem while maintaining the filtering shape and order,

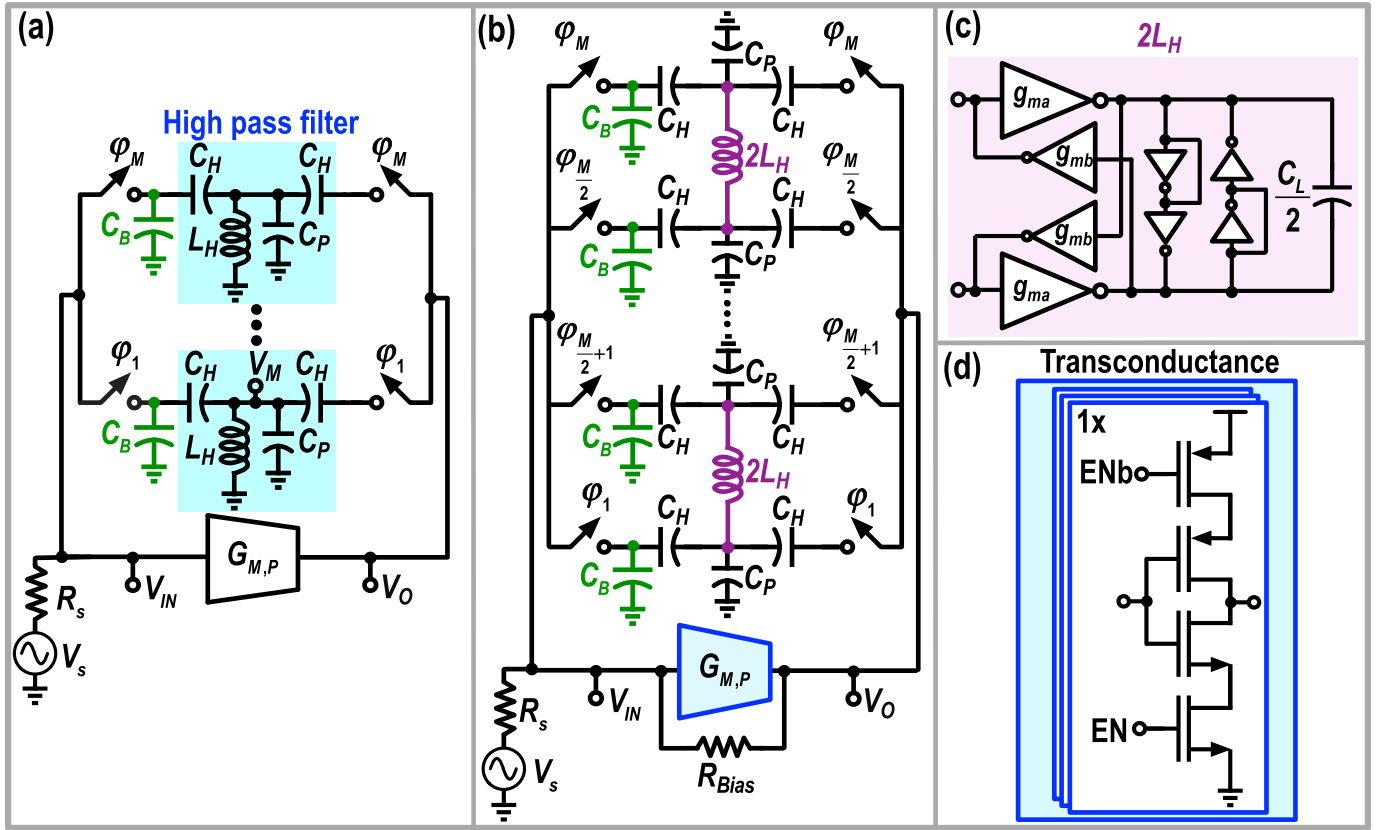


Fig. 2. (a) Initial schematic and (b) final implementation of the proposed parallel preselect filter using impedance up-conversion of a third-order high-pass filter. (c) Implementation of the BB inductor using active gyrator. (d) Schematic of the parallel preselect filter's transconductance.

C_P and L_H must resonate at a frequency higher than the desired BB bandwidth, but lower than the minimum LO frequency. In the presence of large blockers at far-out frequencies, a large voltage appears at the BB port of the switches, disrupting the parallel preselect filter operation due to the switch failures. Consequently, as shown in Fig. 2(a), M shunt capacitors (C_B) are added at the source terminal of the switches to further attenuate the far-out blockers at those nodes, thus improving the out-of-band B_{1dB} without affecting the parallel preselect filter bandwidth and roll-off.

Fig. 2(b) shows the final implementation of the parallel preselect filter. To implement the BB inductors, the ground ports of the inductors which are driven by 180° out-of-phase clocks (i.e., j_i and $j_{i+M/2}$ where $i = 1, \dots, M/2$) are connected, and then they are replaced with one inductor. As shown in Fig. 2(c), the resulting inductor can be easily realized using a gyrator with a load capacitor. This way, C_P is implicitly realized by the gyrator's parasitic capacitance. The same bias circuit as in [36] is also used to keep the common-mode voltage of the gyrator's input and output nodes around $V_{DD}/2$.

The transconductance of the parallel preselect filter is implemented using an inverter [see Fig. 2(d)]. The inverter is sliced into three parts for measurement purposes and can be controlled through a serial peripheral interface (SPI). As illustrated in Fig. 2(b), a bias resistor (R_{Bias}) is placed in the transconductance feedback to bias the inverter around $V_{DD}/2$.

C. Design Guide for the Parallel Preselect Filter

This section develops a general design guide for determining the values of different components (i.e., $G_{M,P}$, R_{ON} , C_H , and L_H) of the proposed preselect filter based on high-level system specifications, such as the required 3-dB bandwidth (ω_{3dB}) and B_{1dB} , and some circuit-level constraints like the main RX input 1-dB compression voltage for out-of-band blockers ($V_{IN,B}$) and the transconductance output 1-dB compression voltage ($V_{O,B}$). In this analysis, we assume that the main RX provides the input matching; the notch filter does not load the transconductance around ω_{LO} ; and the effect of C_P and C_B on ω_{3dB} is negligible.

The design guide starts with $G_{M,P}$ estimation. At far-out frequencies, the preselect filter's input impedance is approximately $1/G_{M,P}$, and consequently, the transconductance's input voltage can be calculated by

$$V_{IN} = \frac{V_{s,B}}{1 + G_{M,P} R_s} \quad (4)$$

where $V_{s,B}$ is the co-location blocker voltage, estimated by

$$V_{s,B} = \sqrt{8R_s \times 10^{\frac{B_{1dB}}{10}}}. \quad (5)$$

To tolerate the co-location blocker, we need to satisfy $V_{IN} \leq V_{IN,B}$, hence

$$G_{M,P} \geq \frac{1}{R_s} \left(\frac{\sqrt{8R_s \times 10^{\frac{B_{1dB}}{10}}}}{V_{IN,B}} - 1 \right). \quad (6)$$

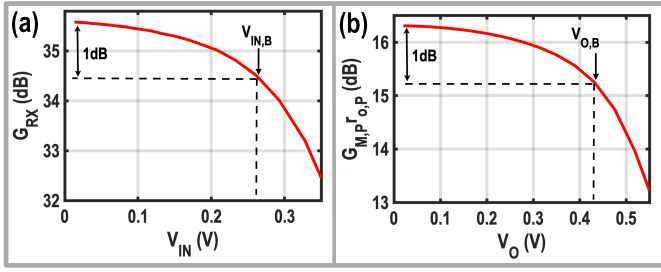


Fig. 3. (a) Simulated main RX gain versus the input voltage created by an out-of-band blocker. (b) Simulated transconductance gain versus its output voltage swing.

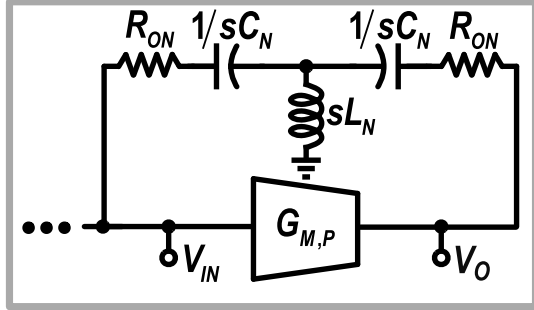


Fig. 4. Simplified model of the parallel preselect filter.

Considering $B_{1dB} = +8$ dBm and $V_{IN,B} = 0.26$ V [see Fig. 3(a)], the required $G_{M,P}$ to satisfy this blocker is ~ 105 mS.

At high offset frequencies from ω_{LO} , C_H and L_H exhibit very low and high impedances, respectively. Thus, the voltage gain of the transconductance can be estimated by $2R_{ON}G_{M,P} - 1$. To tolerate the co-location blocker voltage at the output of the preselect filter, the following condition must be satisfied:

$$R_{ON} \leq \frac{1}{2G_{M,P}} \times \left(\frac{V_{O,B}(1 + G_{M,P}R_S)}{\sqrt{8R_S \times 10^{\frac{B_{1dB}}{10}}}} + 1 \right). \quad (7)$$

Considering $V_{O,B} = 0.43$ V [see the simulation result in Fig. 3(b)], the maximum value of R_{ON} should be 12.5Ω to satisfy the required B_{1dB} of the 3rd generation partnership project (3GPP) applications.

Since the passive mixers up-convert BB impedances into the RF frequencies, the parallel preselect filter in Fig. 2(a) can be modeled with the circuit depicted in Fig. 4. Using the same method presented in [30], the third-order high-pass filters are replaced with $1/sC_N$ and sL_N , where $s = j(\omega - \omega_{LO})$ and C_N and L_N can be calculated by

$$C_N \approx \frac{M \cdot C_H}{\text{sinc}^2\left(\frac{\pi}{M}\right)} \quad (8)$$

$$L_N \approx \text{sinc}^2\left(\frac{\pi}{M}\right) \frac{L_H}{M}. \quad (9)$$

The next step is calculating C_H and L_H based on the ω_{3dB} requirement of the 5G applications. In this regard, the input

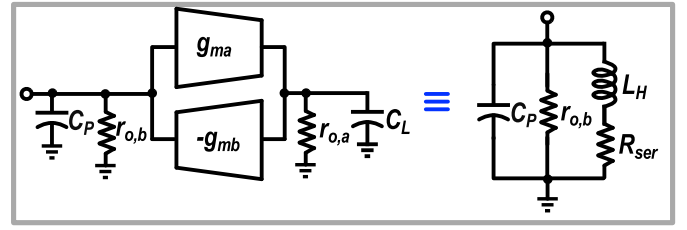


Fig. 5. Gyrator schematic with its equivalent lumped-element model.

transfer function at the RX input is derived as

$$G_{IN} = \frac{1}{2} \frac{2 \frac{s^2}{\omega_N^2} + 1}{\frac{s^3}{\omega_N^3 \omega_P} + 2 \frac{s^2}{\omega_N^2} + \frac{s}{(1 + G_{M,P}r_{o,P})\omega_P} + 1} \quad (10)$$

where ω_N and ω_P are $1/(L_N C_N)^{(1/2)}$ and $2/(R_S C_N (1 + G_{M,P}r_{o,P}))$, respectively. Note that the effect of passive mixers' R_{ON} is neglected in this calculation.

As can be inferred from (10), G_{IN} has two zeros at $\pm \omega_N/(2)^{(1/2)}$ and two complex conjugate poles and one real pole created by the miller effect of C_N and $R_S/2$. Mathematical derivations lead to the following estimate for the 3-dB bandwidth:

$$\omega_{3dB} = \omega_P \left| \frac{1 - \frac{2}{\gamma^2}}{\frac{1}{\gamma^2} - \frac{1}{1 + G_{M,P}r_{o,P}}} \right| \approx \omega_P (\gamma^2 - 2) \quad (11)$$

where $\gamma = \omega_N/\omega_{3dB}$. Since the frequency of the zeros should lie outside ω_{3dB} , the minimum value of γ is $\sqrt{2}$. As can be gathered from (10), if a much larger value for γ is chosen, ω_{3dB} will mainly be defined by $(1 + G_{M,P}r_{o,P})\omega_P$. This means that L_N shorts the middle point of the notch filter to the ground even after ω_{3dB} , and the transfer function relies on the real pole created by C_N and $R_S/2$. Hence, the filtering slope at the RX input becomes first-order, and the benefit of the proposed structure diminishes. On the contrary, choosing a value close to $\sqrt{2}$ for γ pushes the zeros toward ω_{3dB} , creating stability issues.

By substituting ω_P in (11), the values C_N and L_N may be calculated by

$$C_N = \frac{2(\gamma^2 - 2)}{\omega_{3dB}(1 + G_{M,P}r_{o,P})R_S} \quad (12)$$

$$L_N = \frac{1}{\gamma^2 \omega_{3dB}^2 C_N}. \quad (13)$$

Finally, one can determine the values of C_H and L_H from (8) and (9). As a design example, by choosing $\gamma = 1.8$, $\omega_{3dB} = 200$ MHz, $M = 8$, and an intrinsic gain of 6.5 for the transconductance, the calculated values of C_H and L_H are 2.2 pF and 350 nH, respectively. Similar values for C_H and L_H are used in the final implementation of the parallel preselect filter.

After determining L_H , the design guide concludes by investigating the tradeoffs in the L_H implementation using a gyrator with a load capacitor of $C_L/2$ [see Fig. 2(d)]. Fig. 5 shows the single-ended gyrator schematic with its equivalent lumped-element model. The gyrator is realized by a feedforward ($g_{m,a}$)

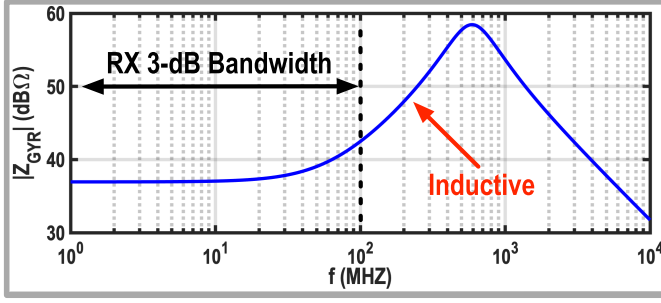


Fig. 6. Simulated input impedance of the implemented gyrator.

and a return ($g_{m,b}$) transconductance with an output resistance of $r_{o,a}$ and $r_{o,b}$, respectively. In this model, C_P is the total parasitic capacitor at the gyrator input, dominated by $g_{m,a}$ input capacitor. As can be gathered from the lumped-element model and the simulation result in Fig. 6, the gyrator's input impedance at low frequencies is limited by an undesired series resistance, estimated by

$$R_{\text{ser}} = \frac{1}{g_{m,a} r_{o,a} g_{m,b}}. \quad (14)$$

To minimize R_{ser} , the intrinsic gain of $g_{m,a}$ and the value of $g_{m,b}$ should be maximized. Hence, using long-channel devices for $g_{m,a}$ implementation and the minimum channel length transistors for $g_{m,b}$ realization is beneficial.

Beyond a cutoff frequency of $\omega_{\text{ser}} = R_{\text{ser}}/L_H$, the gyrator's input impedance becomes inductive with a value of

$$L_H = \frac{C_L}{g_{m,a} g_{m,b}}. \quad (15)$$

Since the effect of gyrator noise on the RX NF is negligible, (15) suggests choosing smaller values for C_L , and $g_{m,a}$ to optimize the chip area and power consumption. Note that ω_{ser} should be safely smaller than $\omega_{3\text{dB}}$ to ensure sharp filtering order at the RX input, resulting in a required minimum output resistance for the feedforward transconductance

$$r_{o,a} = \frac{1}{C_L \omega_{3\text{dB}}}. \quad (16)$$

L_H eventually resonates with C_P at a self-resonance frequency of

$$\omega_{\text{SRF}} = \frac{1}{\sqrt{C_P L_H}}. \quad (17)$$

Beyond ω_{SRF} , the gyrator's input impedance becomes capacitive, and the filtering slope drops dramatically, as will be demonstrated in the measurement results. This means to maintain the filtering order over a wider frequency range, C_P must be minimized by realizing $g_{m,a}$ with the minimum channel length transistors. However, according to (14), this will increase R_{ser} , affecting the filtering shape at the passband edges. Consequently, there is a tradeoff between R_{ser} and gyrator bandwidth.

III. TRANSLATIONAL FEEDBACK NETWORK

A. Input Matching in Current-Mode RXs

In voltage-mode RXs, a resistor with a value of $R_s \times G_{\text{LNA}}$ (G_{LNA} : LNA's voltage gain) is usually placed in the LNA

feedback to provide the input matching [37]. However, since the LNTA gain is small in current-mode RXs, the feedback resistor must be significantly reduced, thus degrading the RX's NF. To decouple input matching from the LNTA's gain, as highlighted in purple shown in Fig. 7(a), a translational feedback network [38], [39], [40] is adopted here by up-converting BB signals at TIAs' outputs and feeding them back to the RX input through a matching resistor (R_m) and an ac coupling capacitor (C_m). Due to the effective use of the RX voltage gain (A_0), the R_m value increases to $R_s \times A_0$, thus contributing negligibly to the RX's NF. Note that A_0 has a positive sign; thus, -1 multiplication is required in the translational feedback network to avoid positive feedback.

B. Delay of the Transconductance

In the preselect filter, the transconductance stage has a delay, which introduces an undesired phase shift in the current passing through the notch filter, thus changing the input impedance at the passband edges in opposite directions and creating a negative center frequency shift and a gain peaking at the lower edge of the passband, as shown in Fig. 7(b). To analyze this phenomenon without any loss of generality, we assume that the notch filter is a simple first-order notch filter composed of an up-converted capacitor and a parallel resistor [i.e., $j(\omega - \omega_{\text{LO}})C_N$ and R_N in Fig. 7(a)]. In this simplified case, the transfer function at the RX input is $G_{\text{IN}} = Z_{\text{IN}}/(Z_{\text{IN}} + R_s)$, in which

$$Z_{\text{IN}} \approx R_s \parallel \frac{Z_N}{G_{M,PRo,P}} \times e^{j\omega t_d} \quad (18)$$

and t_d is the delay of the transconductance. In the derivation of (18), it is assumed that the input impedance of the parallel preselect filter is the Miller effect of Z_N , and the voltage gain of the parallel preselect filter, $G_{M,PRo,P}$, is much higher than one. By setting $d|G_{\text{IN}}|^2/d\omega = 0$, the shifted center frequency can be derived by

$$\begin{aligned} \omega_{\text{peak},n} &\approx \omega_{\text{LO}} \left(1 - \frac{2t_d}{G_{M,PRo,P} R_s C_N} \right) \\ &\approx \omega_{\text{LO}} \left(1 - \frac{\omega_{3\text{dB}} t_d}{2} \right). \end{aligned} \quad (19)$$

As indicated in (19), the amount of the frequency shift is much more severe in high bandwidth applications, such as 5G. For example, with $G_{M,PRo,P} = 6$, $R_s = 50 \Omega$, $C_N = 8 \text{ pF}$, $t_d = 20 \text{ ps}$, and $f_{\text{LO}} = 2 \text{ GHz}$, (19) estimates that the center frequency shifts to 1.967 GHz, while the simulation result in Fig. 8 shows that the center frequency lies at 1.962 GHz. Consequently, the simulation result is in good agreement with the presented calculations. To solve this issue, a polyphase notch filter has been proposed [17], [18], which requires M extra amplifiers to share the in-phase (I) and quadrature (Q) signals to compensate for the LNTA delay. However, these extra amplifiers should handle the large blockers in co-location applications, demanding substantial power consumption.

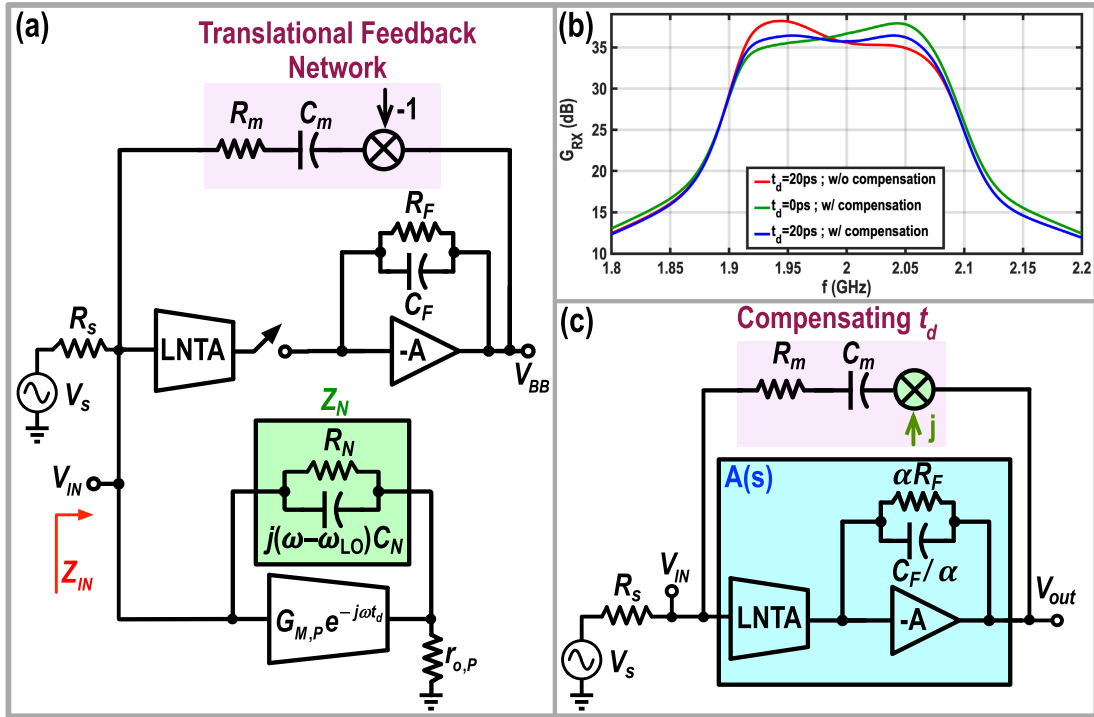


Fig. 7. (a) Simplified block diagram of the proposed RX with a conventional translation loop for providing the input matching (for the sake of simplicity, Z_N is replaced by a first-order notch filter). (b) Simulated G_{RX} in different scenarios. (c) Simplified block diagram of the main RX path with the proposed translational feedback network for compensating the side effects of parallel preselect filter delay.

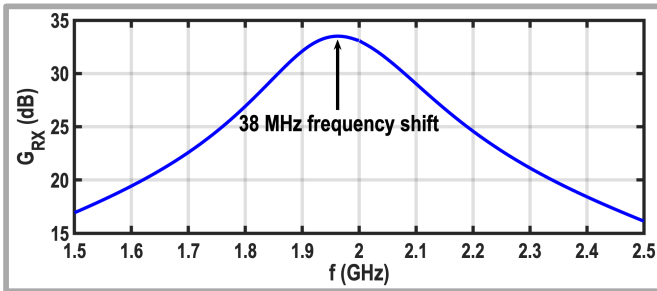


Fig. 8. Simulated gain of Fig. 7(a) RX with $G_{M,P,r_o,P} = 6$, $R_S = 50 \Omega$, $C_N = 8 \text{ pF}$, $t_d = 20 \text{ ps}$, and $f_{LO} = 2 \text{ GHz}$.

C. Proposed Translational Feedback Network

To compensate for the negative center frequency shift caused by the transconductance delay, we propose to intentionally realize a positive center frequency shift in the main RX path. Consequently, as shown in Fig. 7(c), “-1” multiplication is replaced with “j” multiplication in the translational loop to accomplish this goal. To calculate the induced frequency shift and for the sake of simplicity, the main RX path is modeled with a bandpass amplifier

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_{P1}}} \bigg|_{s=j(\omega-\omega_{LO})} \quad (20)$$

where ω_{P1} is the dominant pole of the amplifier and equals to $1/(R_F C_F)$. Moreover, A_0 can be approximated by $\alpha G_M R_F$, in which α is $\text{sinc}^2(\pi/M)/M$ [41]. The amplifier has its maximum gain at ω_{LO} , and the gain drops with a first-order slope at out-of-band frequencies. The transfer function of the

RX from the source (V_s) to the TIAs’ outputs (V_{out}) can be derived as follows:

$$\frac{V_{out}}{V_s} = \frac{A_0}{1 + \frac{\omega R_m C_m}{1 + (\omega R_m C_m)^2} + j \left(\frac{\omega - \omega_{LO}}{\omega_{P1}} - \frac{(\omega R_m C_m)^2}{1 + (\omega R_m C_m)^2} \right)}. \quad (21)$$

In the derivation of (21), R_m is assumed to be $(1 + A_0) \times R_s$ to satisfy the input matching requirements. By setting $d|V_{out}/V_s|^2/d\omega = 0$, the center frequency of the main RX path can be estimated by

$$\omega_{\text{peak},p} \approx \omega_{LO} + \omega_{P1} \times \frac{\omega_{LO}^2 R_m^2 C_m^2}{1 + \omega_{LO}^2 R_m^2 C_m^2}. \quad (22)$$

Consequently, the proposed technique shifts the passband center toward higher frequencies, and the amount of the frequency shift can be controlled by adjusting C_m without affecting other RX’s characteristics. In the above analysis, it is assumed that the signal in the main RX path does not experience any delay for the sake of simplicity. In Appendix B, the center frequency of the main RX path is recalculated by considering the delay of the main RX path, $t_{d,RX}$. The main conclusions remain the same, but a larger C_m is needed to also compensate for $t_{d,RX}$. As displayed in the green curve in Fig. 7(b), when the preselect filter transconductance is replaced with an ideal component with no delay, the proposed translational loop changes the simulated RX transfer function by realizing a positive center frequency shift and a gain peaking at the upper edge of the passband. When the transconductance is implemented using real devices, the peak created by the translational feedback network cancels out the peak on the lower side, and a flat gain response can be achieved, as shown in the blue curve in Fig. 7(b).

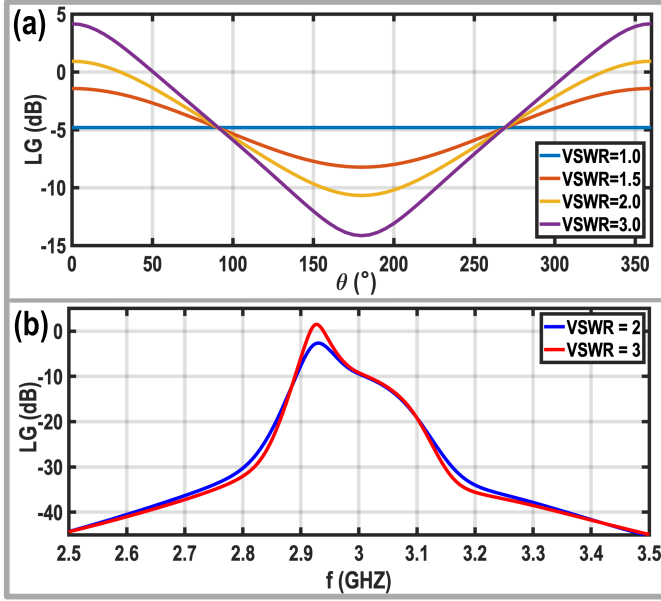


Fig. 9. (a) Simulated loop gain versus the angle of the reflection coefficient for different VSWR values, using (23) and considering $f_{LO} = 3$ GHz and $C_m = 300$ fF. (b) Simulated loop gain of the implemented RX for VSWR = 2 ($Z_s = 100 \Omega$) and 3 ($Z_s = 150 \Omega$).

To ensure that the proposed translational loop does not sacrifice the RX stability, the RX loop gain, LG, in the simplified model is calculated

$$LG = \frac{j A_0 Z_s}{R_m + Z_s + \frac{1}{j\omega C_m}} \quad (23)$$

where Z_s is the antenna source impedance. To satisfy the input matching, R_m should equal $(1 + A_0) \times 50 \Omega$. Therefore, (23) can be simplified to

$$LG = \frac{j A_0 Z_s}{Z_s + 50 \times (1 + A_0) + \frac{1}{j\omega C_m}}. \quad (24)$$

When $Z_s = 50 \Omega$, even in the worst case scenario, in which the C_m impedance becomes much smaller than R_m , the loop gain reaches $(A_0/2 + A_0) < 1$, proving that the proposed translational network will not cause any stability issues. However, in practice, the antenna's impedance varies from its ideal value. Fig. 9(a) shows the loop gain versus the angle of the reflection coefficient (θ) for different voltage standing wave ratios (VSWRs), using (23) and considering $f_{LO} = 3$ GHz and $C_m = 300$ fF. Based on (23) estimation, the loop gain exceeds one for $VSWR \geq 2$ at $\theta \approx 0$, where the antenna impedance is almost purely resistive and considerably larger than 50Ω . To verify the presented analysis, the loop gain of the entire RX chain is also simulated in Cadence using "PSS" and "PSTB," and the results are shown in Fig. 9(b) for VSWR = 2 and 3. The loop gain of the RX chain is slightly lower than 0 dB, proving that the translational feedback network is stable for $VSWR \leq 2$.

IV. CIRCUIT IMPLEMENTATION

Fig. 10 shows the complete block diagram of the LO generation unit. After the ON-chip 50Ω termination resistors,

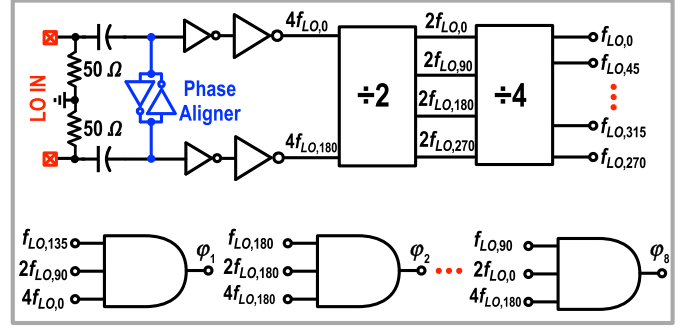


Fig. 10. Block diagram of the LO generation circuit [17].

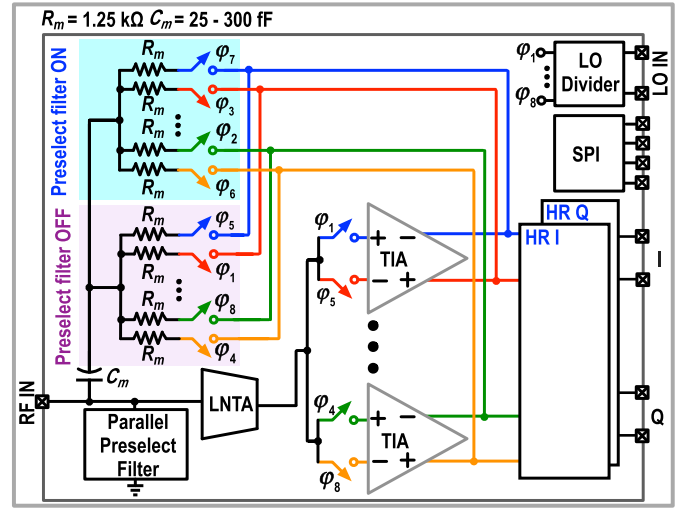
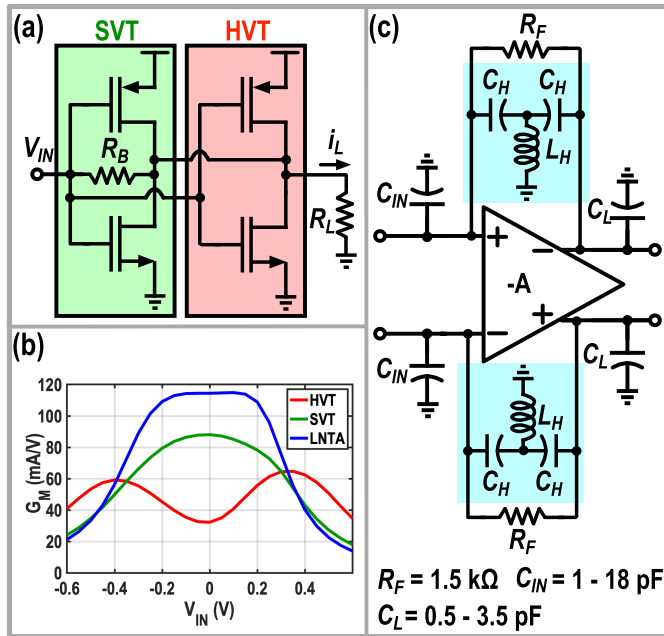
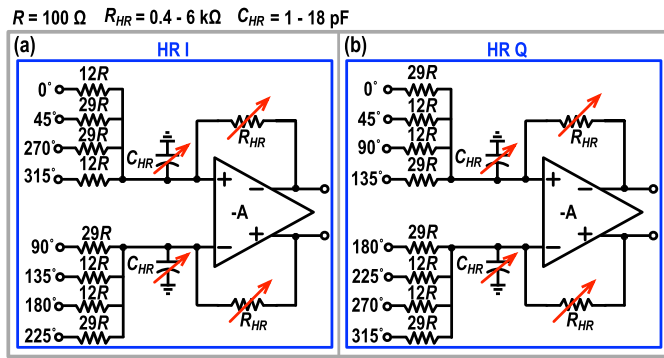


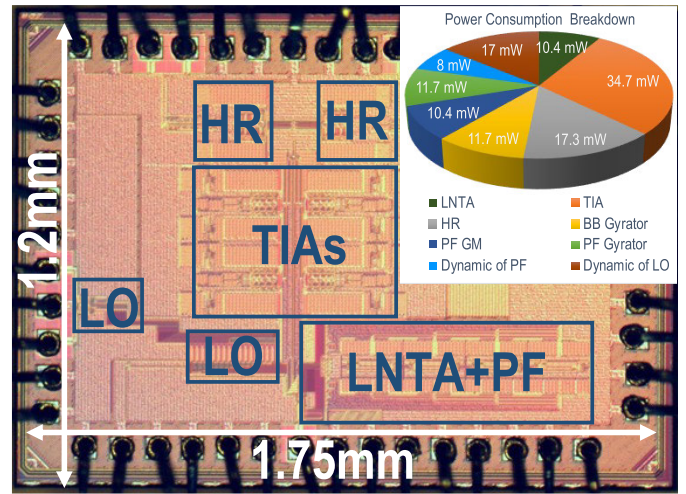
Fig. 11. Complete block diagram of the proposed RX.

a phase aligner is used at the input of the LO generation to compensate for any phase and amplitude imbalance of the incoming differential OFF-chip clock. Then, OFF-chip LO is buffered and applied to a divide-by-two followed by a divide-by-four stage. Finally, the divide-by-four outputs are resampled with the outputs of the input buffer and the divide-by-two to generate nonoverlapping LOs with minimum phase noise penalty, as described in [17].

Fig. 11 shows the complete block diagram of the proposed RX. SPI has been used to configure the chip in the linear and low-noise mode and to control all the tunable components. The RF input signal is converted into an RF current by the LNTA, and then the RF current is down-converted into a BB current using passive mixers. The TIA converts the BB input current into a BB output voltage. Harmonic rejection (HR) [42] combines the output voltages of the TIAs to generate the BB I and Q signals. As illustrated in Fig. 12(a) and (b), like in [18], the ratio of resistors is used to implement the $1 + \sqrt{2}$ scaling factor needed for the HR. An input capacitor (C_{HR}) is placed at the HR amplifier to absorb the out-of-band blocker current, thus relaxing the requirements of the HR amplifier. Since the voltage gain of the TIA is used to provide input matching, the RX voltage gain is only controlled by the tunable feedback resistor of the HR amplifier (i.e., R_{HR}).



The RX out-of-band linearity performance is mainly determined by the LNTA. Hence, the LNTA should be able to handle the voltage swing created by large out-of-band blockers and stay linear. Fig. 13(a) depicts the schematic of



Since the TIA converts the BB current into a BB voltage, a voltage swing will appear at its output. The close-in blockers of the base station applications create a large voltage swing at the output of the TIA, saturating its amplifier. Hence, it is desirable to also have sharp filtering at the output of the TIA. As shown in Fig. 13(c), a third-order high-pass impedance is also placed in the TIA's feedback to provide sharp filtering at the output of the TIA. Like the parallel preselect filter, BB inductors of the TIA are also implemented using a gyrator. The values of C_H and L_H here are similar to those used in the parallel preselect filter. Finally, a common-mode feedback similar to [44] is used to keep the dc bias of the TIA output around $V_{DD}/2$.

The proposed RX was fabricated in TSMC 40-nm technology. As shown in Fig. 14, the fabricated prototype occupies $1.2 \times 1.75 \text{ mm}^2$, while the core area of the chip is 0.8 mm^2 . The power consumption of the different blocks is summarized in Fig. 14 when the LO frequency is 1.5 GHz. The proposed RX was directly bond-wired on a four-layer FR4 printed circuit board (PCB). Fig. 15 shows the measurement setup. Keysight NF analyzer (N8973A) and network analyzer (P9375A) were used to, respectively, measure the NF and the input matching of the proposed RX. Keysight Infiniium (MSOS804A) with embedded 10-b ENOB analog-to-digital

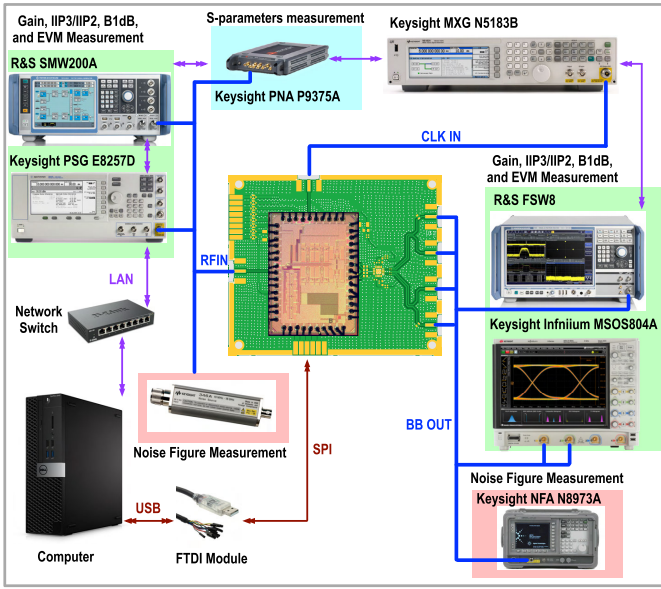
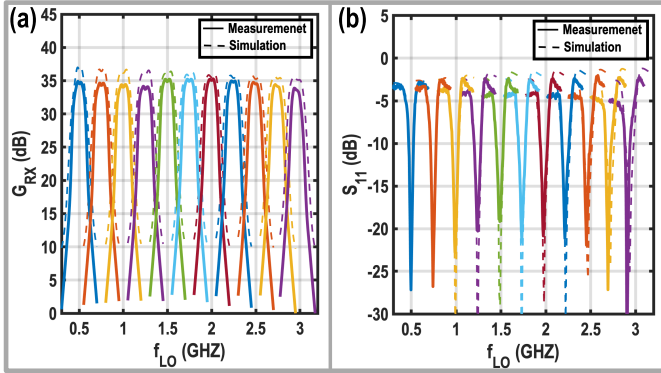


Fig. 15. Measurement setup.

Fig. 16. Measured (a) RX gain and (b) S_{11} over operating frequency.

converters (ADCs) was used to capture the BB output of the chips for the error vector magnitude (EVM) measurements and 3GPP requirements. For the linearity and gain measurements, an R&S signal analyzer (FSW8) was used.

A. Wideband Operation

As shown in Fig. 16(a), the proposed RX is functional from 0.5 to 3 GHz. The RX gain is 34.5 dB at 0.5-GHz LO frequency, and it reduces to 33.5 dB at 3 GHz due to the parasitic input capacitance of the RX. Moreover, the measured 3-dB bandwidth of the proposed RX is about 150 MHz. Fig. 16(b) shows the measured S_{11} over the operating frequency range. The bandwidth in which S_{11} remains below -10 dB is $\sim 40\%$ lower than the RX 3-dB bandwidth. As mentioned earlier, the input matching is provided by the Miller effect of R_m . Due to RX channel selectivity, the RX's voltage gain reduces near the passband edges, increasing the RX input impedance and degrading S_{11} , as also discussed in [45].

The measured NF is depicted in Fig. 17(a) versus the LO frequency. In the low-noise mode, the NF is 2.6 dB at 0.5-GHz LO frequency and increases to 3.9 dB at the maximum

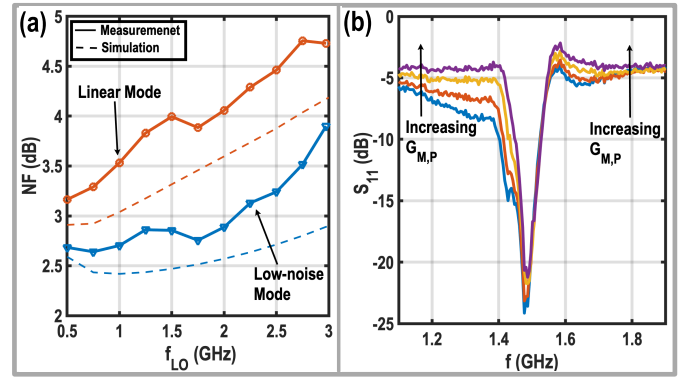
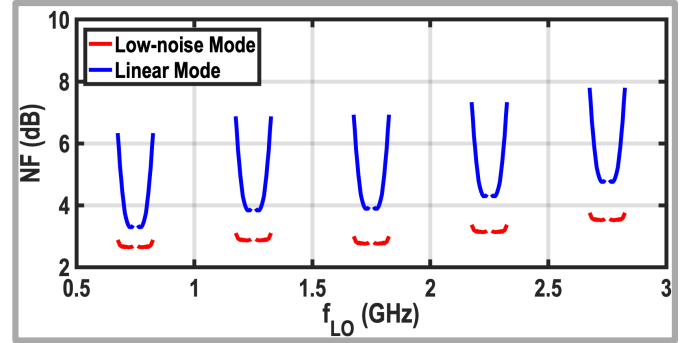
Fig. 17. Measured (a) NF versus the LO frequency and (b) S_{11} for different $G_{M,P}$ values at 1.5-GHz LO frequency.

Fig. 18. Measured NF versus the BB frequency for different LO frequencies.

LO frequency. In the worst case, the parallel preselect filter degrades the NF by 1.2 dB compared with the low-noise mode. As predicted by (3) and illustrated in Fig. 17(b), increasing $G_{M,P}$ reduces the input impedance of the RX at the out-of-band frequencies, and therefore, S_{11} reaches -4 dB for the maximum $G_{M,P}$, thus reflecting blocker at those frequencies. Fig. 18 shows the measured in-band NF versus the BB frequency for different LO frequencies. The NF is measured for the BB frequencies above 10 MHz due to the limitation of our instrument, Keysight N8974A. In the linear mode, the NF degrades near the passband edges for two reasons. First, as explained in the previous paragraph, the RX input impedance increases in those regions. Second, as shown in Appendix A, the noise penalty of the parallel preselect filter is proportional to $(R_S/(R_{Bias}||Z_N))^2$. At low BB frequencies, by choosing R_{Bias} big enough, this noise penalty can be ignored. However, as the BB frequency increases, Z_N drops below R_{Bias} , thus making the noise penalty of the parallel preselect filter visible around the bandwidth edges.

Fig. 19(a) shows the RX transfer function and filtering order in three different scenarios. In case-1, the parallel preselect filter and the BB inductors in the TIAs are disabled. Hence, the system just relies on the single real pole of the TIAs, showing only ~ -20 dB/dec roll-off. The BB inductors are turned on in case-2 while the parallel preselect filter is still off. In this case, the third-order high-pass filter creates complex conjugate poles, thus achieving a flat gain response and ~ -60 dB/dec roll-off. Finally, activating the parallel preselect filter realizes another third-order filtering and increases the transition

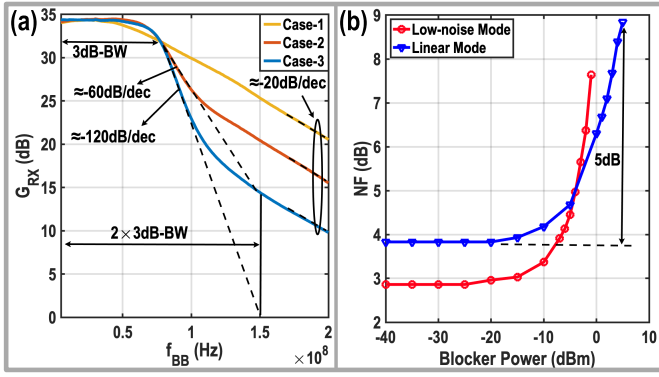


Fig. 19. (a) Channel selectivity of the proposed RX. (b) Blocker NF.

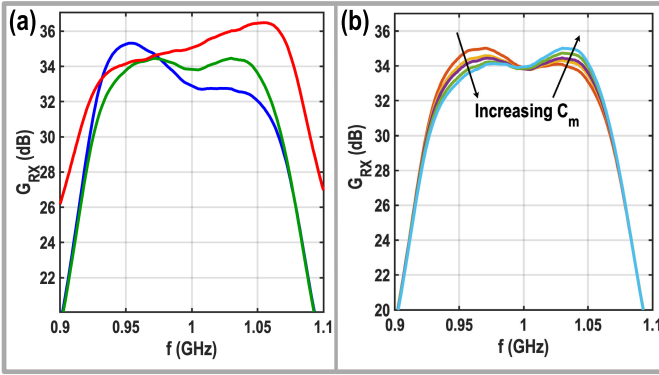


Fig. 20. (a) In-band gain response of the proposed RX in different scenarios. (b) Effect of C_m on the RX transfer function.

roll-off to ~ -120 dB/dec for close-in blockers. Due to the limited bandwidth of the BB inductors in the TIAs and parallel preselect filter, the slope of the transition band returns to ~ -20 dB/dec when the frequency exceeds the gyrators' bandwidth. The bandwidth of the BB inductors can be increased to preserve sixth-order filtering for a wider frequency range at the cost of power consumption.

The NF is also measured versus the power of the out-of-band blocker. The ratio of the blocker offset frequency to the BW_{RF} is 3.3. As depicted in Fig. 19(b), in the presence of a +5 dBm out-of-band blocker, the NF degrades only by 5 dB.

Fig. 20 shows the RX in-band gain response in different cases. When the translational feedback network is off, there is a gain peaking at the lower side of the RX operating frequency due to the delay of the preselect filter transconductance [see blue curve in Fig. 20(a)]. Then, the translational feedback network is turned on, and the parallel preselect filter is disabled. As depicted in Fig. 20(a), the translational feedback network creates another peak at the upper side of the transfer function (red curve). Finally, when both the translational feedback network and the parallel preselect filter are on, the peaks at the lower and upper sides cancel out each other. Hence, a flat gain response can be achieved, and the in-band gain ripple is below 0.5 dB [green curve in Fig. 20(a)]. As predicted by (22) and measured in Fig. 20(b), increasing the value of C_m shifts the peak frequency toward the upper side of the operating frequency.

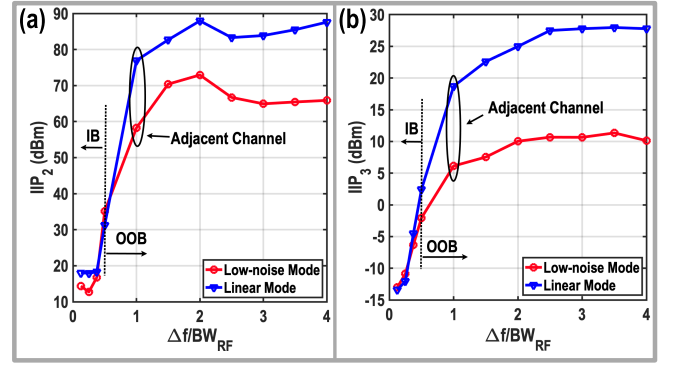


Fig. 21. Measured (a) IIP2 and (b) IIP3 versus the offset frequency normalized to the RF bandwidth.

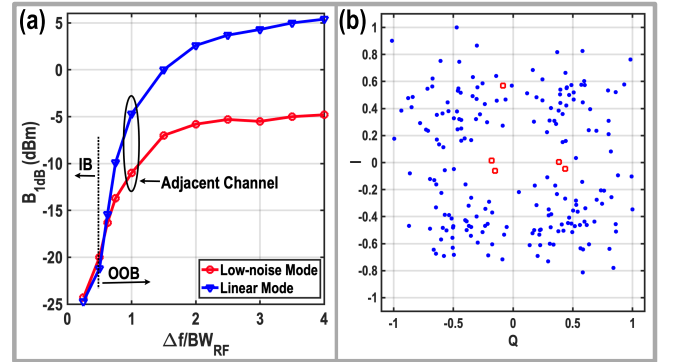


Fig. 22. (a) Measured $B_{1\text{dB}}$ versus the normalized offset frequency. (b) Measured constellation at the reference sensitivity for 100-MS/s signal (red squares represent the missed symbols).

B. Linearity Measurements

The in-band and out-of-band IIP3 and IIP2 measurements are exhibited in Fig. 21(a) and (b), respectively. The in-band IIP2 (IIP3) in the linear mode is +18 dBm (−13 dBm). Since the last gain stage of the RX limits the in-band linearity, in-band IIP2 (IIP3) for the low-noise mode is also +18 dBm (−13 dBm). For the linear mode, the out-of-band IIP2 of the proposed RX is +65 dBm. Enabling the parallel preselect filter improves the out-of-band IIP2 to +85 dBm.

The out-of-band IIP3 for the low-noise mode is +11 dBm. Moreover, in the linear mode, the out-of-band IIP3 is +28 dBm which shows a 17-dB improvement compared with the low-noise mode. The large-signal operation of the proposed RX is depicted in Fig. 22(a). An in-band blocker with −24 dBm power drops the gain of the proposed RX by 1 dB. Thanks to the sharp filtering of the proposed RX, the $B_{1\text{dB}}$ improves from −24 to −5 dBm for the adjacent channel. For the low-noise mode, the out-of-band $B_{1\text{dB}}$ of the proposed RX is −5 dBm, and enabling the preselect filter improves it to +5 dBm. The measured $B_{1\text{dB}}$ is −15.4 dBm for a close-in blocker located at the 20-MHz offset frequency. While this $B_{1\text{dB}}$ is 0.4 dB lower than the required value of the 3GPP standard, it is still good enough to satisfy the close-in blocking test of the 3GPP.

C. 3GPP Requirements

The performance of the proposed RX is also measured based on the 3GPP requirements for the microcell base station

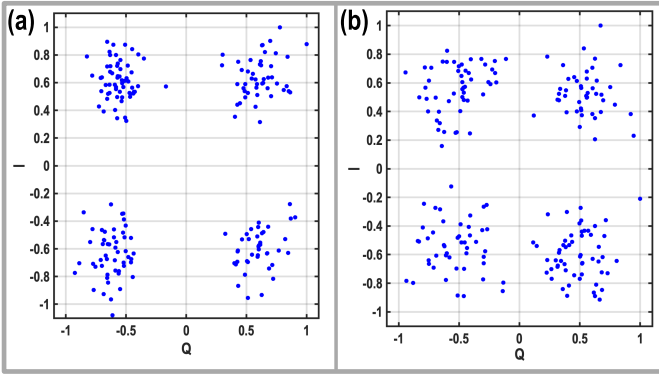


Fig. 23. Measured constellation for 100-MS/s signal: (a) in the presence of a -38 dBm in-band blocker and (b) when a -15 dBm out-of-band blocker at the 20-MHz offset frequency is applied to the RX.

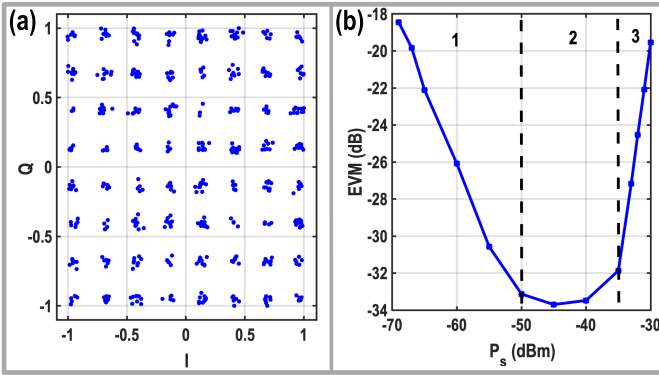


Fig. 24. (a) Measured constellation for a 100-MS/s QAM-64 -60 dBm signal. (b) Measured EVM versus the input power of the desired signal.

applications [1]. To do so, a 100-MS/s quadrature phase shift keying (QPSK) signal is applied to the input of the RX. The RX I and Q BB signals are then converted into digital by the ADC of the high-speed oscilloscope. The voltage gain of the RX assures that the quantization noise of the ADC does not degrade the SNR of the received signal. Finally, the captured BB data of the oscilloscope are postprocessed in MATLAB.

First, the reference sensitivity requirement of the 5G microcell base station is investigated. Since the power of the desired signal is low, the proposed RX is configured in the low-noise mode to ensure sub-3-dB NF. The power of the desired signal is -83.7 dBm, and hence, the SNR of the signal at the RX output is 7.5 dB (note that the NF is 2.8 dB). As shown in Fig. 22(b), the RX throughput is 97.5% for the reference sensitivity, thus satisfying the 3GPP requirement by a 2.5% margin.

Second, the RX performance is measured in the presence of an in-band blocker. In this test, the RX throughput should be better than 95%, while the power of the desired signal is 6 dB higher than the reference sensitivity and an in-band modulated blocker with 20-MHz bandwidth and -38 dBm power is present. As depicted in Fig. 23(a), since the EVM of the received signal is low enough (i.e., -11.7 dB), all the symbols are detected correctly, thus comfortably meeting the 3GPP requirement.

Third, the out-of-band blocking of the 5G microcell base station applications is investigated. A -15 dBm out-of-band blocker can be located at a 20-MHz offset frequency from the

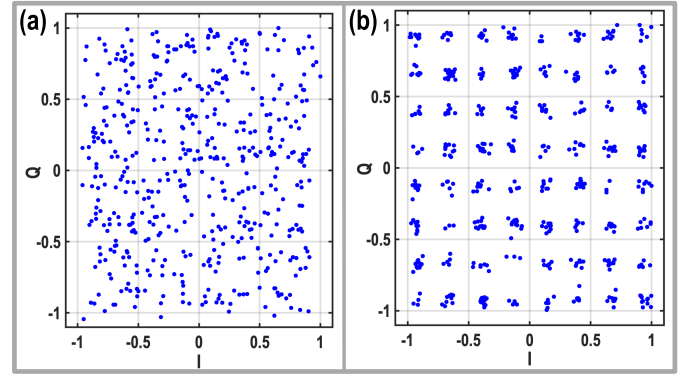


Fig. 25. Measured constellation for a 100-MS/s QAM-64 -60 dBm signal in the presence of a 0-dBm out-of-band blocker: (a) low-noise mode and (b) linear mode.

passband edge. In the presence of this blocker, sharp filtering is required to avoid gain saturation at the BB outputs of the RX. Hence, the proposed RX is configured in the linear mode. Similar to the in-band blocking scenario, the power of the desired signal is 6 dB higher than the reference sensitivity, representing 12.3-dB SNR (note that NF is 4 dB in the linear mode). As shown in Fig. 23(b), the measured EVM is -9.7 dB in this case, and the throughput is 100%.

D. High-Order QAM

In the next test, a 100-MS/s QAM-64 OFDM signal is applied to the input of the RX. As depicted in Fig. 24(a), when the power of the input signal is -60 dBm, the measured EVM is -26.3 dB (note that the RX is configured in the linear mode). Then, the EVM is plotted versus the power of the input signal, P_s , in Fig. 24(b). This curve can be divided into three regions. In region 1, the EVM is limited by the thermal noise, and increasing the signal power improves the EVM. Then, the EVM is limited by the I/Q imbalance and the phase noise of the LO in region 2. Finally, in region 3, the EVM is restricted by the distortion at the output of the RX due to limited in-band linearity. It is worth mentioning that the input signal has around a 10-dB peak to average ratio (PAPR). Hence, the high PAPR of the input signal degrades the performance of the RX for high input power signals.

In Fig. 25, the performance of the proposed RX is investigated in the presence of a 0-dBm continuous wave (CW) blocker located at a 500-MHz offset frequency from the desired -60 dBm 100-MS/s QAM-64 OFDM signal. In the low-noise mode, the out-of-band blocker saturates the LNTA, and the desired signal cannot be appropriately received [see Fig. 25(a)]. Then, the proposed RX is configured in the linear mode. As illustrated in Fig. 25(b), the measured EVM is -24.3 dB in this case, which shows only 2-dB degradation compared with the EVM of 24(a). This 2-dB degradation can also be inferred from Fig. 19(b), where the NF degrades by 2-dB in the presence of a 0-dBm blocker.

E. Performance Summary and Comparison

The performance of the proposed RX is summarized in Table I and compared with the state-of-the-art RXs. In the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RXS

	This Work		Wang JSSC 2021[16]	Razavi JSSC 2022[41]	Montazerolghaem ISSCC2021[23]	Musayev JSSC2019[45]	Kim OJSSC2022[46]	Krishnamurthy JSSC2019[14]	Pini JSSC2020[11]	Krishnamurthy SSCL2021[12]	Bu JSSC2022[42]
	Low Noise	Linear									
Architecture	LNTA Based		LNTA Based	LNTA Based	LNTA Based	LNTA Based	LNTA Based	Mixer First	Mixer First	Mixer First	Slice-Based
Technique	Preselect filter and third-order TIA		Gm boosting N-path filter	Harmonic rejecting	Programmable zeros and second-order TIA	Quantized RX	Calibrated Quantized RX	Second-order TIA	Third-order current-mode filtering	High order impedance + N-path	Filtering by aliasing
Technology	40 nm CMOS		45 nm FDSOI	28 nm	40nm CMOS	65nm CMOS	65nm CMOS	28 nm CMOS	28nm CMOS	28nm CMOS	28 nm
f_{RF} (GHz)	0.5 - 3		0.2 - 2	0.4 - 6	0.4 - 3.2	0.7 - 1.4	1.7 - 2.2	0.2 - 2	0.5 - 2	0.2 - 3.5	0.1 - 1
Gain (dB)	25-45		40	54	36	36.8	23.2	13	32.4	16.3	10
Single Ended Input	Yes		Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Supply (V)	1.3		1.2/1.6	1	1.3/1.2	0.8/1/1.2	0.4/1.2/2.5	1.2	1.8/1.2	1.4/1.2	0.9
Active Area (mm ²)	0.8		1.05	1.9	0.6	0.25	0.33	0.48	0.16	1.5	1.3
NF (dB)	2.6 - 3.9		2.1-2.5	2.1/1.4, 4.2 [§]	2.7 - 3.6	1.9	2.5	4.3 - 7.6	5.5 [§]	6.5 - 12	10.8
0dBm BNF (dB)	N/A	6.5 $\Delta f/BW_{RF} = 3.3$	6.7 $\Delta f/BW_{RF} = 4$	5.2/7.4 [§]	8.4 $\Delta f/BW_{RF} = 3.1$	6.6	5.9	6.4 $\Delta f/BW_{RF} = 5$	10 $\Delta f/BW_{RF} = 4$	9 $\Delta f/BW_{RF} = 3.1$	14 $\Delta f/BW_{RF} = 6$
In-band flatness	Yes	Yes	No	No	Yes	No	No	Yes	Yes	Yes	No
BW_{RF} (MHz)	180	150	20	0.2 - 160	160	30	80	18	260	30	5 - 20
Filtering-order (dB/dec)	-60	-120	-40	-60	-60	-20	-20	-40	-60	-80	-60 [†]
RF Selectivity (dB/dec)	N/A	-60	-20	-20	-20	N/A	N/A	-40	-20	-80	N/A
OOB IIP ₃ (dBm)	7.5 $\Delta f/BW_{RF} = 1.5$	22.6 $\Delta f/BW_{RF} = 1.5$	5 $\Delta f/BW_{RF} = 1.5$	9.8 $\Delta f/BW_{RF} = 25$	10 $\Delta f/BW_{RF} = 1.5$	1	26.1 $\Delta f/BW_{RF} = 1.5$	19 $\Delta f/BW_{RF} = 1.6$	21 $\Delta f/BW_{RF} = 1.5$	23 $\Delta f/BW_{RF} = 1.5$	30 $\Delta f/BW_{RF} = 1.5$
OOB IIP ₂ (dBm)	70.4 $\Delta f/BW_{RF} = 1.5$	82.7 $\Delta f/BW_{RF} = 1.5$	48 $\Delta f/BW_{RF} = 1.5$	30 $\Delta f/BW_{RF} = 25$	50 $\Delta f/BW_{RF} = 1.5$	35	71 $\Delta f/BW_{RF} = 2.5$	N/A	70 $\Delta f/BW_{RF} = 1.5$	N/A	82 $\Delta f/BW_{RF} = 8$
B_{1dB} (dBm)	-5 $\Delta f/BW_{RF} = 3.5$	5 $\Delta f/BW_{RF} = 3.5$	N/A	N/A	-5 $\Delta f/BW_{RF} = 2.5$	-8.5	0.5	7 $\Delta f/BW_{RF} = 1.6$	3 $\Delta f/BW_{RF} = 3$	10 $\Delta f/BW_{RF} = 2$	12.1 $\Delta f/BW_{RF} = 4$
LO Leakage (dBm) at 1GHz	-90	-76	-85	N/A	-77	N/A	N/A	N/A	N/A	N/A	-85
EVM (dB)	-27.6 [†]	-26.3 [†]	N/A	-25.3 [†]	-26.4 [§]	N/A	N/A	N/A	N/A	N/A	N/A
0dBm Blocker EVM (dB)	N/A	-24.3 [†] $\Delta f/BW_{RF} = 3.3$	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Power (mW)	74 +17mW/GHz	96 +25mW/GHz	68-95	23 - 49	58.5 +17.6 mW/GHz	14 +37.2/GHz	6.5 18.5/GHz	143 18mW/GHz	21.6 + 7.8 mW/GHz	100 mW at 1GHz	21 - 31 /Channel

[†]Low noise mode, [§] Harmonic reject mode, [‡] loss of input balun excluded, [¥] Estimated from figure, [‡] -60dBm 100MS/s 64QAM OFDM, [§] -60dBm 140MS/s 64QAM OFDM, [¶] -57dBm 80MS/s 256QAM.

low-noise mode, the proposed RX can achieve sub-3-dB NF while showing similar linearity performance compared with the other LNTA-based RXs. In the linear mode, however, it outperforms LNTA-based RXs [18], [26], [45], [47]. The LNA-based RX in [48] offers better out-of-band IIP₃, at the cost of using multiple supplies and a complex calibration scheme. Moreover, it only achieves 0.5-dBm B_{1dB} and 80-MHz RF bandwidth compared with 5 dBm and 150 MHz of the proposed RX. Compared with the mixer-first RXs [11], [13], the proposed RX achieves comparable out-of-band IIP₂ and IIP₃ while demonstrating better NF and filtering order. Filtering by aliasing RX [46] reports a better out-of-band IIP₃ but with much higher NF, lower bandwidth, and operating frequency while its passband is not flat. Moreover, the proposed RX is the only RX that reports EVM in the presence of a 0-dBm blocker.

VI. CONCLUSION

This article presents a wideband RX in the 40-nm CMOS technology for 5G microcell base station applications. Thanks to the proposed parallel preselect filter, a +5 dBm out-of-band B_{1dB} is achieved, making the proposed RX a good candidate for microcell co-location applications. Third-order RF and BB filters are used to achieve -120 dB/dec channel selectivity to satisfy the close-in blocking scenario of the base station applications. A translational feedback network is placed in the feedback of the RX to reduce the in-band gain ripple to below 0.5 dB. The proposed RX is reconfigurable, and in the low-noise mode, it can achieve sub-3-dB NF while achieving +28 dBm out-of-band IIP₃ in the linear mode. With

a -60 dBm 100 MSym/s (0.6 Gb/s) 64-QAM OFDM input signal, the RX EVM only degrades from -26.3 to -24.3 dB when facing a 0-dBm out-of-band blocker. Moreover, thanks to its current-mode operation and sharp filtering, the proposed RX meets all the in-band and out-of-band 3GPP blocking requirements.

APPENDIX A

This appendix calculates the NF of the proposed RX in Fig. 1(b) in the low-noise and linear modes. In the low-noise mode, the parallel preselect filter is off, and as explained in [44], the noise contribution of TIAs and the O_N -resistance of the mixer switches to the RX NF can be neglected due to the LNTA's high output impedance. Consequently, the NF in the low-noise mode can be estimated by

$$F_1 = \left(1 + \frac{1}{G_{M2}R_s} + \frac{R_s}{R_B}\right) \times \frac{1}{\text{sinc}^2\left(\frac{\pi}{M}\right)} \quad (25)$$

where R_B is the bias resistor of the LNTA [see Fig. 13(a)]. Typically, R_B is chosen large, and the NF is related only to $G_{M2}R_s$. Considering $G_{M2} = 100$ mS, $M = 8$, and $R_B = 300 \Omega$, (25) estimates an optimistic RX NF of 1.55 dB in the low-noise mode.

The next step is calculating the noise penalty due to the parallel preselect filter. Fig. 26 shows the equivalent model of the parallel preselect filter with the input-referred noise of the gyrator and the output current noise of the parallel preselect filter transconductance. Since sL_N is short to ground at the in-band frequencies, the total input-referred noise penalty due

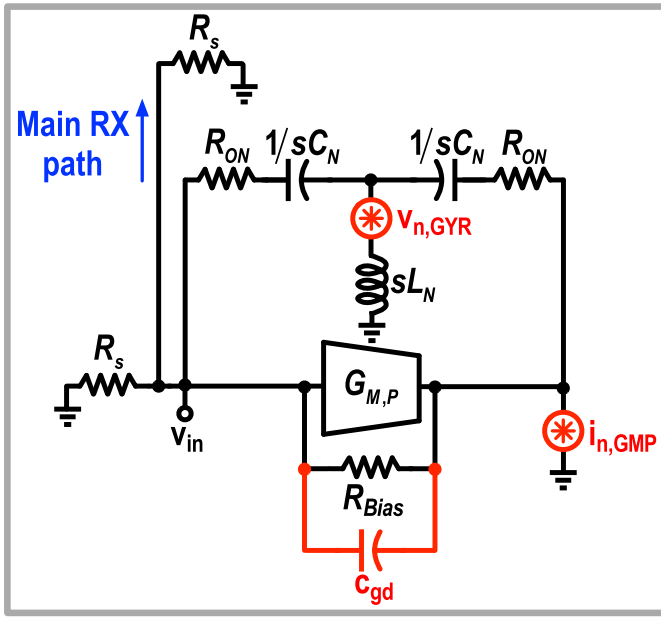


Fig. 26. Simplified model of the proposed parallel preselect filter with the input-referred noise of the active blocks.

to the parallel preselect filter can be derived as follows:

$$v_{n,in}^2 = \left(\frac{r_{o,P} R_s}{2Z_F} \right)^2 i_{n,GMP}^2 + \left| \frac{j(\omega - \omega_{LO}) C_N R_s}{2 + j(\omega - \omega_{LO}) C_N R_s} \right|^2 v_{n,GYR}^2, \quad (26)$$

where $Z_F = R_{Bias} || Z_N$, and R_{Bias} is the bias resistor of the transconductance of the parallel preselect filter. As can be deduced from (26), the noise of the gyrator is high-pass-filtered by the notch filter capacitors and has a negligible effect on the noise penalty of the parallel preselect filter. Then, the NF of the proposed RX in the linear mode can be calculated by

$$F_2 = \left(1 + \frac{1}{G_{M2} R_s} + \frac{R_s}{R_B} + \frac{1}{G_{M,P} R_s} \left(\frac{A_P R_s}{2Z_F} \right)^2 \right) \times \frac{1}{\text{sinc}^2\left(\frac{\pi}{M}\right)} \quad (27)$$

where $A_P = G_{M,P} \times r_{o,P}$. Consequently, by choosing $Z_F \gg A_P \times R_s$, the noise penalty due to the activation of the parallel preselect filter can be minimized. In practice, as shown in Fig. 17(a), the measured NF at the lowest operating frequency degrades only by 0.6 dB when changing the RX configuration from the low-noise mode to the linear mode. However, it is worth mentioning that the parallel preselect filter adds an extra parasitic capacitor to the RX input (especially the Miller effect of c_{gd} in Fig. 26). This extra parasitic capacitor degrades the NF of the proposed RX as the LO frequency increases.

APPENDIX B

This appendix recalculates the center frequency shift due to the proposed translational feedback loop by considering the delay of the main RX path, $t_{d,RX}$. The source of this

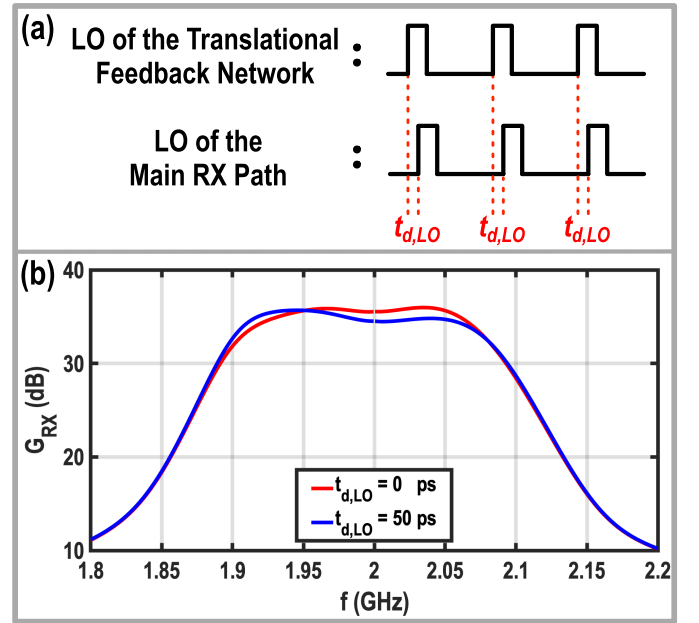


Fig. 27. (a) Illustration of the phase misalignment between the LOs of the main RX path and the translational feedback network. (b) Simulated RX gain for different time shifts between the LOs of the main RX path and the translational feedback network.

delay mostly comes from the LNTA and the TIA's amplifier. Moreover, depending on the sign of the phase misalignment between the LOs of the main RX path and the translational feedback network, $t_{d,RX}$ slightly increases or decreases [for example, positive $t_{d,LO}$ increases $t_{d,RX}$ in Fig. 27(a)]. Taking the $t_{d,RX}$ into account, the main RX path can be modeled by a bandpass amplifier with a transfer function of

$$A(s) = \frac{A_0}{1 + \frac{s \cdot e^{-j\omega_{d,RX}}}{\omega_{P1}}} \bigg|_{s=j(\omega - \omega_{LO})}. \quad (28)$$

The transfer function from the source to the output of the TIA can be derived using (28)

$$\frac{V_{out}}{V_s} = \frac{A_0}{D(\omega)} \quad (29)$$

where $D(\omega)$ is given by

$$D(\omega) = 1 + \frac{\omega R_m C_m}{1 + (\omega R_m C_m)^2} + \sin(\omega t_{d,RX}) \times \frac{\omega - \omega_{LO}}{\omega_{P1}} + j \left(\cos(\omega t_{d,RX}) \times \frac{\omega - \omega_{LO}}{\omega_{P1}} - \frac{(\omega R_m C_m)^2}{1 + (\omega R_m C_m)^2} \right). \quad (30)$$

By setting $d|V_{out}/V_s|^2/d\omega = 0$, the center frequency of the main RX path can be estimated by

$$\omega_{peak,p} = \frac{\omega_{LO} + \omega_{P1} \times \frac{(\omega R_m C_m)^2}{1 + (\omega R_m C_m)^2}}{1 + t_{d,RX} \omega_{P1} \times \left(1 + \frac{\omega R_m C_m}{1 + (\omega R_m C_m)^2} \right)}. \quad (31)$$

As can be gathered from (31), due to $t_{d,RX}$, the center frequency is shifted to lower frequencies than predicted by (22). This issue is also observed in the simulation results in Fig. 27(b), in which adding a delay between the LOs of the

main mixers and the translational feedback network creates a negative center frequency shift and a gain peaking at the lower edge of the passband. Hence, the value of C_m must be increased further to also compensate for the delay of the RX main path and LO misalignment.

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REFERENCES

- [1] *Base Station (BS) Radio Transmission and Reception (Release 15)*, document TS 38.104, Version 15.14.0, 3GPP, European Union Timber Regulation Access, Jun. 2021.
- [2] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
- [3] C. Andrews, L. Diamante, D. Yang, B. Johnson, and A. Molnar, "A wideband receiver with resonant multi-phase LO and current reuse harmonic rejection baseband," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1188–1198, May 2013.
- [4] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1348–1360, May 2018.
- [5] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "High-linearity bottom-plate mixing technique with switch sharing for N-path filters/mixers," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 323–335, Feb. 2019.
- [6] E. Zolkov and E. Cohen, "A mixer-first receiver with enhanced matching bandwidth by using baseband reactance-canceling LNA," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 109–112, 2021.
- [7] V. K. Purushothaman, E. A. M. Klumperink, B. T. Clavera, and B. Nauta, "A fully passive RF front end with 13-dB gain exploiting implicit capacitive stacking in a bottom-plate N-path filter/mixer," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1139–1150, May 2020.
- [8] V. K. Purushothaman, E. A. M. Klumperink, R. Plompen, and B. Nauta, "Low-power high-linearity mixer-first receiver using implicit capacitive stacking with 3x voltage gain," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 245–259, Jan. 2022.
- [9] H. Shao, G. Qi, P.-I. Mak, and R. P. Martins, "A 1.7–3.6 GHz 20 MHz-bandwidth channel-selection N-path passive-LNA using a switched-capacitor-transformer network achieving 23.5 dBm OOB-IIP3 and 3.4–4.8 dB NF," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 413–422, Feb. 2022.
- [10] A. N. Bhat, R. A. R. van der Zee, and B. Nauta, "A baseband-matching-resistor noise-canceling receiver with a three-stage inverter-only OpAmp for high in-band IIP3 and wide IF applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 1994–2006, Jul. 2021.
- [11] G. Pini, D. Manstretta, and R. Castello, "Analysis and design of a 260-MHz RF bandwidth +22-dBm OOB-IIP3 mixer-first receiver with third-order current-mode filtering TIA," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1819–1829, Jul. 2020.
- [12] S. Krishnamurthy and A. M. Niknejad, "An enhanced mixer-first receiver with distortion cancellation, achieving 80-dB/decade RF selectivity and +8-dBm B1dB for adjacent channel blockers," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 64–67, 2021.
- [13] S. Krishnamurthy and A. M. Niknejad, "Synthesis and design of enhanced N-path filters with 60-dB/decade RF selectivity," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 522–525, 2020.
- [14] S. Krishnamurthy and A. M. Niknejad, "Design and analysis of enhanced mixer-first receivers achieving 40-dB/decade RF selectivity," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1165–1176, May 2020.
- [15] F.-W. Kuo et al., "A Bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.
- [16] C.-K. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.4–6-GHz 17-dBm B1dB 36-dBm IIP3 channel-selecting low-noise amplifier for SAW-less 3G/4G FDD diversity receivers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1110–1121, Apr. 2016.
- [17] J. W. Park and B. Razavi, "Channel selection at RF using Miller band-pass filters," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3063–3078, Dec. 2014.
- [18] H. Wang, Z. Wang, and P. Heydari, "An LO leakage suppression technique for blocker-tolerant wideband receivers with high-Q selectivity at RF input," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1682–1696, Jun. 2021.
- [19] H. Razavi and B. Razavi, "A 0.4–6 GHz receiver for LTE and WiFi," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.
- [20] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in spatio-spectral-filtering MIMO receiver arrays for digital beamforming," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3152–3166, Dec. 2016.
- [21] F. Lin, P.-I. Mak, and R. P. Martins, "An RF-to-BB-current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2547–2559, Nov. 2014.
- [22] G. Qi, B. van Liempd, P. Mak, R. P. Martins, and J. Craninckx, "A SAW-less tunable RF front end for FDD and IBFD combining an electrical-balance Duplexer and a switched-LC N-path LNA," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1431–1442, May 2018.
- [23] G. Qi, P.-I. Mak, and R. P. Martins, "A 0.038-mm² SAW-less multiband transceiver using an N-path SC gain loop," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2055–2070, Aug. 2017.
- [24] Z. Lin, P.-I. Mak, and R. P. Martins, "Analysis and modeling of a gain-boosted N-path switched-capacitor bandpass filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2560–2568, Sep. 2014.
- [25] M. A. Montazerolghaem, L. C. N. de Vreede, and M. Babaie, "19.1 A 300 MHz-BW, 27-to-38 dBm in-band OIP3 sub-7 GHz receiver for 5G local area base station applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 292–294.
- [26] M. A. Montazerolghaem, S. Pires, L. C. N. de Vreede, and M. Babaie, "6.5 A 3dB-NF 160 MHz-RF-BW blocker-tolerant receiver with third-order filtering for 5G NR applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 98–100.
- [27] P. Song and H. Hashemi, "RF filter synthesis based on passively coupled N-path resonators," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2475–2486, Sep. 2019.
- [28] M. Darvishi, R. van der Zee, and B. Nauta, "Design of active N-path filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, Dec. 2013.
- [29] M. A. Montazerolghaem, L. C. N. de Vreede, and M. Babaie, "A 0.5–3 GHz receiver with a parallel preselect filter achieving 120dB/dec channel selectivity and +28dBm out-of-band IIP3," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 11–12.
- [30] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 52–65, Aug. 2012.
- [31] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS quad-band SAW-Less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.
- [32] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.
- [33] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
- [34] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. 2010.
- [35] A. Ghaffari, E. A. M. Klumperink, and B. Nauta, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, Jun. 2013.
- [36] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.

- [37] J. W. Park and B. Razavi, "A harmonic-rejecting CMOS LNA for broad-band radios," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1072–1084, Apr. 2013.
- [38] X. He and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Apr. 2011, pp. 372–374.
- [39] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1097–1111, May 2014.
- [40] R. Chen and H. Hashemi, "Reconfigurable receiver with radio-frequency current-mode complex signal processing supporting carrier aggregation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3032–3046, Dec. 2015.
- [41] S. Krishnamurthy, F. Maksimovic, L. Iotti, and A. M. Niknejad, "Analysis and design of submilliwatt interference-tolerant receivers leveraging N-path filter-based translational positive feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 7, pp. 3496–3509, Jul. 2021.
- [42] J. A. Weldon et al., "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003–2015, Dec. 2001.
- [43] R. Chen and H. Hashemi, "Reconfigurable blocker-resilient receiver with concurrent dual-band carrier aggregation," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Nov. 2014, pp. 1–4.
- [44] D. Murphy et al., "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.
- [45] H. Razavi and B. Razavi, "A 0.4–6 GHz receiver for cellular and WiFi applications," *IEEE J. Solid-State Circuits*, vol. 57, no. 9, pp. 2640–2657, Sep. 2022.
- [46] S. Bu and S. Pamarti, "A dual-channel high-linearity filtering-by-aliasing receiver front-end supporting carrier aggregation," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1457–1469, May 2022.
- [47] J. Musayev and A. Liscidini, "A quantized analog RF front end," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1929–1940, Jul. 2019.
- [48] J. Y. Kim and A. Liscidini, "A reconfigurable power-efficient quantized analog RF front-end with smart calibration," *IEEE Open J. Solid-State Circuits Soc.*, vol. 2, pp. 165–174, 2022.



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