An 11-bit 2MS/s column parallel SAR-RAMP ADC for ToF imager readout

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Abstract

Time-of-Flight (ToF) is an optical range detection technique that derives range from the round-trip time of light pulse between the imager and the target. Due to the simple hardware and distance extraction algorithm, ToF imagers are widely adopted in existing (automotive, consumer electronics, etc.) and emerging (AR/VR, etc.) applications requiring depth information. ToF is divided into Direct-ToF (D-ToF) and Indirect-ToF (I-ToF). Compared with the D-ToF system which directly measures the round-trip time of the laser beam, the I-ToF system indirectly measures the time from a phase measurement of the received modulated pulse. I-ToF provides a smaller detection range but it is less sensitive to jitter in the system and can achieve higher accuracy. Hence, I-ToF is used in short-range high precision applications such as face recognition.

This thesis describes the readout ADC design for the next-generation I-ToF imagers used for smartphone face recognition in collaboration with Infineon. A compact 11-bit 2 MS/s column-level ADC is developed in 65nm CMOS image technology. To balance between the available area and required speed, a hybrid SAR-RAMP ADC concept is proposed, which also embeds a threshold comparison phase to relax requirements on successive phases. The ADC has been verified with the post-layout extracted view of the column-level analog circuits and the schematic view of the central/digital circuits with an ideal ramp buffer, achieving a 1.1 V - 3.3 V input range with a 1.1 V reference, a signal-to-noise and distortion ratio (SNDR) of 64.3 dB, 45 µW power consumption, a Walden figure of merit (FOM_W) of 107 fJ/conv-step and an area of 7 µm $\times$ 815 µm.

Contents

1 Introduction

Time-of-Flight (ToF) is a widely used range detection technique that records the time delay of transmitting a modulated light toward the target and capturing the reflected light with a sensor. This time delay is proportional to the round-trip distance between the sensor and the target. Therefore, the distance could be calculated with the speed of light. Fig. 1.1 is an example of the image taken with a ToF imager. Unlike the traditional 2D image that captures the color of an object, a 3D image captures the object's distance from the imager with the color of every pixel representing the distance. Due to the simple hardware and easy distance extraction algorithm, ToF imagers are widely used in consumer electronics, automotive, industrial, medical, and other applications requiring distance information. Research interest in ToF imager has been on the rise in recent years [1, 2, 3, 4, 5].

Figure 1.1: Example image of using time of flight measurement for people classification and range detection [6].

This thesis describes a readout ADC for the next-generation ToF imager under development for smartphone face unlock in collaboration with Infineon.

1.1. ToF imager working principle

A Direct-ToF (D-ToF) imager system consists of a pulse emitter, single-photon avalanche diodes (SPADs), and Time-to-Digital-Converters (TDCs) (see Fig 1.2). ΔT seconds after emitting a pulsed laser beam, the reflected pulse from the target will be sensed by the SPAD. The TDC converts the time difference ΔT to a digital word.

Multiplying $\frac{\Delta T}{2}$ with speed of light c in digital gives the distance D:

$$D = \frac{\Delta T}{2} \times c \tag{1.1}$$

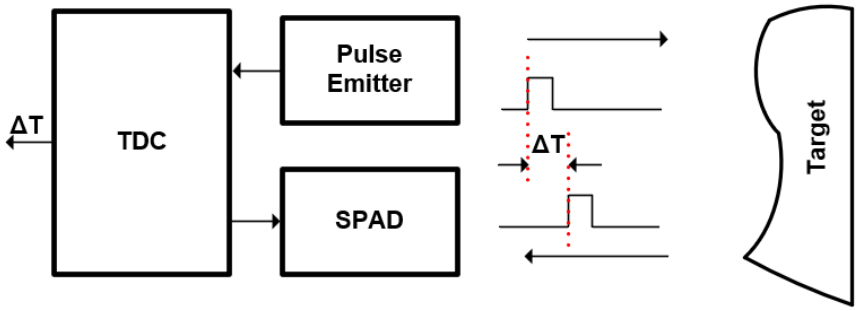


Figure 1.2: Simplified block diagram of a D-ToF imager system.

The D-ToF method could detect long ranges even in adverse environments, as the emitted pulse is usually much stronger than the background light [7]. Depending on the application, commercial D-ToF imagers could detect ranges from dozens of centimeters to several kilometers, with varying accuracy also depending on the environment. D-ToF imagers generally have poor accuracy for shorter ranges due to internal timing variation. An RMS jitter σ_j of the system will lead to an RMS distance error of σ_D:

$$\sigma_D = \frac{\sigma_j}{2} \times c \tag{1.2}$$

which is fixed and more pronounced in short ranges.

An Indirect-ToF (I-ToF) imager system consists of a pulse emitter, pixels consisting of a photodiode (PD) with differential output, and analog-to-digital converters (ADCs) (see Fig. 1.3a). In I-ToF, the pulse emitter transmits pulses at a much higher frequency. The pixel senses the reflected pulses from the target and derives the phase difference θ between transmitted pulses and reflected pulses with a differential measurement (see Fig. 1.3b and 1.3c). The pixel consists of two capacitors that integrate the sensed current separately. When Φ_0 is high, C1 is active and integrates the sensed current. When Φ_{180} is high, C2 is active and integrates the sensed current instead. A differential voltage (V_0-V_{180}) is thus generated at the end of the integration, the value of which is proportional to θ (see Fig. 1.3c). The ADC converts the differential voltage to derive θ in digital. Distance D could be calculated with the laser modulation frequency f as:

$$D = \frac{\theta}{360^\circ} \frac{c}{2f} \tag{1.3}$$

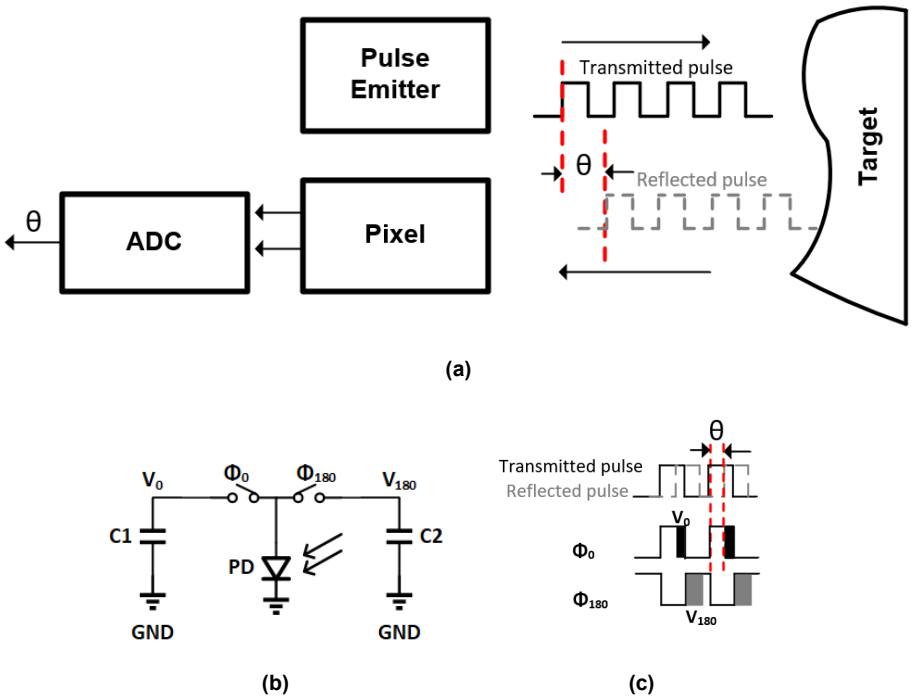


Figure 1.3: Simplified I-ToF imager system (a) Block diagram. (b) Pixel structure. (c) Two-phase measurement of the reflected pulse timing waveform.

The I-ToF method is less sensitive to jitter as jitter transfers to an error on θ during the phase measurement, and the final distance error could be negligible with a high modulation frequency f, thus I-ToF provides higher accuracy in low ranges. Also, as the I-ToF pixel has a similar working principle as a standard 2D imager pixel, it can be implemented with CMOS image sensor technology, achieving high resolution with a small pixel pitch in a limited area. This work focuses on I-ToF since it is better suited for face recognition applications.

I-ToF differential pixel working principle

Except for the differential output, the pixel used in the I-ToF imager has a similar structure thus working principle as a normal active pixel usually used in a 2D imager (see Fig. 1.4). The charge transfer and photodiode integration are performed in-pixel and the voltage levels are read out. At first, V_0 and V_{180} are reset to the pixel supply VDD_{pixel} when the Reset is high. When Reset is low, PD sensed current I_{PD} is integrated on C1 and C2 in Φ_0 and Φ_{180} separately. V_0 and V_{180} will drop from the reset level until the end of integration with value:

$$V_0 = VDD_{pixel} - \int_{\Phi_0} \frac{I_{PD}}{C1}\, dt$$

$$V_{180} = VDD_{pixel} - \int_{\Phi_{180}} \frac{I_{PD}}{C2}\, dt$$

V_0 and V_{180} act like DC signals afterward and can be read out when Row decode goes high.

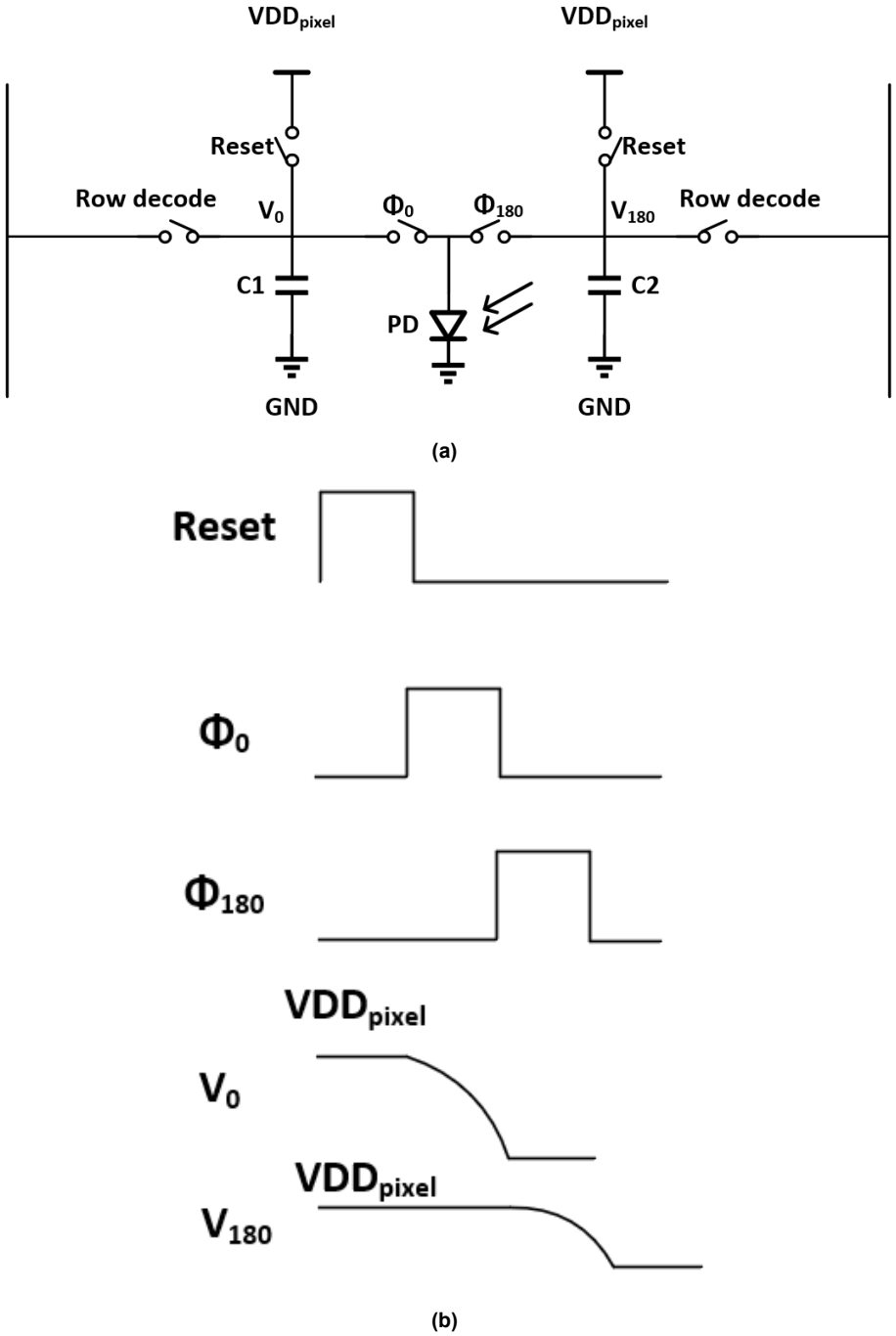


Figure 1.4: I-ToF pixel (a) Structure. (b) Operation waveform.

1.2. I-ToF imager readout

1.2.1. Readout circuit

A block diagram of a typical I-ToF imager readout circuit is shown in Fig. 1.5. The pixel with differential outputs in the array is shown in Fig. 1.4a. These outputs are selected through the row decoder and sent to a buffer, usually programmable gain amplifiers (PGAs). The PGA provides different gain settings and amplifies the pixel outputs to match the full-scale range (FSR) of the (ADC, maximizing the signal-to-

noise ratio (SNR). Another function of the PGA is to drive the ADC by separating the signal source (pixel) and load (ADC). The ADC converts the pixel outputs to digital signals for further processing.

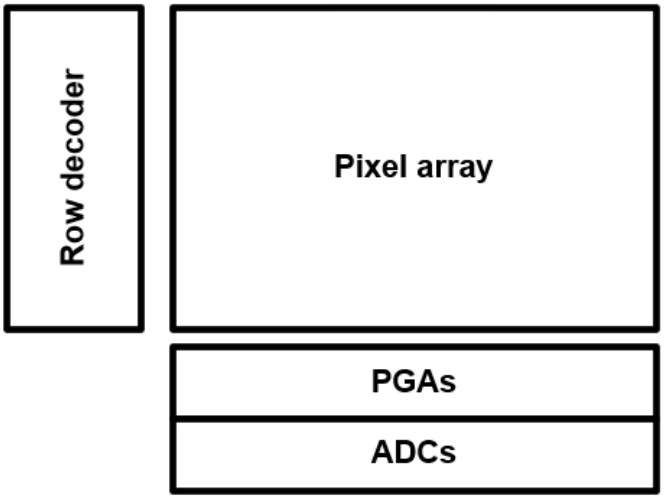


Figure 1.5: Simplified block diagram of an I-ToF imager readout circuits.

The I-ToF imager readout circuit in this project is formed by the pixel array (size 905×678) with differential pixel, the row decoder, and the column-level readout circuit which consists of two source followers and one single-ended ADC in every column (see Fig. 1.6). Instead of PGA, two source followers are used to reduce system complexity and power consumption. Instead of using differential ADCs to convert the differential outputs directly, single-ended ADCs are used to read out the two outputs individually. This provides an accurate value of the voltage pixel outputs and allows monitoring the pixel's correct functionality. Instead of using two single-ended ADCs for two single-ended outputs respectively, one single-ended ADC running at twice the sampling speed is used to read the two outputs sequentially to reduce the area consumption. This also allows performing correlated double sampling on the ADC's offset in the digital during the subtraction of the two single-ended signal conversion results.

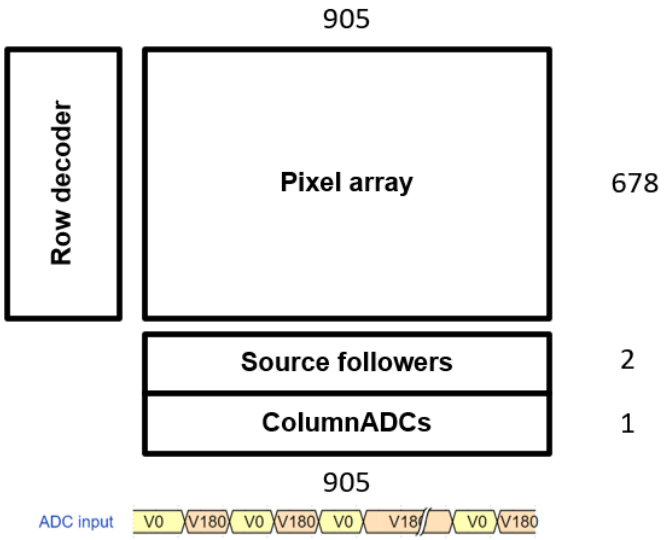


Figure 1.6: I-ToF imager readout circuit of this thesis.

1.2.2. ADC requirements analysis

The main requirements of the ADC are given in Table 1.1.

Parameter	**Value**
Technology	65nm
Power supply	1.2V ± 10%
Resolution	11-bit
Sampling rate	2 MS/s
RMS Noise	<= 0.6 V_{LSB}
Current consumption	<= 200 µA
Input range	1.1V - 3.3V
DNL	<= 0.8 LSB
RMS Offset	<= 5 V_{LSB}
Width	<= 7 µm
Length	<= (678 $\times$ 3.5) µm

Table 1.1: Requirements for the column-level ADC.

The sampling rate is set by the conversion time for 1 column (1ms), the number of pixels in one column (678), and the reset time (0.35µs) of the pixel before the integration.

The input range is very wide because the pixel power supply will affect the pixel output level, thus possible power supply variation is included.

The differential non-linearity (DNL) should be within 0.8 LSB to ensure monotonicity, which is important in imager applications for sharp edge detection [8].

The offset requirement is relatively relaxed, as the ADC offset will be canceled during the subtraction in digital.

The width and length requirement comes from the available area of a column in the pixel array. The I-ToF imager under development consists of a sensor chip and

a logic chip stacked together and connected with direct bond interconnects (see Fig. 1.7a), so the width available for a column-level ADC is the same as the pixel pitch. In this project, the pixel pitch is 3.5um. Typically, column-level ADCs occupy twice the pixel pitch in width [9], as it is impractical to fit the ADC within the width of a single pixel. The length of the ADC is reduced by half to compensate for the double pitch width used (see Fig. 1.7b). ADC1 and ADC2 with double pixel pitch width and half column length are placed in the two columns' area. On average, one ADC is used for one column.

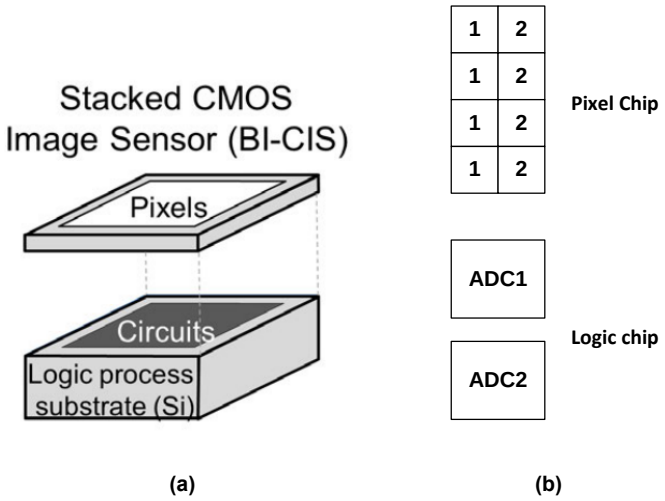


Figure 1.7: (a) Oblique view of stacked sensor chip and logic chip [10]. (b) ADC placement of 2 columns.

1.3. Reviews on Nyquist-rate column-level ADCs

Nyquist-rate ADCs are the most common architecture in column-level imager readouts. Over-sampled ADCs are also reported in literature [11]. The key advantage of an over-sampled ADC is the noise shaping which moves quantization error from lower frequency to higher frequency of the Nyquist frequency band with a sigma-delta modulator and removal of the noise outside the signal band with a digital low-pass filter. The quantization error at the band of interest is shaped to a sunken spectrum, and the effective number of bits (ENOB) is thus limited less by quantization error compared with Nyquist-rate ADCs. In this review, over-sampled ADCs are not considered because, for the required 1 MHz Nyquist rate, they would require a high-speed clock to be distributed across the entire array, resulting in high power consumption of the clock distribution system.

This review focuses on the following aspects:

1. Area. The width of the ADC is strictly limited by the pixel pitch, so the ADC is desired to be narrow. Also, routing congestion at the system level needs to be avoided to enable large arrays. On the other hand, the area is less constrained in the vertical direction, allowing for a medium level of complexity in the ADC to improve the overall performance.

2. Speed. The sampling rate of the ADC is determined by the desired frame rate per second (FPS) of the pixel array and allocated time for other operations (e.g., pixel reset). Another dimension of evaluating speed is the clock cycles needed for a single conversion, as there is usually a maximum clock frequency available for the ADC. The maximum available clock cycles depend on the sampling rate and the maximum clock frequency.
3. Power. As the I-ToF imager targets consumer electronics applications, power consumption should be minimized after meeting the area and speed requirements.

1.3.1. Ramp ADC and variants

Ramp ADC (also known as single-slope ADC) is the most popular column-level ADC for imagers. The core blocks are a comparator and a ramp generator (see Fig. 1.8a). The digital code is determined by counting the clock cycles needed for the comparator to invert its output as in Fig 1.8b. When multiple synchronized ramp ADCs are running in parallel, the same ramp is needed in every ADC, so the ramp could be shared through a buffer. The price for such simplicity is the intrinsic low speed. The conversion time grows exponentially with the resolution. For the target sampling rate of 2 MS/s and 11-bit resolution, a ramp ADC would require a 4 GHz clock, which is 20 times faster than the provided clock.

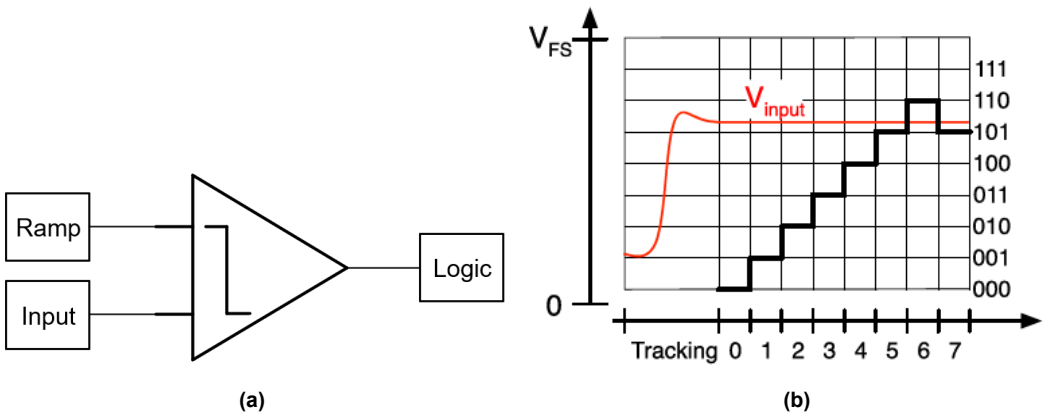


Figure 1.8: Ramp ADC (a) Conceptual diagram. (b) Waveform [12].

To increase the speed of ramp ADC, look-ahead ramp ADC [13] introduces look-ahead operation to the ramp generator and predictors (a capacitor) for storing the comparison results (see Fig. 1.9). Look-ahead operation is a ramp step equals k LSB instead of 1 LSB. After the operation, if the comparator output inverts, the actual code is between t (counter value before look-ahead) and t+k, and the counter output is set to t+0.5K and stored as the output code. Predictors would sum an analog voltage Vpred proportional to the number of comparator outputs inverted. The look-ahead operation is kept if Vpred is smaller than a predefined Vref1 voltage. Speed up of K-1 clock cycles is achieved at a price of code errors up to 0.5k for the number of columns defined by the Vref1. Otherwise, it is undone, and the ramp will count 1 LSB at a time for K steps. The advantage of this architecture is that a negligible additional column-level circuit (only the predictor) is needed. According to simulations with actual image

data sets and different settings of k and Vref1, a maximum speed-up of four times [13] compared to ramp ADC is achieved. The disadvantage is that code errors can be up to 0.5k LSB, which degrades the signal-to-noise and distortion ratio (SNDR).

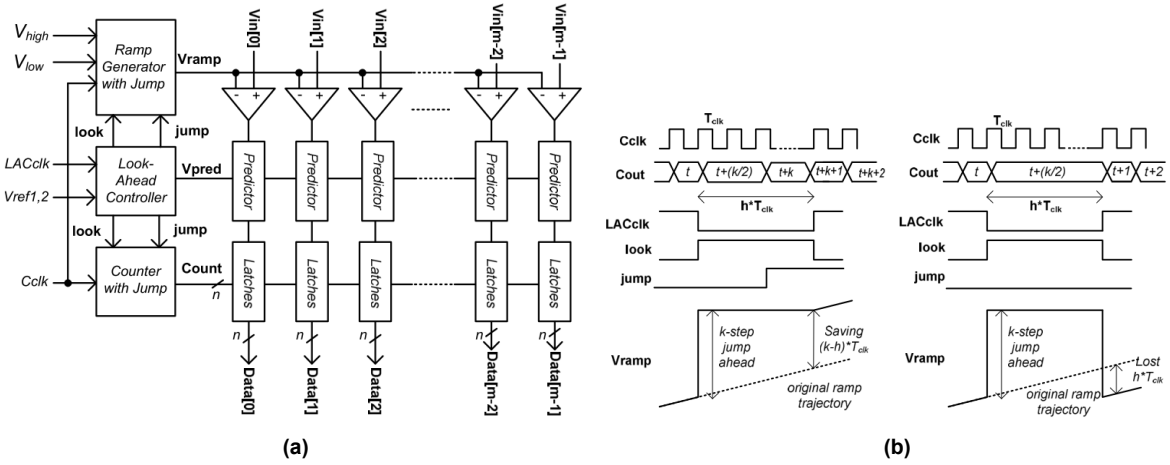


Figure 1.9: Proposed look-ahead ramp ADC (a) Block diagram. (b) Timing waveform of the look-ahead operation.

Another approach is to add a second ramp stage and divide the ADC operation into two phases, to form a multiple-ramp single-slope (MRSS) architecture [14]. The column circuit is nearly the same as ramp ADC, while the central circuit consists of a coarse ramp for the same first phase in every column and multiple ramps for the second phase (see Fig. 1.10).

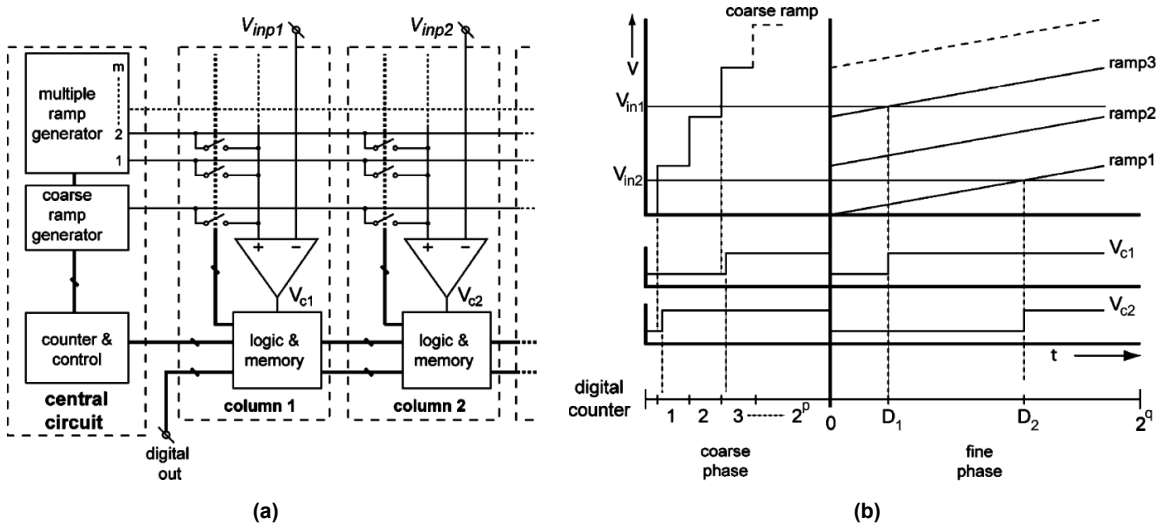


Figure 1.10: Proposed MRSS ADC (a) Block diagram. (b) Timing waveform.

The coarse ramp first determines the MSBs. Based on the MSBs, the corresponding fine ramp is selected for every column. Assuming an ADC with (a+b)-bit, the ratio of clocks cycles needed for a ramp implementation over an MRSS implementation is:

$$R = \frac{2^{a+b}}{(2^a + 2^b)} \tag{1.4}$$

The maximum R is obtained when a = b. For an 11-bit MRSS ADC with a = 5 and b = 6, only 96 clock cycles are needed, while a ramp ADC would require 2048 cycles. The disadvantage is that 2^b fine ramps and buffers are needed, leading to increased complexity in the ramp generation. Since the fine ramp connected to every column depends on the MSBs of that column, the loading of fine ramps is signal dependent. The driving ability of the buffers has to be designed for the worst case, e.g., all columns are connected to the same fine ramp, which suggests more area/power is needed.

A two-step ramp ADC needing only one ramp for the second stage, with few additional switches and capacitors in the column, is also reported (see Fig. 1.11) [15]. The pixel output is capacitively coupled to the comparator negative input. During the first phase, a coarse ramp is connected to the comparator positive input through switch S_c. Once a comparator output inverts, switch S_C of that column is open, storing the coarse result on capacitor C_H. When the second phase starts, switch S_F in every column is closed, and the same fine ramp is capacitively coupled to the comparator positive terminal through C_H, on top of the coarse result of every column. The advantage over MRSS is that only one fine ramp is needed instead of 2^b fine ramps, which significantly simplifies the ramp generation at the price of additional capacitors and switches in the columns. The disadvantage compared with MRSS is that one $\frac{kT}{C_H}$ noise is added when storing the coarse result on C_H since it is a sampling process (k is the Boltzmann constant. T is the absolute temperature). Thus, sufficient area for C_H is needed to suppress the sampling noise. In MRSS, the fine ramp directly connects to the comparator without any capacitors so that the column circuitry can be very compact.

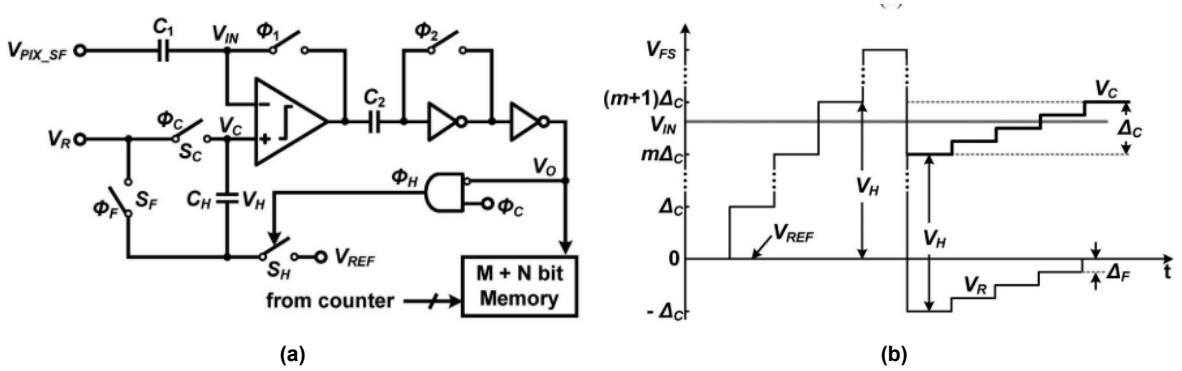


Figure 1.11: Proposed two-step ramp ADC (a) Simplified schematic. (b) Comparator input signal waveform.

1.3.2. Hybrid SAR-RAMP ADC

A column-level SAR-RAMP ADC is also reported [16]. Fig. 1.12 introduces a 12-bit SAR-RAMP ADC, where a 6-bit coarse SAR ADC is implemented in every column, and a 6-bit central buffered fine ramp is connected to every column through the redundant unit cap in the charge-redistribution-based DAC. The DAC is the main area consumption contributor. This approach reduces the number of unit caps needed in every column from 2^{12} to 2^6. Although the DAC is 6-bit, it should meet 12-bit linearity as the ADC linearity is determined by the DAC (see section 2.2). To first order, the

matching of two adjacent capacitors can be modeled as [17]:

$$\sigma_{\Delta C} = \frac{A_{\sigma_{\Delta C}}}{area} \tag{1.5}$$

where $\sigma_{\Delta C}$ is the RMS mismatch, and $A_{\sigma_{\Delta C}}$ is the mismatch coefficient determined by the used technology. As the capacitor value is proportional to the area, in theory, the 6-bit DAC needs the same area as a 12-DAC to reach 12-bit linearity. From a layout perspective, however, it is much more practical to lay out a 6-bit DAC inside one column than a 12-bit DAC. The total clock cycles needed for a single conversion in this architecture is $6+2^6 = 70$. The advantage of the SAR-RAMP scheme is the high speed provided by the SAR, while the disadvantage comes from the area-consuming DAC.

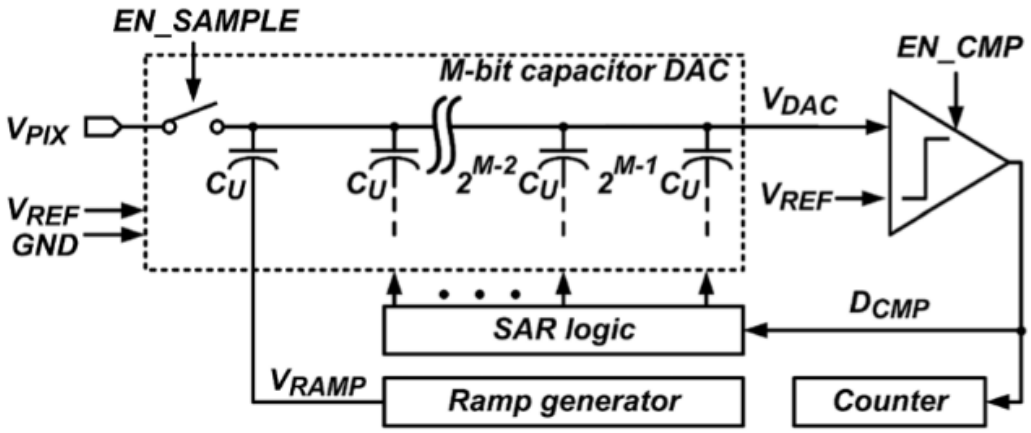


Figure 1.12: Block diagram of the proposed SAR-RAMP ADC.

A RAMP-SAR ADC is also reported, with a first-stage RAMP and a second-stage SAR requiring one ramp and multiple references [18] (see Fig. 1.13a). According to the result of the MSB stage, corresponding references are selected for the SAR conversion. Compared with the SAR-RAMP architecture, the RAMP-SAR approach has a similar speed with the same bit allocations. However, multiple references are needed, which complex the central circuits.

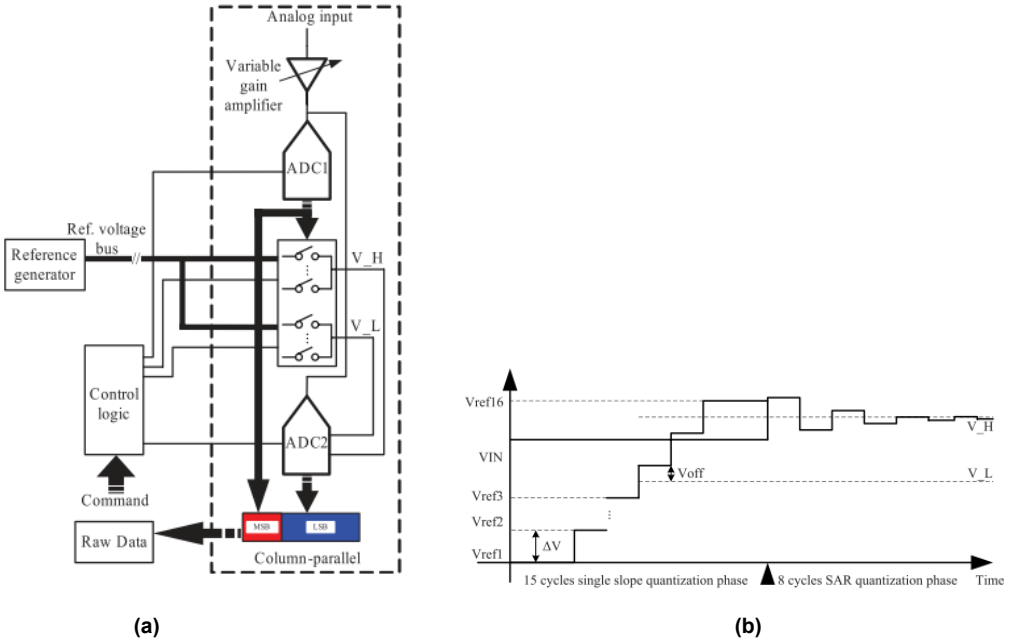


Figure 1.13: Proposed RAMP-SAR ADC (a) Block diagram. (b) Signal waveform.

1.3.3. Cyclic ADC

Cyclic ADC is less popular but also reported in the literature as column-level ADC [19]. A cyclic ADC includes a sub-ADC, a sub-DAC, and an amplifier (see Fig. 1.14). After the signal is sampled, the sub-ADC converts it and outputs this cycle's result. The multiply DAC (MDAC) generates the residue voltage for the next cycle by subtracting the analog voltage through the sub-DAC and amplifying it with the amplifier. The clock cycles needed are similar to that of a SAR ADC with the same resolution, while less area is required for the DAC. The main disadvantage is the high gain amplifier needed, which is power and area consuming.

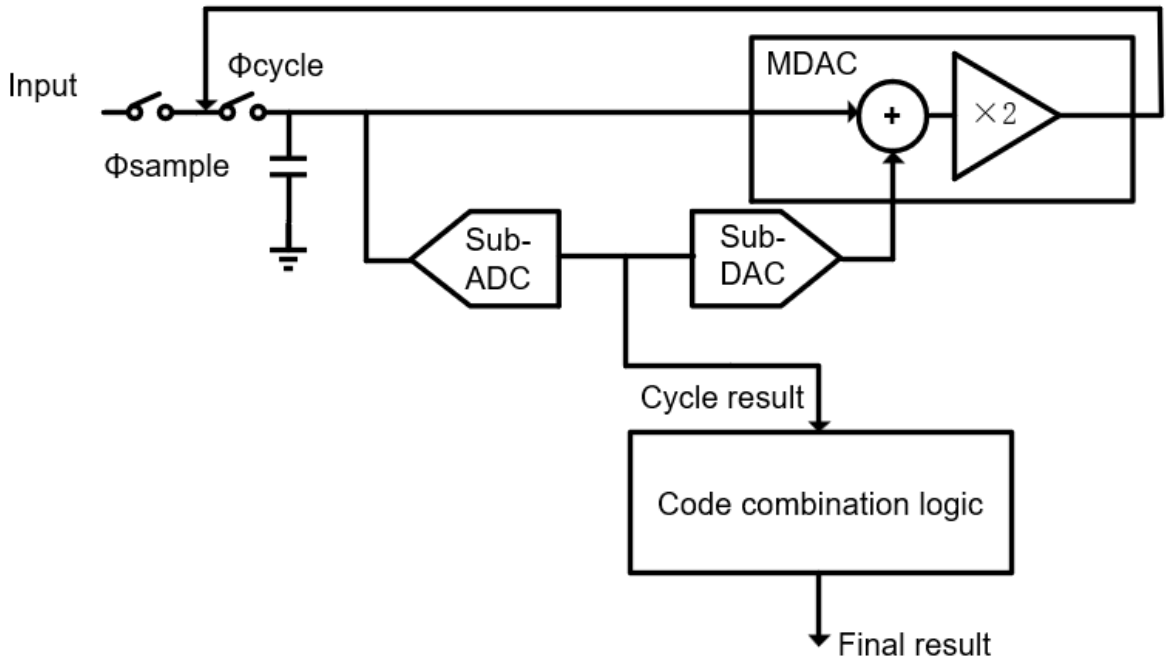


Figure 1.14: Block diagram of a Cyclic ADC.

1.3.4. Comparison and Summary

Table 1.2 summarizes the different types of column-level ADC in imagers and compares area, speed, power, and design efforts for each architecture. $+/-$ indicates the positive/negative rating on the aspect. The area and speed estimation is a rough indication based on analyzing the main area consuming blocks and the clock cycles needed for a single conversion. Power consumption is estimated from the required blocks' static/dynamic power consumption. Design efforts are estimated from the column-level circuit and central circuit.

Scheme	Area	Speed	Power	Design efforts
Ramp	++	-	-	++
look-ahead ramp	++	-	-	+
MRSS	++	+	+	-
Two-step ramp	++	+	+	+
SAR-RAMP	+	++	++	+
RAMP-SAR	+	++	++	-
Cyclic	++	+++	+	-

Table 1.2: ADC scheme comparison.

For this project, the SAR-RAMP scheme is chosen due to the following considerations:

1. Ramp and look-ahead Ramp are small in area as the ramp generation could be central and shared, but their conversion clock cycles grow exponentially with resolution and cannot suffice the speed requirement of our target 11-bit resolution.

2. With an equal allocation of bits in the two phases, MRSS and two-step Ramp is feasible in speed if operating under the maximum clock frequency of 200 MHz. However, they still require around 100 clock cycles, which suggests high comparator power consumption. The comparator could be either dynamic or continuous, as only the moment the ramp crosses the input determines the code. For a fully dynamic comparator, 100 clock cycles mean 100 comparisons, thus high dynamic power. For a continuous-time comparator, a high gain/multi-stage amplifier is needed, meaning high static power consumption.
3. Cyclic ADC outperforms other schemes in terms of area and speed with medium power consumption. However, the amplifier in the MDAC will require design efforts in 65nm, given that the available width is only 7um. It is also power-consuming because of the required amplifier.
4. SAR-RAMP and RAMP-SAR schemes require a medium area for the DAC and meet the speed requirement with a medium clock frequency because of the binary search in the SAR stage. It is also power efficient without static power-consuming blocks in the column circuitry. Compared to RAMP-SAR, SAR-RAMP avoids the generation/routing of many reference voltages and is thus less complex.

1.4. Innovations of the proposed ADC

The required input signal has a wide range (2.2V, between 1.1V to 3.3V) and is larger than the DAC's maximum available VREF (1.1V). Fig. 1.15 shows the proposed ADC to address this problem. Instead of connecting the input and VREF to the DAC capacitors' bottom plate, the input signal connects to the sampling capacitor Cs, and VREF connects to the DAC capacitor array Cdac. This allows to couple the input and reference signals to the input of the comparator with different weights, providing easy and sufficient conditioning of the input signal in our application. The main problem of this approach is SNR degradation. At the comparator input, the signal is attenuated, making the comparator and sampling noise more problematic.

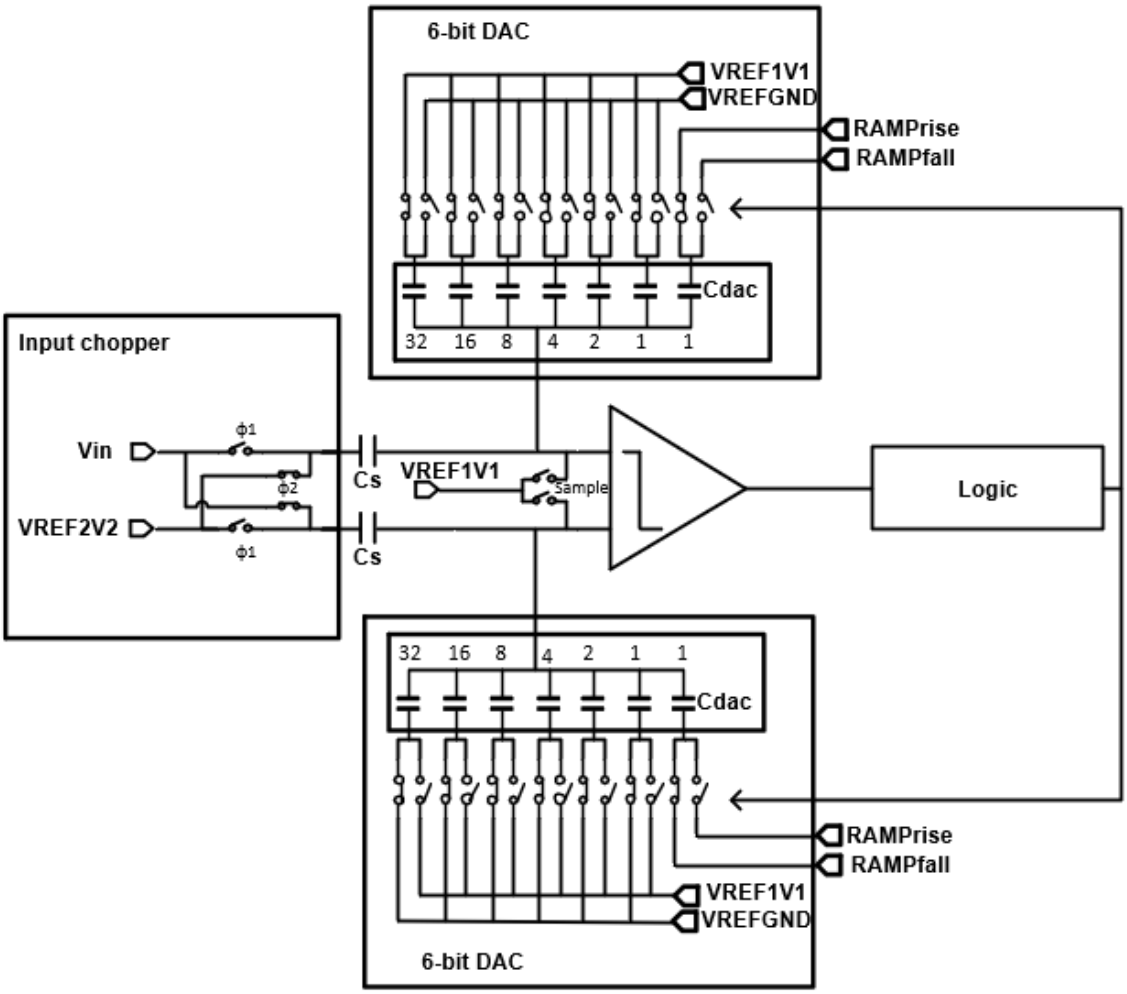


Figure 1.15: Block diagram of the proposed ADC.

Two methods are proposed to improve the SNR that relies on the DC-like characteristic of the pixel voltage during conversion[1]:

1. An input chopper is used to create a differential signal from the single-ended Vin with the help of reference VREF2V2, which increases the signal swing and compensates for the structure's signal attenuation.
2. The input voltage polarity is determined before the SAR conversion. This sample determines the MSB bit and halves the input range, relaxing the signal attenuation needed for the following ADC to operate with a 1.1V reference.

The details will be further explained in Chapter 2.

1.5. Thesis structure

This introduction chapter includes the basic principles of the ToF imager, the readout circuitry of the I-ToF imager under development with the ADC requirements, and the

[1]After the integration of the photo-diode sensed current on the capacitor in the pixel, the pixel output is fixed and fed to the ADC through source follower, acting like a DC voltage

literature review on column-level ADC for imagers.

Based on the literature review, a hybrid SAR-RAMP ADC architecture is chosen. Chapter 2 describes the ADC architecture. Chapter 3 describes the transistor-level implementation of the ADC and the layout. Chapter 4 describes the ADC simulation result, the comparison with others' work. Chapter 5 concludes this work and points out the limitations and possible future work.

2

ADC architecture

2.1. ADC operations

The proposed 11-bit ADC has the following operation modes: (1) single-ended to differential conversion, (2) MSB decision, (3) 6-bit SAR conversion, and (4) 4-bit RAMP conversion. The functional blocks to realize these operations include an input chopper, sampling capacitors Cs, a 6-bit capacitive DAC, a 4-bit ramp generator, a comparator, a voltage reference, and logic circuits.

2.1.1. Single-ended to differential conversion and MSB decision

Single-ended to differential conversion

An input chopper is used to convert the single-ended pixel signal (1.1V - 3.3V) to a differential signal with the help of reference VREF2V2 (2.2V) and sampling capacitor Cs (see Fig. 2.1). When the Sample goes low, the VREF1V1 (1.1V) switch is open and samples the reference as the common-mode voltage for the comparator. The chopper then inverts the input connections. With Cs, the differential input voltage is capacitively coupled to the comparator inputs and is effectively doubled. [1]

[1] Bottom-plate sampling is by default adopted to enable the single-ended to differential conversion with the input chopper.

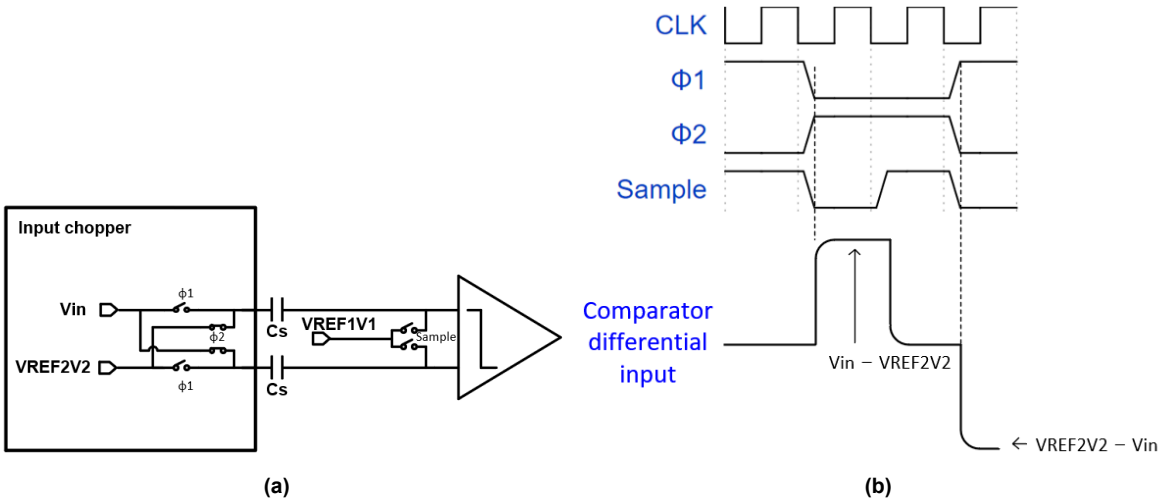


Figure 2.1: Input chopper (a) Block diagram. (b) Timing waveform and comparator input during Single-ended to differential conversion and MSB decision.

Using a chopper has two advantages compared to using one switch to track the signal:

1. The chopper converts the single-ended signal to a differential signal, doubling the signal swing, thus improving SNR.
2. Compared to a single-ended ADC, a differential ADC is immune to common-mode interference. Any power supply variation and other interference would be rejected by the common-mode rejection of the ADC.

MSB decision

The polarity of the differential signal (Vin - VREF2V2) decides the MSB already and is called the MSB decision in this project (see Fig. 2.1b). The reduced 1-bit is allocated to RAMP conversion and relaxes half conversion clock cycles. When Sample goes high again after the MSB decision, the comparator inputs are reconnected to VREF1V1. After it is fully reset, the Sample goes low, opening the VREF1V1 switch and the input chopper inverts the input connection again. A differential signal with inverse polarity (VREF2V2 - Vin) is sampled to comparator inputs for the following SAR-RAMP conversion.

During the reset after the MSB decision, the reference and ramp connections in the 6-bit DAC are reset according to MSB as well, selecting the right FSR (1.1V - 2.2V or 2.2V - 3.3V) in SAR-RAMP conversion that matches with the differential signal with inverse polarity (VREF2V2 - Vin).

2.1.2. 6-bit SAR conversion

A 6-bit DAC connected to the comparator input performs the SAR conversion on (VREF2V2 - Vin) (see Fig. 2.2). The DAC resolution is determined from the available area. More bits in the DAC improve the overall performance at the cost of the area. 6-bit is estimated to be feasible in layout while meeting the speed requirement. After sampling, SAR conversion starts with moving the capacitor to the other reference in 6-bit DAC from MSB to LSB capacitor to successively approximate the comparator

differential input back to 0. The presence of the 6-bit DAC attenuates the coupled voltage from the input chopper with the capacitance ratio between Cs and the total capacitance at the comparator input. The 6-bit DAC output is also attenuated by the capacitance ratio between Cdac and the total capacitance at comparator input.

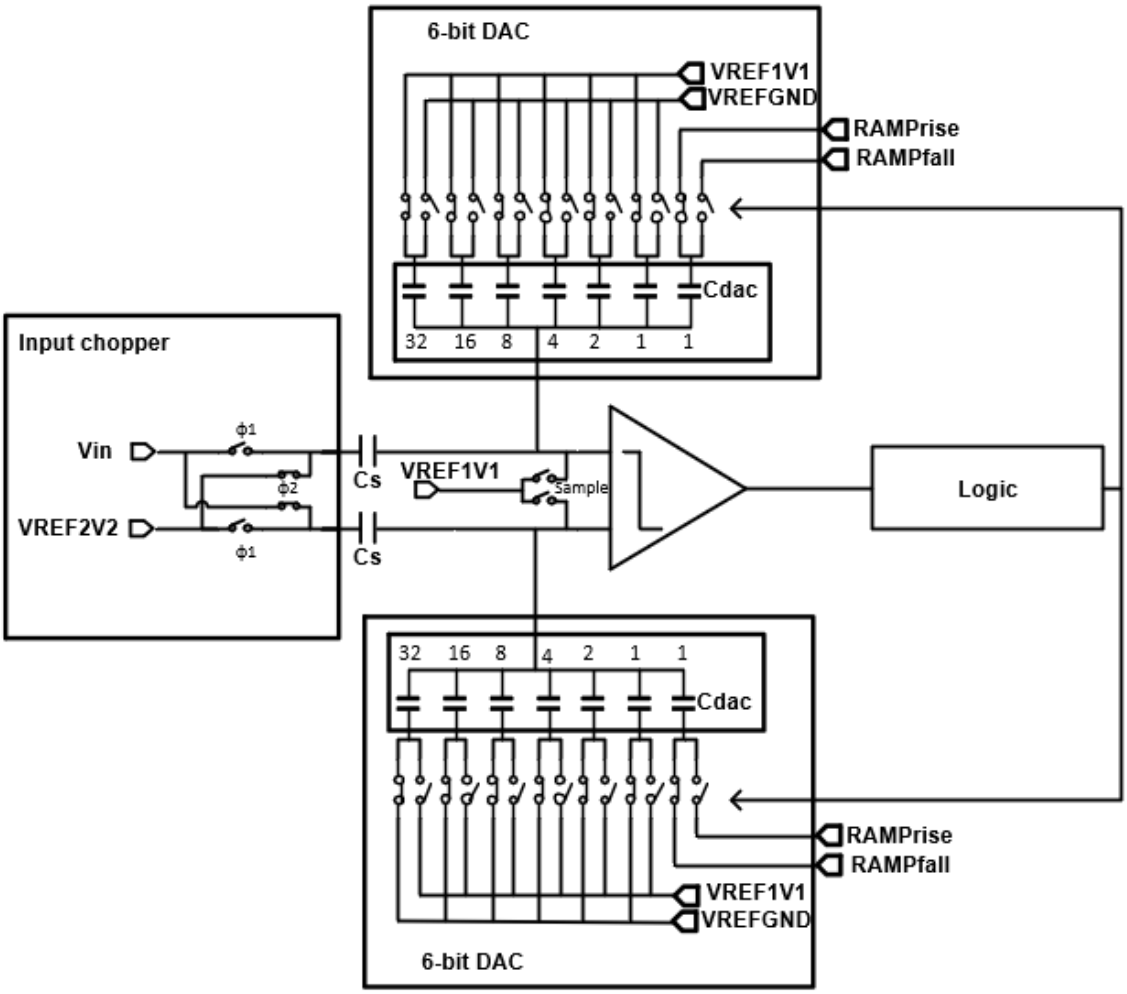


Figure 2.2: ADC Block diagram.

In order to avoid clipping and waste of ADC FSR, the attenuated input signal should match with the attenuated DAC output at the comparator input:

$$(Vin_{max} - VREF2V2)\frac{Cs}{Cs + Cdac + Cp} = (VREF1V1 - VREFGND)\frac{Cdac}{Cs + Cdac + Cp}$$

$$(VREF2V2 - Vin_{min})\frac{Cs}{Cs + Cdac + Cp} = (VREF1V1 - VREFGND)\frac{Cdac}{Cs + Cdac + Cp}$$

Cp is the parasitic capacitance to ground at comparator input. Vin is in the range of 1.1V - 3.3V. Simplifying the equation would cancel Cp, and the resulting relationship between Cdac and Cs is:

$$\frac{Cdac}{Cs} = \frac{1}{1}$$

This modified SAR has the following characteristics:

1. The highest reference used in the DAC is limited to 1.1V [2], while the input signal is between 1.1V and 3.3V. Coupling the input signal and DAC output to the comparator with different capacitors provides a low-cost, flexible solution.
2. Neglecting the parasitic capacitor Cp, comparator noise is amplified by $\frac{1}{50\%} = 2$ when referring back to the Vin. The same amplification also applies to the sampling noise at comparator input after opening the common-mode switch. Since the chopper doubles the signal already, the SNR of the ADC is not changed.

SAR logic: synchronous or asynchronous?

The block diagram of synchronous/asynchronous SAR logic is given in Fig. 3.12. In synchronous SAR logic, the clock signal triggers every bit in the SAR search. Each comparison is triggered by the clock and allocated the same amount of time, based on the worst-case scenario needed for the metastability requirement. In asynchronous SAR logic, each comparison is allocated as much as needed based on the current input of the comparator, and results in a faster conversion for asynchronous design, for the same metastability constraint since there is only one comparison that takes as long as the worst-case scenario and all the others are much faster.

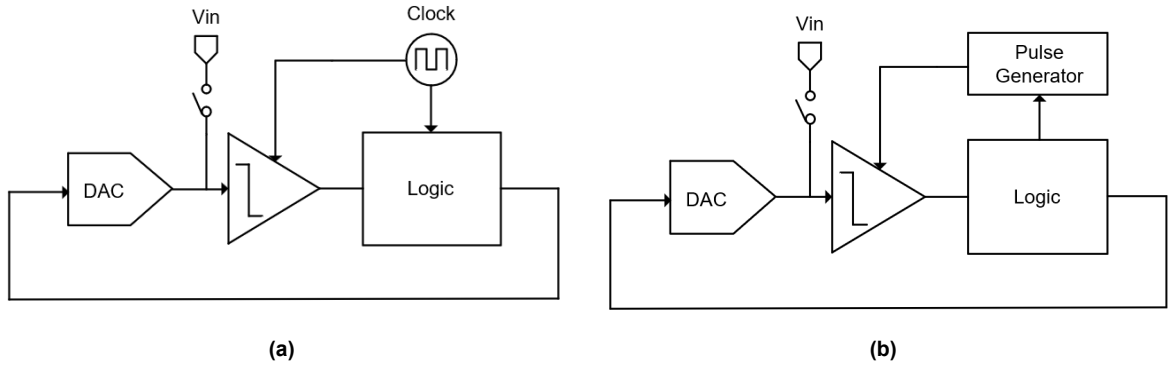


Figure 2.3: SAR logic block diagram (a) Synchronous. (b) Asynchronous.

However, when multiple SAR ADCs are running in parallel with a shared reference voltage, asynchronous logic is problematic due to the kickback on the reference. The diagram of a differential SAR is given in Fig. 2.4. The DAC code determines the loading of the reference voltage on two sides of the comparator. If the loading is different, any reference voltage variation will lead to a differential voltage at the comparator input. For one ADC that finished a comparison and is moving the DAC, the reference buffer and decoupling caps will see a capacitive load change which temporarily varies the reference voltage. A voltage peak as large as 0.2 V is observed in the reference after moving the DAC and is recovered before the next decision time. When multiple asynchronous SAR ADCs are running in parallel, reference variation will change the

[2]The main supply is 1.2V. Considering 10% variation, the maximum VREF is around 1.1V. VREF larger than 1.1V would require bulky level shifters for the SAR logic and high-voltage transistors for the DAC switches to the reference and thus are avoided.

DAC output voltage, thus, comparators' differential input. If some ADCs are deciding, they might have a decision error. With synchronous logic, reference kickback is not an issue, as the clock triggers all the ADCs' operations. The DACs are moving simultaneously when all ADCs are not deciding.

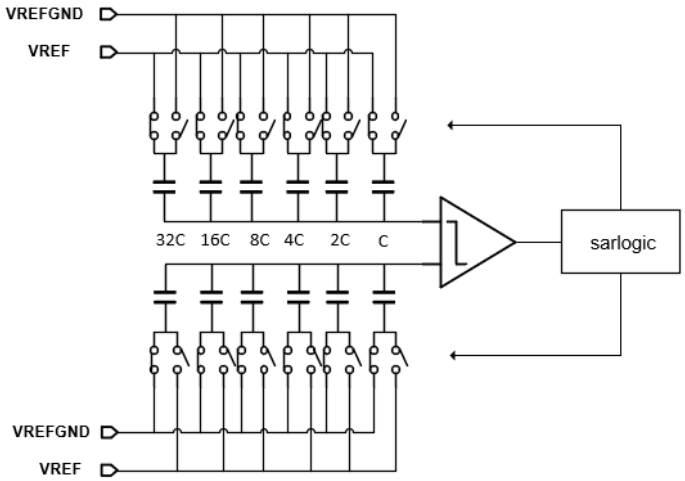


Figure 2.4: The diagram of a 6-bit differential SAR.

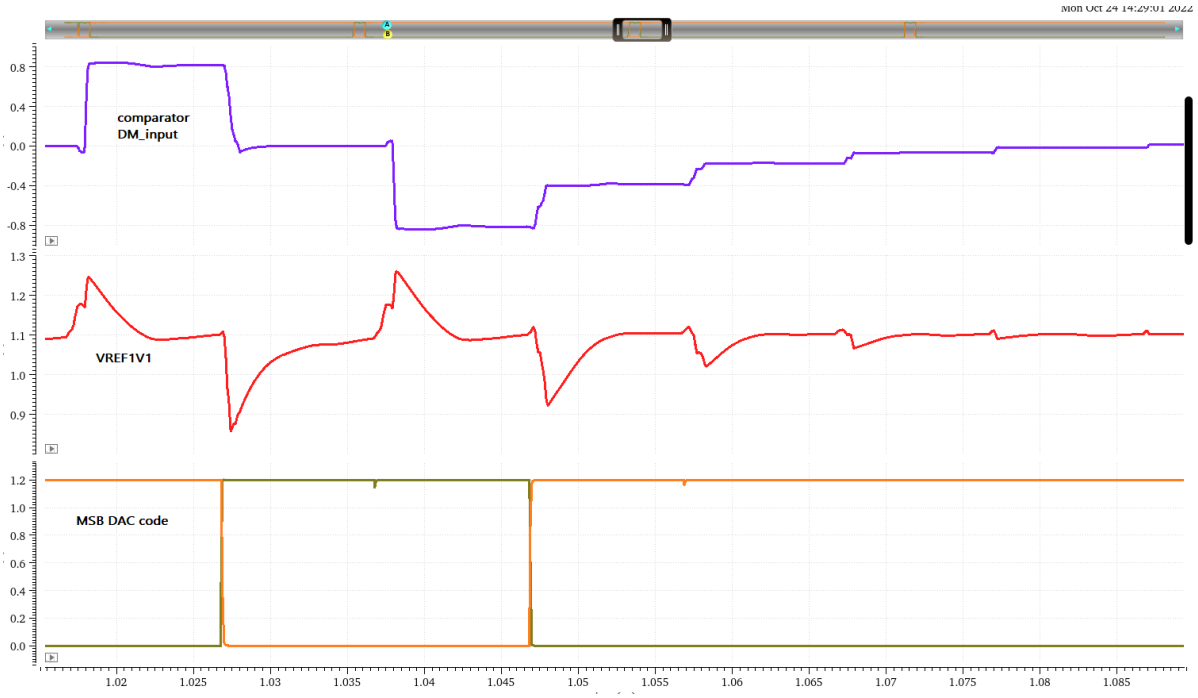


Figure 2.5: The waveform of comparator input, reference voltage, and MSB DAC code of a SAR ADC with real reference buffer and decoupling capacitors.

In our ADC, there is redundancy in the ramp, and it could correct the decision error in the SAR. During the RAMP conversion, no DAC is switching, and the reference is at the nominal value. However, since 905 ADCs are running in parallel, it is impossible to simulate the error because of the kickback on reference. Besides, increasing the

redundancy to increase the error correction ability in the RAMP conversion is time and power-consuming. Considering a 10 mV error on the reference voltage when the DAC is fully connected to VREF1V1 (or VREFGND), the comparator differential input change ΔV_{DM}would be:

$$\Delta V_{DM} = \Delta VREF1V1 \frac{63C_{unit}}{64C_{unit}} = 9.8mV = 9.7LSB \tag{2.1}$$

The error could easily be in the range of 10 LSB, and 10 LSB is 62.5% of the ramp, meaning 62.5% more comparisons are needed in the RAMP conversion. The speed advantage of asynchronous logic thus no longer exists, and synchronous logic is adopted in this project.

2.1.3. 4-bit RAMP conversion

After SAR conversion, RAMP conversion further converts the SAR residue voltage. A differential ramp signal is coupled to the comparator inputs through the extra unit cap in the 6-bit DAC (see Fig. 2.2). A 4-bit unary capacitor DAC is selected to implement a digital ramp as the central ramp for the following reasons:

1. An analog ramp is usually implemented with an integrator. It is compact in area, especially for high resolution, but needs clock synchronization and trimming/calibration to ensure desired performance over process-voltage-temperature (PVT). A DAC-based digital ramp is robust to PVT. The ramp voltage is only determined by the reference voltage and the matching of the unary cells, which are robust over PVT without trimming/calibration. As the required resolution is only 4-bit, the area of the DAC is negligible.
2. Compared with resistor ladder, switched-capacitor based DAC doesn't have static power consumption. Capacitors are more robust to temperature drift than resistors as well.

As the ramp is coupled to the comparator input through the redundant unit cap to make up the binary value in the 6-bit DAC, the noise of the ramp is attenuated by $\frac{1}{64}$ and is negligible.

Due to the mismatch in the 6-bit DAC, the input voltage might not be precisely within the range ramp could cover, thus redundancy is needed. If the input signal is converted to the nearby SAR LSB region due to mismatch, redundancy in the ramp would make sure to cover this region and avoids dead bands in the final digital code (see Fig.2.6) [20].

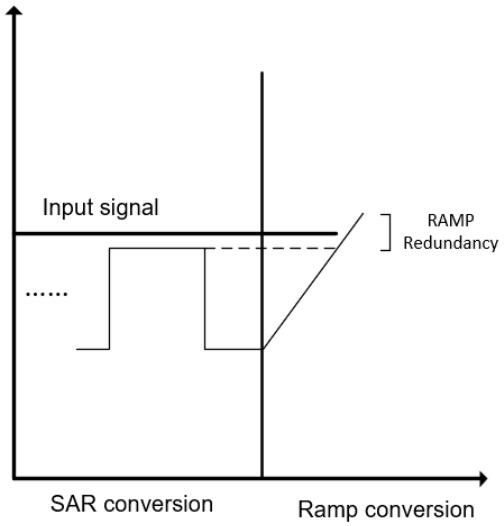


Figure 2.6: Redundancy ensures crossing when input is wrongly converted due to mismatch.

The redundancy needed is simulated by a Matlab script. The transfer curve of a 6-bit DAC with unit cap $\sigma = 0.5\%$ is simulated 1000 times, and the maximum code-width is recorded (see Fig. 2.7). 25% of redundancy in the ramp would be sufficient with around 10% additional margin.

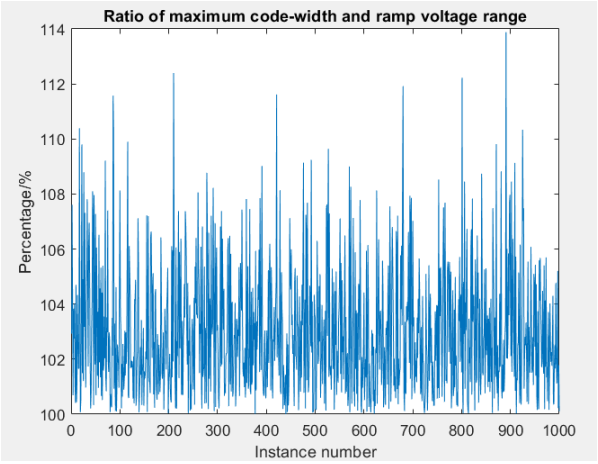


Figure 2.7: Matlab simulated maximum code-width.

2.1.4. ADC block diagram and timing

The proposed ADC block diagram, timing, and comparator input waveform are shown in Fig. 2.8. Central circuits are shared by 905 column-level ADCs, including the timing logic triggering different ADC modes and the 4-bit ramp generator. The clock cycles needed for MSB decision, SAR conversion, and RAMP conversion are 1, 8, and 20 respectively. An adder is used to combine the results of different modes.

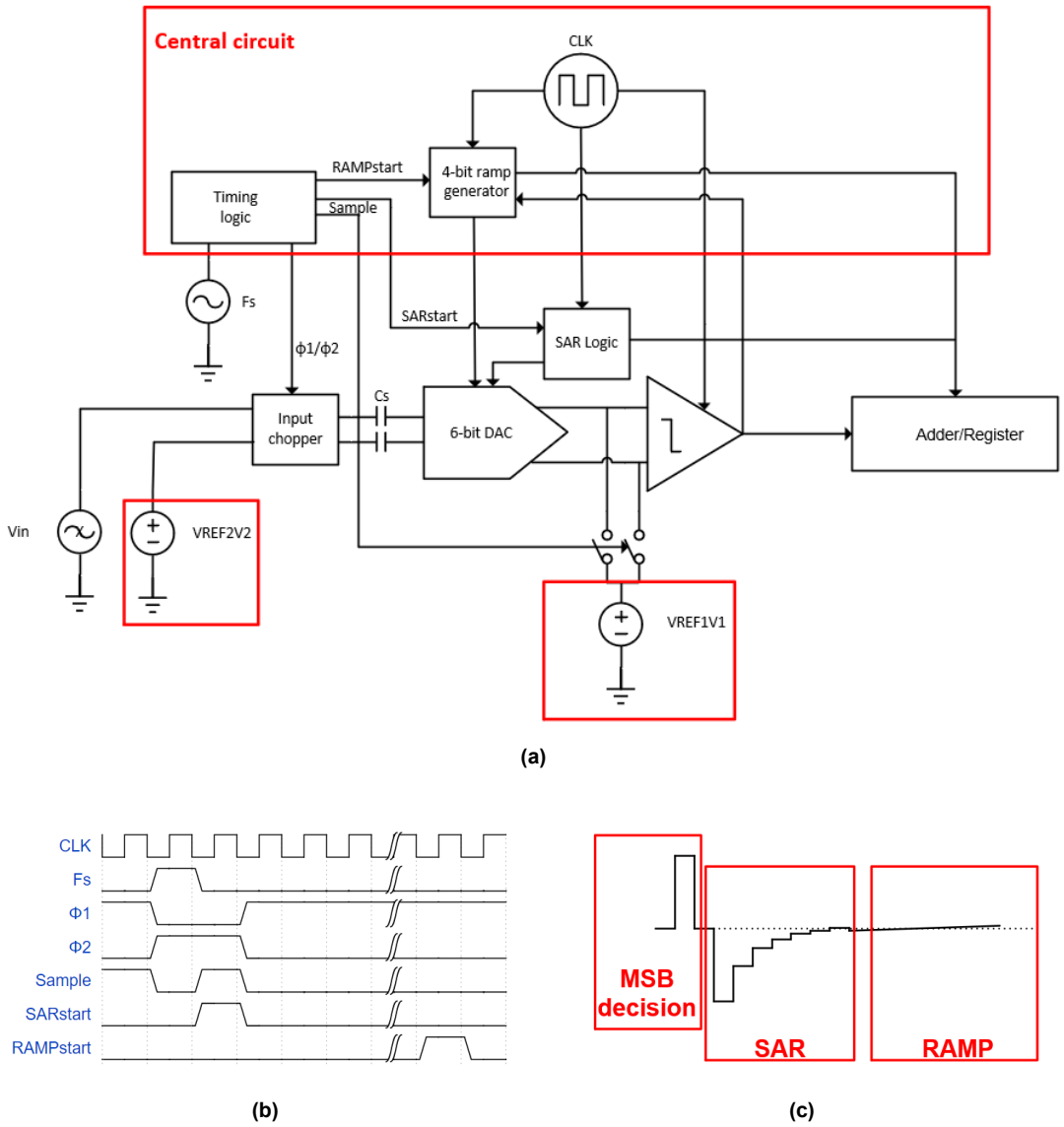


Figure 2.8: Proposed ADC (a) Block diagram. (b) Timing waveform. (c) Comparator differential input.

2.2. Linearity Analysis

Mismatch is the main factor degrading ADC linearity. It is a common issue for all the ICs, due to the non-idealities in the fabrication process. For example, the device dimension may differ from the designed value due to edge effects. Different parts of the IC might have different doping densities. The typical way to reduce mismatch is to increase the area of the device. Trimming and calibration are also possible if the added circuit/complexity is affordable. Besides, efforts in layout like adding dummies to ensure a similar environment and placing critical devices closely and symmetrically, are also important.

The most stringent linearity specification in this project is DNL < 0.8 LSB. As the polarity of the sampled differential voltage determines the MSB, only 10 bits are determined by the 6-bit DAC and the 4-bit RAMP. Hence, the ADC DNL requirement is relaxed to 10 bits as well. The ADC DNL is determined by the DAC DNL. Considering

a 6-bit charge-redistribution-based DAC in the SAR and a 4-bit resistor-ladder ramp (see Fig. 2.9), the DNL of the hybrid DAC is mainly determined by the capacitor DAC.

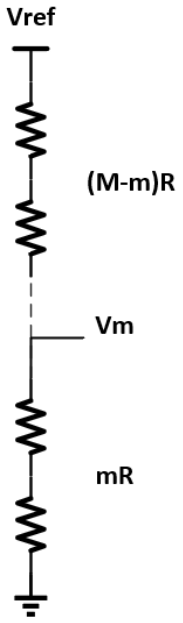


Figure 2.9: Resistor ladder with M resistors.

To illustrate this, we assume the resistors have an RMS mismatch of σ. V_m is the output analog voltage of code m. V_{m+1}-V_m and its variance $\sigma^2_{Vm+1-Vm}$ would be:

$$V_{m+1} - V_m = \frac{1}{M} V_{ref} = V_{LSB} \tag{2.2}$$

$$\sigma^2_{Vm+1-Vm} = \sigma^2_R * V^2_{LSB} \tag{2.3}$$

So the DNL of the ladder is given as:

$$\sigma_{DNL} = \sigma_R \tag{2.4}$$

Similar analyses apply to other types of unary DAC with similar results. Unary DAC performs well in DNL as only a single unit element's mismatch contributes. Moreover, since the ramp is central and shared by the whole pixel array, it could be implemented with low area consumption, thus a slight mismatch and negligible contributions to DNL.

A 3.2 fF unit cap is chosen from the allocated DAC area in a column. A sandwich capacitor is chosen to ensure better isolation of the capacitor top plate connected to the comparator input (see Chapter 3.2). Silicon-proven measurements ensure σ = 0.5% mismatch for such a structure.

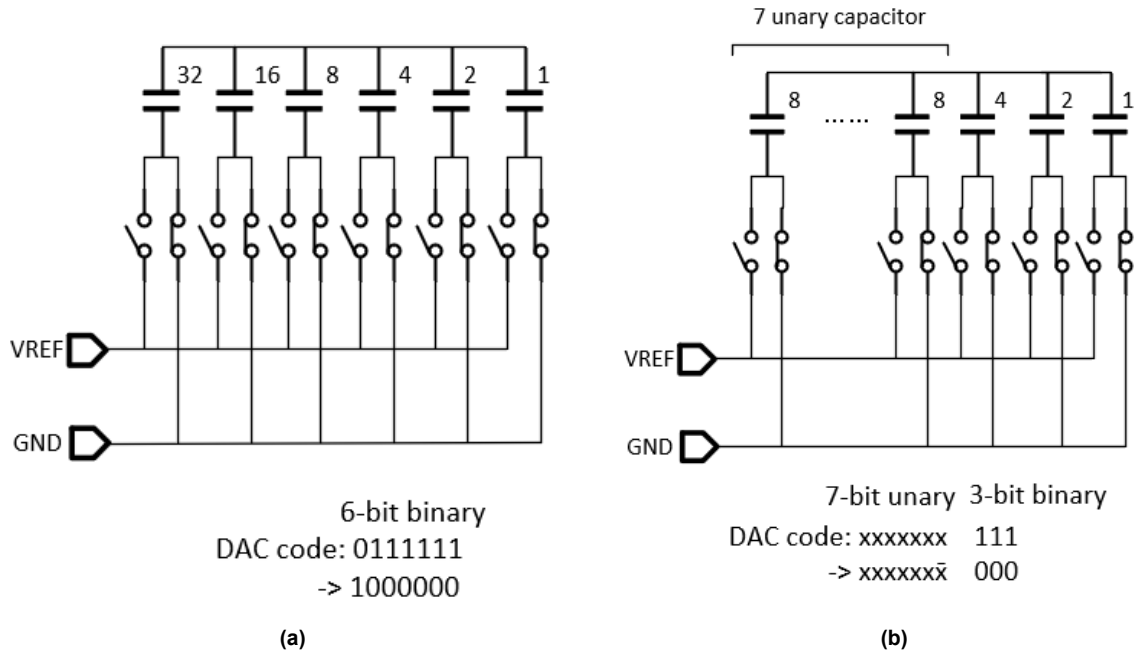


Figure 2.10: Worst DNL code for (a) 6-bit binary DAC. (b) 3-bit unary MSB + 3-bit binary LSB.

For a 6-bit binary DAC, the worst DNL is in the mid-code transition when all capacitors are toggled (see Fig.2.10a). As all capacitors are involved in this transition, the differential 6-bit binary DAC mid-code's code width and the variance would be:

$$V_{100000} - V_{011111} = V_{MSB} - \sum_{n=0}^{4} V_{SARLSB+n} \tag{2.5}$$

$$\sigma^2_{V_{100000}-V_{011111}} = 2\times \sum_{n=0}^{5} 2^n \sigma^2_{cunit} (\frac{V_{SARLSB}}{2})^2 = 31.5\sigma^2_{cunit} V^2_{SARLSB} = 8064\sigma^2_{cunit} V^2_{LSB} \tag{2.6}$$

So the DNL of the binary DAC is given as:

$$\sigma_{DNL} = 90\sigma_{cunit} = 0.45LSB \tag{2.7}$$

Thus a fully binary implementation would lead to a 3σ DNL of 1.35 LSB. To reduce the maximum DNL, the first 3-bit of the DAC is thermometer-coded. The worst DNL code now only involves the binary capacitors and one unary capacitor (see Fig. 2.10b) and is given as:

$$\sigma_{DNL} = 30\sigma_{cunit} = 0.15LSB \tag{2.8}$$

So the 3σ DNL of the 3-bit unary + 3-bit binary DAC is 0.45LSB.

Matlab DNL simulation confirms the 6-bit binary DAC's DNL calculation, while the 3-bit unary + 3-bit binary DAC's DNL is 1.4 times larger than the calculation (see Fig. 2.11). This is because the calculation assumes the worst DNL involves one unary capacitor and all the binary capacitors, while in reality, the worst DNL involves the

unary capacitor with the worst mismatch in the 3-bit unary DAC and all the binary capacitors.

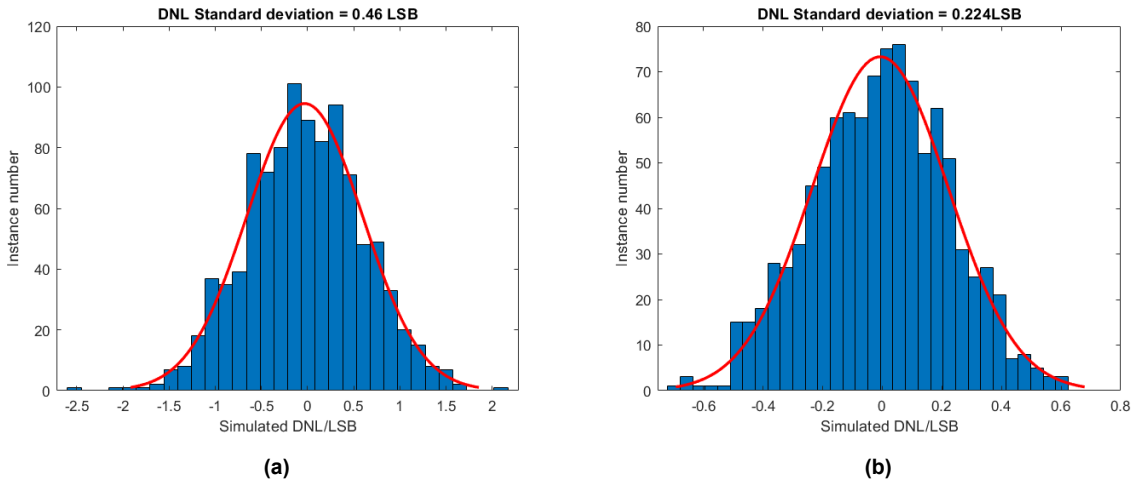


Figure 2.11: Matlab Monte Carlo simulation (1000 instances) (a) DNL distribution of the 6-bit binary DAC. (b) DNL distribution of the 3-bit unary + 3-bit binary DAC.

The simulated 3σ DNL of the 3-bit unary + 3-bit binary DAC is 0.67 LSB and is within specification.

2.3. Noise Analysis

The three primary noise sources in the ADC are quantization error, sampling noise, and comparator noise.

For converters with a resolution larger than 7-bit, quantization error can be modeled as noise with a white spectrum if the input is sufficiently active. The RMS noise voltage derived from this is given as:

$$V^2_{quantization} = \frac{V^2_{LSB}}{12} \tag{2.9}$$

For our ADC with 2.2V FSR and 11-bit resolution, the RMS noise voltage of quantization error is 310 µV.

Sampling noise is determined the moment the common-mode switches are open. In the charge domain, a random noise charge adds to the comparator input. As Cs and Cdac are in parallel and both sampled, the noise charge variance is:

$$Q^2_{sample} = kT(Cs + Cdac) \tag{2.10}$$

After setting the common-mode voltage, the comparator input has no DC path to other circuit nodes, and the charge is fixed. The switching in the chopper/DAC changes the voltage at the comparator input, but it cannot influence the charge. Thus the sampling noise could be calculated with the noise charge, and the RMS value is:

$$V_{sample} = \sqrt{\frac{2kT}{(Cs + Cdac)}} \tag{2.11}$$

Due to the differential structure, a factor of 2 is added to the numerator. In this design, Cdac = Cs = 204.8 fF. The RMS sampling noise voltage is 141 μV.

In SAR ADC, the comparator noise's contribution to ADC noise depends on the LSB size, the switching algorithm used, and the RMS value of the comparator noise [21]. Typically, the comparator noise is referred to the input of the ADC with a transfer function of less than one. This is due to the different instantaneous comparator noise present at different comparisons during the SAR search.

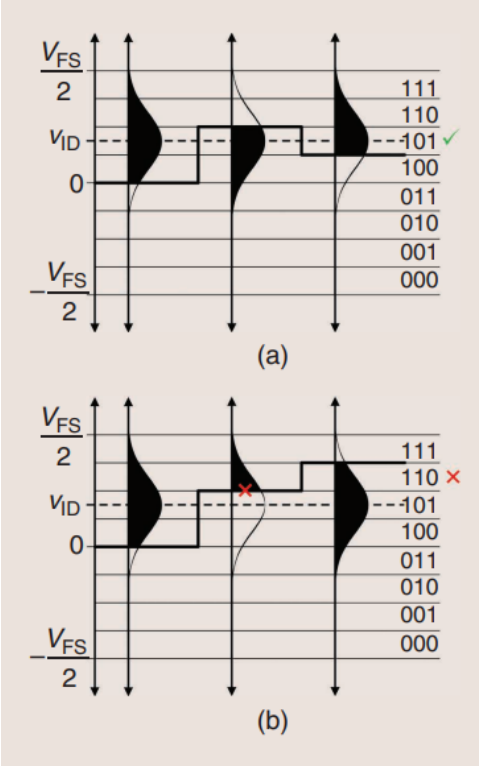


Figure 2.12: 3-bit SAR search comparator input waveform (a) Each bit is resolved correctly. (b) Comparator noise flips the second MSB decision.

A 3-bit example showing the successive approximation of a deterministic input in the presence of comparator noise is given in Fig. 2.12 [22]. If each bit is resolved correctly with comparator noise, the code error is 0. Suppose the instantaneous comparator noise leads to a decision error and flips the second decision. The third decision will likely be correct as the input differential voltage becomes larger due to the previous wrong decision. Only extreme noise could flip its decision and, finally, likely lead to a code error of 1 LSB. Such phenomena limit the code error due to the comparator noise, especially for larger comparator noise.

For a standard binary SAR algorithm, if the comparator noise is much smaller than the LSB size (for example, $\sigma_{comparator}$ = 0.2 V_{LSB}), directly adding the comparator noise to the ADC input-referred noise is a reasonable approximation, as the theoretic contribution is close 98% according to simulation [21]. If the comparator noise is comparable to the LSB size (for example, $\sigma_{comparator}$ = 1 V_{LSB}), 90% of the comparator noise would add to the ADC input-referred noise. The simulated RMS comparator noise in our ADC is 180 μV < 0.2 V_{LSB}. Hence, we assume the comparator noise is

directly referred to the input of the ADC.

The ADC total input-referred noise can then be calculated as:

$$V_{ADC} = \sqrt{V_{quantization}^2 + V_{sample}^2 + V_{comparator}^2} = 385\mu Vrms = 0.35V_{LSB} \tag{2.12}$$

3

ADC implementation

3.1. Input chopper

The input chopper consists of 4 switches connected to the input and bottom plates of Cs. The main non-ideality of a MOS switch is the charge injection when it turns off and the on-resistance when it is on. The first non-ideality results from the channel charge absorbed by the MOS switch when turned on to form the inversion layer as the channel. The channel charge of a MOS switch in a triode region is:

$$Q_{ch} = WLC_{ox}(V_{GS} - V_{th}) \tag{3.1}$$

W and L are the width and length of the transistor, C_{ox} is the oxide capacitance per unit area, and (V_{GS} - V_{th}) is the overdrive voltage.

These charges split and inject into two sides of the switch when the MOS switch turns off. The channel charge split to the sampling capacitor side creates an offset voltage on the ideal sampled voltage. As the channel charge is input-dependent, the offset is also input-dependent and introduces harmonic distortion.

The second non-ideality, the on-resistance of a switch, is modeled as:

$$R_{on} = \frac{1}{\mu \frac{W}{L} C_{ox}(V_{GS} - V_{th})} \tag{3.2}$$

Where μ is the carrier's mobility (either electrons or holes). R_{on} is also input-dependent and will introduce harmonic distortion when tracking high-speed signals. However, the input signal in this ADC is DC-like, so the contribution of R_{on} to the total harmonic distortion is negligible.

As bottom-plate sampling is adopted in the ADC, the common-mode voltage switch samples a fixed reference voltage with a fixed charge injection and on-resistance and fixes the charge at the comparator input. The charge injection of the input chopper switches is less of a concern as they do not affect the comparator input directly. The input signal is DC-like, so the signal dependant on-resistance of the switches is not problematic.

Thus four transmission gates (see Fig. 3.1a) controlled by complementary non-overlapping clock signals are adopted. With a transmission gate (see Fig. 3.1b) as the switch, the on-resistance is more constant over the entire input signal range, and the

introduced harmonic distortion is already negligible along with bottom-plate sampling. Non-overlapping clock signals (see Fig.3.1c) control the on/off of the switches to avoid a short circuit between Vin and VREF2V2. With a Set-Reset latch (SR latch), signals ϕ_1 and ϕ_2 cannot be high simultaneously (see Fig. 3.1d), so a short circuit is avoided. Buffers consisting of 4 inverters with a tapering factor of 2 are used to delay and increase the non-overlap period.

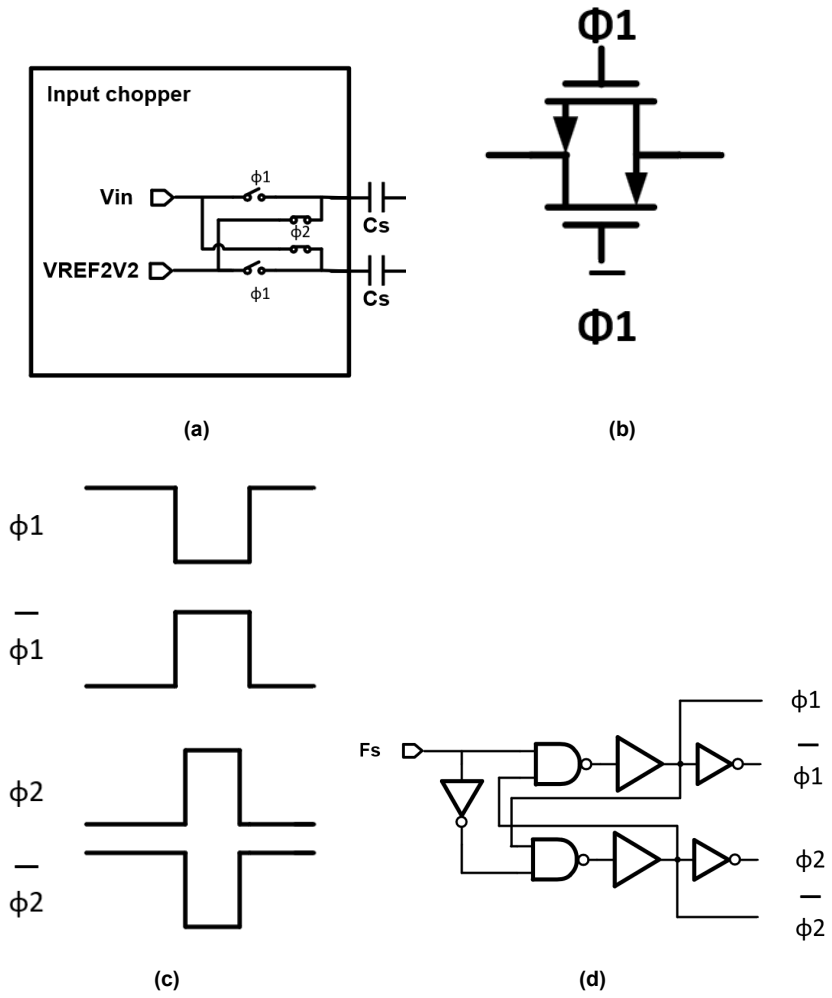


Figure 3.1: (a) Input chopper block diagram. (b) Transmission gate schematic. (c) Non-overlapping clock signal waveform. (d) Non-overlapping clock generator.

3.2. Unit cap and 6-bit DAC

The schematic of the 6-bit DAC with 64 unit caps is given in Fig. 2.10b. The unit cap is implemented with a ”sandwich” capacitor consisting of 3 metal layers (see Fig. 3.2). M2 and M4 are connected through vias and form the bottom plate. M3 is the top plate connected to the comparator input. The effective capacitance is proportional to the area of the two plates. With M3 dummies, the comparator input node is well-shielded from other circuit nodes at the price of larger parasitic capacitance to the ground. As discussed in Section 2.1.2, these capacitances only attenuate the signal/reference more and degrade the SNR. They do not degrade the linearity/FSR of the ADC.

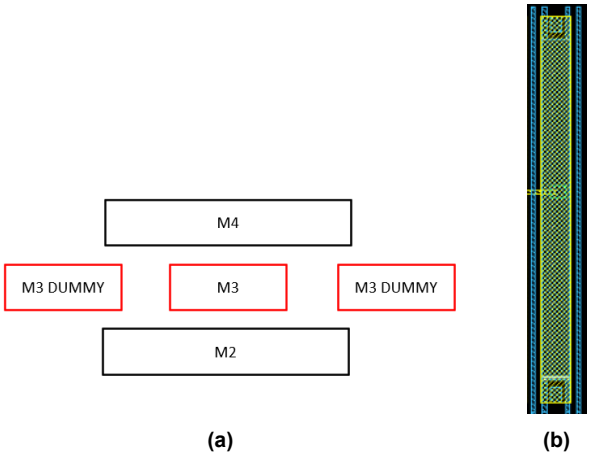


Figure 3.2: Unit cap (a)Cross section view. (b)Top view (dimension 0.5).

The settling time needed to meet 11-bit resolution is 8.3 τ. The DAC switches are sized to ensure low enough on-resistance to meet the settling accuracy.

The unit cap is laid out so that routing the digital signals for the DAC is possible within the available width. The dimension is 0.5 µm ×5.0 µm. The extracted unit cap capacitance is 4 fF, which meets the requirement for sampling noise (3.2 fF).

To improve DNL, the 6-bit DAC consists of 3 binary LSB segments with 4, 2, and 1 unit caps and 7 unary MSB segments, each with 8 unit caps. The 7 unary segments cannot be directly controlled with the 3-bit binary MSB codes and need a decoder.

The 3-bit binary to thermometer decoder schematic and truth table is given in Fig. 3.3. The 3-bit binary input is decoded to a 7-bit thermometer output, and two adjacent binary inputs will only have a 1-bit difference in the thermometer code.

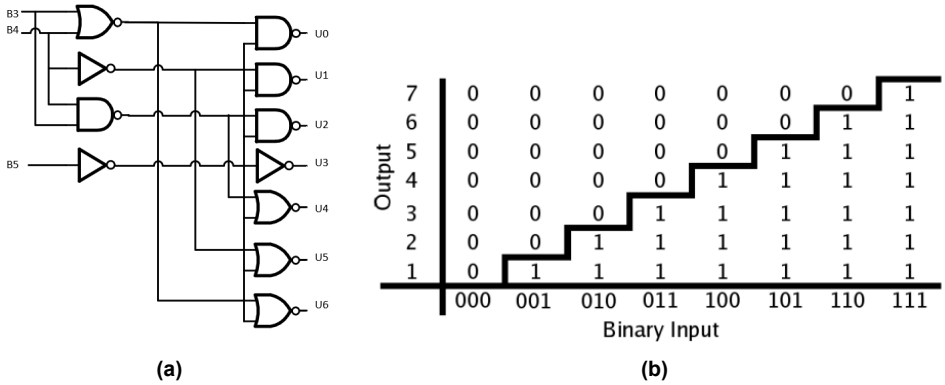


Figure 3.3: 3-bit binary to thermometer decoder (a) Schematic. (b) Truth table.

The binary segments are placed together on the bottom side of the DAC area for simplicity in the routing (see Fig. 3.4). The unary segments are placed in the common-centroid way to minimize the effect of stress and doping gradients across the long DAC area. All the digital signals are routed from the bottom side with wires in M1, M2, M3, and M4. Longer wires are placed further from the active area of the caps to minimize parasitics between capacitor plates and digital signal wires. The total area of the DAC is 7 µm × 340 µm.

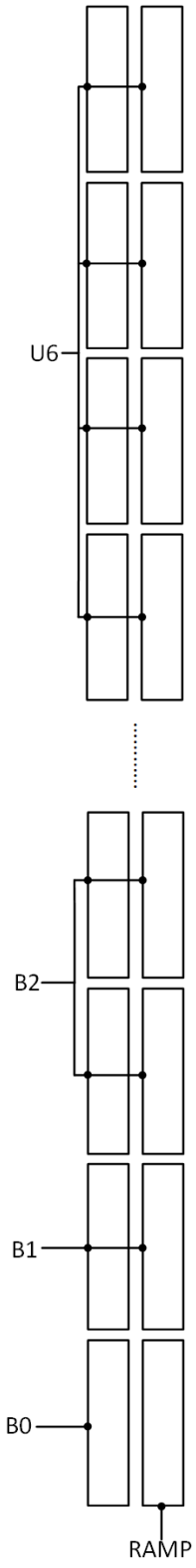


Figure 3.4: Layout placement of the 6-bit DAC. Due to the too-small width/length ratio of the DAC area, the actual layout is not shown.

3.3. Ramp generator

The ramp generator consists of two 4-bit unary DACs with 25 % redundancy, the 5-bit counter and 5-bit binary to thermometer decoder triggering the ramping, and a buffer to drive the unit caps in all the columns. When RAMPstart enables RAMP conversion mode, switches S1 and S2 are open. The counter counts up and drives the 5-bit binary to the thermometer decoder to switch the DAC to the other reference voltage one by one. A digital differential ramp is created and fed to all the ADCs through the buffer.

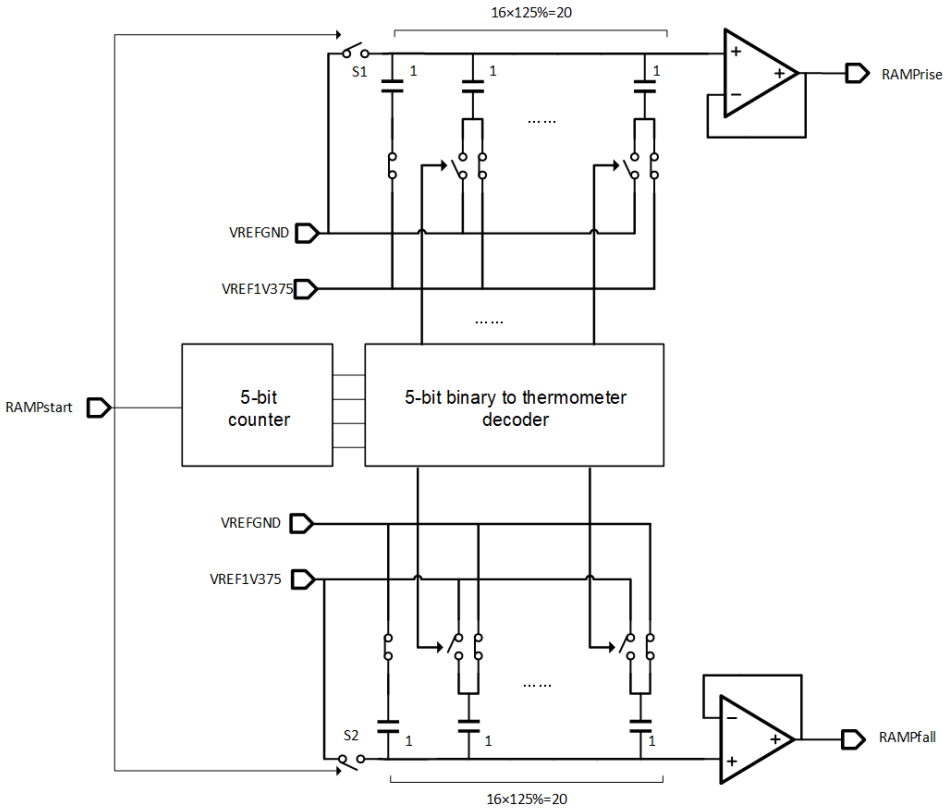


Figure 3.5: Ramp generator.

Linearity, noise, and speed should be considered during the design of the ramp. As discussed in Section 2.2, mismatch in the ramp has a small impact on DNL and is thus neglected. Ramp noise is also negligible, as in Section 2.1.3. Two processes determine the speed of the ramp. The first process is the settling after switching one capacitor. As the ramp signal is attenuated by $\frac{1}{64}$, the required settling accuracy is only 5-bit, and the settling time is negligible (less than 1 ns) with 5 ns settling time. The second process is the step response settling of the buffer. The buffer drives 905 unit caps, and the loading is 3.6 pF. As the ramp generator is central and shared by all columns, there is enough power and area budget for the buffer. An ideal buffer is used in this project due to limited time. The 5-bit counter and 5-bit binary to thermometer decoder are also implemented with Verilog-A.

3.4. Comparator

In this design, the double-tail latch is used as the comparator (see Fig. 3.6) [23]. Like other latches, it is fully dynamic with no static power consumption and decides fast even with small differential input due to the exponentially growing gain during regeneration. A latch is thus more power efficient in providing high gain compared with amplifiers and is a good comparator candidate in a sampled data system [12]. The main reason for choosing the double-tail latch instead of the popular strong-arm latch is the low dynamic offset obtained by separating the input differential pair and the latch transistors on two stages.

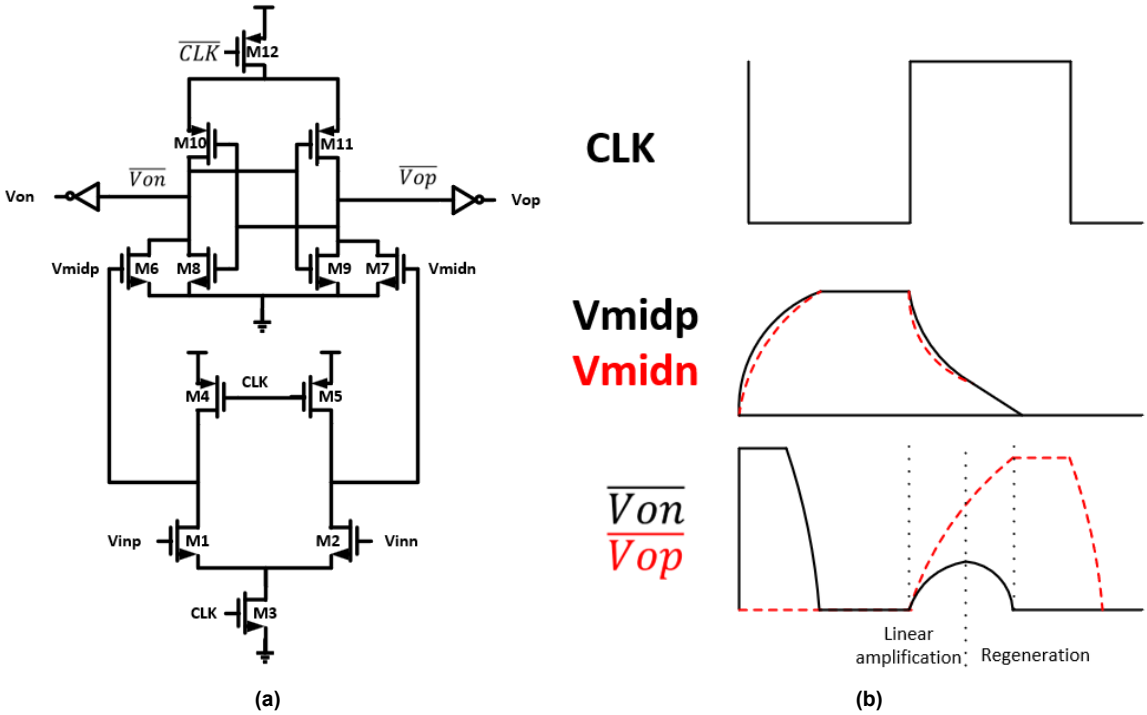


Figure 3.6: Double-tail Latch (a) Schematic. (b) Operation waveform.

The operation of this latch can be roughly divided into linear amplification and regeneration (see Fig. 3.6b). When CLK is low, tail switches M3 and M12 are open, and no current flows in the latch. M4 and M5 are closed and connect nodes Vmidp and Vmidn to supply. M6 and M7 are thus closed and connect output nodes $\overline{Vop}$ and $\overline{Von}$ to the ground. When CLK goes high, M3 and M12 are turned on and act as current sources. M4 and M5 are now open and thus allow Vmidp and Vmidn voltages to drop at a rate defined by rate $\frac{I_{M3}}{C_{mid}}$ (I_{M3} is the drain current of M3 and C_{mid} is the capacitance at node Vmidp/Vmidn), and on top of this, an input dependent differential voltage will build up. The inverters start regenerating the voltage difference as soon as the common-mode voltage at the Vmid nodes is no longer high enough for M6 and M7 to clamp the $\overline{Vop}$ and $\overline{Von}$ to ground. Two additional inverters are added at the latch output to separate from the following load and increase the speed.

The primary design considerations of a latch are the offset, noise, speed, and kick-back.

Offset analysis

The offset has a static component independent of the input common-mode voltage and a dynamic component that varies with the input common-mode voltage. The static component is mainly from the input differential pair's threshold voltage and node Vmid's parasitic capacitance mismatch. The dynamic offset is mainly from the inverters' (M8-M11) mismatch. Inverters' mismatch would be suppressed by the gain of M1/M2 and M6/M7 in the linear amplification phase when referred to the input and is negligible after fine-tuning during sizing and thus will not affect the ADC linearity. To limit the offset within requirements (5 LSB), 5-bit cap arrays are connected to Vmidp and Vmidn and controlled by a logic similar to SAR logic (see Fig. 3.7). The capacitors in the arrays are initially connected to the Vmid nodes. During an offset calibration phase before the normal conversions of the ADC, the comparator inputs are connected to the common-mode voltage. Then the comparator is enabled, and the offset now determines the decision. Depending on the comparator output, the capacitors are either switched to GND or not, from the largest capacitor to the smallest capacitor. In the end, the total capacitance difference from the arrays between Vmidp and Vmidn will adjust the voltage-dropping speed during linear amplification to cancel the offset of the latch itself. The capacitors are implemented with N-type MOS transistors for higher capacitance density and lower area. MOS capacitors-based DAC are problematic due to their non-linearity and large device mismatch, which can result in large DNL errors, limiting the calibration resolution. Thus redundancy is added to the three smallest capacitors by enlarging the width[1] to correct for any possible error in the MOS capacitors [24]. Latch offset is simulated by fixing one input to the common-mode voltage and the other input to a ramp signal around the common-mode voltage. A Montecarlo simulation shows an offset standard deviation equal to 6.5 mV_{rms}, and equal to 1.1 mV_{rms} after calibration (see Fig. 3.8).

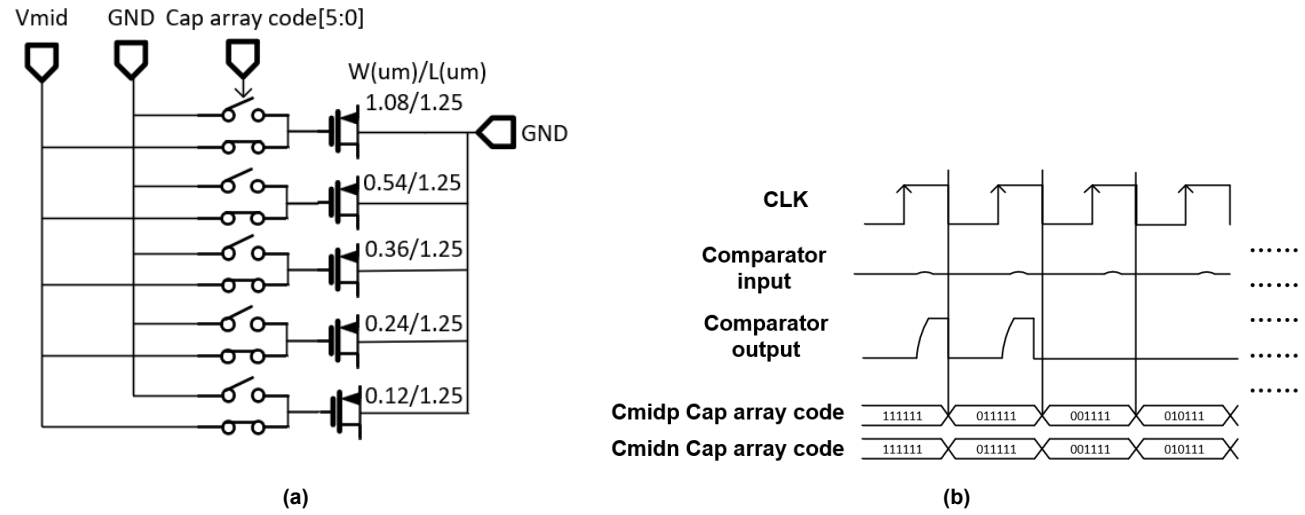
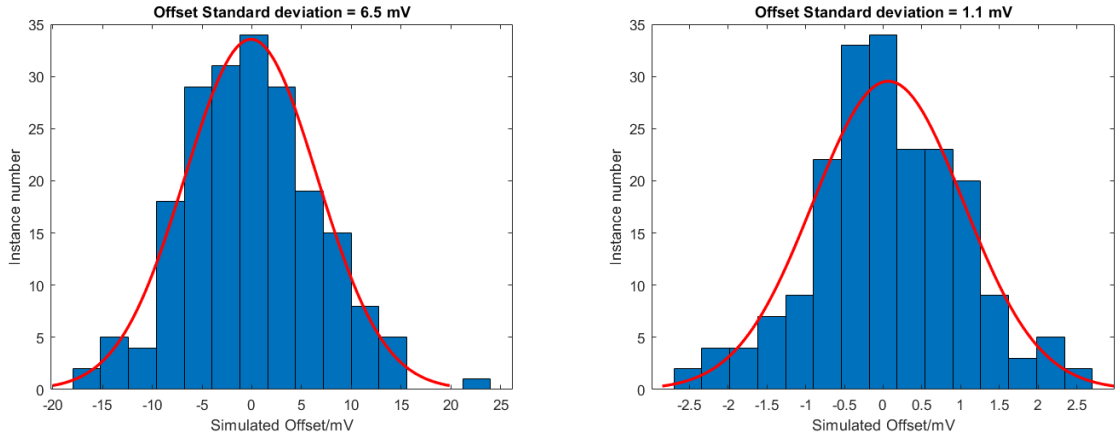


Figure 3.7: Offset calibration. (a) Cap array. (b) Waveform.

[1]The width ratio of the MOS capacitors are not fully binary but [12 6 4 2 1]



(a) (b)

Figure 3.8: Offset histogram (200 instances) (a) Before calibration. (b) After calibration.

Noise analysis

Noise analysis of latches is more complex than amplifiers due to the non-linear regeneration phase. One way to analyze their noise is to divide the operation of the latches into different phases [25]. By simplifying the latch at different phases with corresponding equivalent circuits and assuming sharp transitions between phases, noise is calculated with stochastic calculus in the time domain. Observing the derived equations from a strong-arm latch noise analysis, the main factors affecting latch noise are[2]:

1. The input differential pair channel thermal noise current integration on node Vmidp during the linear amplification. The input referred noise power and linear amplification time t_1 is:

$$\sigma_{M1}^2 = \frac{4kT\gamma}{g_{m1,t_1} t_1} \tag{3.3}$$

$$t_1 = \frac{V_{th,M6} C_{midp}}{I_{M3}} \tag{3.4}$$

In the equations, k is the Boltzman constant, T is the absolute temperature, γ is the noise factor with a value around 1, g_{m1,t_1} is the transconductance of M1 during t_1, $V_{th,M6}$ is the threshold voltage of M6, and I_{M3} is the large signal current through M3 during t_1. The noise could be reduced by increasing the product of $g_{m1,1}$ and t_1. The following strategies could be applied to do so:

- Decreasing the input common-mode voltage to push M1 into weak inversion with larger $g_{m1,t1}$. It also decreases the drain-source voltage of M3, so I_{M3} is reduced, which increases t_1.
- Decreasing the M3 width/increasing M3 threshold voltage to decrease I_{M3} and increase t_1.
- Increase $V_{th,M6}$ and/or C_{midp} to increase t1.

[2]The circuit is symmetric, so only the left half nodes are mentioned.

Also, increasing the W/L ratio of M1/M2 increases $g_{m1,t1}$ at the price of larger gate parasitic capacitance, attenuating the signal swing at comparator input which decreases the noise budget of the ADC to maintain the same SNR. Thus there is an optimum W/L ratio for M1/M2.

2. The $\frac{kT}{C}$ noise from opening the reset switches at node Vmidp. Increasing C_{midp} decreases its contribution at a speed price.
3. The noise from the latch transistors has a smaller contribution. They mostly operate during the regeneration when the output differential voltage grows exponentially towards one direction, so they are unlikely to affect the comparison result except with extreme values. Their contribution is more pronounced when transistor channel thermal noise increases at higher temperatures.

The noise of the comparator is simulated with periodic steady-state (PSS) analysis and periodic noise (PNOISE) analysis [26]. PSS analysis forces the comparator to run in a periodic steady state (for example, a clock signal with an identical waveform in every cycle is in a periodic steady state). Consequently, PNOISE analysis can capture any comparator internal node noise at any time of the periodic steady state defined in the simulation setup. In the case of a double-tail latch, by simulating the RMS noise of nodes $\overline{Vop}$ and $\overline{Von}$ at T during the linear amplification, the input-referred noise could be calculated with the gain A (see Fig. 3.9). The noise simulated from this method is very similar to the traditional noise-transient simulation that fits the output probability of 1 and 0 to the Gaussian distribution deriving the noise. However, PNOISE simulation runs much faster. Besides, noise contribution from different devices can be identified and provide designers insight into the noise sources.

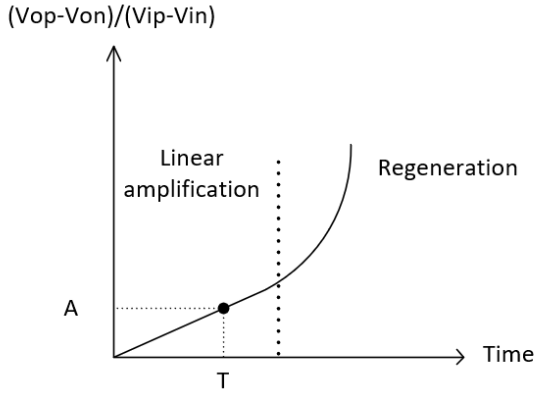


Figure 3.9: PSS+PNOISE noise simulation method.

Speed analysis

The speed of the comparator can be characterized through the linear amplification time T_{amp} and the latch's time constant τ. By applying a small differential input (0.25 LSB, for example) on the common-mode voltage, T_{amp}, A, and τ could be measured from the comparator output wave. The metastability probability could be calculated as follows:

$$P_{meta} = \frac{VDD}{e^{\frac{0.5T_{CLK}-T_{amp}}{\tau}} V_{LSB}} = 1.67\times10^{-8} \tag{3.5}$$

where VDD is the supply, T_{CLK} is the clock period, and V_{LSB} is the LSB size.

The mean time to failure (MTTF) can be calculated as:

$$T_{MTTF} = \frac{1}{FsP_{meta}} = 18s \tag{3.6}$$

Memory effect may appear if internal comparator nodes are not fully reset during the reset time. The reset switches M4 and M5 are sized wide enough to ensure adequate reset speed.

Kick-back noise appears when the exponential voltage change during regeneration is capacitively coupled back to comparator inputs, and it is generally not an issue in SAR ADC. The kick-back noise influences the comparator input voltage temporarily when the comparator has just finished a comparison and disappears after reset, thus having no impact on either the current or the next comparison (see Fig. 3.10).

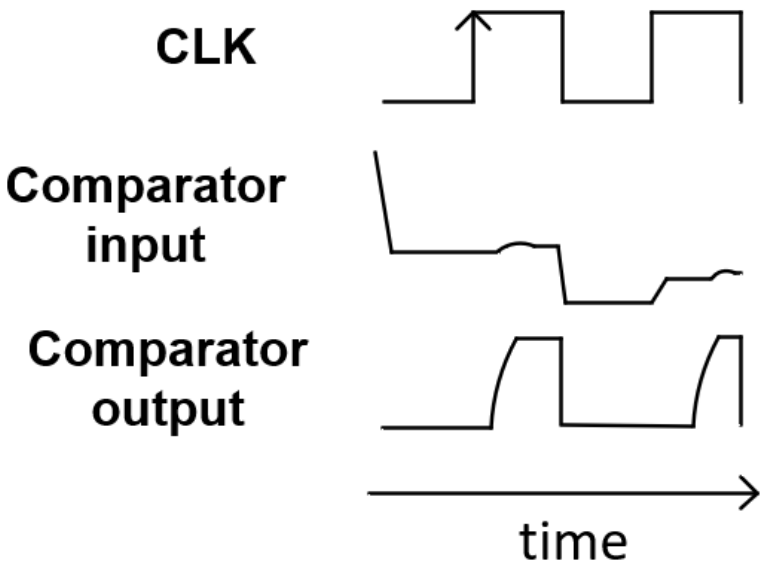


Figure 3.10: Comparator differential input, clock, and comparator output waveform.

Layout and performance summary

The layout of the comparator is shown in Fig. 3.11. Asymmetry in layout introduces about 40 μV systematic offset. Comparator post-layout performance at room temperature with nominal supply is summarized in Table 3.1.

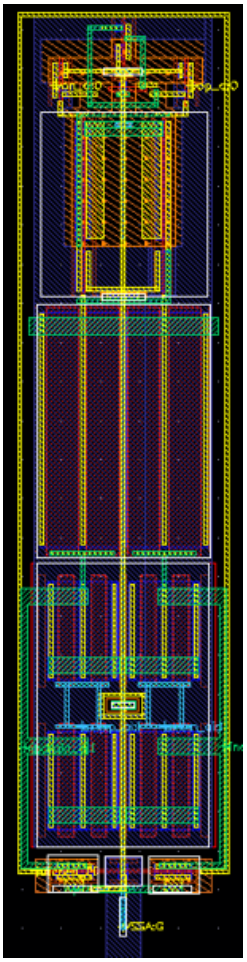


Figure 3.11: Comparator layout.

Parameter	Value
RMS Noise	0.17 V_{LSB} (180 µVrms)
RMS Offset	6 V_{LSB} (6.5 mVrms)
RMS Calibrated offset	1 V_{LSB} (1.1 mVrms)
Metastability	1.67×10^{-8}
Power consumption	18 µW
Area (with the MOS cap array)	7 µm × 35 µm

Table 3.1: Comparator performance.

3.5. Digital logic

SAR logic

The SAR logic consists of a shift register with 8 D-Flip-Flops (D-FFs), 7 D-FFs to store the comparator decision as the DAC code, 1 D-FF to store the MSB decision, and 7 multiplexers (see Fig. 3.12).

There are 2 additional D-FFs in the shift register compared with a standard 6-bit SAR logic. The first additional D-FF is to delay the SARstart pulse by one clock cycle. During this clock cycle, the D-FFs are reset by SARstart. The comparator has finished

the MSB decision, and the 1 D-FF stores the negative decision Von as MSB since 2's complement is used to represent the output code. MSB multiplexes the correct polarity of the comparator's output and 7 D-FFs' output to be used during the SAR search, so the correct FSR is set and searches toward the converging direction. The second additional D-FF is to add one more comparison after the SAR search to ensure the polarity of the residue voltage and switch the LSB cap to ensure the residue crosses zero during RAMP conversion (see Fig.3.13).

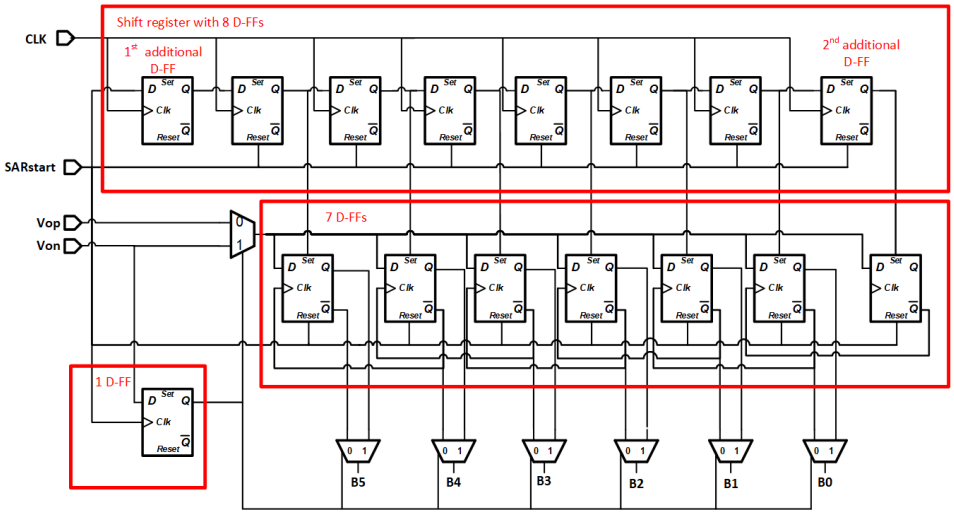


Figure 3.12: Schematic of SAR logic.

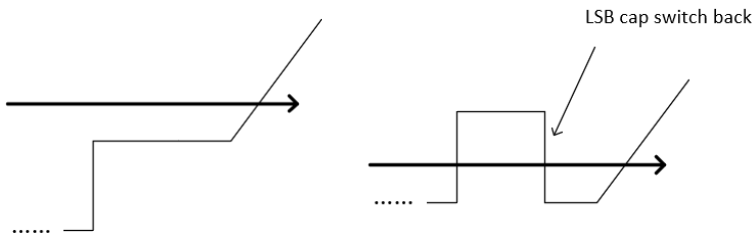


Figure 3.13: LSB cap (a) Not switched with the correct polarity. (b) Switch back to invert the polarity of the SAR residue voltage.

Adder

An adder combines the MSB, SAR result, and RAMP result due to the redundancy in the ramp. The result is represented with 2's complement to simplify the digital processing needed for the subtraction.

Fig. 3.14 gives the conversion waveform of a Vin > 2.2 V and the digital code corresponding to the analog voltage range. Since Vin > 2.2 V, MSB is 0 and indicates Vin is between 2.2 V and 3.3 V. SAR and RAMP convert the difference between Vin and 2.2 V. Directly adding their result gives the correct 11-bit result of the Vin. Table 3.2 gives the initial code of MSB, SAR, and RAMP results. The 5th bit in the RAMP result is redundant, and it needs to add with the LSB in the SAR result with possible

carry, while the 1st - 4th bits in the ramp result could be directly kept. The combined 11-bit result is initially 0.

For an analog input 2.2 + 0.5 V_{LSB}, the SAR DAC voltage will be 0 at the end of the SAR conversion. The RAMP voltage will be 1 V_{LSB} as only after one step in the ramp does it cross 0, and the comparator output inverts. The result digital code is 1.

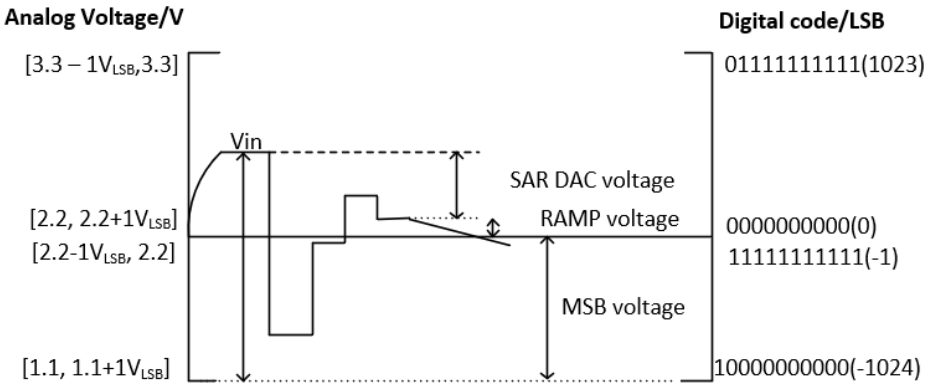


Figure 3.14: Conversion waveform of an input > 2.2 V.

	Binary code	Decimal value
MSB	0xxxxxxxxxx	0
SAR result	x000000xxxx	0
RAMP result	xxxxxx00000	0
11-bit result	00000000000	0

Table 3.2: Initial result when Vin > 2.2 V .

For a Vin < 2.2 V as shown in Fig. 3.15, MSB is 1 and indicates Vin is between 1.1 V and 2.2 V. SAR-RAMP converts the difference between 2.2 V and Vin, while the desired signal is the difference between Vin and 1.1 V. Thus the 1s and 0s in SAR result and RAMP result needs to be flipped which gives the desired difference between Vin and 1.1 V. Table 3.3 gives the initial code of MSB, SAR and ramp result. With redundancy in the ramp, the combined 11-bit result is 15.

For an input analog input 2.2 - 0.5 V_{LSB}, the SAR DAC voltage will be 0 at the end of the SAR conversion. The RAMP voltage will be V_{LSB}, and the result Digital code will be 14.

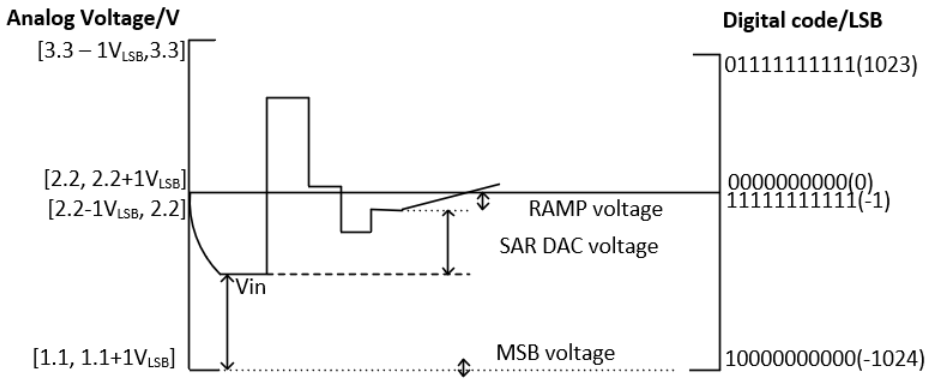


Figure 3.15: Conversion waveform of an input < 2.2 V.

	Binary code	Decimal value
MSB	1xxxxxxxxxx	-1024
SAR result	x111111xxxx	1008
RAMP result	xxxxxx11111	31
11-bit result	00000001111	15

Table 3.3: Initial result when Vin < 2.2 V.

Thus, an offset of 14 LSB exists between the results with different MSB. A simple fix is to add 14 LSBs only when MSB is 0. The final adder is shown in Fig. 3.16. MSB selects between the RAMP result and flipped RAMP result, adding 2+4+8=14 LSB if MSB is 0, by connecting MSB after an inverter to the 2nd, 3rd, and 4th full adder input.

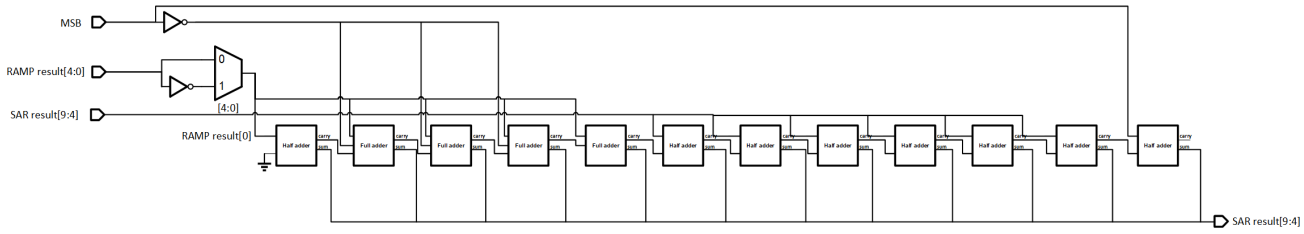


Figure 3.16: Adder to combine the results.

The offset introduced by the adder shifts the ADC FSR by 14 V_{LSB} (15 mV), and it is now between (1.1 V - 14 V_{LSB}) and (3.3 V - 14 V_{LSB}). This magnitude of the shift is acceptable in this project.

4

Summary

4.1. Simulation results

The ADC has been verified with the post-layout extracted view of the column-level analog circuits and the schematic view of the central/digital circuits, with an ideal ramp buffer and reference. Fig. 4.1 shows the post-layout noise-transient simulated output spectrum. To mimic the DC-like pixel signal during conversion, the input signal is an ideally sampled sine wave (see Fig. 4.2). The achieved SNDR is 64.3 dB, which results in an ENOB equal to 10.3 bits. The RMS noise is 470 µV = 0.43 LSB and is within specification.

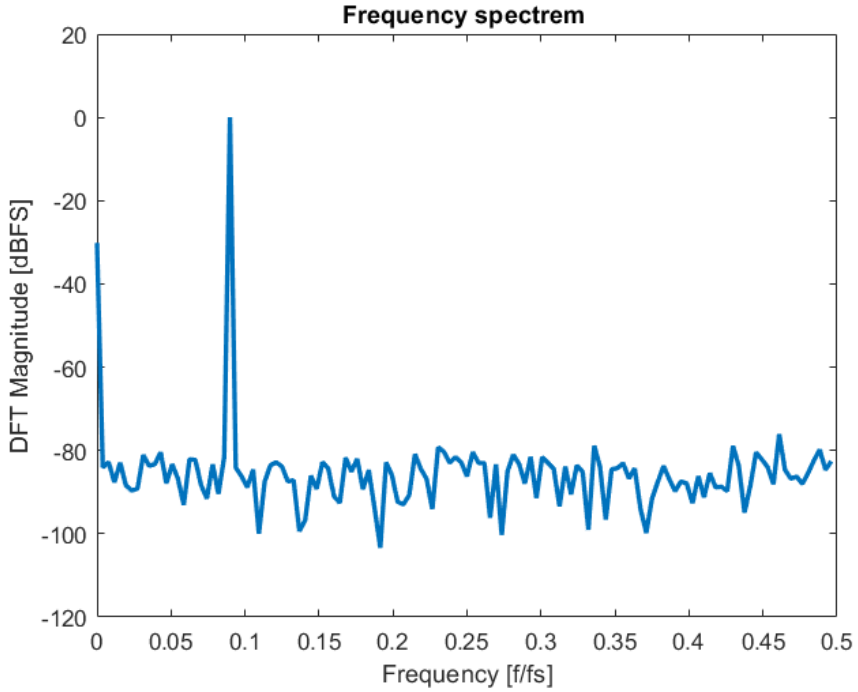


Figure 4.1: Post-layout noise-transient simulated output spectrum for Fin = 0.0898 MHz and Fs = 2 MS/s with a 256 points FFT.

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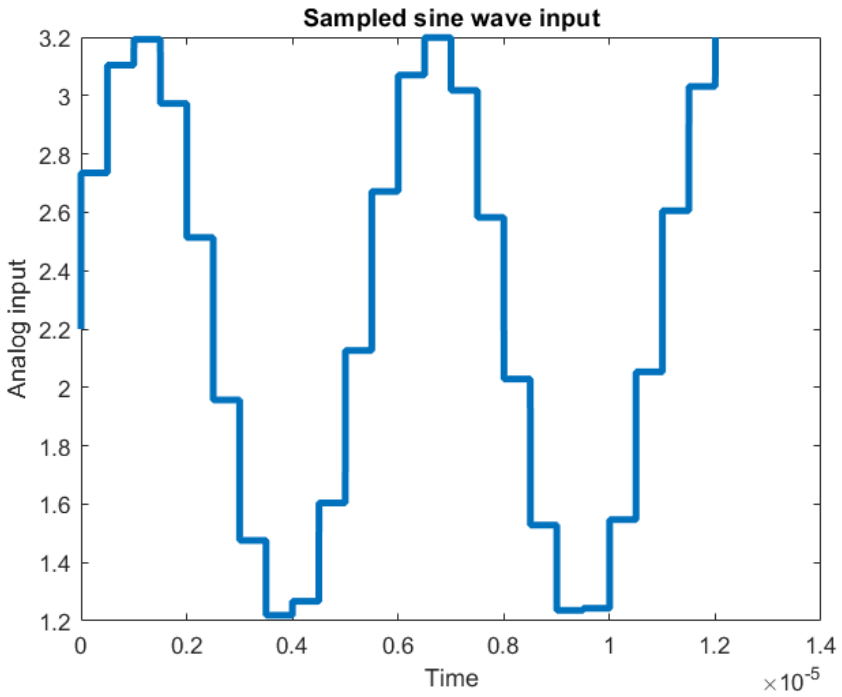

Figure 4.2: Ideally sampled sine wave with Fin = 0.0898 MHz and Fs = 2 MS/s.

Fig. 4.3 shows the simulated ADC power breakdown at room temperature under the nominal power supply of 1.2 V. The total power consumption is 45 µW. The power consumption is dominated by the digital logic (49%) and the comparator (40.8%), while the input chopper (4.5%) and DAC switching (4.5%) only contribute 9% of the total power. The power consumption of the reference and ramp is not considered as they are central blocks, and the average power on one of the 905 columns should be negligible. The resulting Walden figure of merit (FOM_W) is 106.8 fJ/conv-step[1].

[1]The sampling rate of the designed ADC could meet 3.3 MS/s while the required sampling rate is 2 MS/s. FOM_W is calculated with 3.3 MS/s.

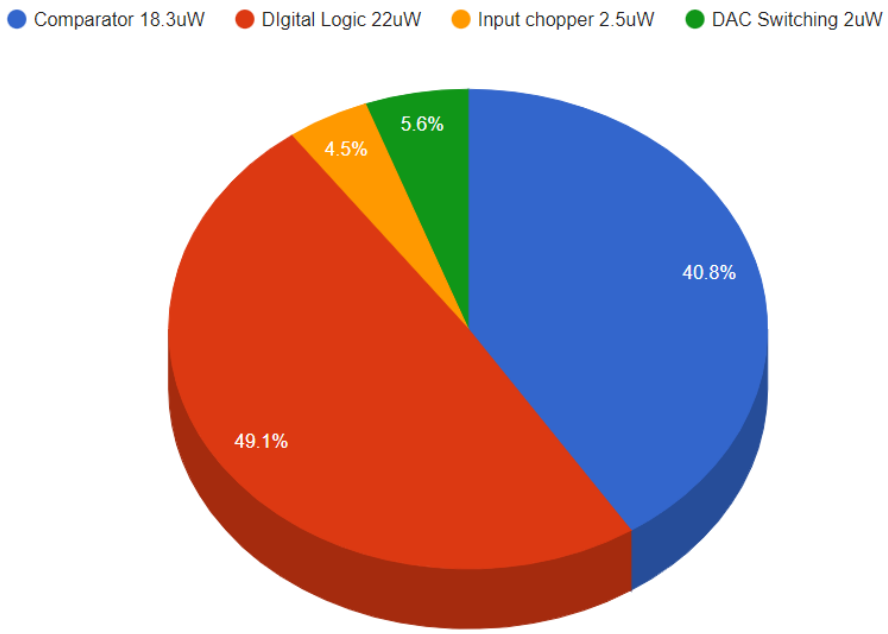

Figure 4.3: Simulated ADC power breakdown.

The simulated ADC performance is summarized in Table 4.1.

Parameter	**Value**
Technology	65nm
Resolution	11-bit
Sampling rate	3.3 MS/s
Input voltage range	1.1V - 3.3V
RMS Noise	0.43 V_{LSB}
Power consumption	45 µW
RMS Offset	1 V_{LSB}
Area	7 µm $\times$ 815 µm

Table 4.1: Performance summary of the designed column-level ADC.

4.2. Comparison

The FOM_W as a function of the area for state-of-the-art ADCs with a sampling rate between 0.5 MS/s and 10 MS/s is given in Fig. 4.4 [27]. In similar technology nodes, this work occupies the least area while maintaining medium FOM_W, and with larger area, better FOM_W is observed. The main reason is that, the RAMP phase relaxed the DAC area by reducing unit caps from 2048 to 64, at the price of 2.5 times more comparisons and additional logic circuits than a pure SAR implementation which degrades the energy efficiency.

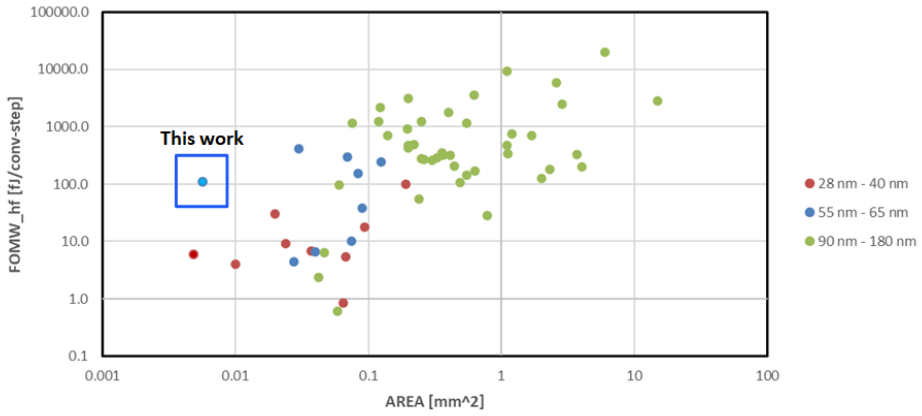

Figure 4.4: Comparison with state of the art.

Table 4.2 lists a performance comparison with other column-level imager ADCs from [27]. This work achieves the highest sampling rate and best FOM_W within one column area of the pixel array, thanks to the combination of power-efficient and fast SAR with area-efficient but slow RAMP with a shared ramp generator for the array. The area is relatively large due to the sandwich capacitor implemented DAC and sampling capacitors.

	[16]	**[15]**	**[28]**	**[29]**	This work
Technology	90nm	350nm	180nm	65nm	65nm
Resolution (bit)	12	11	11	12	11
Sampling rate (MS/s)	0.37	0.25	0.83	1.08	3.3
Architecture	SAR-RAMP	Two-step RAMP	SAR	Cyclic-SAR	SAR-RAMP
RMS Noise (µV)	527	490	527	414	470
Area (µm × µm)	2.24 × 998	5.6 × 450	7 × 350	4.4 × 920	7 × 815
Power (µW)	30	112	209	388	45
FOM_W (fJ/conv-step)	200	3000	2000	1400	107

Table 4.2: Comparison with column-level imager ADCs.

5 Conclusion

5.1. Discussion

In this work, an 11-bit column-level ADC for an I-ToF imager has been designed, and the core column-level analog blocks have been laid out. The post-layout simulated performance meets the requirements. By coupling the input signal through a dedicated sampling capacitor Cs instead of the DAC bottom plate, the proposed low-voltage ADC can convert the high-voltage signal directly and reduce the system-level complexity. Taking advantage of the DC-like input signal from the pixel:

1. A threshold comparison phase reduces 1-bit resolution in the RAMP and improves the ADC speed and power consumption.
2. A chopper efficiently converts the single-ended signal to a differential signal, improving the SNR and gaining all the advantages of differential ADCs.

5.2. Limitation

The proposed architecture attenuates the input signal through capacitive division and reduces the signal swing to enable a higher-than-reference input range. Although the attenuation is compensated through the single-ended to differential conversion with the input chopper, the quantization error determined by the FSR and resolution is also scaled up, becoming the main limitation of ENOB at room temperature.

5.3. Future work

In further work, the SAR DAC and sampling capacitors can be implemented with metal-insulator-metal (MIM) capacitors with much higher capacitance density. This will increase the unit cap number in the limited DAC area so that more bits can be converted with SAR, reducing the clock cycles and power consumption.

Moreover, as quantization error limits the ENOB mainly, and if higher ENOB is desired, besides increasing the resolution, noise-shaping SAR could be implemented. One possible implementation is to replace the RAMP with a loop filter H_{EF} and perform over-sampling with the saved clock cycles (see Fig. 5.1). The loop filter shapes the residue voltage after the SAR conversion (effectively the quantization error) and sums it to the next sample. The Noise Transfer Function of quantization error (NTF_Q) is:

$$NTF_Q(Z) = \frac{D_{out}(z)}{V_{RES}(z)} = 1 - H_{EF}(z)z^{-1} \tag{5.1}$$

With H_{EF} approximating 1, quantization error could be significantly reduced, thus improving the ENOB. Although the column-level circuit becomes more complex, the central ramp is eliminated and greatly relaxes the layout efforts.

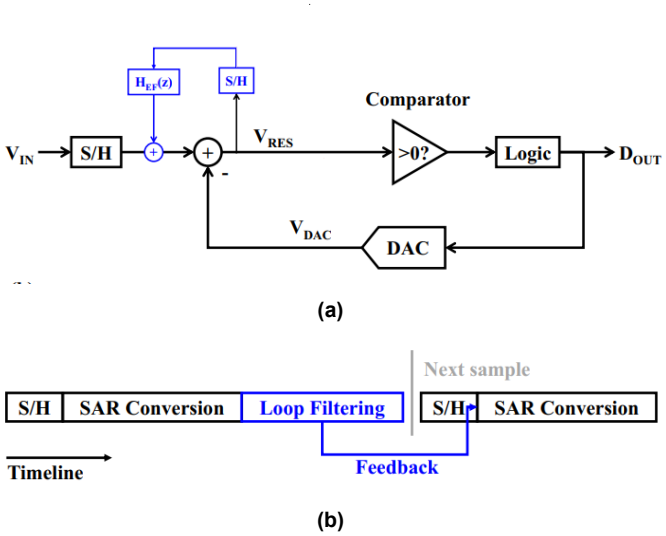

Figure 5.1: Noise-Shaping SAR. (a) A generalized model. (b) Operation timing. [30]

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