Beamforming Noise-Shaping SAR ADC for 3-D Ultrasound Imaging

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Abstract

3-D ultrasound imaging using a 2-D array provides much more information about our body than conventional 2-D imaging. However, due to the large number of elements in a 2-D array, channel count reduction is required and the power and area budget for each element is limited. It is quite challenging to design an ultrasound interface circuit with limited power and area budget. In the interface circuit, the ADC usually consumes considerable amount of power and area, which limits the performance of the whole system.

This thesis explores a new ADC architecture: a beamforming noise-shaping SAR ADC (BENSSAR), in an attempt to reduce power and area of the ultrasound receiver and thus improve the performance of 3-D ultrasound imaging. BENSSAR mainly consists of three parts: a subarray beamformer, a charge-sharing SAR ADC and a loop filter. They all operate in the charge domain, which makes the communication between each other efficient and thus reduces power and area.

Previously published works on noise-shaping SAR ADCs are all based on charge-redistribution SAR. In BENSSAR, the noise-shaping function is built based on the charge-sharing SAR. With the help of noise-shaping, the strict requirement on comparator noise, a disadvantage of charge-sharing SAR, is greatly relaxed. Since the error-feedback (EF) structure typically operates in the charge domain, this structure is very suitable for the charge-sharing noise-shaping SAR.

An active charge amplifier is implemented in the EF loop filter to achieve sufficient SNR improvement. The charge amplifier is realized by a current conveyor. We find out that the noise of the basic current conveyor is inherently limited but can be reduced by adding auxiliary amplifiers.

The BENSSAR has been designed in 0.18μm CMOS technology and has a subarray size of 9. The sampling rate is 30MHz. The BENSSAR consumes 1.31mW from a 1.8V supply and occupies an estimated area of 0.096mm^2. In a bandwidth ranging from 3.75MHz to 6.25MHz, the BENSSAR achieves a SNR of 63.25dB, an ENOB of 10.21 bits and a Schreier Figure of Merit (FoM) of 156.1dB.

Acknowledgements

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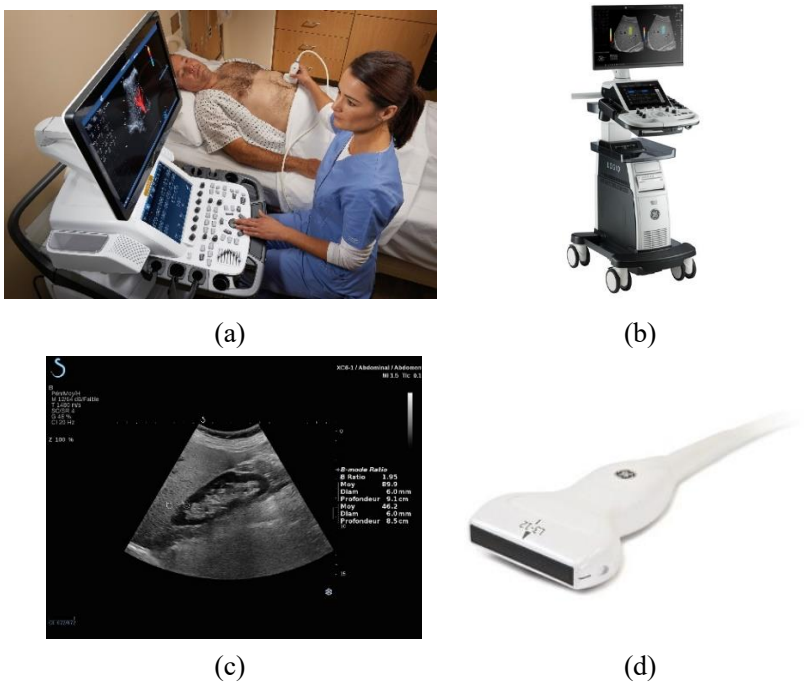
Contents

Chapter 1 Introduction

1.1 Background and motivation

Ultrasound has been widely used in medical imaging for decades due to its safety, cheapness and speed. Conventional ultrasound examination is done by an expert sonographer operating a cart-based imaging system (Figure 1.1(a)(b)). Typically, a 2-D B-mode image is obtained by means of a probe based on a 1-D transducer array (Figure 1.1(c)(d)). This conventional way has some shortcomings. First, the cart-based imaging system is bulky, which limits its usage scenarios and locations. Second, the 2-D image only shows a cross-section of our 3-D anatomy, which is insufficient for clinical diagnosis.



(a) (b)

(c) (d)

Figure 1.1 (a) an expert sonographer is operating a cart-based imaging system [1]; (b) Cart-based imaging system [2]; (c) 2-D B-mode image [3]; (d) probe with 1-D array used in cart-based imaging system [4].

To overcome these shortcomings, compact imaging systems with 3-D ultrasound imaging are required. In general, there are two ways to generate 3-D images, one is mechanically moving a 1-D array and the other is electronically scanning the anatomy using 2-D array, as shown in Figure 1.2. The first solution can be achieved simply by hand movements [5] or by using sophisticated mechanical structure [6]. They are both unprecise and slow. Furthermore, hand movements are highly dependent on the sonographer's experience and a sophisticated mechanical structure is difficult to make [7]. The second solution, electronically scanning using 2-D array, is fast and precise.

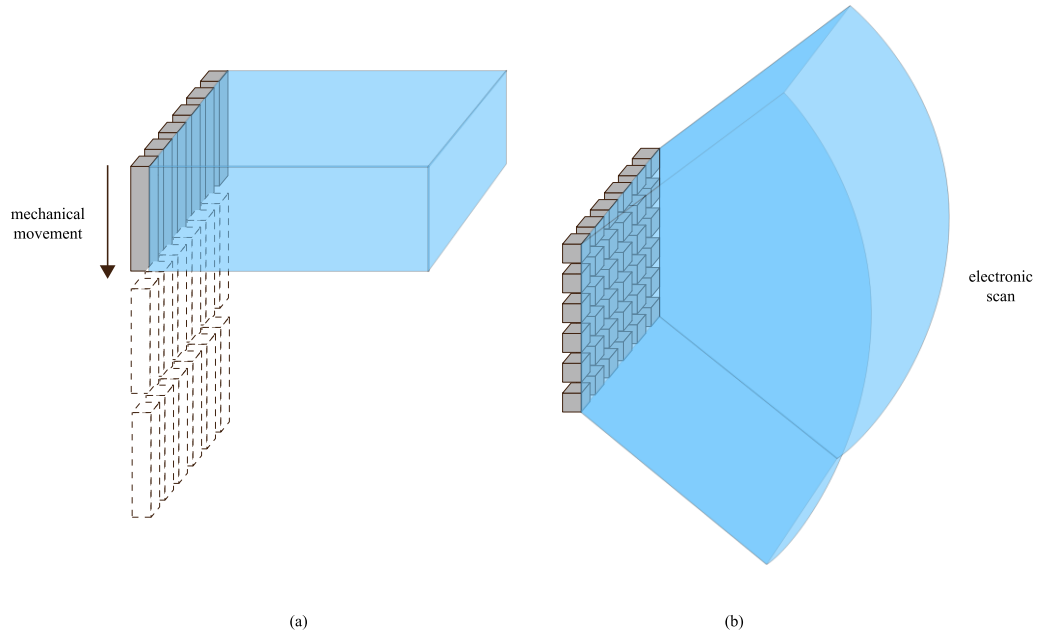


Fig 1.2 (a) mechanical movement using a 1-D array (b) electronical scan using a 2-D array

Electronic scanning is realized by beamforming as shown in Figure 1.3[1]. The acoustic waves reflected from a focal point arrive at each element at a different time. Then, they are converted into electrical signals. After adding a proper delay to each channel, these signals are aligned in time and can be easily summed up to generate a large signal. Acoustic waves from other directions cannot be aligned in time by the delay so there is no way to generate a large signal. It can be noticed that at a specific delay the system is sensitive to signals from a specific point. By varying the delay, the system can focus on different points in space and thus realize electronic scan.

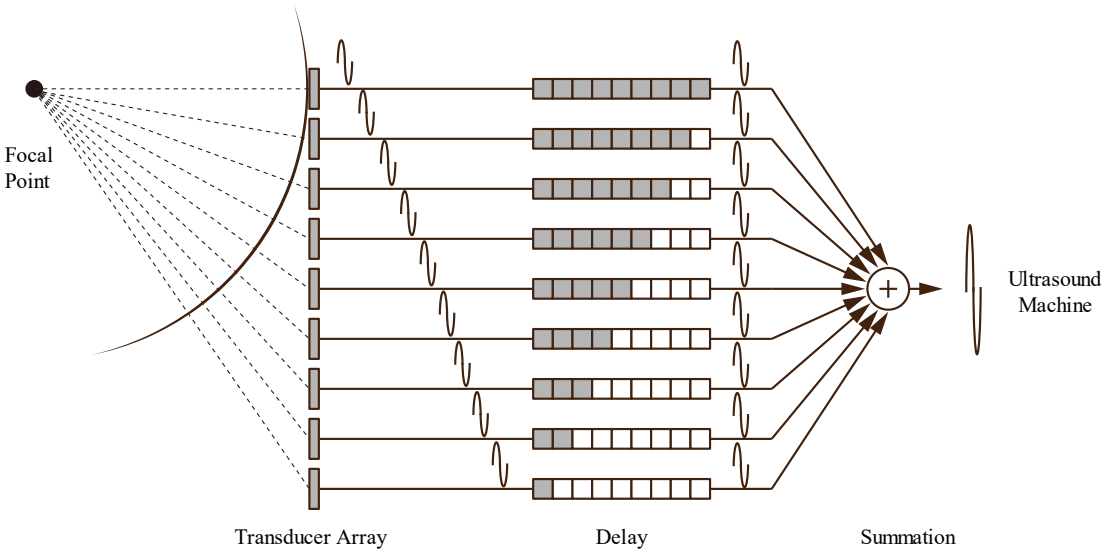


Fig 1.3 Basic Principle of Beamforming [8]

[1] For simplicity, 1-D array is used to explain the basic principle of beamforming

However, it is challenging to realize a compact 3-D ultrasound imaging system using a 2-D array. Since 2-D arrays have many more elements than 1-D arrays, the channel count increases with the number of the elements, so it is not possible to directly connect each element to an external imaging system using cables as in the conventional method (Figure 1.4(a)). Channel count reduction in the probe is required (Figure 1.4(b)) [9].

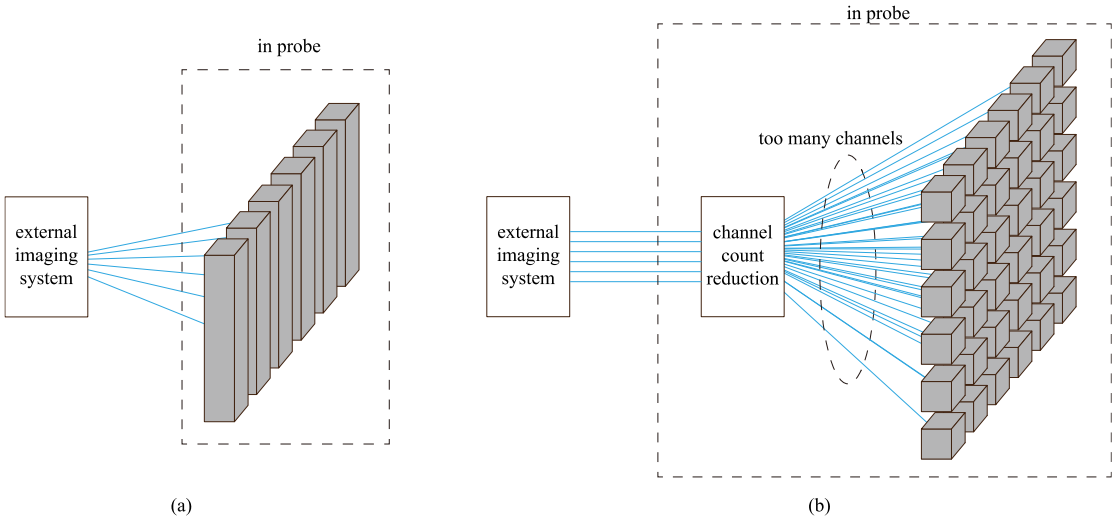


Fig 1.4 (a) Conventional 1-D array directly connected to the external imaging system (b) 2-D array with channel count reduction

Many solutions have been proposed to reduce the channel count including analog multiplexing [10,11], subarray beamforming [12,13,14,15] and digital multiplexing [14,15,18]. Digital multiplexing requires in-probe digitization, which might increase power and area of the whole system. However, in-probe digitization has the possibility to achieve a higher channel-count reduction than purely using analog techniques [14], which helps to reduce cable count and thus cost and size. In addition, transmitting data in digital domain is more robust and in-probe digitization makes it possible to perform digital processing in the probe, as will be needed in future handheld and wearable devices. Pure digital processing requires element-level in-probe digitization and thousands of ADCs should be integrated into the probe. Efforts have been made such as [19] and [20] but they have large area and power or low SNR.

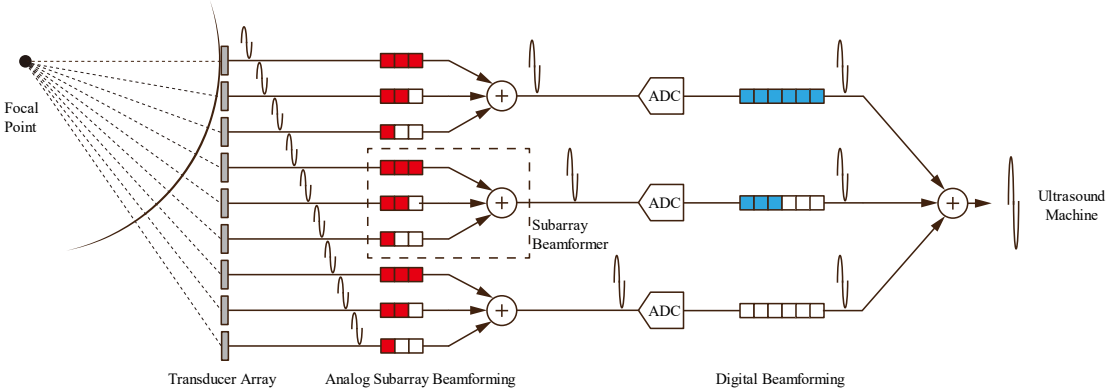


Figure 1.5 Subarray Beamforming [8]

Research shows that combining subarray beamforming and digital processing can achieve a better trade-off [13,14,15]. Subarray beamforming provides part of the delay in the analog domain and the rest is in the digital domain as shown in Figure 1.5. It can reduce the number of ADCs required, making total power and area acceptable. However, even with subarray beamforming, the ADC is still the main bottleneck. [14] reduces power and area by merging a charge-sharing SAR ADC and an analog subarray beamformer. [15] uses a single-slope ADC to derive the least-significant bits, further improving the performance. In [14] and [15], the ADC still consumes a considerable amount of power and area. A new architecture is required for better performance.

It is worth noting that ultrasound ADCs should oversample the input signal to reduce the side lobes caused by time quantization in digital beamforming [21]. Most of them such as [14], [15], [22] simply oversample without shaping the noise. We can naturally get SNR improvement if we add some noise shaping.

The noise-shaping (NS) SAR ADC has been proven to be power and area efficient, especially in the several kilohertz to several megahertz range [16,17]. The received ultrasound signals are usually at several megahertz, just within this range. Furthermore, the beamformer is mainly made up of delay elements, which can be seen as a FIR filter. It is attractive to merge it into the loop filter of the NS SAR to further save power and area.

The objective of this thesis is to explore the potential of organically merging the beamformer and the noise-shaping SAR ADC, in an attempt to improve the performance of 3-D ultrasound imaging. In this article, we call this architecture the beamforming noise-shaping SAR ADC (BENSSAR). The design detail will be described in the following chapters.

Table 1.1 Target Specifications

	This work	[14]
Process	180 nm	180nm
Supply voltage	1.8 V	1.8V
Subarray size	9	9
Maximum differential input amplitude	0.4V	0.4V
Sampling rate	30MHz	33MHz
Center frequency	5MHz	5MHz
Bandwidth	3.75MHz-6.25MHz	3MHz-7MHz
SNR	62 dB	51.8dB[II]
ENOB	10 bits	8.31 bits
Area	<0.099mm^2	0.099mm^2
Power	<1.55mW	1.55mW
FoMs[I]	>154.1dB	N/A

I Schreier Figure of Merit: $FoM_S = SNR + 10\log_{10}(\frac{Bandwidth}{Power})$.

II Including AFE noise.

1.2 Specifications

The idea of BENSSAR can be applied to various ultrasound applications with different specifications. Since this is a proof-of-concept design, we choose to set our specifications similar to [14] so that some circuit blocks can be reused and the performance can be easily compared to evaluate our idea. The specification is shown in Table 1.1.

1.3 Thesis organization

This thesis explores a new ADC architecture for 3-D ultrasound imaging: a beamforming noise-shaping SAR ADC (BENSSAR). The following chapters are arranged as follows.

Chapter 2 describes the architecture level design of BENSSAR. First, three individual topics: the subarray beamformer, the charge-sharing SAR and the noise-shaping SAR will be analyzed separately. Then, the merged BENSSAR is proposed and analyzed.

Chapter 3 discusses the circuit implementation of BENSSAR. The whole circuit structure is introduced first. Then, several components are described and analyzed, including feedback loop, CDAC and dynamic comparator.

Chapter 4 presents the simulation results of BENSSAR.

Finally, Chapter 5 concludes this thesis and also discusses future improvements.

Chapter 2 System architecture

In this Chapter, the system-level design of BENSSAR will be discussed. First, three key topics will be analyzed separately: the subarray beamformer, the charge-sharing SAR and the noise-shaping SAR. Then, the architecture of BENSSAR will be introduced based on this analysis and the system specification will be derived for the circuit level design (Chapter 3).

2.1 Analysis of key modules

2.1.1 Subarray beamformer[2]

The basic working principle of the beamformer has already been discussed in Chapter 1 and a mathematical representation will be given here. Assume the beamformer has N channels, associated with input signals $x_1(t)$ to $x_N(t)$ and delays t_{d1} to t_{dN}. The output $y(t)$ can be expressed as

$$y(t) = \sum_{i=1}^{N} x_i(t - t_{di}) \tag{2.1}$$

It can be noticed that the beamformer mainly performs summation and delay operations. The order of summation and delay leads to two types of circuit implementations. One is delay-and-sum and the other is sum-and-delay. A typical circuit implementation of delay-and-sum is based on analog capacitor delay lines and summation in the charge domain [14], while a sum-and-delay can be implemented by means of current-mode summation followed by boxcar-integration [23]. They will be discussed in sections 2.1.1.1 and 2.1.1.2, respectively.

2.1.1.1 Delay-and-sum beamformer based on capacitive delay lines

A delay-and-sum beamformer can be implemented using switch-capacitor memory cells as shown in Figure 2.1 [24]. The switch S_n and switch R_n control the writing and reading of the memory cell, respectively. Delay is realized by controlling the interval between writing and reading. Summation is realized by connecting the memory cells together at the output, which is basically a charge sharing process. On the whole, the beamformer first samples and stores the inputs $V_{in}[1]$ to $V_{in}[N]$ in the memory cells. After a certain delay, specific memory cells are connected together at the output and the summation is done.

This beamformer is simple, as it only consists of passive switch-capacitor memory cells. However, due to the delay-and-sum operation, 72 capacitors are required, which is far more than in a sum-and-delay beamformer (Section 2.1.1.2).

[2] "beamformer" is used to refer to subarray beamformer for the rest of the thesis

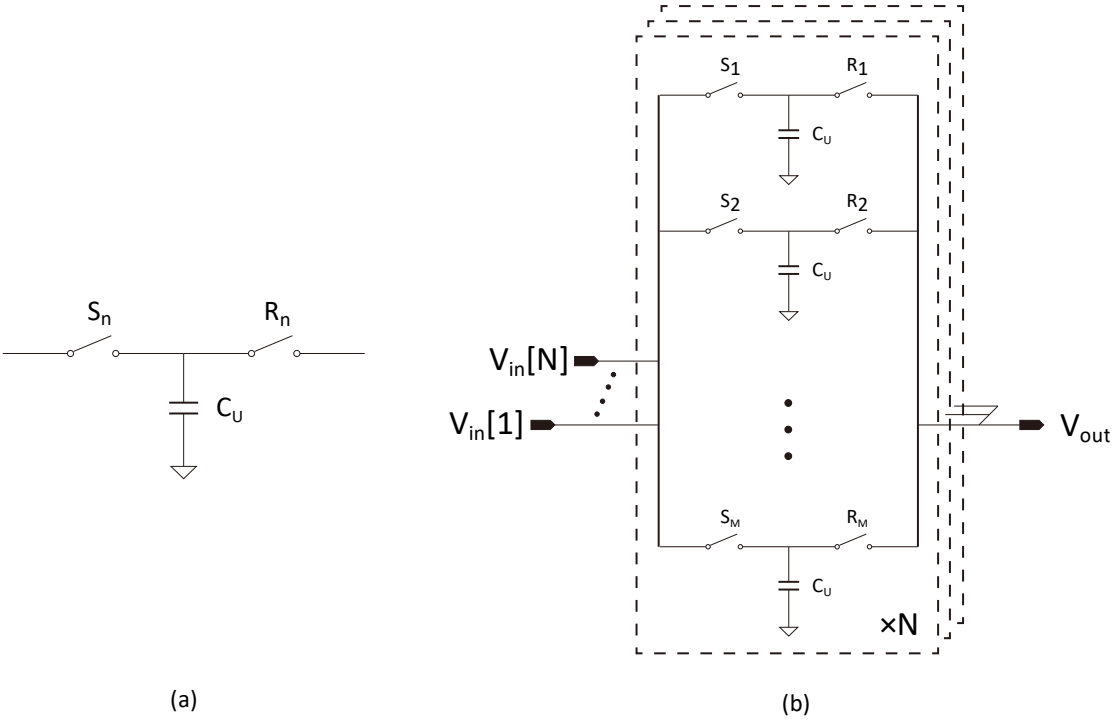


Fig 2.1 (a) Switch-capacitor memory cell [24] (b) Schematic of a delay-and-sum beamformer [24]

2.1.1.2 Sum-and-delay beamformer based on boxcar integration

The boxcar-integration-based beamformer first sums the input signals in the current domain and then stores the result on a memory capacitor as shown in Figure 2.2 [23]. Since summation happens before delay, only one memory capacitor is required per delay step instead of *N* memory capacitors.

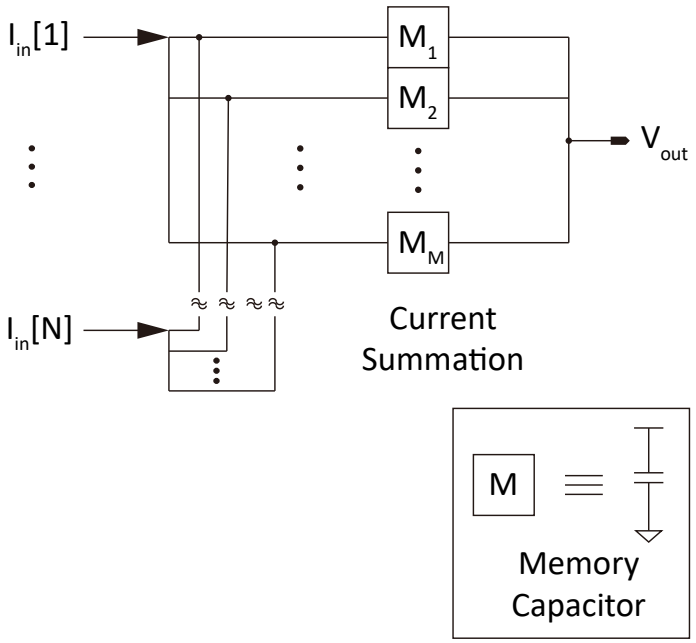


Fig 2.2 Boxcar-integration-based beamformer [23]

This solution greatly reduces the number of capacitors required, thus reducing the die area. Furthermore, due to the boxcar-integration process , the beamformer has a built-in anti-aliasing filter [23]. The downside of this beamformer is that it is challenging to guarantee sufficient linearity while maintaining low power consumption. In [23], OTAs are used which consume static current and the circuits are more complicated than a beamformer based on analog capacitor delay lines.

2.1.2 Charge-sharing SAR ADC

Unlike many scenarios where the ADC is responsible for both sampling and quantization, in an ultrasound system with subarray beamforming, sampling is typically done by the beamformer and the ADC is only responsible for quantization. Therefore, the input signal of the ADC is a sampled signal which is essentially in the charge domain. A buffer is required to convert the signal to the voltage domain if a conventional voltage-input ADC is used, as shown in Figure 2.3. The power consumption of this buffer can be comparable to the ADC itself [14].

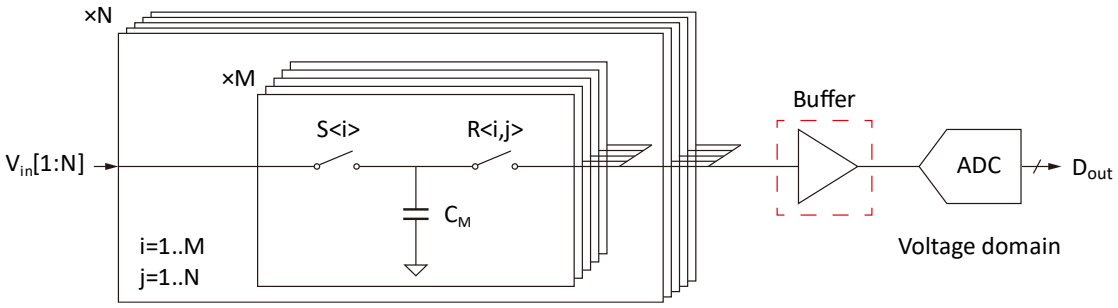


Fig 2.3 A delay-and-sum beamformer followed by a buffer and a voltage domain ADC [14].

To obviate the need for this buffer, it is preferred to quantize the signal in the charge domain as shown in Figure 2.4. Since we aim for a 10-bit resolution, the SAR ADC is a good candidate due to its excellent power efficiency. Therefore, the charge-sharing SAR is our choice. In this thesis, the charge-sharing SAR structure in [14] will be used as a main reference and a starting point.

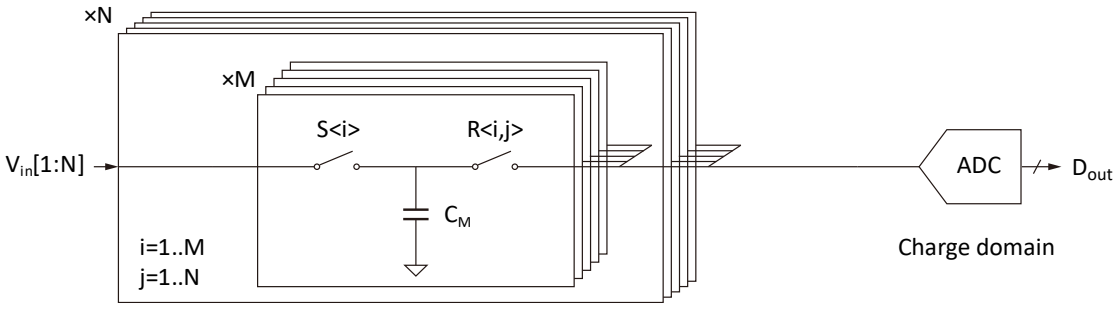


Fig 2.4 A delay-and-sum beamformer followed by a charge domain ADC [14].

The combination of a delay-and-sum beamformer and a charge-sharing SAR is shown in Figure 2.5 and its basic working principle is as follows. The beamformer first connects a specific memory capacitor of each channel, thus realizing passive charge summation. After a short time, the comparator detects the polarity of the voltage on the memory capacitors and makes a decision. Then,

a capacitor of the CDAC containing reference charge CV_{ref} is connected to the memory capacitors based on the decision, tying to neutralize the signal charge on the memory capacitors. Again, the comparator makes a decision. In the next cycle, a capacitor with reference charge $0.5CV_{ref}$ is connected. The ADC repeats this process until all bits have been resolved.

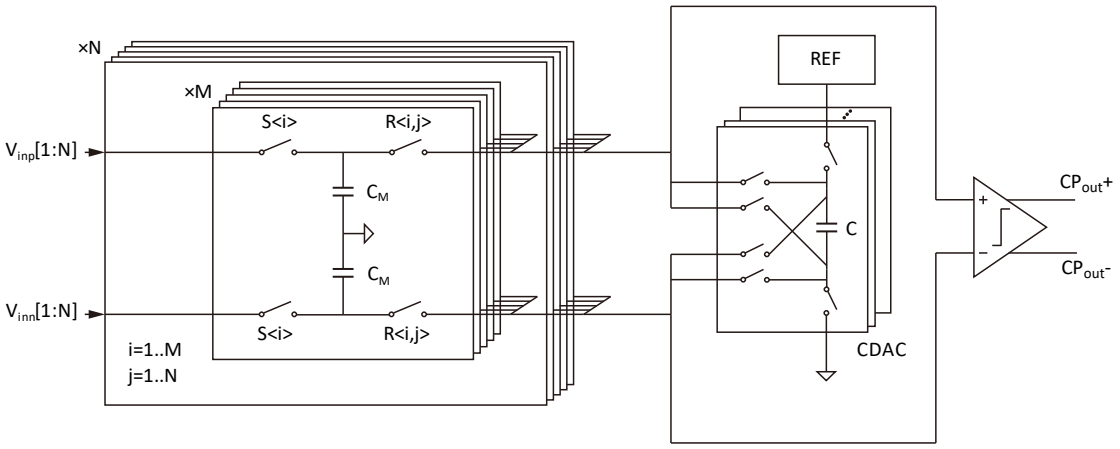


Fig 2.5 A delay-and-sum beamformer combined with a charge-sharing SAR ADC [14].

The key difference compared with a voltage-input charge-redistribution SAR ADC is that a reference charge instead of a reference voltage is used to neutralize the signal. The downside of the charge-sharing SAR ADC is that the voltage is attenuated during the conversion process, resulting in a higher requirement on the noise of the comparator. This shortcoming can be mitigated by noise-shaping, which will be discussed in the following sections.

2.1.3 Noise-shaping SAR ADC

Like conventional sigma-delta modulators, the noise-shaping SAR oversamples the input signal and shapes the quantization noise and part of the thermal noise with the help of a loop filter. Depending on the position of the filter in the loop, the noise-shaping SAR can be divided into two categories: the cascaded integrator feed-forward (CIFF) noise-shaping SAR and the error-feedback (EF) noise-shaping SAR [17].

2.1.3.1 CIFF noise-shaping SAR ADC

The block diagram of a CIFF noise-shaping SAR ADC is shown in Figure 2.6 [17]. After SAR conversion, the residual voltage V_{res} is present on the CDAC and it contains the information of the quantization error $E_q(z)$, thermal noise of the comparator $E_{n\_comp}(z)$ and the settling error $E_{settle}(z)$. By creating a loop filter $H_{CIFF}(z)$ in the forward path as shown in Figure 2.6, these errors can be shaped out of band of interest. The mathematical representation is:

$$D_{out}(z)=\frac{H_{CIFF}(z)}{1+H_{CIFF}(z)}\cdot V_{in}(z)+\frac{H_{CIFF}(z)}{1+H_{CIFF}(z)}\cdot(E_s(z)+E_{n\_LF}(z))+\frac{1}{1+H_{CIFF}(z)}\cdot(E_q(z)+E_{n\_comp}(z)+E_{settle}(z)) \quad (2.2)$$

$E_q(z)$, $E_{n\_comp}(z)$ and $E_{settle}(z)$ are shaped by gain $\frac{1}{1+H_{CIFF}(z)}$. $H_{CIFF}(z)$ should satisfy $H_{CIFF}(z)\to\infty$ in the band of interest to suppress the errors mentioned above. Therefore, $H_{CIFF}(z)$ is typically an integrator. However, also shown in the formula, the sampling noise $E_s(z)$ and the input-referred noise of the loop filter $E_{n\_LF}(z)$ are not shaped. Therefore, the loop filter should be carefully designed to reduce the noise $E_{n\_LF}(z)$.

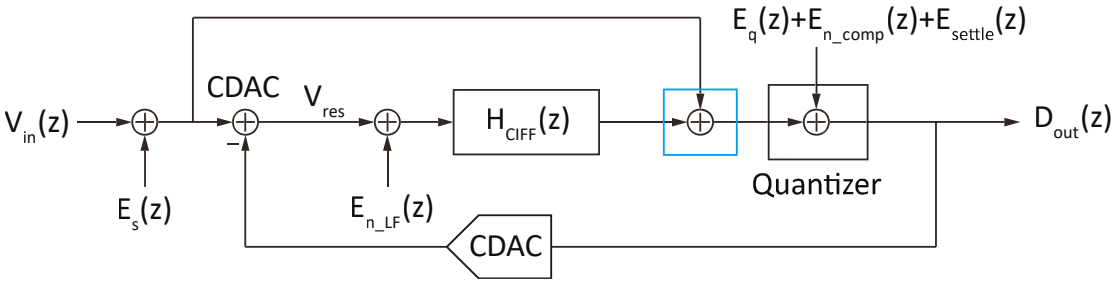


Fig 2.6 The block diagram of a CIFF noise-shaping SAR ADC [17].

It is worth pointing out that the CIFF path should be always active during SAR conversion. This is because, in the circuit implementation, the summation of the output of the SAR conversion and loop filter, shown in the blue box in Figure 2.6, is typically realized by a multi-input comparator [25] or capacitor stacking [26]. Both ways require a separate CIFF path during the SAR conversion, unlike the EF path being discussed in the next section. The downside of a multi-input comparator is the higher power consumption, while a shortcoming of capacitor stacking is that it suffers from parasitics.

2.1.3.2 EF noise-shaping SAR ADC

The loop filter of the EF structure is implemented in a feedback path, as shown in Figure 2.7 [17]. The residual voltage V_{res} is first filtered by $H_{EF}(z)$ and then added to the input. The mathematical representation is:

$$D_{out}(z)=V_{in}(z)+E_s(z)-H_{EF}(z)\cdot E_{n\_LF}(z)+(1+H_{EF}(z))\cdot(E_q(z)+E_{n\_comp}(z)+E_{settle}(z)) \quad (2.3)$$

$E_q(z)$, $E_{n\_comp}(z)$ and $E_{settle}(z)$ are shaped by gain $1+H_{EF}(z)$. Unlike $H_{CIFF}(z)\to\infty$ in the CIFF structure, $H_{EF}(z)$ should satisfy $H_{EF}(z)\to -1$ in the band of interest to suppress errors mentioned above. $E_s(z)$ is not shaped. Since $H_{EF}(z)\to -1$ in the band of interest, $E_{n\_LF}(z)$ is not suppressed by the loop filter either.

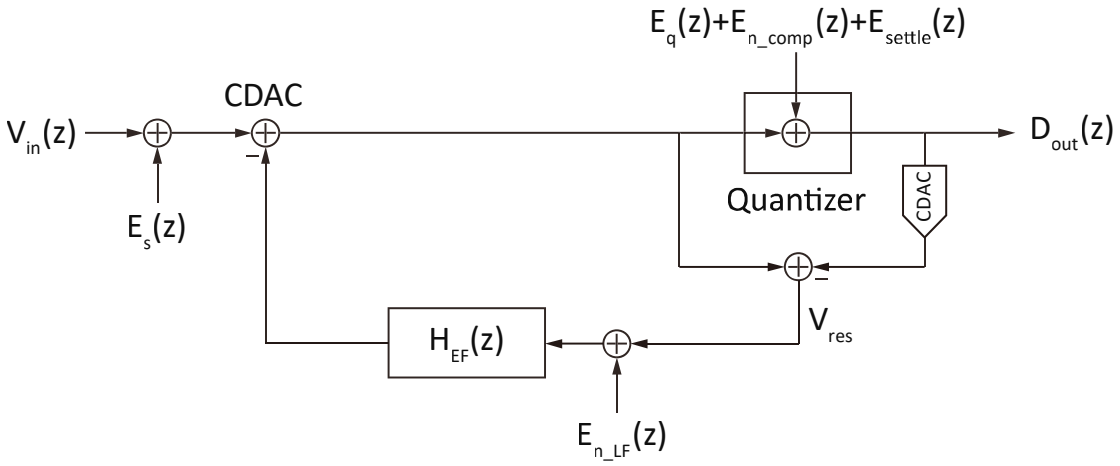


Fig 2.7 The block diagram of an EF noise-shaping SAR ADC [17].

Since the output of the loop filter is added to the input, no additional path needs to be always active during the SAR conversion, which is an advantage compared with the CIFF structure. The addition is typically realized by passive charge sharing at the SAR input. Furthermore, since $H_{EF}(z)$ is at the numerator of the gain $1+H_{EF}(z)$, a band-stop noise transfer function can be easily realized at the circuit level, by simply changing the feedback capacitor size for example. In contrast, $H_{CIFF}(z)$ is at the denominator of the gain $\frac{1}{1+H_{CIFF}(z)}$ and a local feedback path is typically required to realize a band-stop noise transfer function, which increases circuit complexity. The main disadvantage of the EF structure is that $H_{EF}(z)$ must be close to -1 instead of $H_{CIFF}(z)$ being close to infinite in the CIFF structure. It is more difficult to realize an accurate gain of -1 than a sufficiently large gain in the circuit implementation. In this sense, the EF structure is more susceptible to PVT variations than the CIFF structure.

2.2 BENNSAR

In the previous section, the key modules have been analyzed separately. However, in order to design BENNSAR, a hybrid architecture, interactions between these modules need to be taken into account. Therefore, based on the analysis of the individual modules, design choices will be made in this section. Then, the whole architecture will be presented and analyzed. The system parameters will be derived. System-level simulation results will also be presented. Finally, a conclusion of the system architecture design will be given.

2.2.1 Design choices

In this section, design choices of the SAR architecture, the loop filter of the noise-shaping SAR and the subarray beamformer will be made. We will not only be concerned with the performance of the module itself but also focus on how it will affect the whole system.

2.2.1.1 Charge-redistribution SAR vs charge-sharing SAR

The reason why the charge-sharing SAR is preferred over the charge-redistribution SAR in the ultrasound system with subarray beamforming has been explained in section 2.1.2. Taking noise-shaping into consideration, since they both perform successive approximation operations and both have the residual signal on the CDAC, both structures can be used to build noise-shaping SARs. Practically speaking, the noise-shaping SAR based on charge-redistribution has proven references [16,25,26,27], which will make the design easier. In contrast, there is no reference design for a noise-shaping SAR based on charge-sharing. Despite this practical disadvantage, we opt for a charge-sharing SAR because we do not want to lose the advantages mentioned in Section 2.1.2.

2.2.1.2 CIFF noise-shaping SAR vs EF noise-shaping SAR

As analyzed in previous section, the advantage of the CIFF structure is that it is more PVT-robust. The shortcoming is that the additional CIFF path should be always active during SAR conversion. In addition, it is more complicated to realize a band-pass ADC using the CIFF structure. In contrast, the advantage of the EF structure is that no additional path needs to be always active during SAR conversion. Furthermore, it is much easier to realize a band-pass ADC based on the EF structure. The downside of the EF structure is that it is difficult to control the gain of $H_{EF}(z)$ to be exactly one. Thus, it is more susceptible to PVT variation.

Since we decide to use the charge-sharing SAR, the EF structure is more suitable for the following reasons.

First, as mentioned in section 2.1.3.2, the summation between the input and the filtered residual is typically realized by passive charge sharing, which is exactly compatible with the charge-sharing SAR. In other words, both summation and SAR conversion operate in the charge domain, which eliminates the need for the voltage-to-charge conversion. In contrast, the summation between the input and the filtered residual in the CIFF structure is typically realized by a multi-input comparator or capacitor stacking which both operate in the voltage domain. The voltage-to-charge conversion is required in the CIFF structure.

Second, since our input ultrasound signal has a center frequency of 5MHz and a bandwidth from 3.75MHz to 6.25MHz, a band-pass design is better than a low-pass design. As mentioned previously, it is much easier to build a band-pass noise-shaping SAR ADC using the EF structure than the CIFF structure.

2.2.1.3 Beamformer based on analog capacitor delay lines or boxcar integration

As analyzed in the previous section, the advantage of a beamformer based on analog capacitor delay lines is its simple circuit structure and fully passive operation. The disadvantage is that more capacitors are required. In contrast, boxcar-integration-based beamformer requires fewer capacitors but increases circuit complexity and may need active component which increases the power consumption.

Taking noise-shaping into account, for a beamformer based on analog capacitor delay lines, additional capacitors are required to store the filtered residual charges $Q_{EF}[1]-Q_{EF}[K]$ as shown in Figure 2.8. $V_{EF}[1]-V_{EF}[K]$ are the outputs of the loop filter of the EF structure. The number of outputs K depends on the order of the noise-shaping, which will be discussed in the following section. For a boxcar-integration-based beamformer, since it is a sum-and-delay operation, no additional capacitors are required, as shown in Figure 2.9. The delay operations that would normally be performed in the loop filter are now moved to the beamformer, sharing the same capacitors with the beamformer. In other words, the beamformer now implements part of the functionality of the FIR loop filter. Therefore, using boxcar-integration-based beamformer in BENSSAR can save even more capacitors compared with the beamforming charge-sharing SAR.

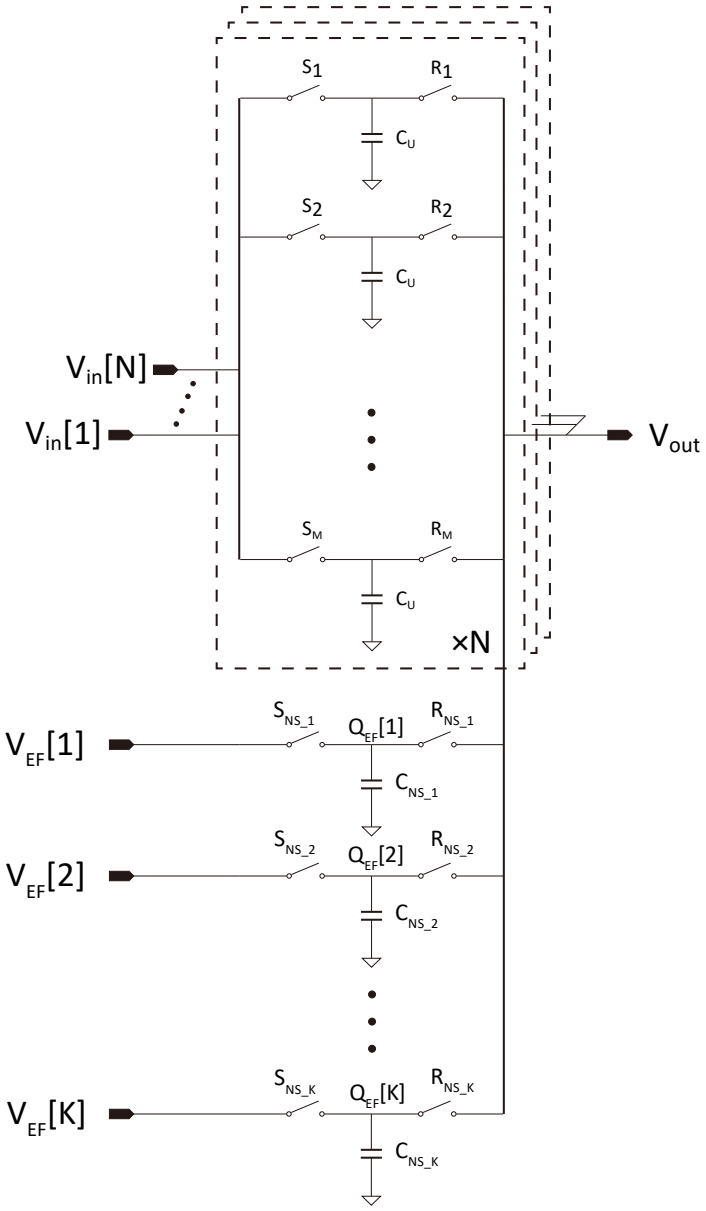


Fig 2.8 Schematic of the beamformer based on analog capacitor delay lines with noise-shaping function

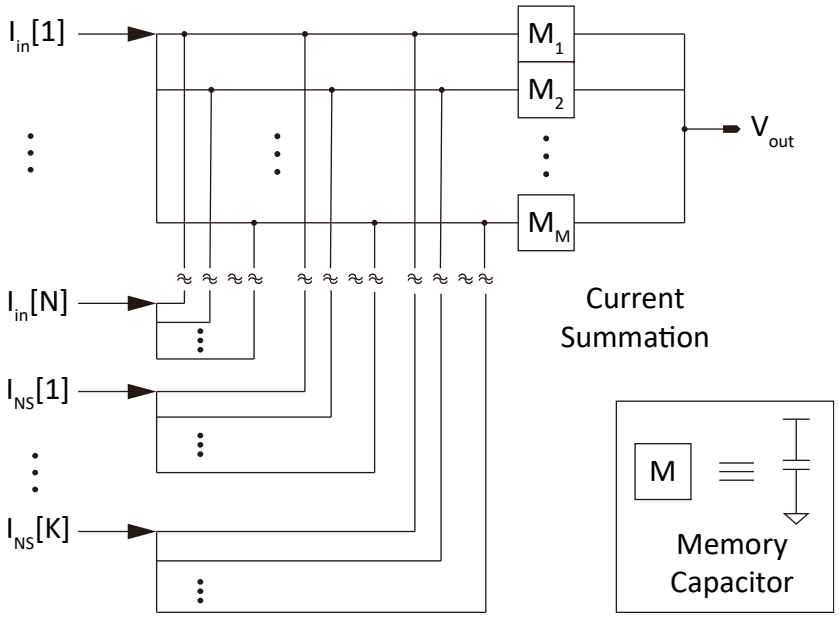


Fig 2.9 Schematic of the boxcar-integration-based beamformer with noise-shaping function

Therefore, both beamformers have their advantages and both can be implemented in BENNSAR. Practically, since our design is for the proof of concept, the analog capacitor delay lines beamformer is our final choice because of its simple circuit structure, but the analysis and simulation of a BENNSAR based on boxcar-integration-based beamformer will also be presented in the following section for the future design.

2.2.2 System architecture of BENSSAR

The system architecture of BENSSAR based on the discussed design choices is shown in Figure 2.10. Since BENSSAR, including the beamformer, the loop filter and the charge-sharing SAR, operates in the charge domain, all the signals inside BENSSAR are represented in the charge domain.

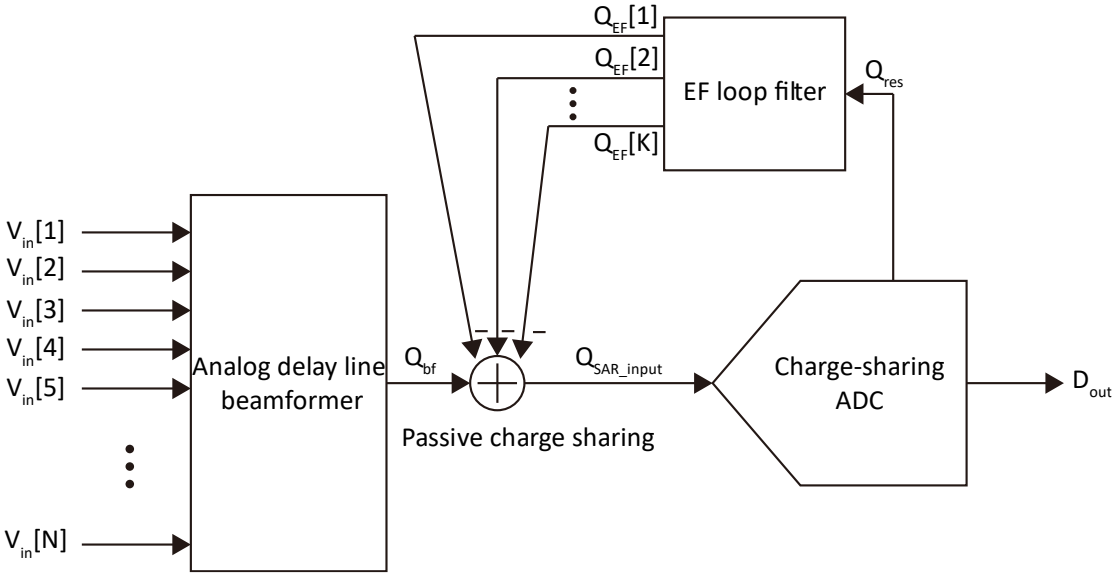


Fig 2.10 System architecture of BENSSAR

BENSSAR works as follows. The ultrasound signals from the AFE $V_{in}[1]-V_{in}[N]$ are sampled by the analog delay line beamformer and stored on the capacitors. According to the delay applied, the beamformer chooses a specific capacitor from each channel and connects them together to get output signal Q_{bf} . In the meanwhile, the capacitors with the filtered residual charges $Q_{EF}[1]-Q_{EF}[K]$ are connected to the output of the beamformer. All capacitors chosen from the beamformer and the EF loop filter share charge with each other, obtaining a total charge Q_{sar_input} which is the input signal of the charge-sharing SAR. After SAR conversion, we get the digital output D_{out} and also the residual charge Q_{res} . Q_{res} is sent into the EF loop filter to produce $Q_{EF}[1]-Q_{EF}[K]$. This process will repeat cycle by cycle.

2.2.3 System parameters

After determining the system architecture, some system parameters need to be defined.

2.2.3.1 Number of input channels

The number of channels per beamformer depends on the design specifications. In general, a smaller number leads to more ADCs for a given overall transducer-array size, which increases the power and area overhead of the whole ultrasound system. But it may provide more flexibility because more data is processed in digital domain. A larger number of input channels leads to a higher channel-count reduction in the analog domain but longer delay lines are required. Since the design specifications are similar to [14], 9 channels per beamformer are chosen.

2.2.3.2 Sampling frequency and OSR

The sampling frequency is mainly influenced by the two factors in BENSSAR.

(1) OSR. According to the previous research [17,28], most noise-shaping SARs have an OSR ranging from 4 to 10, especially those with input frequencies greater than 1MHz. This is due to the fact that SAR is slower compared with the Flash ADC commonly used in the conventional sigma-delta ADC.

(2) Delay resolution. The delay resolution mainly affects the ultrasound imaging quality. In order to keep the sidelobe level low enough, the sampling frequency should be 4 to 10 times the center frequency [21,24].

Both factors limit the sampling frequency to 20MHz-50MHz. Considering we are using a 180nm process, 30MHz is chosen, corresponding to an OSR of 6 and a delay resolution of 33ns, to achieve both sufficient performance and acceptable power and area overhead.

2.2.3.3 Number of the memory cells in the beamformer

The number of memory cells per channel depends on the field of view required by the ultrasound system. More memory cells provide greater maximum delay. Greater maximum delay can accommodate a larger steering angle which means larger field of view. For an ultrasound signal with a center frequency of 5MHz and a sampling frequency of 30MHz, 8 memory cells are chosen to allow pre-steering up to ±37° in both the azimuthal and elevation directions [14].

2.2.3.4 Transfer function of the EF loop filter

The transfer function of BENSSAR can be expressed as

$$D_{out}(z) = Q_{bf}(z) + E_s(z) - H_{EF}(z)\cdot E_{n\_LF}(z) + \underbrace{(1+H_{EF}(z))}_{NTF}\cdot(E_q(z) + E_{n\_comp}(z) + E_{settle}(z)) \quad (2.4)$$

which is similar to the formula (2.3). In formula (2.4), Q_{bf} is the output of the beamformer expressed in the charge domain and $E_s(z), E_{n\_LF}(z), E_q(z)$, $E_{n\_comp}(z)$ and $E_{settle}(z)$ are also charge-domain errors. $1+H_{EF}(z)$ is the noise transfer function (NTF).

As mentioned in the previous section, we aim for a band-pass design. A band-stop NTF needs conjugate zero pairs as graphically shown in Figure 2.11. Since our design only needs the notch at 5MHz, we assume the conjugate zero pairs are in the same position. The NTF is also expressed as

$$NTF = \left[(1+a_1z^{-1}+a_2z^{-2})\right]^{\frac{n}{2}} = \left[(1-z_1z^{-1})(1-z_2z^{-2})\right]^{\frac{n}{2}} \quad (2.5)$$

z_1 and z_2 is a conjugate zero pair expressed as

$$\begin{aligned} z_1 &= \cos\theta + i\sin\theta \\ z_2 &= \cos\theta - i\sin\theta \end{aligned} \quad (2.6)$$

The number n in formula (2.5) is the order of noise-shaping. Since two conjugate zeros form a notch in the band-stop NTF, n is typically an even number. θ is

$$\theta = \pi\cdot\frac{\omega_{notch}}{\frac{\omega_s}{2}} \quad (2.7)$$

Then, we take formula (2.6) and formula (2.7) into formula (2.5) and get

$$\begin{aligned} \Rightarrow NTF &= \left(1-2\cos(\pi\cdot\frac{\omega_{notch}}{\frac{\omega_s}{2}})z^{-1}+z^{-2}\right)^{\frac{n}{2}} \\ a_1 &= -2\cos(\pi\cdot\frac{\omega_{notch}}{\frac{\omega_s}{2}}) \\ a_2 &= 1 \end{aligned} \quad (2.8)$$

Since the input center frequency is 5MHz and the sampling frequency is 30MHz, the NTF is expressed as

$$\begin{aligned} &\Rightarrow NTF = \left(1 - z^{-1} + z^{-2}\right)^{\frac{n}{2}} \\ &a_1 = -1 \\ &a_2 = 1 \end{aligned} \tag{2.9}$$

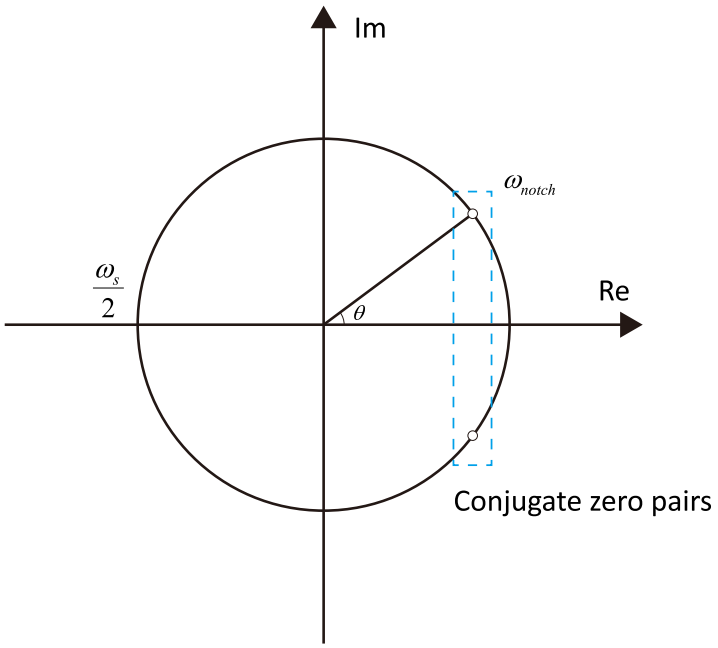


Fig 2.11 Graphical representation of complex zeros

As mentioned previously, the EF structure is sensitive to the PVT variation. This sensitivity is also affected by the order of noise-shaping. The higher the order of EF structure, the more sensitive it is to the PVT variation. A behavior model simulation will be presented below.

First, we have to model the variation. The NTF of the 2nd, 4th and 6th order noise-shaping are

$$\begin{aligned} &NTF_{2nd} = 1 + a_1 z^{-1} + a_2 z^{-2} = 1 - z^{-1} + z^{-2} \\ &NTF_{4th} = 1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} = 1 - 2z^{-1} + 3z^{-2} - 2z^{-3} + z^{-4} \\ &NTF_{6th} = 1 + c_1 z^{-1} + c_2 z^{-2} + c_3 z^{-3} + c_4 z^{-4} + c_5 z^{-5} + c_6 z^{-6} = 1 - 3z^{-1} + 6z^{-2} - 7z^{-3} + 6z^{-4} - 3z^{-5} + z^{-6} \end{aligned} \tag{2.10}$$

The magnitude of ideal NTF_{2nd}, H_{EF_2nd}, NTF_{4th}, H_{EF_4th}, NTF_{6th} and H_{EF_6th} are illustrated in Figure 2.12. The green rectangle in the figure indicates the bandwidth. It can be seen from the figure that the depth of notch increases with the order of NTF. It can also be noticed that as the order increases, H_{EF} in the bandwidth get closer to 1. This is because $NTF = 1 + H_{EF}$. When NTF is close to 0, the magnitude of H_{EF} is close 1.

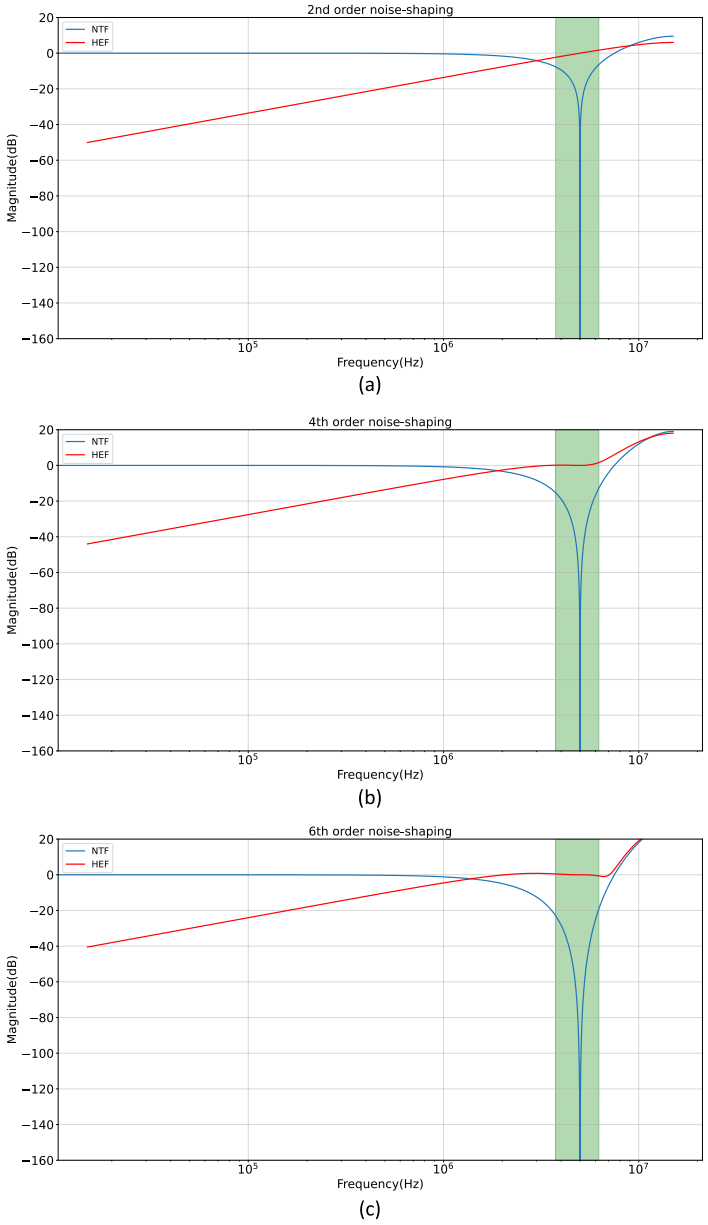


Fig 2.12 Plots of the ideal NTF and H_{EF} (a) 2nd order noise-shaping (b) 4th order noise-shaping (c) 6th order noise-shaping

Since $NTF = 1 + H_{EF}$, $a_1, a_1, b_1, \ldots b_4$ and $c_1, \ldots c_4$ are coefficients which should be implemented in the EF loop filter. Due to the circuit implementation which will be discussed in the next chapter, the coefficients can be divided into two categories: the absolute gains a_1, b_1, c_1 and the relative gains $\frac{a_2}{a_1}, \frac{b_2}{a_1} - \frac{b_4}{a_1}, \frac{c_2}{a_1} - \frac{c_6}{a_1}$. Equation (2.10) can be rewritten as

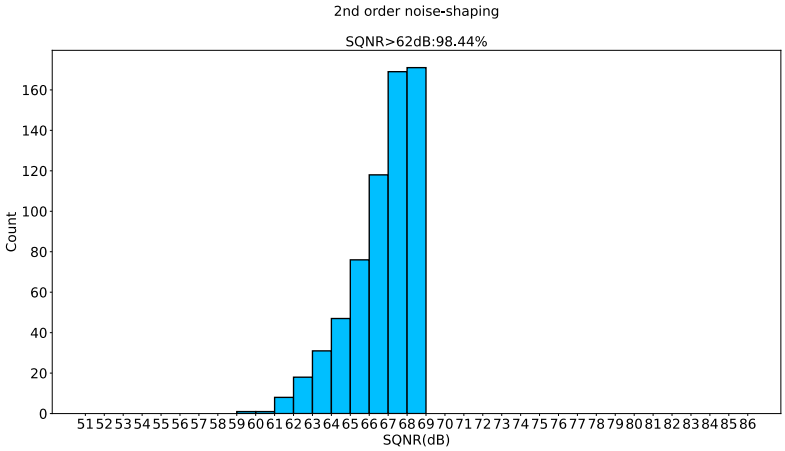
$$
\begin{aligned}
NTF_{2nd} &= 1 + a_1\left(z^{-1} + \frac{a_2}{a_1} z^{-2}\right) = 1 - z^{-1} + z^{-2} \\
NTF_{4th} &= 1 + b_1\left(z^{-1} + \frac{b_2}{b_1} z^{-2} + \frac{b_3}{b_1} z^{-3} + \frac{b_4}{b_1} z^{-4}\right) = 1 - 2z^{-1} + 3z^{-2} - 2z^{-3} + z^{-4} \\
NTF_{6th} &= 1 + c_1\left(z^{-1} + \frac{c_2}{c_1} z^{-2} + \frac{c_3}{c_1} z^{-3} + \frac{c_4}{c_1} z^{-4} + \frac{c_5}{c_1} z^{-5} + \frac{c_6}{c_1} z^{-6}\right) = 1 - 3z^{-1} + 6z^{-2} - 7z^{-3} + 6z^{-4} - 3z^{-5} + z^{-6}
\end{aligned}
\tag{2.11}
$$

In the real circuit implementation, which will be discussed in next chapter, the absolute gain is

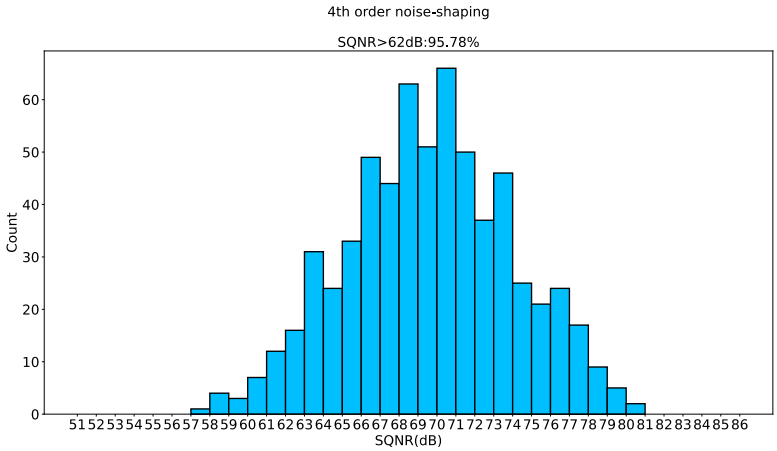
realized by active charge amplification and the relative gain is realized by passive charge sharing. Therefore, the relative gain can be more accurate than absolute gain. Here, the error of the absolute gain σ_{abs} and the relative gain σ_{rel} set in the simulation are

$$\begin{aligned} \sigma_{abs} &= 20\% \\ \sigma_{rel} &= 5\% \end{aligned} \tag{2.12}$$

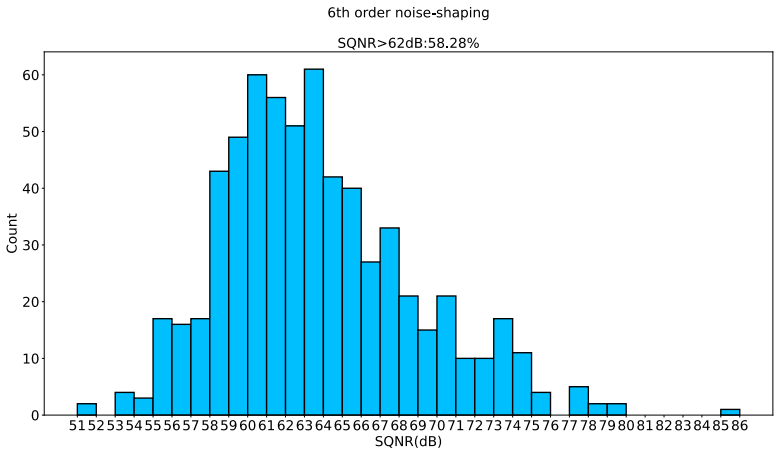
The simulations are based on an 8-bit SAR.



(a)



(b)



(c)

Fig 2.13 640 points Monte Carlo simulation of (a) 2nd order noise-shaping (b) 4th order noise-shaping (c) 6th order noise-shaping

640-point Monte Carlo simulations of the 2nd, 4th and 6th order noise-shaping are shown in Figure 2.13. Although higher order noise-shaping can achieve higher maximum SQNR, it can be clearly seen from Figure 2.13 that the variation of SQNR increases with the order of noise-shaping, because the NTF of higher order noise-shaping has more varying coefficients making it much harder to reach the maximum SQNR. The mean SQNR of the 6th order noise-shaping becomes even lower than that of the other two due to the large number of varying coefficients. Under the condition that our target SQNR is 62dB and 8-bit SAR is used, only 95.78% of the 4th order noise-shaping ADC and 58.28% of the 6th order noise-shaping ADC meet our target. In contrast, for 2nd order noise-shaping, 98.44% of the ADC meet our target. Therefore, we choose the 2nd order noise-shaping. Finally, the NTF is

$$\begin{aligned} NTF &= 1 - z^{-1} + z^{-2} \\ a_1 &= -1 \\ a_2 &= 1 \end{aligned} \tag{2.13}$$

and $H_{EF}(z)$ is

$$\begin{aligned} H_{EF}(z) &= -z^{-1} + z^{-2} \\ a_1 &= -1 \\ a_2 &= 1 \end{aligned} \tag{2.14}$$

2.2.3.5 Number of bits of the charge-sharing SAR

After determining the transfer function of the EF loop filter H_{EF}, we have to decide the number of bits of the charge-sharing SAR. A plot of the SQNR vs the number of bits is shown in Figure 2.14. From the figure, 7 bits are required at least. However, this simulation is based on the ideal transfer function. Variation of the coefficients in the transfer function has to be taken into account.

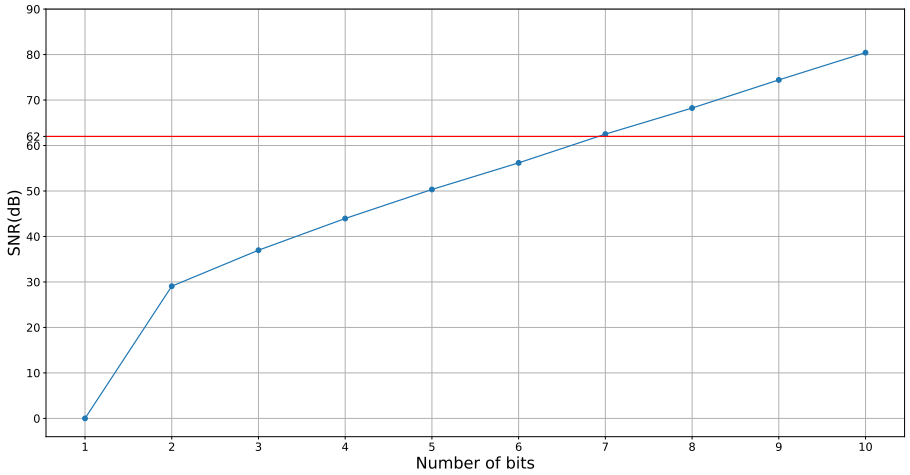
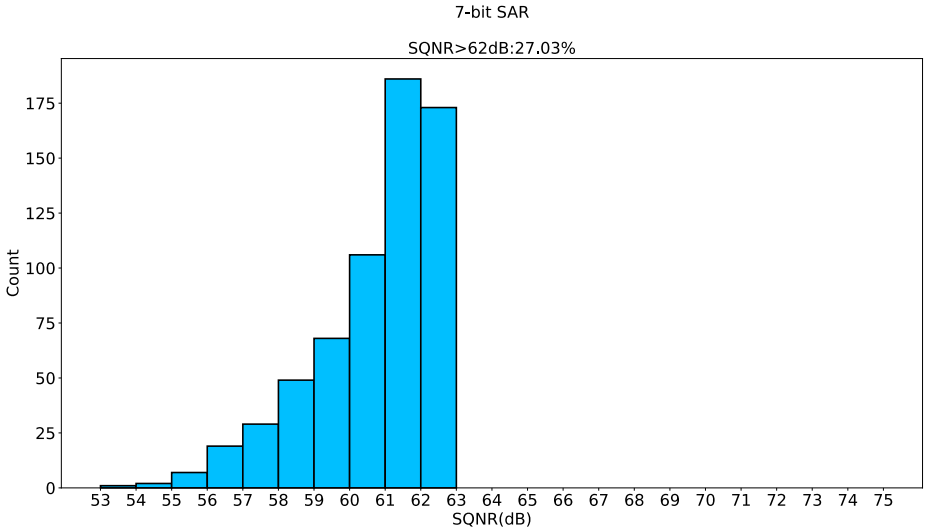
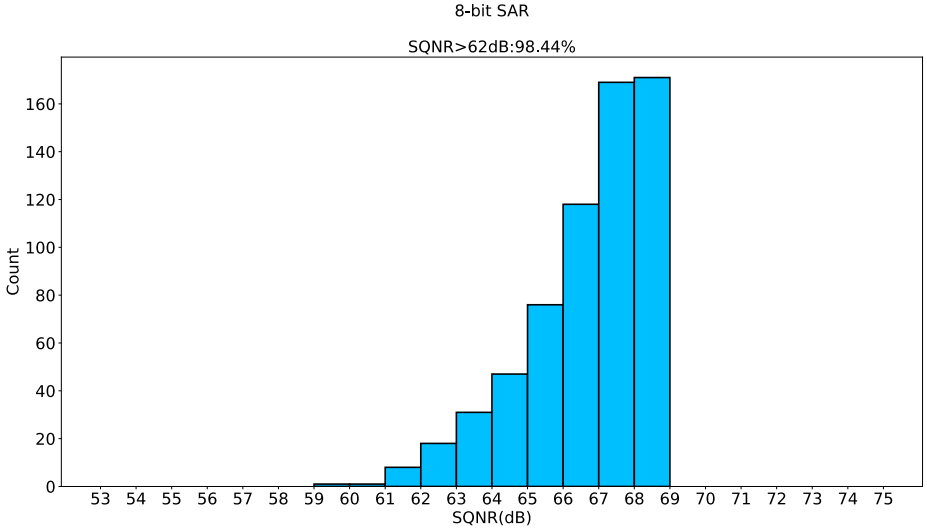


Fig 2.14 SQNR vs Number of bits

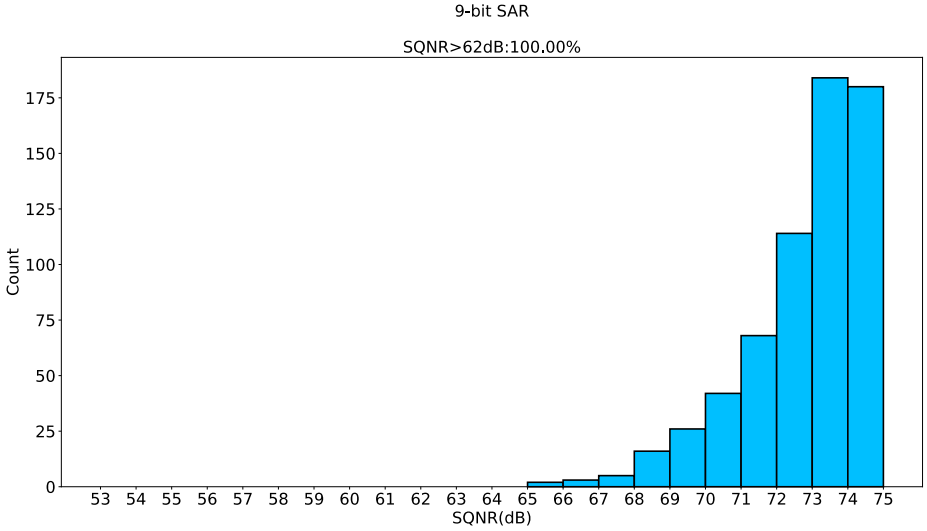
Therefore, we perform 640-point Monte Carlo simulations of the 7-bit SAR, the 8-bit SAR and the 9-bit SAR as shown in Figure 2.15, which have the same error settings as in Figure 2.12. Figure 2.15 indicates that the 7-bit SAR is not sufficient because only 27.03% of the total points achieve an SQNR greater than 62dB. It is acceptable that 98.44% of the 8-bit SARs achieve an SQNR greater than 62dB. Although 9-bit SAR has a slightly higher yield, it is not worth adding an extra bit. Finally, we choose an 8-bit charge-sharing SAR.



(a)



(b)



(c)

Fig 2.15 640 points Monte Carlo simulation of (a) 7-bit SAR (b) 8-bit SAR (c) 9-bit SAR

2.2.4 Simulation results

2.2.4.1 Output spectrum

First, the output spectrum is simulated without adding nonideal factors as shown in Figure 2.16. A single tone of 5MHz is applied at the input. From the output spectrum, we can clearly see the 5MHz output signal and the shaped quantization noise. Ideally, BENSSAR can achieve an SQNR of 68.2dB and an ENOB of 11.04 bits.

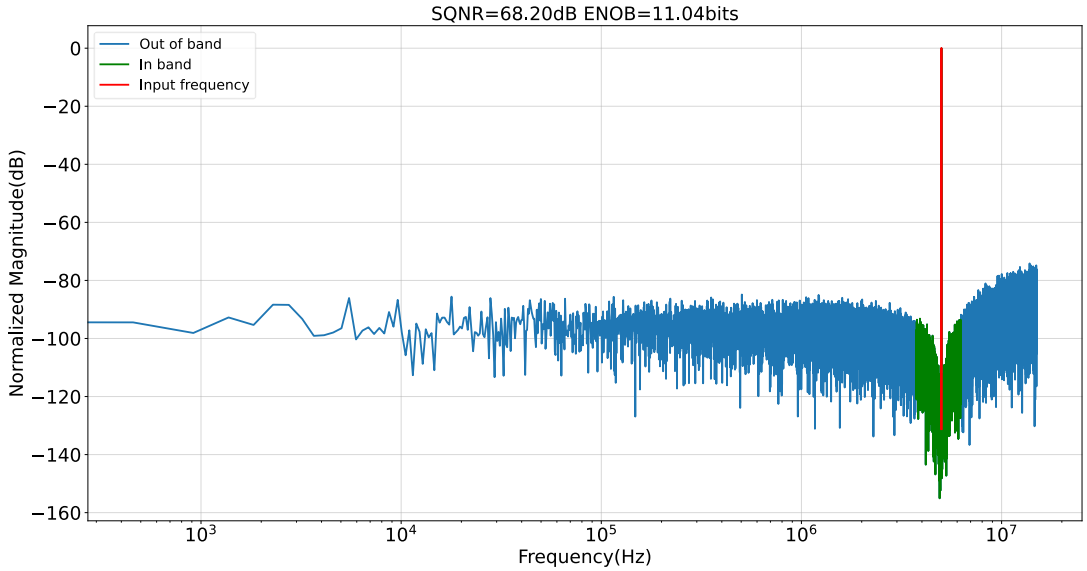


Fig 2.16 The ideal output spectrum

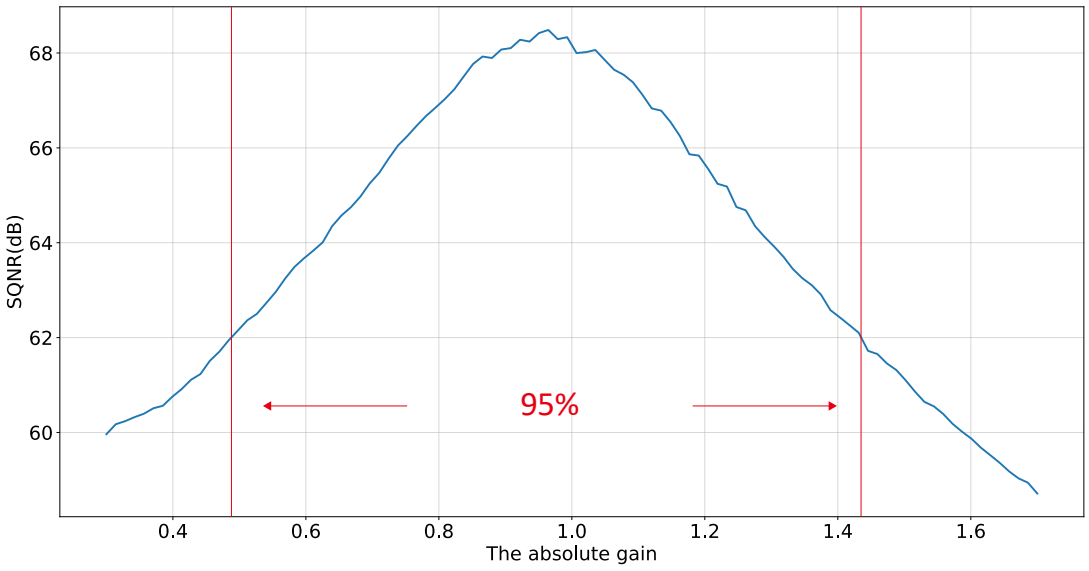


Fig 2.17 The absolute gain vs SNR

2.2.4.2 Nonideal EF loop filter

Since this topic is discussed in previous section, we only briefly review some important conclusions and present more simulation results. To know how the absolute gain alone affects the SQNR, a sweep of the absolute gain is simulated as shown in Figure 2.17. 95% variation of the absolute gain is allowed if only the absolute gain varies.

2.2.4.3 Noise in BENSSAR

Based on equation (2.4) in Section 2.2.3.4, the noise in BENSSAR can be divided into 3 categories:

(1) Unshaped noise including the sampling noise $E_s(z)$

(2) Noise shaped by $H_{EF}(z)$ including the noise in the EF loop filter $E_{n\_LF}(z)$.

(3) Noise shaped by $1+H_{EF}(z)$ including the quantization noise $E_q(z)$ and the comparator noise $E_{n\_comp}(z)$.

We will first analyze them separately and then take all of them into account.

① Unshaped noise

The sampling noise $E_s(z)$ is not shaped. If only $E_s(z)$ is considered, the maximum sampling noise in voltage domain $V_{n,\max}$ is

$$V_{n,\max}=V_{in}\cdot\frac{\sqrt{2}}{2}\cdot 10^{-\frac{SNR}{20}}\cdot\sqrt{OSR}\approx 550\mu V \tag{2.15}$$

where V_{in} is the maximum differential input amplitude which is 0.4V and SNR is 62dB. The sampling noise in our design should be less than half of $V_{n,\max}$ to avoid significant SNR degradation. Since BENSSAR uses a charge-sharing SAR, the capacitors in the beamformer should be sufficiently large to avoid significant signal attenuation during the SAR conversion. Therefore, we size the total capacitor of the beamformer to be 602fF obtaining a sampling noise of $83\mu V$, which is same as the design in [14].

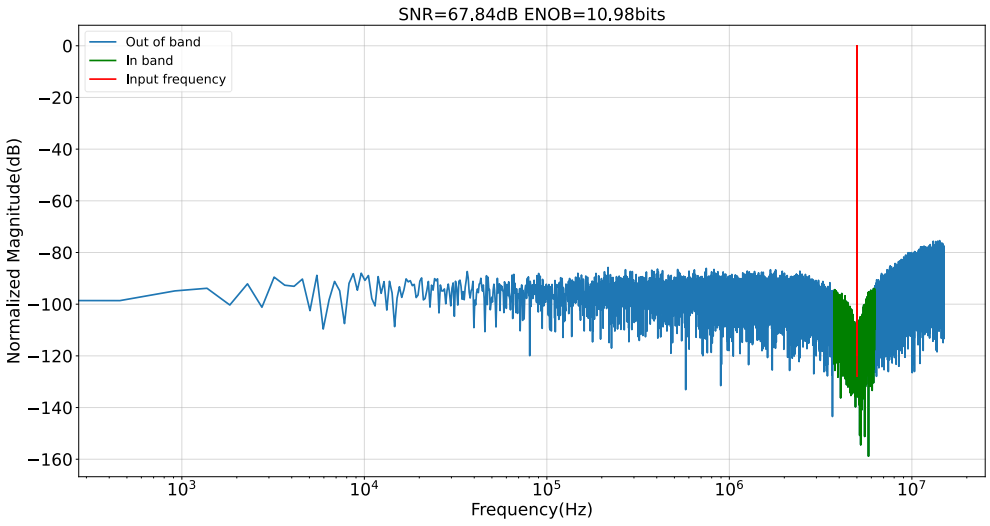


Fig 2.18 Output spectrum with only sampling noise

Then, the effect of the sampling noise is simulated. First, the output spectrum is obtained using the ideal EF loop filter as shown in Figure 2.18. Compared with the noise-free case, the SNR is reduced by 0.36dB.

The simulation results show that the sampling noise has little effect on SNR because the sampling noise is not the limiting factor for the chosen capacitor size.

② Noise shaped by $H_{EF}(z)$

The noise in the EF loop filter $E_{n\_LF}(z)$ is shaped by $H_{EF}(z)$. Unfortunately, the in-band magnitude of $H_{EF}(z)$ is close to 1 as shown in Figure 2.13 so $E_{n\_LF}(z)$ is not suppressed. Therefore, $E_{n\_LF}(z)$ affects the SNR significantly and should be as low as possible. However, reducing $E_{n\_LF}(z)$ means increasing the power consumption of the EF loop filter so there is a trade-off between SNR and power consumption. We choose $V_{n\_LF} = 300\mu V$ [3] trying to achieve a good trade-off.

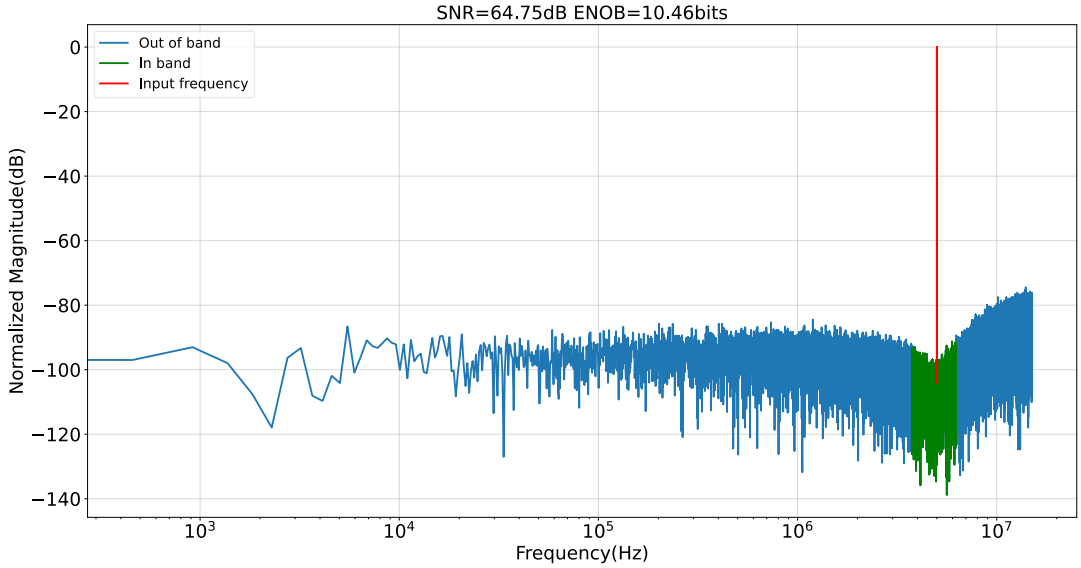


Fig 2.19 Output spectrum with only noise in the EF loop filter

The output spectrum using the ideal EF loop filter is shown in Figure 2.19. We can clearly see the noise fills in the notch, thus reducing SNR by 3.45dB.

③ Noise shaped by $1+H_{EF}(z)$

The quantization noise $E_q(z)$ and the comparator noise $E_{n\_comp}(z)$ are shaped by $1+H_{EF}(z)$. Fortunately, these noises are shaped out of band, thus allowing us to choose a large value. The quantization noise is determined by the resolution of the charge-sharing SAR. This can be calculated as

[3] Strictly speaking, this noise should be analyzed in charge domain but since the comparator noise is in voltage domain, we represent this noise in voltage domain for convenience. In the next chapter, this noise will be converted into a charge domain representation.

$$V_q = Attn \cdot V_{LSB} \cdot \frac{1}{\sqrt{12}} \approx 338\mu V \tag{2.16}$$

where $Attn$ is the attenuation factor due to charge sharing.

The comparator noise should be smaller than the quantization noise to avoid significant SNR degradation. Therefore, we choose the comparator noise $V_{n\_comp} = 280\mu V$ to achieve a good trade-off between SNR and power consumption of the comparator.

The output spectrum using the ideal EF loop filter is shown in Figure 2.20. The notch is not filled by the noise, which indicates that the comparator noise is shaped out of band. Since we choose a relatively large comparator noise, the SNR is still reduced by 1.57dB. Compared with the noise in the EF loop filter, the comparator noise contributes much less in-band noise.

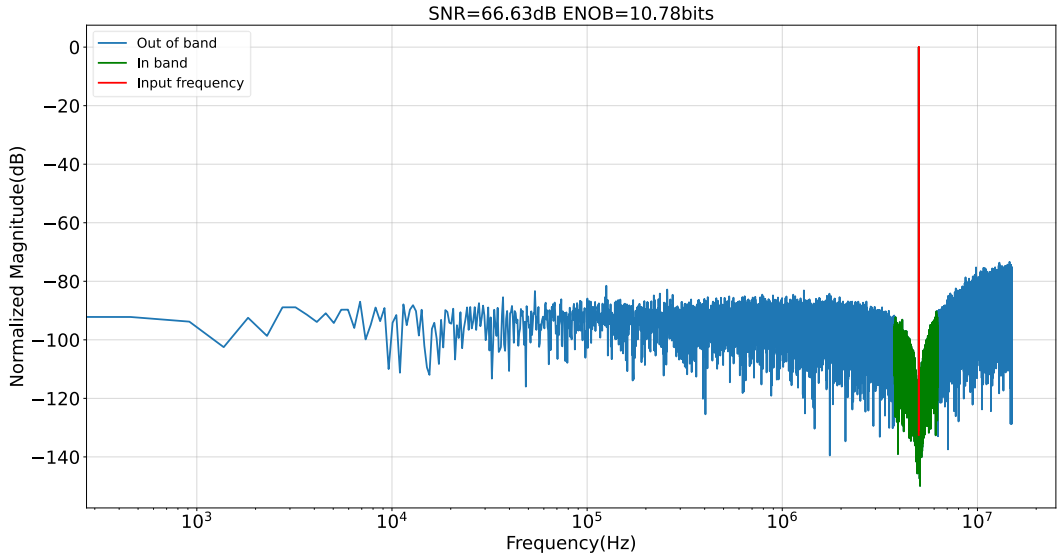


Fig 2.20 Output spectrum with only noise in the comparator

④ All types of noise combined

After analyzing each type of noise separately, all types of noise are combined here. The sampling noise V_{n_s}, the noise in the EF loop filter V_{n_LF} and the comparator noise V_{n_comp} take values as follows:

$$\begin{aligned} V_{n\_s} &= 83\mu V \\ V_{n\_LF} &= 300\mu V \\ V_{n\_comp} &= 280\mu V \end{aligned} \tag{2.17}$$

The output spectrum using the ideal EF loop filter is shown Figure 2.21. The notch is filled by the noise in the EF loop filter which is the major contributor to the total noise. SNR is reduced by 4.66dB but it is still above 62dB.

640 points Monte Carlo simulation in Figure 2.22 shows that 77.03% of points can achieve an SNR greater than 62dB. Compared with the noise-free case, the result decreases by 21.41%. This is

mainly influenced by the combination of the noise in the EF loop filter and the comparator noise. The points below 62dB are mainly in the range from 59dB to 62dB, which is still acceptable for the ultrasound AFE in [14].

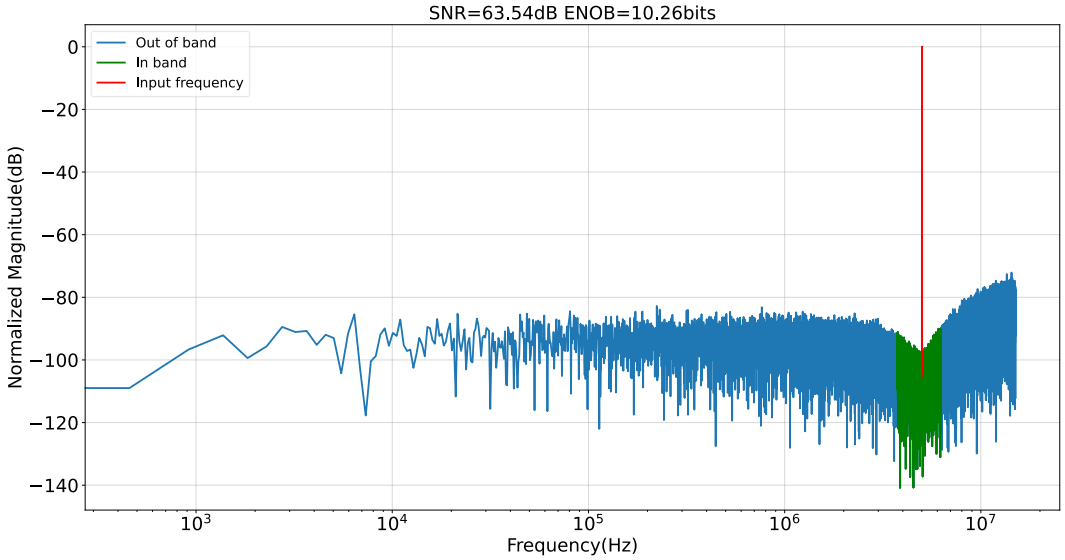


Fig 2.21 Output spectrum with only noise in the EF loop filter

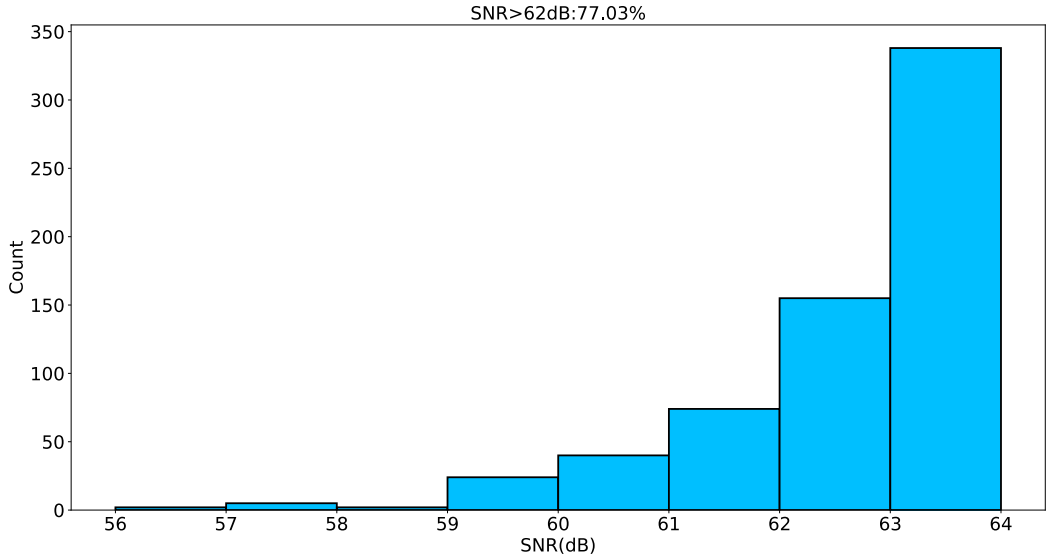


Fig 2.22 640 points Monte Carlo simulation with the nonideal EF loop filter

2.2.4.4 Mismatch of the CDAC in BENSSAR

Since the harmonic distortion is less important in ultrasound applications, and hence matching requirements can be relaxed. This work uses the same unit capacitor size as [14] achieving 9-bit linearity.

2.3 BENSSAR based on boxcar-integrator-based beamformer: an alternative approach

As mentioned before, a boxcar-integrator-based beamformer is another option for BENSSAR. Although the circuit is more complex and the power consumption may be higher, this solution requires fewer capacitors.

Since this option has been investigated early in the project, some settings are different from the design choices discussed in the previous sub-section and can be further optimized. Nevertheless, we report the results here as a starting point for a future design. We use a 7-bit charge-redistribution SAR and a buffer is placed between the beamformer and the charge-redistribution SAR. We use ideal components to build an ideal BENSSAR in Cadence and the simulation result is shown in Figure 2.23. From the figure, we can clearly see the notch and this ideal BENSSAR achieves an SQNR of 61.76dB and an ENOB of 9.96bits. This result indicates that ideally both beamformer types can work in BENSSAR.

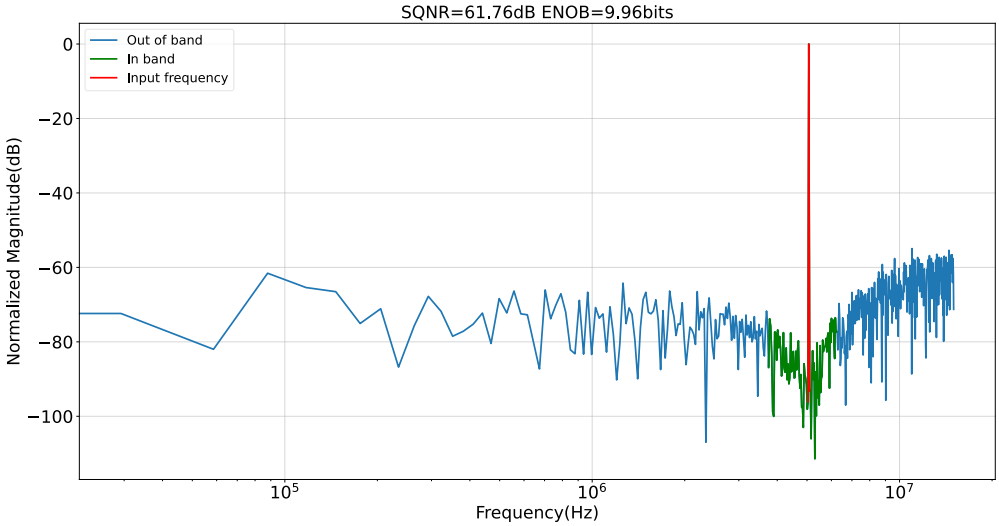


Fig 2.23 Output spectrum of BENSSAR based on boxcar-integrator-based beamformer

2.4 Conclusion

In this chapter, the system level design has been discussed. First, the individual blocks have been analyzed separately. Then, the whole architecture has been proposed based on the previous analysis. The system parameters have been determined. Behavioral simulations have been performed for verification. Finally, an alternative architecture has been briefly introduced. In the next chapter, the details about the circuit design will be discussed.

Chapter 3 Circuit implementation

In this Chapter, the circuit implementation of BENSSAR will be discussed. First, the key topic will be described in detail: the EF loop filter. Then, an improved architecture of the EF loop filter will be presented. Finally, the key circuit blocks of the charge-sharing SAR ADC will be discussed: the CDAC and the comparator.

3.1 The EF loop filter

In this section, the design of the EF loop filter will be described. First, we divide the EF loop filter into two blocks: the charge amplifier and the passive charge sharing circuit, and analyze the EF loop filter at the system level. Then, we dive into the transistor design of the charge amplifier and topics such as speed, error sources and noise will be covered there. Finally, simulation results will be presented.

3.1.1 System-level design of the EF loop filter

The EF loop filter in a conventional noise-shaping SAR is typically based on passive charge sharing. However, if only passive charge sharing is used, the gain is less than one. Therefore, it is not possible to realize aggressive noise shaping, and a high SNR improvement cannot be obtained. In addition, the noise in the EF loop filter is not suppressed by the passive charge sharing, which leads to a stringent requirement on noise. Therefore, many designs such as [27] and [29] add an active amplifier before the passive charge sharing node, in an attempt to both provide sufficient gain and suppress noise. However, since these designs are all based on the charge-redistribution SAR, their active amplifiers all operate in the voltage domain. It is not a good idea to use such a voltage domain amplifier in the charge-sharing SAR, because the residual voltage is attenuated by the charge sharing process during the SAR conversion. We have to add another gain factor in the EF loop filter to compensate for this attenuation, which makes the EF loop filter more susceptible to PVT variations.

Processing the residual signal in the charge domain can avoid such compensation because the charge is not attenuated. Therefore, we decide to design a charge amplifier which directly amplifies the residual charges on C_{total}, where C_{total} refers to the capacitors involved in the SAR conversion including the CDAC, the beamformer capacitors C_{bf}, the noise-shaping capacitors and the parasitic capacitors C_p. Based on the analysis above, the EF loop filter in our design can be divided into two parts: the charge amplifier and the passive charge sharing circuit, as shown in Figure 3.1.

The charge amplifier amplifies the residual charges Q_{res} on C_{total} and stores its output Q_{CA} at the passive charge sharing circuit. Q_{CA} is the total charge required for noise shaping. According to

the expression of $H_{EF}(z)$ in formula (2.14), the amount of charge required for z^{-1} and z^{-2} are:

$$\begin{aligned} z^{-1}: \ & Q_{a1} = -Q_q = Q_{res} \\ z^{-2}: \ & Q_{a2} = Q_q = -Q_{res} \end{aligned} \tag{3.1}$$

It is worth noting that due to practical circuit implementation, Q_{res} and the quantization noise Q_q are equal in absolute value but opposite in sign:

$$\begin{aligned} & Q_{res} = Q_{bf} - D_{out} \\ & Q_q = D_{out} - Q_{bf} \\ & Q_{res} = -Q_q \end{aligned} \tag{3.2}$$

Therefore, Q_{CA} can be calculated as

$$Q_{CA} = |Q_{a1}| + |Q_{a2}| = 2Q_{res} \tag{3.3}$$

That is, the charge amplifier should have a gain of 2.

The passive charge sharing circuit consists of memory capacitors, which hold the residual charge for a certain time. Since the EF loop filter has a second-order transfer function, a delay of one clock cycle z^{-1} and a delay of two clock cycles z^{-2} are required as mentioned previously in formula (2.14). For a delay of N clock cycles, at least N+1 memory capacitors are required because there is always one memory capacitor involved in the SAR conversion. Therefore, as shown in Figure 3.1, at least five capacitors are required in total: two capacitors for z^{-1} and three capacitors for z^{-2}. It is also shown in the timing diagram that capacitors $C_{NS\_a1\_1}$ and $C_{NS\_a1\_2}$ are connected to $CDAC + C_{bf} + C_p$ after holding the residual charges for one clock cycle and capacitors $C_{NS\_a2\_1}$, $C_{NS\_a2\_2}$ and $C_{NS\_a2\_3}$ are connected to the $CDAC + C_{bf} + C_p$ after holding the residual charges for two clock cycles. Since $|Q_{a1}| = |Q_{a2}|$, all capacitors in the passive charge sharing circuit have equal capacitance. However, Q_{a1} and Q_{a2} have opposite signs. To implement $Q_{a2} = -Q_{res}$, the capacitors $C_{NS\_a2\_1}$, $C_{NS\_a2\_2}$ and $C_{NS\_a2\_3}$ are reversely connected to $CDAC + C_{bf} + C_p$ as shown in Figure 3.1.

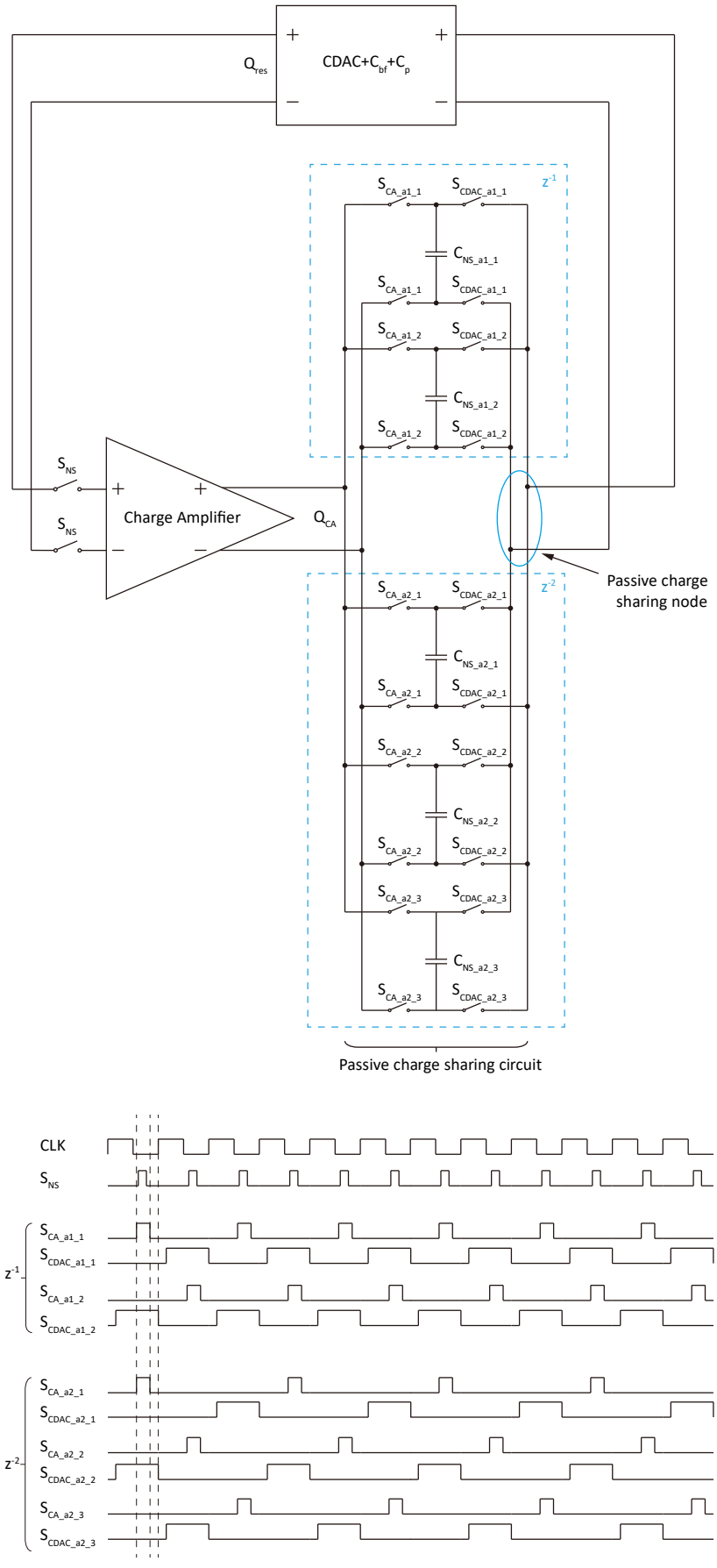


Fig 3.1 Block diagram and timing diagram of the EF loop filter

3.1.2 Transistor-level design of the charge amplifier

3.1.2.1 Circuit architecture

The conventional way to move charge is based on the voltage-input op-amp. The voltage-input op-amp extracts the charge by forcing the voltage across a capacitor to be zero and directs this charge to another capacitor. However, this method can only achieve a gain of less than one. To amplify charge, an additional circuit which provide some form of charge gain is required. The current mirror is the simplest circuit that provide this function. Since current mirror operates in current domain, a current-input amplifier is better than the voltage-input op-amp.

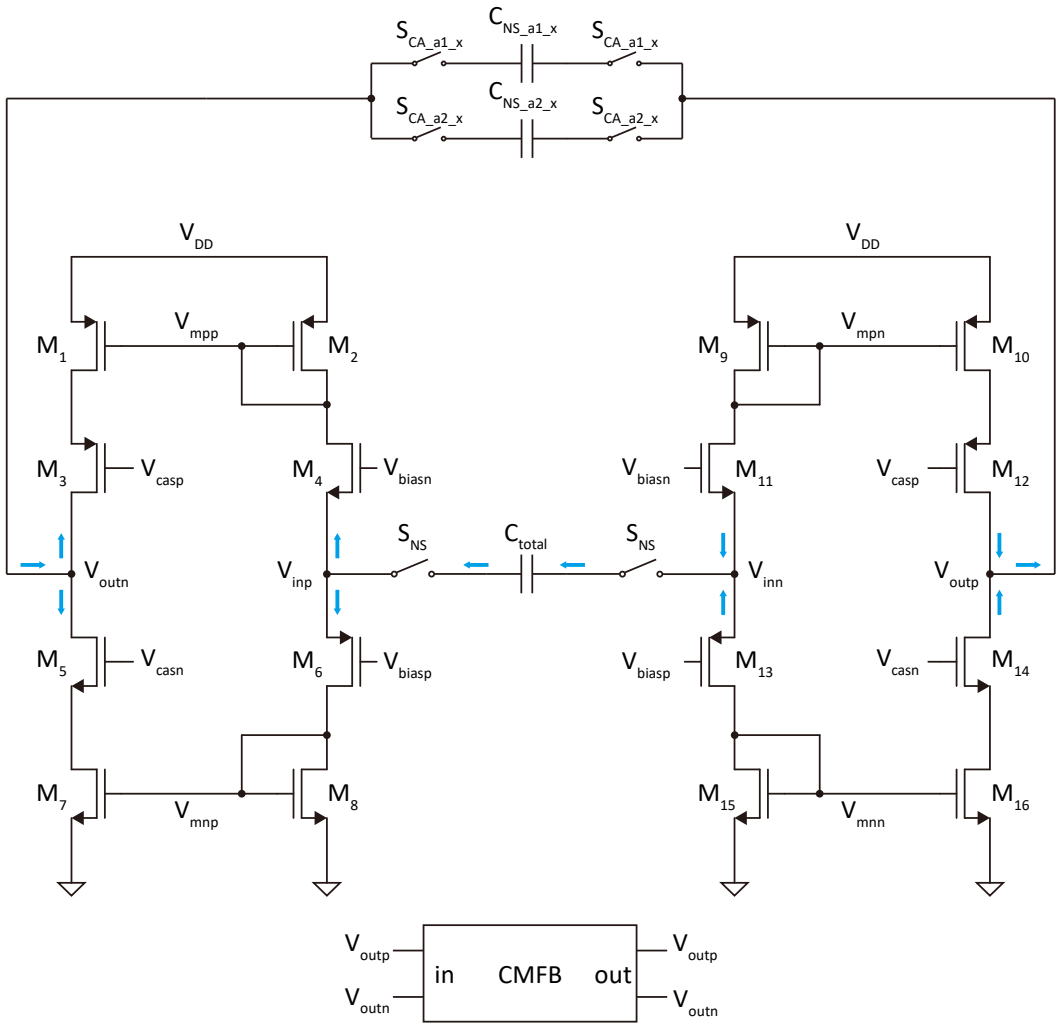


Fig 3.2 The schematic of the charge amplifier

Therefore, we design the charge amplifier shown in Figure 3.2. The input transistors M_4, M_6, M_{11}, M_{13} set V_{inp} and V_{inn} to a fixed voltage. If offset is not considered, $V_{inp}-V_{inn}$ should be zero. When switch S_{NS} is closed, the input transistors force the voltage across the capacitor C_{total} to be zero and extract the charge out. These charge flows into M_2, M_8, M_9, M_{15} which are the

input transistors of the current mirrors. M_1, M_7, M_{10}, M_{16} amplify the current in M_2, M_8, M_9, M_{15} respectively. Since our charge amplifier should have a gain of 2, the total width of M_1, M_7, M_{10}, M_{16} should be twice that of M_2, M_8, M_9, M_{15} respectively. Then, the amplified charge flows into the memory capacitors $C_{NS\_a1\_x}$, $C_{NS\_a2\_x}$ waiting for passive charge sharing with the input signal. Since the output resistance should be as large as possible to reduce the charge leakage on $C_{NS\_a1\_x}$ and $C_{NS\_a2\_x}$, cascode transistors M_3, M_5, M_{11}, M_{13} are added to the circuit.

This type of circuit is also known as the current conveyer [30]. It is usually used in the high speed continuous-time system, but here we use it in a switched-capacitor circuit.

The bias voltage $V_{biasp}, V_{biasn}, V_{casp}, V_{casn}$ are generated by the bias circuit as shown in Figure 3.2. An ideal CMFB circuit is used due to limited time and will be replaced with the real CMFB circuit in future design.

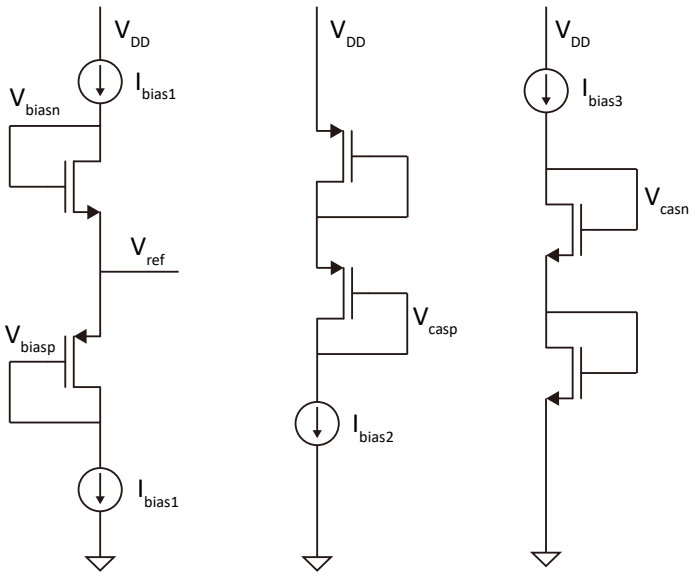


Fig 3.3 The bias circuit of the charge amplifier

3.1.2.2 Design consideration

After introducing the working principle of the charge amplifier, we will discuss some topics related to errors and noise. These topics will help us to determine the circuit parameters such as the size of the transistors and the bias current.

① Settling error

Since the residual voltage on C_{total} is less than 620μV, we can use small signal modelling to analyze the settling behavior of the charge amplifier as shown in Figure 3.4.

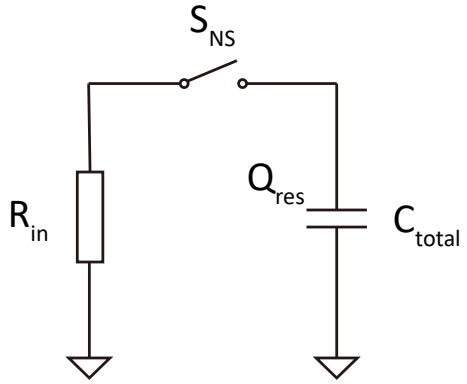


Fig 3.4 the small signal model for analyzing the settling behavior of the charge amplifier

It is just a simple RC circuit and the settling error is

$$Error = e^{-\frac{T_{CA}}{\tau_{CA}}} \tag{3.4}$$

T_{CA} is the time of charge amplification and the time constant τ_{CA} can expressed as

$$\tau_{CA} = R_{in}C_{total} \tag{3.5}$$

Let

$$T_{CA} = \alpha\tau_{CA} \tag{3.6}$$

The settling error can be rewritten as

$$e^{-\alpha} \tag{3.7}$$

α determines the settling accuracy of the charge amplifier.

In our design, we allocate 11ns for the charge amplification. Since the settling error belongs to the absolute gain error which has 20% tolerance as mentioned in Chapter 2, we choose

$$\begin{aligned} &\alpha=3 \\ &T_{CA} = 3\tau_{CA} = 11ns \end{aligned} \tag{3.8}$$

Then the time constant should be

$$\tau_{CA} \approx 3.67ns \tag{3.9}$$

The settling error is

$$Error = e^{-3} \approx 5\% < 20\% \tag{3.10}$$

Since there are other error sources, we choose 5% error here leaving sufficient margin.

Based on the settling requirement, some circuit parameters can be derived. R_{in} can be calculated as

$$R_{in} = \frac{1}{g_{m,M_4} + g_{m,M_6}} + \frac{1}{g_{m,M_{11}} + g_{m,M_{13}}} \tag{3.11}$$

Set $g_{m,in} = g_{m,M_4} = g_{m,M_6} = g_{m,M_{11}} = g_{m,M_{13}}$ and R_{in} can be rewritten as

$$R_{in} = \frac{1}{g_{m,in}} \tag{3.12}$$

The time constant can be calculated as

$$\tau_{CA} = \frac{C_{total}}{g_{m,in}} \tag{3.13}$$

Since $C_{total} \approx 1500\,fF$, the transconductance of each transistor should be

$$g_{m,in} = \frac{C_{total}}{\tau_{CA}} \approx 409\mu S \tag{3.14}$$

$\frac{g_m}{I_d} = 25$ is chosen to achieve both sufficient speed and good power efficiency. The bias current is

$$I_d = 16.36\mu A \tag{3.15}$$

② Current copying error of the current mirror

To improve the accuracy of the current mirror, the length of the transistors of the current mirror should be as large as possible.

③ Settling error of the current mirror

Settling also happens inside the current mirror and the RC small signal model can also be used. The time constant at node V_{mpp} [4] is

$$\tau_{mp} = \frac{C_{p,V_{mpp}}}{g_{m,M_2}} \approx \frac{C_{g,M_1} + C_{g,M_2}}{g_{m,M_2}} \tag{3.16}$$

$C_{p,V_{mpp}}$ is the total parasitic capacitance at node V_{mpp}. Since the gate capacitance of M_1 and M_2 is much larger than other parasitic capacitances, $C_{p,V_{mpp}}$ can be approximated by $C_{g,M_1} + C_{g,M_2}$. Similarly, the time constant at node V_{mnp} can be expressed as

$$\tau_{mn} = \frac{C_{p,V_{mnp}}}{g_{m,M_8}} \approx \frac{C_{g,M_7} + C_{g,M_8}}{g_{m,M_8}} \tag{3.17}$$

Since the characteristic frequency of the transistor is

$$f_T = \frac{g_m}{2\pi C_g} \propto \frac{1}{L^2} \tag{3.18}$$

τ_{mp} and τ_{mn} can be written as

$$\begin{aligned} \tau_{mp} &= \frac{1}{2\pi f_{T,M_1}} + \frac{1}{2\pi f_{T,M_2}} \propto L^2 \\ \tau_{mn} &= \frac{1}{2\pi f_{T,M_7}} + \frac{1}{2\pi f_{T,M_8}} \propto L^2 \end{aligned} \tag{3.19}$$

L is the channel length of the transistors of the current mirror. Since PMOS is slower than NMOS, we will focus on τ_{mp}.

Figure 3.5 is an example of insufficient settling of the current mirror. After charge amplification, node V_{mpp} stores some charge, which leads to charge loss.

[4] Since the circuit is fully symmetrical, only half of the circuit will be analyzed.

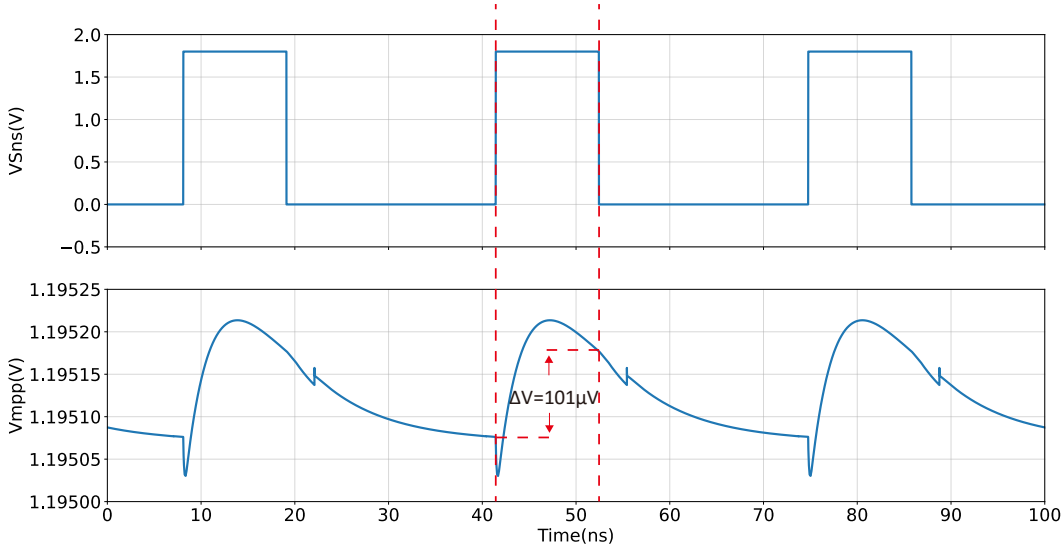


Fig 3.5 The settling behavior at node V_{mpp}

The charge loss at node V_{mpp} can be calculated as

$$Q_{error,V_{mpp}} = \Delta V \cdot C_{p,V_{mmp}} \approx 0.07\,fC \tag{3.20}$$

This corresponds to the absolute gain error

$$E_{absgain} = \frac{Q_{error,V_{mpp}}}{2Q_{res}} \approx 7.5\% \tag{3.21}$$

This absolute gain error is relatively large. To reduce the absolute gain error, we have to reduce τ_{mp}. According to formula (3.19), reducing τ_{mp} means reducing the length of the transistors. However, reducing L will increase the current copying error of the current mirror, so a trade-off must be made. Figure 3.6 illustrates how L influences the errors in the current mirror. $L = 600nm$ is chosen to achieve a total error of the current mirror of less than 2%.

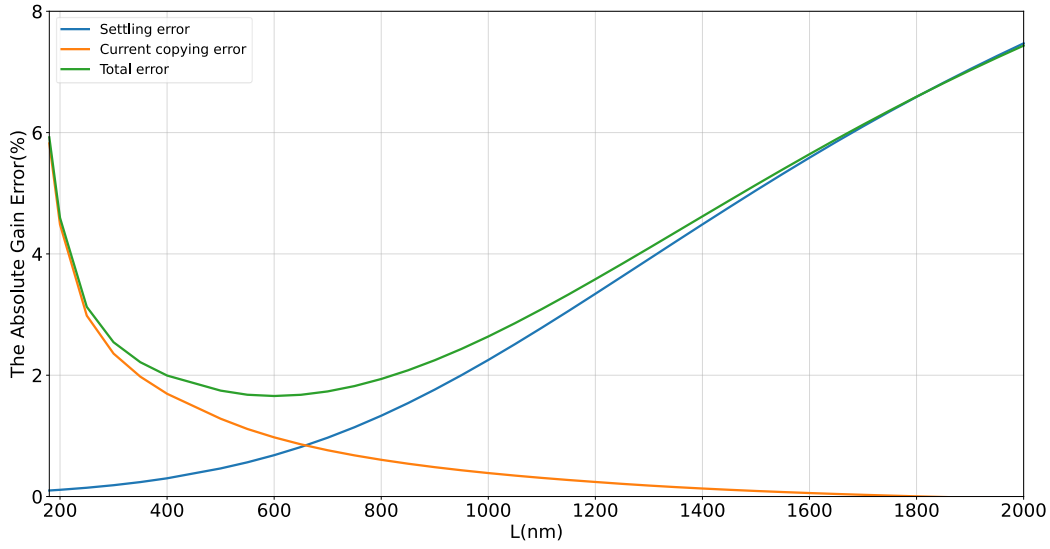


Fig 3.6 Errors in the current mirror vs L

④ Charge leakage

Finite output resistance leads to charge leakage, so the output resistance should be as large as possible.

⑤ Parasitic capacitors at the output

Parasitic capacitors at output nodes V_{outp} and V_{outn} share charges with $C_{NS\_a1\_x}$ and $C_{NS\_a2\_x}$, causing charge loss. Therefore, the cascode transistors and switch $S_{CA\_a1\_x}, S_{CA\_a2\_x}$ should be sized small.

⑥ Noise

Unlike the conventional voltage amplifier which always converges to a steady state, the charge amplifier works like an integrator which continuously accumulates charges. During the charge amplification process, both signal charge and noise charge continuously accumulate at the output. Therefore, there is no steady state and the noise is non-stationary. We will use the basic theories and methods provided by [31] to analyze the non-stationary noise in our charge amplifier.

First, let us consider a simple RC model which models the integrator as shown in Figure 3.7.
I_s and I_n are the signal current and the noise current respectively.

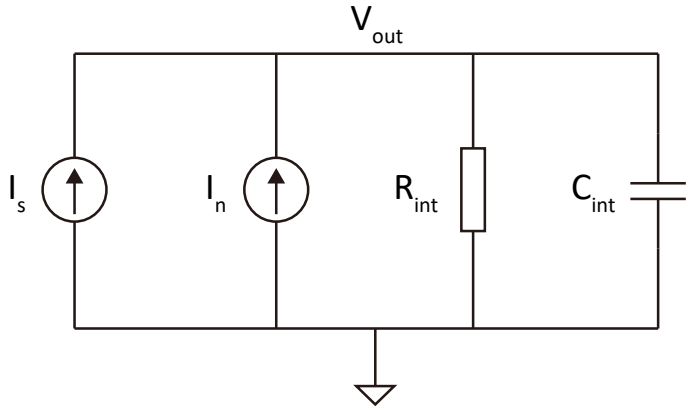


Fig 3.7 a simple RC model which models the integrator [31]

The rms noise at the output is basically a random walk noise [31] and can be expressed as

$$V_{n,out}{}^2 = \frac{1}{2} \cdot S_{I_n}(0) \cdot \tau_{\text{int}} \cdot \frac{1}{C_{\text{int}}{}^2} \cdot (1 - e^{-\frac{2T_{\text{int}}}{\tau_{\text{int}}}}) \quad [31] \tag{3.22}$$

S_{I_n} is the double-sided power spectrum density of the current noise and the time constant of the integrator is $\tau_{\text{int}} = R_{\text{int}} C_{\text{int}}$. T_{int} is the time of integration. Then, the charge domain noise can be expressed as

$$Q_{n,out}{}^2 = \frac{1}{2} \cdot S_{I_n}(0) \cdot \tau_{\text{int}} \cdot (1 - e^{-\frac{2T_{\text{int}}}{\tau_{\text{int}}}}) \tag{3.23}$$

For an integrator, T_{int} is usually much smaller than τ_{int}. In this case,

$$(1-e^{-\frac{2T_{\text{int}}}{\tau_{\text{int}}}}) \approx \frac{2T_{\text{int}}}{\tau_{\text{int}}} \quad [31] \tag{3.24}$$

Then formula (3.23) can be simplified as

$$Q_{n,out}{}^2 = S_{I_n}(0) \cdot T_{\text{int}} \tag{3.25}$$

The output of the charge amplifier can be seen as an integrator with the output resistance $R_{out} = R_{\text{int}}$. The integration capacitor can be calculated as

$$C_{\text{int}} = C_{NS\_a1\_x} + C_{NS\_a2\_x} \tag{3.26}$$

Then, the only thing left is to refer the noise generated by the transistors to the output which is I_n in the integrator model. The charge amplifier consists of three types of transistors: cascode transistors, input transistors, and current mirror transistors. Since it is known that cascode transistors contribute little noise, we will mainly analyze the noise contribution of the other two types of transistors.

Since the poles at V_{inp}, V_{mpp} and V_{mnp} [5] are at much higher frequency than the output pole, we can ignore the influence of capacitors when we refer the noise to the output. First, the noise contribution of the input transistors is considered and we will take transistor M_4 as an example. As shown in Figure 3.8[5], the noise current of M_4 flows through both M_2 and M_8 and it is amplified by the current mirror. Then, the noise current from the upper current mirror $2I_{n,in\_up}$ and the noise current from the lower current mirror $2I_{n,in\_up}$ meet at the output. Since $2I_{n,in\_up}$ and $2I_{n,in\_up}$ are fully correlated, the output-referred current noise of M_4 can be calculated as

$$I_{n,out\_M_4} = 2I_{n,in\_down} - 2I_{n,in\_up} \tag{3.27}$$

Since capacitors can be ignored,

$$I_{n,in\_up} = I_{n,in\_down} = I_{n,in} \tag{3.28}$$

Therefore,

$$I_{n,out\_M_4} = 0 \tag{3.29}$$

Formula (3.25) shows that the input transistors contribute little noise. In reality, within the bandwidth set by the output pole, there is still a very small portion of the noise current flowing into the capacitor as shown in Figure 3.7. Therefore,

$$I_{n,out\_M_4} \approx 0 \tag{3.30}$$

Obviously, the noise from the current mirror transistors can be directly referred to the output:

$$I_{n,out\_crm} = I_{n,crm} \tag{3.31}$$

[5] Since the circuit is fully symmetrical, only half of the circuit will be analyzed

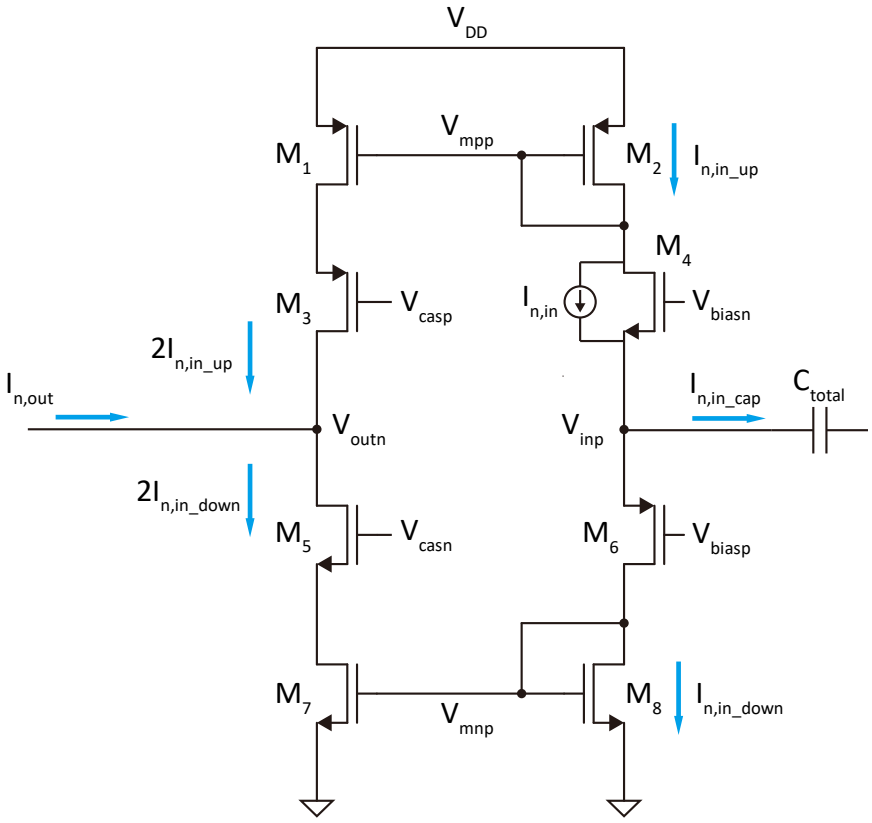


Fig 3.8 Noise analysis of the input transistors

The above analysis shows that current mirror transistors are the main noise sources. Therefore, the output-referred noise spectrum density can be expressed as

$$S_{I_n}(0) = 2kT(g_{m,M_1} + g_{m,M_2} + g_{m,M_7} + g_{m,M_8} + g_{m,M_9} + g_{m,M_{10}} + g_{m,M_{15}} + g_{m,M_{16}}) \tag{3.32}$$

Since the current mirror has a gain of 2, let

$$\begin{aligned} g_{m,crmp} &= \frac{g_{m,M_1}}{2} = g_{m,M_2} = g_{m,M_9} = \frac{g_{m,M_{10}}}{2} \\ g_{m,crmn} &= \frac{g_{m,M_7}}{2} = g_{m,M_8} = g_{m,M_{15}} = \frac{g_{m,M_{16}}}{2} \end{aligned} \tag{3.33}$$

Then, formula (3.29) can be rewritten as

$$S_{I_n}(0) = 12kT(g_{m,crmp} + g_{m,crmn}) \tag{3.34}$$

Therefore, the charge domain output noise of the charge amplifier can be expressed as

$$Q_{n,out}{}^2 = 12kT(g_{m,crmp} + g_{m,crmn})T_{CA} \tag{3.35}$$

It seems that reducing T_{CA} and $g_{m,crmn}$ can reduce the noise. However, this may affect the settling accuracy of the charge amplifier. To find the fundamental way to reduce the noise, we will take settling into consideration below.

First, we substitute formula (3.6) and (3.13) into formula (3.35), and get

$$Q_{n,out}{}^2 = 12kT(g_{m,crmp} + g_{m,crmn})\frac{\alpha C_{total}}{g_{m,in}} \tag{3.36}$$

Let

$$\eta_{gm,crmp} = \frac{g_{m,crmp}}{I_{bias}}$$
$$\eta_{gm,crmn} = \frac{g_{m,crmn}}{I_{bias}} \tag{3.37}$$
$$\eta_{gm,in} = \frac{g_{m,in}}{I_{bias}}$$

η_{gm} is the gm efficiency of the transistor, which is affected by its operating region.

Then, formula (3.36) can be rewritten as

$$Q_{n,out}{}^2 = 12kT\alpha \frac{\eta_{gm,crmp} + \eta_{gm,crmn}}{\eta_{gm,in}} C_{total} \tag{3.38}$$

Formula (3.38) indicates that besides temperature, the charge noise at the output only depends on three factors: the settling accuracy, the operating region of each transistor and the total capacitance discharged by the charge amplifier.

First, the total capacitance is set by system parameters, which we cannot change.

Reducing the settling accuracy can also reduce the output noise. This reflects the trade-off between settling accuracy and noise. As mentioned before, we choose $\alpha = 3$ to achieve sufficient settling accuracy so there is nothing we can do about it.

The only thing we can optimize is the operating region of each transistor. To reduce the noise, we should bias the current mirror transistor in strong inversion and bias the input transistor in weak inversion, which means decreasing the width of the current mirror transistor and increasing the width of the input transistor. However, there is a limitation. The width of the current mirror transistor cannot be arbitrarily small, otherwise the input transistor will enter the linear region. The width of the input transistor cannot be arbitrarily large, otherwise the parasitic capacitor of the input transistor will slow down the charge amplifier. Essentially, factor $\frac{\eta_{gm,crmp} + \eta_{gm,crmn}}{\eta_{gm,in}}$ is limited by the supply voltage. Since we use a 1.8V supply, we have some room to optimize this factor, but not a lot.

Since these three factors have their own minimum value, there is a minimum achievable Q_n, which limits the SNR. As we will see next, this limitation is just around 10-bit. Therefore, this architecture is just enough for our 10-bit design. However, if we want to achieve a higher SNR, this architecture will not work anymore. An improved architecture which tries to break through the SNR limitation will be briefly discussed in section 3.2.

3.1.2.3 Simulation results

The transient simulation of the charge amplifier is shown in Figure 3.9. The maximum residual

charge $Q_{res} = 0.93\,fC$ is used as the input. The amplifier achieves a gain of 1.957 and thus has an absolute gain error of 2.2%.

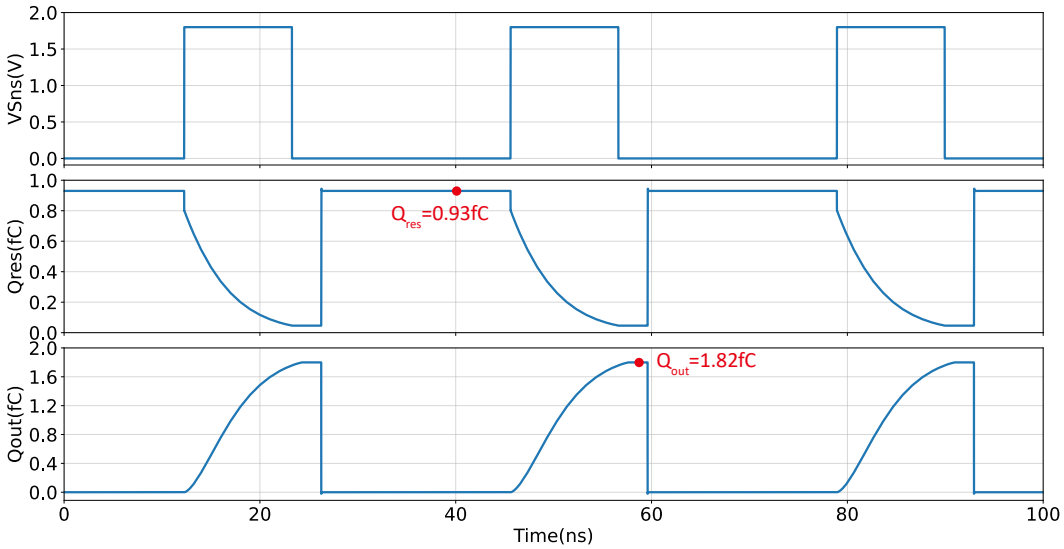


Fig 3.9 Transient simulation of the charge amplifier.

The charge domain noise of the amplifier is

$$Q_{n\_LF} = 174.5aC \tag{3.39}$$

and the equivalent voltage noise is

$$V_{n\_LF} = 289.9uV \tag{3.40}$$

It is a little smaller than our target in Chapter 2, which just satisfies the requirement for the 10-bit design.

The noise break-down of the charge amplifier is shown in Figure 3.10. The simulation result validates previous analysis that the noise of the current mirror transistor dominates.

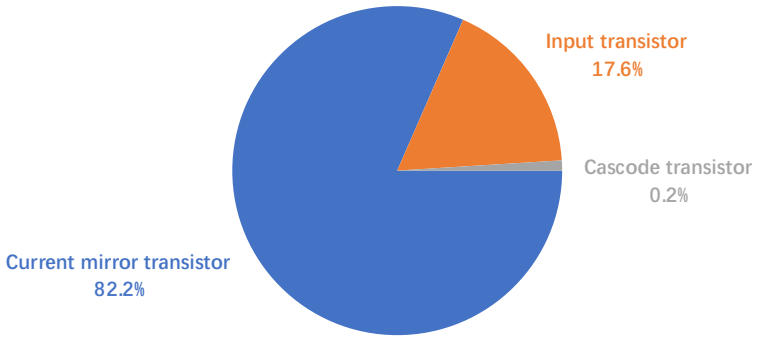


Fig 3.10 Noise break-down of the charge amplifier

3.2 The EF loop filter: an improved architecture

The problem of the charge amplifier in Figure 3.2 is that it should satisfy both speed and noise requirements in a single stage, and thus a trade-off must be made, which limits its SNR. To decouple these limiting factors, auxiliary amplifiers can be added to the input transistors, as shown in Figure 3.11. These auxiliary amplifiers combined with the input transistors can be seen as big input transistors which provide sufficient g_m. With these auxiliary amplifiers, the input transistors can be sized much smaller, and thus much smaller bias current will flow through the current mirror, which greatly reduces the noise generated by the current mirror. Since the current mirror is the dominant noise source in the charge amplifier, the total noise of the charge amplifier will also greatly reduce. Compared with the charge amplifier in Figure 3.2, this improved architecture has a lower slew rate since the bias current is much smaller, but our design does not require a high slew rate since the charge amplifier only needs to amplify very little charge. The power consumption of the improved charge amplifier may increase but a better SNR can be achieved. Therefore, if a higher SNR is required in the future design, this architecture can be used.

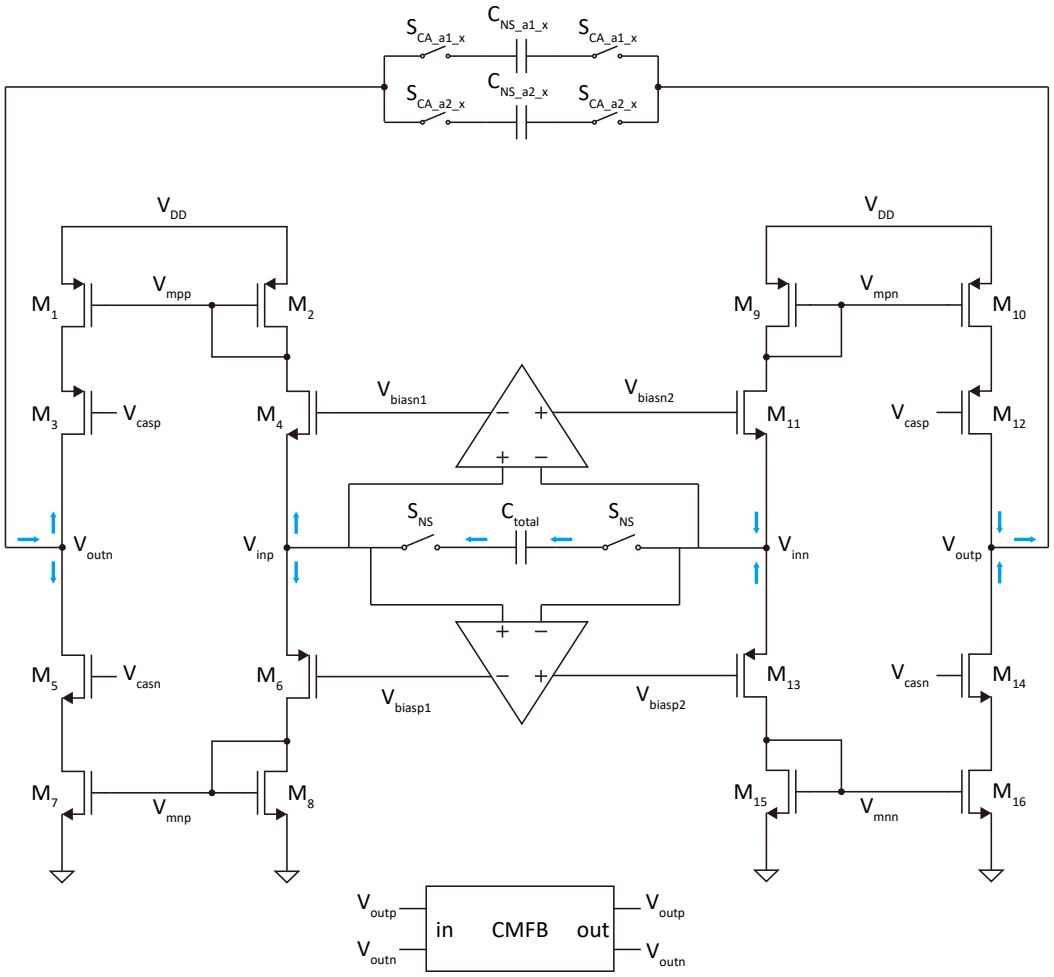


Fig 3.11 The schematic of an improved charge amplifier

3.3 Charge-sharing SAR ADC

The charge-sharing SAR ADC is based on the design in [14]. Some modifications are made as follows.

3.3.1 CDAC

Since an 8-bit SAR is chosen and linearity requirements are relaxed in ultrasound application, we choose to remove the most significant bit capacitor as shown in Figure 3.12. It is worth noting that an extra bit is required to obtain the residual voltage on the CDAC.

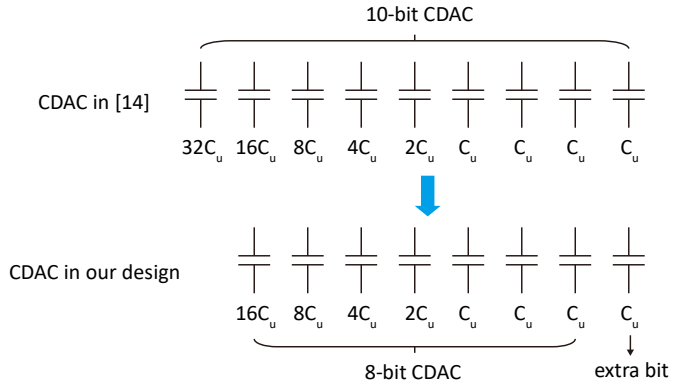


Fig 3.12 CDAC in [14] vs CDAC in our design

3.3.2 Comparator

The comparator is a conventional double-tail comparator with offset calibration and the details can be found in [14]. Since the comparator in [14] is designed for a 10-bit charge-sharing SAR, we choose to modify it to accommodate for a 8-bit charge-sharing SAR by reducing the size of the transistors in the first stage of the comparator. Some parameters are listed in Table 3.1. It can be clearly seen from the table that the average power consumption of the comparator is greatly reduced. This is due to the following three reasons:

(1) Since the comparator noise can be shaped by the EF loop filter, the noise requirement of the comparator is greatly relaxed.
(2) Since the 8-bit SAR is used, there are only 8 conversion cycles per sample instead of 10 cycles.
(3) The sampling frequency is reduced to 30MHz, which reduces the average power.

Table 3.1 Comparison between [14] and our modified design[I]

	[14]	Our modified design
Sampling frequency of the ADC	33MHz	30MHz
Noise	108μV	280μV
Average power	598.7μW	201μW

I Simulation results are obtained with offset calibration turned off.

3.4 Conclusion

In this chapter, the circuit implementation has been discussed. First, the architecture of the EF loop filter has been presented. The key circuit parameters have been derived by analyzing the circuit nonidealities. Simulation results have been provided to validate the previous analysis. Then, an improved architecture has been proposed to address the shortcomings of the previous basic architecture. Finally, the CDAC and comparator have been briefly described. In the next chapter, the simulation results and analysis of the whole circuit will be discussed.

Chapter 4 Simulation results and analysis

In this chapter, the simulation results will be presented and analyzed. We will cover the following topics in turn: basic function, noise, power and area. Finally, a comparison with other designs will be made.

4.1 Basic function

Before discussing the simulation results, we will briefly describe the simulation setup. A single sine wave of 5MHz is applied to the input of BENSSAR and the sampling frequency is 30MHz. 1024 points are calculated to plot the output spectrum. There are still two ideal blocks in whole circuit: the CMFB circuit of the charge amplifier and the digital block that controls the noise-shaping, which will be realized in future work. To make the simulation simple and fast, the reference generation circuit is replaced with a voltage source.

The output spectrum without noise is shown in Figure 4.1. A clear notch is placed in the band of interest. The figure shows that the circuit works as designed achieving a SQNR of 68.10dB and an ENOB of 11.02 bits.

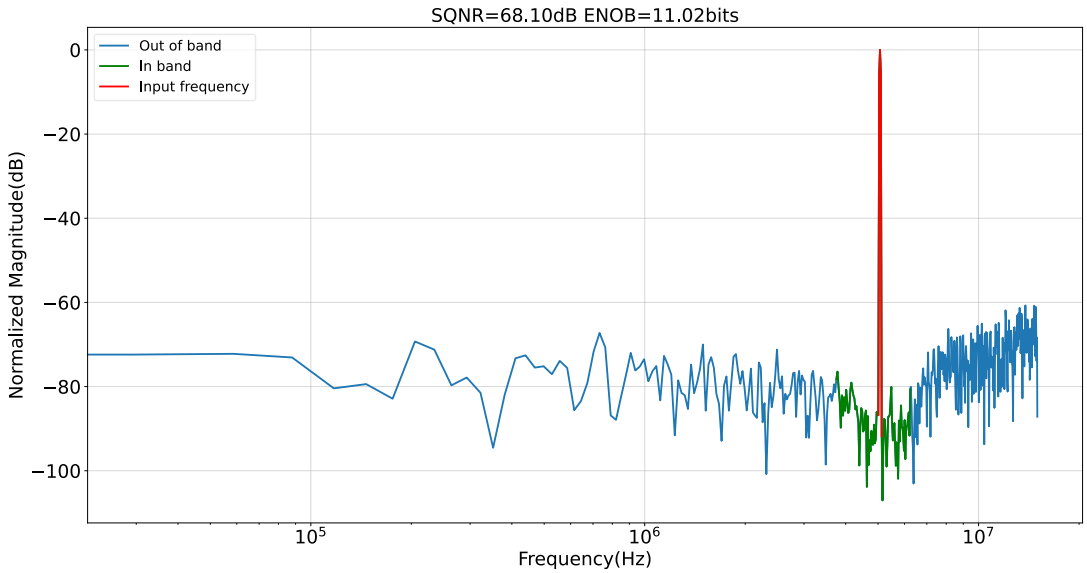


Fig 4.1 The output spectrum of the charge amplifier without noise.

4.2 Noise

After verifying the basic function of BENSSAR, noise is added and the output spectrum is shown in Figure 4.2. We can clearly see that the noise fills up the notch, which degrades the SNR. BENSSAR achieves a SNR of 63.25dB and an ENOB of 10.21 bits.

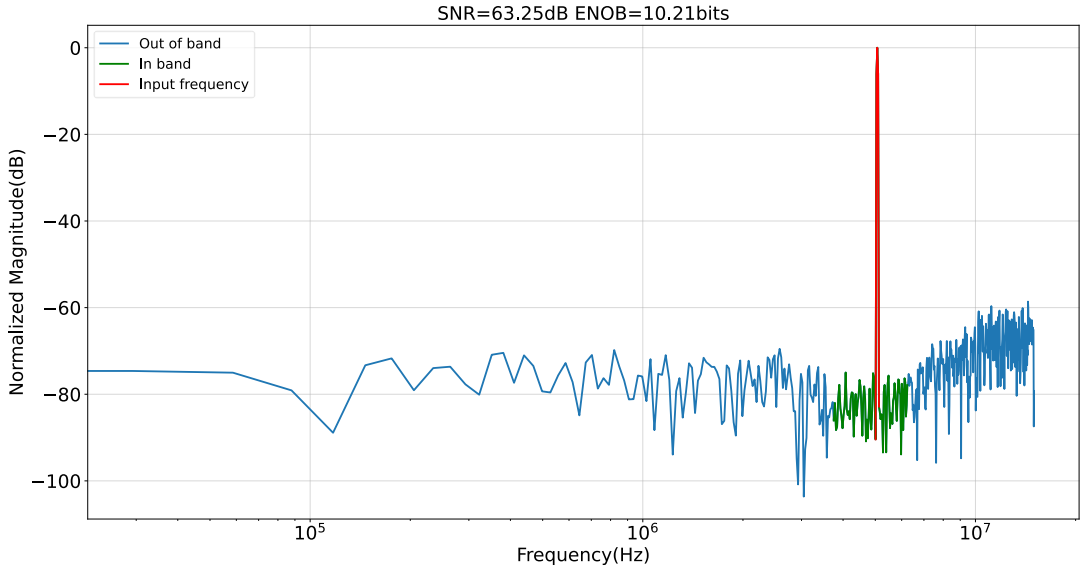


Fig 4.2 The output spectrum of the charge amplifier with noise.

Then, we examine how the EF loop filter's noise and the comparator's noise each affect the overall performance. First, the output spectrum with only EF loop filter noise is plotted in Figure 4.3. As predicted in behavior model simulation in Chapter 2, the EF loop filter noise fills up the notch, resulting in a SNR of 64.52dB and an ENOB of 10.42 bits.

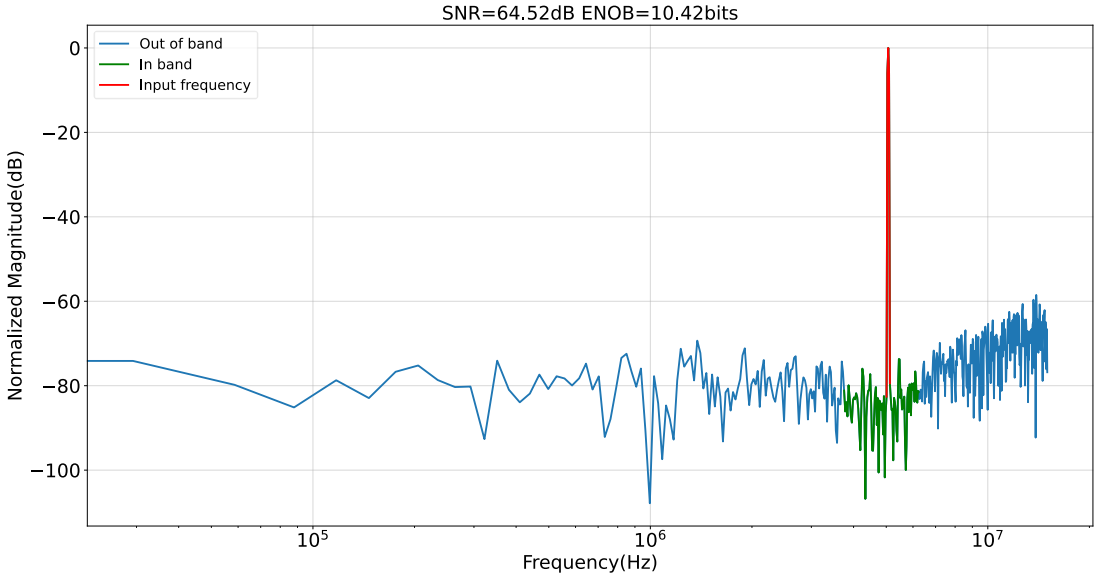


Fig 4.3 The output spectrum of the charge amplifier with only EF loop filter noise.

The output spectrum with only comparator noise is plotted in Figure 4.4. As predicted in behavior model simulation in Chapter 2, the comparator noise is shaped out of band, resulting in a SNR of 65.65dB and an ENOB of 10.61 bits.

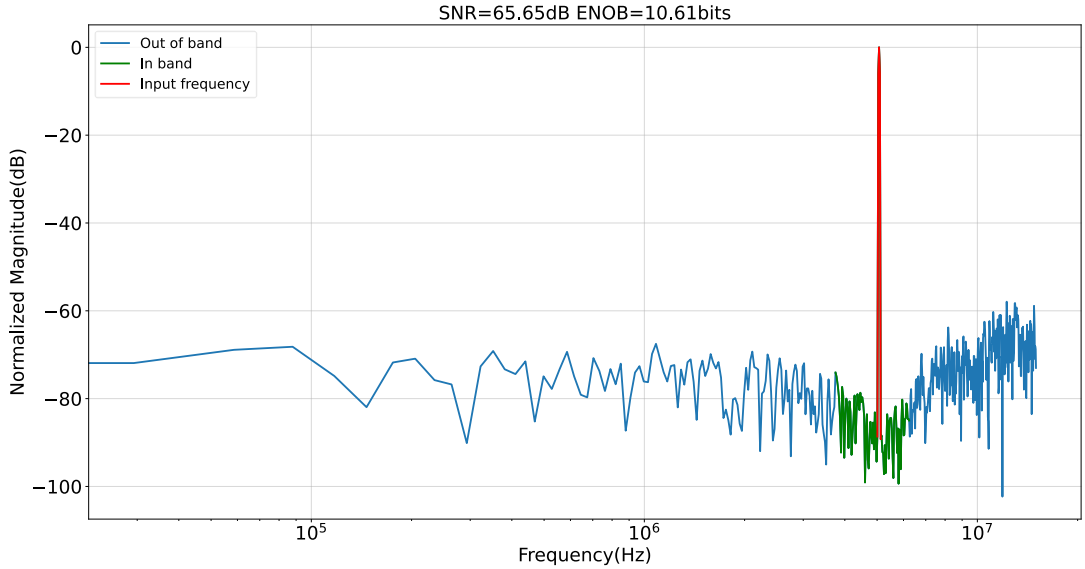


Fig 4.4 The output spectrum of the charge amplifier with only comparator noise.

Table 4.1 below gives a noise summary. The summary shows that the circuit simulation results are generally consistent with the behavioral simulation results. The results indicate that the EF loop filter is the dominant noise source as predicted by behavioral simulation. Compared with the behavioral simulation, the SNR of the circuit simulation drops a little. This drop is because of circuit non-idealities such as kick-back noise of the comparator, and inaccurate gain of the charge amplifier. In addition to these circuit non-idealities, the noise of auxiliary circuits increases the total noise, which is not considered in the behavioral simulation. Since we overdesign each block a little bit, the SNR of the circuit simulation is close to that of the behavioral simulation. A more intuitive comparison of the noise contribution is shown in Figure 4.5.

Table 4.1 Noise summary

	Circuit simulation			Behavior simulation[II]		
Noise type	SNR(dB)[I]	ENOB(bits)[I]	Input-referred noise(μV)	SNR(dB)[I]	ENOB(bits)[I]	Input-referred noise(μV)
Quantization noise	68.10	11.02	111.3	68.20	11.04	110
EF loop filter noise	64.52	10.42	126	64.75	10.46	121.2
Comparator noise	65.65	10.61	96.9	66.63	10.78	72.6
Total noise	63.25	10.21	194.6	63.54	10.26	188.2

I Results include quantization noise.

II Rectangular window is used instead of Hanning window in behavior simulation, which leads to an underestimation of SNR.

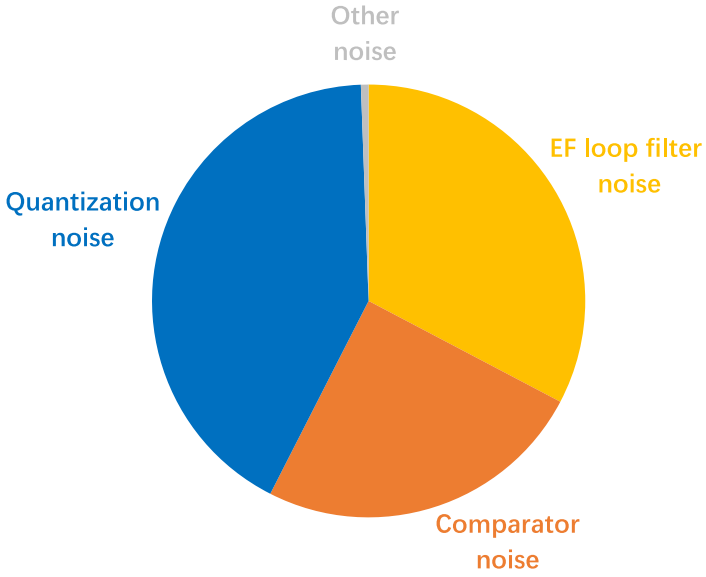


Fig 4.5 Noise break-down of BENSSAR

4.3 Power

The total power consumption of BENSSAR is 1.31mW and the power break-down is shown in Figure 4.6.

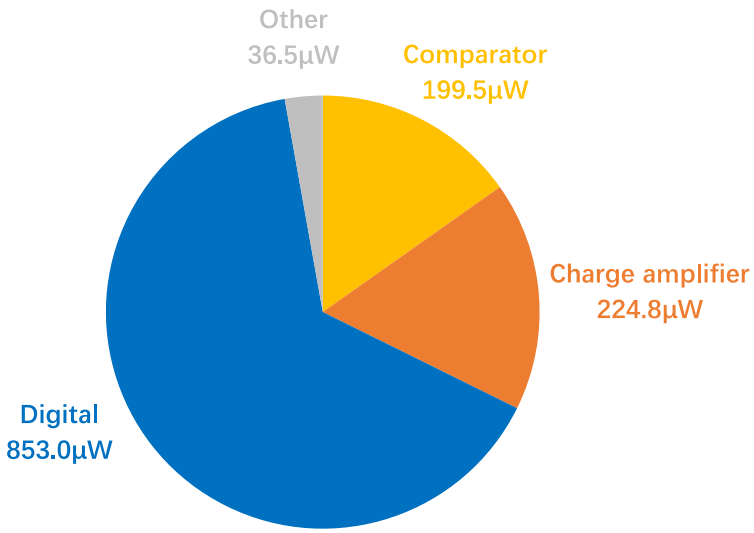


Fig 4.6 Power break-down of BENSSAR

From the figure, we can clearly see that the power consumption of the digital blocks dominates. This is because the power consumption of the digital blocks is not optimized and 0.18µm technology is used. We find out that the SAR logic consumes 340µW and the driver consumes 331µW, which dominate the digital power as shown in Figure 4.7. The driver includes the buffers that drive the

flip-flops of the SAR logic and the buffers that drive the comparator clock. These two parts can be optimized in future work.

The comparator consumes 199.5μW and the charge amplifier consumes 224.8μW. It is worth noting that since the CMFB circuit of the charge amplifier is ideal, the power consumption of the charge amplifier should be higher in reality. However, since the output load of the charge amplifier is more than 10 times smaller than the input load, the CMFB circuit may consume less power than the main circuit. Moreover, since the charge amplifier only operates during the noise shaping process which occupies only 33% of total time, power gating or amplifier sharing can be used to save power. Therefore, despite the fact that the CMFB circuit is ideal, 224.8μW is still a good estimate of the real power consumption of the charge amplifier.

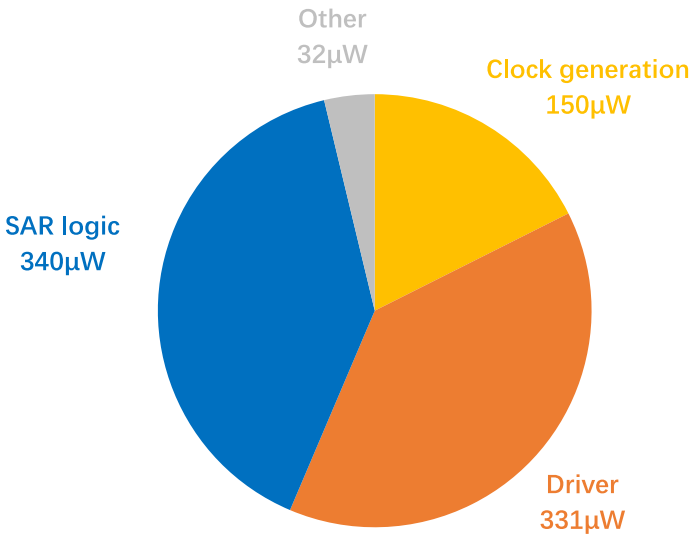


Fig 4.7 Power break-down of digital power

4.4 Area

Since the layout has not been done yet, we can only give an estimation based on the schematic of BENSSAR and the layout of [14]. The area of a SAR ADC is usually dominated by the area of the CDAC and SAR logic. Compared with [14], the CDAC of BENSSAR is 48.5% smaller, which saves 0.008mm^2. The SAR logic is 20% smaller due to the 8-bit SAR, which saves 0.001mm^2. A smaller comparator and smaller buffer in the SAR logic can also save some area. However, the EF loop filter requires a capacitance of 250fF which occupies around 0.002mm^2. The charge amplifier also occupies around 0.002mm^2 due to its large input transistors. The digital control logic of the noise shaping will probably occupy around 0.002mm^2. The total area saved is around 0.003mm^2, which is only 3% of the total area of the beamforming ADC. Therefore, total area of BENSSAR is approximately 0.096mm^2. The area of SAR is 0.043mm^2 and the area of the micro-beamformer is 0.053mm^2.

4.5 Comparison with other designs

A performance summary of BENSSAR and a comparison with the state-of-the-art are shown in Table 4.2 below.

This work achieves a SNR of 63.25dB which meets the SNR requirement of 62dB. The SNR is mainly limited by the noise performance of the charge amplifier. As to be expected, the presented design cannot compete in terms of area and power efficiency with state-of-the-art general-purpose NS-SAR designs like [27], which employ a better technology node and do not realize beamforming functionality. Compared to earlier beamforming SAR ADCs [14,15], a comparable area and power efficiency is achieved. Compared to [32], which reports a noise-shaping SAR ADC for an ultrasound application without beamforming functionality, a more than 2x smaller area is achieved.

Table 4.2 Comparison with the state-of-the-art

	This work[II]	[15]	[14]	[32]	[27]
Process	180 nm	180 nm BCD	180 nm	180 nm BCD	40 nm
Architecture[I]	CS-NS-SAR	CS-SAR & SS	CS-SAR	CR-NS-SAR	CR-NS-SAR
No. of channels per subarray	9	3	9	N/A	N/A
Sampling rate	30 MHz	24 MHz	33 MHz	16 MHz	10 MHz
Center frequency	5 MHz	6 MHz	5 MHz	N/A	N/A
Bandwidth	3.75 MHz – 6.25 MHz	3.6 MHz – 8.4 MHz	3 MHz – 7 MHz	3 MHz – 5 MHz	0.625 MHz
SNR	63.25 dB	52.3 dB[III]	51.8 dB[III]	78 dB	79 dB
Area	0.096 mm^2	0.018 mm^2 [V]	0.099 mm^2	0.19 mm^2 [IV]	0.024 mm^2
Power	1.31 mW	1 mW	1.55 mW	9.15 mW	0.084 mW
FoM_S [VI]	156.1 dB	N/A	N/A	161.4 dB	177.7 dB

I CS-NS-SAR = charge-sharing noise-sharing SAR

CS-SAR = charge-sharing SAR

CR-NS-SAR = charge-sharing SAR

CS-SAR & SS = charge-sharing SAR & single-slope

II Two blocks are ideal: the CMFB circuit of the charge amplifier, the digital block that controls noise-shaping. The power consumption of the beamforming control logic and delay programming logic is not considered.

III Including AFE noise.

IV Estimated from the die micrograph.

V Only 3 channels per subarray so the beamformer is much smaller.

VI Schreier Figure of Merit: $FoM_S = SNR + 10\log_{10}(\frac{Bandwidth}{Power})$.

Chapter 5 Conclusions

5.1 Thesis contribution

A novel beamforming noise-shaping SAR ADC (BENSSAR) for 3-D ultrasound imaging has been proposed in this thesis. The ADC achieves a SNR of 63.25dB in a bandwidth ranging from 3.75MHz to 6.25MHz. The total power consumption of the ADC is 1.31mW and the estimated total area of the ADC is 0.096mm^2. The ADC achieves a Schreier Figure of Merit (FoM) of 156.1dB. Although the overall performance of the ADC cannot compete with state-of-the-art general-purpose SAR ADCs realized in denser technology nodes, our work has discoveries which might be helpful.

(1) This thesis explores the potential of merging beamformer and noise shaping SAR.

Since digitization in the voltage domain requires a buffer between the beamformer and the ADC, charge-domain digitization is preferred. The EF structure typically realizes noise shaping in the charge domain and thus can be easily merged with the beamformer. Since the EF structure is susceptible to the PVT variations, lower-order noise-shaping is preferred over higher-order noise-shaping. For a 2-D array, the SNR requirement is usually moderate because the equivalent transducer aperture for each ADC is small. Therefore, a second-order EF noise-shaping SAR is a good choice to be merged with the beamformer. The merged ADC can achieve a low power consumption because the signals are efficiently transferred inside the ADC. This has been partially confirmed by the simulation results. Although the power consumption of the digital blocks is high, the power consumption of the other parts is kept low. The power consumption of the digital blocks is not an inherent bottleneck of the merged ADC and can be further optimized in the future.

(2) This thesis presents a novel architecture: charge-sharing noise-shaping SAR.

So far, all noise-shaping SAR ADCs in published papers are based on the charge-redistribution SAR. This is probably because most circuits give a voltage output and no additional sample-and-hold circuit is required in a charge-redistribution SAR. However, in an ultrasound system with subarray beamforming, the beamformer can realize the sample-and-hold function, so the charge-redistribution SAR loses its advantage. In contrast, the charge-sharing SAR can be organically merged with the beamformer [14]. However, the charge-sharing SAR has its own disadvantage: the comparator has a higher noise requirement due to the signal attenuation during the charge-sharing process. This higher noise requirement increases the power consumption of the comparator. Since comparator noise can also be shaped out of band in a noise-shaping SAR like quantization noise, the noise-shaping SAR can greatly relax the noise requirement of the comparator, thereby alleviating this disadvantage. Therefore, it is natural to build a charge-sharing noise-shaping SAR to save power. The simulation results have already shown that the power consumption of the comparator is greatly reduced with the help of noise-shaping.

(3) This thesis explores the use of current conveyer in the switch-capacitor circuit.

Since the charge-sharing noise-shaping SAR operates in charge domain, a charge amplifier is required in the EF loop filter. It is problematic to get a charge gain larger than 1. The current conveyer is often used in high speed continuous-time systems, but it can also be used as a charge amplifier. This thesis explores the use of a current conveyer as a charge amplifier in the switch-capacitor circuit. We find out that the noise performance of the basic current conveyor is inherently limited. Although it is just enough for our design, an improved architecture has been proposed to make the current conveyor suitable for the high SNR scenario.

5.2 Future work

The proposed BENSSAR partially solves the problems in the ultrasound circuit design mentioned in the thesis and thus could potentially improve the performance of 3-D ultrasound imaging devices. However, several steps are needed to arrive at a practical demonstrator:

(1) The power consumption of the digital blocks is unacceptably high, so the first thing to do is to optimize the digital power consumption.

(2) The ideal blocks: the CMFB of the charge amplifier and the digital logic that controls noise-shaping should be replaced with real circuits.

(3) Since the charge amplifier operates in class A mode, its power consumption is still high. We can make this charge amplifier operate in class AB mode to save power because the linearity does not matter a lot during the charge amplification process.

(4) The comparator can also be further optimized.

(5) To make a prototype, the layout and post-simulation are required.

In addition, the BENSSAR based on boxcar-integrator-based beamformer is also a promising architecture that is worth exploring in the future.

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