Conducted EMI in Inverters with SiC Transistors

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To my parents: Zhenju Gong and Liangjun Yi

Abbreviations

2D	Two Dimensional
3D	Three Dimensional
AC	Alternating Current
Av	Average detector
AMN	Artificial Mains Network
AZSPWM	Active Zero State Pulse Width Modulation
CENELEC	European Committee for Electro-technical Standardization
CISPR	International Special Committee on Radio Interference
CM	Common mode
CMC	Common Mode Choke
CSI	Current Source Inverter
DC	Direct Current
DM	Differential Mode
DPWM	Discontinuous Pulse Width Modulation
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPC	Equivalent Parallel Capacitance
EPR	Equivalent Parallel Resistance
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EUT	Equipment Under Test
FCC	Federal Communications Commission
FFT	Fast Fourier Transform

GaN	Gallium Nitride
IC	Integrated Circuit
IEC	International Electromechanical Commission
IGBT	Insulated Gate Bipolar Transistor
IMS	Insulated Metal Substrate
JFET	Junction Field Effect Transistor
JBS	Junction Barrier Schottky
LISN	Line Impedance Stabilization Network
MM	Mixed Mode
MOSFET	Metal oxide Semiconductor Field Effect Transistor
NSPWM	Near State Pulse Width Modulation
PCB	Printed Circuit Board
PE	Protective Earth
PFC	Power Factor Corrector
Pk	Peak Detector
PWM	Pulse Width Modulation
RFI	Radio Frequency Interference
Si	Silicon
SiC	Silicon Carbide
SMT	Surface Mount Technology
PWM	Pulse Width Modulation
TDR	Time Domain Refectometry
THD	Total Harmonic Distortion
THT	Through Hole Technology
VSD	Variable Speed Drive
VSI	Voltage Source Inverter

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Actually I had never expected to own a doctoral degree during the 19 years of study. In February, 2008 I was accepted as a PhD student by Electrical Power Processing (EPP) group of TU Delft, the Netherlands. It was such a surprise to me that I can not wait to share this news with my parents. In my childhood, my parents were always alerting me: be diligent, save time and study hard, otherwise I can not even pass the entrance examination to the universities. Looking back upon, although it was a painful experience that I started studying when I was very little, all these efforts become the foundation stone to my success. My parents' words that were used to making me anxious become the encouragements and motivations, driving me forward all the time.

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Xun Gong

Contents

Chapter 1

Introduction

1.1 Background

Electromagnetic Interference (EMI) is defined as any electromagnetic disturbance that interrupts, obstructs, degrades or limits the effective performance of electronic or electrical equipment [Pau06]. Adopting the practice of meeting EMI standards is defined as Electromagnetic compatibility (EMC), which is the ability of a device, unit of equipment or system to function satisfactorily with other electronic systems, and not produce or be susceptible to interference. Before being placed on the market, any power electronics product must be not only functionally compatible with other systems but must also meet legal requirements in virtually all countries of the world.

The switched mode power conversion systems generate EMI noise at each switching transient. Usually the noise is separated into two modes: differential mode (DM) and common mode (CM). The CM noise is defined as the type of EMI noise induced on signals with respect to a reference ground [Ski99]. The DM noise is defined as the type of noise flowing between power supplying cables. As the application of switched power converters increases, concerns about EMC strategies grow for both power electronics system designers and users.

EMI can be categorized into two groups of conducted and radiated emissions [Pau06]. Conducted emission mainly concerns electromagnetic energy that is propagated through cables connecting the system to the grid or interconnecting subsystems. These interference signals pass together with the functional signals. The frequency range where conducted emissions are regulated is generally up to 30 MHz. Radiated emission mainly concerns electromagnetic energy the frequency of which is higher than 30 MHz. In this frequency range the energy is generally propagated in the form of electromagnetic waves through air rather than by direct conduction through cables. In power electronics systems a conducted emission can produce a radiated emission and vice versa.

1.2 Research target and EMC challenges

1.2.1 Research target

As power electronic technology grows, power converters are present everywhere and modify the form of electrical energy in industrial, commercial, and residential environments. As a

result, frequency converters have become the main EMI sources and design efforts are needed to ensure an electromagnetic friendly environment.

In this thesis Variable Speed Drives (VSDs) are investigated, and for the following reasons:

1. VSD for speed control of motors provides energy savings and ease in control. Nowadays it is estimated that 60% ~ 65% of electricity generated in the United States is consumed by motor drives. [Asa93].

2. The switching frequencies of VSDs are in the range of 10 ~ 20 kHz when Insulate Gate Bipolar Transistors (IGBTs) are used. It is possible to increase switching frequencies of existing motor drives by employing new Silicon Carbide (SiC) or Gallium Nitride (GaN) devices.

1.2.2 EMC design in motor drives

The standard industrial solution for VSDs uses induction motors fed by voltage source inverters (VSI). The inverter generates Pulse Width Modulated (PWM) voltages, with dv/dt values of 10kV/µs or more. Consequently, both conducted and radiated EMI have become major problems which make EMC design essential. Many conducted EMC strategies have been developed in the past decades for motor drive systems. They can be categorized into three groups: passive filtering, active cancelling, and other techniques, as shown in Fig. 1.1.

Traditionally, passive filtering methods especially power line filters have mostly been used to suppress conduced EMI. Filter solutions include chokes, high frequency filters, dv/dt suppressors, sine-wave filters, and filters with DC bus connection [Han06; Han07].

Methods of active cancelling usually apply active devices and control to compensate for the dv/dt transients generated by the PWM switching scheme[Jul99; Pia09]. Generally an extra winding is needed to form a coupled transformer which generates the opposite voltage to the other three inverter phases.

The other techniques include: modification of PWM strategy, impedance balancing, modification of motor structure, etc. Detailed reviews on various EMC design strategies will be given in Chapter 2.

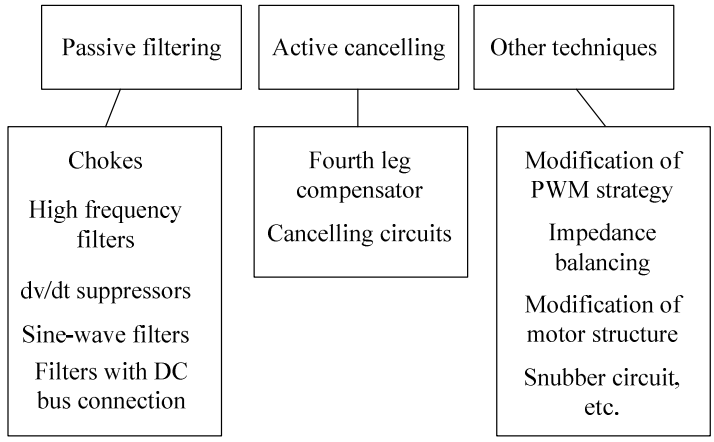


Fig. 1.1 Summary of EMC strategies for motor drives

1.2.3 Technological advances in power electronics and relevance to EMC challenges

Two important technology developments that will affect EMC are SiC power devices and increased integration of inverters.

SiC power devices – faster switching but increased EMI

After 30 years of development, wide band-gap material SiC now has great potential to replace Si as the dominant transistor technology because of its having a number of superior qualities [Ozp10]:

- SiC material's critical breakdown field is approximately 10 times that of silicon, which enables the development of a thinner structure of a stated breakdown voltage, which in turn reduces the channel on-resistance [Cal08].

- SiC has a thermal conductivity of 2.8 times higher than that of Si, providing a much higher current density at a given junction temperature.

- With a band-gap of approximately 3 times wider than Si, the SiC devices also exhibit significantly lower leakage current at high temperature operation [Onl11b].

Although the advantages of SiC material have been recognized since 1980s, immature technology that limited the breakdown performance became the main barrier for the introduction of SiC devices. In 2004, the first successful commercial adoption of SiC Junction Barrier Schottky (JBS) diodes and power switch product – 1200V, 80mΩ SiC MOSFET from Cree - was reported [Das11]. In 2008, the enhanced mode SiC Junction Field Effect Transistor (JFET) that can be used as a direct replacement for Si MOSFETs and IGBTs was announced by the SemiSouth Laboratories, Tennessee, USA. They were applied on an off-the-shelf solar inverter, whose energy loss is effectively reduced by as much as 50% [Onl08]. In this research

the normally-OFF trench SiC power JFETs have been chosen because of the good match of their blocking voltage and current levels with the traditional Si IGBT.

Over the last couple of years, the SiC devices have been subjected to extensive research in an attempt to exploit the above properties. For example, in [Kra09; Fun07], very high converter efficiencies were reported under high temperature and low switching frequency conditions. A comparative study shows that the losses of SiC MOSFETS can be reduced by a factor ranging from two to five, compared to normal Si MOSFETS [Gla11]. The enhanced switching performance of the SiC switches, allowing for increased switching frequencies and lower losses, leads to increased power density by size reduction of magnetic components and heat sinks [Jos11b]. At the same time, EMI emissions are increasing due to the SiC transistors' faster switching speed. Nowadays, with a more stringent EMC environment due to the fast growing power electronics applications, smart EMI filter development that has better filtering abilities becomes essential for the acceptance of SiC power converters.

Higher integration levels – small filters and increased EMI coupling

Increasing the power density is one of the main objectives. Therefore a compact EMI filter design is essential. Nowadays, EMI filters are still most commonly composed of passive components that can make up more than 50% of the volume of the entire system. Numerous techniques, such as topology optimization, components packaging and manufacturing have been developed to reduce the size of EMI filters, while maintaining high filter performances, for example:

- Filter topology optimization

This technique optimizes filter design to fulfill noise attenuations while avoiding over sizing and large components. Usually the focus is on advanced measuring techniques and elements extraction methodology in order to develop an accurate model [Har10; Tar10].

- Integration technology

Integration technology is mostly realized through new component material [Wu11], and reshaping or unifying the component profiles [Jos09; Che03]. Hence optimized spatial design and packaging are achieved.

- Parasitic cancellations

This technique aims to make EMI coupling effects as low as possible [Neu04a; Hel08; Wan06a; Wan08b]. It improves the filter high frequency performance. Generally additional components are added to cancel high influence parasitics such as those in CM capacitors [Wan10; Tao 11].

- Thermally enhanced passives

This technique aims to enhance the components thermal performance of the components in order to operate under high temperature and high power conditions. Examples such as [Wyk03] where the inductor is encapsulated into a heat sink, and [Dir05] the heat extractors are integrated into power passive modules to improve the thermal performance.

1.3 Problem description and thesis objectives

1.3.1 Problem description

EMC problems addressed in this thesis are:

Increased EMI due to the use of SiC devices

The first problem is increased noise emissions due to the employment of SiC transistors. Depending on the circuit configurations, the switching speed of a SiC JFET can be two to six times higher than a traditional Si IGBT [Hor06], which leads to degraded EMC performances. To accommodate SiC switches in motor drives, investigations are necessary to improve filter designs. The questions that need to be answered are: 1. How much would the spectral contents would be increased? 2. How would the filter design be influenced?

Complicated coupling paths and the role of parasitics

Circuit parasitics that were previously neglected start to play a role in EMI production due to the faster switching transients. The capacitive coupling existing in the circuits become more prominent, because they create loops for high frequency noise propagation generated with fast switching due to SiC devices. Hence EMC designs that have high frequency attenuation abilities are essential. Traditional filter designs targeting a too low frequency range may become inadequate.

More sensitive EMI receptors

The third problem is that EMI receptors have become more sensitive due to the reduced logical and threshold levels of the electronic devices. It is necessary to put more effort into limiting the emitted noise in the source or decreasing the coupling effects. For example, the gate threshold the SiC JFET has been reduced to 1.5V which is half of the 3.0V threshold voltage of a traditional Si IGBT. For embedded logical devices as the controller part, the general power supplying voltage has been dramatically reduced from 5V to 3.3V in order to reduce power consumptions, for example, DSP TMS320F2808 which is 3.3V as opposed to classic ADMCF328 from Texas Instruments for motor control. Innovative methods rather than traditional methods, e.g. shielding, insert of the chokes, are preferred in order to lower the system cost and the volume.

1.3.2 Thesis objectives

Based on the problems listed above, the objectives of this thesis are:

- To improve filter performances without increasing volume and cost.
- To provide quantitative understanding on EMC differences when using SiC JFETs and Si IGBTs in motor drive systems.
- To accommodate SiC JFETs in motor drives from EMC point of view.

- To develop a systematic EMI Filter design procedure.

In this thesis the focus is on the remedies and techniques to suppress the conducted EMI of inverters in VSD systems, using wide band-gap SiC JFETs as the switches, within the frequency range of interest from *9 kHz* to *30 MHz*.

1.4 Research method

In this thesis, the following approaches are developed in order to achieve the aforementioned objectives.

1. System modeling using equivalent circuits.

It is proposed that equivalent circuits be used to analyze and predict EMI levels in VSD systems. The predictable frequency range is up to 30 MHz of conducted EMI range.

The state of the art approach and significance of the approach:

Elements extraction is traditionally used for modeling the behavior of discrete components. Depending on the investigation purpose and prediction at concerned frequencies, the model can be adjusted by including elements that cause the corresponding influences, thereby extending the predictable frequency range.

2. Parasitic cancellations in 3D spatial layout.

The filtering performance is enhanced by applying parasitics cancellation techniques which are implemented in 3D spatial layout.

The state of the art approach and significance of the approach:

Previous techniques in this field are implemented in 2D and limited by space and spatial constrains. With the generation of innovative passive components a new concept named 3D parasitic cancellations is proposed. Compared to traditional 2D methods it is more effective in obtaining cancellations while without lowering power density and increasing parasitic loops.

3. EMC comparison between SiC JFETs and Si IGBTs based drive systems.

For comparative EMC studies, two 2.2 kW inverter prototypes which are IGBTs and SiC JFETs based respectively are built using the same layout. Their switching waveforms and spectra are compared in order to identify their EMC differences.

The state of the art approach and significance of the approach:

Nowadays the EMC remedies are mostly applied on the conventional Si IGBT based inverter systems. Even though the previous research unanimously concludes that the use of new SiC power devices increases the level of EMI noise, a quantitative understanding of the differences compared to Si devices is still elusive.

4. SiC noise source suppression.

The implementation of the discrete SiC JFET with external free wheeling diode on top of the substrate creates capacitive coupling that close loops with considerable high frequency EMI propagations. Two substrates of insulated metal substrates (IMS) and heat sinks are employed. The proposed methods include using separated substrates layout, damping circuits, and insert of ferrite beads at difference positions.

The state of the art approach and significance of the approach:
During recent investigations the influence of substrate layout was ignored because the influence is not evident in IGBTs based inverters where dv/dts values are relatively low. Minimization on substrate influences thus becomes critical when SiC power devices are directly attached on top of substrates. The proposed approaches suppress the SiC noise at its source.

5. The procedure of systematic filter design.
Equivalent circuit modeling as introduced in Chapter 3 is used to develop the procedure. The designed filter is applied to the IMS inverter.

The state of the art approach and significance of the approach:
Nowadays, the trail-and-error process is still usually involved when designing EMI filters. The proposed procedure adopts the filter insertion losses as the modeling target, which avoids the onerous tasks of noise source analysis. The model is able to evaluate insertion losses of various filter topologies over a broad conducted EMI frequency range, which is essential in order to achieve an optimized filter design balanced between performance and cost.

1.5 Thesis layout

The layout of this thesis is illustrated in Fig. 1.2.

- Chapter 2 reviews the EMC strategies for VSD systems. Mechanism of EMI generation and propagation is investigated. The reviewed filter strategies include active and passive ones.

- Chapter 3 proposes the equivalent circuit modeling method for EMC performance predictions. A commercial industrial drive is taken as the case study. The parasitic elements are characterized by curve-fitting of impedance-frequency characteristics with the aid of inverter hardware disassembling.

- Chapter 4 presents parasitic cancellation techniques for EMI filters. A new concept named 3D parasitic cancellations for better filter performance is presented.

- Chapter 5 investigates the EMC differences, causes and approaches to improve filter design for SiC JFETs based motor drives, with a comparative Si IGBT based drive as the reference. The inverter prototypes are built using the same layout. Comparisons include switching waveforms and spectra measured by the LISN. The equivalent circuit modeling method is used for analyzing their spectral differences.

- Chapter 6 presents two methods namely the use of separated substrates and a broadband modeling procedure to suppress EMI under the influence of substrate capacitive coupling. The implemented substrates include Insulated Metal Substrate and Heat sink.

- Chapter 7 concludes the achievements and recommends for future research of this thesis.

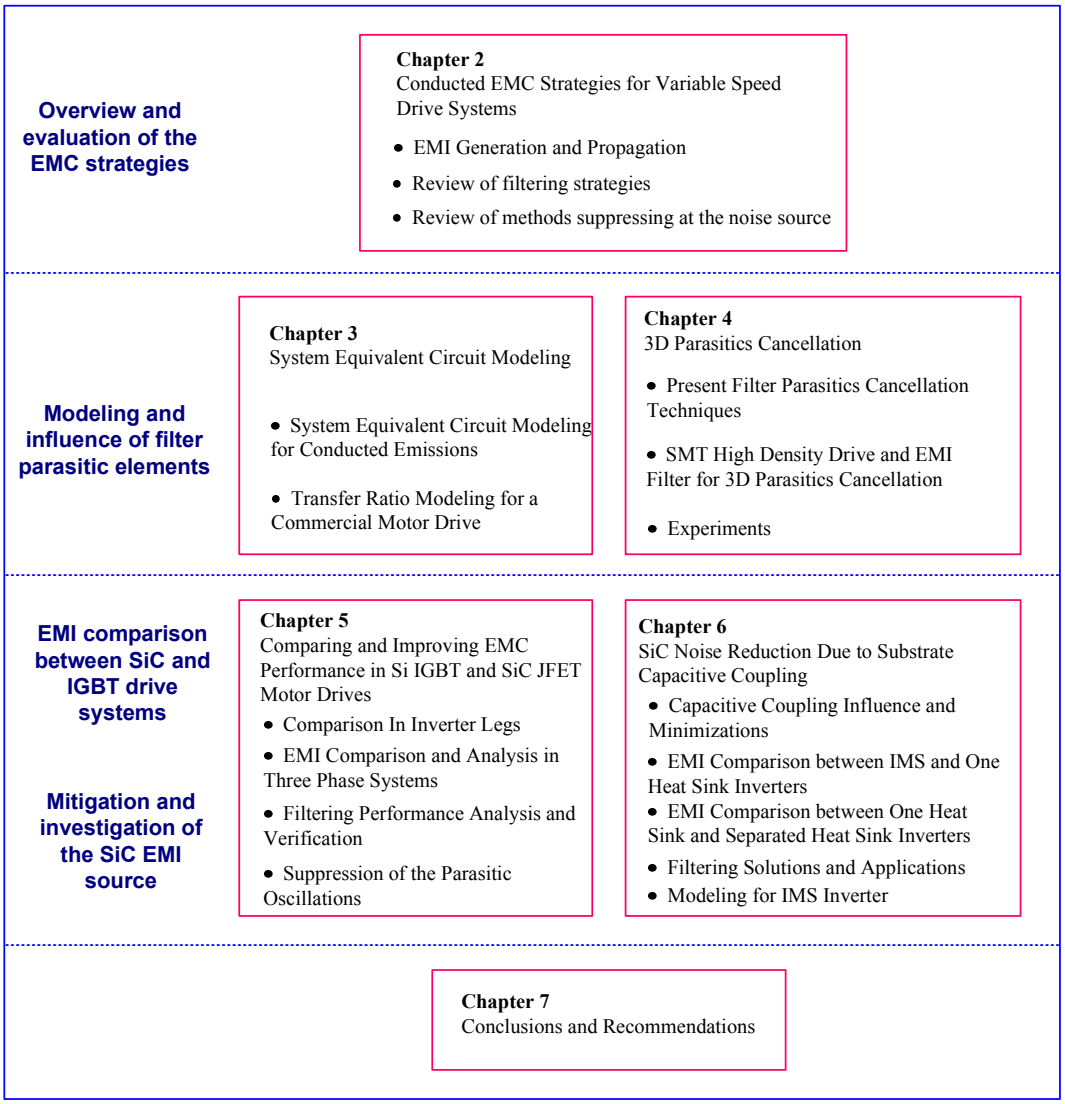


Fig. 1.2 Layout of the thesis

Chapter 2

Conducted EMC Strategies for Variable Speed Drive Systems

2.1 Introduction

Like any other power electronics product, Variable Speed Drives (VSDs) must be designed so as not to interfere with other equipment in the surroundings. To ensure compliance with this requirement, numerous EMC standards are imposed by the authorized departments. In this chapter a common understanding of the EMI generation and propagation mechanisms is provided and the recent research on conducted EMC strategies of variable speed PWM drive systems is reviewed.

Conducted EMI emission is often defined as the undesirable electromagnetic energy emitting from an emitter and entering a receptor via any of its respective connecting wires or cables. The conducted EMC strategies for a VSD system can be categorized into two groups namely passive suppression, and active suppression methods. They can be used in the following three basic ways:

1. Suppress the emission at the noise source
2. Suppress the noise propagation path.
3. Increase the immunity to the noise emission of the receptor

Nowadays passive suppression methods especially the use of a passive filter, are common, because of their relevantly low cost, high efficiency and because they are easy to implement. However, because the switching frequency of the VSD systems is usually below 20 kHz, which is relatively low in the power electronics field, the sizes of the passive filters are usually very bulky. Additionally, as the switching speed of transistor increases, EMI level also increases. The requirements regarding product volume, weight, and cost, lead to the EMI filter becoming smaller and smaller. As a result, in recent years, active suppression methods have been under extensive investigations and developed fast.

2.2 Standards for conducted emission

Standards of conducted EMI can be divided into civilian and military standards and further sub-divided into categories in accordance with different application environments. This thesis focuses on the civilian standards [Yaz79].

There are four major standard imposing authorities: the International Electromechanical Commission (IEC), the Federal Communications Commission (FCC) in the United States, and the European Committee for Electro-technical Standardization (CENELEC) and the European Telecommunications Standards Institute (ETSI) in European countries.

IEC has the biggest number of committees and working groups that are active in more than 40 countries including the United States and most of the European countries [Win88]. Now there are major two IEC technical committees: TC77, which is associated with the IEC 61000 series, and the international special committee on radio interference (CISPR) which is a branch committee initially specializing on radio interference. Nowadays, CISPR has grown into a major authority issuing standards that are used worldwide. Examples of some main standards for conducted emission are:

- CISPR 11: limits for industrial, scientific and medical radio frequency equipment
- IEC 61800-3: limits for variable speed electrical power drive systems
- EN 55011: limits and methods of measurement for industrial scientific and medical radio frequency equipment
- CISPR 12: limits for ignition systems in vehicles
- CISPR 15: limits for lighting
- CISPR 16: measurement equipment and testing techniques

Some EMC standards stipulate the same limits, for example: IEC 60000 series, which define the safety characteristics of environments, measurement instructions, etc. and CISPR 11, which specifies the quality and interoperability requirements for specific equipment types or product families [Onl11a]. Examples of conducted emissions of FCC and CISPR are shown in Fig. 2.1. For the harmonized standards, the equipment are divided into two classes (class A and class B) according to the environment where the application of the equipment takes place, for example, residential, commercial, light industry and industry.

Standard for VSD

The product specific standard IEC 61800-3 deals with the emission limits especially defined for VSD systems. Therefore it is the main standard that is used in this thesis. This standard is further divided into two categories. The first is identical to CISPR 11 class B. The second depends on the agreement among the manufactures and the industry. It is usually the same as

the limits of CISPR 11 class A. Therefore the limits of CISPR 11 are valid for directing VSD as well.

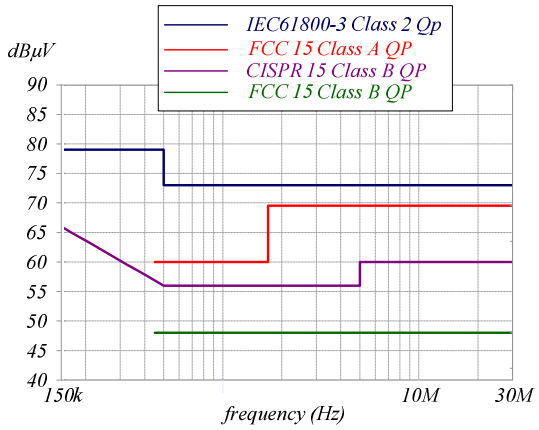


Fig. 2.1 Conducted emission standards of FCC and CISPR

Measurement for VSD

Fig. 2.2 shows the configuration of EMI measurement for the VSD system. The Line Impedance Stabilizing Network (LISN) provides the constant impedance (50 Ω) as seen by the inverter. The noise received by the LISN transmits to the Spectrum Analyzer. A three phase cable is used to connect the inverter and motor. The equipment under test must be placed at least 80 cm away from the LISN according to CISPR 16 standard. To ensure all emitted noise is picked up by the LISN, a copper plate that is connected to Protective Earth (PE) is used to provide the lowest grounding impedance. A detailed description of the LISN is given in Chapter 3, Section 2.1.

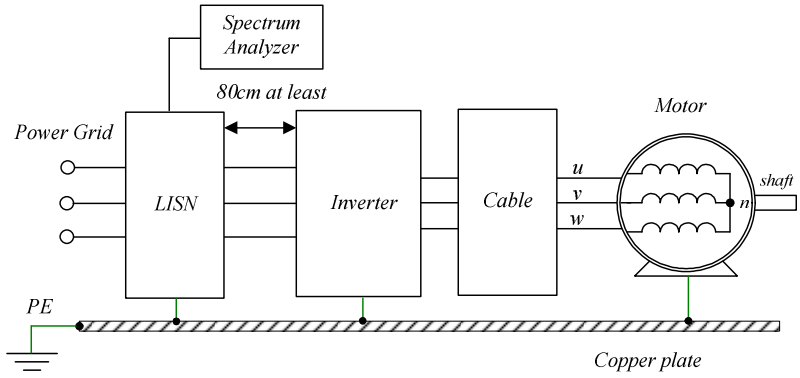


Fig. 2.2 EMI measurement for VSD system

2.3 EMI generation and propagation

Fig. 2.3 illustrates the schematic diagram of a typical voltage source VSD system. The system consists of the three-phase AC source from the grid, line cable, diode rectifier, DC bus capacitors, power semiconductors (IGBT), motor cable and a three phase motor. Usually bulky inductors are needed to reduce harmonic distortion of the line current and to absorb the surges and spikes of the line voltage. The power IGBTs are switched under pulse width modulation (PWM) schemes to generate the three phase fundamental sine waveforms at the inverter outputs. These fundamental sine waveforms are operated at a desired variable output frequency to control the motor speeds, torque, etc. When the semiconductors are fast switched on and off, pulsed voltages appear at the semiconductor drain as the result of the high dv/dt transitions.

In the case of a simple loop with only a single inductor and capacitor, when a pulsed voltage source is induced, the inductor stores the magnetic energy and the capacitor stores the electric energy. Overvoltage occurs at the very beginning of the resonance, and then the two energy-storage components start resonating at a certain frequency. Additionally, fast di/dts are also created as a result of the semiconductor's switching. If the circuit dimension is comparable to the wavelength of this particular resonant frequency, the current loop acts as an efficient loop antenna. The produced current and voltage spikes and oscillations are directly transformed into the contents in the EMI spectrum. These constitute the first level that generates the conducted EMI. Subsequently, the electric and magnetic energy continues propagating and is received by the energy-storage components in the surrounding loops. In this stage the inductive and capacitive mechanisms start playing dominant roles, these constitute the second level that generates the conducted EMI.

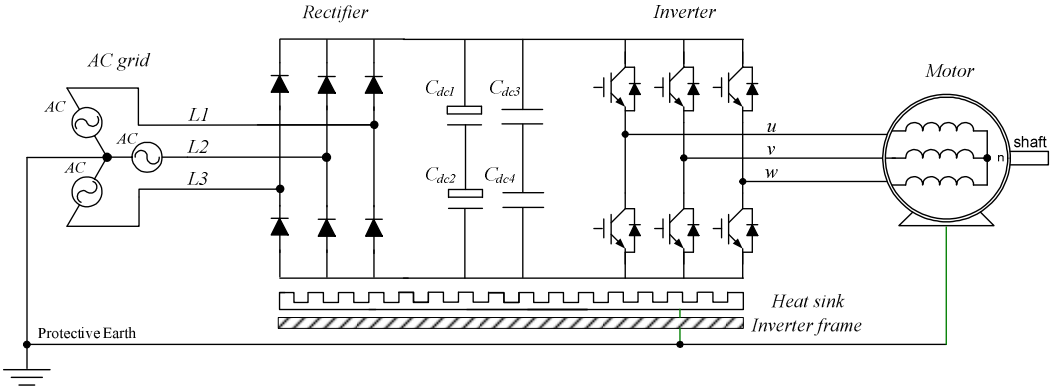


Fig. 2.3 Schematic diagram of a typical inverter driven motor system

2.3.1. EMI propagation mechanisms

EMI propagation can also be regarded as the process of coupling. As the result, one of the most important schemes for EMI suppression is to make the coupling path as less effective as possible. The capacitive and inductive coupling is two dominant mechanisms [Lan06]. The principles are explained in Fig. 2.4 (a) and (b) respectively. The noise source V_1 is as the result of the abrupt voltage change at the transistor switching transitions. As shown in Fig. 2.4 (a),

capacitive coupling occurs due to the stray capacitance (C_s) existing between the two conduction loops. The higher the frequency of the noise V_1, the more easily it is coupled into the external loop. It is estimated that two wires with 2mm diameter and spaced by 1cm creates about 0.1 pF/cm of parasitic capacitance.

As shown in Fig. 2.4 (b), inductive coupling occurs due to the mutual magnetic coupling between two inductors located in two loops. I_{noise} is introduced by a variable current noise source I_1 across the coupled inductor L_{s1}. Coupling magnitude is proportional to the value of di/dt, mutual inductance, distance between two inductors, and the radius of the two loops. Direction of I_{noise} is determined by the right hand rule. It is estimated that two wires with 2mm diameter and spaced by 1cm have about 10 nH/cm of parasitic inductance.

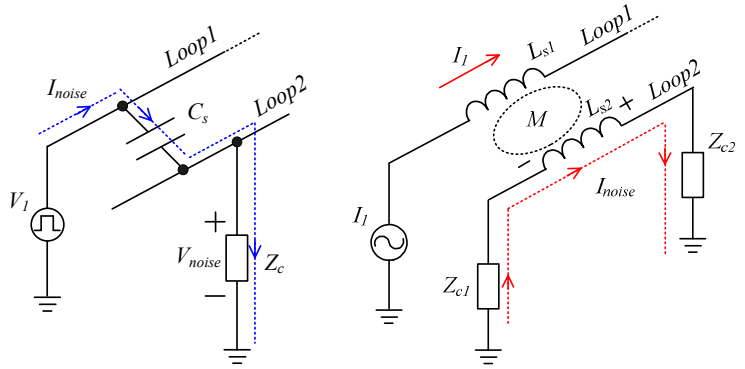


Fig. 2.4 Fundamental mechanisms propagating EMI (a) capacitive coupling (b) inductive coupling

In the motor drive system there are numerous capacitive and inductive coupling points. For the sake of analysis the noise modes are separated into two parts: the Common Mode (CM) and the Differential Mode (DM). CM noise is defined as the noise flowing from the system to earth, and back to the system. Because inverter three phases are considered as symmetrical, all three phase switching nodes are usually summed into one CM source. It can be modeled as square waveform voltage source with respective to the ground. The DM noise is defined as the noise flowing between the system power leads. It is mainly a current source considering the power is mainly flowing in the form of DM.

Another type of elementary EMI is identified as impedance coupling. It occurs when different circuits (e.g. loop *A* and *B*) use the common lines or grounding path whose impedance is Z_m. When noise current in *A* flows through Z_m, a voltage V_m across Z_m is generated. As the consequence, V_m is also seen by *B*. If the noise current or/and Z_m are large enough, the superimposed voltage V_m could be large enough compared to the function signals in loop *B*. The disturbance is induced. In a power system, the noise generated in the power stage can be substantially coupled into its control circuit when a common piece of ground is used. An example is presented in Fig. 2.5.

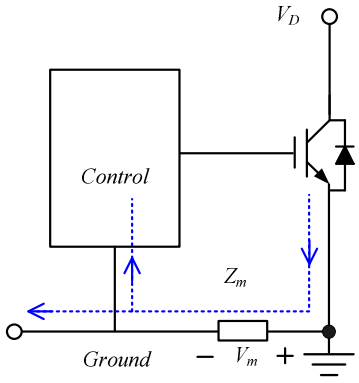


Fig. 2.5 Example of impedance coupling

2.3.2. Noise emission at input

A VSD system can be divided into the rectifying stage as the input and the inverting stage as the output. Noise emits at the switching transient of any semiconductor. Therefore both rectifying diodes at the input and inverting switches at the output are noise sources. Numerous capacitive and inductive coupling points propagate the generated noise to the LISN. Consequently, suppression at the source and making noise coupling as less effective as possible are the two important suppression strategies. In the VSD system, the output inverter part is dominant for noise generation. Therefore this thesis focuses on noise suppressions at the output. Noise propagations are introduced in DM and CM separately in the next sections.

The input source can be either a passive or an active rectifier. Since active rectifier such as buck-type PWM rectifier is much more complicated, it is out of the investigation scope of this research [Nus06].

In a power grid connected three phase diode bridge, noise generates at each transient of phase change. Fig. 2.6 (a) shows the voltage waveforms of the grid which consists of three phases L_1, L_2 and L_3. Points *A*, *B*, *C* indicate the phase change transients. Fig. 2.6 (b) shows the current flow at the transients of phase change from L_1 to L_2. C_1 is the parasitic capacitor of the diode D_1. During the period between point *A* and *B*, the current flows through D_1 in the direction of the arrow. The voltage across C_1 is the conducting voltage of D_1 (around 0.7 V). At the transient of point *B*, the DC+ bus voltage is taken over by phase L_2, D_1 is blocked. C_1 discharges and then recharged in the reversed direction. A reverse recharging current which is also the noise current is formed, as indicated in Fig. 2.6 (c). The voltage across C_1 is the difference between L_1 voltage and L_2 voltage. The noise magnitude is proportional to the values of C_1 and voltage change speed (dv/dt). The noise fundamental frequency is three times of the power grid frequency. During phase change, the resonances between C_1 and parasitic inductance of the diode generate the noise harmonics.

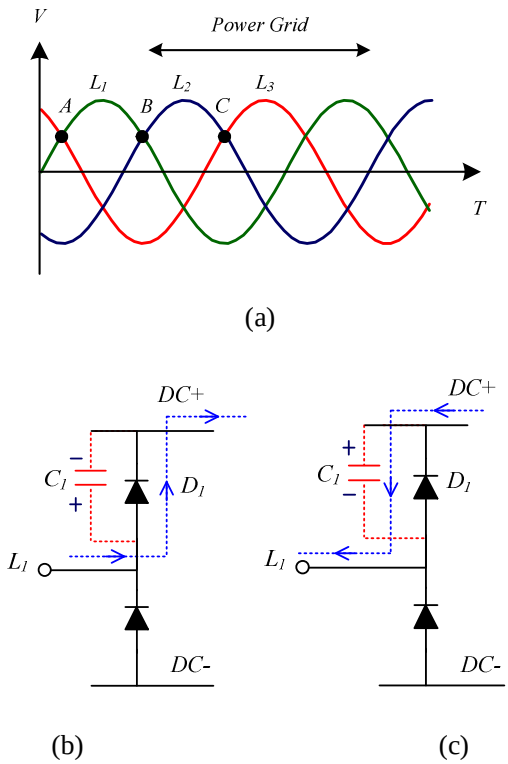


Fig. 2.6 Transient of phase change in the passive rectifier

Applying input filters is very common in power electronic converters. Due to the presence of bulky inductors, noise coupling occurs between filter and power inductors. [He05] investigates the magnetic coupling effect in a PFC converter. It is found that the filter attenuation level is greatly deteriorated due to the magnetic coupling between the input CM filter and PFC inductor, while the electric coupling is not that important. [Poo03] analyzes how coupling can substantially influence the EMI that is measured by the LISN. A lumped circuit model that contains essential coupling paths is proposed.

Noise can be coupled into the converter from input due to the use of long input cables. Fig. 2.7 illustrates an example. Converter 1 and 2 are connected to the same power source. Converter 1 applies CM capacitors both from input to PE (C_1) and from output to PE (C_2). CM loop1 is formed, and CM current from converter 1 dominantly circulates in this loop. Since long input cable for converter 2 is used, the radiuses of both CM and DM current flowing loops are increased. Based on inductive coupling mechanism, noise coupling from CM loop1 into CM loop2 and DM loop2 becomes much easier.

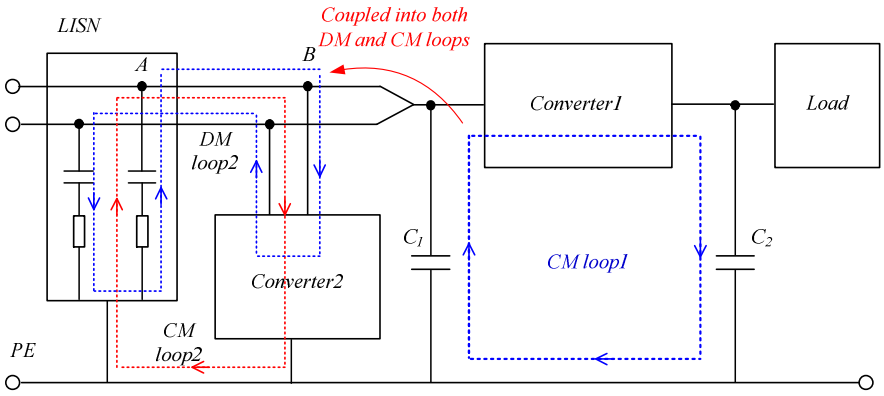


Fig. 2.7 Noise coupling due to long input cables

2.3.3. Noise emission at output

Inverter generates the output signals and it is the main noise source of the VSD system. It is the focus of this thesis.

DM propagation

DM source has a smaller propagating loop. In VSD system it appears as the current spikes or oscillations superimposed on the functional signal waveforms at the inverter output. Fig. 2.8 presents the DM noise propagation due to capacitive coupling at the VSD output. The noise currents are shown in dash line and flow through LISN phases in series. At the turn on transition of the upper switch V_1, the DM noise is generated from the following coupling paths:

- I_{ps} due to the dv/dt imposed across the parasitic capacitance in parallel to the lower switch (C_{ps}).
- I_{uw} due to the dv/dt imposed across the parasitic capacitance between the output phase cables (C_{uw}).
- I_{ug} due to the dv/dt imposed across the series connection of line-to-ground parasitic capacitance (C_{ug}) and back to the phase *w* through the drain-to-ground parasitic capacitance (C_{wg}).

The DM noise magnitude depends on the voltage transient slope and the impedance along the DM current propagation path. The DM noise frequency depends on the contents frequency

from the source and the oscillations occurring between the inductive and capacitive components along the DM propagation path.

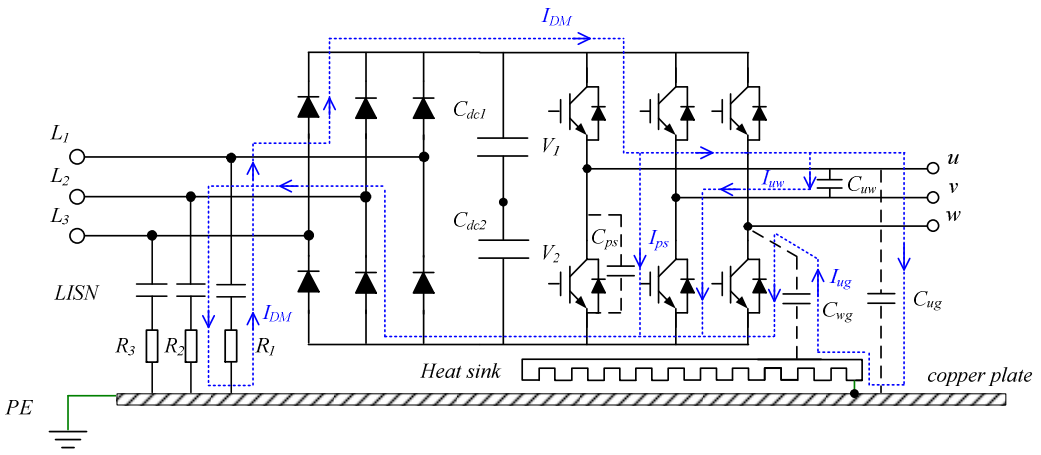


Fig. 2.8 DM noise propagation due to capacitive coupling

DM noise propagation due to inductive coupling predominantly occurs in the cables and motor windings. Fig. 2.9 shows the DM inductive coupling occurring between two phases in the output cable. As can be seen from Section 2.3.1, good coupling nature between cables and motor windings makes this form of coupling very harmful.

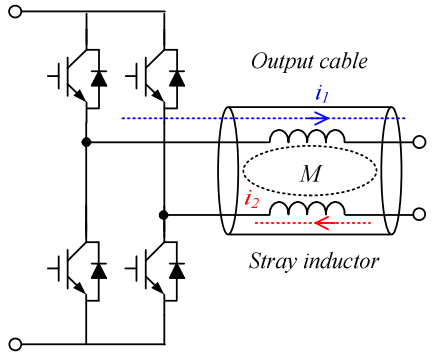


Fig. 2.9 DM noise propagation due to inductive coupling

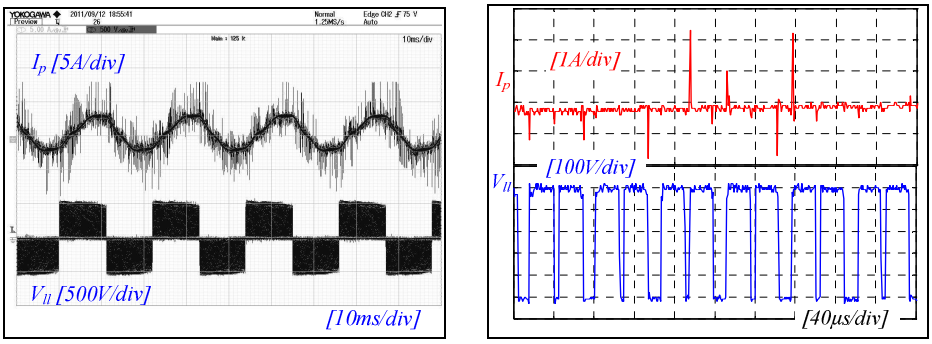
Fig. 2.10 shows a measured typical line-to-line voltage (V_{ll}) and the PWM modulated sine wave output phase current (I_p) of the inverter. Fig. 2.10 (b) is the time-expanded scale of Fig. 2.10 (a). The repetition rate of the voltage pulse is the carrier frequency. There are no external filtering components when performing the waveform measurements except four DC bus capacitors positioned across the DC bus, as shown in Fig. 2.3. It can be seen that the current noise is generated at the moment of each switching transition. The conducted DM noise consists of all those current spikes that are superimposed on the fundamental current sine wave. The waveform I_p consists of three components:

- The fundamental sine waveform which is generated based on the PWM modulation scheme.

- The ripple current which is generated due to the switched mode at the carrier frequency.

- Current spikes to charge and discharge the coupled parasitic capacitors (C_{ps}, C_{uw}, C_{wg}, and C_{ug} in Fig. 2.8) as introduced in the previous paragraph.

The source or victim from inductive coupling can be a component, for example, filter inductor, parasitic inductance of a capacitor, printed circuit board (PCB) trace loop, or a motor winding. As DM loops are much smaller than CM loops, inductive coupling mainly induces DM sources [He05].



(a) (b)

Fig. 2.10 (a) Pulsed DM voltage and current waveforms of a PWM switched variable speed drive (b) DM waveforms in expanded scale, where V_{ll} is the inverter output line-to-line voltage, and I_p is the motor phase current

CM propagation

The CM noise is much more harmful and dominates the EMI spectrum. In VSD system it appears as the noise currents flowing though PE and being picked up by the LISN. Capacitive coupling is the main mechanism. Fig. 2.11 is the simplified presentation of the CM noise propagation from the inverter. The noise currents are shown in dash line and flow through LISN phases in parallel. When the switch V_6 is turned on, CM noise is generated from the different coupling paths:

- I_{dg} due to the dv/dt imposed across the parasitic capacitance (C_{dg}) between the switch drain and the grounded heat sink.

- I_{wg} due to the dv/dt imposed across the parasitic capacitance between the output phase cable *w* and the earth (C_{wg}).

- I_{ng} due to the dv/dt imposed across the parasitic capacitance between the neutral point of the motor windings and the motor frame (C_{ng}).

The CM noise magnitude is dependent on the voltage transient slope and the impedance along the CM current propagation path. CM noise frequencies are the result of the spectral contents from the source and the oscillations occurring between the LC components along the CM propagation path.

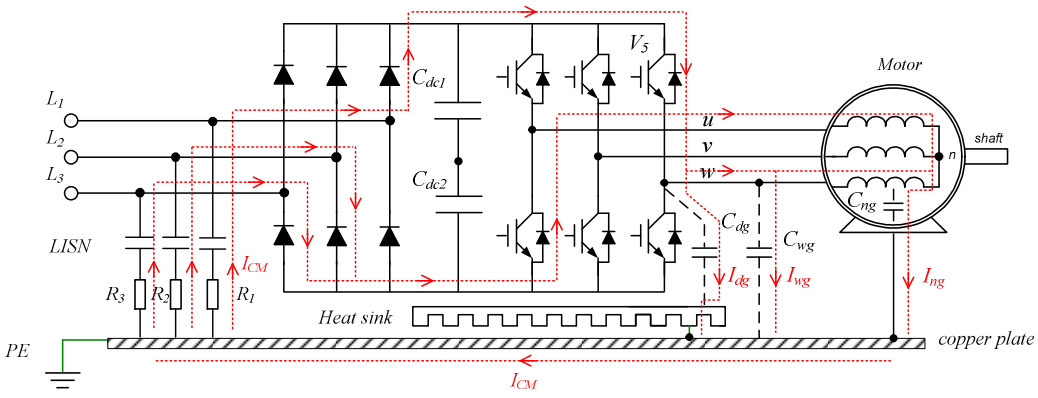


Fig. 2.11 CM noise propagation due to capacitive coupling

Following the same theory as DM inductive coupling mechanism, CM noise is also coupled into PE cable from phase cables as shown in Fig. 2.12.

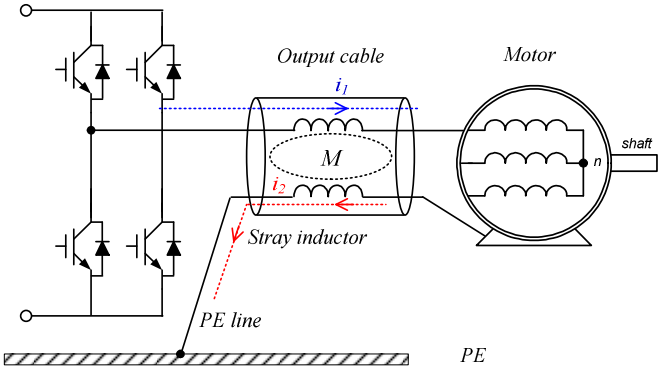
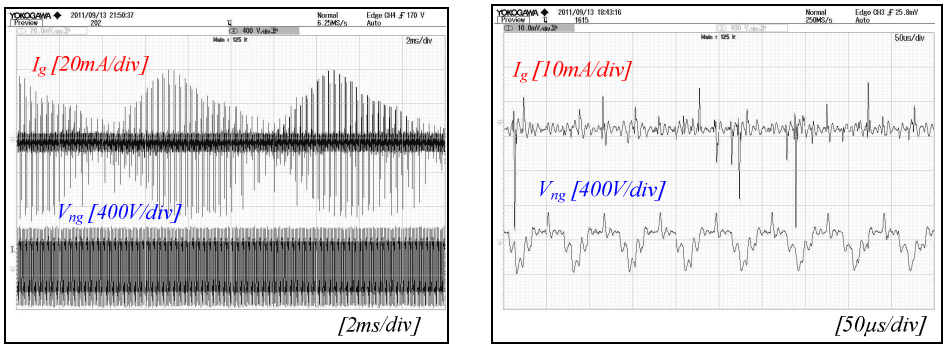


Fig. 2.12 CM noise propagation due to the inductive coupling

Measured typical CM waveforms of a VSD system are shown in Fig. 2.13. Fig. 2.13 (b) is the time-expanded scale of Fig. 2.13 (a). V_{ng} is the voltage between the neutral point of motor windings and earth. I_g is the earth current that is contributed from all VSD phases and motor windings. It can be seen that the I_g waveform is comprised of a low frequency 150 Hz modulated ripple component which is further modulated by the PWM high frequency switching. Generation of the $+I_g$ at 150 Hz is due to the summed plus voltage of the inverter three phase outputs referred to the earth, and likewise generation of $-I_g$ at 150 Hz is due to the summed minus voltage of the inverter three phase outputs referred to the earth. Corresponding

to each switching transient, there is a generated CM current spike. According to the PWM switching technique, the voltage at the inverter output phase nodes of *u*, *v* and *w* are pulsed between the DC+ bus voltage ($+V_{dc}/2$) and DC- bus voltage ($-V_{dc}/2$). When taking the motor winding neutral point n as the reference, the CM voltage source between n and earth is step-wised with the discrete values of $\pm V_{dc}/2$ and $\pm V_{dc}/6$ (see Fig. 2.13 (b)). The frequency is three times that of the carrier frequency. The components of the waveform I_g consist of the charging and discharging currents of the parasitic capacitors (C_{dg}, C_{wg}, and C_{ng} shown in Fig. 2.11).



(a) (b)

Fig. 2.13 (a) CM pulse voltage and current waveforms of a PWM switched VSD (b) CM waveforms in expanded scale

2.4 Review of suppression strategies along noise coupling path

The noise suppression strategies on noise coupling paths can be categorized into four methods as follows:

- Front stage passive filters positioned at the inverter input
- Output passive filters positioned between the inverter output and motor cables
- Proper low and high frequency grounding
- Other passive methods to capture and return the noise to the source

2.4.1. Passive filters

Passive filters are the most widely used to suppress the noise along the propagation path because of the relatively low cost and high effectiveness. Their general functions are hindering the noise current propagating to the mains by providing high impedance in the direction to the mains and/or by providing paths with low impedance around the rectifier elements which are responsible for the generation of the noise sources. Thus the noise currents are circulated back internally. The EMI filter is a combination of inductors and capacitors. Design of the EMI filters is based on the needed attenuation which is the differential amplitude between the noise magnitude and the standard to be complied with. Previous research has developed many filter design procedures to determine the filter topology and component values [Cap02; Oze96;

Nag00; Yua96; Nus06; Har10]. However at certain stages the trial-and-error process is always involved. Because the complicated high frequency behavior of the filtering components, the influence of circuit parasitics, and the dynamic power signal flowing make the precise calculations or measurements of the noise coupling impedance nearly impossible.

EMI passive filter performance is dependent on two aspects:

1. The frequency-impedance characteristic of the filter itself.

2. The frequency-impedance characteristic from the source of the inverter system under test.

This can be seen from the simplified CM equivalent circuit model of the VSD system shown in Fig. 2.14, where V_{CM} is the CM noise source, Z_s is the impedance-frequency characteristic of the inverter source, Z_f is the impedance-frequency characteristic of the applied filter, Z_L is the impedance-frequency characteristic of the LISN. It can be seen when excluding the noise emission from CM source, the CM noise magnitude received by the LISN is determined by the Z_s and Z_f together. Moreover, the impedance provided by them can not be constantly high within the frequency range of conduced emission. Therefore for an effective EMI filter design, it is critical to determine the impedance valleys that are caused by the component resonances, both among the components of the filter itself and among those between the filter and external circuits. Some of the modeling methods target on characterizing the noise source impedance, for example, the methods described by [Zha00; Yak04; Tar10], some of the methods target on characterizing the filter itself, for example, he methods described by [Kot11; Ste11; Mir07], while most of them consider the entire impedance over the coupling path, as was done in the studies of [Lei10a; Liu07; Ran98; Men06; Gra04].

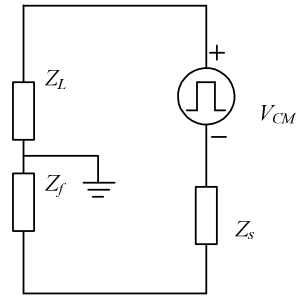


Fig. 2.14 Simplified CM equivalent circuit model of a VSD system

Although there are basic guidelines for filter determination, specific considerations are always needed to figure out the most suitable design in different cases. There are normally two install locations for the passive filters in a VSD system. They are shown in Fig. 2.15. The first is at the inverter input before the power flows through the switches. The placed filter is accordingly called a front stage filter. Depending on being placed before or after the rectifier, the front stage filter can be separated into AC line filter and DC bus filter. Since AC line filters

can mostly fulfill the filtering requirements, DC bus filter is rarely seen [Zha09]. The second is at the inverter three phase output and the placed filter is called output filter.

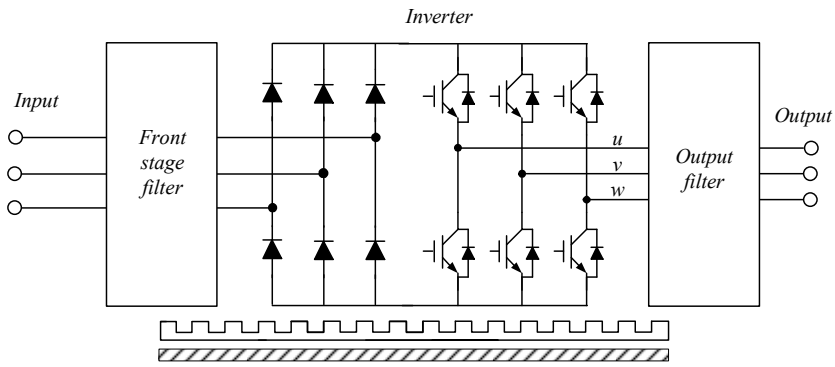


Fig. 2.15 Install locations in the VSD system for passive filters

From the function point of view the passive filters are divided into CM and DM filters respectively. They are usually combined in order to save the volume and cost. The leakage inductance is usually taken as the DM inductance. Fig. 2.16 depicts an expanded CM model of the VSD system from Fig. 2.14 to explain the role of CM passive filters, which is fundamentally conducting the CM leakage currents back to the source (V_{inv}) before they flow into the LISN. The CM voltage noise source formed by the arbitrary PWM voltage signals is shown as V_{inv}. The assumption is that the layouts from the three inverter legs are symmetrical to the earth. The generated CM leakage currents flow along the motor load, ground, LISN and then back to the AC lines.

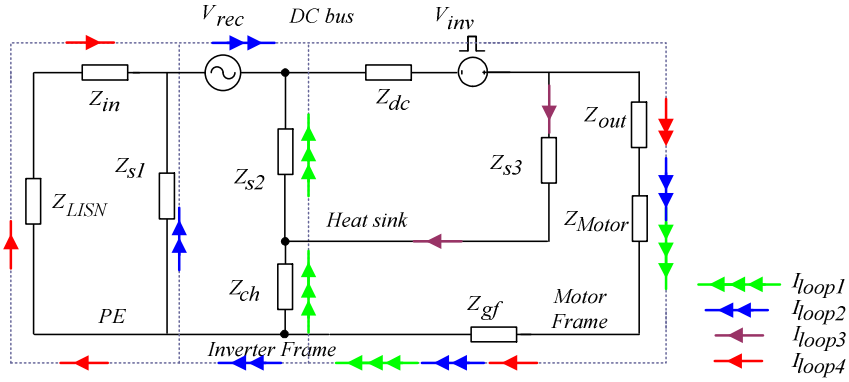


Fig. 2.16 Simplified CM model to explain the role of CM passive filters in directing the CM currents

where:

- V_{inv} is the common-mode voltage source
- V_{rec} is the noise source of the rectifier
- Z_{LISN} is the equivalent impedance of LISN

- Z_{dc} is the lumped inductance of the DC-bus
- Z_{in} is The impedance between the LISN and inverter input terminals
- Z_{s1} is The impedance between the inverter input and the protective earth
- Z_{s2} is the impedance between the inverter DC-bus and the heat sink
- Z_{s3} is the impedance between inverter output terminals and the heat sink
- Z_{out} is the impedance between the inverter output terminals and the motor
- Z_{Motor} is the equivalent impedance of motor
- Z_{ch} is the impedance between the inverter heat sink and the inverter frame
- Z_{gf} is the impedance between the motor frame and the inverter frame

In VSD system, V_{in} appears at the switching nodes of low side switches at every switching transient. For simplification the three phase nodes are summed as one. V_{rec} appears at the transients that diodes are turning on or turning off. It is simplified as a 150 Hz (three times of the grid frequency) low frequency noise source. For the front stage filter the rule is to increase the ratio of T_1 or T_2 which are expressed by (2.1) and (2.2) respectively.

$$T_1 = \frac{I_{loop1}}{I_{loop1} + I_{loop2} + I_{loop3} + I_{loop4}} \tag{2.1}$$

$$T_2 = \frac{I_{loop2}}{I_{loop1} + I_{loop2} + I_{loop3} + I_{loop4}} \tag{2.2}$$

Likewise for the output filter the rule is to increase the ratio of T_3 as expressed by (2.3).

$$T_3 = \frac{I_{loop3}}{I_{loop1} + I_{loop2} + I_{loop3} + I_{loop4}} \tag{2.3}$$

Front stage filter

A front stage filter is the most common solution in VSD systems. Apart from the reasons of simplicity, low cost and effectiveness, another reason is to prevent EMI noise interaction between the tested power electronic system and the surroundings [Nav91]. A comprehensive design procedure for a CM input filter design was performed in [Tus06]; A two stage CM filter is designed to comply with the standard of CISPR 22(see Fig. 2.17). Beforehand a simplified model of the CM noise propagation was developed and the relevant parasitic impedances are identified.

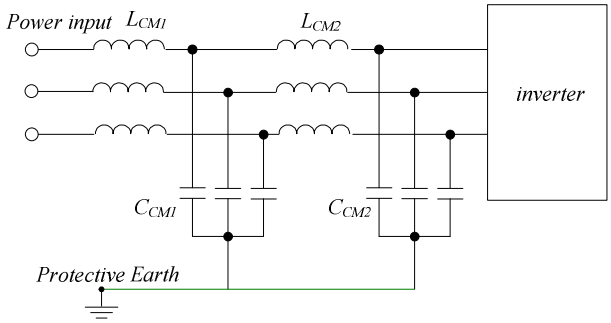


Fig. 2.17 Two stage CM filter topology designed in [Nus06]

The inductor choke inserted in the propagation path mitigates the peak value of the noise currents. The choke design involves many issues, such as core material and geometry selection, power losses, winding arrangement and inductance. These are investigated in many papers, for example, A. Muetze, et al. provides a simplified calculation method for CM choke design which significantly reduces the task [Mue06]. Ogasawara, et al. proposes a simplified CM equivalent model to calculate the CM current reduction magnitude in the VSD system (given in Fig. 2.18) [Oga96]. The method shows that the choke inductance can be calculated for any desired reduction of the CM peak current. Based on Ogasawara's work, a higher order CM equivalent circuit model is proposed in [Mei02]. The selection of the choke parameters and the corresponding response of the system are discussed. The author also provides guidelines for core material selection and winding arrangement. A behavioral model to evaluate the CM choke is proposed in [Roc07]. Designers could use measured values of currents, voltages and physical system impedance, etc. to model the dynamic behavior of the choke. Thus the CM current magnitude with inserted CM choke can be predicted. All the above information is very useful when seeking to understand the role of the input inductors.

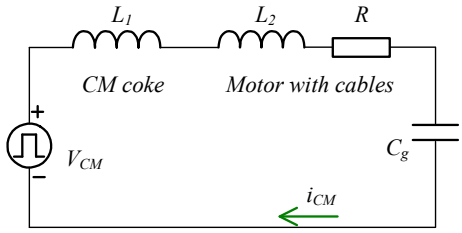
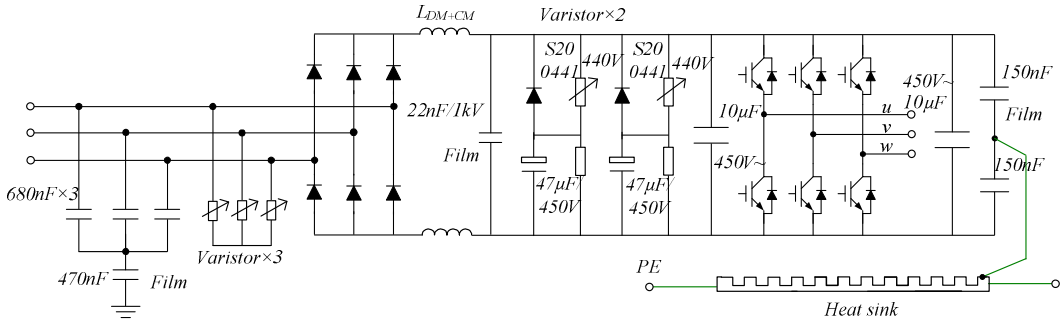


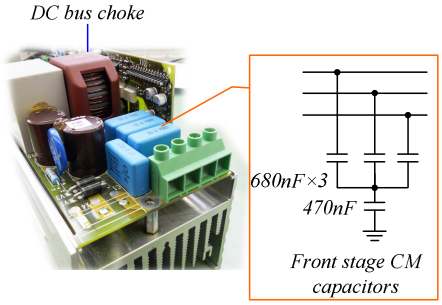
Fig. 2.18 The CM equivalent circuit model proposed in [Oga96].

In the commercial production of motor drives, especially in the medium power range, front stage passive filters are implemented in more than 90% of the drives. Of these the simplest topologies of C and LC are mostly selected. Fig. 2.19 presents the circuit diagram and photograph of the employed front stage CM filter of a 2.2 kW commercial motor drive (SEW Movitrac07A). It can be seen from Fig. 2.19 (b) that the four capacitors are in Y connection which on one hand limits the capacitance to prevent the high leakage currents flowing into the earth, and on the other hand serves as both DM and CM filters. Fig. 2.20 presents the circuit diagram and photograph of the employed front stage CM filter of another 2.2 kW commercial motor drive from Schneider Electric (Telemecanique Altivar 31ATV31HU22N4). It can be

seen that a LC filter consists of a three phase choke, and five Y- capacitors are employed as the CM filter at the AC line side.

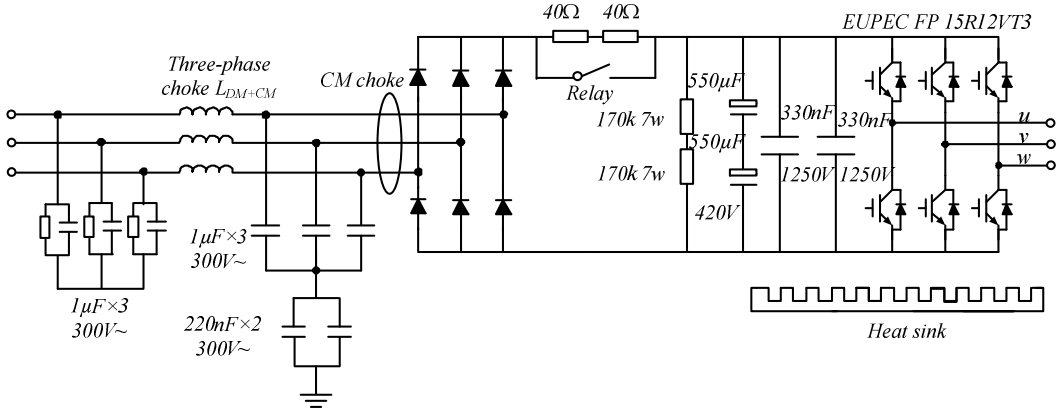


(a)

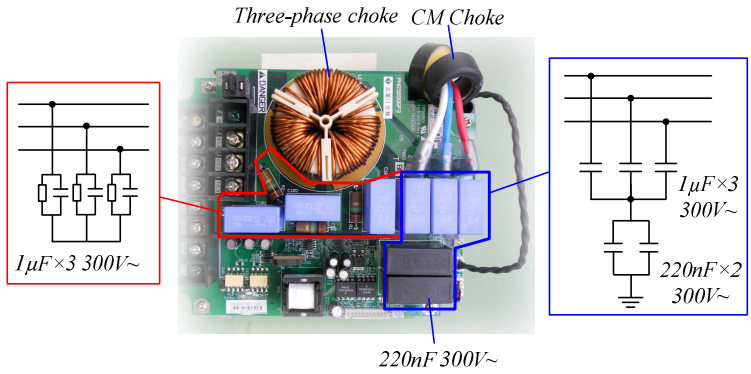


(b)

Fig. 2.19 2.2 kW SEW Movitrac07A commercial motor drive (a) overall schematic diagram (b) AC line EMI filter - C



(a)



(b)

Fig. 2.20 2.2 kW Schneider Electric (Telemecanique Altivar 31ATV31HU22N4) commercial motor drive (a) overall schematic diagram (b) EMI front stage CM filter – LC

In addition to the AC lines, another position where the front stage filter can be inserted is the DC bus, and this is where DM DC-bus filters are mostly installed. However the CM DC bus filters are rarely seen. Because in this way the noise emitted from the rectifier is omitted. Zhao, et al. proposes to use transfer ratio measurements to evaluate and compare the performance between AC line filtering and DC-bus filtering [Zha09]. This shows that with the careful design, the CM DC-bus filter can achieve the same or even better noise suppression than to insert in the AC lines.

Output filter

Compared to the front stage filters, application of output filters can achieve better modulated sine waveforms which results in better EMC performance and moreover increases the motor operation reliability. However relative large values of inductance or resistors must be added to limit and damp the current overshoot and oscillations. The overshoot and oscillations are due to the large dv/dt values appearing at the inverter three output phases. Besides classical output filters, Y. Sozer et al. proposes the filter topology named LC trap to reduce the high frequency harmonics, which eliminates the need to use low cut-off frequency filters, thereby avoiding the use of damping resistors [Soz00].

Output filters suppress the noise in the first propagation place before propagating to the motor. Therefore they present considerable benefits, such as decreasing bearing currents, extending life of insulation, and decreasing stress of motor windings. In the past years, various output filter topologies have been developed to suppress the CM voltages or currents. Akagi is one of the main contributors. For example, an output filter is proposed to cancel the high frequency common-mode and normal-mode voltages as shown in [Aka04a], where the pure line-to-neutral and line-to-line voltages are obtained. A similar approach but with different filter configuration is proposed in [Aka04b], the proposed passive filter requires the motor neutral point to be accessible to utilize the stator windings as a part of the filter. Later, a new filter structure (see Fig. 2.21) is proposed to eliminate both the bearing current and ground leakage current, which are fundamentally the by-product of the motor shaft voltage as the noise source [Aka06].

Other authors, such as Hanigovszki et al. compares the EMC performance of a VSD system in different configurations: without output filter, with a classical LC output filter and with an advanced output filter with DC link feedback [Han06]. The advanced output filter is proposed to reduce EMI to acceptable levels when using unshielded cables instead of shielded cables. Since there is no feed-back control the system can become unstable. The improvement can be done by applying active filters, which will be introduced in the next section. The passive filters mentioned above behave as voltage compensators. The output filters are simultaneously designed as the DM filters to save the volume and cost [Pal02; Ren98; Che07].

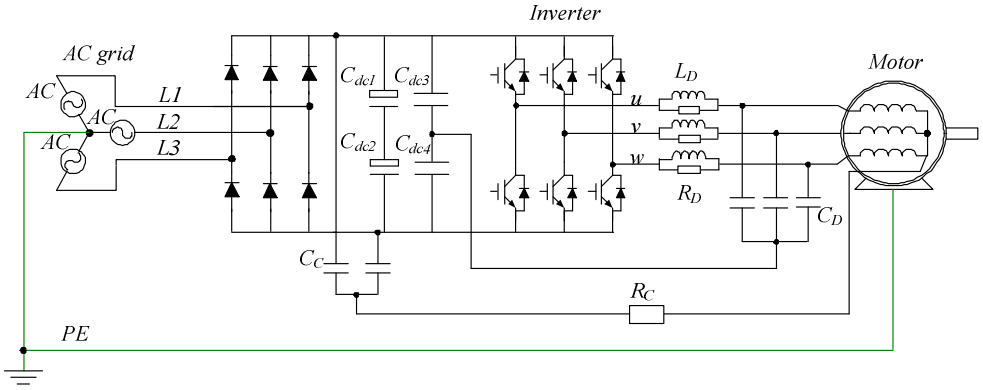


Fig. 2.21 Output passive filter to eliminate bearing current and ground leakage current, as proposed in [Aka06]

2.4.2. Proper low and high frequency grounding

Grounding of the VSD system is divided into two categories, one from the mains side and the other from the VSD system side. The grounding philosophy for process industry applications has historically been based on the concerns of providing safe and reliable power distribution, while insuring maximum protection against transient voltages and maintaining uptime availability during grounding safeties [Nel99]. Significant EMC improvement can be achieved by careful grounding design.

Neutral grounding configurations

There are three neutral grounding configurations of the power input, namely ungrounded, high resistance grounded and solidly grounded as shown in Fig. 2.22 (a), (b) and (c) respectively [Ski99]. Different grounding configurations influence the CM noise magnitude through providing different line-to-ground impedance. With respect to the EMI from VSD systems, the ungrounded configuration beneficially break the CM noise return path to the AC lines connected to the VSD input. Thus the CM noise is substantially reduced. However many disadvantages exist:

- The primary line-to-ground voltages are transferred to the secondary without attenuation.

- The floating potential may overstress the insulation system.

- An arcing ground fault can cause escalation of the system line-to-ground systems to several times higher than that of normal line-to-ground values.

The solidly grounded configuration eliminates the problems that may be encountered in the ungrounded configuration. However since the neutral and the ground have the same potential, a disadvantage is that the line-to-ground fault may inflict a great damage due to the large energy dissipation. The resulting EMI magnitude is the highest among the three grounding configurations.

Due to existence of above advantages, the high resistance grounded configuration is most commonly adopted. The added impedance of R_g greatly increases the fault current capability therefore a line-to-ground fault will not cause immediate shutdown of the affected device, however it may corrupt the sense voltage for the ground fault indicator. From the EMC point of view, the increased resistance decreases the peak value of the CM current.

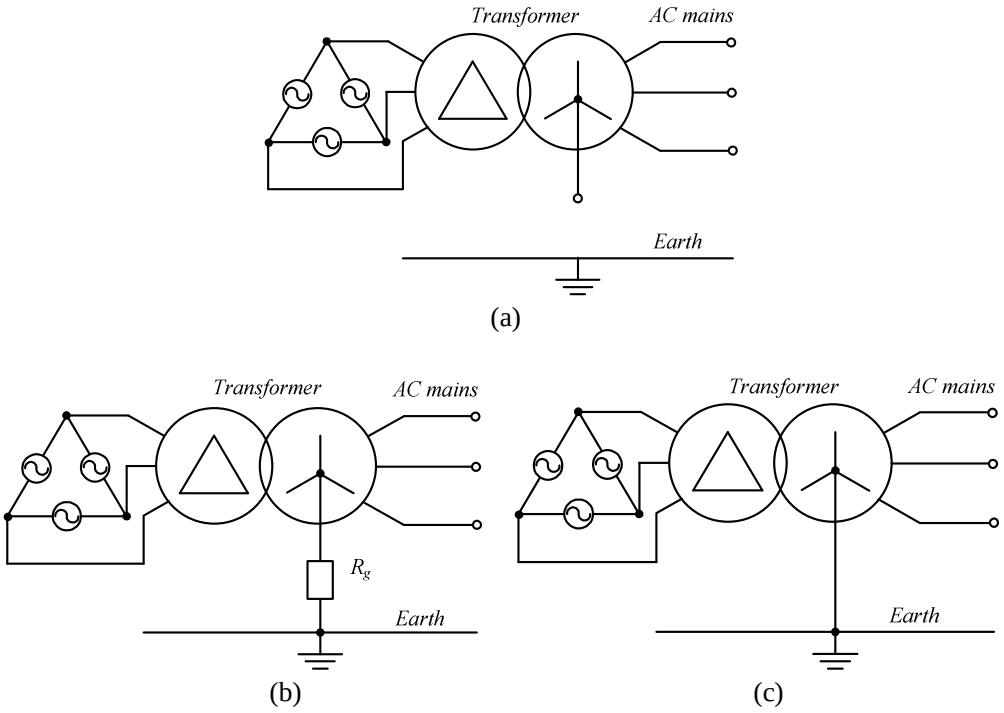


Fig. 2.22 Neural grounding configurations of the power input (a) ungrounded (b) high resistance grounded (c) solidly grounded

Grounding of VSDs

Grounding configurations of the EMI filter and heat sinks are the two aspects that significantly influence the EMC performance of the VSD systems. CM EMI filter performance

is mainly limited by the Equivalent Series Inductance (ESL). The mutual coupling between ESL and its surrounding inductance further degrades the performance. It has been more and more popular to apply cancellation techniques to reduce the filter grounding impedance. Some methods cancel the ESL of filter capacitors by adding external circuits [Pie07; Wan04b; Pie06]. Wang et al. reduces the mutual coupling between two capacitor branches to improve the high frequency filtering performance [Wan08b]. However, their validations are mostly done through small signal measurements from a network analyzer instead of being performed by LISN.

Transistors are usually mounted on top of the heat sinks to achieve the best cooling effect. However, at the meantime parasitic capacitance is created between the switch drain plate and the heat sink, for example, C_{dh} as shown in Fig. 2.23. A TO-220 package drain could result in 40pF parasitic capacitance or more, depending on many parameters, such as the thickness of the thermal pad, switching frequency, current flowing level. During the PWM switching, pulsed voltages (dv/dts) appear at the transistor drain, thus resulting in the pulsed currents flowing through this capacitor, which becomes one important mechanism that propagates EMI.

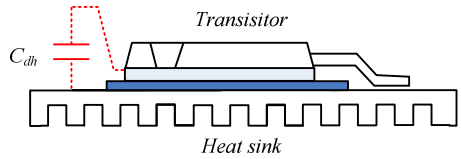


Fig. 2.23 Parasitic capacitance is created due to transistor drain being attached on top of the heat sink

Due to existence of C_{dh}, grounding the heat sink is the worst solution from the EMC perspective. For C_{dh}= 20pF 200V DC bus voltage, and 40ns switching transient will result in a pulsed current of 10^5μA. 12μA of steady-state currents flowing in the LISN fails the FCC class B standard. Fig. 2.24 illustrates the best solution for heat sink referencing, which to a large extent prevents the CM noise propagation by minimizing the current flowing loops. However, the volume of the heat sink is proportional to the converter power rating. Especially for VSDs, bulky heat sinks are inevitably used to achieve enough cooling. Since heat sinks of the VSDs are usually integrated with the enclosure, hard earth grounding is necessary to comply with safety requirements.

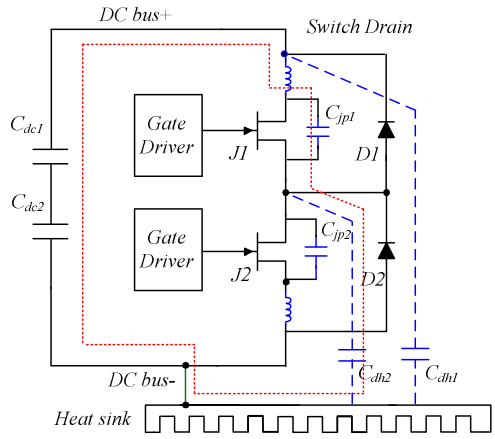


Fig. 2.24 Best solution for heat sink referencing – heat sink is connected to DC bus- to minimize the CM current flowing loop

A compromise way between safety and EMC perspectives can be achieved by "low frequency" referencing the heat sink to the earth, and simultaneously "high frequency" referencing it to the DC- bus, as is shown in Fig. 2.25, where C_{hc} is added to circulate the high frequency noise, and L_{hc} is used to prevent the shock hazard. This configuration keeps the heat sink energy within the safe range, at the same time improves EMC performance.

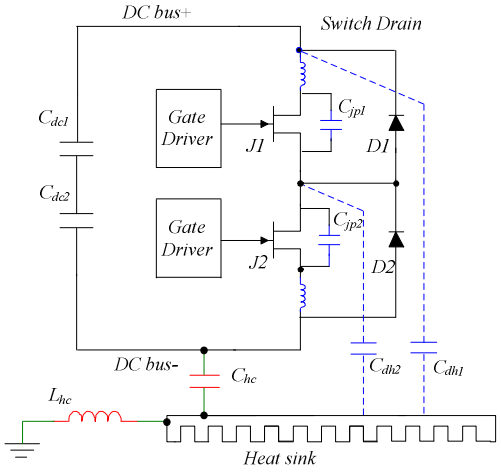


Fig. 2.25 Proper low and high frequency referencing of the heat sink

2.4.3. Other passive suppression methods

The other passive suppression methods are summarized as below:

- Use shielded cables. The emitted noise at the inverter output contains several frequency components. The shielded cables decrease the inductive coupling magnitude both in CM and DM. They trap the CM current and change its path from

flowing through the ground to the shield of the motor line cables. A detailed investigation is presented in [Ski99].

- Use multi-layer PCB at the motor terminals. Muetze proposes a multi-layer PCB structure attached to the motor terminals to reduce EMI [Mue04]. The formed capacitors between the second PCB layer and the power transmission line effectively bypass the micro-surge currents.

- Input filter damping. This method fully exploits the filter attenuation by mitigating unintended interactions between the filter and converter [Lei09]. The resonance valley that exists at the input impedance seen by the inverter source causes great EMC degradation at these frequencies. Therefore damping resistors are required to stabilize the impedance.

- Use twisted wires. Twisting the wires such as VSD input wires and motor cables, greatly reduce the high frequency noise by cancelling the mutual fluxes and minimizing the noise emitting areas. Subsequently, the conducted emission coupled from radiated emission is reduced as well. This method can also be applied in the toriodal inductor and PCB tracks [Ros98].

- Modification of the motor configuration. Instead of solely using AC line filters, Akagi further reduces the EMI level by directing a RC path between the middle point of DC bus and the neutral point of the motor three-phase windings[Aka08]. In this way, the CM currents that are mainly propagated from the motor side are largely circulated back to their sources.

2.5 Review of suppression techniques at the EMI source

2.5.1. Optimization of circuit design

This method aims at optimizing the location of components and the PCB design to achieve better EMC and electrical performance, which decreases EMI without degrading system performance. A basic rule can be accorded is to keep the components' leads as short as possible and to minimize the length of the critical PCB traces. This helps to reduce the voltage and current ringing at the switching transients and to decrease the high frequency noise. It is suggested that sensitive circuits be placed away from the noise sources. However in many cases such an optimum design is not easily achievable because of the cost, manufacturability constraints, etc. [Reo00] evaluates different circuit design and layout solutions for a single phase boost converter. High dv/dt and di/dt PCB track loops are twisted to cancel the magnetic coupling. The inductors are implemented with toroidal cores and wound in a special configuration to reduce the radiated noise.

2.5.2. The fourth-leg active filtering

As discussed previously, the advantage of high performance while small volume makes the active filtering method a hot spot in the research field. In 1999, Julian et al. proposed an active filtering solution which is named the fourth-leg active filter [Jul99]. The idea is to utilize/add the fourth leg of the inverter to compensate for the CM dv/dt transients with the opposite switching. By this means, ideally the CM step-wise voltages can be cancelled in one step. When there is no zero state, the CM voltage can be fully compensated to zero. Fig. 2.26 illustrates the schematics of the fourth-leg active filter applied in the VSD system. An extra winding is added between the output node of the inverter fourth leg and the middle point of the DC bus. The winding together with the output inductor composes the coupled transformer to compensate for the generated CM voltages.

The proposed CM voltage waveforms of the fourth inverter leg and the time sequence corresponding to the other three legs are illustrated in Fig. 2.27, where V_u, V_V, and V_W are the voltages between the inverter output nodes (u, v, w are considered as one node) and the earth, + represents when the upper switch is turned on, and – represents when the lower switch is turned on, V_{CM} is the CM voltage after compensation. The scheme is summarized as follows:

1. When one of the switches is turned on, turn on the switch in the fourth leg to produce the opposite polarity voltage to the PWM inverter voltage synchronously.

2. Reset the voltage in the fourth leg with a slow slope if the next transient of the other three inverter legs is in the same direction.

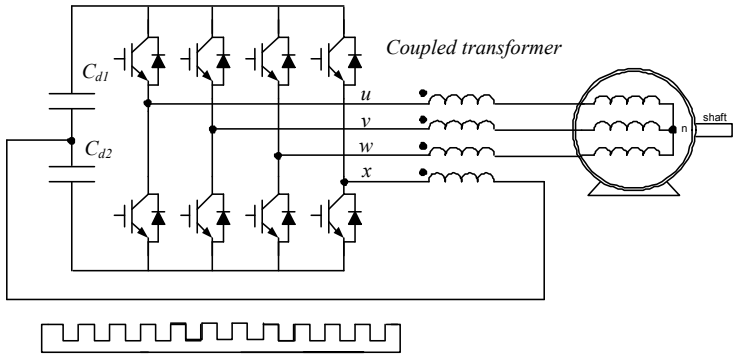


Fig. 2.26 Schematic diagram of the fourth-leg active filter

As time pass by, numerous methods have been developed in an attempt to make this method easy and practical to be applied. [Son06] analyzes the mechanism and presents a systematical review on the various active filtering approaches. S. Ogasawara et al. developed an active EMI filter that bypasses the zero-sequence current from the ground wire to reduce the ground leakage current [Oga98]. Based on this work, two different configurations are developed in [Oga00]. The approaches are based on the complementary push-pull transistors that rely on the passive control feed forwarded by the voltage detection points from the decoupled capacitors. Therefore the control variability is still limited. In [Zha08] an enhanced control scheme for the fourth-leg switches is proposed. The driver function is separated into logic control and slope

control. The logic control is used to generate the fixed dv/dt slopes to compensate the switching transitions at the inverter output legs, and the slope control is used to reset the fourth inverter leg for next transient compensation.

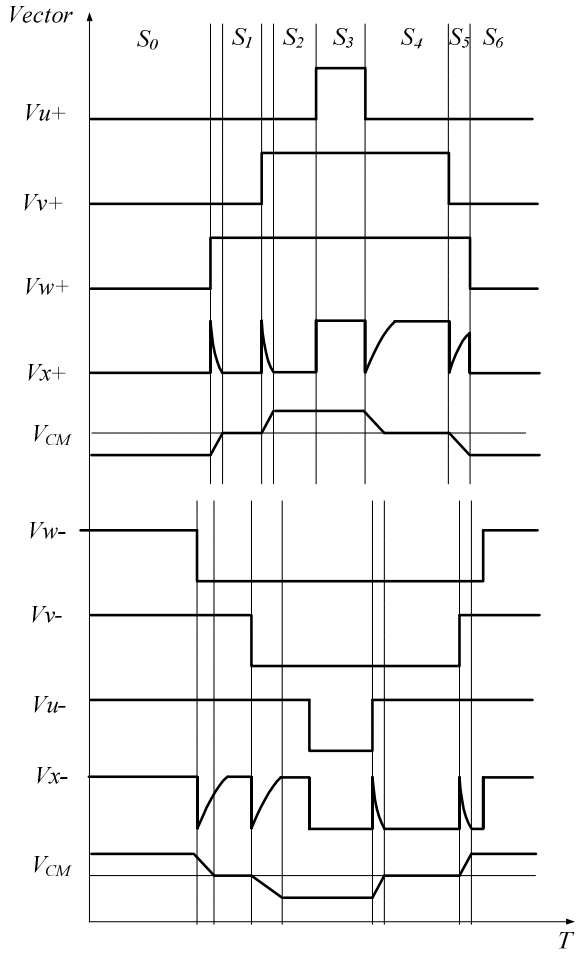


Fig. 2.27 CM Voltage waveforms of inverter output and the fourth-leg filter

2.5.3. Active gate control

Active gate control mainly deals with the switching performance under hard switching conditions. It combines the requirements between the slow switching voltage edges for lower emitted noise and the fast switching of linear regions for lower switching losses. V. John et al. develops a three-stage active gate driver which reduces the di/dt and the tail voltage at the turn-on transient and controls overvoltage at the turn-off transient [Joh99]. S. Park et al. introduces another driver which works on the principle of utilizing the effective miller capacitance between the switch gate and the source to adjust the slope electronically [Par01]. Another method is to change the gate-driving signal into sinusoidal from the conventional trapezoidal

wave shapes. If this is done the transistor doesn't lose the switching speed, while at the same time high frequency harmonics are decreased [Hol04].

2.5.4. Modification of PWM strategy

The conventional PMW strategy with the constant switching sequence results in the up boundary spectrum of the EMI noise, because the harmonics at the carrier frequency multiples are maximized. Modification of the PWM strategy decreases EMI by spreading the energy of harmonics concentrated around the switched frequency into other frequencies. D. Jiang et al. applies the random PWM scheme into a Vienna-type rectifier [Jia11]. The carrier frequency is changed randomly in the range between 55 kHz and 70 kHz. The noise in middle frequency range (1 MHz ~ 10 MHz) is reduced. H. Chung-Chuan, et al. compares the performance of three PWM schemes, named discontinuous PWM (DPWM), active zero state PWM (AZS-PWM), and near state PWM (NSPWM) [Chu10]. The goal is to reduce the CM current and the fault current. Rather than applying complicated computations, it is found in [Lee00] that a displacement of the three-phase carrier waveforms also helps to reduce EMI. The main drawback is that DM voltage distortion is increased.

2.5.5. Snubber circuit at the source

Proper design of sunbber circuit is very effective to reduce EMI while without losing efficiency. A slower voltage rising at switching transitions decreases high frequency noise. A proper compromise between the two slopes between turn-on and turn-off will maintain efficiency.

Fig. 2.28 illustrates a typical snubber circuit that is applied surround one switch. C_{jp} is the intrinsic parasitic capacitor of J_1. At turn-on transition, the slope of V_{ds} is determined by two factors:

1. Discharging speed of C_{jp}.

2. The time constant multiplied by R_s and C_s.

At turn-off transition, the current in the path is divided by three branches: switch J_1, capacitor C_{jp}, and snubber capacitor C_s. As C_s is much larger than C_{jp}, more current is divided into this branch, which decreases the current flowing into the switch and thereby decreases the switching losses. The added diode D_s accelerates the charging speed of C_s.

Some research employ high ESR capacitors to damp the overshoot and oscillations. Because there is no resistor, high power dissipation is avoided. The constrain of this method is the voltage rating of the capacitors [Zei11].

In comparison with using RC snubber, soft switching is another effective way to keep EMI low while maintain high efficiency for the system. However the peak values of the resonant current must be controlled under acceptable levels [Chu96].

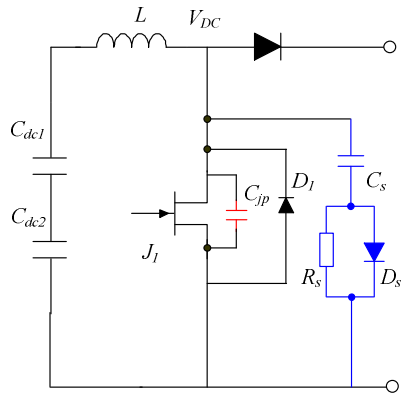


Fig. 2.28 Schematic diagram of a snubber circuit

2.5.6. Other methods

Some other active suppression methods at the source are summarized as below:

- Shift the input filter resonance away from the critical frequency range. This method optimizes the filter performance by shifting the filter impedance valley into an unproblematic frequency range. Instead of using damping resistors, the method utilizes the frequency dependent nature of the converter source impedance as to generate a virtual active damping effect [Sch10].

- Optimization of applied components. Device characteristics such as core material of the inductor, semiconductor package, equivalent output capacitance, reverse recovery characteristic of the diode, equivalent series inductance of the Y-capacitor, etc. have the influence on EMC performance. Enhancement of this aspect helps to reduce high frequency noise.

- Increase the gate resistance. This method slow down the switching speed of semiconductors and in return decreases the dv/dt and di/dt slopes. However the quasi-linear parts of the slopes may receive little influence and the switching losses could subsequently be increased.

- Interleave of the multi-inverter outputs. This method deals with the converters in parallel operation. The aim is to shift or cancel the switching harmonics to the same frequency as that is generated from each converter branch. Referring to the traditional symmetric interleaving methods, In [Lei10b] an asymmetric interleaving method based on the impedance frequency characteristic of the motor is proposed.

2.6 Conclusion

Selection of the particular EMI mitigation method depends on the various requirements on the system such as performance, size, cost, and topology. EMC design is not only minded to

not disturb surrounding systems but also mainly the reliability of the target system. Normally, different noise suppression techniques have to be applied simultaneously to comply with the specific standard. For example, for a systematic EMC design, the PCB layout needs to be optimized for less noise emission and enhanced electrical reliability, the gate driver has to be optimized to minimize the potential ringing reflected on the gate, a compromise needs to be reached in the snubber circuit between the switching losses and parasitic oscillations, proper grounding point has to be selected, and the appropriate filter topology and components have to be designed.

In this chapter, those mitigation methods for VSD systems are reviewed and classified into two groups namely suppression along the noise propagation path and suppression at the noise source respectively. Usually suppression of the noise source is more effective. Especially those active CM source cancellers such as the fourth-leg active filter can achieve a great noise attenuation level whereas in a much smaller volume than using passive filters. However at present those techniques are still not practical enough, where the circuit reliability, filtering frequency band, and very restricted timing sequence are the main constraints. More efforts and developments are needed.

In industries, the passive filters are still undeniably the first choice for VSDs at present, and C and LC filters are used most frequently. Even within many advanced suppression methods, the employing of bulky passive filtering components is still inevitable due to their many favorable features such as low cost, high efficiency, and easy to implement. Suppressing noise at its source is the most effective way comparing to the other two methods. However this approach is much more complicated and can be very costly.

Chapter 3

System Equivalent Circuit Modeling

3.1 Introduction

In this chapter, an equivalent circuit modeling method for the analysis of the EMC performance of VSD systems is introduced. Elements extraction of the model is based on curve-fitting of the impedance-frequency characteristics measured on the leads of individual components and different portions of the system. An impedance analyzer is taken as the measurement tool. Various sub-circuits of the system are modeled as equivalent circuits composed of detailed RCL components in order to capture the emitted high frequency EMC performance. For verification the calculated results are compared with the measured impedances over the conducted emission frequency range, portion by portion.

Because it is straight forward and easy to follow, equivalent circuit modeling is widely used to predict EMI spectrum and filter insertion losses [Zhu99; Has10; Kye04]. However, constraints and limitations also exist. Firstly, it is not easy to measure the parasitics when their values are relatively small and coupled with other circuit elements. The influences from the adjacent parasitics are very difficult to identify. Secondly, large errors may exist due to researchers being unaware of the poor calibration of the measurement setup. Thirdly, the accuracy of the equivalent circuit models is compromised because of the simplifications involved. It is also inherently difficult to develop a model that is accurate for the entire frequency range and under various operating conditions.

In this chapter, a CM EMI equivalent circuit modeling procedure for the VSD system is presented. The modeling target is illustrated in Fig. 3.1. It includes a LISN, an uncontrollable rectifier, an inverter, power cables and an electrical machine. The procedure is based on curve fitting of measured the impedance-frequency characteristics. Inverter hardware disassembly is involved to separate the inverter into different portions. Firstly, the study target are separated into different parts and modeled accordingly. Those parts include: LISN circuit, power cables, three phase electrical machine and the three-phase PWM inverter. Secondly, A 2.2 kW commercial motor drive (SEW Movitrac 07A) is employed to generate PWM signal. To derive the values of elements that can not be measured directly, open- and short- circuit measurements are used. Lastly, large signal measurements that based on current transfer ratio measurement are used to verify the model.

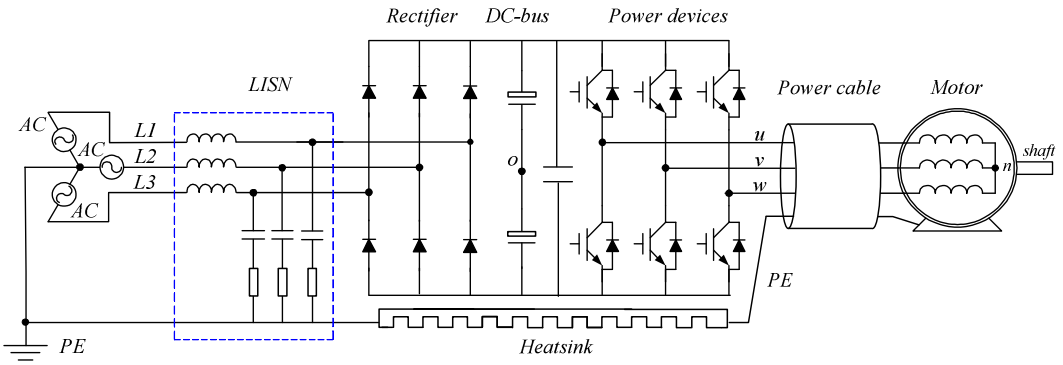


Fig. 3.1 The basic topology of a VSD system for equivalent circuit modeling

3.2 Modeling of Conducted Emission Environment

As shown in Fig. 3.1, the conducted emission environment of the VSD system includes the power cable, motor, Protected Earth (PE), LISN, AC lines, rectifier, and DC-bus. Equivalent circuit models for these elements are proposed and discussed respectively in the following sections.

3.2.1 LISN

A Line Impedance Stabilizing Network (LISN), also known as Artificial Mains Network (AMN) is specified for most of the conducted emission measurements. It aims to provide constant line impedance (50Ω) as seen by the equipment under test. Additionally, the LISN also blocks the noise from the mains side to ensure the measurement accuracy, while acting as a bidirectional filter. It is built for various applications with different current ratings and has single- and three-phase versions.

The schematics of a typical three-phase, single stage LISN that suits VSD system is depicted in Fig. 3.2, in which three signal flowing paths are provided by four groups of components: L_1, C_1, C_2 , and the 50Ω impedance. The low frequency components are passed through the inductors L_1 from the equipment under test (EUT) to the power grid. Additionally it also allows the AC power from the grid to feed into the EUT. The high frequency contents emitted from the EUT will be by-passed from the grid and coupled to the 50Ω impedance through the capacitors C_2. One of the 50Ω impedance is provided by connecting the test receiver (usually a spectrum analyzer) to the LISN output termination. As a consequence, the emitted noise coupled into the corresponding phase is measured. The other 50Ω resistors are terminated internally. The capacitors C_1 together with the inductors L_1 filter the high frequency emissions from the grid, preventing them from influencing the measurements.

The key components of the LISN are the three 50Ω impedances that should be approximately constant seen by the EUT over the conducted EMI frequency range. Fig. 3.2 illustrates the most widely used configuration specified in the CISPR 16 standard. In Fig. 3.3, the measured and calculated CM impedance-frequency characteristics of a LISN (Cranage VN3-100S) are compared. The schematics shown in Fig. 3.2 is used as the model. It can be seen that two curves from 150 kHz to 6 MHz agree well. The components of L_1, C_1 and C_2

affect the fitted characteristics in the low frequency range up to 60 kHz. Deviation in the high frequency range is due to the non-ideal component characteristic of the LISN and the reflection effects from the externally added cables for measurement. Therefore before EMC tests, the calibrations to LISN at high frequencies is usually needed. As the result, in simplified cases, the model of Fig. 3.2 (a) show adequate accuracy and can be used to determine the conducted emission characteristics. For further simplifications, the LISN plus test receiver connected to one phase is simply modeled as a series connection of a 0.1μF capacitor and a 50Ω resistor as illustrated in Fig. 3.2 (b).

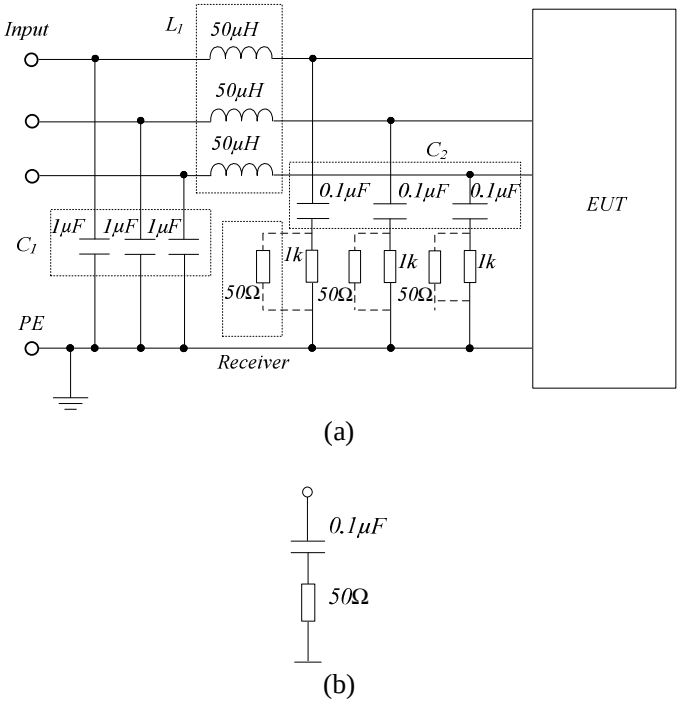


Fig. 3.2 Schematic of a typical three-phase LISN that is positioned between the mains and equipment under test. (a) full model (b) simplified model

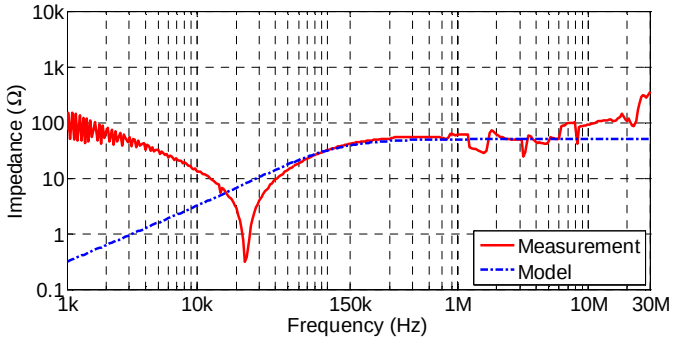


Fig. 3.3 Comparison of LISN impedance seen by one phase of the EUT between measurement and calculation using the model of Fig. 3.2 (b)

3.2.2 Power Cables

In a standard VSD system, both of the LISN and electrical machine are typically connected to the inverter through the three-phase power cables. The input cables that connect the VSD system to the power grid, usually contain five conductors, three for the input phases, one is the neutral line from the remote transformer station and the other one is connected to the protective earth. Some power converters utilize the input cables as part of the filter. However because of the relatively limited influence compared to the input filters, the input cables are generally neglected during the filter design and are regarded as a margin. In the equivalent circuit models they are usually represented by an increased inductance. Their parasitic capacitance is usually neglected since the parasitic capacitance is much lower than that of a CM filter. However, due to the abrupt voltage and currents changes (dv/dts and di/dts) at the inverter output phases, the output cables that connect the inverter to its load (resistors, electric machines, converters, etc.) have a strong influence on the high frequency conducted emission levels [Pig03; Han06]. Therefore they are an important aspect of an accurate high frequency modeling procedure.

The output cable has no neutral line. Typically, there are two types of output cables used for PWM inverter-fed motor system. They are named shielded and unshielded cables depending on if a shielding layer covering the other conductors is included. The main objective of the shielding layer is to prevent high frequency noise emissions that may strongly deteriorate the EMC high frequency performance and signal integrity. An explanation on this phenomenon is illustrated in Fig. 3.4, where the numerous stray capacitors are distributed along with the cable. The capacitance is proportional to the cable length while inversely proportional to the distance between the contact areas of any two other conductors. According to the PWM switching scheme, pulsed voltages appear at the inverter output phases. As a result, the existed capacitors deteriorate the DM performance. In addition, they also couple CM noise (i_{CM}) to the earth, which deteriorates the CM performance, as shown in the Fig. 3.4. The current magnitude is highly dependent on the cable characteristics such as length, impedance, and construction, etc.

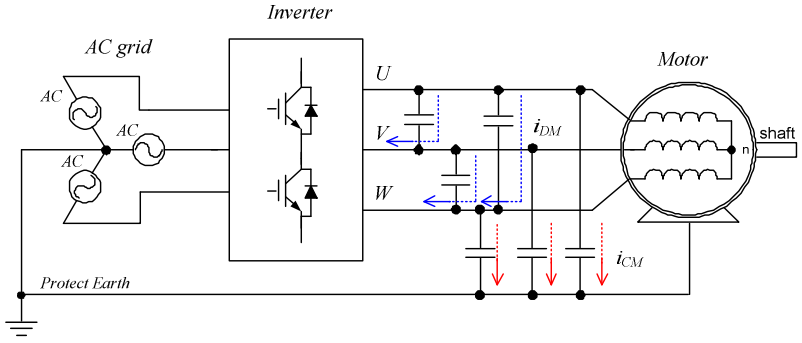


Fig. 3.4 DM and CM current coupling

Although the above mentioned benefits are obtained from the shielded cables, unshielded cables are still most commonly adopted as the solution by industries and companies. Because the shielded cables are so expensive that their use significantly increases the overall installation cost.

The cross section of a typical unshielded cable that includes four conductors (three phase conductors and one *PE* conductor) is shown in Fig. 3.5. For the lab testing scale it is usually rated for 450V and with 2.5 mm^2 of copper area per core. Elements of its model are obtained by referring to open-circuit and short-circuit measurements. Both CM and DM impedance-frequency characteristics are taken into consideration. Fig. 3.6 (a) and (b) illustrate the experiment setup for measuring the cable CM and DM characteristics under the open-circuit condition. The measurements are performed by the Agilent 4294A impedance analyzer.

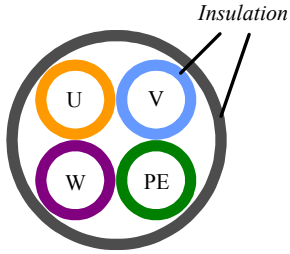


Fig. 3.5 Cross section of an unshielded cable

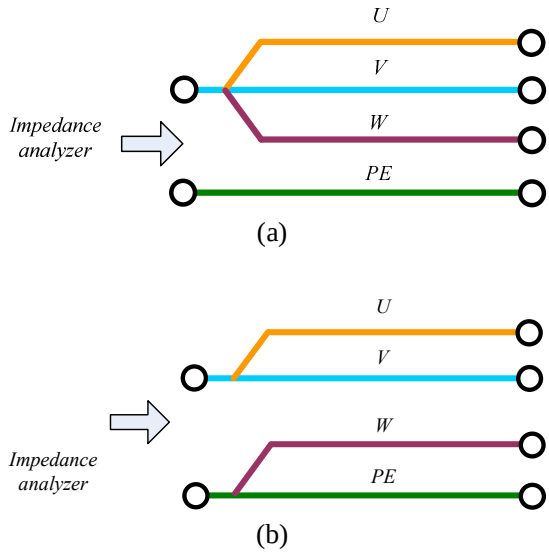


Fig. 3.6 Experiment setup for measuring the cable CM and DM characteristics under the open-circuit condition (a) CM (b) DM

Based on the configuration of Fig. 3.6 (a) and (b), a lossless transmission line model with the single-cell parameters is presented as shown in Fig. 3.7 (a) and (b) respectively, where R is the lumped resistance of each conductor, L is the lumped inductance of each conductor, C_1 and R_1 are the lumped capacitance and resistance between the summed three-phase conductors and the *PE* conductor respectively, C_2 and R_2 are the lumped capacitance and resistance between the summed conductors of each two phase conductors respectively (phase *U* and phase *V* as one, phase *W* and phase *PE* as the other one). It is assumed that the parameters of different

conductors are equal. Configuration of performing the short- and open-circuit measurements is realized by switching the switch *K*.

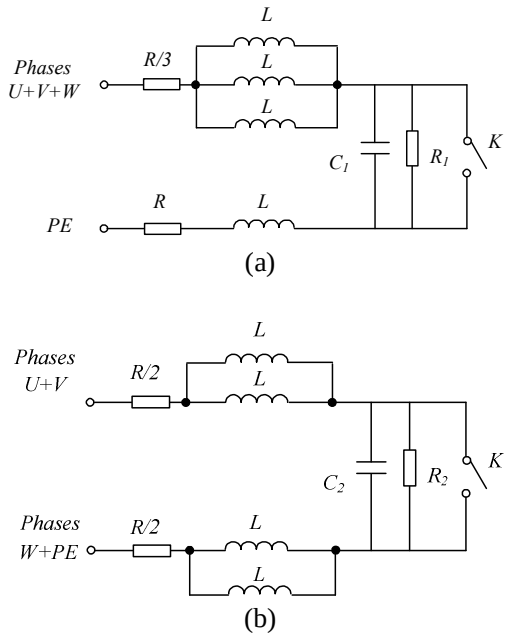


Fig. 3.7 The single-cell model of the unshielded cable (a) for CM (b) for DM

The established single-cell model of an unshielded cable is shown in Fig. 3.8. The parameters are extracted through the measured CM impedance-frequency characteristics as shown in Fig. 3.9, where Fig. 3.9 (a) shows the measured characteristic in open circuit condition (when *K* shown in Fig. 3.7 (a) is switched off). Fig. 3.9 (b) shows the measured characteristic in short circuit condition (when *K* shown in Fig. 3.7 (a) is switched on). To calculate the parameters, several characteristic points are specified from the measured characteristics, as shown in Fig. 3.9 (a). Since the model is predominantly capacitive when the cable termination is open, the capacitance of C_1 is derived from the slope of k_1. The lumped resistance of each conductor is derived from the minimum impedance as shown in Fig. 3.9 (b). (Z_2). The inductance and capacitance create the resonant frequency of f_1. In equations they are expressed by:

$$\begin{cases} k_1 = \dfrac{1}{2\pi \cdot x_1 x_2 C_1} \\ Z_2 = P \cdot R \\ f_1 = \dfrac{1}{2\pi \cdot \sqrt{(\dfrac{L}{3} + L) \cdot C_1}} \end{cases} \tag{3.1}$$

where x_1 and x_2 are the two selected frequencies for calculating the slope k_1, as shown in Fig. 3.9 (a). The value of P is calculated as 0.75 in order to Z_2.

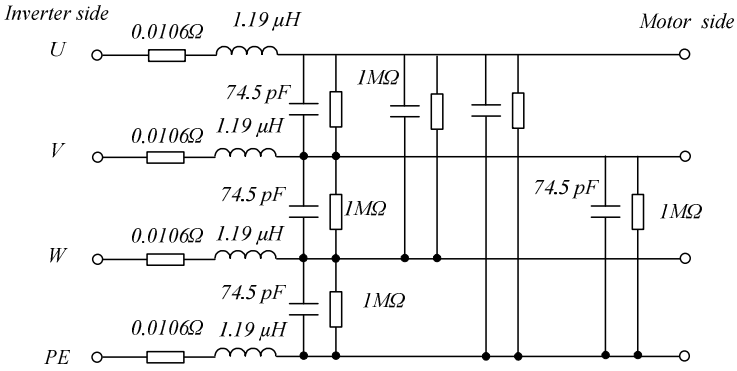
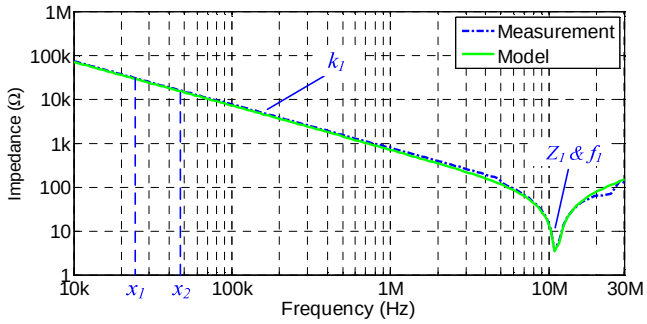
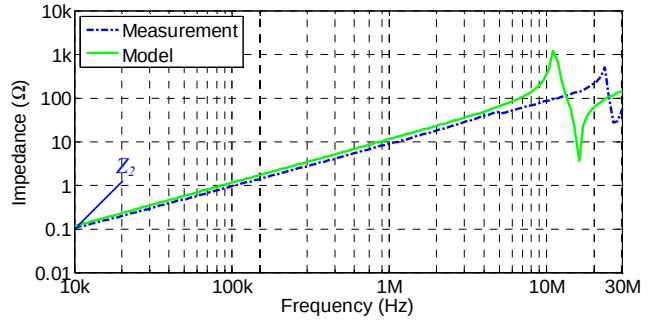


Fig. 3.8 The single-cell model of the unshielded power cable with extracted parameters



(a)



(b)

Fig. 3.9 Comparison of the measured and calculated cable CM impedance from a single-cell model (a) open-circuit (b) short-circuit

When comparing the measurement with calculated results shown in Fig. 3.9, good accuracy up to 20 MHz is observed in the open-circuit condition. Whereas in short-circuit condition a

relatively large difference exists. To increase the modeling accuracy at higher frequencies, a more complex model including proximity and skin effects as well as dielectric losses, will be used. A practical and convenient way to achieve this is to implement multi-stages that divide the cable into finite lengths. This approach can be applied as long as each stage of the cable length is much smaller than the minimum wavelength of the conveyed signal.
The double-cell model that is derived from the single-cell version is illustrated in

Fig. 3.10, where the provided impedance is equivalent as provided by the single-cell model. Comparisons of the measured and calculated CM impedance-frequency characteristic in open- and short-circuit conditions are illustrated in Fig. 3.11 (a) and (b) respectively. When comparing the results with those obtained by the single-cell model (given in Fig. 3.9), it can be seen that the accuracy in the short-circuit condition is significantly improved. This modeling accuracy is sufficient for most of the conducted emission studies.

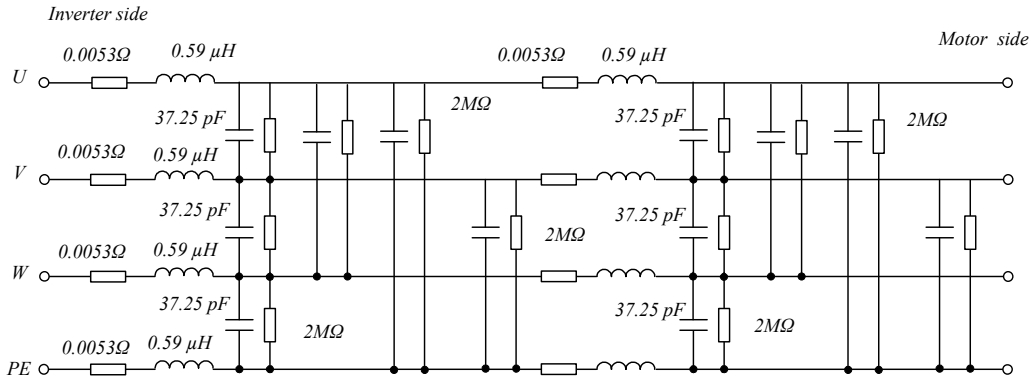
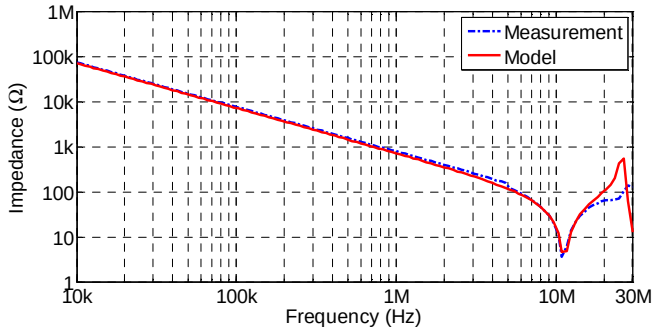
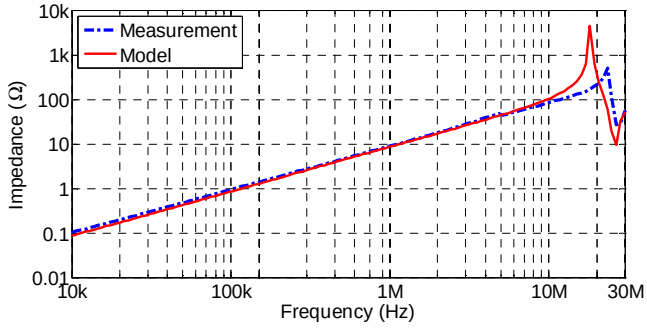


Fig. 3.10 The double-cell model of the unshielded model with extracted parameters



(a)



(b)

Fig. 3.11 Comparison of the measured and calculated CM impedance from double-cell model of the cable (a) open-circuit (b) short-circuit

In simplified cases, the cable can be simplified as an inductor in the series direction and a capacitor connected to the center of inductor in the parallel direction, as illustrated in Fig. 3.12. For further simplifications, an inductor is used.

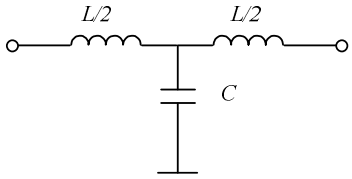


Fig. 3.12 Simplified model of the power cable

3.2.3 Electric Machine

Accurate modeling of electric machines that are driven by inverters is important in investigating the drive overvoltage and EMI predictions [Mor02; Web04; Sch06;]. The majority of the noise inside the system is emitted from the motor side as the load. The equivalent circuit model of the machine is obtained through the lumped three-phase impedance characteristics. The modeling method uses the similar measurement and parameterization procedure as those used for the power cables.

The experiment setup for measuring the motor CM and DM impedance is shown in Fig. 3.13 (a) and (b) respectively. The motor under investigation is a 4 - pole, wye - connected, 2.2 kW asynchronous motor. However, based on the Y-Δ transformation, the model validity is independent of the actual physical connection of the stator windings. In other words, it does not matter whether the actual motor is wye or delta connected, overall the circuit model can be obtained assuming a wye connection of three single-phase circuits. Such an assumption is broadly used in high frequency models of the machine, because it has the advantage of simpler model structure and the associated parameters can be identified more easily.

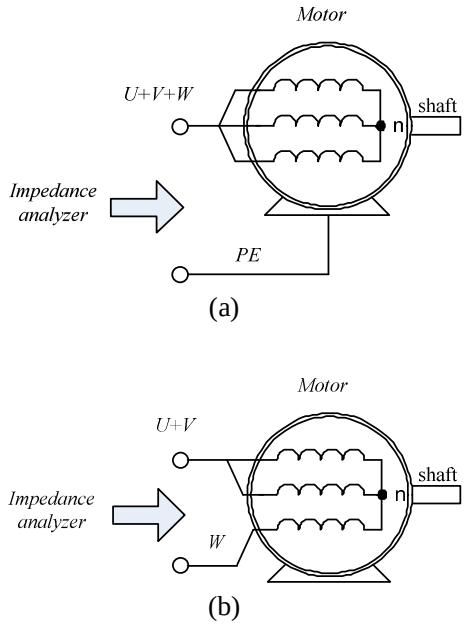


Fig. 3.13 Experiment setup for identifying the CM and DM impedance-frequency characteristic of a three-phase inductor motor. (a) CM (b) DM

The proposed equivalent circuit model that represents one single phase of the motor is illustrated in Fig. 3.14, where the associated physical meaning and significance is interpreted as follows: R_{wg} and C_{wg} represent the parasitic resistance and capacitance between the motor winding and the motor frame; R_{ng} and C_{ng} represent the parasitic resistance and capacitance between the stator neutral and the motor frame; L_e represents the stator winding DM leakage inductance; L_t represents the high frequency skin effect of the windings; C_t represents the stator winding stray capacitance; R_t represents the iron loss of the stator.

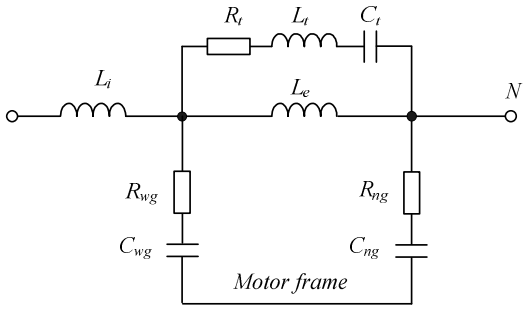


Fig. 3.14 Equivalent circuit model for one-phase of the motor

Based on the single-phase circuit model, the CM and DM equivalent circuit models of the full motor are shown in Fig. 3.15 (a) and (b) respectively. The calculated impedance-frequency characteristics are based on the experiment setup shown in Fig. 3.13. The CM model is built by connecting all three phases in parallel, as shown in Fig. 3.13 (a). The DM model is built by connecting two of the phases in parallel to the remaining phase, as shown in Fig. 3.13 (b).

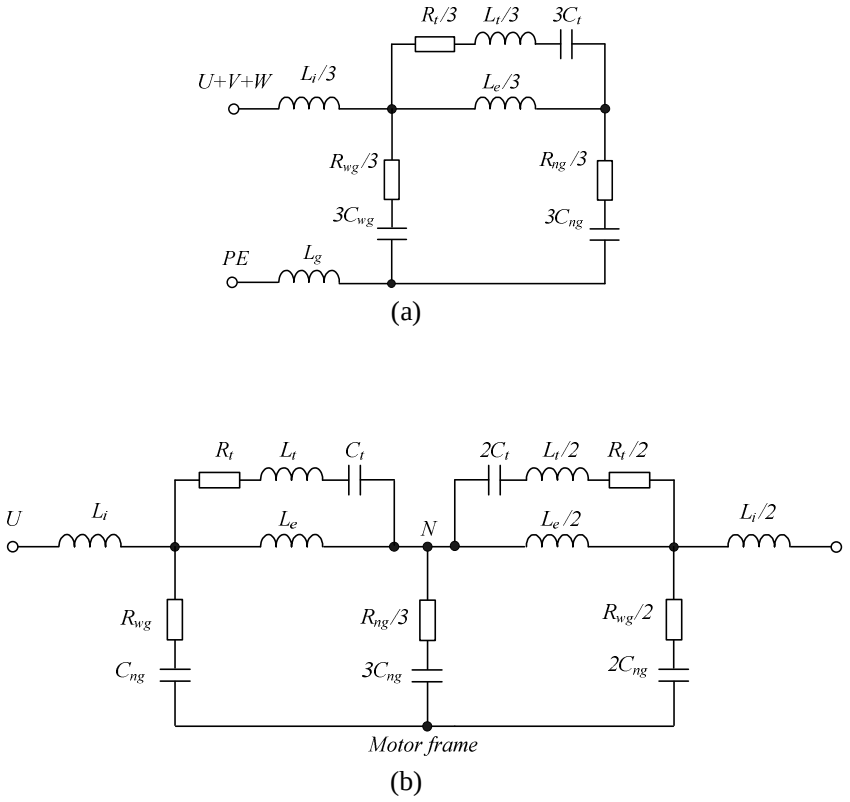


Fig. 3.15 Combined CM and DM equivalent circuit model of the motor based on the one-phase model (a) CM (b) DM

To extract the parameters, several characteristic extraction points are specified from the measured impedance-frequency characteristics as shown in Fig. 3.16, where both of the CM and DM characteristics are used. In the CM characteristic, the total CM capacitance ($3C_{ng}$ + $3C_{wg}$) is derived from the low frequency slope k_1. The capacitance in the circuit branch with fewer components ($3C_{wg}$) determines the high frequency slope k_2. The lumped CM inductance and the capacitance in the circuit loop with more components ($3C_{ng}$) determine the frequency and magnitude of first zero point Z_1. The summed inductance in the loop (L_i + L_g) and capacitance C_{wg} determine the frequency of high frequency zero point Z_2. In the DM characteristic, the total DM inductance is calculated from the low frequency slope k_3. L_t and C_t determine the resonance frequency of the first zero point Z_2. In equations they are expressed by:

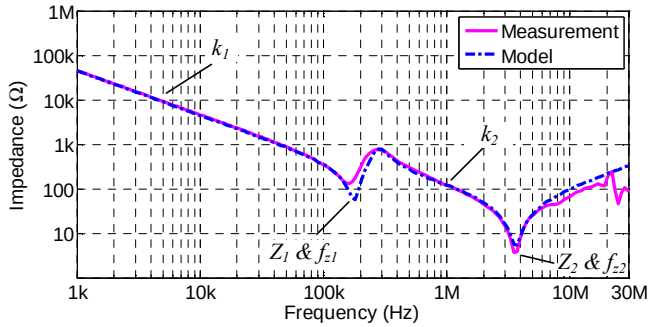
$$\begin{cases} k_2 = \dfrac{3}{2\pi \cdot x_1 \cdot x_2 \cdot C_{wg}} \\ k_1 = \dfrac{3}{2\pi \cdot x_3 \cdot x_4 \cdot (C_{wg} + C_{ng})} \\ f_{Z1} = \dfrac{1}{2\pi \cdot \sqrt{3 \cdot L_{CM} \cdot C_{ng}}} \\ R_{ng} = \dfrac{Z_1}{30} \\ R_{wg} = \dfrac{Z_4}{10} \\ L_{DM} = \dfrac{k_3}{2\pi} \\ L_e = L_{CM} + \dfrac{2 \cdot L_{DM}}{9} \\ C_t = \dfrac{C_{wg} + C_{ng}}{6} \\ f_{Z3} = \dfrac{1}{2\pi\sqrt{C_t \cdot L_t}} \\ R_t = Z_3 \cdot \cos(\theta_{Z3}) \\ f_{Z4} = \dfrac{1}{2\pi\sqrt{C_{wg} \cdot (L_i/3 + L_g)}} \\ L_g = L_i \end{cases} \tag{3.2}$$

where x_1 and x_2 are the two selected frequencies for calculating the slope k_2, and x_3 and x_4 are the two selected frequencies for calculating the slope k_1. θ_{Z3} is the phase angle of point Z_3.

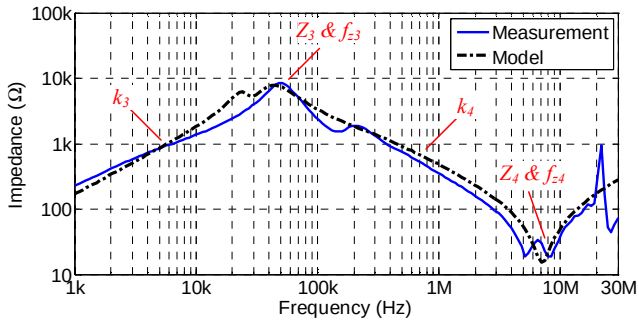
The calculated elements of the target model are summarized in Table 3.1. Based on these values and the schematics as shown in Fig. 3.15 the calculated results are compared to the measurements, as shown in Fig. 3.16. It can be seen that both of the fitted DM and CM characteristics agree well, which validates the model accuracy in conducted emission analysis.

Table 3.1 Extracted values of the parameters in the model

Description	Value
L_i	$0.39\mu H$
R_{wg}	1.884Ω
C_{wg}	$0.35nF$
L_e	0.774mH
R_t	$1.18k\Omega$
L_t	$0.09\mu H$
C_t	$0.2nF$
R_{ng}	6.67Ω
C_{ng}	$0.83nF$
L_g	$0.39\mu H$



(a)



(b)

Fig. 3.16 Comparison of the measured and calculated impedance-frequency characteristics (a) CM (b) DM

In conducted emission analysis, equivalent circuit modeling is widely used because they have the clear meaning and significance. The CM equivalent circuit model of motor is usually used to analyze and predict EMI levels, while the DM equivalent circuit model is usually used for overvoltage studies.

3.3 VSD system equivalent circuit modeling

Traditionally, identification of parasitic elements is difficult because their values are hard to measure directly and may be physically inaccessible inside the converter integral package. As a result, many approaches were developed to solve this problem. For example, some software tools have been introduced for calculating the parameters [Zhu99]. This requires detailed geometric data and material properties for generating the accurate results. In [Yan07] a small inductor is added in parallel to the target stray capacitors for extraction. The parasitic high frequency behavior can be influenced in this way.

In this section, the modeling method is applied to a VSD system where a commercial industrial drive (SEW Movitrac 07A 2.2 kW) is employed as the inverter. The schematic diagram of the system is shown in Fig. 3.17. The inverter is connected to the grid through a four-line LISN. The EMI filter consists of four CM capacitors at the inverter input side, a combined CM and DM choke at the DC-bus, and two Y capacitors connected the DC- bus to the earth line. All the semiconductors (Rectifier, IGBT switches) are integrated into the power module (SKiiP 20NAB12 SEMIKRON).

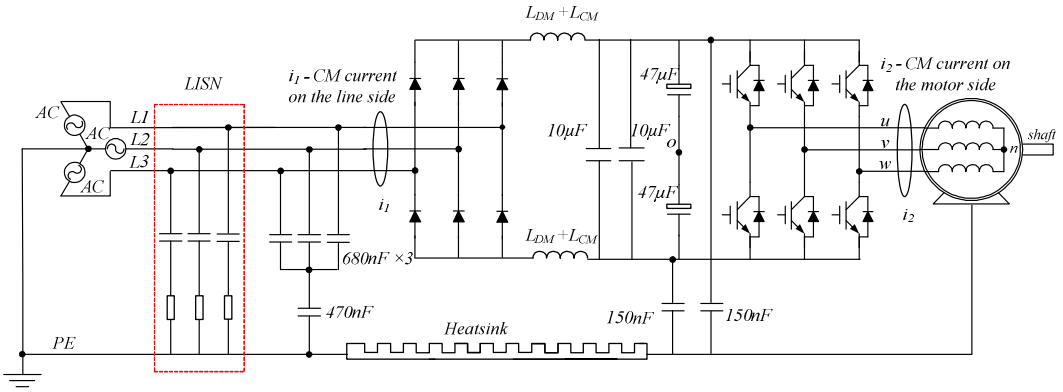


Fig. 3.17 Circuit diagram of the investigated VSD system

The established CM equivalent circuit model of the drive system is shown in Fig. 3.18, where the following reasonable assumptions are applied:

- The parameters in the three input and output phases of the inverter are the same.
- The CM noise sources representing fast switching transients that occur between the output of inverter legs and the earth are treated as three superimposed identical CM voltage sources and merged into one noise source V_{inv}.
- The parameters in the DC+ bus and DC- bus are the same.

The CM currents flow through the motor, along the PE line, LISN, AC lines and back to the source. Two CM current measuring points, on the input line side (i_{CM1}) and the motor side (i_{CM2}) are also depicted. They are used to calculate the transfer ratio as verification under large signal

conditions, which will be introduced in the last part of this section. As shown in the circuit diagram, the CM current loop is formed by connecting the motor *PE* line and the earth to the heat sink.

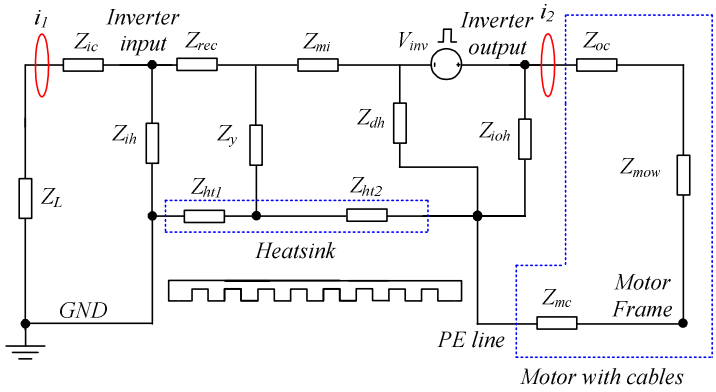


Fig. 3.18 CM equivalent circuit model of the investigated VSD system

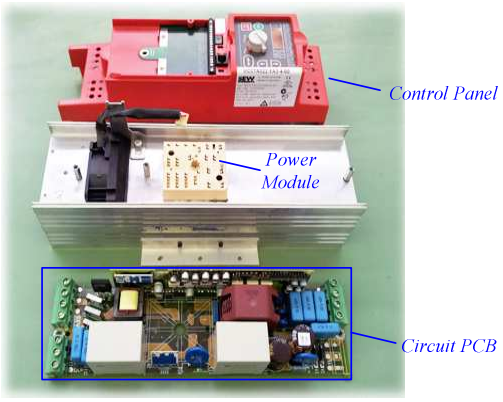
Abbreviations and explanations of model elements are listed in table 3.2.

Table 3.2 Abbreviations and explanations of parameters in the model

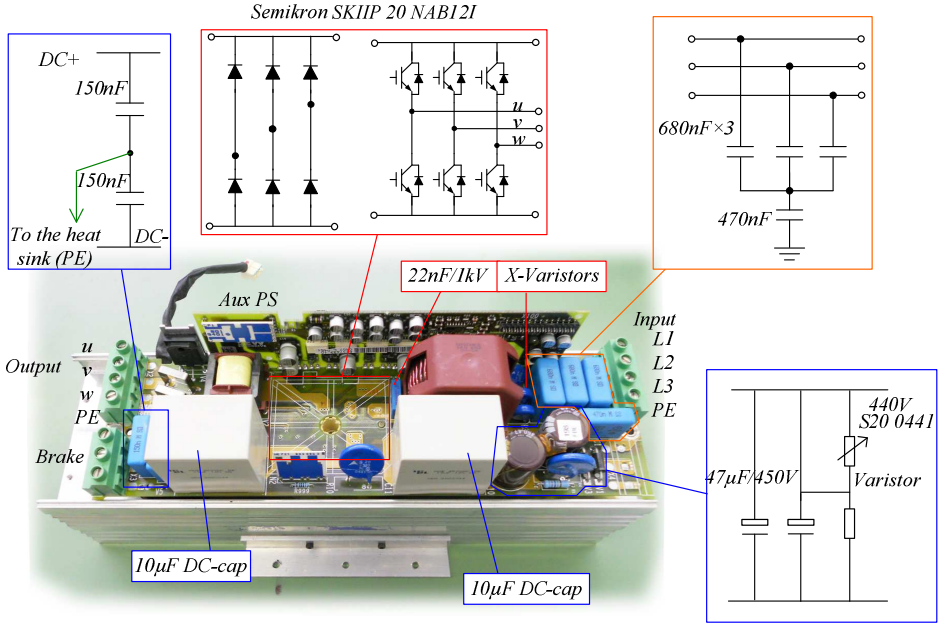
Abbreviation	Explanation
V_{inv}	The CM noise source
Z_L	The impedance of LISN
Z_{ic}	The impedance of the inverter input cable
Z_{ih}	The impedance between the inverter input and the heat sink
Z_{rec}	The impedance of the rectifier and the DC bus
$Z_{ht(1,2)}$	The impedance between the two ends of the heat sink
Z_y	The impedance between DC bus and the heat sink
Z_{mi}	The impedance between the SKiiP 20NAB12 module rectifier node and IGBT node
Z_{dh}	The impedance between the module IGBT node and the heat sink
Z_{ioh}	The impedance between output terminal of the inverter legs and the PE line
Z_{oc}	The impedance between the inverter output and motor
Z_{mow}	The impedance of Motor
Z_{mc}	The impedance between the motor frame and inverter heat sink

Parameters extraction through direct measurements

The parameters are categorized into two groups based on the extraction methods of through direct measurements and calculations respectively. When performing direct measurements, the inverter is disassembled into three parts: control panel, PCB circuit, and semiconductor module with the heat sink, as shown in Fig. 3.19 (a). Photographs of the circuits and the corresponding schematics from the disassembled SEW drive are illustrated in Fig. 3.19 (b).



(a)



(b)

Fig. 3.19 Photographs of the circuits and the corresponding schematics from the disassembled SEW drive (a) circuit parts after disassembly (b) corresponding schematics

Referring to the complete circuit model (shown in Fig. 3.18), the separation of the control circuit board leads to the parameters of Z_{ih}, Z_{rec}, and Z_{mi} being isolated from the other parameters, which is shown in Fig. 3.20. Hence it is possible to extract the following elements by direct measurements.

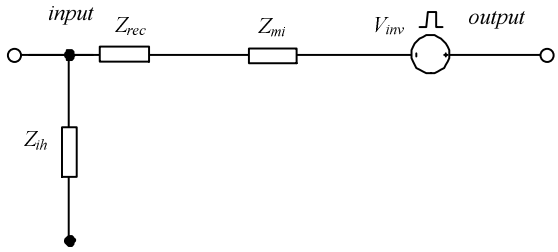


Fig. 3.20 The remaining parameters after disassembling the PCB circuit from the module and heat sink

1. Z_{ic}:

The impedance-frequency characteristic of the inverter input cable is directly measured by disconnecting its terminations to the LISN and the inverter respectively. The experiment setup is illustrated in Fig. 3.21. Two red crosses mark the circuit disassemble break points. Two copper plates are used to short-circuit the cables. The comparison between the measured and calculated characteristics is shown in Fig. 3.22. The parameter values are listed at the right side of the figure, where L_1 is calculated according to slope k of the impedance curve, R_1 is the minimum impedance of the curve, and C_1 and L_1 create the resonant frequency f_2.

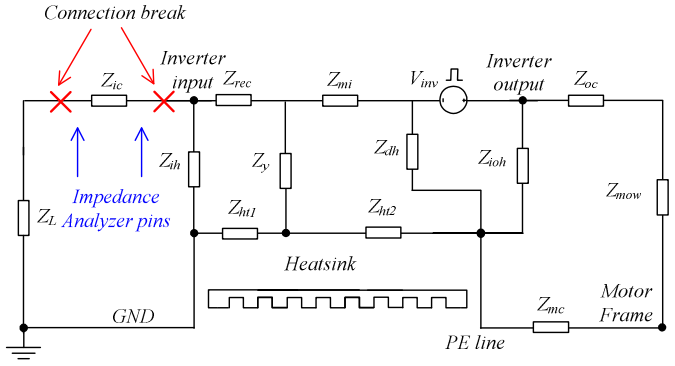


Fig. 3.21 Experiment setup to measure Z_{ic}

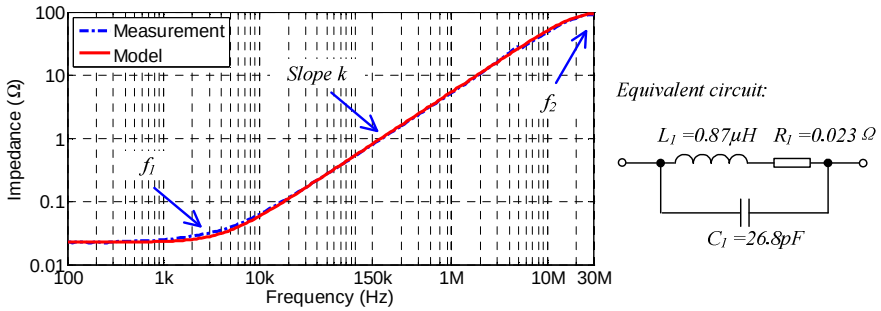


Fig. 3.22 Comparison between the measured and calculated characteristics of Z_{ic}

2. Z_{rec}:

To measure the impedance between the input nodes of the rectifier and DC bus, both of the three-phase rectifier bridge input and DC+ and DC– bus are short-circuited. A 2V DC voltage which is generated from the impedance analyzer is applied to keep the diodes conduct. The measurement setup is shown in Fig. 3.23. Disconnected points after circuit disassembling are marked by the red crosses. Comparison between the measured and calculated characteristics is shown in Fig. 3.24. The parameter values are shown at right side of the figure, where L_1 is calculated according to slope k of the impedance curve, and R_1 equals to the minimum value of the impedance.

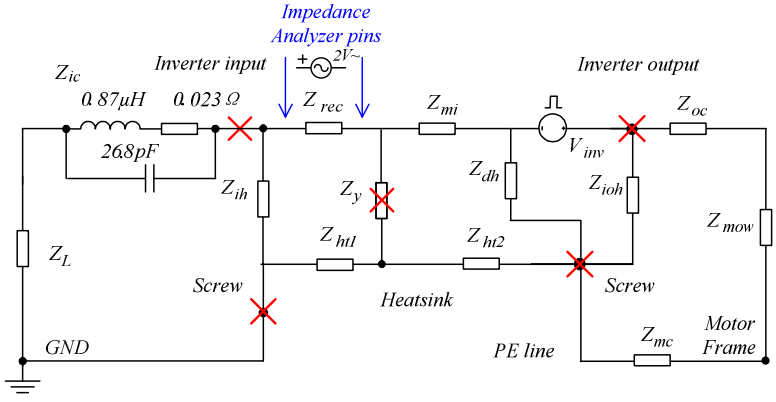


Fig. 3.23 Experiment setup to measure Z_{rec}

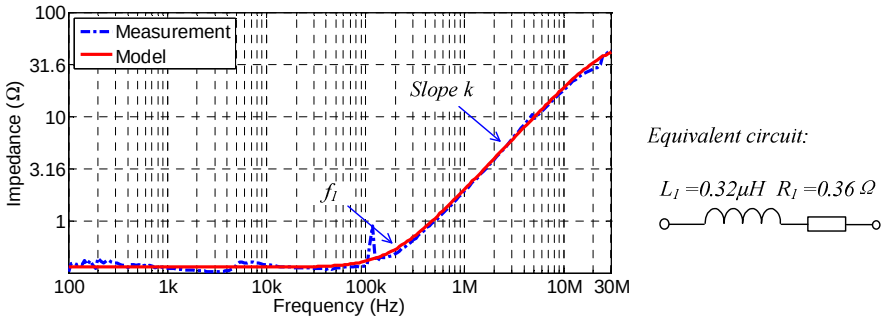


Fig. 3.24 Comparison between the measured and calculated characteristics of Z_{rec}

3. Z_{ht1}+Z_{ht2}:

The impedance of Z_{ht1}+Z_{ht2} is obtained by connecting the impedance analyzer pins to the two screws located in the input and output sides of the heat sink. The two screws are used to connect the PCB circuit to the heat sink. The experiment setup to measure Z_{ht1}+Z_{ht2} is illustrated in the Fig. 3.25. The comparison between the measured and calculated characteristics of Z_{ht1}+Z_{ht2} is illustrated in the Fig. 3.26. Extraction of the parameters follows a similar process to that of Z_{rec}.

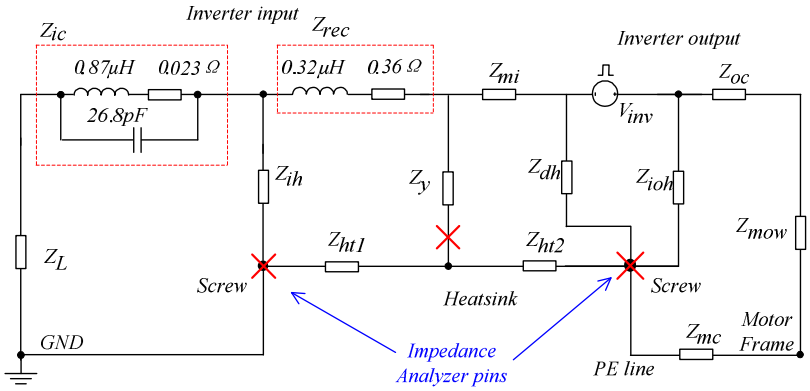


Fig. 3.25 Experiment setup to measure Z_{ht1}+Z_{ht2}

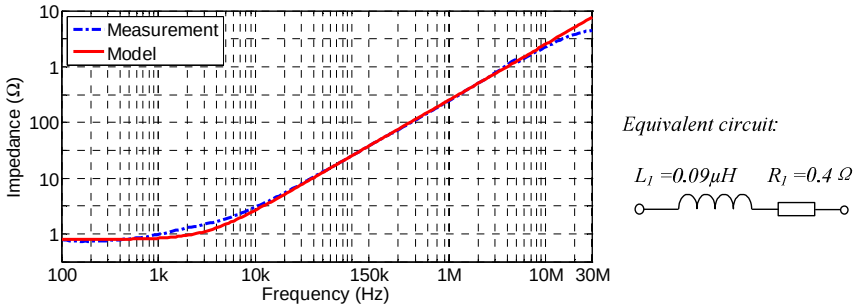


Fig. 3.26 Comparison between the measured and calculated characteristics of Z_{ht1}+Z_{ht2}

4. Z_{oc}+Z_{mow}+Z_{mc}+Z_{ioh}:

Extraction of Z_{mow} follows the same procedure as introduced for the electric machine in Section 3.2.3. The same motor is used. The impedance of Z_{oc}+Z_{mc} corresponds to a 2m long power cable that is connected between the inverter and motor. Z_{oc} corresponds to the three-phase conductors and Z_{mc} corresponds to the PE conductor. The simplified cable model of Fig. 3.12 is used. Z_{ioh} (300pF) is identified from the lumped capacitor values of the cable model shown in Fig. 3.7. The inductance value of the cable is also lumped and summed into the inductance of L_i and L_g in the motor model as shown in Fig. 3.14. The cable is connected to the motor when measuring the characteristics. The experiment setup to measure the impedance of Z_{oc}+Z_{mow}+Z_{mc}+Z_{ioh} is illustrated in Fig. 3.27. The built model of the motor with cables is shown in Fig. 3.28.

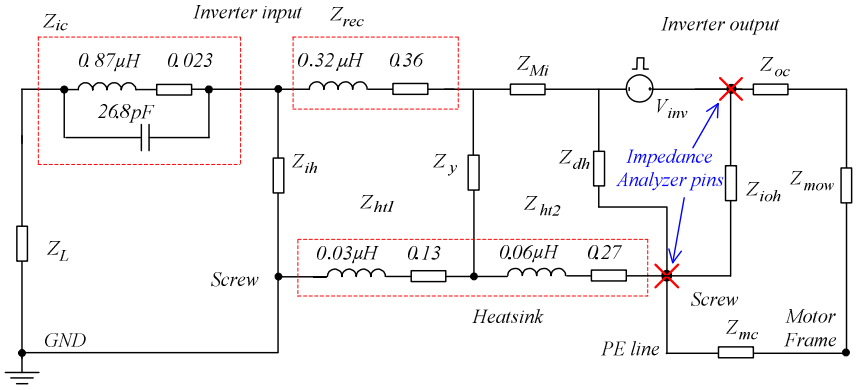


Fig. 3.27 Experiment setup to measure Z_{oc}+Z_{mow}+Z_{mc}+Z_{ioh}

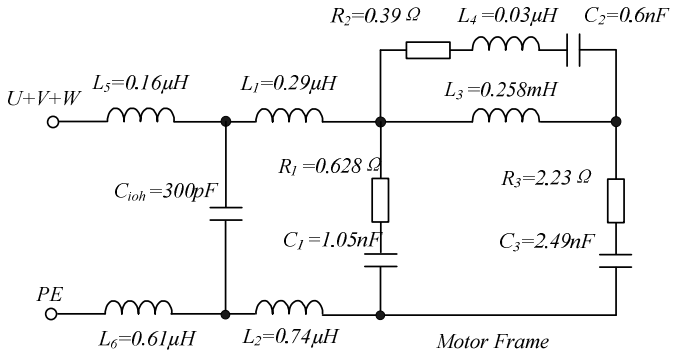


Fig. 3.28 Equivalent circuit model of parameters Z_{oc}+Z_{mow}+Z_{mc}+Z_{ioh}

Up to now, the procedure for extracting the parameters by direct measurement has been introduced. The equivalent circuit model with extracted elements is shown in Fig. 3.29.

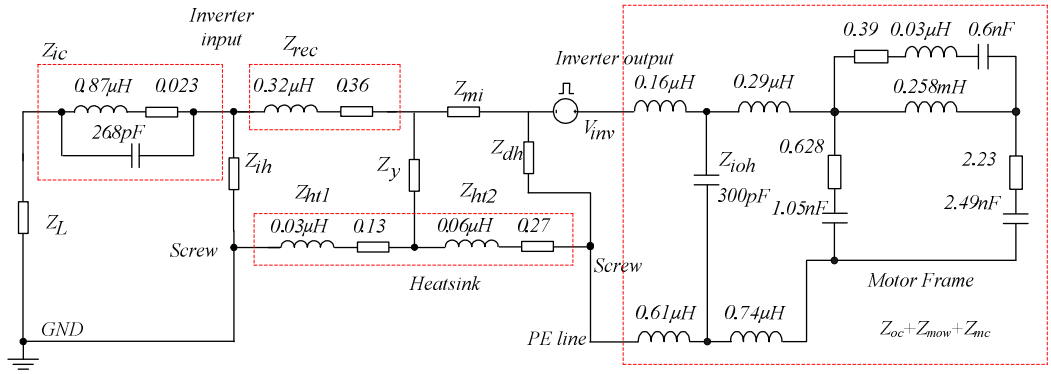


Fig. 3.29 Equivalent circuit model with parameters extracted through the direct measurements

Parameters extraction through open- and short-circuit measurements

The remaining parameters illustrated in the Fig. 3.29 are extracted through open- and short-circuit measurements, which means one side of the inverter (output or input) is kept open or short circuited during measurement at the other side of the inverter. The drain and source of the IGBTs are short circuited. Elements are extracted through the characteristics measured at the input side of the inverter. Measurement at the output side is used to verify the results. Photograph of the short-circuit measurement setup measured at the inverter input side is shown in Fig. 3.30. The obtained characteristic is shown in Fig. 3.31.

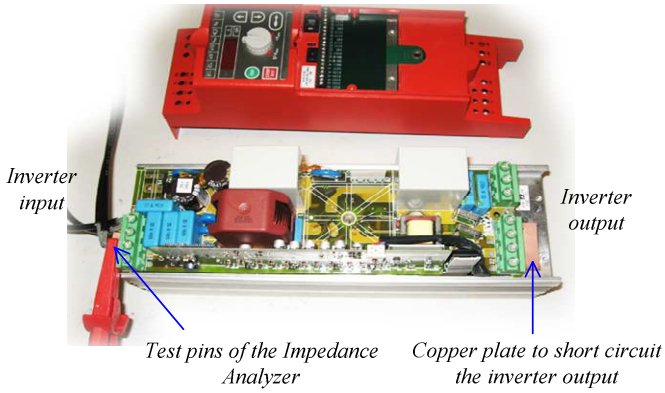


Fig. 3.30 Photograph of the short-circuit measurement setup

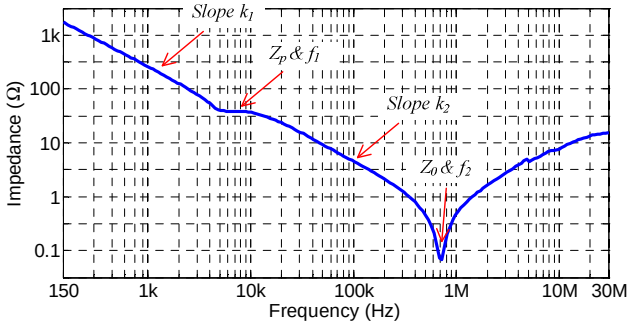
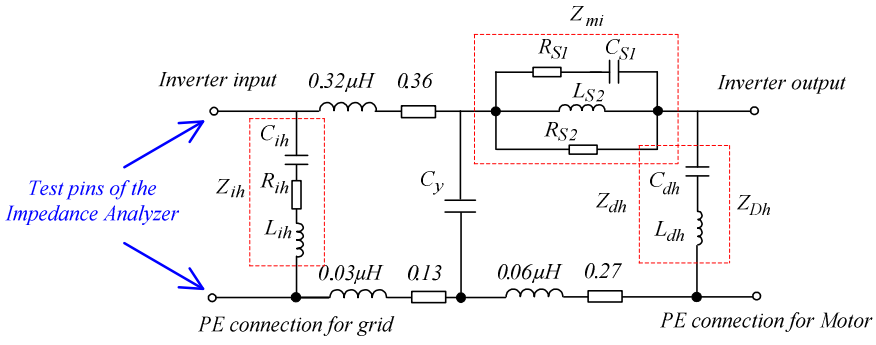
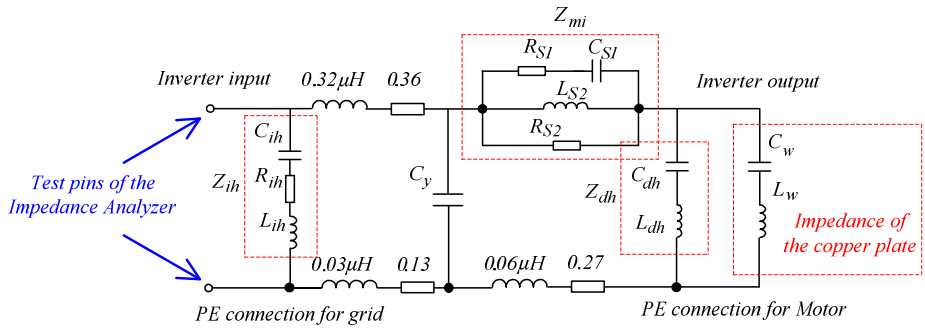


Fig. 3.31 Measured open-circuit impedance-frequency characteristics at the inverter input side

An equivalent circuit model of the inverter is proposed in Fig. 3.32, where configurations for both the open- and short-circuit measurements are shown. Parameters extracted previously are also shown. To calculate the parameters that are still unknown in the model, several points are selected in the measured characteristics. The parameters have physical meanings associated with schematics of Fig. 3.17, Z_{ih} represents the Y capacitors. L_{s2} represents the DC bus inductance of inductor choke. C_{s1} represents the parasitic capacitance of the inductor. R_{s2} is used to limit the peak impedance of Z_p (shown in Fig. 3.31). C_y represents the parasitic capacitance between traces of DC bus and the heat sink. C_{dh} represents the parasitic capacitance between the inverter phases and the heat sink. C_w and L_w represent the equivalent capacitance and inductance respectively of the added copper plate which is used to short-circuit the inverter output or input.



(a)



(b)

Fig. 3.32 Proposed equivalent circuit model of the inverter under open- and short-circuit conditions (a) for open-circuit (b) for short-circuit

Extraction of parameters through open- and short-circuit measurements is introduced as follows. According to Fig. 3.31, the total capacitance of $C_{ih} + C_y + C_{dh}$ is derived from the slope k_1 at low frequencies. The capacitance of C_{ih} determines the slope k_2 of high frequencies. L_{s2} and C_{s1} create the first zero point Z_1 of the curve. L_{s2} and C_{dh} create the resonance at the frequency f_2. The inductance of L_{s2} is adjusted to fit the slope at low frequencies under the short-circuit condition. The calculated values are shown in Fig. 3.33. Comparisons between the measured and calculated characteristics of the inverter model are shown in Fig. 3.34 (a) and (b) respectively. The calculated results agree well with the measurements.

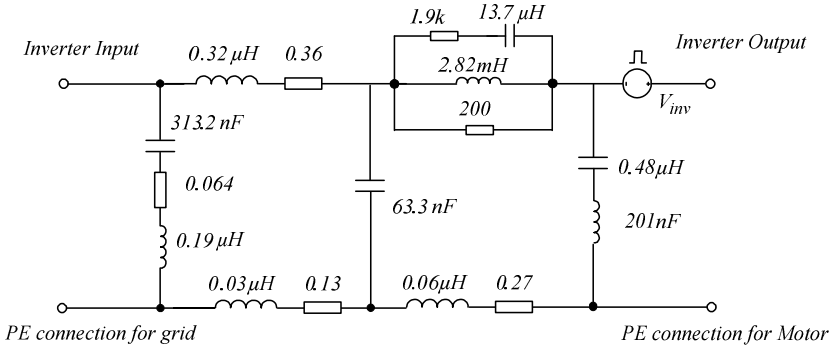
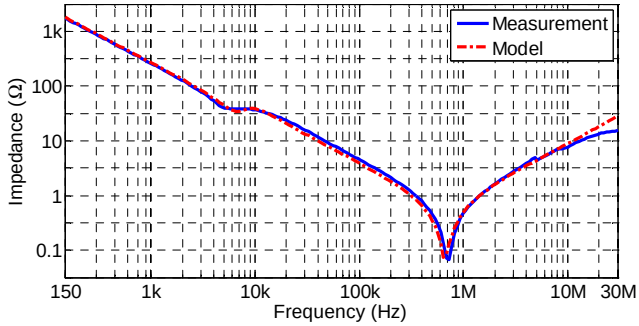
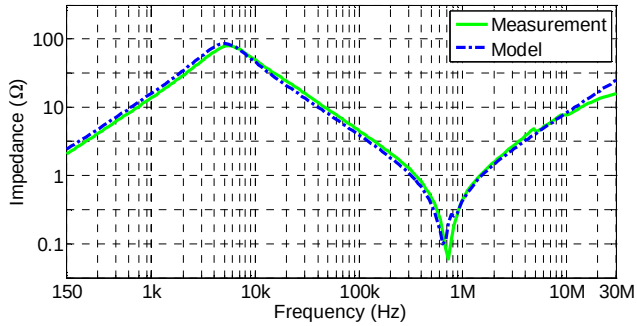


Fig. 3.33 Equivalent circuit model of the inverter with extracted elements



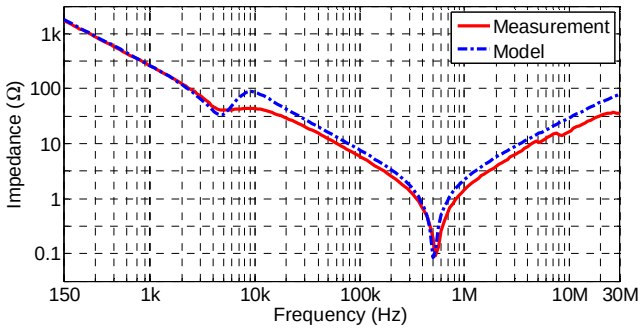
(a)



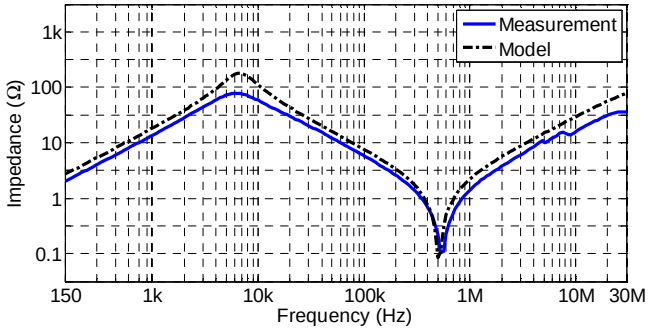
(b)

Fig. 3.34 Comparison between the calculated and measured characteristics of the inverter model (a) open-circuit (b) short-circuit

The frequency-impedance characteristics are measured at the inverter output side and compared with calculations to verify the inverter model. The three-phase inputs of the inverter are short- and open-circuited to the PE respectively. Comparisons between the measured and calculated characteristics under the two conditions are shown in Fig. 3.35 (a) and (b). Since calculations are done using extracted values in Fig. 3.33, the two characteristics resembled closely, and no new calculations are introduced, the inverter model is thus verified.



(a)



(b)

Fig. 3.35 Comparison between the calculated and measured characteristics of the inverter model at the inverter output side (a) for open-circuit (b) for short-circuit

Up till now all the model elements are extracted through the proposed procedure. They are shown in Fig. 3.36. The impedance of Z_L is modeled as a series connection of $50/3\Omega$ and $0.3\mu F$ according to the equivalent circuit of LISN proposed in Fig. 3.2.

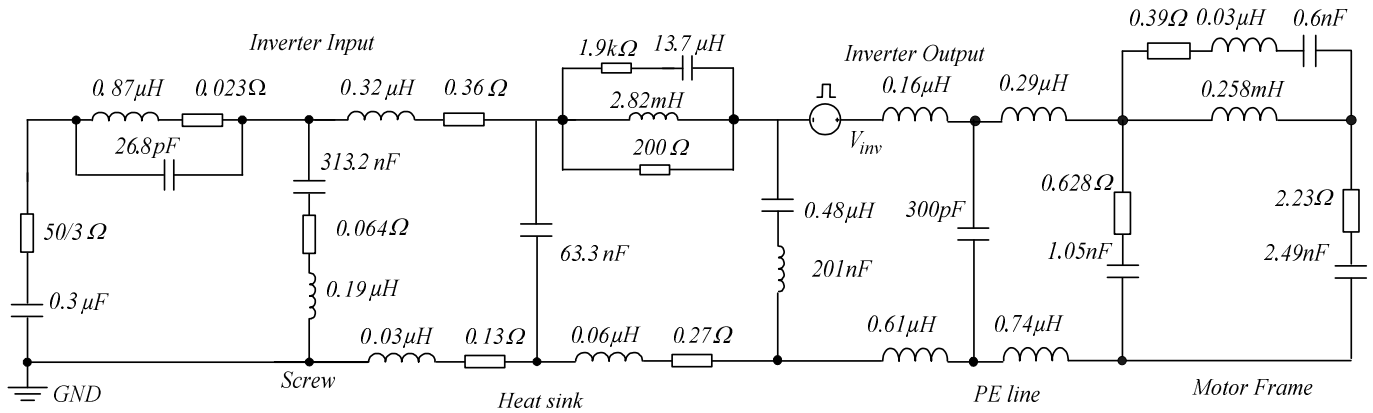


Fig. 3.36 Final CM equivalent circuit model with extracted elements

Verification in large signal condition

As aforementioned, the current transfer ratio measurements are used to verify the model under the large signal condition. The current transfer ratio is defined as the ratio of the CM current on the inverter input lines side (i_1 as shown in Fig. 3.17) to the CM current on the motor side (i_2 as shown in Fig. 3.17). In equation it is expressed as:

$$T = 20 \cdot \log_{10}(\frac{i_1}{i_2}) \tag{3.3}$$

The ratio reflects the conversion efficiency from i_{CM2} to $i_{CM1.}$ It is used to indicate how efficient the EMI noise propagation loops are suppressed by the applied filter.

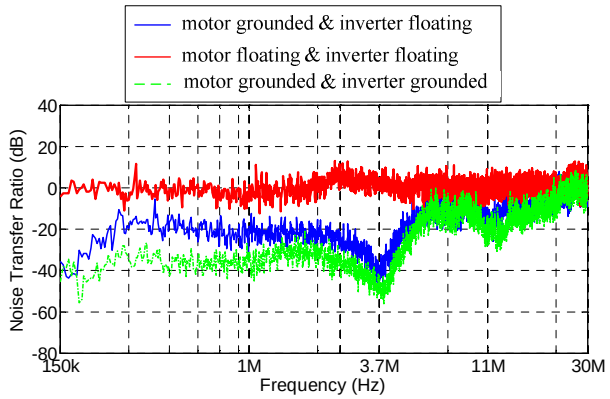
The current transfer ratio is measured under three conditions:

1. The motor is grounded and the inverter is floating
2. Both the motor and inverter are floating
3. Both the motor and inverter are grounded

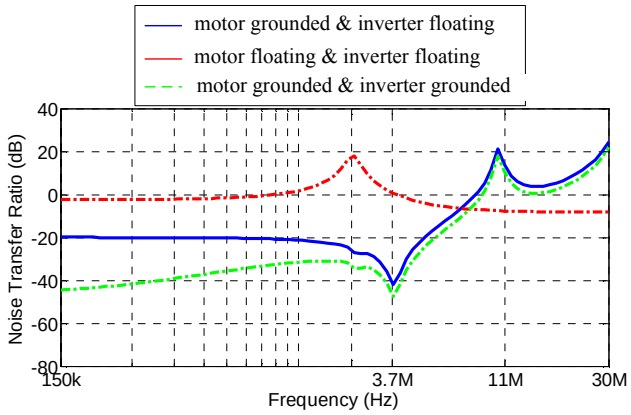
The measured and calculated noise transfer ratio curves are illustrated in Fig. 3.37 (a) and (b) respectively. Fischer F-75 current probes are used as the measurement tool. It can be seen that the calculations based on the built model show good agreements with the measurements. The ratio magnitude also agrees well with the measurements at low frequencies. Variations between the measurements and calculations in high frequency range are analyzed as follows:

1. Simplification of the model.
2. Temperature increases when the system operates. Therefore the resistance is increased.
3. High frequencies cause the inductance and capacitance nonlinear any more.

Although above variations exist, the proposed model shows acceptable accuracy under both small and large signal conditions.



(a)



(b)

Fig. 3.37 Current noise transfer ratio of the system under three conditions (a) experimental results (b) calculated results

3.4 Conclusion

Equivalent circuit models are widely used to analyze and predict the conducted emissions for power electronic systems. This provides acceptable accuracy and is a compromise between the complicated numerical computations considering associated device physics and oversimplified assumptions. In this chapter the focus is on the equivalent circuit modeling for conducted EMI frequencies. The study target includes the LISN, power cables, electrical machine and a 2.2 kW motor drive system.

The aim of adding elements in the model is to present details of filter high frequency attenuations. Prediction of high frequency is difficult to obtain because it is largely influenced by various component resonances and interactions. Depending on the investigation purpose and concerned frequency ranges the model can be adjusted by including elements which greatly influence the correlated performance.

In this chapter, element extraction procedure is systematically introduced. Disassembly of the inverter is involved for easy access of the instrument probes and parameters isolation. The

elements in the high-frequency equivalent circuit of the model are derived using by measuring impedance-frequency characteristics under open- and short- conditions. Good agreement between measured and calculated impedance-frequency characteristics verifies the model accuracy.

For the large signal experiment, current noise transfer ratio is used as the modeling target. The ratio is defined as the CM currents on the inverter input side to the CM currents on the motor side. It reflects the noise suppressing efficiency of the filter. Analyses on noise spectral contents are avoided, which simplify the process. The experimental measurements show good agreement with the calculated results. Based on the model, performances of various filtering solutions can be evaluated. Hence the optimal filter design can be obtained.

Chapter 4

3D Parasitics Cancellation

4.1 Introduction

In this chapter three-dimensional (3D) parasitics cancellation techniques for EMI filters in a high density motor drive, are explored. The high density drive is constructed using the multi-layer PCB technology and employs surface mount technology (SMT) components. The employed SMT components are x-dimensional (x-dim) components that have the same height (x=14mm) and double sided SMT electrical terminations [Fer10]. The components are stacked between planar substrates and can be soldered on both, top and bottom sides of each PCB layer, hereby a platform for 3D spatial placement is provided. The 3D parasitic cancellation allows for better EMI filtering performance while without scarifying the filter power density.

The filter parasitics which include both self-parasitics and mutual coupling are detrimental to the filtering performance especially in the high frequency range. The well-known self-parasitics include the equivalent series inductance (ESL) and equivalent series resistance (ESR) in capacitors, and equivalent parallel capacitance (EPC) and equivalent parallel resistance (EPR) in inductors. ESL is generated with the capacitor's leads and internal rolled film. In the case of a Y-capacitor, its noise shunting performance is largely dependent on its grounding impedance. In the case of an inductor, EPC is generated due to the electric field distributed between the winding turns and between the windings and the core. The ideal inductor impedance is proportional to the frequency. However, in practice it is decreased by the EPC effect especially in the high frequency range. In other words, the inductor's high frequency blocking ability is reduced.

Mutual coupling occurs between different components. It appears as the increased parasitics in the filter. In a circuit there are various mutual coupling points because each component acts as an electromagnetic field source. It is shown in many papers that much better filtering performance can be achieved through the proper design of PCB layout and components placements. Previous investigations show that two filters with identical topology and components can exhibit a significant difference in filtering performance when their layout and integration methods are different [Wan04a].

In this chapter, the 3D cancellation techniques used to cancel both the self parasitics and mutual coupling of EMI filters are presented. The EMI filter implements multi-layer PCB technology which enables 3D component placement. In addition to positioning the employed x-dimensional SMT components 360° in the two dimensional (2D) plane, the components are

able to be placed in a third dimension by adding more PCB layers, as shown in Fig. 4.1. Cancellation windings are designed and implemented to cancel the self-parasitic effects of the x-dim SMT components. The proposed techniques are applied on a LC CM filter for a motor drive. The filter equivalent circuit model that includes only the component self parasitics is built. Through the model essential parasitic and mutual coupling effects are identified. The techniques are verified by both of the insertion losses measured from a network analyzer and spectra measured from a LISN.

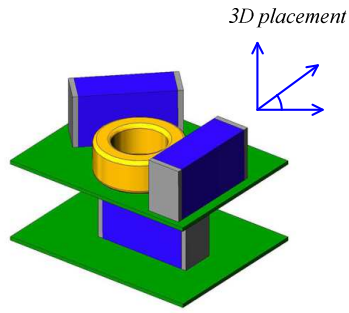


Fig. 4.1 Placement of EMI filtering components in 3D for mutual coupling cancellation

4.2 Present filter parasitics cancellation techniques

Over the last couple of years, many filter parasitics cancellation techniques have been developed. There are two groups of parasitic effects to be cancelled. One is self-parastics which include capacitor ESL and inductor EPC effects, and the other is the mutual coupling which occurs among different filtering components. Cancellation of self-parasitic effects is achieved by generating an equal value which is negative to the self-parasitics. In the cause of mutual coupling, reduction is usually achieved by either shielding the susceptible components to prevent the emission from the sources or positioning the components to achieve the lowest magnetic flux links. Nowadays mutual coupling reduction is based on the 2D spatial layout using the single PCB technology as can be seen in the following sections.

4.2.1 EPC cancellation techniques

Capacitance cancellation techniques are generally applied to cancel the EPC of a wounded inductor. In principle it can be used to cancel any stray capacitance in the circuits, such as the parasitic capacitance between the power device drain and the attached heat sink. Wang et al. applies two external capacitors to cancel the EPC in both CM and DM inductors based on the balance condition in the Wheatstone bridge, as shown in Fig. 4.2 (a) [Wan06b]. It is assumed that the two DM conductors are identical. If the product of C_{p1} and C_{p2} is equal to the product of added capacitance of C_{cl1} and C_{cl2}, the effects of C_{p1} and C_{p2} are cancelled. Two shunt capacitors of C_1 and C_2 are equivalently paralleled across the inductor's two sides, as shown in the Fig. 4.2 (c). The idea of EPC cancellation for CM inductors is the same. In the case of CM, the two windings of the CM inductors are center tapped and the two grounded capacitors are

connected to this center tap. The same impact as when cancelling the EPC in DM windings is achieved.

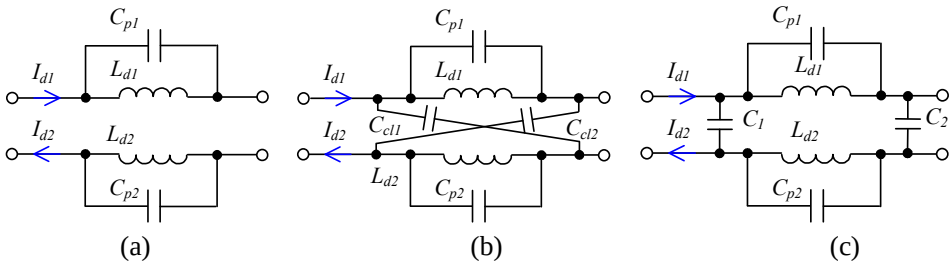


Fig. 4.2 Cancellation of the DM inductor parasitic capacitance in single phase [Wan06b] (a) DM inductor structure (b) winding EPC cancellation method (c) equivalent circuit network after applying the method

In [Hel07], EPC cancellation techniques from the single-phase inductor are extended to three-phase power line filters. It is found that the cancellation network can be achieved without the cancellation capacitors added symmetrically in the three phase, a single capacitor connected to the center of one winding would ideally be enough, as shown in Fig. 4.3 (b). This has the same effect as connecting the compensation capacitors to the center point of each winding as shown in Fig. 4.3 (a).

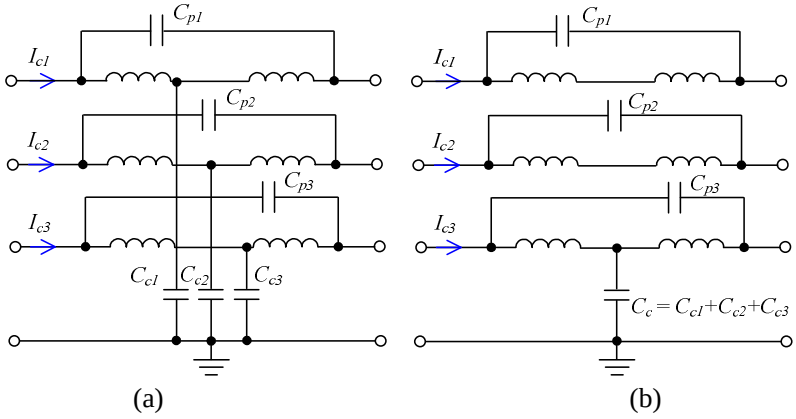


Fig. 4.3 Cancellation of the CM inductor parasitic capacitance in three phase [Hel07] (a) three capacitors symmetrically connected to the three windings (b) a single capacitor connected to one of the windings

Wang et al. proposes a method to cancel the parasitic capacitance between the switch drain and the earth utilizing the inductor mutual inductance [Wan07]. However, this method is also valid to cancel the EPC for discrete inductors. The cancelling principle is presented in Fig. 4.4, where Fig. 4.4 (a) shows the network that provides the cancellation effect. In the figure, two inductors with the inductance of L and n^2L are two coupled inductors, and n is the turn ratio of the two inductors. Assuming the coupling coefficient k is 1, the mutual inductance M is

calculated as nL ($M = k\sqrt{L \cdot n^2 L}$). Therefore the "T" network having same impedance transfer matrix as Fig. 4.4 (a) is achieved as shown in Fig. 4.4 (b). Further, according to the $Y-\Delta$ transformation, the "π" equivalent network of Fig. 4.4 (c) is derived. A negative capacitance is generated as opposite to the EPC of the inductor. Two grounded capacitors are also equivalently produced at the two sides of the inductor. This principle is also used to cancel ESL in Y capacitors, which will be introduced in section 4.4.4.

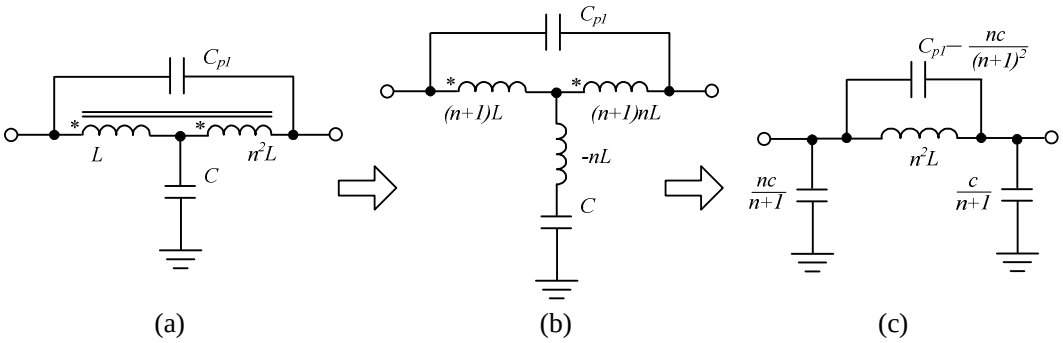


Fig. 4.4 Cancellation of the inductor parasitic capacitance utilizing the inductor mutual inductance [Wan07] (a) the network providing the cancellation effect (b) "T" equivalent circuit network (c) "π" equivalent circuit network

4.2.2 ESL cancellation techniques

ESL cancellation techniques are carried out on both CM and DM filtering capacitors. The techniques are used to decrease the grounding impedance of CM capacitors, and also to reduce the low frequency oscillations and the ripple of the DM current. Neugebauer et al. proposes the use of coupled magnetic windings to cancel the parasitic inductance in discrete capacitors [Neu04b]. The principle is illustrated in Fig. 4.5.

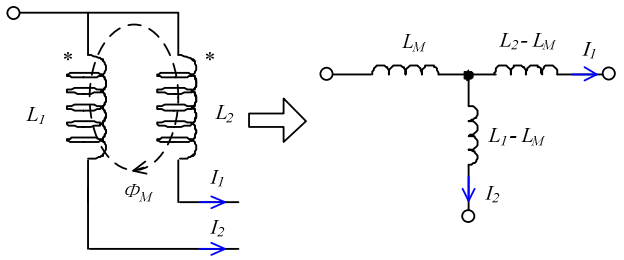
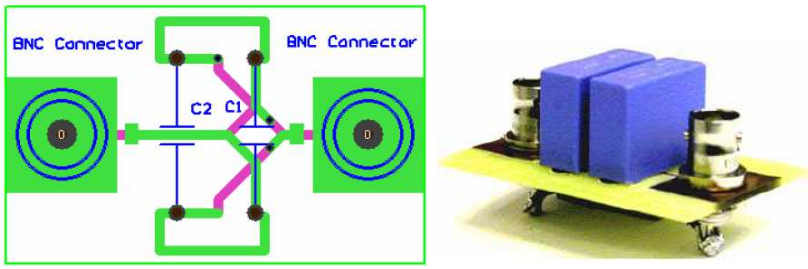


Fig. 4.5 Cancellation of the capacitor parasitic inductance [Neu04b]

In addition to discrete capacitors, techniques are also developed to cancel the ESL in capacitors in pairs. In [Wan06a] the PCB layout design is optimized to cancel ESL of two capacitors in parallel connection. The cancellation windings are realized using rectangular PCB traces. The design principle is the same as that was introduced to cancel the EPC in DM inductors (shown in Fig. 4.2). The designed PCB layout and the ESL cancelled filter prototype are illustrated in Fig. 4.6 (a) and (b), respectively.



(a) (b)

Fig. 4.6 ESL simultaneous cancellation for two paralleled film capacitors [Wan06a] (a) PCB layout (b) photograph of the prototype

4.2.3 Mutual coupling cancellation techniques

Mutual coupling cancellations are more effective than self-parasitic cancellations. When developing the self-parasitics cancellation techniques, the research is mostly based on ideal conditions, and inductors and capacitors are generally not used alone. Because of the complexity of circuit, cancellation on the mutual coupling is more difficult. The inductive coupling mechanism is dominant in mutual coupling mechanism.

After identifying the parasitic effects on a CLC filter, [Wan05] verifies that although the self-parasitics degrade the filter performance in the high frequencies, more improvement can be achieved by reducing mutual coupling, which is realized by rotating the inductor winding by $90°$. A cancellation inductor is integrated with the capacitor to cancel the mutual coupling between two capacitors.

Another method is to shield the capacitors, which is proposed in [Wan04a]. Additionally, the capacitors are placed on the other side of the PCB to further reduce the coupling. The experiments show that carrying out mutual coupling cancellation is more effective than solely reducing self parasitics.

A simply way to cancel mutual coupling is to increase the distance between components. However, this is not desired because it decreases the power density. Additionally, since the length of PCB traces are increased, parasitics are also increased. For EMI filters manufactured on single PCBs, this acts as a barrier that greatly restricts the application of parasitics cancellations. With the generation of new power electronics construction technology and new components packaging with new properties, a platform is provided for applying 3D cancellation techniques. More flexibilities and better effects can be achieved.

4.3 SMT high density drive

The new components are called x-dim components. Such components allow for high components packaging density and double-sided heat removal from all x-dim components. Some samples of x-dim components, namely metal film capacitors, electrolytic capacitors, and SMT DM inductors are shown in Fig. 4.7. The electrolytic capacitors are designed to have the height of 1.5x. Thus when they are used in multi-layer PCBs two stacked electrolytic capacitors have the same height as three other inductors or metal film capacitors. The SMT

high density drive employs new SMT x-dim components which have the same (or compatible) heights x, and are stacked between planar substrates.

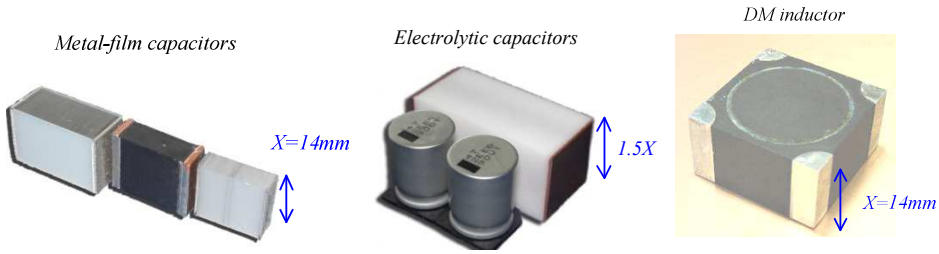


Fig. 4.7 SMT x-dim component samples [Jos10]

The assembly concept and the prototype of the SMT multi-layer 2.2 kW industrial drive is illustrated in Fig. 4.8 and Fig. 4.9 respectively. The topology is based on the two stage EMI filter topology which consists of a front stage EMI filter and DC bus EMI filter. The filtering components are arranged in the two sandwich layers. Electric connections are done by soldering the components to the bottom and top sides of the layer. In addition to the EMI filters, the other components include: Bridge rectifier, three-phase inverter stage, and control circuit. The input rectifier, braking chopper and IRC components are placed downwards on the bottom side of the second layer.

The possibilities for a third dimensional decoupling are achieved with x-dim components and by extending the conventional single PCB construction to the multi-layer PCB construction. The 2D and 3D parasitics coupling with the multi-layer PCB construction is illustrated in Fig. 4.10, where Φ_C represents the lumped fluxes generated from the capacitor side, and which are rooted from the ESL of the capacitor. Φ_i represents the lumped fluxes generated from the inductor, which are mainly from the leakage flux produced by the winding. The flux direction is determined by the right hand rule. These fluxes are linked from one loop to another so that the mutual coupling is formed (M_{ic}). The 3D cancellations aim at cancelling the 3D coupling.

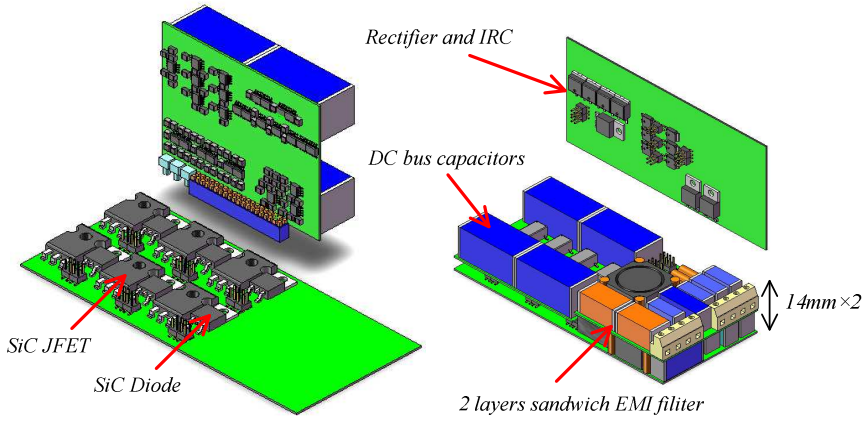


Fig. 4.8 Assembly concept of the 2.2 kW SMT multi-layer PCB industrial drive [Jos11b]

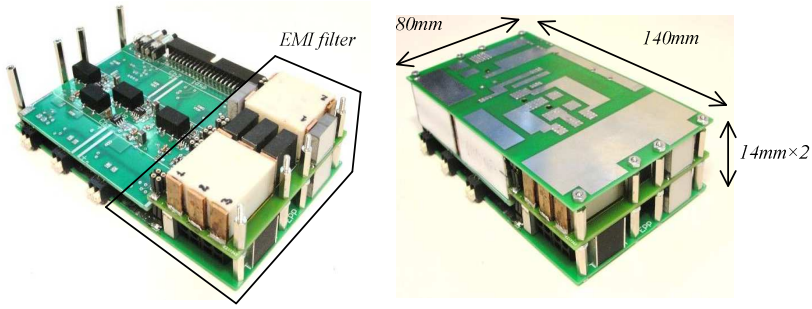


Fig. 4.9 2.2 kW SMT multi-layer PCB industrial drive demonstrator [Jos11b]

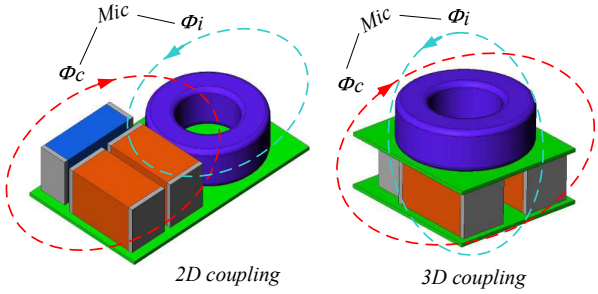


Fig. 4.10 2D and 3D parasitics coupling with the multi-layer PCB construction

4.4 3D parasitics cancellation

4.4.1 Parasitic effects of SMT components

ESL in a film capacitor is composed of the inductance of the metal film or electrode roll. Its value depends on the capacitor manufacture method and metal sprayed leads at the two ends of the capacitor. EPC in an inductor arises due to the stray capacitance which is distributed between windings of the inductor, between the winding and the core. Fig. 4.11 and Fig. 4.12 compare the calculated insertion losses of a sole x-dim capacitor and inductor with and without including self-parasitic effects respectively. The equivalent circuits of the capacitor and inductor are shown at right side of the figure. It can be seen that the parasitic effects greatly degrade the component filtering performance up to 45dB in high frequencies of the conducted EMI range.

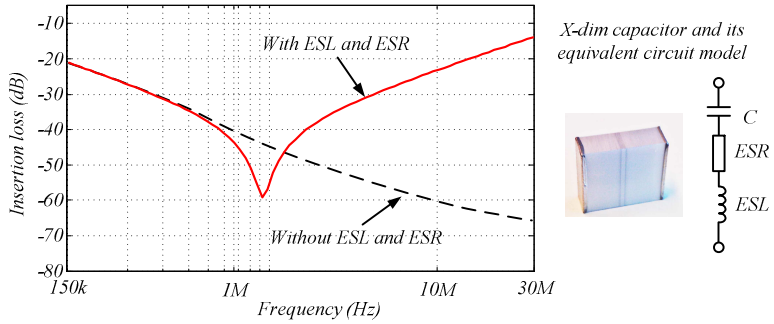


Fig. 4.11 Calculated single capacitor insertion losses using the model with and without self parasitics

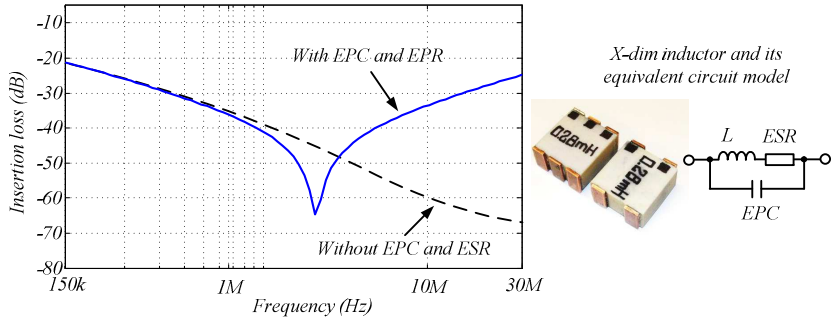


Fig. 4.12 Calculated single inductor insertion losses using the model with and without self parasitics

4.4.2 Parasitic effects in LC filters

In this section, 3D parasitics cancellation techniques are proposed and implemented in a LC filter for a motor drive. The drive is built using x-dim components introduced previously. Firstly, it is important to identify parasitics that greatly deteriorate the filtering performance. Therefore an equivalent circuit model is built. Secondly, filter insertion losses are measured and compared under conditions with and without applying cancellations. Thirdly, an ESL cancellation winding is proposed and implemented to cancel self parasitics of x-dim capacitors. Lastly, the techniques are implemented in the motor drive system. EMI spectra are measured by LISN to verify the discussions.

The LC CM filter is composed of a 0.4mH inductor choke (L_1) in series of two 470nF Y-capacitors (C_{p1} and C_{p2}). The equivalent circuit model including the self-parasitics and mutual coupling of the filter is shown in Fig. 4.13, where ESL_1 and ESR_1 are self parasitics of capacitor C_{p1}, ESL_2 and ESR_2 are self parasitics of C_{p2}, EPC and EPR are self parasitics of inductor L_1, and L_{in} and L_o are the inductance of PCB input and output traces respectively. The parasitic elements are extracted by curve fitting to the impedance as introduced in Chapter 2. The impedance analyzer Agilent 4294A is used as the measurement tool. In the case of the low pass filter design, minimizing the shunt-path impedance and maximizing the series-path impedance at high frequencies is the goal. These roles are taken by the choke inductor and Y-capacitors

respectively. At high frequency range, the EPC decreases the inductor blocking impedance and the ESL increases the capacitor shunting impedance. Fig. 4.14 compares the insertion losses between the calculation and measurements where 50Ω is taken both as the source and load impedances. The calculated result uses only the component self-parasitics of the model shown in Fig. 4.13. Two resonance corners (at K_1) appear. The first one is determined by ESL_1 and C_1, and the second one is determined by ESL_2 and C_2. The slope of K_2 is determined by EPC and L_D, which is self resonance of inductor L_1. The high frequency resonance K_3 is created by the resonance between the output trace L_o and the summed capacitance of C_1 and C_2. The low frequency level of from 100 kHz to the resonant corner K_1 is determined by the product value of L_D and C_p ($C_p = C_{p1} + C_{p2}$). Consequently, the calculation results indicate that the capacitor ESLs are essential in deteriorating the filter mid and high frequency (1 MHz ~ 30 MHz) attenuation performances. In other words, the filter capacitors are the most susceptible from the electromagnetic coupling. Therefore it is essential to cancel three couplings. They are:

- M_1: Coupling between L_D and ESL_1
- M_2: Coupling between L_D and ESL_2
- M_3: Coupling between ESL_1 and ESL_2

Coupling from the PCB input and output traces to the capacitors is neglected since it is sufficiently smaller than those from the inductor. When the capacitor values are small, the self-resonant frequencies of them are higher than the self-resonant frequency of the inductor. Therefore the EPC effect will be dominant [Wan04a].

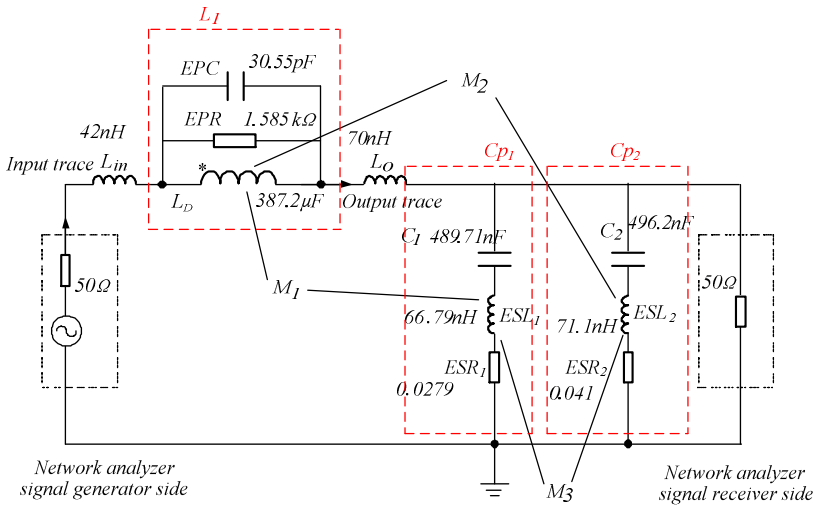


Fig. 4.13 Equivalent circuit model of the LC CM filter including self-parasitics and mutual coupling.

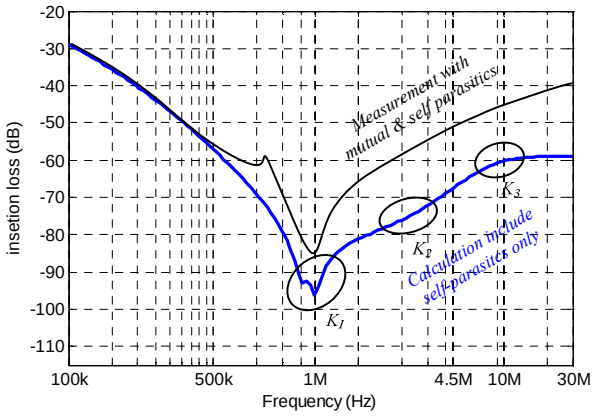


Fig. 4.14 Comparison of the measured and calculated insertion losses of the LC filter

4.4.3 Reduction of mutual inductive coupling

Reduction of mutual coupling between SMT capacitors

To reduce mutual coupling between the inductor and capacitors, the key action is to decrease the net magnetic fluxes linking to the capacitors. Generation of ESL in x-dim SMT capacitors is the same as that in the traditional film rolled capacitors [Fer10]. The SMT x-dim capacitor is composed of thousands of displaced parallel metalized films, its active part is connected to the SMT tabs through thermo-mechanical stress reliefs. The internal equivalent current flowing path is formed via one welding SMT tab to the other. These current loops link external magnetic flux therefore their mutual inductance is generated. Fig. 4.15 illustrates the mutual coupling generation mechanism between two SMT capacitors in parallel connection [Wan05]. The equivalent circuit i_1 that flows internally in capacitor C_1 links the magnetic flux Φ_2 produced from C_2, which acts as the increase of a mutual inductance M_3 onto the ESL of C_1. Similarly, M_3 is also added onto C_2. This impact leads to an increased ESL to both capacitors.

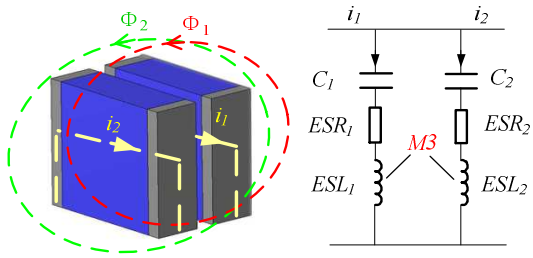
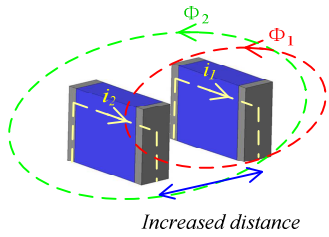


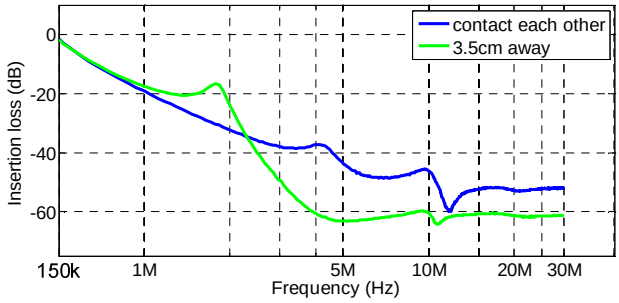
Fig. 4.15 Mutual coupling between two parallel SMT capacitors and the equivalent circuit model

The easiest way to reduce M_3 is to enlarge the distance between the two capacitors. Additionally, shielding materials can be added in between to further reduce the coupling. In 2D construction, this is at the cost of increased cost and total volume. In the SMT multi-layer PCB

constructed drive, these limitations are overcome by arranging the components onto different layers. The planar substrates placed in the middle are utilized as the shield. Fig. 4.16 (a) and (b) illustrate the placement of capacitor. The insertion losses are compared when the two parallel capacitors contact and are 3.5 cm away from each other. Both capacitor values are 470nF. The measurement was performed through a network analyzer (Anritsu-ms 4630b) where both source and load impedances are 50Ω. 10dB improvement is achieved above approximately 4 MHz. The resonance occurring at around 2 MHz is due to the increased inductance in the loop between the two capacitors.



(a)



(b)

Fig. 4.16 Mutual coupling reduction between two parallel SMT capacitors (a) increased distance between the capacitors (b) insertion loss measurement

Another method to reduce the mutual coupling is to position the two capacitors perpendicularly, which is shown in Fig. 4.17. In this way the net magnetic flux linking between two capacitors is reduced.

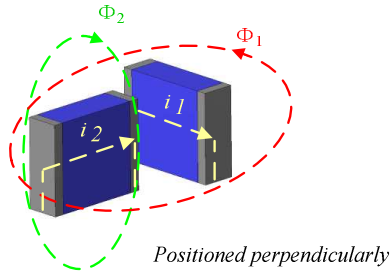


Fig. 4.17 Capacitors are positioned perpendicularly to reduce their mutual coupling

Reduction of mutual coupling between SMT inductor and capacitors

The coupling from the inductor side is mainly from the leakage flux produced by the inductor windings. The flux direction is based on the right-hand rule. Since the inductor leakage inductor is much larger than the ESL of the capacitors, it is more important to decrease the flux link from the inductor to the capacitor. The ideal cancellation is to impose the mutual inductance on the capacitor ESL to have the opposite polarity and the same amount. However this is difficult to realize due to the complicated flux distribution and nonlinear behavior of circuit parasitics. In 3D construction, two methods to minimize the mutual coupling between SMT inductor and capacitors are illustrated in Fig. 4.18 and Fig. 4.19 respectively. Fig. 4.18 illustrates the components arrangement of a single phase LC filter, the magnetic flux from the single phase inductor flows symmetrically to the center line of the two SMT capacitors. The height of the inductor can be designed to be the same height as that of the SMT capacitors so as to comply the x-dim components concept. In another method illustrated in Fig. 4.19, the inductor and capacitors are placed in different sandwich layers, and the middle board is utilized as the shield to prevent the electromagnetic fluxes coupling to the capacitors.

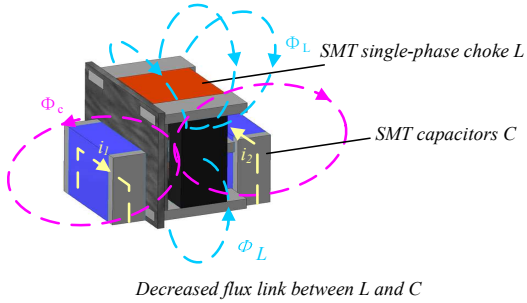


Fig. 4.18 Decrease the flux link between the inductor and capacitors

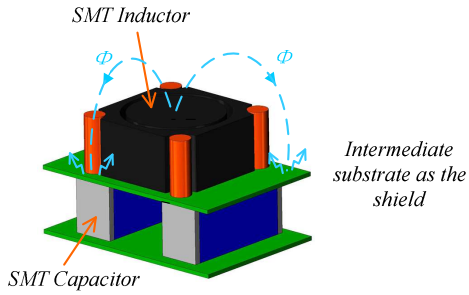


Fig. 4.19 Utilize the intermediate board as the shield

Intermediate substrate as shield

The planar substrates on which SMT components are stacked, can be utilized to prevent the coupling from inductors to capacitors. For single layer PCB integration technology, the components are arranged along the power flowing path for the convenience of layout design, as

shown in Fig. 4.20. Consequently, the components arranged from AC line input to the output are AC line EMI filter, the rectifier bridge, DC-bus EMI filter, power devices, and output EMI filter. This layout structure results in such a complex flux distribution environment that the capacitors are inevitably to be influenced. With the multi-layer PCB construction, the power flows are conducted to different layers through the SMT tabs or sprays of those SMT passive components, thus a more flexible circuit layout can be implemented. The substrate with the components are stacked in-between is designed as the shield to prevent the susceptible components from external coupling. This technique can be realized by implementing a PCB filling with copper or using IMS.

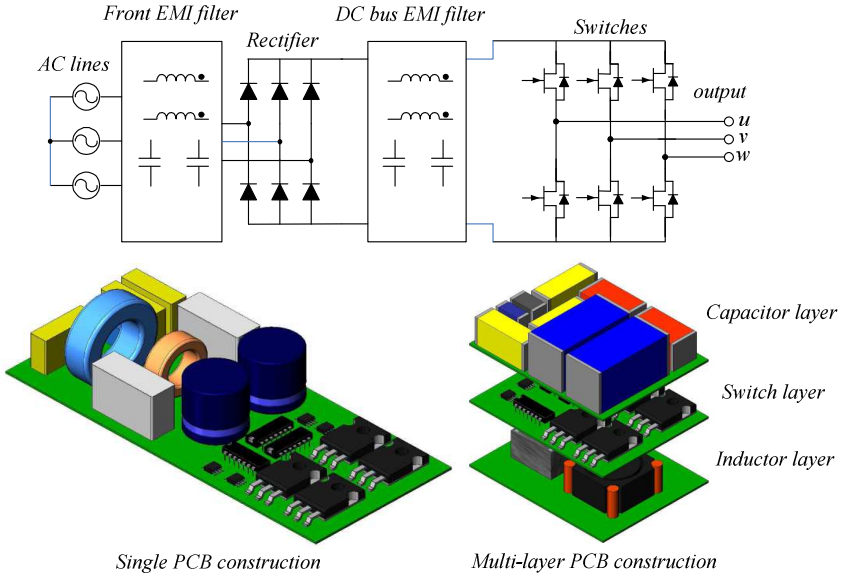


Fig. 4.20 The reduction of mutual coupling of susceptible components by multi-layer shielding

4.4.4 Design of ESL cancellation winding for SMT capacitors

In this section, ESL cancellation windings are designed to improve the filtering performance of SMT capacitors. The principle is to create an inductance which is equal to and has the negative polarity of the capacitor ESL. This is achieved by integrating a coupled air-core magnetic windings with the primary and secondary symmetrically connected to the SMT capacitor tab. Hence a three-terminal device is formed. The equivalent circuit model of the cancellation winding integrated capacitor is shown in Fig. 4.21. The two windings have the same polarity. Φ_{12} represents the mutual flux that links the primary and secondary windings. L_M is the resulting mutual inductance. For the network of Fig. 4.21(a), the relationship between the port voltages and currents are expressed as equation 4.1.

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = jw \cdot \begin{pmatrix} L_1 & -L_M \\ -L_M & L_2 \end{pmatrix} \cdot \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} + \frac{1}{Z_C} \cdot \begin{pmatrix} i_1+i_2 \\ i_1+i_2 \end{pmatrix} \tag{4.1}$$

where Z_C is the impedance of capacitor. It is the summed impedance of *ESL*, *C* and *ESR*. In the network shown in Fig. 4.21(b), the relationship between the port voltages and currents satisfy equation 4.2.

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = jw \cdot \begin{pmatrix} L_1 + L_M & 0 \\ 0 & L_2 + L_M \end{pmatrix} \cdot \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} + (\frac{1}{Z_C} - jwL_M) \cdot \begin{pmatrix} i_1 + i_2 \\ i_1 + i_2 \end{pmatrix} \tag{4.2}$$

It can be deduced that the two networks have the same characteristics. Ideal cancellation is achieved when the created mutual inductance is equal to the capacitor ESL. However, the stray inductance of PCB traces also contributes to the cancellation effect, which is difficult to calculate.

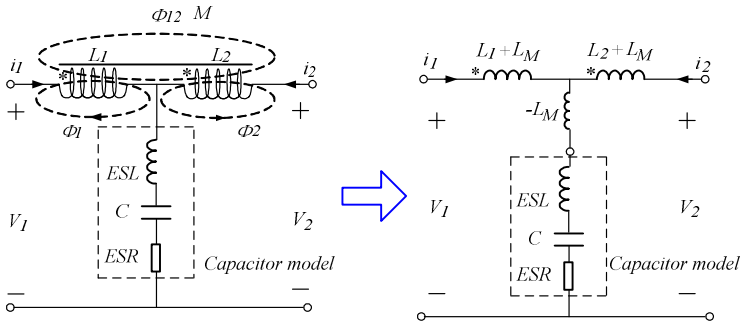


Fig. 4.21 Flux linkage and resulted equivalent circuit model of a capacitor with the cancellation winding (a) winding structure (b) equivalent circuit model

Fig. 4.22 illustrates the design and implementation of the two-coil layer structure of the cancellation windings. The winding is constructed out of a 1mm diameter common copper coil which can be adjusted according to the current flow rating. The height of the windings is designed as 14mm to comply with the multi-layer PCB construction. For different types of SMT x-dim capacitors, the winding widths are adjusted optimally according to the calculated mutual inductance and the resulted rectangular winding cross window area. The mutual inductance L_M of the two single-turn coils is approximated by equation 4.3 [Ye09].

$$L_M = \frac{\mu_0}{2\pi}[2a \cdot \ln(\frac{2a + 2vv'}{2a + 2wu}) + 2b \cdot \ln(\frac{2b + 2v'v}{2b + 2wu}) - 4(v - w + v' - u)] \tag{4.3}$$

Where: μ_0 is the air permeability, u is the distance between the primary and secondary winding window area, and a and b are the width and height of the coil window respectively. $v = \sqrt{a^2 + u^2}$, $w = \sqrt{a^2 + b^2 + u^2}$, $v' = \sqrt{b^2 + u^2}$. The two coils are assumed to have the same height and width. Accuracy of the calculation is also determined by the coupling coefficient between the primary and secondary sides. Taking the 470nF SMT capacitor as an example, the capacitor ESL value is measured as 9.6nH by the impedance analyzer (Agilent 4294A).

Therefore L_M is expected to be 9.6nH, and b is assigned as 14mm. As a result a is calculated as 29mm.

Fig. 4.23 shows the measured insertion losses before and after integrating the cancellation winding onto a 470nF SMT capacitor. The integrated capacitor is shown in Fig. 4.22. It can be seen that 20dB at most has been reduced in the high frequency range. it is found that a two or three layer of one cancellation winding is adequate for most of the capacitors.

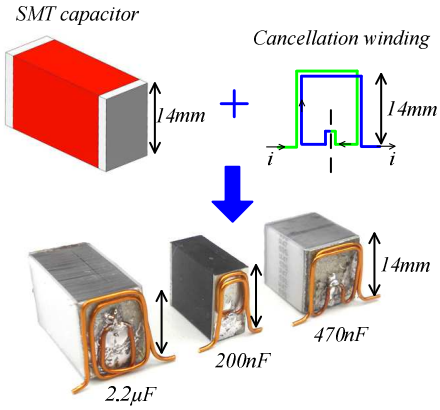


Fig. 4.22 ESL cancellation winding design and integration with different types of SMT capacitors

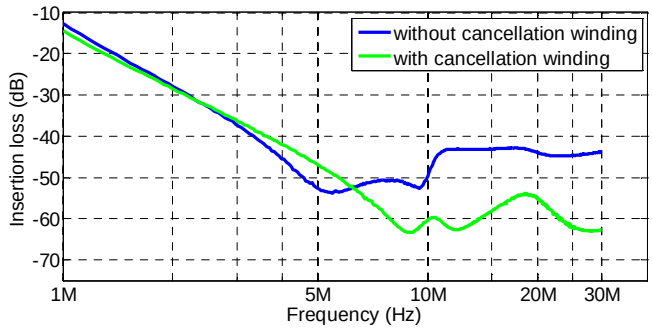


Fig. 4.23 Comparison of the measured insertion losses to a single SMT capacitor (470nF) with and without integrated cancellation windings.

4.5 Experimental verification through network analyzer and LISN

4.5.1 Insertion losses measured from network analyzer

Based on the understanding of the coupling effects and cancellation methods introduced previously, the filter components are positioned in 3D in order to achieve the reduced mutual magnetic fluxes. A group of insertion loss measurements are performed. Fig. 4.24 illustrates the experiment setups and the corresponding measured insertion losses. Two BNC connectors

are screwed on the two sides of the PCB board for injecting and receiving signals. A trail-and-error process is adopted instead of using the complicated theoretical calculations. The experimental results show that with the identical filter components and topology, different insertion loss curves are obtained. Position case 3 exhibits the best performance at the high frequencies. However, degraded performance occurs at the first resonant corner of around 1.6MHz. This is due to the increased length of inductor leads. Position case 2 increases the resonant frequency, which leads to better performance at the resonant frequencies, but an increased slope in the high frequency range. Overall, position case 1 exhibits the worst performance.

Secondly, the proposed ESL cancellation winding is integrated with the capacitors positioned in case 3 to further improve the filter performance. The experimental result is compared with the previous achievements under the condition of the three cases. It can be seen that 15dB more attenuation is achieved. The filter high frequency performance is significantly improved.

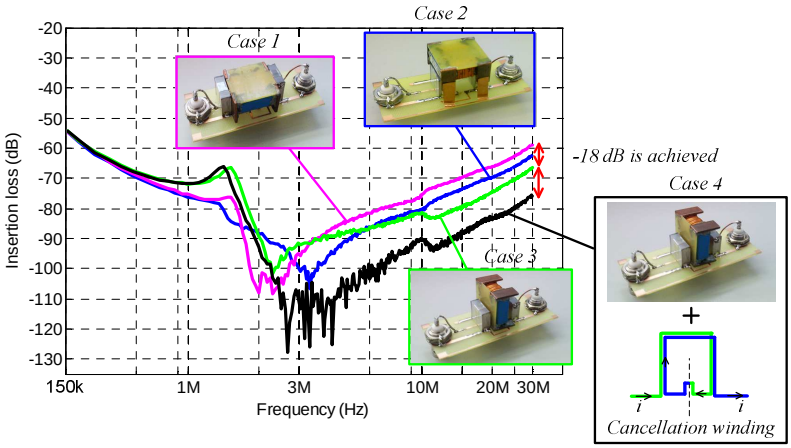


Fig. 4.24 Positioning the filter components to reduce their mutual coupling

4.5.2 Noise spectra measured from LISN

In addition to the small-signal measurements from the network analyzer, experimental verifications are also done through measurements by a LISN.

The first group of measurements is performed to investigate the effect of reducing the mutual coupling between the SMT inductor and capacitors. Fig. 4.25 illustrates the configuration of the motor drive system and how the cancellations are applied. The distance between L_1 and C_p is increased by positioning them into different sandwich layers. A three-phase LISN (Cranage VN3-100S) is positioned between the power grid and the motor drive system to measure the EMI emission level. The CM inductor (L_1) and Y capacitors (C_{p1} and C_{p2}) are positioned in the DC bus as the second stage. The component values of L_1, C_p and L_2 are 0.28mH, 470nF and 0.23mH respectively. The Y capacitors provide the shunting path from the DC bus to the earth. The heat sink and LISN are grounded to the same copper plate so as to provide the lowest

grounding impedance. As a consequence, the filtering performance is greatly dependent on the capacitor impedance.

Fig. 4.26 compares the LISN measured noise spectra when capacitors C_{p1} and C_{p2} are placed differently referred to the inductor L_1. It can be seen that more than 10dB improvement is achieved between 3.5 MHz and 15 MHz, which greatly reduces the noise in critical range to comply with the IEC61800-3 C2: Qp standard.

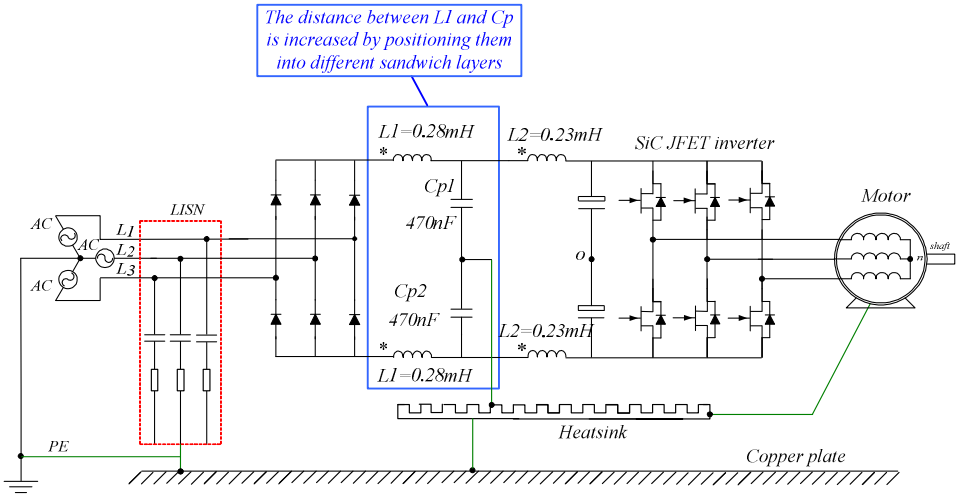


Fig. 4.25 Configuration of the motor drive system for reducing the mutual coupling between the filter inductor and capacitors

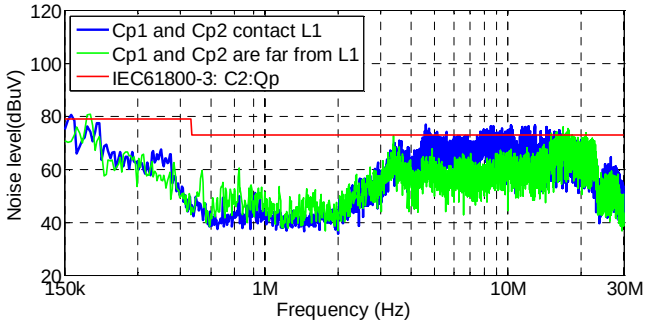


Fig. 4.26 Comparison of the LISN measured noise spectrums when C_{p1} and C_{p2} are in contact and far from the inductor L_1.

The second group of measurements is performed with the aim of investigating the cancellation effect of the proposed cancellation windings. Fig. 4.27 illustrates the configuration of the motor drive system and the photograph of the CM capacitors. A DC-fed IGBT based motor drive prototype is employed for the test. The experimental environment is the same as that for the configuration illustrated in Fig. 4.25. The same LISN and motor are employed. Two lines of the LISN are placed between the power grid and drive system. 550V from a DC power supply is applied to the DC bus of the inverter from a DC power supply.

The achieved results before and after applying the cancellation windings are compared in Fig. 4.28. It can be seen that 2 ~ 8 dB improvements are achieved in the frequencies of above 6 MHz. Additionally, when comparing the LISN measurements with the network analyzer measurements (given in Fig. 4.23), the improvement is lower although the employed capacitors and cancellation windings are identical. The deviations are analyzed as follows:

1. Due to the circuit layout difference when performing two different types of experiments.

2. The noise source impedance difference into different testing environments, which is operated inverter driven motor system and a constant value of 50Ω provided by the network analyzer.

3. The difference of parasitic values resultant from the large- and small-signal also contributes to the difference.

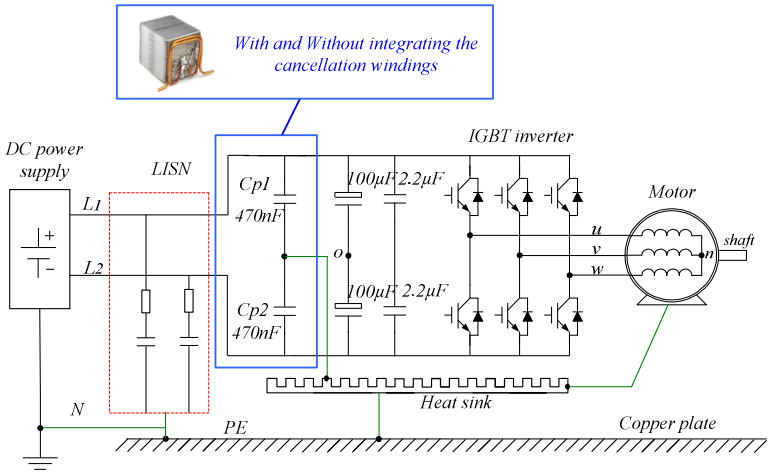


Fig. 4.27 Configuration of the motor drive system with the CM capacitors integrated with ESL cancellation windings

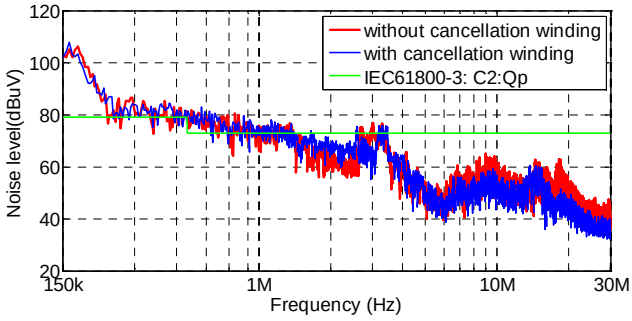


Fig. 4.28 Comparison of the LISN measured noise spectrums before and after applying the cancellation windings for the CM capacitors.

4.6 Conclusion

This chapter extends the parasitics cancellation techniques from 2D to 3D spatial layout for better EMI performance. The approaches utilize x dimensional components and the multi-layer PCB integration technology. A platform for 3D parasitics cancellations is provided. In the first part of this chapter, the previous cancellation techniques that are implemented in 2D are reviewed. Possibilities to extend them into 3D are analyzed. In single PCB technology, the cancellation techniques are strictly constrained in 2D spatial layouts. However 3D cancellation techniques effectively overcome these constrains. Better filtering performance can be achieved without increasing the size and cost of the filter. Applicable 3D cancellation techniques are discussed. Insertion losses measured from a network analyzer are used to verify the discussions. Finally, the proposed techniques are implemented into a LC filter for motor drives. Due to the complicated electromagnetic field distribution in the operating system, it is advisable, as the first step, to characterize parasitic effects that critically deteriorate the filter performance. Therefore techniques can be addressed on cancelling these parasitics.

Most researchers use small-signal measurements to evaluate the cancellation effects, because they are easier and more flexible to be performed than large-signal measurements done with a LISN. In this study both types of measurements are adopted. A better insight is provided. The LISN measurements show less improvement than that from a network analyzer. Both methods show the improved effects of the proposed methods. When comparing the effects of the self-parasitics cancellation and mutual coupling cancellation, the latter effort is proven to be more effective.

Chapter 5

Comparing and Improving EMC Performance in Si IGBT and SiC JFET Motor Drives

5.1 Introduction

With the IGBT based inverter as reference, this chapter discusses the reduction of conducted EMI to accommodate SiC JFETs in motor drives. The reasons why EMC performs in a certain way, and techniques to improve the EMI filter design for motor drives by replacing Si IGBTs with SiC JFETs, are presented. Two inverter prototypes – with SiC JFETs (SJEP120R100 normally-off) and Si IGBTs (IRG4PH40U) as the transistors are built using the same circuit layout and compared accordingly. Their different filter properties and requirements are analyzed and concluded.

The switching speed of SiC JFET can be two to six times higher [Hor06] than that of the conventional Si devices, leading the power converters switching frequency much higher. Furthermore, with SiC's blocking capability much higher than Si, higher power can be applied. Both factors significantly increase the EMI magnitude, an example is shown in Fig. 5.1. Fig. 5.1 (a) shows the measured EMI from the same VSD system that is operated under 1.55 kW and 450 W power levels. Fig. 5.1 (b) shows the same system that is operated under 16 kHz and 4 kHz switching conditions. 550V DC is applied to the DC bus when performing all the tests. A 2.2 kW motor is loaded. It can be seen that EMI is increased in the entire frequency range instead of at discrete frequencies. In specific circuit configurations, the high frequency noise level of a SiC JFET based motor drive system can be 20dB higher than that of a comparable Si IGBT based motor drive, with both systems driven by the same switching frequency, and utilizing identical EMI filters [Gon11]. As the conclusion, the EMC design has become more critical than ever, which is against many benefits obtained with the SiC transistors.

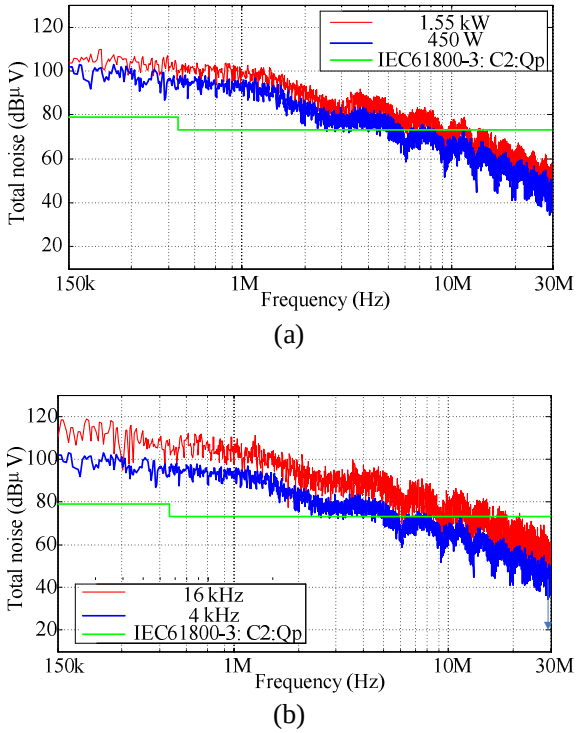


Fig. 5.1 Measured EMI from the VSD system under different power and switching frequency conditions

Additionally, the faster switching transient of SiC leads to a significantly higher voltage and/or current overshoot during the switching transients. With the increased high frequency contents, the influence of previously negligible circuit parasitics starts to play an increasing role in EMI production. Investigation shows that depending on the DC bus capacitance and layout design, parasitic oscillations that occur at SiC JFET switching transients can vary from 10 MHz to 100 MHz [Jos11a]. Even though all of the previous researchers conclude that SiC power devices increase the level of EMI noise, a quantitative understanding of the EMI source and differences in Si devices is still elusive. The questions to be asked is: whether the existing EMI filtering techniques need to be improved to accommodate SiC based motor drives.

In this chapter, both SiC JFET and Si IGBT inverters are implemented with discrete semiconductors with externally added diodes in anti-parallel attached to the heat sink (shown in Fig. 5.2). A 150μm thick polyimide layer is inserted between the semiconductor drain (cathode of diodes) and heat sink for electrical insulation. Their conducted EMI levels are measured without any EMI filter and subsequently compared to the levels obtained in the presence of two different CM filters. It is shown that different switching dv/dts result in different parasitic oscillations which significantly deteriorate the EMC performance. The oscillations are magnified to a greater extent in the SiC JFET system than that in Si IGBT's. Lastly, a solution based on inserting ferrite beads at different current paths is proposed to suppress the parasitic oscillations. Equivalent circuit modeling is used to predict the suppression effects. Respectively, the mid and high frequency noise of SiC JFET drive system are effectively suppressed to comply with the IEC61800-3-C2: Qp standard.

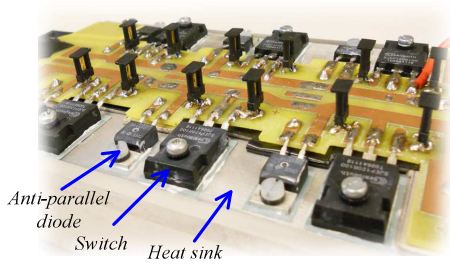
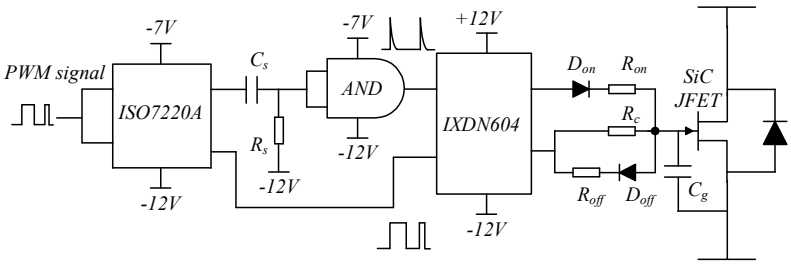


Fig. 5.2 Discrete transistor with external anti-parallel diodes are attached on top of the heat sink

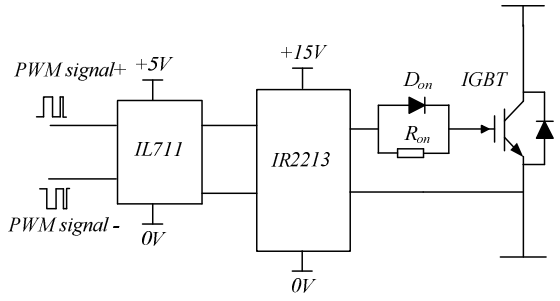
5.2 Comparison in inverter legs

5.2.1 Configuration of gate drivers

The schematics of the implemented gate drivers for the Si IGBTs and SiC JFETs are illustrated in Fig. 5.3 (a) and (b) respectively, where only the relevant components are shown. Although the employed two semiconductors (Si IGBT and SiC JFET) are both normally-off devices, their gate drivers are significantly different due to their physically structural differences [Onl10]. The gate driver designs accommodate different driving features as the priority. In addition, they also aim to create comparable switching conditions. Both gate drivers deliver signal through channels for turn-on and turn-off respectively. The turn-on channel exploit the switching speed of two different types of transistors, and the turn-off channel provides comparable conditions considering their gate discharges, which will be explained respectively in the following sections.



(a)



(b)

Fig. 5.3 Schematic diagrams of the implemented gate drivers (a) for SiC JFET (b) for IGBT

5.2.2 Turn-on of transistors

Because the equivalent structure between the gate and source of the SiC JFET is a p-n parasitic diode and parasitic capacitor in parallel connection (D_{g2} and C_{ss2} as shown in Fig. 5.5 (a)), the gate driver turn-on channel must meet three special requirements in order to fully exploit the SiC JFET fast switching.

- The gate driver must ensure a high peak current (3A in this case) at the beginning with the duration of typically 100ns in order to fast charge the parasitic gate-source capacitor C_{ss2} and miller capacitor. The current is delivered through diode D_{on} and resistor $R_{on.}$ The pulse current duration is set by values of C_s and R_s and the threshold voltage of the AND gate (74VIT). The peak current value is set by resistor $R_{on.}$ IC IXDN604 is chosen to ensure the high current delivery.

- After the current spike the gate driver must be able to deliver steady current and voltage to minimize the channel resistance over the specified temperature range. In order to increase the device channel width, the gate-source voltage V_{gs} should be around 1.5V higher than the gate threshold voltage of the JFET (typically $V_{gs(th)}$=1V). Due to the existence of the parasitic p-n diode in the gate-source structure, V_{gs} is determined by the forward characteristic of the parasitic diode. The delivered current is determined by a combination of forward characteristic of the parasitic diode and the added resistor R_c. The diode carries 2.5V voltage in the on state of the JFET, with 12V driver supplying voltage, and the resistor $R_c = 110\Omega$ in the path, the current is set to around $I_g = (12\,\mathrm{V} - 2.5\,\mathrm{V}) / 110\Omega = 85\,\mathrm{mA}$.

- The gate driver must have increased immunity to the excited overshoot and noise disturbance during the operations. Since the SiC JFET turn-on threshold voltage of 1.0 V is very low, a negative voltage of -12 V is applied in order to increase the turn-off safety margin. In Addition, because power supply pins of IXDN604 is very sensitive to the noise, the gate driver layout for SiC JFET must be optimized. The signal loops especially between the power supply and the chip must be minimized.

The output waveform of SiC JFET gate driver is illustrated in Fig. 5.4, where the 100ns pulse at the turn-on transient is shown.

Additionally, in order to prevent SiC JFET from faultily turn-on operations, an external capacitor C_g is added between the gate and source. Because SiC JFET has the much lower intrinsic gate to source capacitance, the impedance ratio from gate-source to drain-gate is relatively high. Due to the low threshold voltage, the current charged to the gate capacitor C_{ss2} through the miller capacitor during the fast switching transients may faultily turn-on the switch. The added capacitor C_{gs}=1nF reduces the turn-off impedance in order to prevent such problems.

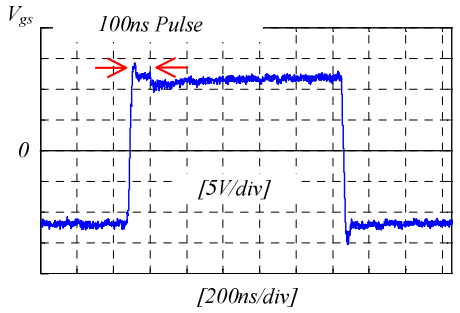


Fig. 5.4 Output voltage waveform of the SiC JFET gate driver

The equivalent structure between the gate and source of the IGBT is a parasitic capacitor with the value in order of C_{ss2} = 1782pF (shown in Fig. 5.5 (b)). Unlike with the SiC JFET, there is no equivalent parasitic p-n junction diode positioned forward biased from gate to source, therefore a steady and relatively low charge current (typically 40mA) is sufficient to charge the gate capacitor to keep it in on-state. Additionally, without the parallel diode at the gate the delivery of high spike current for driving SiC JFET is less important therefore there is no need for driving the IGBT switch. In order to decrease the turn-on time of the IGBT, a diode D_{on} is added in parallel with R_{on}. The charging current is limited by the equivalent series resistance of D_{on}.

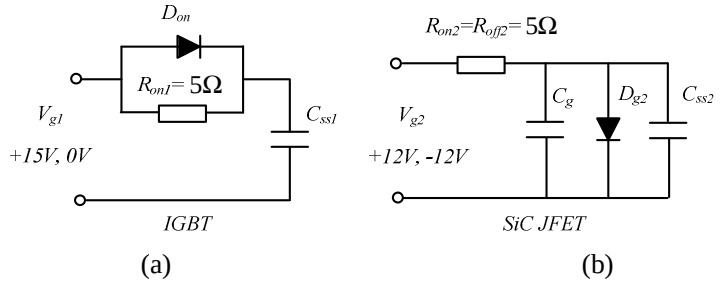


Fig. 5.5 Equivalent gate driving circuits (a) for IGBT (b) for SiC JFET

5.2.3 Turn-off of transistors

Comparable turn-off conditions are created for two types of transistors because:

- For SiC JFET, the applied driving voltage for turn-off is -12V, and the initial voltage over C_{ss2} at turn-off transient is +2.5V, therefore the voltage difference is V_{off1}=2.5V- (-12V) =14.5V. For IGBT, because the threshold gate is high (3.0V), the applied driving voltage for turn-off is 0V. The initial voltage over C_{ss1} at turn-off transient is +15V, therefore the voltage difference is V_{off2}=15V–0V=15V. Consequently the same voltage differences are created for turning off the two types of transistors.

- The same gate resistance R_{on1}=R_{on2}= 5Ω is applied.

- Because of the added external capacitor C_g, the gate-source capacitance of SiC JFET is increased from the intrinsic capacitance of C_{ss2}=711pF to C_{g2}=C_{ss2}+C_g=711pF+1nF=1711pF, which becomes comparable to the gate-source capacitance of IGBT (C_{ss1}=1782pF).

5.2.4 Inductive switching waveforms

The inductive switching waveforms are measured in the inverter bridge legs to compare the switching transients. The schematic diagram is shown in Fig. 5.6. The circuit layout is the same as used for three-phase inverter shown in Fig. 5.12 (a). The external freewheeling diodes – C2D05120A and ISL9R18120P are added in anti-parallel to each SiC JFET and IGBT respectively. SiC and Si diodes are used for two types of power devices to comply with actual situations. The switches S_1 and S_2 represent either an IGBT or SiC JEFT. The upper switch S_1 is clamped in off state while the lower switch S_2 is driven by pulse signals. A 800µH inductive load is connected between DC- bus and the drain of S_2. The measured waveforms are illustrated in Fig. 5.7, where V_{ds} is the voltage between the switch drain and source, I_g is measured between the heat sink and earth, and I_{ds} is the current flowing through the switch channel from drain to source. These measured points are indicated in Fig. 5.6.

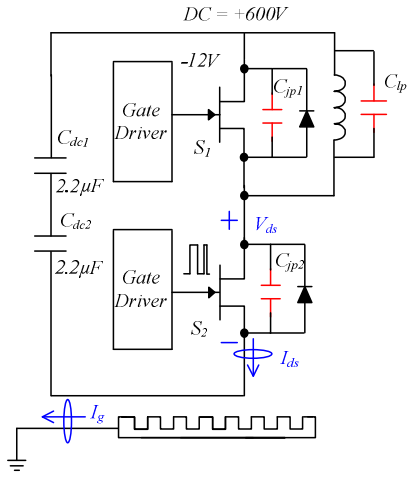


Fig. 5.6 Inverter bridge leg for inductive switching transients comparison of two transistors

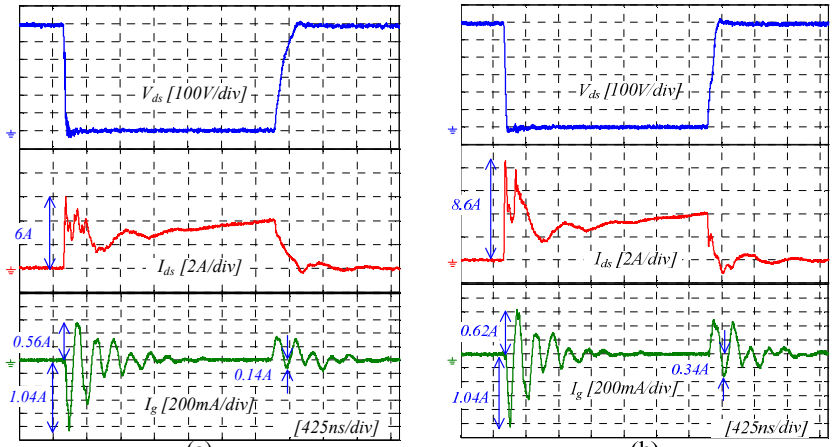


Fig. 5.7 Comparison of two semiconductors' switching transients (a) IGBT (b) SiC JFET

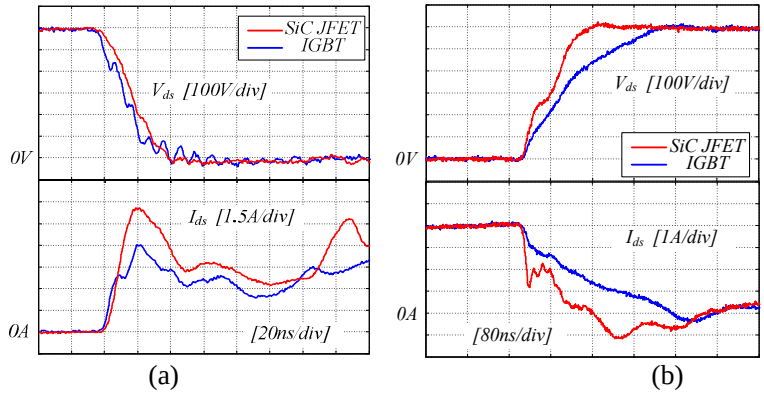


Fig. 5.8 Comparison of the SiC JFET and IGBT voltage and current switching transients in expanded scale (a) turn-on (b) turn-off

Fig. 5.8 shows DM switching transients in expanded scale. It can be seen that at turn-on transient, the switching dv/dt of SiC JFET is a little higher than that of IGBT (16.67kV/μs versus 15kV/μs), however for SiC JFET the DM current overshoot is much higher which results in the di/dt values being much higher (430A/μs versus 300A/μs). These will predominantly contribute to the high frequency contents in the spectrum. At turn-off transient (Fig. 5.8 (b)), SiC JFET is switching more than twice faster than IGBT (4.62kV/μs versus 2.07kV/μs), which excites a lower current overshoot than that at the turn-on transition. The reasons are analyzed as follows:

The DM overshoot is determined by the value of switching dv/dt, the on-resistance in the switch channel, and the equivalent capacitance in parallel to the upper switch (C_{jp1}, shown in Fig. 5.6), while the oscillation frequencies are mainly determined by the parasitic inductance and capacitance in the circuit layout. Since the SiC JFET and Si IGBT turn on within more or less the same time, their dv/dts are the same. Additionally, since the same load is used, the

equivalent parallel capacitance C_{lp} is also the same. Therefore C_{jp1} and on-resistance of the switch are the only components that differentiate the overshoot magnitude. C_{jp1} of two transistors are more or less the same. With on-resistance being much lower than that of IGBT, the SiC JFET current overshoot is also higher. C_{jp1} and C_{jp2} come from two sources: 1) the intrinsic parasitic drain-source capacitance of the switch plus the junction capacitance of the added diodes. 2) the equivalently added capacitance from the external circuits (e.g. parasitic capacitance from upper switch drain plate to the heat sink and from the heat sink back to the lower switch drain plate). The low frequency oscillations are determined by the circuit parasitic inductance and load parasitic capacitance C_{lp}.

However, the resulting CM current is more or less the same. Because CM impedance mainly depends on the circuit layout. Since the two inverters are constructed using the same layout and connected to the same load, and since the same packages are selected for the two transistors and anti-parallel diodes respectively, the CM impedance is also the same. The only difference exists between the switch die and the Aluminum base plate, inside the device package.

The performed inductive switching test indicates that the main difference in the spectra of the two transistors will be in DM. Big overshoot magnitude difference and small oscillation difference indicate that the differences will be experienced mainly at high frequencies.

5.2.5 Noise source analysis

Next, based on the inductive switching performance, differences between SiC JFET and IGBT sources are analyzed and calculated using Fast Fourier Transform (FFT). In the motor drive system, the dominant CM noise is regarded as being voltage sourced because of the existing valley in the load impedance. The voltage is between the neutral point of the inverter output and the earth. The dominant DM noise is regarded as being current sourced because suppression of low frequency harmonics is critical for DM filters. Therefore the voltage dv/dts dominant the CM noise magnitude. The current di/dt dominants the DM noise magnitude.

To analyze the difference, the influence from switching dv/dts is calculated using FFT. It is shown from Fig. 5.8 that SiC JFET is switching over two times faster than IGBT at the turn-off transition while their dv/dts at turn-on is almost the same. Their spectra are calculated with different turn-off dv/dt values. The same turn-on dv/dt (15kV/µs) is applied. The results are shown in Fig. 5.9. It can be seen that small difference exists. Pure square voltage waveforms without considering parasitic oscillations are used for calculation. Fig. 5.10 shows the calculated the noise source magnitude based on the measured voltage switching waveforms of Fig. 5.8. The resulted spectra are very similar. A noise spike appearing at 8 MHz in the SiC JFET spectrum is due to the resonance at turn-off voltage slope that is originated from the current oscillations. Therefore it can be expected that the emitted CM noise from two types of transistor sources will be similar.

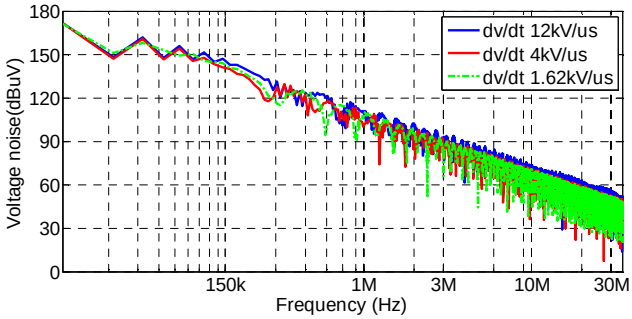


Fig. 5.9 Calculated DM noise source emissions based on different turn-off dv/dts

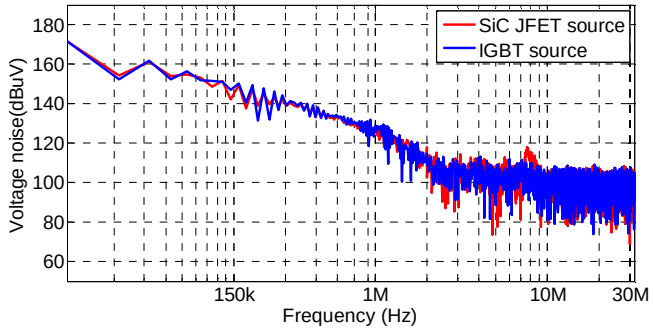
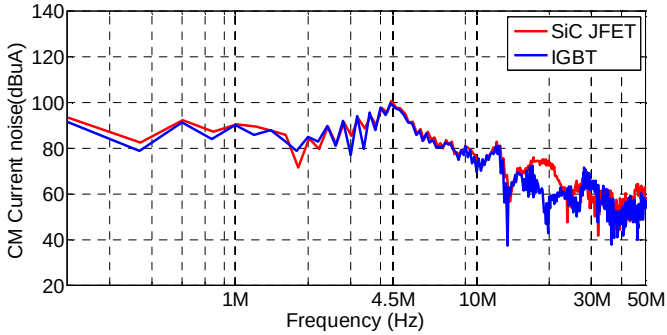
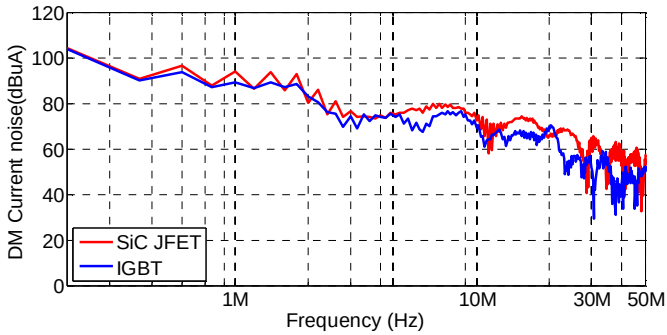


Fig. 5.10 Measured DM noise source emissions based on FFT transformation

Secondly, the influence of switching di/dts is calculated. The CM and DM current noise spectra are transferred from the measured CM and DM current transient waveforms of Fig. 5.8 and shown in Fig. 5.11 (a) and (b) respectively. As can be seen from Fig. 5.11 (a), the CM current noise levels from two systems are very similar. The noise spike at 4.5 MHz corresponds to the main oscillation frequency in the CM currents. An average of 8dB difference exists in DM spectra from the whole of the frequency range beyond 5 MHz. It can be seen that the noise level difference and resonant frequencies are nonlinear to as to associate with time-domain waveforms (8.6A as opposed to 6A at 18 MHz as shown in Fig. 5.8). Therefore it is concluded that parasitic oscillations with faster SiC switching will increase noise level over a broad high frequency range rather than at discrete frequencies.



(a)



(b)

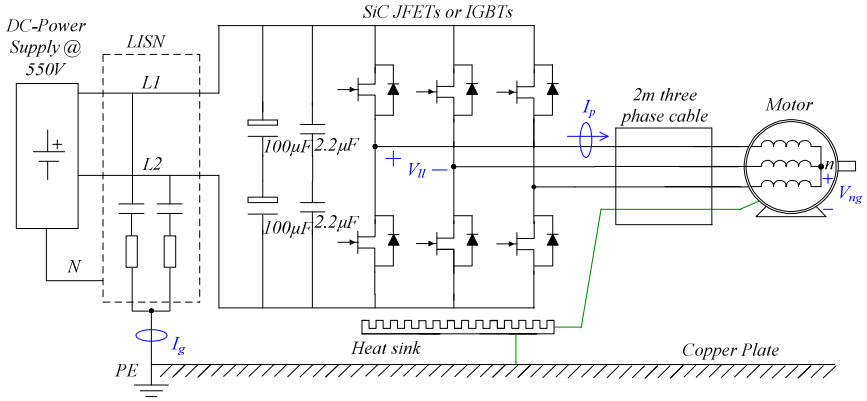
Fig. 5.11 Measured current noise spectra from SiC JFET and IGBT inductive switching test (a) for CM (b) for DM

5.3 EMI Comparison and analysis in three phase systems

5.3.1 Experiment configuration

Next, their EMI spectra of three phase drive systems are measured. Photographs of the implemented inverter layouts are presented in Fig. 5.12 (a). The gate drivers are placed on top of the power board. The experiment configuration of EMI measurements for both of the two drive systems is illustrated in Fig. 5.12 (b). The two inverters are powered by a DC power supply at 550V DC through a LISN (Cranage VN3-100S). A 2.2 kW induction motor is driven at 50Hz modulation frequency. The inverter switching frequency is set to 16 kHz by programming the driving signal source from a DSP. The inverter and motor are grounded to the same copper plate. The EMC spectrum analyzer is set for 9 kHz resolution bandwidth and 18s sweep time. The two inverters are placed in the same experimental environment with the same measuring equipment.

(a)

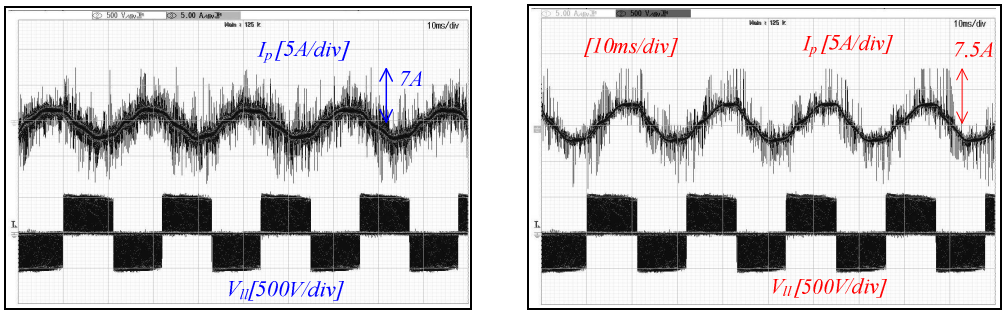


(b)

Fig. 5.12 Experiment configuration of two motor drive systems under comparison (a) layout comparison (b) system configuration

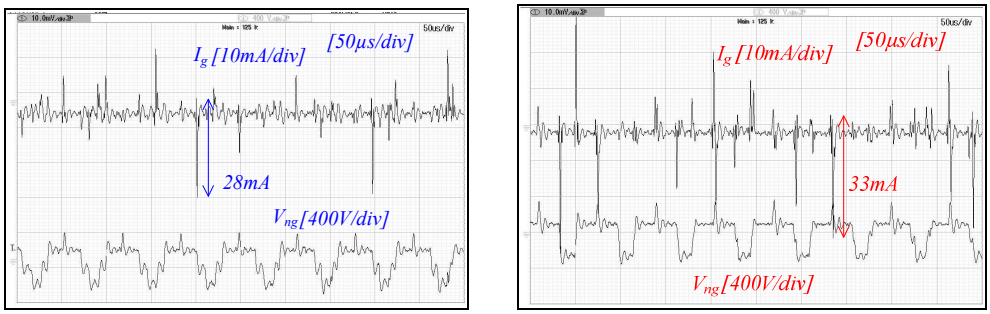
5.3.2 Waveforms without filter

The electrical waveforms of the SiC and Si devices are compared with the inverters running in the three-phase. The configuration is shown in Fig. 5.12. For DM performance, the motor phase current I_p and inverter output line-to-line voltage V_{ll} are measured and shown in Fig. 5.13. For CM performance, the CM current I_g flowing through LISN and CM voltage between motor neutral point and earth V_{ng} are measured and shown in Fig. 5.14. The measured points are indicated in Fig. 5.12. It can be seen that although no significant difference exist between the DM current overshoot magnitude (7.5A as opposite to 7A), large differences exist in spike quantities. The amplitude difference becomes more evident when their CM waveforms are compared (33mA as opposed to 28mA). Those experimental results correspond well with the measurements obtained in the single-phase of the inductive switching test.



(a) (b)

Fig. 5.13 Comparison of DM waveforms of two motor drive systems (a) IGBTs based (b) SiC JFETs based



(a) (b)

Fig. 5.14 Comparison of CM waveforms of two motor drive systems (a) IGBTs based (b) SiC JFETs based

5.3.3 Measured EMI without filter

Fig. 5.12 illustrates the configuration that has the least filtering components and only four DC capacitors – two electrolytic capacitors and two film 2.2µF capacitors placed in the DC bus. This configuration is defined as the case without filter. It is necessary to keep the two inverter heat sinks grounded for the following reasons:

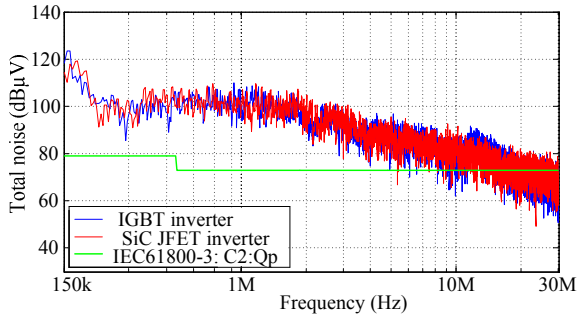
1. To meet the safety requirement because the heat sink is usually integrated with the inverter frame.

2. To include the path between the switch drains and the heat sink hence the noise propagation paths of the two inverters are kept the same [Gon10].

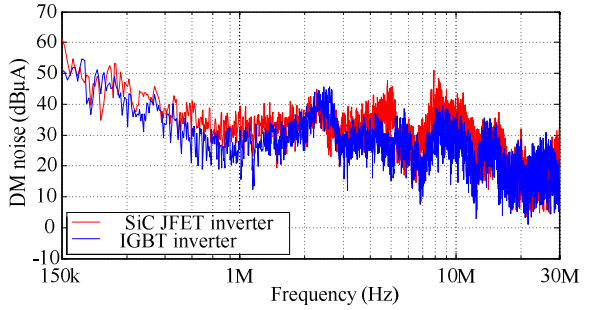
The DM and CM noise are separated by the current probes (Fischer F-75) according to the methods described in [Zha06].

The EMI comparisons of total, DM and CM spectra without filter are illustrated in Fig. 5.15 (a), (b) and (c) respectively. The main difference is found in the DM noise spectrum where the SiC inverter is higher over the frequency range between 3 MHz to 15 MHz. This is because of

the higher DM current overshoot and oscillations excited by the faster SiC switching. The total and CM noise are similar, which agrees with calculations as shown in Fig. 5.10. Measured noise spectra correspond well with the predictions reached by the previous analysis and with predictions during the inductive switching test.



(a)



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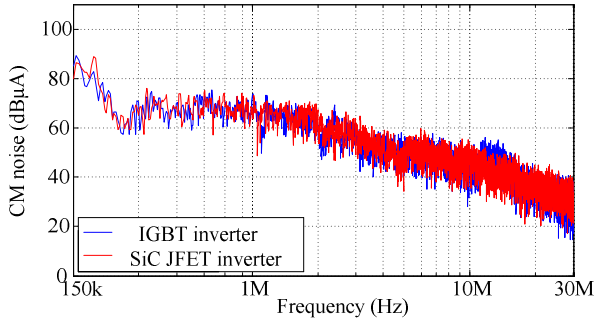


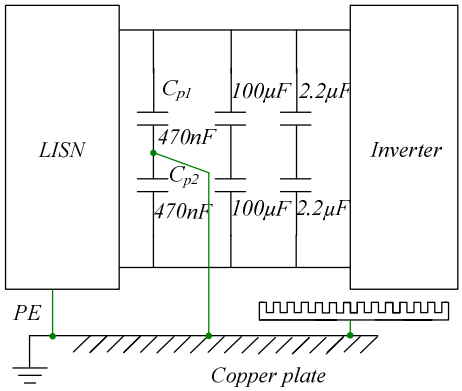
(c)

Fig. 5.15 Comparison of measured EMI spectra in two motor drive systems with no filter (a) total (b) DM (c) CM

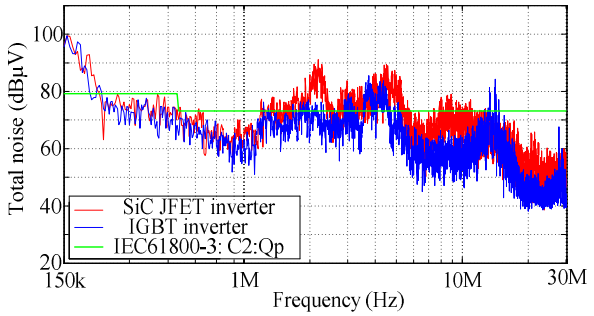
5.3.4 Measured EMI with CM filters

Secondly, their EMI spectra are compared while using C and LC CM filters. The comparison of the measured total, CM and DM EMI spectra with the identical C (470nF) CM filter are

illustrated in Fig. 5.16 (b), (c) and (d) respectively. Fig. 5.16 (a) shows the schematic diagram of the applied filter. It can be seen that both the CM and DM current noise is reduced, when compared to the unfiltered case. Even though the filter is intended for the CM current, it is also found in the DM current. Unexpectedly, the EMI level differences become much more obvious which means that attenuation of the identical filter is different for the two systems.



(a)



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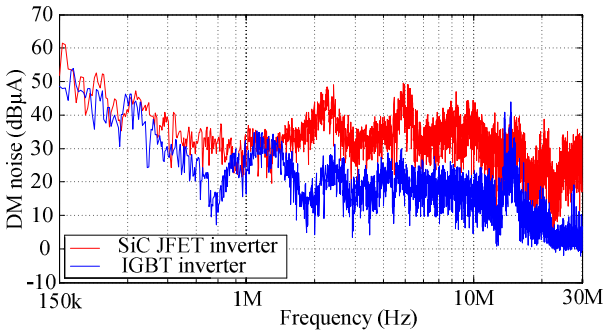
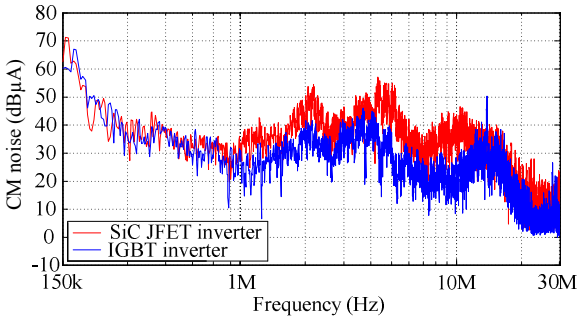


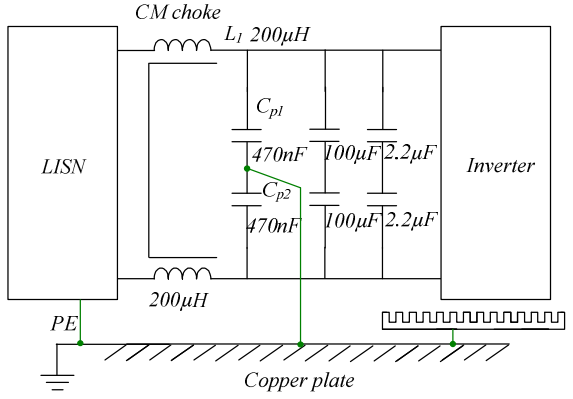
(c)



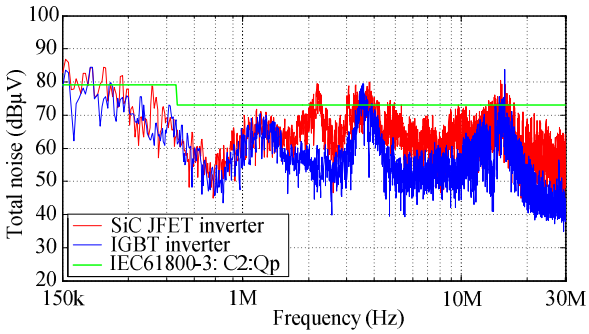
(d)

Fig. 5.16 Comparison of measured EMI spectra in two motor drive systems with 470nF CM filter (a) schematic diagram (b) total (c) CM (d) DM

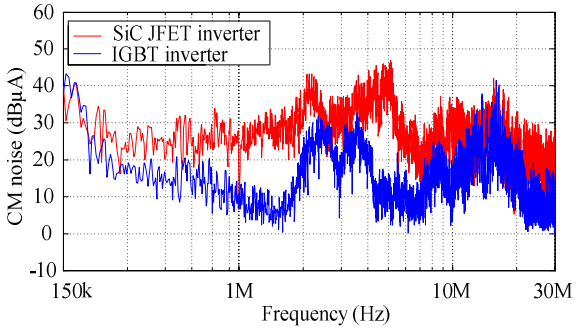
Next, a 200μH CM choke is added in front of the CM capacitors to compose the LC filter, the schematic diagram is shown in Fig. 5.17 (a). The inductor value is not specially selected but obtained empirically and used as the initial design. A comparison of the measured total, CM and DM EMI spectra is given in Fig. 5.17 (b), (c), and (d) respectively. It can be seen that in addition to the results with the purely capacitive filter (given in Fig. 5.16), the difference becomes higher at frequencies above 2 MHz. The noise of SiC JFET inverter is 10dB more than that of the IGBT. Compared to the previous results, the increased differences in the EMI levels of SiC JFET drive system are much higher than those of IGBT drive system.



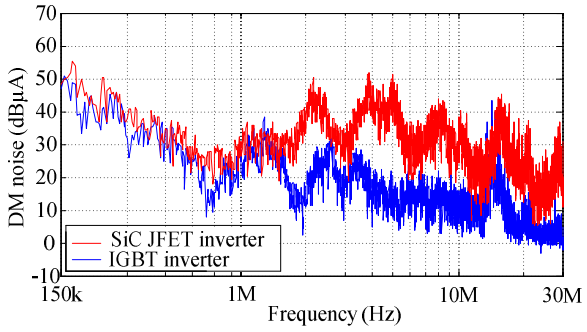
(a)



(b)



(c)



(d)

Fig. 5.17 Comparison of measured EMI spectra in two motor drive systems with 200μH 470nF LC CM filter (a) schematic diagram (b) total (c) CM (d) DM

Several conclusions can be drawn from the above experiments:

- The traditional EMI filter design for Si based motor drive systems can also be applied for the SiC JFET drive system, however more efforts must be addressed on performance at high frequencies, which is because of the increased EMI level due to the higher current and voltage overshoots caused by the SiC's faster switching speed.

- CM noise is dominant and determined by turn-on dv/dts and CM parasitic capacitance. Since the two parameters are the same for two systems, the CM and total EMI levels are similar.

- The parasitic oscillations occurring with switching transients increase the noise level over a broad frequency range rather than at discrete frequencies.

- The identical filters for two systems results in different attenuations. Although the obtained EMI levels are very similar without filter, differences become significantly obvious after applying the identical filters. This phenomenon will be focused on and analyzed in the following sections.

5.4 Filtering performance analysis and verification

5.4.1 Inverter CM test mode

In order to easily identify the CM and DM current waveform differences, two inverters are set under the mode in which three upper or lower switches are switched on or off simultaneously at a fixed 50% duty ratio. This is defined as the inverter CM test mode because CM noise is the largest. In this case no functional current flows in the system. The three poles of the inverter are set to be switched at the same time. The overlaps cause the CM current amplitude to be three times higher. Consequently the CM currents and the mixed DM currents that are superimposed by CM are maximized. Thus differences can be easily recognized in time-domain waveforms.

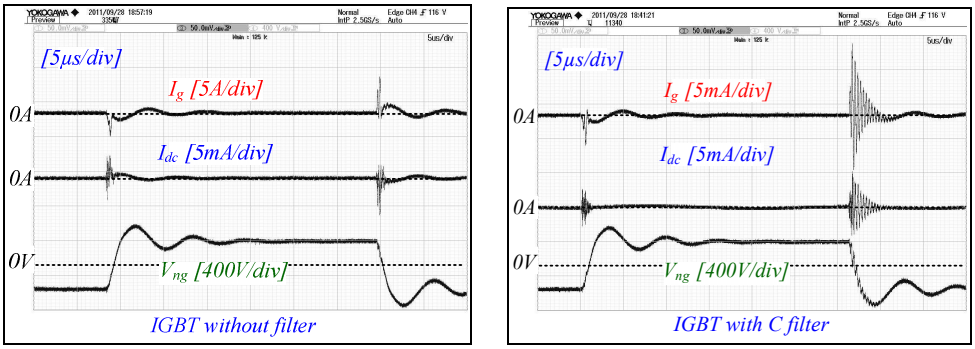
The switching frequency remains 16 kHz. The same motor remains being loaded to the inverters.

5.4.2 Parasitic oscillations

It is found that different parasitic oscillations result in different noise emissions. Hence the differences over the broad frequency range are further increased. When there is no filter, the emitted noise is distributed over the conducted frequency range. The main difference in DM results is the small difference in total EMI spectrum. To create the noise shunting path, two Y capacitors are added as the first filtering stage. Although the low frequency noise is effectively suppressed, the increased capacitance excites different high frequency current oscillations in the two systems. The SiC JFET inverter is magnified further due to the faster SiC switching speed. This is reflected by the increased spikes in the spectra (See Fig. 5.16 (b) and Fig. 5.17 (b)). The frequencies of the spikes correspond to the frequencies of the excited parasitic oscillations.

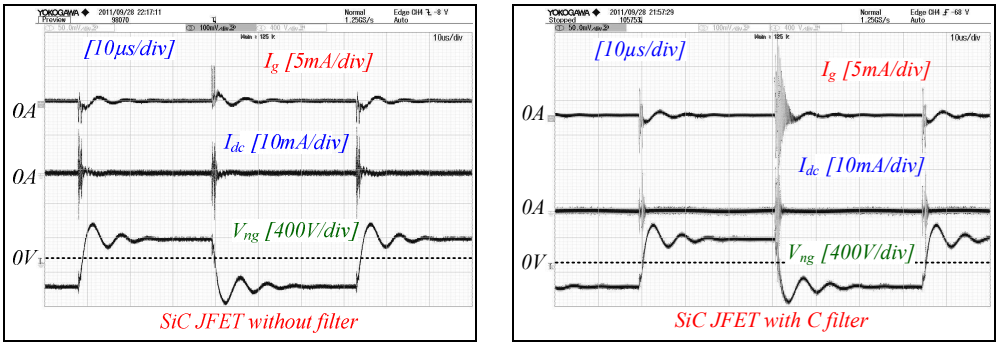
Fig. 5.18 and Fig. 5.19 compare the excited current oscillations before and after adding the 470nF CM capacitors for the inverter systems of IGBT and SiC JFET, respectively, where I_g is measured from earth flowing into LISN, I_{dc} is the DM current measured flowing from LISN to inverter DC bus, V_{ng} is the voltage measured between the motor winding neutral point and earth. It can be seen that the added filter capacitors magnify the parasitic oscillations of both of the

IGBT and SiC JFET switching transients. This is due to the oscillations among the components at input, which is parasitics in the input cable, parasitics in the filter inductor, and parasitics in the filter capacitors. Those parasitics together with the LISN form the noise propagation loop at the input side. It can be seen that oscillations at turn-off are higher than at turn-on. Noise in the mid and high frequency range is significantly increased.



(a) (b)

Fig. 5.18 Comparison of measured CM and DM currents of IGBT system under CM test mode (a) without filter (b) with 470nF C filter

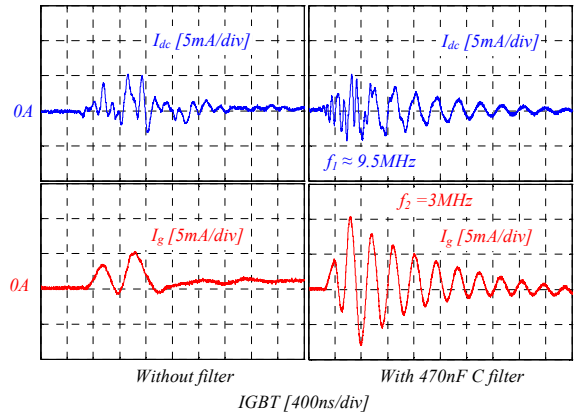


(a) (b)

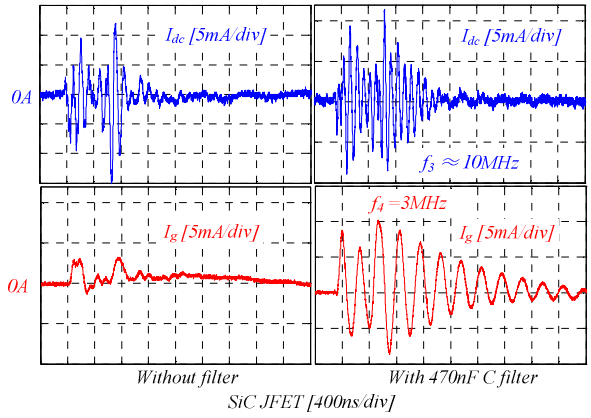
Fig. 5.19 Comparison of measured CM and DM currents of SiC JFET system waveforms under CM test mode (a) without filter (b) with 470nF C filter

The DM (I_{dc}) and CM (I_g) current oscillations at the switching-off transients of both SiC JFET and Si IGBT inverters are magnified and shown in expanded scale of Fig. 5.20. It can be seen that the CM currents (I_g) are oscillating in the mid frequency range (around 3 MHz), and the DM currents (I_{dc}, excluding the superimposed CM current) oscillate in the high frequency

range (beyond 8 MHz). The DM currents contain the same oscillation frequency (3 MHz) that is superimposed by the CM contents.



(a)



(b)

Fig. 5.20 Parasitic oscillations in expanded scale (a) I_g and I_{dc} during the turn-off transient of IGBT (b) I_g and I_{dc} during the turn-off transient of SiC JFET

5.4.3 Increased parasitic oscillations

Fig. 5.21 illustrates a DM current flowing path and parasitics that generate the DM oscillations in an inverter leg. Switch S_1 is either an IGBT or a SiC JFET. L_{dc}, $L_{db1,2}$ are parasitic inductance in the DC capacitor and DC bus respectively, and I_{dc} is the DM current flowing through the switch S_1. At turn-on transient of S_1, voltage across C_{jp1} is $V_{dc}/2 = 275V$. The discharge current of C_{jp1} circulates through the switch S_1 then back to itself. Therefore no resonance occurs between C_{jp1} and external inductors. At turn-off transient, energy stored in C_{jp1} is zero. Energy in the inductors L_{dc} and L_{db1} is full. Therefore the three parasitic components start resonating at their natural frequency $f = 1/2 \cdot \pi \sqrt{L \cdot C}$, where $L = L_{dc} + L_{db1}$, $C = C_{jp1}$. Therefore the parasitic oscillation magnitude at turn-off transient is higher than that at

turn-on transient. According to formula $i = C \cdot dv/dt$, the current overshoot magnitude is determined by the turn-off speed of the switch S_1. At turn-off transient, SiC JFET is switching more than twice faster than IGBT, therefore the generated current overshoot magnitude is higher. The oscillation frequency of SiC JFET is a little higher due to the lower parasitic capacitance, which is also seen in the inductive switching test.

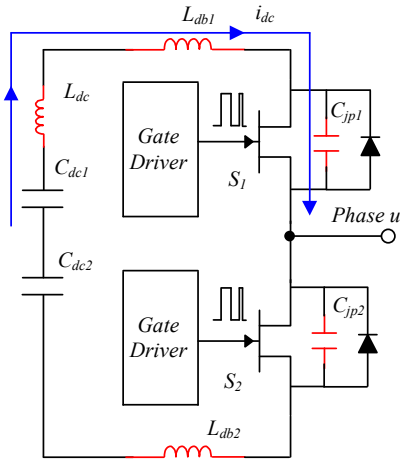
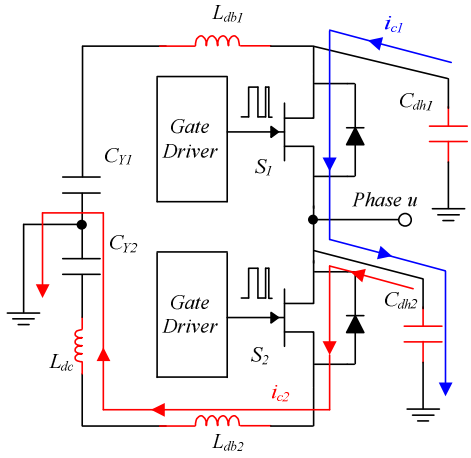


Fig. 5.21 DM current flowing path in inverter leg

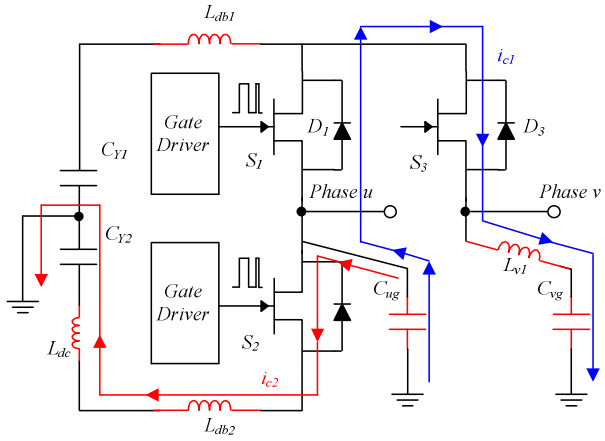
Fig. 5.22 illustrates two cases of CM current flowing paths in an inverter leg, i_{c1} and i_{c2}. C_{Y1} and C_{Y2} are CM capacitors. Fig. 5.22 (a) considers the parasitic capacitors between switch drains and the heat sink. C_{dh1} is the summed parasitic capacitance of the capacitor between the upper switch (S_1) drain plate and heat sink plate, and the one the between upper power diode cathode plate and heat sink plate. C_{dh2} is the capacitance of lower switch (S_2) and lower power diode. At turn-on transition of S_1, current i_{c1} is discharged from capacitor C_{dh1} via S_1 to C_{dh2}. The loop is small. When S_1 is turned off, and S_2 is turned on, current i_{c2} is discharged from C_{dh2} via parasitic inductors L_{db2} and L_{dc} to C_{Y2}. Therefore a much larger loop is formed. The three parasitic components start resonating at their natural frequency $f = 1/2 \cdot \pi\sqrt{L \cdot C}$, where $L=L_{dc}+L_{db2}$, $C=C_{dh2.}$ The addition of C_{Y2} increases the oscillation energy. Therefore the parasitic oscillation magnitude at S_1 turn-off transient is also higher than that at its turn-on transient.

Fig. 5.22 (b) considers the parasitic capacitors between inverter phases and the ground. C_{ug} is summed capacitance between phase u and ground, C_{vg} is the summed capacitance between phase v and ground, and L_{v1} is the parasitic inductance in the flowing path of i_{c1}. At turn-on transient of S_3, current i_{c1} is discharged from C_{ug} via upper diode D_1 and parasitic inductors L_{v1} to capacitor C_{vg}. The loop is small. When S_1 and S_3 are turned off, and S_2 is turned on, current i_{c2} is discharged from C_{ug} via parasitic inductors L_{db2} and L_{dc} to C_{Y2}. Therefore a much larger loop is formed. Three parasitic components C_{ug}, L_{dc} and L_{db2} create the oscillation frequency. Therefore the parasitic oscillation magnitude at S_1 turn-off transient is also higher than that at its turn-on transient. Because CM parasitic values are similar between two types of inverters,

therefore CM parasitic oscillation frequencies are also similar. Higher overshoot is generated in SiC JFET inverter due to the faster switching speed.



(a)



(b)

Fig. 5.22 CM current flowing paths in inverter leg (a) considering parasitic capacitors between switch drain and heat sink (grounded) (b) considering parasitic capacitors between phase and ground

5.4.4 CM superimposed on DM

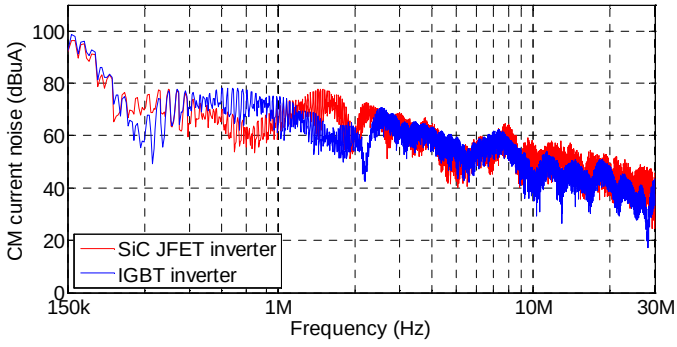
As can be seen from Fig. 5.20, the increased CM parasitic oscillations are also experienced by the DM. Therefore the superposition of the two components further contributes to the attenuation difference.

In motor drive systems, CM noise is usually assumed to be evenly distributed among the inverter phases. Therefore the CM currents distributed in each phase cancel each other out and do not contribute to the DM contents (when measured using the procedure outlined in [Zha06]). However in actual situation it is nearly impossible to completely avoid the phase asymmetry,

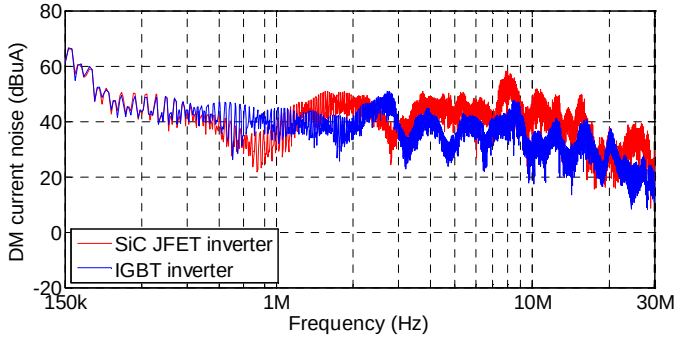
which means the DM contents also contain CM. This is why it is shown in the noise spectra that some CM and DM spikes appear at the same frequencies, and why those CM and DM spikes are increased and decreased simultaneously before and after adding the filter (shown in Fig. 5.16 and Fig. 5.17). Since in SiC JFET inverter system the magnitude of parasitic oscillations after adding filters are higher in both CM and DM, the resulting differences in the total spectra are further increased.

5.4.5 Measured EMI spectra of CM test mode

The DM and CM EMI spectra of the two types of inverters under CM test mode in unfiltered and C filtered conditions are illustrated in Fig. 5.23 and Fig. 5.24 respectively. It can be seen that without filter, emitted noise is flatly distributed over the spectrum, and the EMI levels from the two inverter systems are very similar. After adding the filter capacitor, the magnified parasitic oscillations result in numerous spikes in the spectrum, and the EMI levels of the SiC JFET system become much higher (10dB at most) than those of the IGBT's in the high frequency range (above 10 MHz). In addition, the SiC JFET system presents three spikes in the mid frequency range (2 MHz ~ 5 MHz) of the spectrum rather than one spike appearing in that of IGBT's. However, both of them present a noise spike at 8.5 MHz in the spectrum. These frequency-domain measurements agree well with the CM and DM parasitic oscillations measured in time-domain as shown in Fig. 5.20. Once again the identical filter exhibits different attenuation levels for the two systems. The main differences appear in the mid and high frequency ranges, where the CM and DM parasitic oscillations occur. Additionally, after adding C filter the DM noise becomes dominant, which results in inherent DM differences in high frequencies becoming more obvious, comparing Fig. 5.23 (b) and Fig. 5.24 (b).

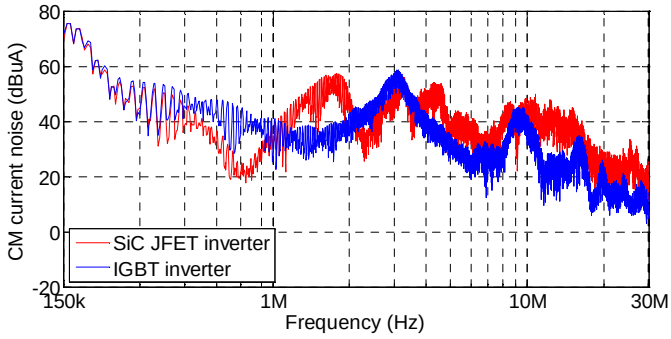


(a)

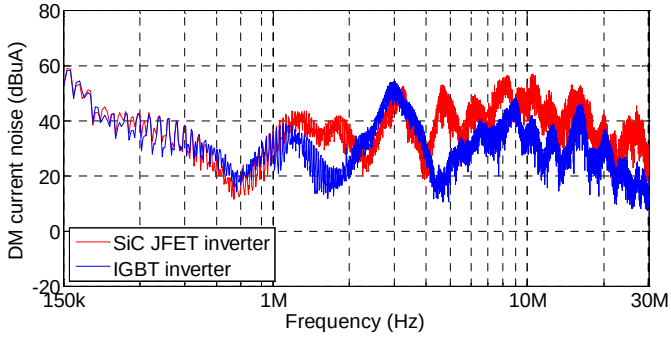


(b)

Fig. 5.23 Measured EMI spectra of two inverter systems under CM test mode without filter for both systems (a) CM (b) DM



(a)



(b)

Fig. 5.24 Measured EMI spectra of two inverter systems under CM test mode, with 470nF CM filters for both systems (a) CM (b) DM

5.4.6 Other causes

Since the EMI magnitude depends logarithmically on the ratio of voltage/current, the same amount of the emitted voltage/current difference causes different levels in the spectrum when

the noise bases are at different levels. For example, a 10mV noise voltage across the LISN results in 80dBµV in the spectrum, whereas 1mV results in 60dBµV. When there is no filter, the EMI levels in both drive systems are mostly higher than 80dBµV (see Fig. 5.15 (a)), which means the noise bases are higher than 10mV. The EMI difference that usually exists in DM spectrum can not be observed in the total noise spectrum. When the C filter is added, most of EMI in IGBT drive system is suppressed to below 70dBµV (see Fig. 5.16 (b)), which means that on average the noise bases are reduced to 3.15mV and lower. As the result, a relatively small voltage/current difference will cause a significant difference in the spectrum. Therefore the existing differences in the DM become more evident.

Up to now, the filtering performances of the two types of drive systems have been investigated. The reasons for obtaining different attenuation levels with the identical filters for the two inverter systems are summarized as follows:

- The filter shunting capacitors close to the switches magnify the current overshoots and oscillations, resulting in the noise at the parasitic oscillation frequencies being filtered much less than at the other frequency ranges. The parasitic oscillations are magnified more in SiC JFET system than in IGBT system mainly because of different switching speeds.

- In actual situations, the CM currents are superimposed on the DM currents due to the asymmetry of the system. Therefore in CM and DM spectra, the EMI spikes at the same frequencies are increased and reduced simultaneously with applied CM filters.

- At certain high frequencies, the DM noise, rather than the CM noise, becomes dominant. Therefore after the CM noise filtered, the DM noise level of SiC JFET system that is originally higher than that of IGBT system becomes more obvious.

5.5 Suppression of the parasitic oscillations

5.5.1 Modeling of CM current spectra

From this section, equivalent circuit modeling and FFT analysis are performed with the aim of improving filter design for the SiC JFET system. Fig. 5.25 illustrates the established model that includes the detailed parasitic elements. E is the CM noise source. I_1 is the CM noise current that is received by the LISN. The elements extraction method follows the procedure outlined in Chapter 3, excepting for the model of motor with cables, where L_{o1}, C_{o1}, L_{o2} and C_{o2} represent a two-cell network of the motor cable, the motor model applies a simplified version. Fig. 5.26 compares the CM impedance-frequency characteristic of the motor with cables with measured and calculated results. Compared to the results obtained from Chapter 3, the accuracy is degraded at the low frequency resonant corner at about 200 kHz. Because SiC JFET system mainly concerns high frequencies, the model shows enough accuracy and is regarded as reliable for the spectrum prediction.

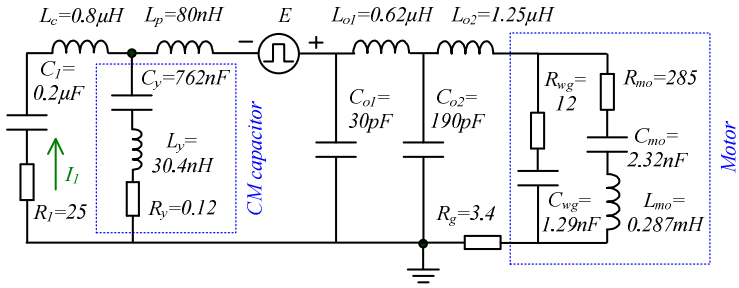


Fig. 5.25 Equivalent circuit model of the drive system for CM current spectra

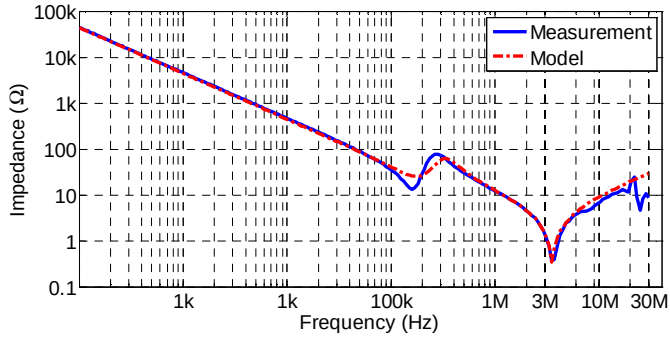
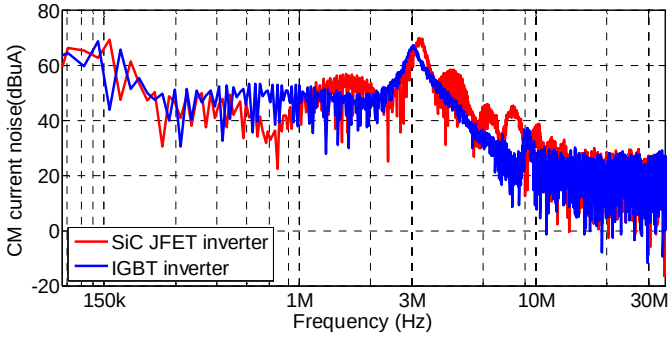
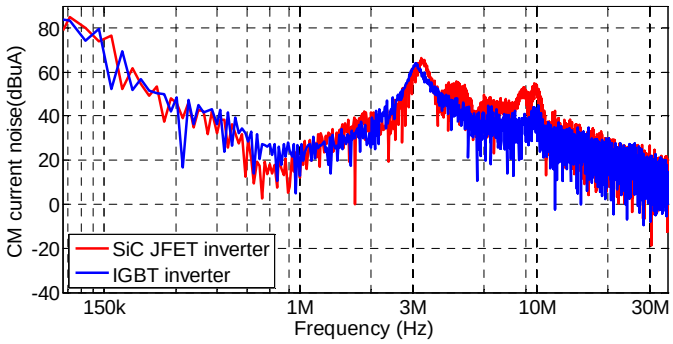


Fig. 5.26 Comparison of the CM impedance-frequency characteristic of the motor with cables between measured and modeled results

To verify the model the calculated noise spectra of CM current (I_1 in Fig. 5.25) is compared with the Fourier Transform of the time domain measurements. Fig. 5.27 (a) shows the Fourier Transform of the measured I_g (shown in Fig. 5.12). Fig. 5.27 (b) shows Fourier Transform of the calculated I_1 (shown in Fig. 5.25) in the model. Noise source E in the model is the Fourier Transform of time domain measurement of the voltage between neutral point of motor windings and chassis (V_{ng} as shown in Fig. 5.12). It can be seen that the two results agree well with each other. Hence the proposed model is reliable for CM spectrum predictions.



(a)



(b)

Fig. 5.27 Calculated CM current noise spectra of SiC JFET and IGBT motor drive systems under the CM test mode, with C filter for both cases (a) based on measurement (b) based on the model

The modeled CM current noise spectrum of SiC JFET motor drive system with the applied LC filter (given in Fig. 5.17 (a)) is shown in Fig. 5.28. The high frequency resonance occurring at 18 MHz is because of the presence of stray capacitance C_{o2} in the circuit model of the cable.

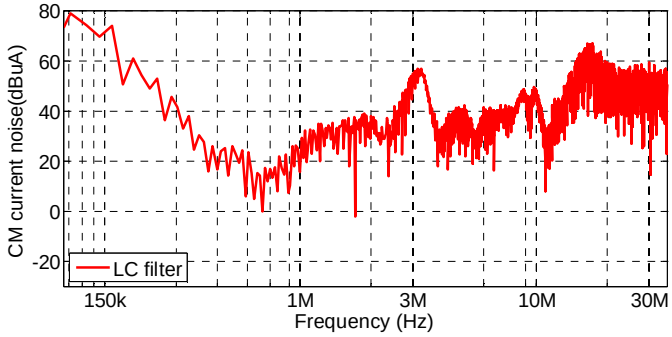


Fig. 5.28 Modeled CM current noise spectrum of the SiC JFET motor drive system with LC filter

5.5.2 Suppression of parasitic oscillations

The experimental results show that both of the CM and the DM parasitic oscillations are magnified more in the SiC JFET drive system than in the IGBT's. The applied filtering components must present high frequency blocking ability in order to suppress the parasitic oscillations as can be observed in Fig. 5.20. Consequently, the solution of inserting ferrite beads (ZCAT3035 TDK) at two different current flowing paths is proposed. The equivalent circuit of the ferrite bead is a series connection of a frequency dependent resistor and inductor, which is very effective in damping and dissipating the high frequency oscillations.

It is shown in Fig. 5.20 that the CM currents are oscillating in the mid frequency range of around 3 MHz and the DM currents are oscillating at the high frequency range of beyond 8 MHz. DM parasitic oscillations are observed in the DC bus, while the inductance in the current flowing path, and the capacitance between motor windings and chassis create a CM impedance

valley. Accordingly, two insert positions – the inverter DC bus and output phases (shown as position 1 and 2 respectively in Fig. 5.29) are specified to suppress the oscillations.

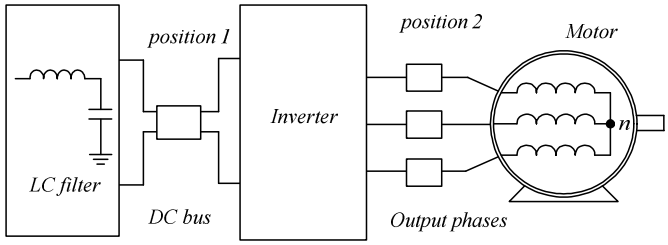


Fig. 5.29 Insert of ferrite beads to suppress the parasitic oscillations

5.5.3 Selection of ferrite beads

To perform an effective parasitics damping, several conditions need to be met when selecting the ferrite bead:

- The cross section area of the ferrite tube must be large enough so that the current carried by the bead will not cause saturation. With the selected bead the maximum current is 12.9A which is sufficiently larger than the current flowing in the DC bus.

- The impedance should be such that $R_s > Z_l$ at the frequency of parasitic oscillations. Z_l and R_s are the inductive and resistive components after adding the ferrite bead, respectively. This criterion ensures that the resistive damping is the main effect. The added capacitance down shifts the oscillations.

- The ferrite bead should be chosen with damping coefficient m in the range from 0.5 ~ 1 at the frequency of parasitic oscillations should be chosen. Hence an effective damping while without scarifying turn on speed is achieved because over-damp (m>1) increases the turn-on transient time. Coefficient m is expressed as:

$$\mathrm{m}= \mathrm{R_s} \big/ (2 \cdot \sqrt{\mathrm{C_e} / L_e}) \tag{5. 1}$$

  Where R_s is the resistive component after adding the ferrite bead, C_e is the lumped equivalent parasitic capacitance from the circuit, and L_e is the equivalent inductance in series of the current, including the inductance of the ferrite bead.

- The power loss of the ferrite bead at the inverter switching frequency should be as low as possible to minimize the overall power losses.

The resistance – and inductance – frequency characteristics of the employed ferrite bead are shown in Fig. 5.30. The selected ferrite bead has a cross section area of $A_c = 6mm \times 22mm = 132mm^2$, the added inductance is 4.8µH at the inverter switching frequency, and the saturation flux density is 470mT. As a result the maximum current can be

conveyed is calculated as $I = B_{\max} \cdot A_c / L_s = 12.9\,\mathrm{A}$ which is sufficiently enough to avoid saturation. The ferrite bead in the DC bus is applied as across both of the DC+ and DC- bus to avoiding saturation. The inverter output frequency is 50Hz based on the PWM control strategy, the output AC current is measured as 2.3A (rms value); and R_s is measured as $1.57m\Omega$ at 50Hz (according to Fig. 5.30), therefore the caused overall losses from the bead are calculated as 8.3mW.

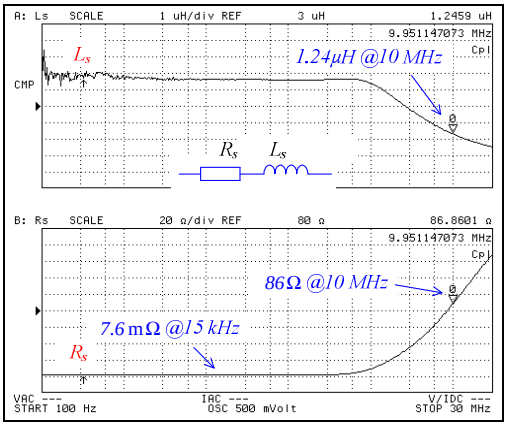


Fig. 5.30 The resistance – frequency (R-f), and inductance – frequency (L-f) characteristics of the ferrite bead used for parasitic oscillations suppression

The proposed solutions are applied in the model as follows:

- For application position 1, the parasitic inductance of L_p is changed to RL (L=1.24μH and R=86Ω) in series connection according to the measurement shown in Fig. 5.30.

- For the ferrite bead inserted at position 2, the inductance of L_{o1} is changed to *RL* (L=1.24×3+0.62=4.34μH and R=86×3=258Ω) in series connection. L_{01} is used instead of L_{o2} because the insert position is close to the inverter side. This will lead to better noise suppression than if it is positioned close to the motor side, as is proven by the modeling.

Correspondingly, the modeled results are shown in Fig. 5.31. In the case of no ferrite beads, the result is the same as shown in Fig. 5.28. It can be seen that adding ferrite beads at position 2 leads to a larger reduction of noise in the mid frequency range, however it causes deterioration at high frequency range, because the addition of inductance lowers the intrinsic resonance frequency of the motor with cables to 10 MHz which is close to the DM parasitic oscillation frequencies. Hence oscillations are magnified. Adding ferrite beads at position 1 reduces noise both in the mid and high frequency ranges, because the inductance increase in series with the noise source is proportional to the filter attenuation. Therefore by combining the two solutions noise emission in high frequencies can be effectively suppressed.

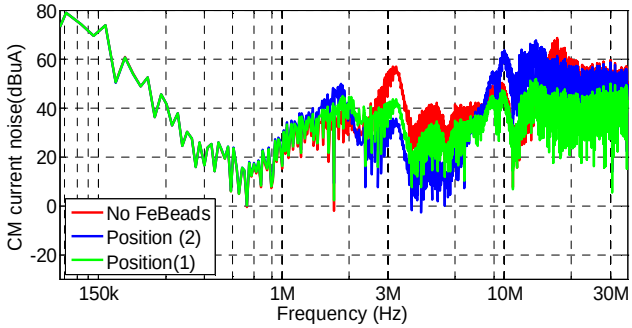
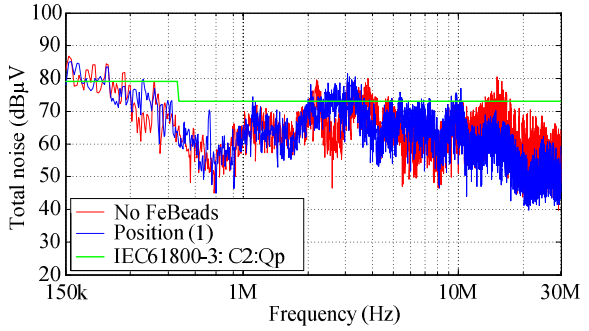


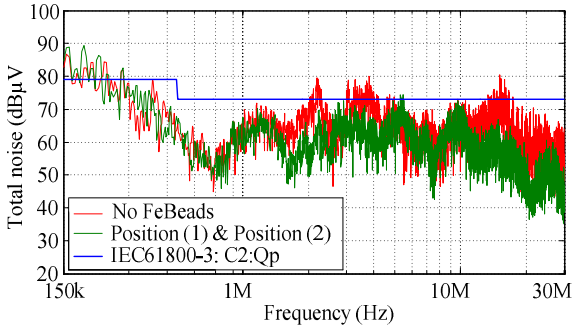
Fig. 5.31 Comparison of the modeled CM current spectra with the proposed solutions – ferrite beads inserted into position 1 and 2 respectively

5.5.4 Validation of suppression effects

The suppression effects are validated by measurements as shown in Fig. 5.32 (a) and (b) respectively. The case of no ferrite beads corresponds to the SiC JFET inverter with LC filter (shown in Fig. 5.17 (a)). It can be seen that after inserting the ferrite beads at position 1, the high frequency noise (beyond 12 MHz) is suppressed, because DM current oscillations are damped. From Fig. 5.32 (b) it can be seen that the mid frequency noise is suppressed, because CM parasitic oscillations are damped. With the combination of two solutions the EMI noise above 500 kHz is effectively suppressed to comply with the standard prescribed by IEC61800-3-C2: QP. The measurements agree well with the modeling shown in Fig. 5.31.



(a)



(b)

Fig. 5.32 Measured EMI spectra of SiC JFET system with the proposed solution (a) ferrite beads inserted into position 1 (b) ferrite beads inserted into positions 1 and 2

5.6 Conclusion

In this chapter, quantitative EMC performance comparisons between SiC JFET and Si IGBT sources are presented. The causes of the differences in EMI levels are analyzed and explained. Two motor drive prototypes using SiC JFETs and Si IGBTs as the switches are built using the same circuit layout and investigated accordingly. The EMI comparisons start from the transient level of the inverter tested under clamped inductive switching conditions by using of a single inverter leg to the three phase systems. The conducted EMI is measured without filter and with conventional CM filters. In the implemented configuration, SiC JFETs switch more than twice the speed of IGBTs, which results in the higher current/voltage overshoots and parasitic oscillations. Although the EMI levels of the two systems without filter are very similar, differences become significant after adding the identical CM filters. It is shown that the noise at the parasitic oscillating frequencies is obviously higher than that of the other ranges.

Additionally, solutions to improve the EMI filter to accommodate SiC JFETs are proposed. It is shown in waveforms that the CM currents are oscillating at the mid frequencies, and the DM currents are oscillating at high frequencies. The oscillations are more highly magnified in the SiC JFET system than those in IGBT's. Accordingly, the proposed solution is to position the ferrite bead on the DC bus between filter and inverter to suppress DM oscillations. In addition, it is also necessary to add the beads between the inverter output and motor to mitigate the CM oscillations. Equivalent circuit modeling is used to predict the suppression effects. Consequently, noise emissions in the mid and high frequency ranges are effectively suppressed to comply with the IEC61800-3-C2: QP standard.

Chapter 6

SiC Noise Reduction Due to Substrate Capacitive Coupling

6.1 Introduction

In this chapter the discussion on the EMC performance of the SiC JFET based motor drives is continued. The causes of different EMI levels are analyzed, and methods to suppress the conducted EMI in the SiC inverters under the influence of substrate capacitive coupling are proposed. The SiC JFETs are placed on top of two types of substrates – Insulated Metal Substrate (IMS) and Heat sink, which creates a different magnitude of capacitive coupling that increases the parasitic oscillations and causes the EMC performance to deteriorate. There is extensive capacitive coupling in IMS between the circuit coil and substrate base plate. Two methods are proposed, the use of separated substrates and the equivalent circuit modeling method, in order to suppress the influence of capacitive coupling.

SiC JFETs significantly improves conversion efficiency, and lead to the reduced size of magnetic components (e.g. EMI filter, transformer) and cooling substrates for power electronics converters. To keep pace with the resulting power density increase, thermal management must be enhanced due to the reduced surface area of the magnetic components which is available for cooling. Applying IMS is one of the most effective methods for use in medium power converters [God97]. On the other hand, IMS is also well known for its susceptibility to EMI crosstalk [Asa93]. Fig. 6.1 (a) illustrates the typical structure of the IMS. It can be seen that because of the very thin dielectric layer (typically 40μm~180μm) placed between the circuit copper foil and the metal (typically aluminum or copper) base plate, a large amount of stray capacitance is formed (Fig. 6.1 (c)), which creates a loop for high frequency currents that can generate EMI. This effect becomes more critical when the IMS is used to cool active power devices, especially when SiC JFETs drain plates are attached on top as illustrated in Fig. 6.1 (b). The capacitive coupling, together with the fast switching of SiC, results in great degradation of the conducted/radiated EMC performance. As a result, costly additionally filtering is needed to keep the emitted noise below the stringent EMI standard. This is the main barrier to increased power density.

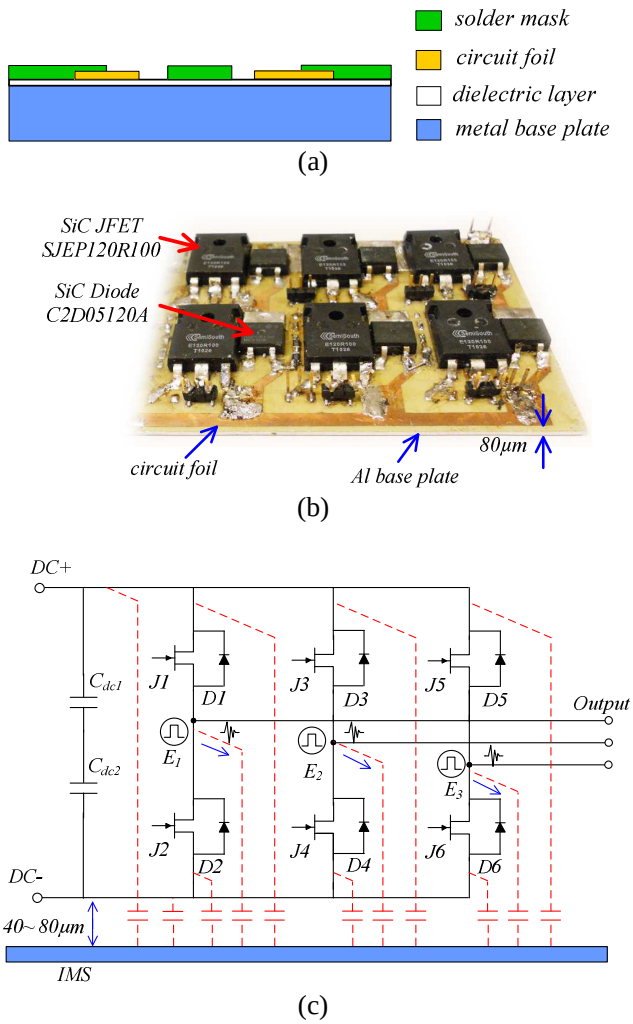


Fig. 6.1 (a) The construction of the IMS (b) a photograph of the investigated IMS inverter prototype and (c) the extensive capacitive coupling created due to the implementation of the discrete SiC JFETs attached on top of the IMS

Moreover, mitigating parasitic oscillation that occurs at the switching transients under the influence of circuit parasitics is a widely encountered problem [Bos00]. Especially when the IMS is used, the deteriorated parasitic environment due to the increased stray capacitors greatly influences the switching performance, causing higher switching losses. Further, because of the "Miller" effect and low thresh-hold gate voltage of SiC devices, fault operations are more common [Pla11]. A detailed investigation presented in [Jos11a] shows that when SiC JFET under the influence of capacitive coupling, the generated high frequency oscillations can prolong the switching transients by seven times and the frequency varies from 10 MHz to 100 MHz. In [Gon12a] it is found that in specific circuit configuration the high frequency noise level of an IMS inverter can be 20dB higher than that of a comparable heat sink inverter, with both systems utilizing identical EMI filters.

In order to increase the reliability and to simplify the EMC design, many methods have been subjected to extensive research over the last couple of years. For example, Josifovic et al. [Jos11a] systematically investigated the damping methods on the DM current oscillations for a SiC JFET inverter, and optimized SiC switching performance was achieved. In [Zei11], high ESR capacitors are used to add a RC snubber to damp the oscillations, which effectively increases the decay rate of the oscillations while without degrading the power efficiency. A method to minimize the PCB layout parasitic inductance is proposed in [Kam09], which effectively mitigates the oscillations but has no negative influence on the performance of the system. However this method is not easy to realize as it relies on circuit complexity and manufacturing constraints. Some other methods such as increasing the gate resistance, adding a gate-source clamp capacitor, slow down the switching speed and increase the losses.

The two methods described in this chapter are:

- Use separated substrates, which means to place each SiC JFET on top of a separated substrate. Three 2.2 kW inverter prototypes – each with six discrete SiC JFETs on the IMS, one on a one common heat sink and one on a separated heat sink are built using the same circuit layout and investigated accordingly.

- Use equivalent circuit modeling to predict filter insertion losses over a broad conducted EMI frequency band. This is essential in order to achieve an optimized filter design balanced between performance and cost. The presented experimental and calculated results form the step-by-step guideline for containing EMI.

Both methods effectively suppress the emitted noise to comply with the standard prescribed by IEC61800-3-C2: Qp.

6.2 Capacitive coupling influence and minimizations

Fig. 6.1 (c) illustrates the capacitive coupling mechanism in the IMS inverter. Due to the very thin dielectric layer placed between the circuit copper foil and the metal base plate, beneath each signal flowing point there is stray capacitance formed to the metal plate. For safety reasons the metal plate is required to be connected to the earth, the formed stray capacitors create extensive EMI coupling paths closing loops with considerable EMI noise propagations. To minimize this influence the method of separating substrate is proposed.

6.2.1 Influences and Solutions

Influence on DM

Fig. 6.2 illustrates the capacitive coupling influence on DM, single inverter leg is used. Parasitic capacitors C_{dh1}, C_{dh2}, and C_{dh3} are the capacitors created when discrete power devices (SiC JFET + Anti-parallel Diode) are attached on top of one common substrate. C_{dh1} and C_{dh2} are the capacitors between the upper and lower switch drain plates and the substrate plate respectively. C_{dh3} is the capacitor between DC- bus and substrate plate. When the substrate is floating, through $Y-\Delta$ transformation these three parasitic capacitors are equivalently added

in parallel to the switch, appearing as the increased values on C_{jp1} and C_{jp2}. Degradations on DM performance are introduced as follows:

- Increase the current overshoot. At switching transients (e.g for J_2), the current overshoot is dependent on the pulsed voltage across the opposite switch (J_1). When the capacitance in parallel to the switch is increased, the overshoot is also increased.

- Increase the parasitic oscillations. The figure in Chapter 5 section 4.3 is shown here again as Fig. 6.3 for ease of explanations. At a turn-on transient of J_1, the discharge current of C_{jp1}+C_{s1} circulates through the switch S_1 and resonates with intrinsic inductors in the switch. At the turn-off transient, C_{jp1} + C_{s1} start resonating with external inductors L_{dc} and L_{db1}. Therefore the added capacitance after $\mathrm{Y}-\Delta$ transformation increases the parasitic oscillations. The oscillation frequencies are likely down shifted to a conducted EMI frequency range between 10 MHz and 30 MHz. Hence the high frequency EMC performance is greatly deteriorated.

- The increased capacitance slows down the switching speed and increases the switching losses.

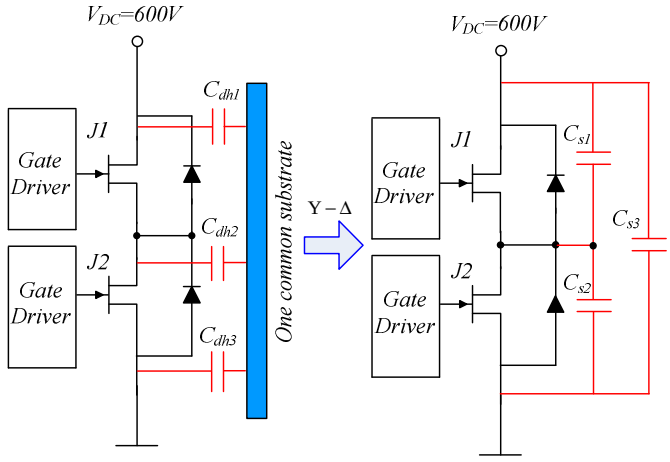


Fig. 6.2 Capacitive coupling and the increased capacitance in parallel to switches

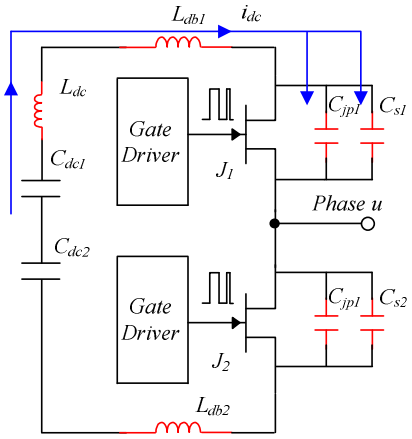


Fig. 6.3 DM current flow path within one inverter leg

Solutions for DM

The principle of minimizing DM capacitive coupling by using separated substrate is illustrated in Fig. 6.4. It can be seen that the use of separated substrates has a decoupling effect by breaking the neutral point of the three capacitors in Y connection, which effectively decreases the equivalent capacitance in parallel to the switches.

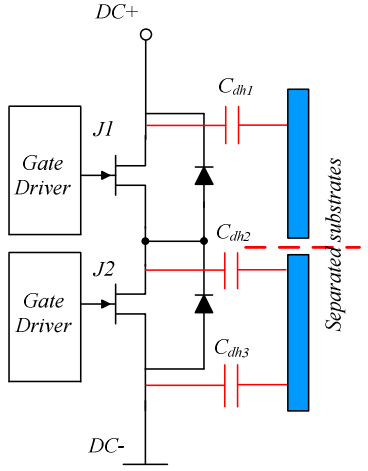


Fig. 6.4 Minimization of DM capacitive coupling by separating substrates

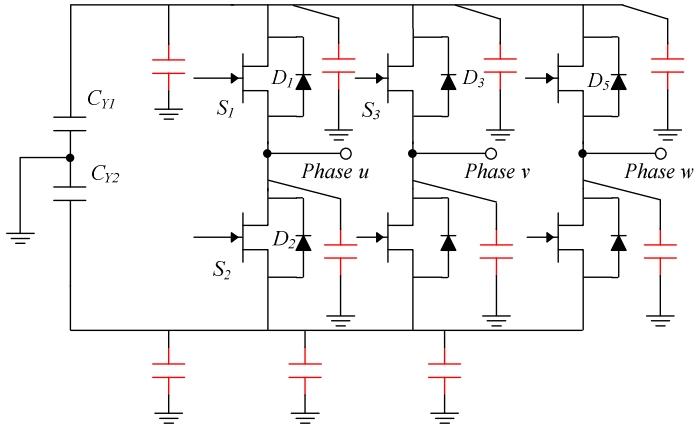
Influence on CM

Fig. 6.5 illustrates the influence of capacitive coupling on CM, which is:

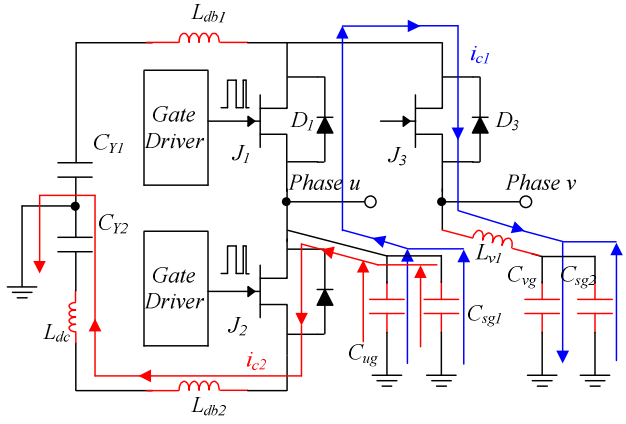
- Parasitic oscillations are increased. There are two current flow paths. One is between the phase and filter capacitor, the other one is between the two inverter legs. C_{sg1} and C_{sg2} are the added capacitors due to capacitive coupling. The energy of the parasitic oscillations is increased for both of the paths. The deterioration is

proportional to the magnitude of capacitive coupling.

- Noise coupling among inverter legs. According to the PWM switching technique, when the upper switch in one inverter leg (e.g. J_3) is switched on while the lower switch in another inverter leg (e.g. J_2) is in off state, pulsed voltage (dv/dt) appears between these two inverter leg output nodes *u* and *v*. As a result, the existing parasitic capacitors between two inverter leg output nodes and the substrate plate form the path that propagates the high frequency noise from one node to the other. Therefore each of the three inverter leg output nodes acts as a noise source, which is expressed by E_1, E_2, and E_3 as shown in Fig. 6.1 (c). Coupling occurs among these three sources when all three lower switches are attached onto one common substrate.



(a)



(b)

Fig. 6.5 CM current flow paths among inverter legs (a) increased stray capacitors (b) current flowing paths

Solutions for CM

The principle of minimizing CM capacitive coupling by using separated substrate is illustrated in Fig. 6.6. The separation of three inverter legs minimizes the parasitic oscillations, and also decouples the coupling from each other.

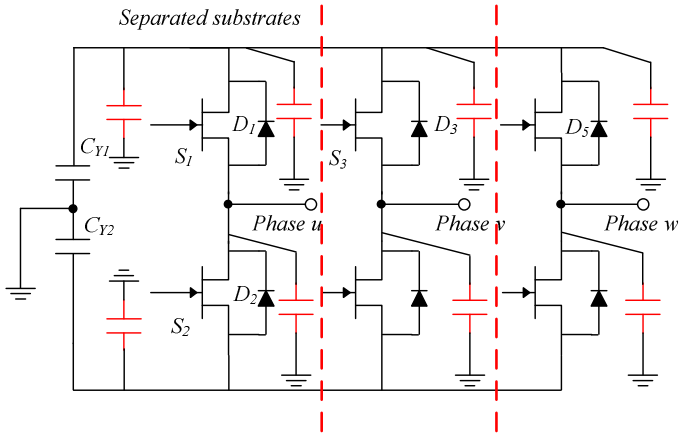


Fig. 6.6 Minimization of CM capacitive coupling by separating substrates

Consequently, separation of the two substrates, one is attached to all three upper switches and the other is attached to lower switches, decouples the upper and lower switches within one inverter leg. The aim is to improve the DM performance. Additionally, it is also necessary to separate the substrate attaching three inverter legs, the aim of which is to improve CM performance. In the following sections, a SiC JFET inverter using separated heat sinks is built to verify the facts mentioned in this discussions.

6.2.2 Circuit parasitics and extraction

The schematic that includes the considered circuit parasitics of the inductive switching test to measure the SiC JFET switching waveforms is illustrated in Fig. 6.7, where C_{dh1}, and C_{dh2} are the parasitic capacitance between the summed area of SiC JFET drain and SiC diode cathode and the heat sink plate, an inductive load is used, and the concerned CM (I_g) and DM (I_{ds}) currents which flow in the earth line and from drain to source of the switch respectively are indicated in the figure. A single inverter leg is used. The implemented circuit layout is shown in Fig. 6.16 (b). Extraction of the parasitic parameters is introduced as follows:

$L_{d1,2}$ and $L_{s1,2}$ are the estimated lead inductance both are in series to the drain and source terminals of the SiC JFET in the TO-247 package. C_{jp1} and C_{jp2} are the summed parasitic capacitance of JFET output and SiC diode p-n junction. These values are obtained through the datasheets. $L_1 - L_4$ are the parasitic inductance of the DC bus cable and foil. The values are measured using impedance analyzer Agilent 4294A by connecting the test pins to starting and ending terminations respectively (e.g. connect to power supply output and DC bus capacitor lead for measuring L_1).

During the test, two 2.2μF film capacitors are connected in series across the DC bus as shown in Fig. 6.7. Each of them comprises the *ESR* and *ESL*. These elements are extracted through curve-fitting of the capacitor impedance-frequency characteristic. The capacitor *ESL*

(L_{dc1}) and capacitance C_{dc1} create its self-resonance at frequency f_s. In equation it is expressed as:

$$f_s = 1/(2 \cdot \pi \cdot \sqrt{L_{dc1} \cdot C_{dc1}}) \quad (6.2)$$

C_{lp} is the Equivalent Parallel Capacitance (*EPC*) of the load inductor. Extraction of C_{lp} follows the same as that for DC bus capacitors.

It is important to minimize the formed parasitic capacitors between the SiC switch drains and heat sink plate (C_{dh1}, C_{dh2}, and C_{dh3}). The SiC JFET (SJEP120R100) is packaged in TO-247 with a drain of Aluminum back plate and the surface area of A_s=20.3*15.3=310.59mm^2. The added diode (C2D05120A) in anti-parallel to the JFET is packaged in TO-220 with the cathode surface area of A_d=9.65*14.3=138.0mm^2. The total surface area of A_s+A_d comprises the parasitic capacitance of C_{dh1} and C_{dh2} (given in Fig. 6.7). With 150µm thick dielectric Sil-pad (l=0.15mm ε_r=5) the capacitance is calculated as C_{dh2}= $\varepsilon_r\varepsilon_0$ *(A_s+A_d)/ l=133pF. The thickness of the isolation pad is inversely proportional to the parasitic capacitance value. The three inverter legs all have 6 top power devices (SiC JFETs + SiC diodes) at the same potential as the DC+ bus voltage, therefore they all contribute to the equivalent value of C_{dh1}. The equivalent capacitance value is: C_{dh1} = 3× C_{dh2} =399pF. Using the same formula, C_{dh3} is estimated by the summed surface area of the DC- bus copper foil, and its distance from the substrate plate. According to the PWM switching scheme, fast switching dv/dts occur between the node of the bridge leg output phase (summed area of SiC JFET drains and diode cathodes, both in the low side) and the base plate. As a result, the parasitic capacitor C_{dh2} is important for the CM EMI propagation. A summary of the parasitic values is given in Tab. 6.1. In case of the IMS inverter, corresponding capacitances are larger because the thickness of dielectric layer is smaller. Corresponding capacitances are used for the modeling, which will be introduced in Section 6.6. Minimization of the coupling for the heat sink inverter will be discussed in DM and CM respectively in the next two sections.

Table 6.1 Summary of parasitic values

Parameter	A_s	A_d	C_{dh1}	C_{dh2}	C_{dh3}
Heat sink inverter	310.59 mm^2	138.0 mm^2	399pF	133pF	35pF
IMS inverter	310.59 mm^2	138.0 mm^2	747pF	249pF	97pF

L_{cb} is the added inductance by the current probe when measuring the earth current I_g. Its value is determined according to the measured inductance-frequency characteristic of a wire with and without being clamped by the current probe (shown in Fig. 6.8). The difference is the introduced inductance. It can be seen that the current probe adds 10nH at 2 MHz. There is hardly any effect in the high frequency range beyond 10 MHz. L_{so} is the same parasitic inductance at the JFET source when measuring the DM current $I_{ds.}$ In addition to the probe inductance, the extracted value also includes the parasitic inductance of the PCB trace.

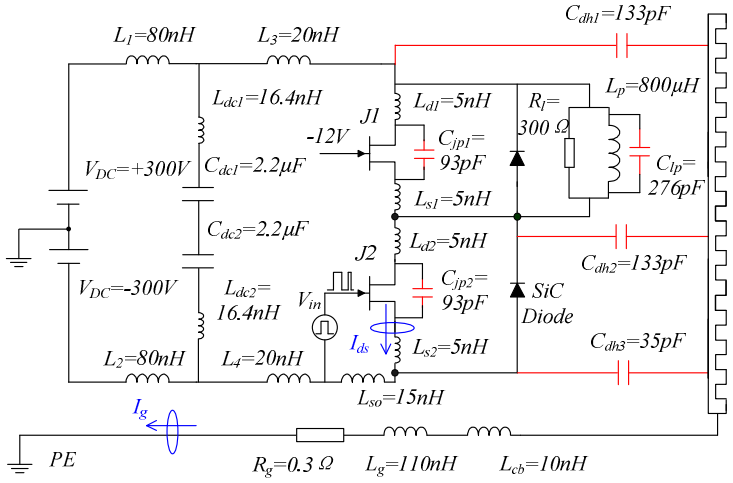
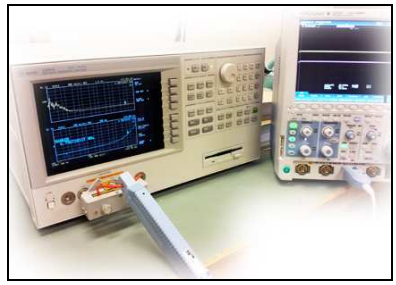


Fig. 6.7 Circuit parasitics considered for use in the heat sink inverter leg in order to measure the SiC JFET inductive switching waveforms



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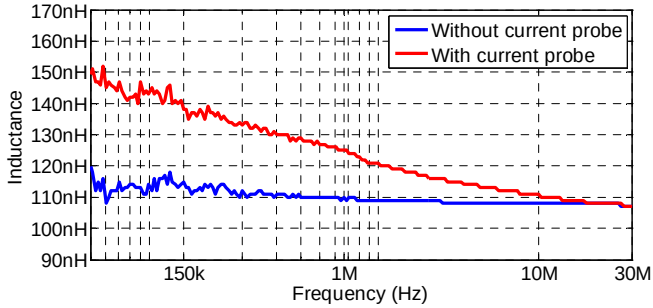


(b)

Fig. 6.8 (a) Measurement setup (b) The measured inductance-frequency characteristics of a 110nH wire with and without being clamped by the current probe

6.2.3 DM Oscillation Damping Methods – Simulation and Implementation

Simulations

The DM switching performance depends on the capacitance between the drain-source terminals of the SiC JFETs. This capacitance consists of two parts: 1) The summed intrinsic parasitic capacitance of the switch and diode (C_{jp1} and C_{jp2}). 2) The capacitance due to the three Y - connected parasitic capacitors ($C_{dh1,}$ C_{dh2} and C_{dh3}), which after the Y – Δ transformation are C_{s1} and C_{s2}.

Using Fig. 6.7 as the schematic, the DM current waveforms (I_{ds}) measured under conditions of using one common heat sink and separated heat sinks are compared in Fig. 6.9. In the case of separated heat sinks, 1 MΩ resistance is inserted in series with capacitors C_{dh1} and C_{dh2}. The other parameters remain the same. It can be seen that the use of separated heat sinks effectively decreases the second spike of DM current. In addition, it also damps the low frequency oscillations during the decay period (see from 0.5μs and on). At the switching transition of the switch J_2, despite the value of switching dv/dt, the first current overshoot is determined by the total capacitance of C_{jp1} and C_{lp}, and the second overshoot is mainly determined by C_{jp1}. With decreased C_{jp1} the second current spike is greatly decreased. The DM parasitic oscillations consist of high frequency and low frequency parts. High frequency oscillations are caused by the resonances between the parasitic inductance along the current flowing loop and the parasitic capacitors C_{jp1}. Low frequency oscillations are determined by the parasitic inductance and C_{lp}. However, the capacitive coupling also has the effect of slowing down the switching speed of J_1 and J_2, and consequently decreasing the values of switching dv/dts. This could be a benefit from the EMC point of view. However, the experiments performed in the following sections verify that this impact is mainly negative.

Additionally, two other damping methods, the insertion of ferrite bead (ZCAT3035 TDK) into the DC bus and the addition of RC snubber tightly across the switch pair are implemented with the separate heat sinks configuration. The aim is to suppress the DM noise further. The schematics are illustrated in Fig. 6.10 as Ferrite bead and RC snubber respectively. The use of ferrite bead is equivalent to adding a frequency dependent resistor and an inductor in series with the current flowing path, which damps and mitigates the high frequency oscillations. The RC snubber (R_{se1}=R_{se2}=50Ohm, C_{se1}=C_{se2}=3300pF) added across the DC bus is designed as two RC branches in series connection. The aim is to combine both of the DM and CM damping methods. Because of the RC snubber across the DC bus, the DM is damped, and by grounding its midpoint, the CM is also damped. The value of the resistor is experimentally adjusted to achieve critical noise damping. The value of capacitor is designed to absorb the energy in the parasitic oscillation. In equation it is expressed as:

$$\frac{1}{2}\cdot C_{ss}\cdot V_{ss}^{\ 2} = \frac{1}{2}\cdot L_{es}\cdot i^2 \qquad (6.\ 3)$$

Where V_{ss} is the voltage across the snubber, L_{es} is the parastic inductance, and i is the current flowing through the switch.

Selection of the ferrite bead is based on same considerations as it was introduced in Chapter

5, section 2.

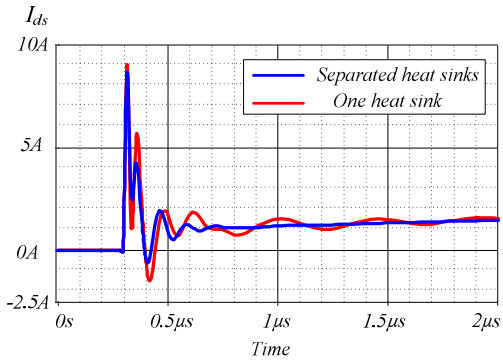


Fig. 6.9 Simulated DM currents (I_{ds}) using one common heat sink as opposed to separated heat sinks

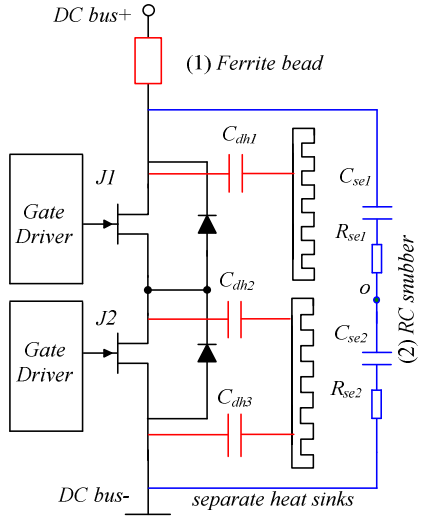


Fig. 6.10 DM Parasitic oscillation damping methods (1) insertion of ferrite bead at DC+ bus (2) RC snubber added tightly across the bridge leg

Inductive switching waveforms

The measured DM switching waveforms are shown in Fig. 6.11 (a), (b), (c), and (d) respectively. Fig. 6.11 (a) shows the waveforms when using one common heat sink which is grounded. Fig. 6.11 (b) illustrates the waveforms when using separated heat sinks. It can be seen that the use of ferrite bead exhibits the best damping effect, however at the cost of higher voltage overshoot of around 50V at the turn off transition. The overshoot is increased by voltage across the bead inductance.

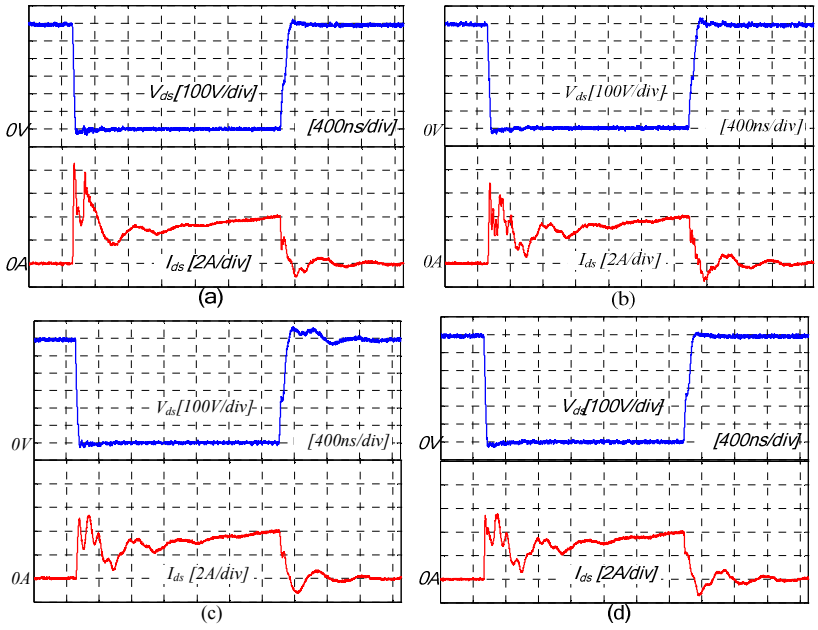


Fig. 6.11. Measured DM switching waveforms with and without applying the damping methods (a) one common heat sink (grounded as shown in Fig. 6.7) (b) separated heat sinks (c) Ferrite bead (*RL*) with one common heat sink (d) DM *RC* snubbers combined with separate heat sinks

6.2.4 CM Oscillation Damping Methods – Simulation and Implementation

The grounding of high side heat sink

For safety reasons the heat sink which is exposed or connected to the frame always needs to be referenced to sufficiently low levels (e.g. ground) to avoid electric shock. There is a choice of two options, either grounding the high or low side heat sink, when using separated heat sinks. It is decided in this case to ground the high side heat sink and connect the low side heat sink to ground via inductive impedance in order to achieve the effective damping. The reason is as follows: according to the PWM scheme, pulsed voltages (dv/dts) appear at the nodes of the three inverter bridge legs. When the lower switch is grounded, the formed parasitic capacitor between the drain and the attached heat sink base plate (e.g C_{dh2} as shown in Fig. 6.7) closes a path that propagates the parasitic oscillations to earth, and increases the CM noise. While in the case of upper switches, their drains are connected to the DC bus+. Because the DC+ voltage is relatively constant, therefore a stable CM voltage is kept across CM coupling capacitors (e.g C_{dh1} as shown in Fig. 6.7) when the high side heat sink is grounded. Direct link from the earth to the high dv/dt values at the node of bridge leg output is avoided.

The simulated CM current waveforms (I_g) are shown in Fig. 6.12. The same schematics are used when performing DM simulations for one common heat sink and separated heat sinks conditions. It can be seen that the use of separated heat sinks effectively decreases the CM current overshoots and oscillations, which is because of the decreased parasitic capacitance in the CM propagation loop. Although the proposed method is effective in reducing the noise

propagation from the SiC JFET drains to the earth, it doesn't reduce the noise propagation from the motor windings to the earth.

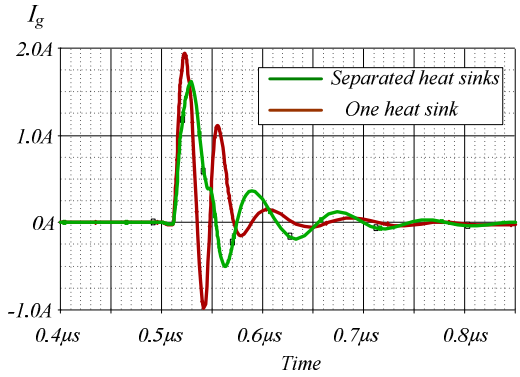


Fig. 6.12 Simulated CM currents (I_g) of using one common heat sink as opposed to using separated heat sinks

Implementations for CM oscillations damping are illustrated in Fig. 6.13. In addition to grounding the high side heat sink, the middle point of the DM snubber (point o as shown in Fig. 6.10) is also connected to the earth. This allows the added snubber circuit to mitigate both CM and DM. The two heat sinks are connected via *RL* ($R = 65\Omega$, L=20µH) as explained previously.

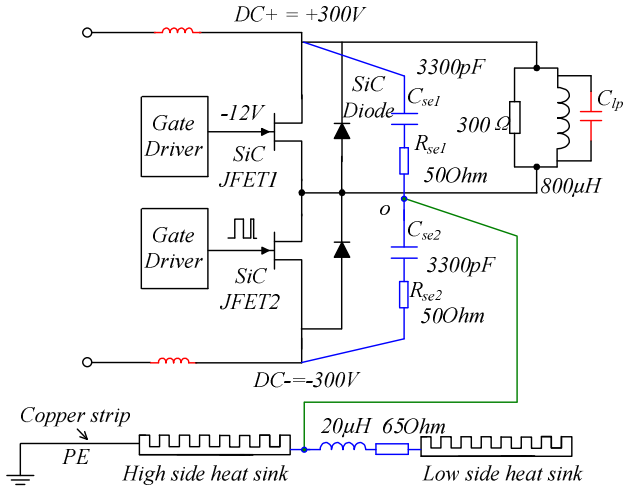


Fig. 6.13 CM parasitic oscillations damping methods: separated heat sinks and combine with the DM damping snubber

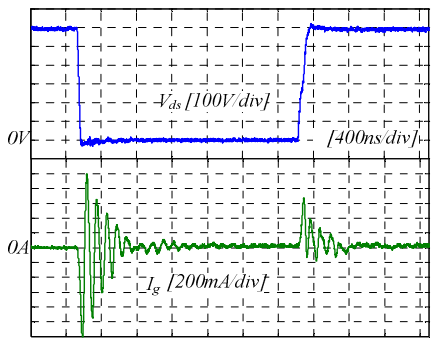
Inductive switching waveforms

The measured CM switching waveforms are presented in Fig. 6.14 (a), (b) and (c) respectively. Fig. 6.14 (b) illustrates the waveforms when using separated heat sinks with low side heat sink floating. Fig. 6.14 (c) illustrates the case when the low side heat sink is grounded through *RL* circuit. Fig. 6.14 (d) illustrates the waveforms when using separated heat sinks

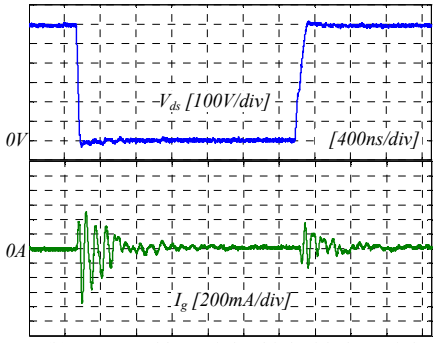
combined with the *RC* snubber. It can be seen that the use of separated heat sinks effectively reduces the CM oscillation magnitudes. When the *RC* snubber is combined, the high frequency noise is significantly dissipated to the low frequency ranges. The reason is that with one heat sink configuration as shown in Fig. 6.7 the oscillation is mainly determined by the capacitance of C_{dh2} and the lumped inductance along the current flowing path. When the configuration is changed into separated heat sinks combined with RC snubber as shown in Fig. 6.13, a *RL* ($R = 65\Omega$, L=20μH) circuit is inserted between the high- and low-side heat sinks. This results in the increased capacitance and inductance of the CM current flowing path (o – $C_{dh,}$ – *RL* – PE). Additionally, at the switching transients the oscillations seen on the DC bus+ are propagated through the load capacitance C_{lp}, which leads to the increased low frequency contents.

It is shown in Fig. 6.14 (d) that although the oscillation frequencies are down shifted, the oscillation magnitude increases, which is due to the increased capacitance from the added snubber. This impact is likely to lead to the deterioration of the CM performance. However, the motor drive system situation differs from that of in the inductive switching test. In the performed inductive switching test, the switching devices are the main source of EMI. The added snubber creates an additional CM noise propagation path to the earth. The increased capacitance in the path excites higher current overshoots that are propagated to the earth through the snubber. However in the motor drive system, the added snubbers act as the filter first stage that filters the high frequency noise propagated from the motor and cables. Therefore although the EMC performance deteriorates at the magnified oscillation frequency, performance in the other frequencies especially in the high frequencies is improved because the high frequency oscillations are damped and down shifted. Therefore the dominating damping effect is the frequency.

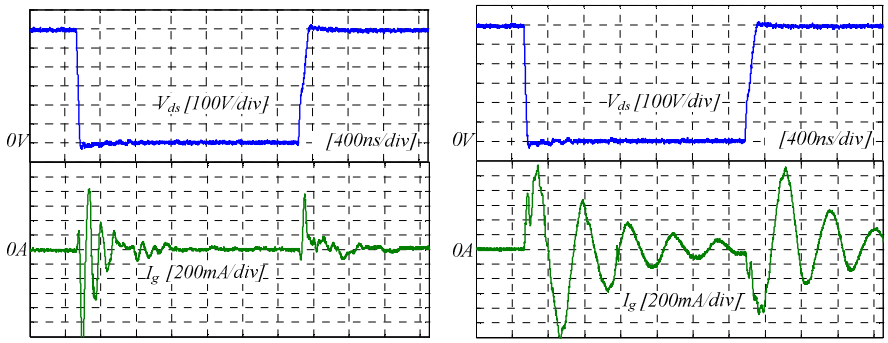
While performing the measurements, attention must be paid to the potential influence of the current probes and measuring techniques. Fig. 6.15 illustrates the inductive switching measurement set up. The voltage measurements are carried through a differential voltage probe (700924 YOKOGAWA) with 100 MHz bandwidth and which is connected to the oscilloscope with a coaxial cable. To minimize the measurement error the test leads are placed very close to the drain and source of the SiC JFET. To avoid crosstalk loops forming, only one single voltage measurement is performed during each test. The current probe that has a bandwidth of 50 MHz (701929 YOKOGAWA) is clamped on the earth line.



(a) One common heat sink



(b) Separated heat sinks, high side heat sink grounded, low side heat sink float



(c) separated heat sinks, high side heat sink grounded, low side heat sink is connected with high side heat sink through RL

(d) separated heat sinks construction combined with RC snubbers, low side heat sink is connected with high side heat sink through RL

Fig. 6.14. Measured CM current switching waveforms with and without the damping methods

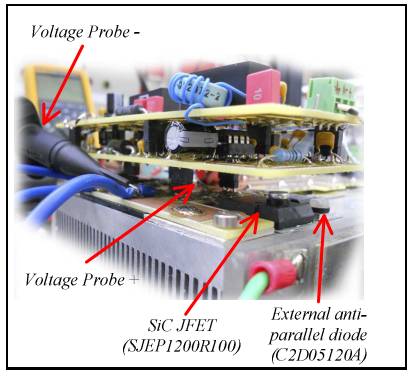


Fig. 6.15 Photograph of the inductive switching measurement setup

6.3 Comparisons between IMS and one heat sink inverters

6.3.1 Experiment configuration

In this section, the EMI levels are compared the facts at system level. Firstly, the SiC JFET IMS inverter and inverter using one common heat sink are compared to determine the influence of capacitive coupling. Secondly, effects of using separated heat sinks are shown. The implemented layouts are illustrated in Fig. 6.16 (a) and (b) respectively. In both cases aluminum is used as the cooling material. The implemented layouts of IMS and heat sink inverters are the same as that in the inductive switching test. The difference in the layout design is due to the following reasons: for the IMS inverter, the drain plates of the SiC JFETs are soldered directly on top of the IMS copper foil to achieve better cooling effect. Therefore the foil traces of the DC bus are soldered to the drain/cathode plate of the semiconductors. The components are placed closer to each other. However in the cause of the heat sink inverter, the thermal Sil-pads ($\approx 150\mu m$) must be inserted to provide electrical insulation, therefore the PCB is used and placed between the upper and lower switches. Although the above-mentioned

differences exist, the EMI levels of the two inverters are comparable making it possible to characterize the capacitive coupling influence. Because both two inverter prototypes are implemented with the same type of discrete SiC JFETs and anti-parallel external SiC diodes in the same package on top of the substrates, the coupling mechanism is assumed to be the same. The configurations for both inverter versions as used in the experiment are illustrated in Fig. 6.17.

All of the tested inverter prototypes are situated in the same EMC testing environment with the same measuring equipment. Unshielded cables are used to connect the inverter to motor. The inverters are powered by 550V from a DC power supply through a LISN (Crange VN3-100S). A 2.2 kW induction motor is driven at 50Hz modulation frequency. The inverter switching frequency is set to 16 kHz by programming the driving signal source from a DSP. The inverter and motor are grounded to the same copper plate. The EMC spectrum analyzer is set for 9 kHz resolution bandwidth and 18 s sweep time.

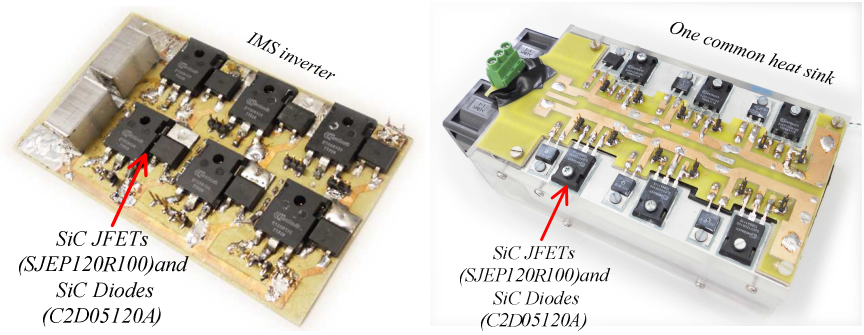


Fig. 6.16 Photographs of the investigated SiC JFET inverters (a) IMS inverter (b) One common heat sink inverter

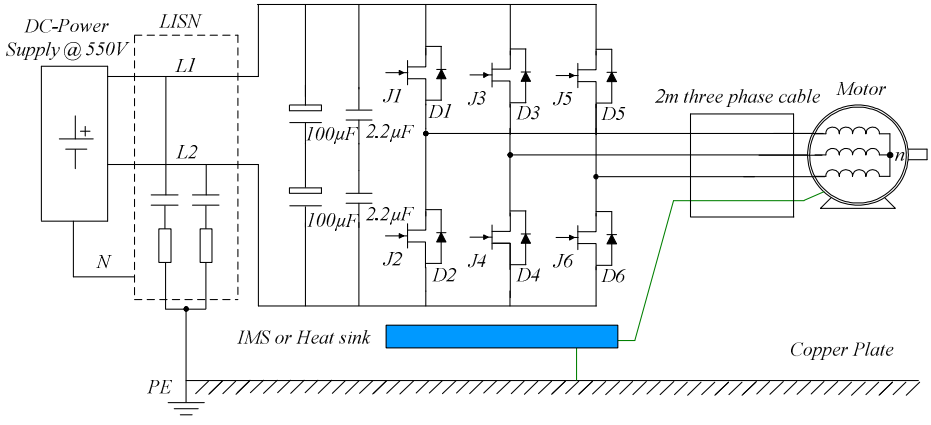


Fig. 6.17 Experiment configuration of the IMS and heat sink inverters

6.3.2 Comparisons without filter

The first group of comparisons is performed with only four DM capacitors – two 100μF

electrolytic capacitors and two 2.2µF film capacitors in parallel across the DC bus as shown in Fig. 6.17. This is defined as the unfiltered condition because it has the fewest necessary filtering components. The measured CM current and DM current noise spectra of three inverters are compared as shown in Fig. 6.18 and Fig. 6.19 respectively. The CM and DM noise are separated by the current probes (Fischer F-75) according to the methods described in [Zha06].

Comparing the spectra emitted from the IMS inverter and heat sink inverter, reasons of exhibited EMI differences are analyzed as follows:

- The IMS inverter can be considered as significantly increased stray capacitors placed between the copper foil and the base plate. On one hand noise with a broad frequency band is propagated to the earth through those capacitors, therefore the noise from the IMS inverter is widely spread over the low frequency range and results in the much higher level of 200 kHz to 700 kHz. On the other hand, those capacitors also partly behave as filtering capacitors to circulate some high frequency noise back to the source, results in the lower CM noise spectrum slope above 5 MHz.

- The lower DM noise of the IMS inverter is due to the influence of the increased capacitance of C_{jp1} and C_{jp2} (shown in Fig. 6.7) as analyzed in the previous section 6.2. The increased DM current overshoots and oscillations lead to the magnified noise level especially in the high frequency range.

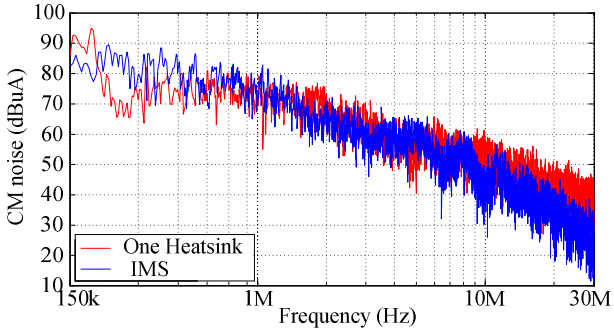


Fig. 6.18 Comparison of measured CM EMI spectra: one heat sink versus IMS

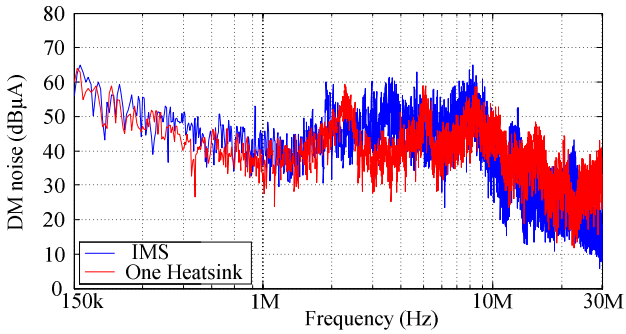


Fig. 6.19 Comparison of measured DM EMI spectra: one heat sink versus IMS

6.3.3 Comparisons with purely capacitive filter

Next, an identical and conventional purely capacitive CM filter (470nF) is placed at the input of both IMS and heat sink inverters. The measured total EMI spectra are presented in Fig. 6.20. It can be seen that the emitted noise in the IMS inverter is significantly higher than that of heat sink inverter in the mid frequency range (3~7 MHz), which is due to the higher frequency current overshoot influenced by the extensive capacitive coupling. Additionally, the grounding of CM capacitors couples high frequency noise into the earth. Since the impedance of noise source in this range is small, the added capacitors have little suppression effect on the emitted noise. Therefore although the low frequency noise is significantly suppressed, the influence results in no and slight improvements in the mid frequency and high frequency ranges respectively. Therefore in the case of the IMS inverter, the added capacitor that is conventionally found in the filter must be carefully designed.

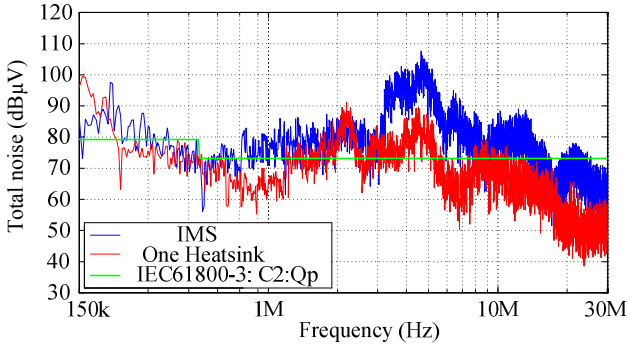


Fig. 6.20 Comparison of measured total EMI spectra: IMS versus one heat sink

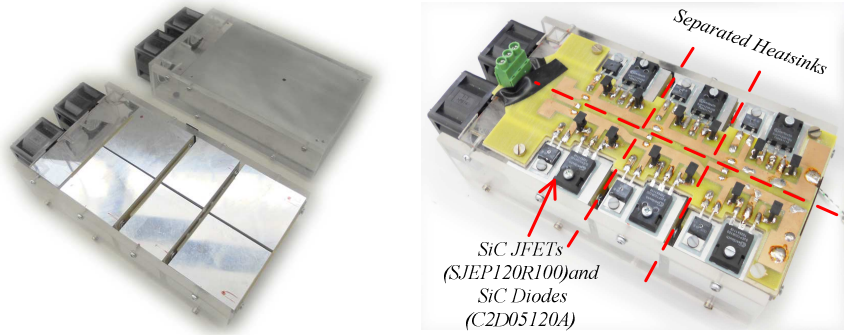
6.4 Comparisons between one heat sink and separated heat sink inverters

6.4.1 Experiment configuration

In this section, the EMI spectra from the inverters using one and separated heat sinks are

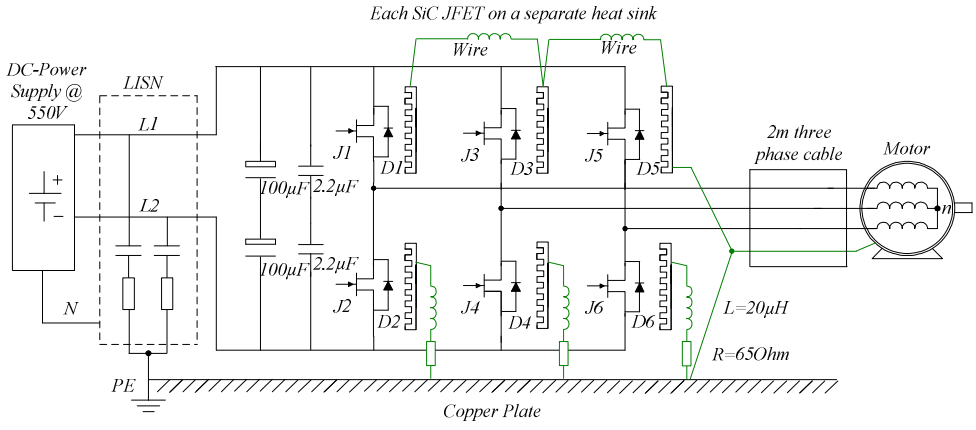
compared. Fig. 6.21 (a) illustrates the heat sink layout. Photograph of the separate heat sink SiC JFET inverter is illustrated in Fig. 6.21 (b). The same PCB layout is implemented in the two inverters. The separated heat sink has the same material and geometry as the one common heat sink. The same thermal Sil-pads with 150μm thickness are used as the dielectric layer. The separated heat sink portions are aligned using steel screws and encapsulated with 11mm thickness plastic.

The experiment configurations for EMI measurements of the inverters using separated heat sinks and separated heat sinks combined with damping snubbers are shown in Fig. 6.22 (a) and (b) respectively. The inverter version of using separated heat sinks uses the same configuration as those used in the inductive switching test of Fig. 6.14 (c). Because any piece of power electronics should be referenced, all the three top side heat sinks in the same voltage potentials are connected together and grounded. The low side heat sink portions are connected to the earth through RL ($R = 65\Omega$, L=20μH) inductive circuits. The EMC test condition is the same as that was introduced in section 6.3.

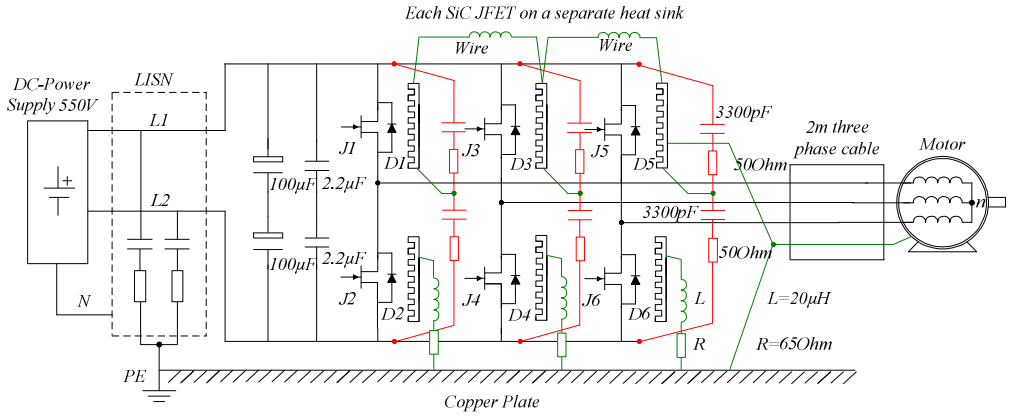


(a) (b)

Fig. 6.21 (a) Heat sink comparison (b) Photograph of the proposed separate Heat sinks inverter: each SiC JFET and SiC diode on top of a separated heat sink.



(a)

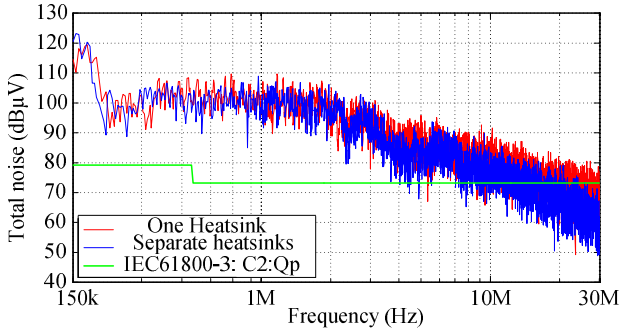


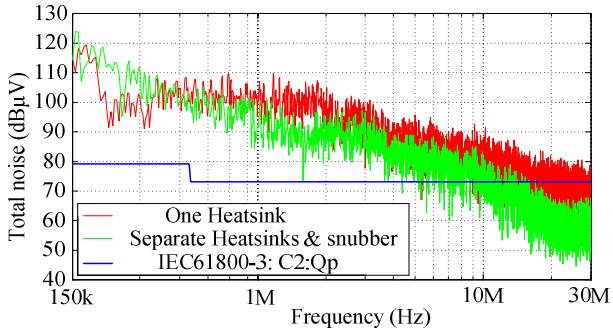
(b)

Fig. 6.22 Experiment configuration of the separate heat sinks inverter (a) separated heat sinks (b) separated heat sinks combined with damping snubbers

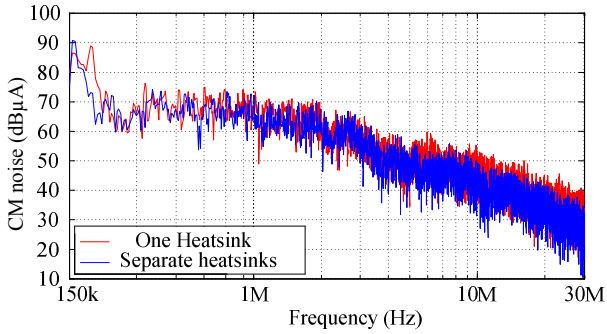
6.4.2 Spectra Comparisons

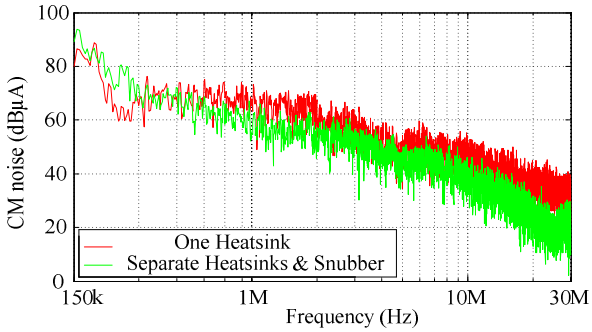
The EMI spectra that include total noise, CM and DM current noise without filter measured from the inverters using one common heat sink, separated heat sinks and separated heat sinks combined with damping snubbers are compared in Fig. 15 (a), (b), and (c) respectively. It can be seen that the implementation of separate heat sinks combined with damping snubbers effectively improve the high frequency EMC performance, while at most 20dB is achieved in DM. The degradation at low frequency range is due to the increased power of low frequency oscillations as explained in section 6.2.4. There is no degradation of DM noise in either case, which agrees well with the results shown in Fig. 6.11. However no significant improvement is achieved in CM when solely using the separate heat sinks because the CM noise in the motor drive system is mainly propagated from the motor side. In specific it propagates through the parasitic capacitors between the motor windings and the stator.



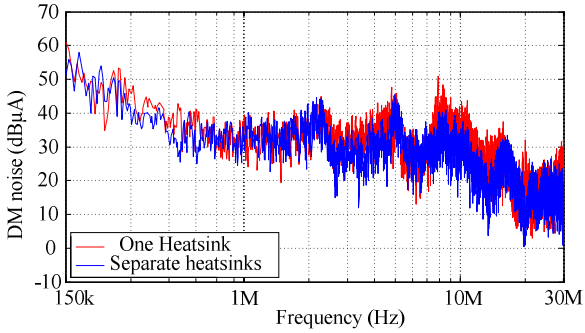

Total noise (dBµV)
130
120
110
100
90
80
70
60
50
40
One Heatsink
Separate Heatsinks & snubber
IEC61800-3: C2:Qp
150k
1M
10M
30M
Frequency (Hz)

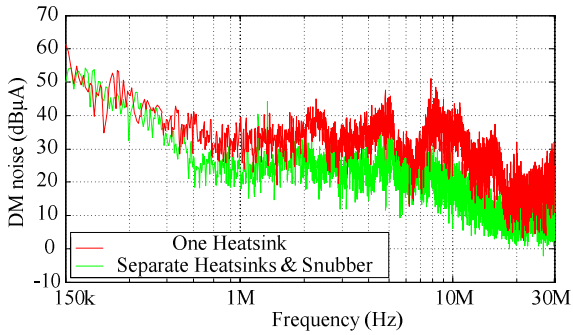
(a)


CM noise (dBµA)
100
90
80
70
60
50
40
30
20
10
One Heatsink
Separate heatsinks
150k
1M
10M
30M
Frequency (Hz)


CM noise (dBµA)
100
80
60
40
20
0
One Heatsink
Separate Heatsinks & Snubber
150k
1M
10M
30M
Frequency (Hz)

(b)


DM noise (dBµA)
70
60
50
40
30
20
10
0
-10
One Heatsink
Separate heatsinks
150k
1M
10M
30M
Frequency (Hz)



(c)

Fig. 6.23 Measured EMI spectra of the three investigated inverter systems (a) total noise comparison (b) CM noise comparison (c) DM noise comparison

Comparing the spectra emitted from the one common heat sink inverter and separate heat sinks inverter, the reason of differences are analyzed as follows:

- The main benefit obtained from using the separated heat sinks lies in the DM EMC performance. The effect is the decreased capacitance of C_{jp1} and C_{jp2} (in Fig. 6.7), which is in the contrast to the degradation effect caused by IMS. In addition, compared to the IMS inverter design, the used PCB board with 1.6mm thickness increases the distance between the DC bus- and the heat sink, therefore the capacitance of C_{dh3} is much lower than that in the IMS. Because of Y-Δ transformation the contribution to the capacitance of C_{jp1} and C_{jp2} is also lower.

- Regarding CM performance there is no significant improvement. This is because the CM noise in the motor drive system is mainly propagated from the motor side. More specifically, it is caused by the parasitic capacitors between the motor windings and the stator/chassis. The slight improvement of CM beyond 6 MHz is because of the purposely grounding of one of the top side heat sinks so as to prevent noise coupling from phase nodes to the earth.

6.5 Filtering solutions and applications

In the above sections, quantitative conducted EMI comparisons are presented by investigating the inverters using three layout substrates. The different parasitic influences of IMS and heat sink substrates that results in significantly different EMI levels, are analyzed and compared. With the aim of designing an effective filter design for above situations, the different EMI filter requirements are discussed and implemented in the following sections.

6.5.1 Filtering solutions

The previous experiments show that significant EMI differences exist among the inverters using different types of substrates. It is shown that the addition of capacitive filter further magnifies the EMI differences between the IMS and heat sink inverters especially around the mid frequency range of 4 ~ 6 MHz. The capacitive coupling that creates the propagation paths that is important for magnifying the emitted EMI levels. Based on this understanding, filtering

solutions for different inverter versions are proposed as follows:

- For the inverter using separated heat sinks with damping snubbers, the conventional LC low pass filter which is the simplest and most adopted topology is selected. Because the inverter has the improved EMC performance especially in the high frequency range, LC filter is considered to suppress noise sufficiently to comply with the IEC61800-3 standard. Attentions are paid to the noise in high frequency range due to the fast switching speed of the SiC JFETs.

- In the case of the IMS inverter, a three order filter order is applied with the aim of suppressing the noise propagated through the stray capacitors. This can be done by adding another CM choke to form a LCL filter, which is shown in Fig. 6.24. The added inductor has a damping effect on the CM parasitic oscillations. Additionally, its leakage inductance also suppresses the DM parasitic oscillations. Therefore both of the mid and high frequency noise can be reduced.

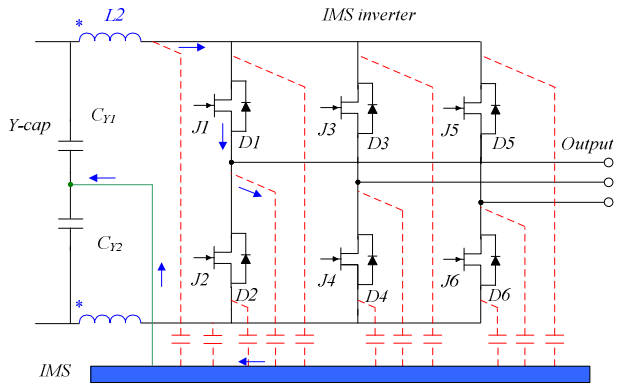


Fig. 6.24 Adding CM choke L_2 to suppress the influence of capacitive coupling in IMS inverter

6.5.2 Implementation for heat sink inverter

The filter schematic for inverters using one common heat sink and separated heat sinks is illustrated in Fig. 6.25. A common LC CM filter is initially applied. The inductance and capacitance are selected as 200µH and 470nF respectively based on the following considerations:

- The applied inductor core is ferrite and toroidal in shape with the maximum magnetic flux density of 380mT, and the cross section area is 30mm^2. To avoid saturation, the applied CM inductance must satisfy the following equations imposed by both DM and CM currents:

$$\begin{cases} B_{max} \geq L_{\sigma} \cdot I_{p1} / N \cdot A_c \\ B_{max} \geq N \cdot I_{p2} \cdot \mu_e / l \end{cases} \quad (6.4)$$

Where L_{σ} is the DM leakage inductance, I_{p1} is the DM peak current flowing through the inductor, which is 7.5A according to the measurements. N is the inductor turn number, A_c is the cross section area of the core. I_{p2} is the CM AC ripple current flowing through the inductor, which is 1.04A according to the measurements. μ_e =0.004 is the effective permeability of the core; and l=87.3mm is the total length of the core. Assuming an applied winding diameter of 1mm the maximum applicable inductance is calculated as 337μH. The impedance provided by the inductor should be sufficiently larger than the LISN impedance (25Ω). The initial applied CM inductance is selected as 200μH. It is worthwhile to keep the inductance small because a smaller filter can be used.

- The capacitance is chosen taking into consideration the difference between the emitted EMI level under unfiltered condition and the imposed standard IEC-61800-3. For the sake of simplification, the calculation is done at 150 kHz where the system emits the largest noise magnitude over the conducted EMI range. The simplified equivalent circuit models of the system that before and after adding the LC CM filter are illustrated in Fig. 6.26 (a) and (b) respectively. Assuming that the CM EMI source E is a purely voltage source, equations to calculate the required capacitance are expressed as:

$$\begin{cases} I = \dfrac{V_{CM}}{(Z_1 + Z_s)} \\ I_1 = \dfrac{V_{CM}}{Z_s + (Z_1 + Z_m) // Z_c} \cdot \dfrac{Z_c}{Z_1 + Z_m + Z_c} \\ T = 20 \cdot \log_{10}(\dfrac{I}{I_1}) \end{cases} \quad (6.5)$$

Where V_{CM} is CM source, Z_s is the noise source, which is represented by the CM impedance of the motor with cables and measured as 145Ω at 150 kHz by the impedance analyzer Agilent 4294A. Z_1 is the CM impedance of LISN, which is 25Ω ; Z_m is the impedance of the added CM choke, which is calculated as 188Ω at 160 kHz; Z_c is the required impedance of the Y capacitor; and T is the needed attenuation, which is 40dB according to the measurement. As the consequence Z_c is calculated as 1.856Ω which is transferred as 290nF for both of the Y capacitors. Taking a safe margin and a practical value the capacitance is selected as 470nF.

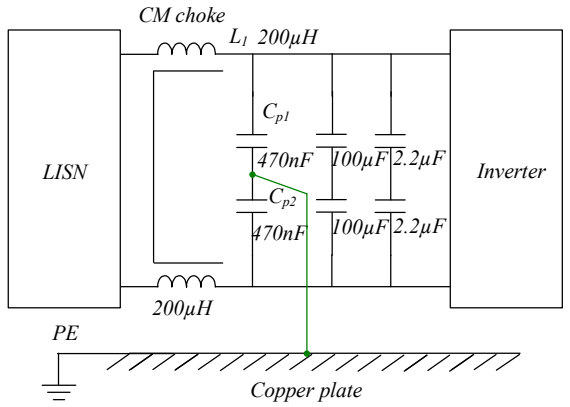


Fig. 6.25 Filter schematic for heat sink inverters

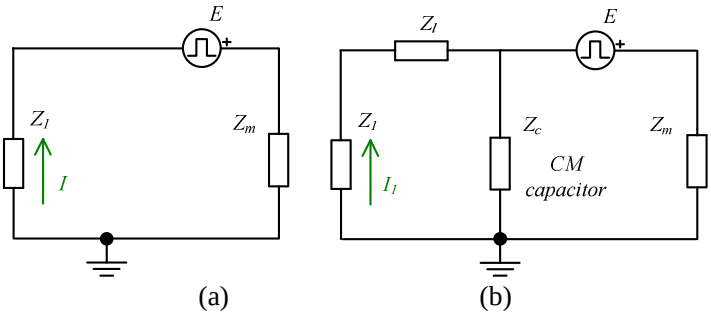


Fig. 6.26 Simplified equivalent circuit model to calculate the CM capacitor values (a) before adding the LC CM filter (b) after adding the LC CM filter

The EMI spectra are measured for the single and separate heat sink inverters with the applied LC filter as shown in Fig. 6.27. The configuration of Fig. 6.22 (b) is applied as the separate heat sinks configuration. It can be seen that the inverter using separated heat sinks has a much lower EMI level especially in the mid and high frequency ranges. Apart from the noise in low frequency range and a noise spike appearing in the mid frequency range, all other noise is suppressed to comply with the IEC61800-3-C2:Qp standard.

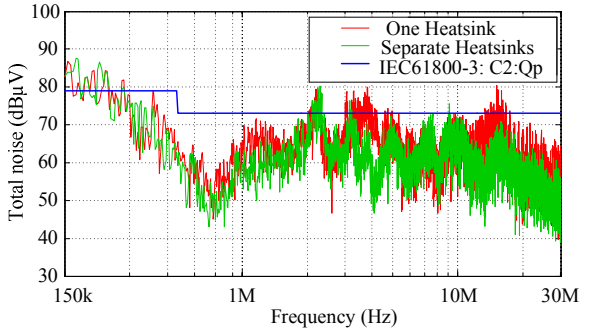


Fig. 6.27 Comparison of measured EMI spectra between one heat sink and separated heat sinks inverters

Taking filtering performance into consideration, the final filter design is improved in the following ways:

- Reduce the applied filter capacitance. This is aimed reducing the parasitic oscillations between the filter capacitor and the parasitic inductance in the current flowing loop. The inductance is fixed by the circuit layout, therefore reduction of capacitance is chosen.

- Increase the inductance which must be effective in mid frequency at the inverter output. This is because in inverter drive motor systems, the noise in the mid frequency range is greatly dependent on the motor CM impedance [Gon12b]. The increased inductance at the motor side will shift the motor self resonance to the lower frequencies where the applied filter has the higher attenuating ability.

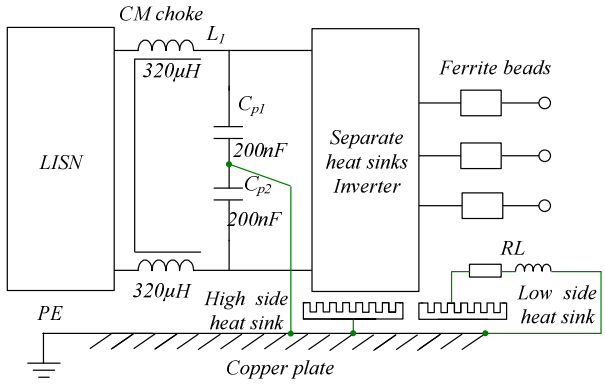
- Increase the inductance in the filter first stage to further reduce the low frequency noise. This is because the inductance in series to the inverter is proportional to the noise attenuation in low frequencies.

The schematic of the final implemented filter for the separate heat sinks inverter is illustrated in Fig. 6.28 (a), where three proposed solutions are realized by:

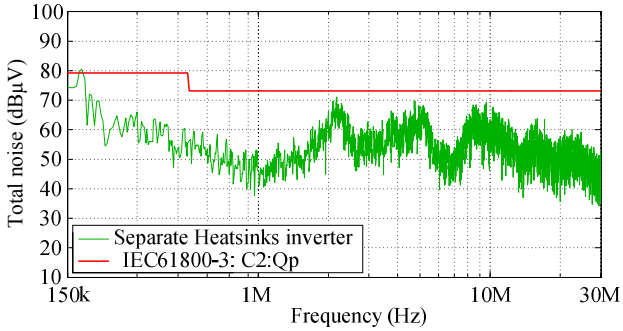
- The filter capacitance being decreased to 200nF.

- Three ferrite beads being inserted between the inverter three phase output phases and the driven motor. The used beads are the same as those introduced in Chapter 5 section 5.

- The LC filter inductance being increased to 320µH. The resulting EMI spectrum is shown in Fig. 6.28 (b). The emitted EMI noise is effectively suppressed to comply with the standard prescribed by IEC61800-3-C2:Qp.



(a)

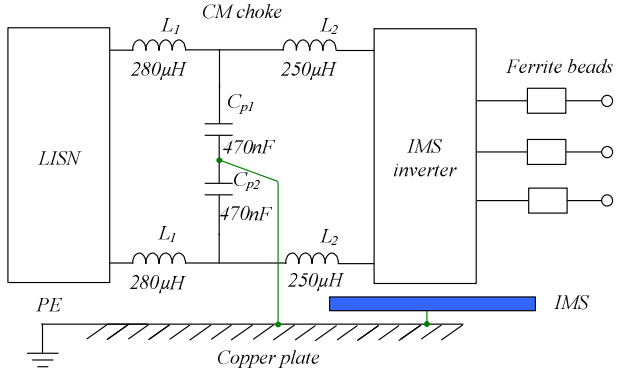


(b)

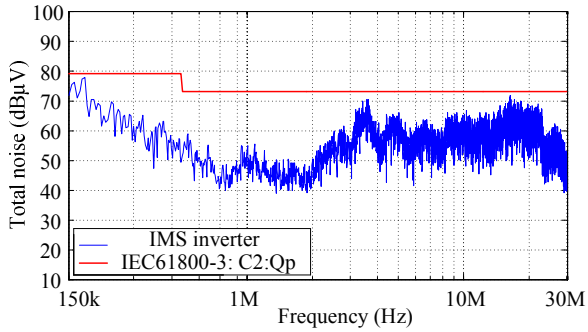
Fig. 6.28 (a) Final filter design for the SiC JFET inverter using separated heat sinks. (b) Measured EMI spectrum

6.5.3 Implementation for IMS inverter

The schematic of the implemented filter for the IMS inverter and the resulting EMI spectra are shown in Fig. 6.29 (a) and (b), respectively. The LCL three-order filter is applied. Additionally, as discussed previously, ferrite beads are inserted at the inverter output phases to further suppress and damp the high frequency noise. The bead inductance is added on both CM and DM. It can be seen that the increased EMI in mid and high frequency ranges caused by the capacitive coupling is effectively suppressed. As the result, the emitted noise is effectively suppressed to comply with the IEC61800-3-C2:Qp standard.



(a)



(b)

Fig. 6.29 Final filter design for the IMS SiC JFET inverter (b) Measured EMI spectrum

6.6 Modeling for IMS Inverter

In the following sections, the second method which is based on a broadband modeling to reduce EMI is proposed. The treatment of the crucial high frequency noise in the IMS inverter requires the applied method to predict the relative noise attenuation performance in a broadband of conducted EMI. Therefore the situation where noise is suppressed in low frequency range but increases in mid frequency and high frequency ranges can be predicted and avoided. The targets of modeling is to predict the filter insertion loss, hence to select the optimal filter design that has better performance while requiring less filtering components. All the following experiments are performed on the IMS inverter.

6.6.1 A Broadband modeling procedure

EMC design methods that enable EMC performance evaluation over a broad frequency band have become the trend and are increasingly popular nowadays. It is possible to predict the EMC and prevent the situation where noise is suppressed in some frequency range but is amplified in other frequency range. This is especially critical when dealing with the increased high frequency noise of the inverters with SiC JFETs on top of the IMS. Filter designs targeting a restricted low frequency band may become inadequate. In the past, many EMI filter design methods were developed to suppress the conducted EMI [Har11; Gra98; Pal02; Ren98; Kot12]. However most of them fail to predict EMI and require a trial-and-error process for a certain high frequency range. For example, a CM input filter design procedure is introduced in [Nus06] for a three-phase buck-type rectifier. A two stage CM filter is designed to suppress the conducted EMI to comply with the standard. However the suppression performance beyond 10MHz is overlooked due to the oversimplification of the model. A step-by-step design procedure is proposed in [Shi96] and proved to be effective below 1 MHz, unfortunately, the filtering performance prediction begins to deviate beyond that frequency. Others researchers have designed filters according to the noise level at the start (150 kHz) or at the frequency requiring maximum attenuation in the conducted frequency range [Aka08; She10]. However other frequencies are not considered. A broadband EMI filter design is presented in [Tar10], however the small signal based methods require very precise measurements, which are not easy to achieve.

The proposed modeling procedure is described as shown in Fig. 6.30.

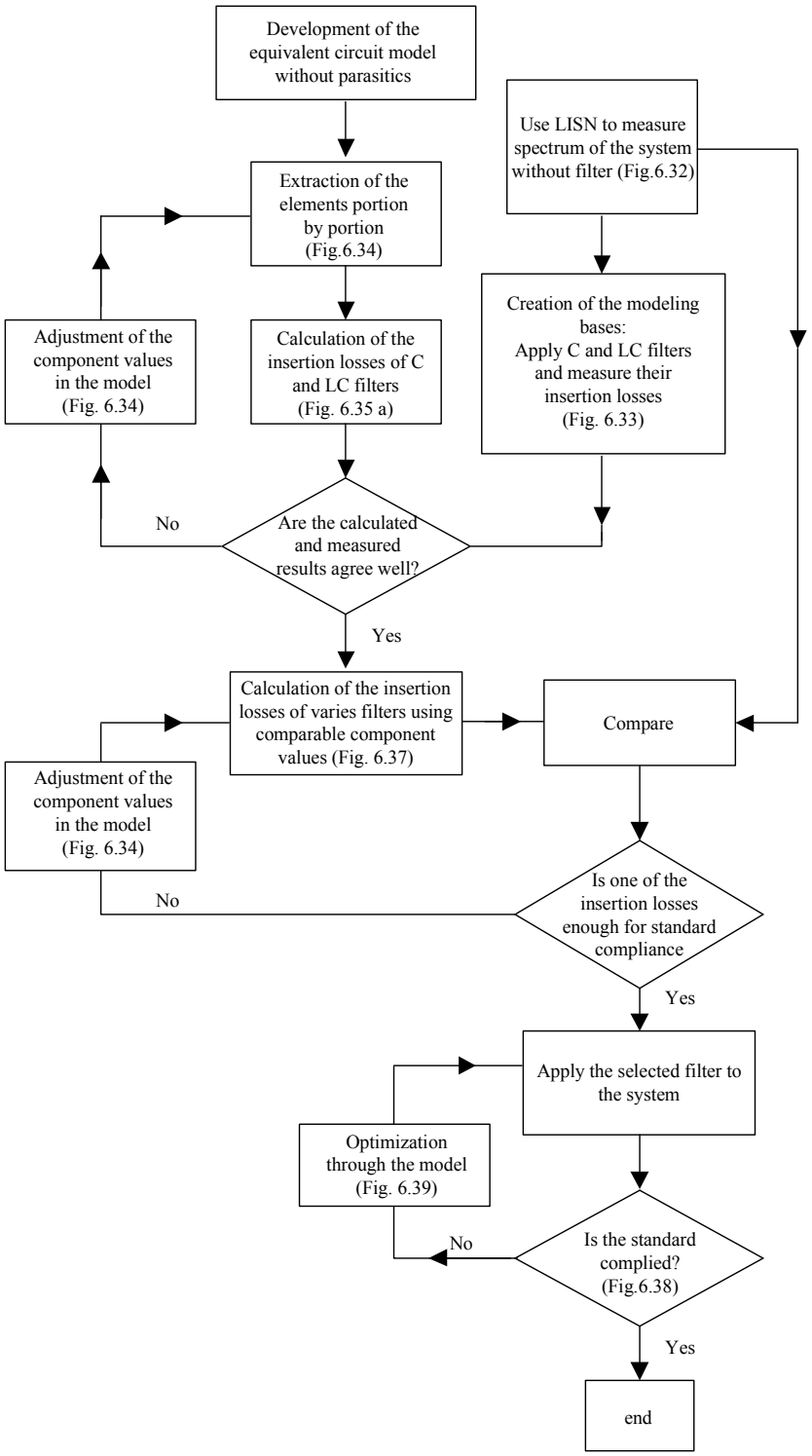


Fig. 6.30 The proposed broadband modeling procedure to predict filter insertion losses

6.6.2 Creation of the modeling bases

The considered CM filter topologies are illustrated in Fig. 6.31, and are named C, LC, LCL, and LCLC respectively. These topologies are chosen because they are widely adopted as the CM filter for inverter driven motor systems. Among them, the easy-to-implement topologies – C and LC are used to create modeling bases.

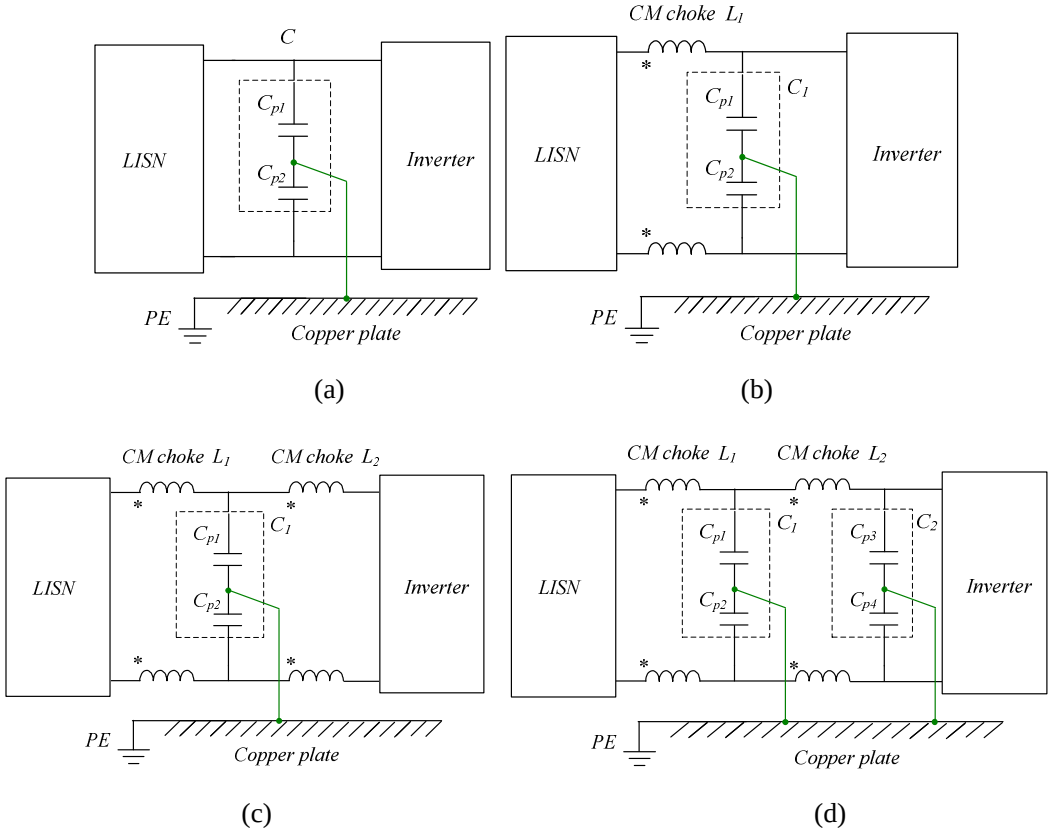


Fig. 6.31 Considered filter topologies: (a) C (b) LC (c) LCL (d) LCLC

The configuration with only two pairs of DM capacitors positioned in the DC bus (see Fig. 6.17) is the configuration without CM filter. The noise emitted from this configuration is defined as the noise baseline. Fig. 6.32 shows the required filter insertion loss which is calculated according to the difference between the IEC61800-3:C2 standard and the noise baseline. The measured insertion loss of the applied C (470nF) and LC (250µH 470nF) filters for IMS inverter is illustrated in Fig. 6.33. It can be seen that noise suppression in the mid frequency range is not sufficient and greatly degraded. This was to be expected as a result according to the analysis in section A. The values of the inductor and capacitor are selected with reference to the actual EMI filtering component values from commercial motor drives. The values of the inductor and capacitor are selected with reference to the actual EMI filtering component values from commercial motor drives. Additionally, design of the inductor value avoids saturation of the selected core.

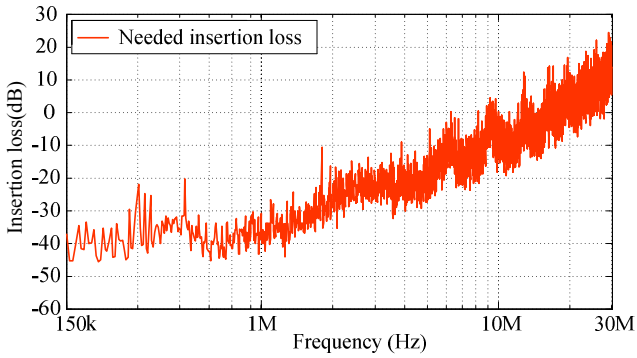


Fig. 6.32 Required filter insertion loss calculated from the noise baseline without filter

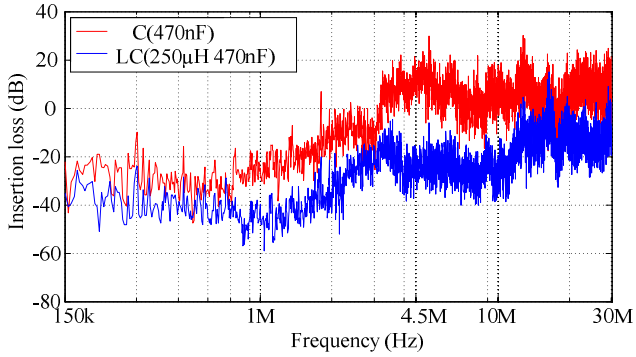


Fig. 6.33 Measured filter insertion loss with the implemented CM filter of: C (C=470nF) and LC (L=250µH, C= 470nF)

6.6.3 Final model for insertion losses

With the insertion losses from the created experimental bases with C and LC filters as shown in Fig. 6.33, the model which includes the detailed parasitic elements is developed as shown in Fig. 6.34. Capacitors C_{s1}, C_{s2}, and C_{s3} were obtained according to calculations described in section 6.22. The values were given in Table 6.1. The total capacitance includes all the capacitance between twelve power devices and the IMS substrate. The values of the stray elements network are lowered in steps to capture the resonances that occur around 4.5 MHz according to the measured insertion losses of Fig. 6.33. The same method as used for modeling the motor with cables as introduced in Chapter 5.5.1. Extraction of other elements will be introduced in section 6.6.3. The voltage appearing across R_1 is the emitted noise voltage picked up by the spectrum analyzer.

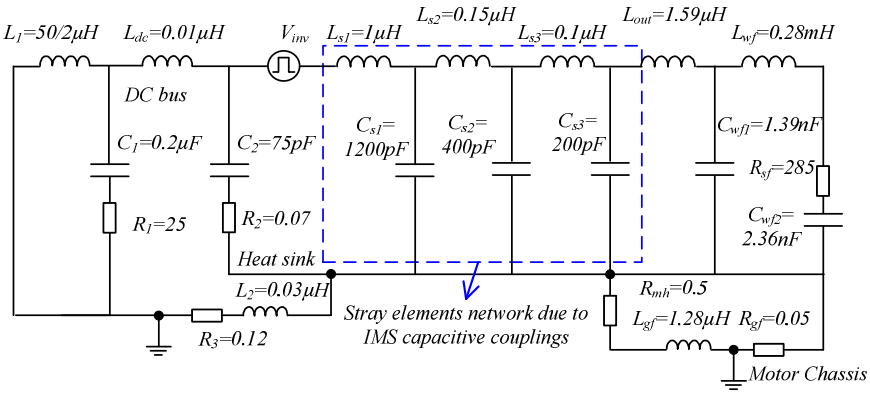
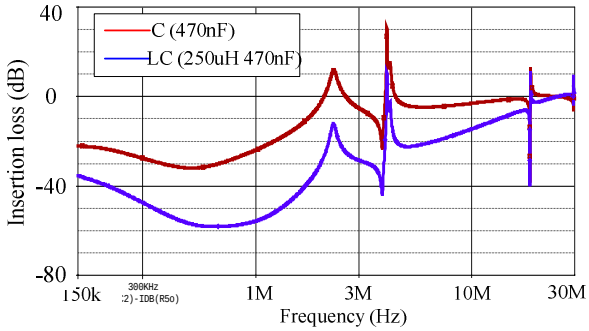


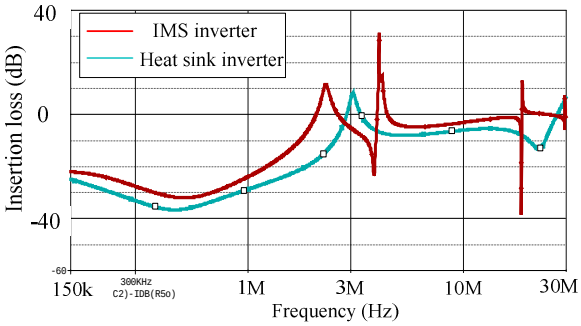
Fig. 6.34 Equivalent circuit model with extracted elements of IMS drive system

The calculated insertion losses of the IMS inverter with the C and LC filter is illustrated in Fig. 6.35 (a). It can be seen that the modeled results of Fig. 6.35 (a) agree well with the measurements of Fig. 6.33. The first spike at 2.5 MHz is caused by the CM intrinsic resonance of the motor with cables. The second spike at 4.5 MHz is caused by the resonance that occurs in the stray elements network which is fundamentally caused by the capacitive coupling influence of the IMS inverter.

The calculated insertion losses with applied pure C filter (470nF) at the input of both the IMS inverter and the heat sink inverter are shown in Fig. 6.35 (b). When calculating the insertion loss for the heat sink inverter, the stray elements network in the model is removed. It can be seen that the main difference occurs at the second spike at 4.6 MHz. Additionally, the noise magnitude of IMS inverter in low frequency range is around 6dB higher than that of heat sink inverter. The results agree well with the experimental results of Fig. 6.20. Therefore the established model is proven to be capable of evaluating the filter performance over a broad conducted frequency band. The spike at 4.5 MHz is mainly caused by the capacitive coupling and is critical for the filter design.



(a)



(b)

Fig. 6.35 Comparison of the modeled filter insertion losses (a) IMS inverter with the implemented CM filter of C (470nF) and LC (250μH 470nF) (b) between heat sink inverter (without stray elements network of capacitive coupling) and IMS inverter with C (470nF) CM filter

6.6.4 Elements Extraction

The elements extraction method is based on curve-fitting of the equivalent circuits CM impedance-frequency characteristic for each circuit portion in the system. Extraction of the stray capacitance in the IMS coupling network is introduced in section Circuit parasitics and extraction, the other main parasitic components are determined according to the equivalent circuit modeling method presented in Chapter 3. The Agilent 4294A impedance analyzer is used as the measurement tool.

Elements extraction for the filter is split into the different orders of the inductor or capacitor respectively. Each inductor or capacitor branch is measured and extracted separately. The CM equivalent circuit model of the applied LCL filter is shown in Fig.13, where the model branch of the third order inductor (250μH) comprises R_{f1}, C_{f1}, and L_{f1}, the model branch of the first order inductor (200μH) comprises R_{f2}, C_{f2}, and L_{f2}. The model branch of the second order capacitor (400nF) comprises R_{f3}, C_{f3}, and L_{f3}. Taking the CM capacitor parasitics extraction as an example, R_{f3} and L_{f3} are respectively the ESR and the ESL of the capacitor. In the measured impedance-frequency characteristic of the capacitor, C_{f3} is extracted according to the slope in low frequency range. The capacitor parasitic inductance L_{f3} is calculated from the occurred resonance in the mid frequency range. R_{f3} equals to the minimum value of the impedances.

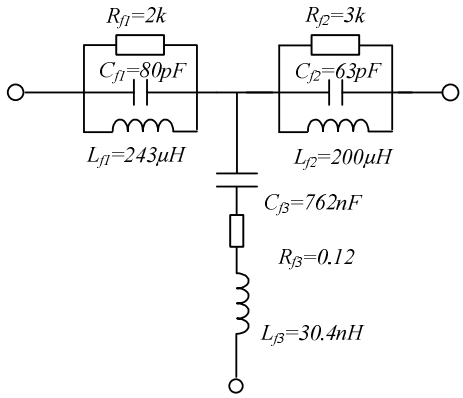


Fig. 6.36 Model of the applied LCL filter (L_1=250μH C_1=400nF L_2=200μH shown in Fig. 6.31 (c)) with extracted elements

6.6.5 Evaluation of different filter topologies

Using the developed model, the calculated insertion losses of each filter (C, LCL, and LCLC) are compared with each other as shown in Fig. 6.37. Selection of the component values is based on four considerations:

- The components should fulfill the calculated filter attenuation to the level required by the insertion loss as shown in Fig. 6.32.
- The component values in each order of the filter are the same, therefore the selected filter topologies as shown in Fig. 6.31 are volumetrically comparable.
- The core saturation caused by both CM and DM leakage magnetic fields must be avoided therefore the applied filter inductors realize their choking ability.

It can be seen that with reference to the required insertion loss, the LCL filter exhibits the best performance which effectively suppresses the noise spike in the mid frequency range while still retaining adequate attenuation ability in the high frequency range. The results are illustrative of an optimized EMI filter design with no excessive components involved. Although the LCLC filter utilizes more components, it does not perform better in suppressing the capacitive coupling influence. The above benefits can only be achieved by the broadband modeling of the conducted EMI.

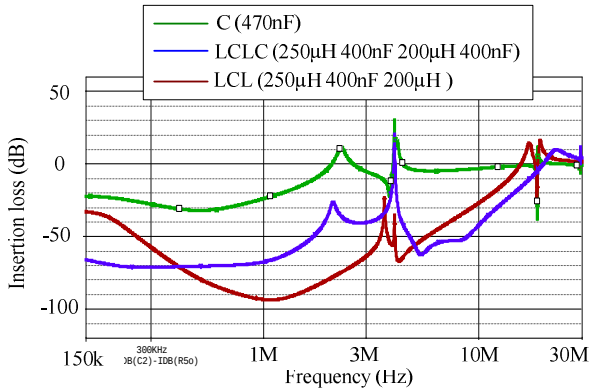


Fig. 6.37 The calculated insertion losses of different applied filters

6.7 Towards The Standard Compliance

6.7.1 LCL filter as the selection

As a result of the above considerations, LCL CM filter is selected as the final design and implemented in the IMS inverter driven motor system. The component values are the same as those in the calculated results shown in Fig. 6.37. The achieved EMI spectrum is compared with that of the LCLC filter which is shown in Fig. 6.38. It can be seen that the measurements agree well with the calculations of Fig. 6.37. The noise spike caused by the capacitive coupling at mid frequency range (around 4.5 MHz) is effectively suppressed. However the noise at the initial frequency of 150 kHz and high frequency range still fails to conform to the standard. This can however be achieved by a few adjustments which will be introduced in the following section.

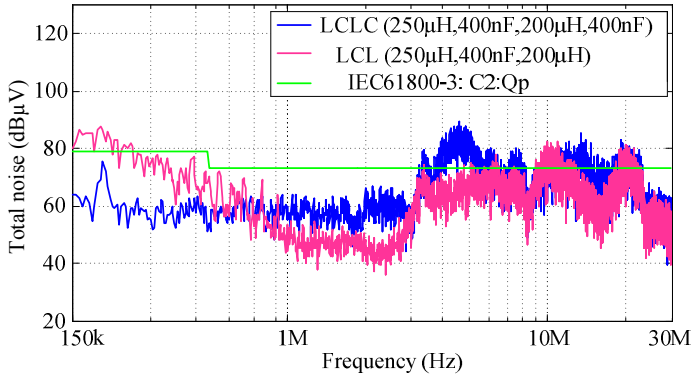


Fig. 6.38 Comparison of the measured total EMI spectra between the system with LCLC (250µH 400nF 200µH 400nH) filter and LCL (250µH 400nF 200µH) filter

6.7.2 Optimization

To further reduce the low frequency noise, the inductance of filter first order (L_2 in Fig. 6.31

(c)) is increased to 280µH. Reduction of the high frequency noise can be achieved in two ways:

- Decrease the grounding inductance (L_{f3} in Fig. 6.36) of the Y-capacitor. The Y-capacitors grounding inductance is lowered by using copper strips instead of wires to connect the capacitor leads to the ground.

- Increase the inductance which must be effective for high frequency noise suppression between the inverter output phases and the motor (L_{s3} in Fig. 6.34). The inductance at high frequencies of L_{s3} is increased to 3µH by adding ferrite beads. This method is the same as was used in Chapter 5 section 2. The beads are inserted across the unshielded cables that connect the inverter and the motor.

The calculated results of the optimization are shown in Fig. 6.39, where the application of LCL (250µH 400nF 200µH) shown in Fig. 6.37 corresponds to the case before optimization. Application of the proposed high frequency improvement solutions corresponds to the case after optimization. The inductance at the inverter output phases (L_{s3}) is increased to 3µH.

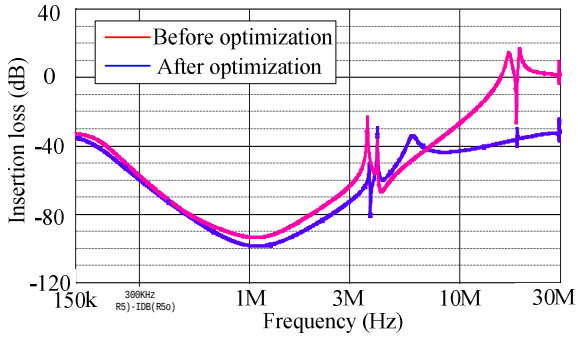


Fig. 6.39 Calculated filter high frequency noise before and after applying the proposed optimized solutions

A comparison of the experimental results before and after applying the optimization solutions is shown in Fig. 6.40. It can be seen that the emitted EMI of the IMS inverter system is effectively suppressed to comply with the standard prescribed by IEC61800-3 C2 QP.

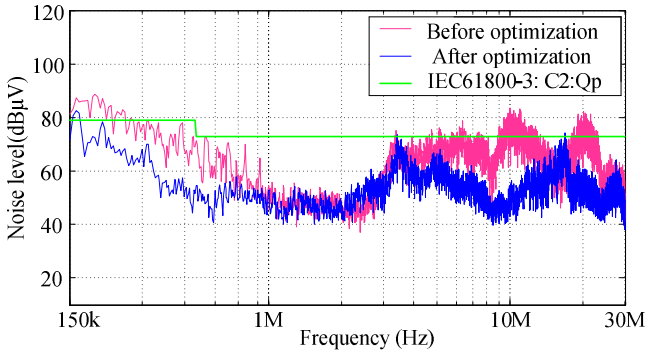


Fig. 6.40 Comparison of the experimental results before and after applying the improved solutions

6.8 Conclusion

Proper filter design is critical for suppressing EMI of the inverters that employ different substrates, because of the created different capacitive coupling magnitude. Applying IMS to improve thermal management of motor drives potentially deteriorates the EMC performance due to its existing extensive capacitive coupling between the circuit copper foil and the substrate base plate.

Firstly, the capacitive influence on both DM and CM performance is analyzed. Based on the understanding gained, the use of separated substrates was proposed as the first method to minimize the capacitive coupling. The EMC performance in inverters employing three different substrate layouts – IMS, single heat sink and separated heat sinks, was presented. The findings of the experiments show that significant EMI difference exists due to applying different substrate layouts. It was presented in chapter 5 that the magnified CM and DM current oscillations by capacitive coupling make the main contributions to the noise in mid and high frequency ranges respectively. Accordingly, it was proposed that ferrite beads be inserted and increasing the filter order be increased for better attenuation.

Secondly, this chapter utilizes the equivalent circuit modeling which was introduced in chapter 3, was utilized as the second method to suppress the IMS capacitive coupling. A CM equivalent circuit model which enables on prediction of the filter performance for the IMS inverter over a broad conducted frequency range, was developed. The optimal filter design is achieved through the insertion loss modeling on varies filter topologies. It is found that the performance of the three-order filter LCL is much better than the others which include the four-order filter – LCLC, hence the filter size and cost are reduced. Lastly, based on the results of the modeling, the methods to further improve high frequency performance are proposed.

The results of the experiments indicated that both methods effectively suppress the emitted noise sufficiently to comply with the standard prescribed by IEC-618003-C2:Qp. Based on the investigations, the required filter design and EMC performance of inverters using three substrate layouts are summarized in Table 6.2.

Table 6.2 Conclusions according to the EMC performance presented by the inverters using three types of substrate layouts

Substrate / Properties	IMS	Single heat sink	**Separated heat sinks**
Capacitive Coupling	High	Middle	**Small**
Without filter	High EMI in low frequency (150 kHz ~ 2 MHz) Low EMI in high frequency (10 MHz ~ 30 MHz)	**Using separated heat sinks has much lower EMI in DM (10 dB highest in mid frequency 2 MHz ~ 10 MHz)**	
With C CM filter	EMI in mid frequency (2 MHz ~ 10 MHz) is significantly higher than others (20 dB at most)	**Using separated heat sinks is slight lower than single heat sink (7 dB at 4.5 MHz)**	
EMI filter implementation	**LCL filter & Ferrite beads**	**LC filter & Ferrite beads**	**LC filter & Ferrite beads, decreased filter capacitor value (compared to single heat sink inverter)**

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

As mentioned in Chapter 1, the emergence of new wide band-gap SiC power devices greatly enhance the switching performance that leads to many advances for power electronics converters. However, these devices also increase the EMI levels, creating the need for mitigating parasitic effects. More filtering efforts are also needed. All of these challenges stimulate this thesis work of containing conducted EMI.

The techniques proposed in this thesis address a variety of aspects to suppress conducted EMI of SiC JFETs based Variable Speed Drive systems. They include equivalent circuit modeling, parasitic cancellations, EMC comparison with IGBT based system, causes of the EMC differences, filter improvement and noise source suppression approaches. The main findings of this thesis are summarized as follows.

Equivalent circuit modeling (Chapter 3)

The equivalent circuit modeling method introduced in Chapter 3 provides acceptable accuracy on EMI level predictions by including high frequency resonances occurring among filter and inverter components. The method is widely applied in other chapters for analysing and predicting EMI levels in motor drive systems. The aim of adding elements in the model is to present details at high frequencies that are influenced by various component resonances and interactions. Depending on the investigation and prediction at concerned frequencies the model can be adjusted by purposing elements that cause the corresponding influences. Hence the predictable frequency range is extended. The method is a compromise between the complicated numerical computations considering associated device physics and oversimplified assumptions. Measurements and curve-fitting of impedance-frequency characteristics are dominant. The method is easy to follow.

3D parasitics cancellation techniques (Chapter 4)

The parasitics cancellation techniques that are introduced in Chapter 4 extend the conventional parasitics cancellation techniques from 2D to 3D by utilizing the multi-PCB integration technology combined with x-dimensional components which are profile unified. By adding planar substrates, the multi-layer PCB technology provides a third dimension layout,

and allows parasitics cancellations to be applied more effectively and flexibility in 3D rather than 2D in single PCB technology. The explored 3D cancellation techniques achieve high component placement flexibility, which is essential in obtaining effective parasitic cancellations while without decreasing power density and adding parasitic inductance. Additionally, IMS substrate or fully copper PCBs can be utilized as shielding layers for filtering capacitors which are more susceptible to noise coupling. Parasitics cancellations increase the filter attenuation ability in high frequencies which is essential in dealing with increased EMI due to SiC fast switching dv/dts or di/dts.

Dominant parameters influencing EMI magnitude (Chapter 5)

In Chapter 5, EMC performances of Si IGBTs and SiC JFETs based motor drive systems using the same layout are compared. It is found that the switching dv/dts and the CM parasitic capacitance between motor windings and the chassis, dominant the CM EMI magnitude. The switching di/dts determine the DM EMI magnitude, because DM impedance is relatively low and mostly inductive. With the comparable driving conditions provided by the gate drivers, the SiC JFET switches at the same speed as the IGBT during turn-on transition, but at more than two times at turn-off. Since the switching speed at turn-off is much lower than that at turn-on, and also the CM parasitic capacitances are the same, the CM EMI emission levels are very similar between the two types of semiconductor based drive systems under unfiltered condition. Since the CM noise is dominant in motor drive systems, the total noise levels emitted from two semiconductor based systems are also similar.

Significantly higher DM noise emitted from SiC JFET system (Chapter 5)

The contribution of turn-off transition of switches is more important than turn-on for EMI emission. Significant DM differences exist between two systems, because DM waveforms are influenced more by the switching speed. In the SiC inverter significantly higher DM parasitic oscillations and overshoots exist. The addition of a filter capacitor further increases the oscillation magnitude. As a result, the DM EMI spectrum is larger. Therefore for SiC JEFTs based drives, DM noise becomes increasingly important and more effort is required during the EMC design. Additionally, since DM contents mainly appear in high frequencies, improving filter high frequency performance thus become essential.

Influence of circuit parasitics (Chapter 5)

Circuit parasitics play an increasing role in SiC JFET based drives due to the significantly higher switching speed. In Chapter 5 it is found that the addition of CM capacitors increases CM and DM parasitic oscillations. Additionally, because of the “Miller” effect and low threshhold gate voltage of SiC devices, fault operations occur more often. It is shown that with the identical CM filter, SiC switching excites larger parasitic oscillations, which is the main contribution to the difference in filter attenuation. The different magnitude of oscillations results in spectral differences in a wide range rather than at discrete frequencies.

High frequency performance improvement (Chapter 5)

The improvement of high frequency filtering of SiC JFET motor drives is achieved by solutions proposed in Chapter 5. The proposed model provides a solid theoretical basis on why solutions are effective and how much more attenuation is gained. When the methods are applied, additional components are required to present high resistivity and a high damping coefficient in high frequencies.

Attachment of power device drain plate to substrate (Chapter 6)

Investigations in Chapter 6 show that the attachment of SiC JFET drain plates to the cooling substrate creates capacitive coupling that significantly deteriorates the EMC performance. The capacitive coupling closes loops with considerable EMI propagations in the mid- and high-frequency ranges. This effect is more critical when SiC JFETs are attached on top of the IMS. In this case two methods are proposed to reduce EMI. The first one is to use separated substrates, which minimizes the coupling by breaking the neutral point of the parasitic capacitors. The method is effective in reducing noise at the source without lowering the system power density. Additionally, two other approaches, RC snubbers across the DC bus and the addition of ferrite beads, are combined with the separated heat sinks, which effectively suppresses the high frequency noise. The second method is based on the equivalent circuit modeling. The proposed model enables predicting the insertion losses of varies filter topologies over a broad EMI band. Hence the optimum filter design has better performance while requiring fewer components.

IMS cooling and increased EMI (Chapter 6)

The EMC performance of an IMS inverter is systematically investigated in Chapter 6. It is found that applying IMS greatly deteriorates EMC performance in mid and high frequency ranges. This is due to extensive capacitive coupling between the circuit foil and metal base plate. It is found that the noise level of an IMS inverter is *20dB* higher than that of a heat sink inverter using the similar layout, with both systems utilizing identical EMI filters. The model proposed in Chapter 6 clarifies this influence and suppresses the increased EMI to comply with the standard.

7.2 Recommendations for further research

Although many achievements and findings as mentioned above are presented in this thesis, some aspects can be improved in order to achieve better results and to further reveal EMC mechanisms.

Equivalent circuit modeling

Since slopes of switching waveforms are time varying, it is recommended that to apply method that is able to represent this nonlinear behavior of the source, thereby achieving more accuracy of the spectral contents in the high frequencies. This information can not be presented by the linear equivalent circuit models.

- The equivalent circuit uses fixed values of impedances to simplify the modeling process. However, in actual situations, the component values (inductance, capacitance, and resistance) are varying, dependent on multi-variables (e.g. frequency, voltage and current). Therefore in different conditions the resulted resonant difference can be shifted from tens of Hz to several kHz.

- Three PWM noise sources at inverter three phase legs are summed as one source that can not present actual situations. In actual situations, especially for AC-AC motor drive conversions, the three inverter legs are switched at different timing sequences. The time interval between transients is not fixed. Additionally, the inverter is operating under a variable range of voltage and current levels. Therefore the voltage and current transient slopes vary. It was found that substituting the idealized square waveforms with the real source signal waveforms as the noise source in the model greatly increases the accuracy of noise spectrum prediction.

3D parasitics cancellation

A systematic approach to perform the 3D parasitic cancellations is recommended because that a trial-and-error process is used, which is very time consuming and complex.

EMI comparison between Si IGBT and SiC JFET based motor drive systems

It is recommended that EMC performance should be compared under optimized circuit layout, and the same power dense conditions. The shortcomings of performing this investigation are:

- The designed inverter layout is not optimized. Parasitics existing in the loop, especially between upper switch source and lower switch drain in one inverter leg, are large. This increases parasitic oscillations and delays the switching speeds of the switches. Although the main goal is to design the same layout for EMC comparisons, inverter layout should be further optimized close to commercial design in order to present more convincing comparisons.

- Much attention has been paid to the gate driver design in order to generate featured signals for the two different types of semiconductors respectively. However physical structure differences were overlooked. The inverter version of using heat sinks is less compact than the inverter using IMS.

Separation of the substrates

This method is easier to apply when the employed substrate becomes small. Therefore it is recommended to apply the method be used for power converters that have high efficiency and small size substrates. The shortcomings of using separated substrates were:

- The proposed method minimizes EMI propagation from switches to earth while it has no effect on other propagation paths. In motor drive systems, the dominant

noise propagation path is the CM capacitance between motor windings and chassis. Although separation of the substrate reduces noise emission from switches, it has little influence on suppressing the noise propagation in the main path. More noise is reduced by adding damping snubbers. Therefore it is recommended to apply this method in converters where noise propagation between power device drain and cooling substrate is dominant.

- Implementation of the method is constrained by the volume of employed substrate. Nowadays cooling substrates for motor drives are usually heavy and bulky. This results in the separation of the substrate being less convenient and the gained EMC benefit becomes less important to compensate the reduction effect. Therefore it is recommended to apply this method in high efficiency, small substrate power converters.

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List of Publications

This thesis is based on the works described in the following journal and conference publications.

1. X. Gong I. Josifovic, and J.A. Ferreira, "Modelling and Reduction of Conducted EMI of Inverters with SiC JFET on Insulated Metal Substrate", *IEEE Trans. Power Electronics,* vol.28 (7): pp. 3138-3146, 2013.

2. X. Gong and J.A. Ferreira, "Investigation of Conducted EMI for SiC JFET Inverters Using Separated Heat Sinks", *IEEE Trans. Industrial Electronics,* vol. 60: 2013. In final production stage.

3. X. Gong and J.A. Ferreira, "Comparison and Reduction of Conducted EMI in SiC JFET and Si IGBT Based Motor Drivers", *IEEE Trans. Power Electronics,* Major Revision.

4. X. Gong and J.A. Ferreira, "Conducted EMI in SiC JFET Inverters due to Substrate Capacitive Couplings", *in Proc. IEEE Applied Power Electronics Conference and Exposition (APEC'13),* Long Beach, U.S.A. March, 2013.

5. X. Gong and J.A. Ferreira, "Comparison and Suppression of Conducted EMI in SiC JFET and Si IGBT based Motor Drives", *in Proc. IEEE 15th European Conference on Power Electronics and Applications (EPE'12),* DS2c.8-1 – DS2c.8-8, Novi Sad, Serbia, September, 2012.

6. X. Gong and J.A. Ferreira, "Modelling and Reduction of Conducted EMI in SiC JFET Inverters with Insulated Metal Substrate", *in Proc. IEEE 4th Energy Conversion Congress and Exposition (ECCE'12),* pp. 629-636, Raleigh, U.S.A. September, 2012.

7. X. Gong and J.A. Ferreira, "Reduction of Conducted EMI for SiC JFET Inverters by Separating Heat Sinks", *in Proc. IEEE International Power Electronics and Motion Control Conference (IPEMC - ECCE Asia'12),* vol.2: pp. 1070-1077, Harbin, China, June, 2012.

8. X. Gong, I. Josifovic, and J.A. Ferreira, "Comprehensive CM Filer Design to Suppress Conducted EMI for SiC JFET Motor Drives", *in Proc. IEEE 8th*

international conference on Power Electronics (ICPE - ECCE Asia'11), pp. 720-727, Jeju, South Korea, June, 2011.

9. X. Gong and J.A. Ferreira, "Three-dimensional Parasitics Cancellation in EMI Filters With Power Sandwich Construction", *in Proc. 14th European Conference on Power Electronics and Applications (EPE'11)*, pp. 1-10, Birmingham, U.K August, 2011.

10. X. Gong and J.A. Ferreira, "Extracting the Parameters of A Common Mode EMI Equivalent Circuit Model for a Drive Inverter", *in Proc. International Power Electronics Conference (IPEC - ECCE Asia'10)*, pp. 892-899, Sapporo, Japan, June, 2010.

Summary

Conducted EMI in Inverters with SiC Transistors

Electromagnetic Interference (EMI) is the main side effect accompanied with the fast voltage and current switching transients in power electronics applications. Compliance of the Electromagnetic Compatibility (EMC) standard is prescribed for any power electronics product before entering the market. In recent years, the new emerged wide band-gap transistor technology Silicon Carbide (SiC) exhibits great potential to replace Silicon (Si) as the dominant transistor because of its superior qualities (e.g. faster switching, higher blocking voltage and higher operating temperature). However, these advances come at the cost of increased EMI resulting from the SiC transistor's faster switching speed and higher switching frequencies. In the past, a large variety of EMI suppression approaches have been developed for motor drive systems. However, most of them serve the conventional Si power devices (e.g. IGBT) based motor drive systems. As the result, exploration of corresponding EMI emission mechanism and new suppression approaches is critical.

The desired EMC investigations should cover the following features of the SiC power devices based drive systems.

- The differences with the Si power devices based motor drive systems and the causes of the differences.
- The common EMC analysis and reduction techniques that can be used for both SiC and Si devices based motor drive systems.
- The approaches that improve the EMC performance for SiC devices based motor drive systems.

In this thesis, with conventional Si IGBTs as the reference, systematic investigations are presented on variable speed drive systems using the latest SiC JFET as the power devices. Main achievements of this thesis are summarized as follows.

System equivalent circuit modeling method for EMC performance evaluation

This modeling method is used for evaluating the noise suppressing performance on varies noise propagation paths of the drive system. Additionally, by introducing the actual noise source emission instead of using idealized noise source (e.g pure square waveforms) emission, improved noise level prediction is achieved. The method is based on curve-fitting of the impedance-frequency characteristics measured on the leads of individual components and between different portions of the system. Various sub-circuits of the system are modeled as RCL composed equivalent circuits in order to represent details within the conducted frequency range. The model development procedure is presented in Chapter 3. Current transfer ratio measurements are used to verify the model. In addition, the model is also applied in Chapter 5 and 6. Chapter 5 utilizes the model to predict the noise emission levels of the SiC JFETs and Si IGBTs based motor drives respectively. Chapter 6 utilizes the model to predict the filter insertion losses. This method is applicable for both SiC and Si based motor drive systems.

Characterization and cancellation of EMI filter parasitics to improve high frequency filtering performance

This study explores the parasitics cancellation techniques for EMI filters with three-dimensional spatial layout that utilizes multi-layer PCB technology and employs surface mount technology (SMT) components. The employed SMT components are named x-dimensional (x-dim) components that have the same height (x=14mm) and double sided SMT electrical terminations. In addition to positioning the employed x-dimensional SMT components 360° in the 2D plane, the components are able to be placed in a third dimension by being stacked onto more PCB layers. This extends the conventional parasitic cancellation techniques to three dimensions. Chapter 4 discusses and implements the 3D cancellation techniques in a LC filter for motor drives. The techniques enhance the filter performance especially in the high frequency range, which is critical to handle the increased EMI due to SiC fast switching speed.

Comparison and identification of noise emission difference between Si IGBTs and SiC JFETs based motor drives

This study compares and identifies the causes of the EMI noise emission differences between Si IGBT and SiC JFET based motor drives. In Chapter 5, two inverter prototypes – with Si IGBTs and SiC JFETs as the power transistors respectively are compared under the same power level and using the same layout. The gate drivers are designed to fully exploit the switching speed for the two types of devices at turn-on transition and to provide the same driving condition at turn-off transition. Their switching waveforms are compared under the inductive switching test condition, using one inverter leg consisting of two switches. The caused EMI level differences are clarified by Fourier analysis transformed from the time-domain measurements. In the system level, their EMI noise levels are compared under unfiltered, C filtered and LC filtered conditions. In order to identify the causes of the noise level differences, the two inverters are operated in the CM testing mode, in which the three top and bottom semiconductors are switched on or off simultaneously at a fixed 50% duty ratio. Hence the maximized CM and DM wave shapes are achieved.

Improve EMI filter to accommodate SiC JFETs in motor drives

In the second part of Chapter 5, the EMI filter design for SiC JFET motor drive system is improved based on the presence of different noise emissions from the Si IGBT and SiC JFET source. An equivalent circuit model is delivered to predict the noise spectrum emitted from the SiC source and stands as the basis for improving the EMI filter design. The proposed EMI method effectively suppress the increased high frequency noise resulted from the SiC faster switching dv/dts and di/dts. The modeled results agree well with the experiments.

Suppression at SiC noise source due to substrate capacitive coupling

Two methods to suppress the noise emission due to capacitive coupling are proposed in Chapter 6. One is to use separated substrate, the other one is to use the broadband modeling. Comparing two inverters that use the conventional heat sink and insulated metal substrate (IMS), the emitted noise levels are significantly different due to the different capacitive coupling magnitude. The first part of the Chapter proposes to use separated substrates. The second part presents a broadband modeling procedure to identify the most effective filter design to suppress the capacitive coupling. Both methods effectively suppress the noise emission to comply with the IEC61800-3-C2 standard. How EMI emission is affected by the capacitive coupling is identified.

Xun Gong
29th July 2012

Samenvatting

Geleide EMI in Inverters met SiC Transistoren

Elektromagnetische interferentie (EMI) is de belangrijkste bijwerking in vermogenselektronica toepassingen, welke gepaard gaat met de snelle spannings- en stroomtransiënten. Voordat een vermogenselektronica product op de markt komt, dient het aan de e*lektromagnetische compatibiliteit* norm (EMC norm) te voldoen. In de afgelopen jaren heeft de nieuwe *wide-band-gap* transistor technologie, *Silicium Carbide* (SiC), aangetoond dat het de halfgeleider schakelaars uit de dominante Silicium (Si) technologie kan vervangen. Dit is voornamelijk vanwege de superieure eigenschappen, zoals hogere schakelsnelheid, grote sperspanning en hoge bedrijfstemperatuur. De vooruitgang in schakelsnelheid echter en de hogere schakelfrequentie van SiC gaat ten koste van een grotere EMI. In het verleden zijn voor aandrijvingen een groot aantal EMI beperkende maatregelen ontwikkeld. Echter, de meeste van deze maatregelen zijn van toepassing op de conventionele inverters, zoals op IGBT technologie gebaseerde aandrijvingen. Hierdoor is onderzoek naar EMI en nieuwe onderdrukkingstechnieken voor deze nieuwe inverters van belang.

Het benodigde EMC onderzoek voor aandrijfsystemen gebaseerd op SiC componenten moet betrekking hebben op de volgende kenmerken:

- De verschillen in EMC bij aandrijvingen gebaseerd op Si technologie en de oorzaken van deze verschillen in vergelijking met SiC technologie.

- Een gemeenschappelijke EMC analyse en reductietechnieken, die kunnen worden gebruikt voor zowel aandrijvingen gebaseerd op SiC als Si technologie.

- De methode, die de EMC prestaties voor aandrijvingen gebaseerd op SiC componenten moet verbeteren.

In dit proefschrift, met conventionele silicium IGBT technologie als referentie, wordt systematisch onderzoek verricht aan aandrijvingen op basis van de nieuwste SiC JFET technologie. De belangrijkste resultaten van dit proefschrift kunnen als volgt worden samengevat.

Evaluatie van de equivalente modellen op het gebied van EMC prestaties op systeem niveau

Deze modelleringsmethode wordt gebruikt om de mate van verstoringsonderdrukking te evalueren en hoe deze varieert voor de verschillende voortplantingspaden binnen de aandrijving. Bovendien, door het gebruiken van de werkelijke stoorbron in plaats van een geïdealiseerde stoorbron, zoals bijvoorbeeld een blokgolf, wordt het mogelijk het stoorniveau beter te voorspellen. De methode is gebaseerd op curve-fitting van de impedantie-frequentiekarakteristiek, welke gemeten is op de aansluitdraden van de individuele componenten en tussen de verschillende delen van het systeem. Verschillende sub-circuits van het systeem worden gemodelleerd als equivalente RCL schakelingen om de details te representeren binnen het toegepaste frequentiebereik. De procedure van de modelontwikkeling wordt beschreven in Hoofdstuk 3. De verhouding van de stroomoverdracht wordt gebruikt om het model te valideren. Bovendien is het model ook toegepast in hoofdstuk 5 en 6. Hoofdstuk 5 maakt gebruik van het model om de stoorniveaus te voorspellen van aandrijvingen welke gebaseerd zijn op de SiC JFET en Si IGBT technologieën. Hoofdstuk 6 daarentegen maakt gebruik van het model om de filterverliezen te voorspellen. Deze methode is toepasbaar op zowel SiC als op Si technologie gebaseerde aandrijvingen.

Karakterisering en het annuleren van EMI filter parasieten om de hoogfrequente filtereigenschappen te verbeteren

Deze studie verkent het annuleren van parasieten in driedimensionale EMI filters, welke gebruik maken van een meer-laags PCB technologie en SMT (surface mount technolgy) componenten. De toegepaste SMT componenten worden *x-dimensionale* (x-dim) componenten genoemd, die dezelfde hoogte (x = 14mm) en dubbelzijdige SMT aansluitingen hebben. Naast het rondom plaatsen van x-dimensionale SMT componenten in het 2D-vlak, kunnen de componenten ook ruimtelijk (3D) worden geplaatst door ze te stapelen op meerdere PCB lagen. Dit breidt de conventionele parasitaire annuleringstechnieken uit naar drie dimensies. Hoofdstuk 4 bespreekt en implementeert de 3D technieken om parasieten te annuleren in een LC-filter voor aandrijvingen. Deze technieken verbeteren de filtercapaciteit vooral in het hoogfrequente gebied. Dit is essentieel voor de verhoogde EMI veroorzaakt door de hogere schakelfrequentie van de SiC technologie.

Vergelijking en identificatie van het verschil in stoorniveau tussen aandrijvingen gebaseerd op Si IGBT en SiC JFET technologie

Deze studie vergelijkt en identificeert de oorzaken en de verschillen in het EMI stoorniveau tussen aandrijvingen gebaseerd op Si IGBT en SiC JFET technologie. In hoofdstuk 5 worden onder dezelfde vermogens- en print lay-out condities twee inverters met Si IGBT's en SiC JFET's vergeleken. De gate drivers zijn zo ontworpen dat de inschakelsnelheid van beide componenten volledig te benut wordt en het uitschakelgedrag is voor beide eender gehouden. Tijdens de testen zijn de golfvormen in één inductief belaste fase-tak gemeten en vergeleken. De veroorzaakte verschillen in EMI niveau worden verduidelijkt door Fourier analyse, welke getransformeerd zijn vanuit de metingen uit het tijddomein.

Op systeemniveau zijn de EMI stoorniveaus onder ongefilterde, met een condensator gefilterde en onder LC-gefilterde omstandigheden met elkaar vergeleken. Om de oorzaken van de stoorniveaus en de verschillen te kunnen identificeren, zijn twee inverters gebruikt in een zogenaamde *common mode* (CM) testmodus. Hierbij worden de drie bovenste en de onderste halfgeleiders ingeschakeld of tegelijkertijd uitgeschakeld met een duty-cycle van 50%. In deze situatie wordt de maximale CM en *differential mode* (DM) golfvorm bereikt.

Verbeterd EMI filter dat geschikt is voor SiC JFET aandrijvingen

In het tweede deel van hoofdstuk 5 wordt op basis van de aanwezige stoorniveaus, veroorzaakt door Si IGBT en SiC JFET bronnen, het ontwerp van het EMI filter voor een SiC JFET inverter verbeterd. Met behulp van een equivalent model wordt het spectrum van het stoorniveau, uitgezonden door de SiC bron, voorspeld. Dit wordt gebruikt als de basis voor het verbeterde EMI filterontwerp. Met de voorgestelde methode is het mogelijk de toename van hoogfrequente stoorniveaus, ten gevolge van hogere dv/dt's en di/dt's veroorzaakt door SiC, effectief te onderdrukken. De gemodelleerde resultaten komen goed overeen met de experimenten.

Onderdrukking van de SiC stoorbron veroorzaakt door de capacitieve koppeling van het substraat

In hoofdstuk 6 zijn twee methoden voorgesteld om het stoorniveau als gevolg van de capacitieve koppeling te onderdrukken. Eén is het gebruik van een gescheiden substraat en de andere maakt gebruik van breedbandige modellering. Door twee inverters te vergelijken, die beide de conventionele opbouw hebben waarbij het koelelement geïsoleerd is van het metalen substraat (IMS), blijkt het stoorniveau aanzienlijk verschillend te kunnen zijn. Dit wordt veroorzaakt door de verschillen in capacitieve koppeling. Het eerste deel van het hoofdstuk stelt voor gebruik te maken van gescheiden substraten. Het tweede deel daarentegen beschrijft de breedband modelleringsprocedure om het meest effectieve filter ontwerp te identificeren en de capacitieve koppeling te onderdrukken. Beide methoden onderdrukken effectief het stoorniveau en voldoen aan de norm IEC61800-3-C2. Ook wordt geïdentificeerd hoe de EMI emissie wordt beïnvloed door de capacitieve koppeling.

Xun Gong
29th July 2012

Curriculum Vitae

Xun Gong was born in Panjin City, Liaoning province, China, on April 4th, 1984. He obtained the Bachelor of Science from Dalian University of Technology, China, in 2006, majored in Control Theory and Control Engineering.

At the same year, he passed national entrance examination for postgraduate and continued his education in Dalian University of Technology for master degree. In the project of his master thesis he developed a Soft-starter prototype for Asynchronous Electrical Machines, supervised by associate Professor Huayi Liu. He obtained his master degree of Control Theory and Control Engineering in 2009.

In 2008, he was accepted as a Ph.D. student with the Electrical Power Processing (EPP) group at the faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS, or in Dutch EWI), Delft University of Technology, the Netherlands. From 22th October, 2008 to 3rd November, 2012 he worked on the project "EMC in Power Electronics Converters" which aims at development and implementation of EMC techniques for industrial and consumer electronics applications.

His research includes EMC strategies, design and applications for mid power (10s of W till 2.2 kW), high density converters, and electromagnetic design of components.