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Molenaar, Margo; Kardan , Fazeh; Shekhar, Aditya; Bauer, Pavol

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Power and Thermal Cycling Testbed for End of Life Assessment of Semiconductor Devices

Margo Molenaar, Faezeh Kardan, Aditya Shekhar, and Pavol Bauer
Dept. Electrical Sustainable Energy - Delft University of Technology, The Netherlands

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***Abstract*—The reliability of semiconductor power devices can be studied by performing a thermal and power cycling test. In order to create the desired temperature cycles, there are four free variables to select during the power cycling test, namely the heating current, heating time, cooling time, and heatsink temperature. In this paper, the relation between the selected variables and the minimum and maximum junction temperature is extensively tested for the silicon IGBT with serial number IKP06N60T. Furthermore, the thermal model is discussed and verified and a rough estimate of the electrical resistance, thermal time constant, thermal resistance, and thermal capacitance are calculated.**

***Index Terms*—Power cycling test, Reliability, Thermal model, Silicon IGBT, Silicon-Carbide MOSFET, Thermal device characteristics, Lifetime testbed**

I. Introduction

Semiconductor devices are essential building blocks in power electronic systems and therefore crucial in our technological society. The most commonly used semiconductor devices are the metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) made from silicon doped with boron and phosphorous [1]. The drive for innovation, like increasing the voltage range and efficiency, has led to the creation of the silicon-carbide MOSFET [2]. The bandgap is increased from 1.12 eV for silicon (Si) to 3.26 eV for silicon-carbide (SiC) [3]. SiC devices have a 2.4 times higher Young's modulus, 410 GPa compared to 169 GPa for Si devices [4]. The coefficient of thermal expansion of SiC devices is $4.0 \cdot 10^{-6}$ °C^{-1}, which is slightly higher compared to $3.5 \cdot 10^{-6}$ °C^{-1} for Si [4], [5].

SiC devices can handle higher operating temperatures, higher voltages, and higher switching frequencies and have lower conduction and switching losses than Si devices [5]. SiC MOSFETs have breakdown voltages up to 3.3 kV and still have a low on-resistance, fast recovery time, and fast switching, while the Si MOSFET has in practice a maximum voltage of 900 V [2], [6].

Another important feature of power devices is their reliability since failures can have severe consequences in e.g. the automotive and aerospace industry [7]–[9]. The semiconductor devices are particularly prone to failure in power converters and machines and are considered a weak link in the system reliability [10], [11]. In most cases, it is not profitable to install new semiconductors and the whole system is replaced leading to more e-waste.

The authors are with the department of Electrical Sustainable Energy in the DCE&S Group at Delft University of Technology. For contact email: F.KardanHalvaei@tudelft.nl.

During the operation of power converters, the generation of power losses results in the occurrence of thermal cycles characterized by repeated heating and cooling. These thermal cycles are primarily caused by variations in the load, switching actions, and environmental conditions. Power semiconductors, which are composed of multiple layers with different coefficients of thermal expansion (CTE), are susceptible to the effects of these temperature cycles [12], [13]. It is crucial to consider these thermal effects and the associated thermo-mechanical stresses in the design and operation of power converters to ensure their reliable performance and longevity. Investigations have shown that thermal stresses account for 55% of all stressors [14]–[18]. Therefore, thermo-mechanical fatigues are the most frequently encountered forms of failure in power devices [19], [20]. For semiconductors with the same geometry, SiC semiconductors will experience larger thermo-mechanical strains inside the device, possibly reducing the lifetime [21]

The thermo-mechanical fatigues that can arise from these thermal cycles are bond-wire cracks, bond-wire liftoff, solder fatigues in the baseplate or chip, and the reconstruction of chip metallization [5], [10], [11], [22], [23]. These phenomena can lead to the deterioration and potential failure of the power devices over time. The most common failure due to thermo-mechanical stresses are bond-wire cracks and bond-wire liftoff because they experience the largest thermal-mechanical stresses since the CTE of the chip ($4{\cdot}10^{-6}$ °C^{-1}) and aluminum wire ($23{\cdot}10^{-6}$ °C^{-1}) differ the most [5], [23], [24].

Due to the time-consuming nature of collecting field data for the reliability evaluation of power devices, accelerated aging tests are frequently employed. These tests, involving power cycling and thermal cycling, aim to replicate the thermal stress effects that power devices undergo when in use [5], [10]. Evaluating the devices' reliability and determining end-of-life under more condensed timeframes is feasible by putting them through accelerated aging tests.

Thermal cycling tests include heating up and cooling down the devices with an external heating source. Power modules are subjected to a controlled thermal condition during thermal cycling tests when temperatures fluctuate between specified minimum and maximum values. The temperature swings could occur quickly and at prescribed rates during the cycle, or they can occur gradually to imitate real-world situations. In

contrast, power cycling tests include periodically applying and removing power to the devices, resulting in active heating due to the power losses. Both tests will replicate the thermal stresses the devices experience in real-world situations and are useful tools to evaluate the device's reliability under various thermo-mechanical stresses [1], [5], [10], [25].

Through these accelerated aging experiments, valuable insights can be gained regarding the reliability of power devices, their main failure mechanism, and expected lifetimes under cyclic thermal loading. This information is essential for designing robust and reliable power electronic systems, as it allows for early identification of potential failure mechanisms and optimizing device lifetimes.

In this paper, the thermal and power cycling tests, used to asses the reliability of the semiconductor power devices, are discussed in Section II. Subsequently, section III explains the thermal model applicable to the semiconductor devices in order to determine the settings of the power cycling test and make the testbed. In section IV, multiple tests are carried out to see the relation between the parameters and the maximum and minimum junction temperature and verify the thermal model. Furthermore, the thermal characteristics of the device, namely the thermal time constant, thermal resistance and thermal capacitance as well as the electrical resistance are determined based on the measurement results. Finally, the conclusion is given in Section V.

II. Methodology

The thermal and power cycling tests are valuable methods to impose thermal-mechanical stresses and determine the semiconductor device's lifetime [5], [10]. During the thermal cycling test, the heatsink is heated and cooled repeatedly. The devices will follow the thermal cycle of the heatsink. During the power cycling test, the pulsating current flowing through the device will heat up the device. During this test, the heatsink has a fixed temperature and is used to cool down the device. The thermal cycles can be executed faster in the power cycling test since only the device itself needs to be heated. Fig. 1 represents the junction temperature cycles obtained during the power cycling test. The other layers of the semiconductor device also experience thermal cycles and since each layer has a different coefficient of thermal expansion (CTE), thermo-mechanical stresses are created between adjacent layers.

The semiconductor devices are thermally connected to both the heatsink and the power cycling machine. The devices can be fixed onto the heatsink with screws and a thermal pad is added in between to fill the air gaps and provide electric isolation. The cables from the power cycling are screwed onto a pre-designed PCB and the devices are soldered onto this PCB. The setup can be seen in Fig. 2.

In the following experiments, four 600V silicon IGBTs are connected in series to the setup. The chosen IGBTs for this experiment are the IKP06N60T from Infineon and are designed for junction temperatures up to 175°C and a peak current of 18A [26]. Fig. 3 shows a schematic representation of the test setup.

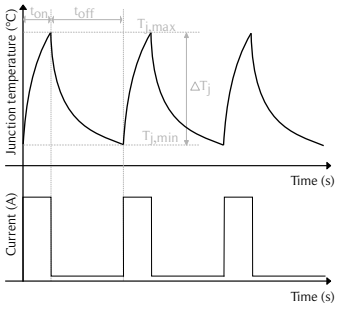

Fig. 1: Illustrative representation of junction temperature cycles created by the pulsating current flowing through the device.

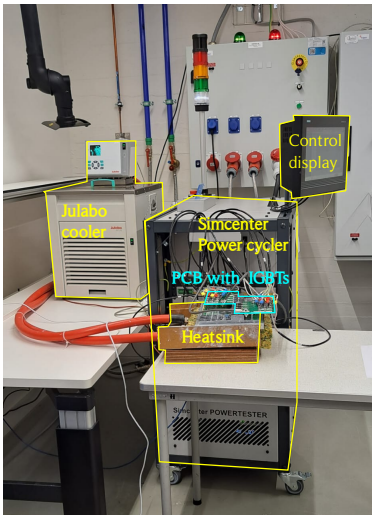

Fig. 2: Picture of the setup between the IGBTs, heatsink, cooling and power cycling machine.

Herein, I_h indicates the pulsating current that will heat up the device. I_s is a small bias current of 100 mA that flows continuously through the IGBT to keep the IGBT in forward-biased mode, such that the voltage drop can be measured to determine the junction temperature. V_{GE} is the gate-emitter voltage and $V_{measure}$ is the collector-emitter voltage drop which is used to calculate the junction temperature. The junction temperature cycles can not immediately be measured with the desired accuracy, so the voltage between the collector and emitter of the IGBT is used since the forward voltage is dependent on temperature. During the calibration, the exact relationship between the junction temperature and the collector-emitter voltage drop is established. For example, the measured relationship during calibration for sample 1 is given in (1) and rewritten to (2).

$$V_{ce} = -3.721 \cdot 10^{-}3 \cdot T_j + 0.789 \tag{1}$$

$$T_j = 212.1 - 267.8 \cdot V_{ce} \tag{2}$$

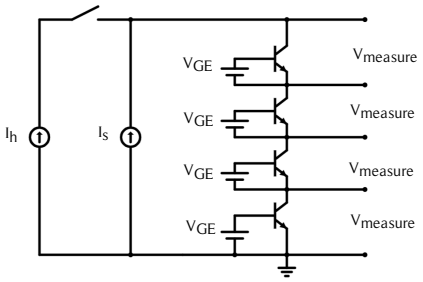

Fig. 3: Schematic representation of the test setup for channel 1 with 4 IGBTs.

III. Thermal model

The thermal model of the device can be simplified to a first-order RC circuit as shown in Fig. 4.

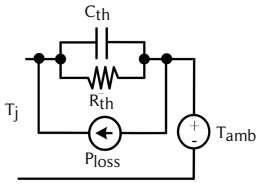

Fig. 4: Simplified thermal model of semiconductor device is a first order RC circuit.

For this first-order RC circuit, the thermal equation is given in (3). By taking the Laplace transformation of (3) and rewriting, we can solve the equation for $T_{\mathrm{j}}(s)$ shown in (4). Converting back to the time domain and substituting $P_{\mathrm{loss}} = I_{\mathrm{h}}^2 \cdot R_{\mathrm{ce}}$ and $R_{\mathrm{th}}C_{\mathrm{th}} = \tau$, we find the expression shown in (5).

$$T_{\mathrm{j}}(t) - T_{\mathrm{amb}} = P_{\mathrm{loss}} \cdot Z_{\mathrm{th}} \tag{3}$$

$$\begin{aligned} T_{\mathrm{j}}(s) - T_{\mathrm{amb}} &= \frac{P_{\mathrm{loss}}}{s} \cdot \frac{R_{\mathrm{th}} \cdot \frac{1}{sC_{\mathrm{th}}}}{R_{\mathrm{th}} + \frac{1}{sC_{\mathrm{th}}}} \\ &= \frac{P_{\mathrm{loss}}}{s} \cdot R_{\mathrm{th}} \cdot \frac{\frac{1}{R_{\mathrm{th}}C_{\mathrm{th}}}}{s + \frac{1}{R_{\mathrm{th}}C_{\mathrm{th}}}} \end{aligned} \tag{4}$$

$$T_{\mathrm{j}}(t) - T_{\mathrm{amb}} = I_{\mathrm{h}}^2 \cdot R_{\mathrm{ce}} \cdot R_{\mathrm{th}} \cdot (1 - e^{\frac{-t}{\tau}}) \tag{5}$$

Lastly, the heating equation of (6) is derived when taking care of the boundary conditions that $T_{\mathrm{j}}(t = \inf) = T_{\mathrm{amb}} + I_{\mathrm{h}}^2 R_{\mathrm{ce}} R_{\mathrm{th}}$ and $T_{\mathrm{j}}(t = 0) = T_{\mathrm{j}}(t_0)$. For the cooling equation of (7), the boundary conditions are $T_{\mathrm{j}}(t = \inf) = T_{\mathrm{amb}}$ and $T_{\mathrm{j}}(t = 0) = T_{\mathrm{j}}(t_0)$.

Heating:

$$\begin{aligned} T_{\mathrm{j}}(t) = (R_{\mathrm{th}} I_{\mathrm{h}}^2 R_{\mathrm{ce}} - T_{\mathrm{j}}(t_0) + T_{\mathrm{amb}})(1 - e^{\frac{-(t-t_0)}{\tau}}) \\ + T_{\mathrm{j}}(t_0) \end{aligned} \tag{6}$$

Cooling:

$$T_{\mathrm{j}}(t) = T_{\mathrm{amb}} + (T_{\mathrm{j}}(t_0) - T_{\mathrm{amb}}) e^{\frac{-(t-t_0)}{\tau}} \tag{7}$$

The thermo-mechanical stresses are strongly related to the thermal cycles. The thermal cycles are represented by the minimum junction temperature $T_{\mathrm{j,min}}$, maximum junction temperature $T_{\mathrm{j,max}}$ and the junction temperature swing $\Delta T_{\mathrm{j}} = T_{\mathrm{j,max}} - T_{\mathrm{j,min}}$. Equation (6) and (7) are rewritten to (8), (9) and (10).

Parameters:

$$T_{\mathrm{j,min}} = T_{\mathrm{hs}} + (T_{\mathrm{j,max}} - T_{\mathrm{hs}})(e^{\frac{-t_{\mathrm{off}}}{\tau}}) \tag{8}$$

$$\begin{aligned} T_{\mathrm{j,max}} = (R_{\mathrm{th}} I_{\mathrm{h}}^2 R_{\mathrm{ce}} - T_{\mathrm{j,min}} + T_{\mathrm{hs}})(1 - e^{\frac{-t_{\mathrm{on}}}{\tau}}) \\ + T_{\mathrm{j,min}} \end{aligned} \tag{9}$$

$$\Delta T_{\mathrm{j}} = (R_{\mathrm{th}} I_{\mathrm{h}}^2 R_{\mathrm{ce}} - T_{\mathrm{j,min}} + T_{\mathrm{hs}})(1 - e^{\frac{-t_{\mathrm{on}}}{\tau}}) \tag{10}$$

Herein, $T_{\mathrm{j}}(t)$ is the junction temperature at time t. $T_{\mathrm{j}}(t_0)$ is the junction temperature at time t_0. T_{hs} is the temperature of the heatsink and can be controlled to implement passive thermal cycles on the test samples. T_{amb} is the ambient temperature, which in this setup is the same as the heatsink temperature. I_{h} is the heating current. R_{ce} is the electrical resistance between the collector and the emitter. τ is the thermal time constant of the system and equal to $R_t h \cdot C_t h$. R_{th} is the thermal resistance from junction to ambient. C_{th} is the thermal capacitance from junction to ambient.

IV. Influence of selected parameters

In the power cycling test, we have four parameters that can be selected to achieve the desired temperature cycle. Those are the heating current I_{h}, heating time t_{on}, cooling time t_{off}, and heatsink temperature T_{hs}. Based on the derived thermal model, it is expected that increasing the heating current and heating time will increase the $T_{\mathrm{j,max}}$ and increasing the cooling time or decreasing the heatsink temperature will decrease $T_{\mathrm{j,min}}$. The thermal resistance and capacitance are inherent to the IGBTs and can not be changed.

The relation between the selected parameters and the resulting temperature cycle will be studied by repeatedly performing the power cycling test. During the test the gate-emitter voltage is set to 15V and the bias current is set to 100 mA. During the measurement the values of the collector-emitter voltage and corresponding $T_{\mathrm{j,max}}$ and $T_{\mathrm{j,min}}$ are determined. On average, the electrical resistance between the collector and emitter is calculated to be 235 mΩ but depends slightly on the temperature.

Furthermore, the thermal model is verified and the missing values of the thermal time constant and thermal resistance are determined with the curve fitting tool of MATLAB. The heating equation (6) has two unknowns, namely the time constant and the thermal resistance, and results in multiple combinations to the curve fitting and it's difficult to decide which is practically realistic. Therefore it makes sense to start with investigating the cooling equation (7) since it has only one unknown, namely the time constant. Secondly, the found time constant can be used as a starting point in the curve fitting of the heating equation (6) to obtain the thermal resistance.

Lastly, the thermal capacitance is calculated according to $C_{\text{th}} = \frac{\tau}{R_{\text{th}}}$.

A. Cooling time

The cooling time only appears in the equation for $T_{\text{j,min}}$ but since $T_{\text{j,max}}$ is strongly dependent on $T_{\text{j,min}}$, both will change by varying the cooling time. The experimental results are shown in Fig. 5. For small t_{off}, $T_{\text{j,min}}$ is way higher than the heatsink temperature. Longer t_{off} will lead to a $T_{\text{j,min}}$ close to the heatsink temperature. $T_{\text{j,max}}$ is less impacted by the change of t_{off} but still varies by 12°C. ΔT is therefore increasing for increasing t_{off} until it's maximum is reached.

By fitting the measurement results of Fig. 5 and (8) using the MATLAB curve fitting tool, we can determine the time constant. The results per sample are shown in Table I. The thermal time constant is around 1.6s. The R^2 and root mean square error (RMSE) values indicate the quality of the fitted curve. The equation after the curve fitting is also plotted in Fig. 5 as a black line.

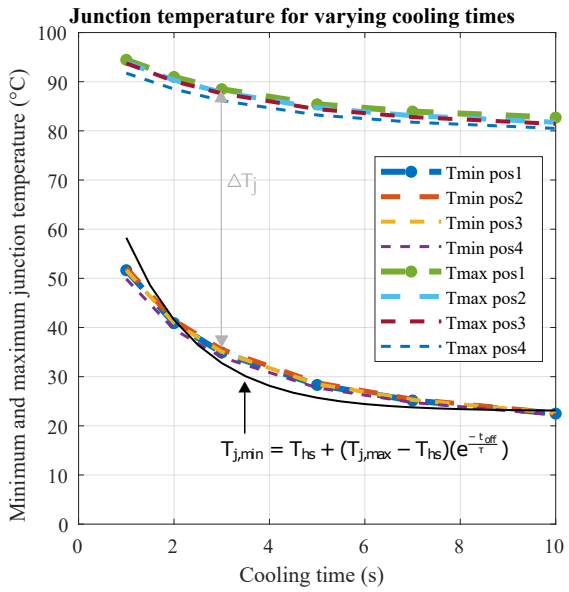

Fig. 5: The relation between the cooling time and minimum and maximum junction temperature. During the experiment $I_{\text{h}} = 10\text{A}$, $t_{\text{on}} = 5\text{s}$ and $T_{\text{hs}} = 20^0\text{C}$.

TABLE I: Results for applying the curve fitting on experimental results of Fig. 5 where the cooling time is varying.

	Pos 1	Pos 2	Pos 3	Pos 4
τ	1.558	1.622	1.586	1.512
R^2	0.7677	0.7642	0.7623	0.7643
RMSE	5.293	5.393	5.33	5.053

B. Heating current

The power losses inside the device will act as a heating source and can be adjusted by selecting the heating current. The relation between the selected heating current, $T_{\text{j,max}}$ and $T_{\text{j,min}}$ is presented in Fig. 6. The selection of the heating current has a large impact on $T_{\text{j,max}}$ and is quadratically increasing as expected from (9). The effect on $T_{\text{j,min}}$ is minimal, in this configuration only 6°C increase is observed, arriving from the increase in $T_{\text{j,max}}$.

By using the curve fitting on the measured results and making use of (9), the thermal resistance and capacitance values are found and presented in Table II. Additionally, the R^2 and RMSE values of the fitted curve are presented in this table. The determined values for the thermal resistance and capacitance are higher than those from the datasheet of the IGBT namely $R_{\text{th}} = 1.67$ K/W and $C_{\text{th}} = 0.164$ Ws/K [26]. This might be because the values from the datasheet are optimistic or due to the addition of the thermal pad and heatsink. Since the R^2 value is almost 1, the theoretical expectation from (9) represents the measurement results well. The analytic equation, shown in black in Fig. 6, starts a little lower than the measurement results and overlaps when applying higher currents.

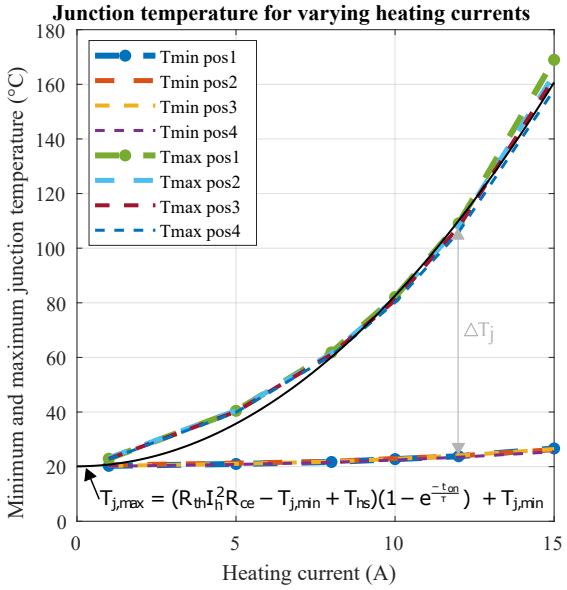

Fig. 6: The relation between the heating current and minimum and maximum junction temperature. During the experiment $t_{\text{on}} = 5\text{s}$, $t_{\text{off}} = 10\text{s}$ and $T_{\text{hs}} = 20°\text{C}$.

TABLE II: Results for applying the curve fitting on experimental results of Fig. 6 where the heating currents is varying.

	Pos 1	Pos 2	Pos 3	Pos 4
τ (s)	2.000	1,756	1,600	1.600
$R_{\text{ce}}(\Omega)$	0.2371	0.218	0.2327	0.2239
R_{th} (K/W)	2.965	3.066	2.808	2.846
C_{th} (Ws/K)	0.6745	0.5727	0.5698	0.5622
R^2	0.9958	0.9966	0.9971	0.9972
RMSE (K)	4.390	3.803	3.497	3.342

C. Heating time

In this experiment, the relation between the heating time and junction temperature is tested and the results are shown

in Fig. 7. Increasing t_{on} will increase $T_{\text{j,max}}$ but eventually will reach a maximum. The selection of t_{on} will have a range of 40°C on $T_{\text{j,max}}$ and 4°C on $T_{\text{j,min}}$ in this setup.

Matching (9) with the measurements, resulted in the time constant, thermal resistance and thermal capacitance as indicated in Table III. Also the electrical resistance for the best fitting is given, which varies slightly per sample. The found values for the time constant are lower than in the experiments before and therefore the thermal capacitance is also lower. The values of the thermal resistance are in the same range as the experiment with the varying heating current. The analytic equation has a larger slope and reaches it's asymptote sooner than the measured results.

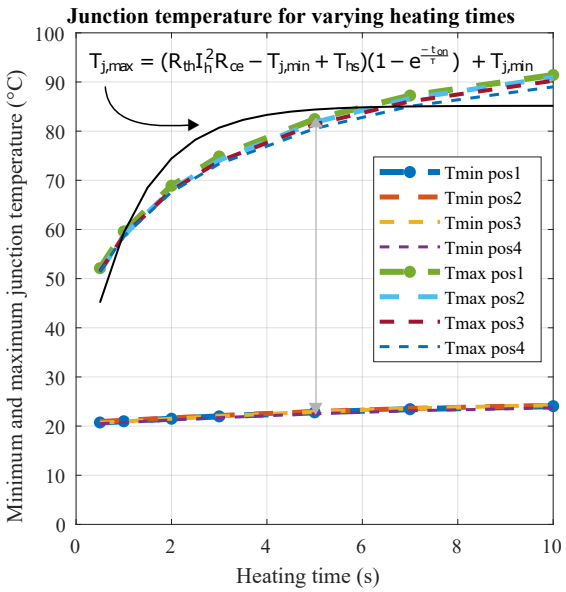

Fig. 7: The relation between the heating time and minimum and maximum junction temperature. During the experiment $I_h = 10$A, $t_{off} = 10$s and $T_{hs} = 20$°C.

TABLE III: Results for applying the curve fitting on experimental results of Fig. 7 where the heating time is varying.

	Pos 1	Pos 2	Pos 3	Pos 4
τ (s)	1.138	1,184	1,148	1.103
$R_{ce}(\Omega)$	0.2243	0.2304	0.2348	0.2175
R_{th} (K/W)	2.909	2.816	2.734	2.898
C_{th} (Ws/K)	0.3946	0.4205	0.4199	0.3806
R^2	0.8555	0.8607	0.8560	0.8540
RMSE (K)	6.754	6.670	6.653	6.503

D. Heatsink temperature

The selection of the heatsink temperature is used to move both $T_{\text{j,min}}$ and $T_{\text{j,max}}$ in an even manner. By fixing the parameter in (8) and (9), the relation between $T_{\text{j,min}}$ and T_{hs} becomes linear similar to the relation between $T_{\text{j,min}}$ and T_{hs}. Nevertheless, the slopes are not the same and ΔT_{j} is slightly increasing as T_{hs} increases.

The results of the experiments with varying heatsink temperatures are shown in Fig. 8. The x-axis shows the setting of the heatsink temperature, but the exact temperature can vary. When the semiconductor devices are heating up, the heatsink area under and next to the device will heat up as well. The temperature sensor of the heatsink is placed lower in the aluminum and will not sense the local temperature fluctuations, the heat should first spread towards the sensor. The air temperature in the room can also have a slight influence on the actual temperature of the heatsink.

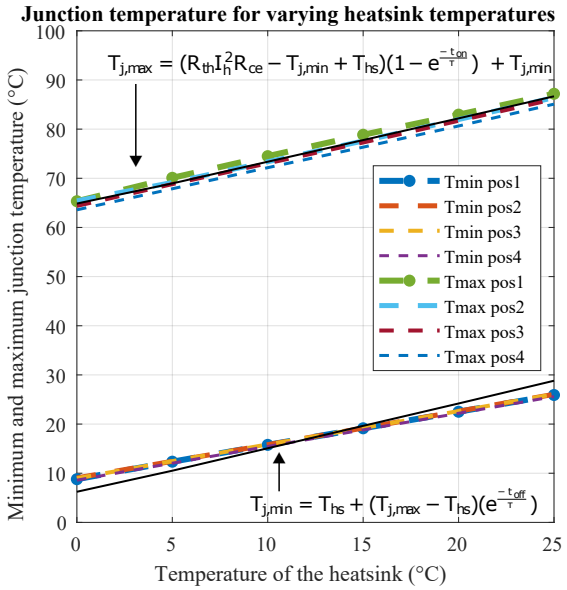

Fig. 8: The relation between the heatsink temperature and minimum and maximum junction temperature. During the experiment $I_{\text{h}} = 10$A, $t_{\text{on}} = 5$s and $t_{\text{off}} = 10$s.

When fitting equation (9) against the measurements results of $T_{\text{j,max}}$, the time constant, electric resistance, thermal resistance and thermal capacitance are found as shown in Table IV. The values are simular to the values obtained in the previous experiments. The measurement results for $T_{\text{j,min}}$ can also be plotted against equation (8). The resulting curve fitting parameters are presented in Table V. The curve fitting was improved by measuring the local heatsink temperature next to the IGBT with another temperature sensor instead of using the selected heatsink temperature. Even so, the values of the thermal time constant are doubled compared to previous experiments, which should not be possible since it is the same setup. We expect that the measured heatsink temperature does not correlate to the actual heatsink temperature at the attachment to the devices and therefore the obtained value of the thermal time constant is inaccurate in this curve fitting.

V. Conclusion

In this paper, the accelerated power cycling test is explained as well as the thermal model of the devices. Furthermore, the relation between the settings of the cooling time, heating current, heating time, and heatsink temperature are extensively

TABLE IV: The values obtained by curve fitting the experimental results of Fig. 8, where the heatsink temperture is varying to the cooling equation (9)

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
$\boldsymbol{\tau}$ **(s)**	1.505	1.500	2.000	1.548
$\boldsymbol{R_{\text{ce}}(\Omega)}$	0.2219	0.2200	0.2265	0.2166
$\boldsymbol{R_{\text{th}}}$ **(K/W)**	2.885	2.871	2.771	2.854
$\boldsymbol{C_{\text{th}}}$ **(Ws/K)**	0.5217	0.5225	0.5734	0.5424
$\boldsymbol{R^2}$	0.9591	0.9629	0.9736	0.9696
RMSE (K)	1.646	1.963	1.698	1.806

TABLE V: The values obtained by curve fitting the experimental results of Fig. 8 where the heatsink temperture is varying to the cooling equation (8).

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
$\boldsymbol{\tau}$	3.584	3.640	3.652	3.529
$\boldsymbol{R^2}$	0.893	0.891	0.893	0.889
RMSE	2.091	2.100	2.089	2.117

tested against the resulting minimum and maximum junction temperature. During each test, the R^2 and RMSE values are reasonable and verify the thermal model. The duration of several power cycling tests can take multiple days to even weeks. Therefore it is important to consider the cycle time, i.e. $t_{\text{on}} + t_{\text{off}}$, and keep it as low as possible while obtaining the desired temperature cycle. It is beneficial to use the heating currents as a free variable over the heating time to obtain the desired $T_{\text{j,max}}$ and keep the cycle time small. The heatsink temperature can be chosen over the cooling time to obtain $T_{\text{j,min}}$.

Furthermore, each test was used to calculate the thermal time constant and if possible also the electrical resistance, the thermal resistance, and the thermal capacitance. Throughout the tests, the obtained values are not identical but their average gives a rough estimate of the values. For this system, $\tau = 1.6$s, $R_{\text{th}} = 2.9$ K/W, $C_{\text{th}} = 0.5$ Ws/K and $R_{\text{ce}} = 220$ mΩ. Using the thermal model, a power cycling testbed with the desired temperature swing can be made.

The obtained thermal model and parameters make it possible to find a suitable power cycling testbed for different heating cycles and loading conditions. This will improve future reliability studies on silicon and silicon-carbide semiconductor power devices.

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