A New Single-Photon Avalanche Diode in 90nm Standard CMOS Technology

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ABSTRACT

A single-photon avalanche diode (SPAD) fabricated in a 90nm standard CMOS process is reported. The detector comprises an octagonal multiplication region and a guard ring to prevent premature edge breakdown using exclusively standard layers. The proposed structure is the result of a systematic study aimed at miniaturization, while optimizing overall performance. The device exhibits a dark count rate of 16 kHz at room temperature, a maximum photon detection probability of 16% and the jitter of 398ps at a wavelength of 637nm. Applications include time-of-flight 3D vision, fluorescence lifetime imaging microscopy, fluorescence correlation spectroscopy, and time-resolved gamma/X-ray imaging. Standard characterization of the SPAD was performed in different bias voltages and temperatures.

Keywords: single-photon avalanche diode, CMOS image sensors, deep-submicron CMOS technology

1. INTRODUCTION

Among solid-state single-photon detectors, CMOS single-photon avalanche diodes (SPADs) have demonstrated their usefulness in applications where single-photon sensitivity, low-noise, high timing resolution, and high dynamic range are important or even critical [1]. Integrating SPADs with high-resolution time-to-digital converters (TDCs) gives them the ability to determine the photon time-of-arrival with an accuracy of a few tens of picosecond [2]. Moreover thanks to CMOS-mediated miniaturization, the integrations of millions of pixels with single-photon detection capability on a single chip is becoming feasible [3]. Hence, the reduction of pixel pitch which is bounded by the scalability of the pixels would facilitate having more electronics on a single imager chip thus putting more functionality for sensing applications [4].

Generally speaking, SPADs are characterized in terms of Photon detection Probability (PDP), dark count rate (DCR), timing resolution, afterpulsing probability, dead time, and the overall speed of operation [5]. Although the smaller CMOS feature sizes advantageously enable smaller pitch, the integration of smaller electronics on-pixel may result in higher fill factor, which, in turn, enables better photon statistics and higher quality imaging. Unfortunately, using deep-submicron CMOS processes involves higher doping, thinner profiles and thicker optical stacks, thus increasing noise and decreasing photon sensitivity.

In this paper we describe the implementation of a SPAD in 90nm standard CMOS technology. By implementing different SPAD structures in this technology we could study the geometric trade-offs involved in the design of deep-submicron SPADs. The paper is organized as follows. After describing the fundaments of CMOS SPADs, we outline the optical characterization of the device in terms of various parameters.

2. SPAD PRINCIPLES AND STRUCTURE

A SPAD is based on a p-n junction biased in the reverse mode of operation above breakdown voltage (Geiger mode) [6]. In Geiger mode, electron and holes generated by photon absorption may initiate a process known as avalanche multiplication [7], whereby each free electron or hole causes a large number of free electrons and holes by impact ionization. The avalanche caused by photon or noise sources must be quenched to prevent destruction of the device by excessive current; this process is known as avalanche quenching and it can be performed using passive or active methods [8].

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In this paper passive quenching resistor is being used for simplicity to explore the highest levels of miniaturization possible in this technology. The avalanche pulse is converted to a digital signal by using a simple inverter. Again, in order to explore miniaturization trade-offs, more complex circuits are intentionally avoided [8].

The noise performance of SPADs is mainly characterized by dark counts which are spurious pulses quantified in terms of mean frequency, or dark count rate (DCR), and afterpulsing [9]. In order to reduce the DCR of a SPAD, different methods should be employed to decrease the Shockley-Read-Hall (SRH) generation, and Tunneling [10]. The sensitivity of SPADs is evaluated by the probability that an impinging photon triggers an avalanche, known as Photon Detection Probability (PDP), that is characterized for different SPADs at different wavelengths. Finally, the timing resolution or timing jitter is defined as the uncertainty of the time delay between the photon impingement and the leading edge of the pulse generated by the sensor.

Fig. 1 shows the cross-section of the SPAD implemented in the 90nm CMOS technology. *Note that all the layers used in designing this family of SPADs are standard in this CMOS technology*. A combination of Shallow Trench Isolation (STI) and n-well is used as a guard ring for preventing the premature edge breakdown. Different types of guard ring with different size and depths were integrated and characterized. The purpose of using a guard ring is to shape the electric field in the active area so as to maximize the high electric field present in the design at the center of the multiplication region and to decrease it at the corners. However, the introduction of some annealing steps near the STI structures which are used in this design can lead to detrimental effects to the noise performance [11].

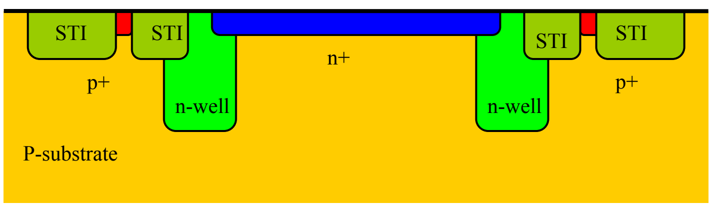

Fig. 1. Cross-section of the implemented SPAD

Fig. 2 shows the photomicrograph of the implemented SPAD in the planar 90nm standard CMOS technology. The photon sensitive area is in the center of the octagonal shape and the other parts are covered with metal in order to reduce the side effect of the absorption of the photons in the guard ring area. The SPAD can be fabricated in different sizes with regarding to the application which is targeted for designing. For the prototype of the SPAD in 90nm technology we used the 8μm diameter size of the octagonal shape.

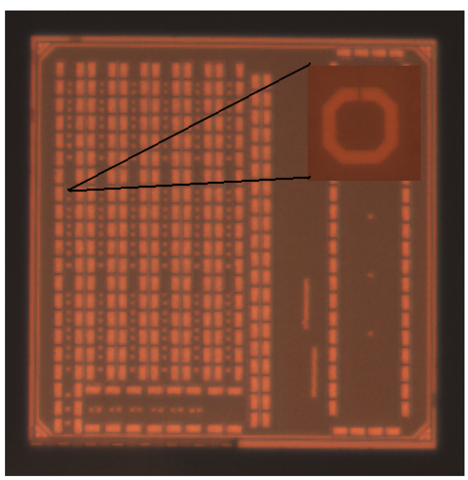

Fig. 2. Photomicrograph of the octagonal SPAD

3. EXPERIMENTAL RESULTS

In order to characterize the number of spurious pulses being generated by tunneling and SRH process the Dark Count Rate (DCR) is being measured. Designing the low DCR SPAD is important for photon-starved applications that are highly sensitive to noise. However, medium or high range noise SPADs can be used in the commercial imaging systems, e.g. 3D vision systems that can use high amount of frame number to omit the intrinsic noise from the device or that are receiving significant background illumination from the scene. Fig. 3 shows the DCR of the fabricated SPAD at different temperatures and excess bias voltages. Passive quenching is being used in the first prototype of the implemented SPAD.

Although tunneling effects increase the DCR with the temperature, the major temperature-dependent DCR contribution is SRH. The SPADs being introduced in this paper exhibit 16 kHz of DCR noise at room temperature with 0.15 volts of excess bias voltage. The DCR can be decreased by further decreasing temperature and/or excess bias voltage. Due to relatively large dead time, the SPAD enters saturation relatively early. The DCR in the plot of Fig. 3 is not being shown after saturation is reached.

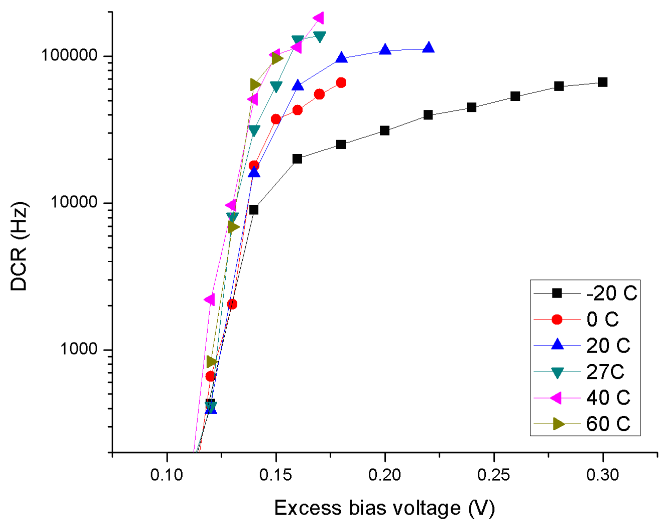

Fig. 3. DCR vs excess bias voltage in different temperatures of the SPAD

The PDP is measured for the entire spectrum of interest (360-800 nm). Fig. 4 shows the PDP of the SPAD at room temperature. The figure shows that the detection probability can be as high as 12% at 480nm wavelength of the light. The shallow doping profile in the 90nm CMOS technology is resulting in a higher PDP in the ultraviolet region and a shift in the peak of the highest PDP to points between 400-600nm. The maximum PDP in different SPADs is in the range of 12-16 %. The lower amount of PDP is predictable due to the shallower multiplication region. This shallow region itself is causing more tunneling.

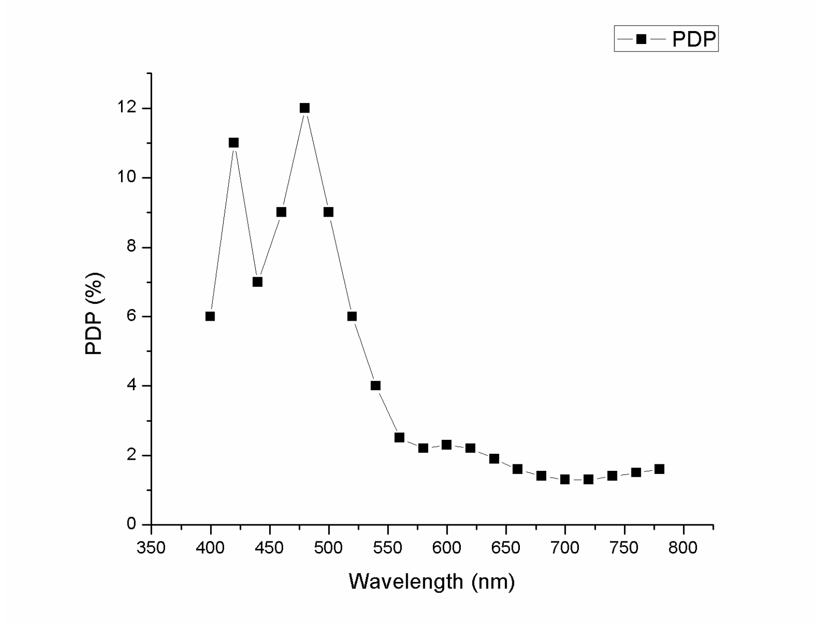

Fig.4. Photon Detection Probability of SPAD at room temperature

The timing jitter is also being characterized in this work. Two fast laser sources with a pulse width of 40ps and repetition rate of 40 MHz emitting a beam of light with the wavelength of 637nm and 405nm, respectively, are being used for the jitter measurement. The time interval between the laser output trigger and the leading edge of the SPAD signal is measured via a high performance oscilloscope operating as a TDC. A histogram is constructed from the time difference of the edges of the laser light and sensing signal. Fig. 5. shows the variation of the PDP in different excess bias voltages at the room temperature.

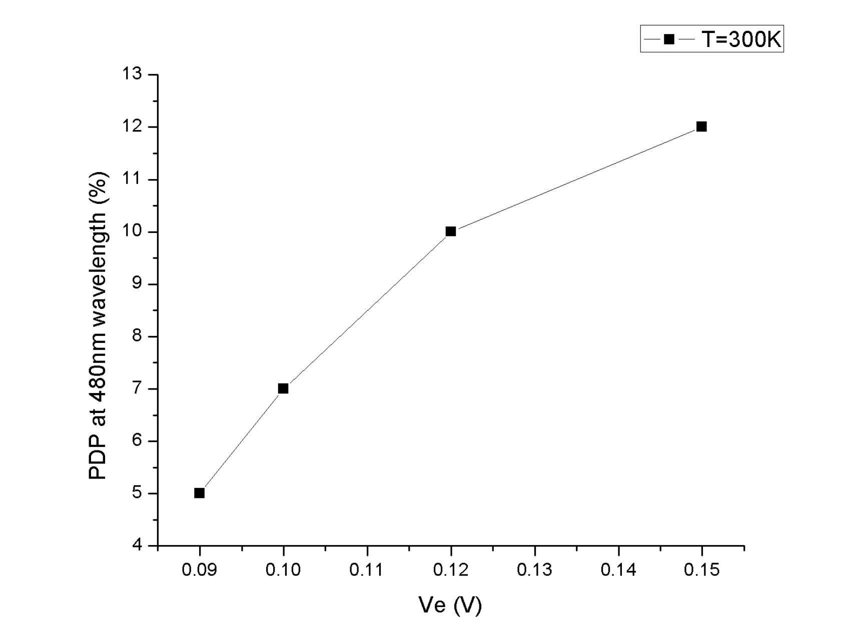

Fig.5. Photon Detection Probability of SPAD at 480nm of wavelength in different excess bias voltages at room temperature

Fig. 6 shows the histogram of this time difference at a wavelength of 637nm. The Full Width at Half Maximum (FWHM) of the time difference histogram was measured to 398ps and 435ps at wavelengths of 637nm and 405nm, respectively.

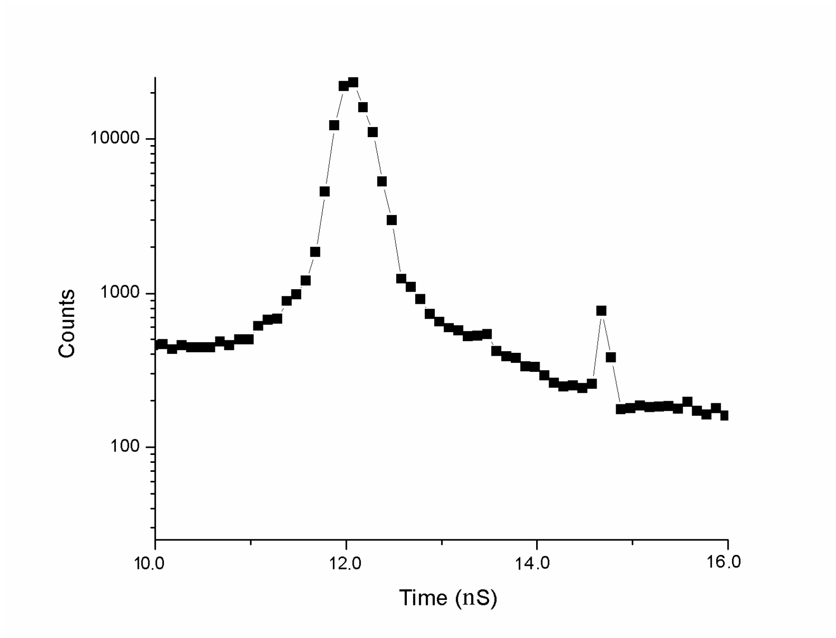

Fig. 6. Histogram of the time between the laser pulse and the SPAD receiving digital pulse.

The performance of the SPAD implemented in the 90nm standard CMOS technology is summarized in Table 1. While the high DCR is expected because of the tunneling and high doping profiles, the PDP is lower due to high, unoptimized optical stack.

Performance	Min	Typ	Max	Unit	Comments
SPAD diameter		8		μm	
DCR		16		KHz	V_e=0.15, T=293K
Timing jitter		398		ps	FWHM at 637nm wavelength
Timing jitter		435		ps	FWHM at 405nm wavelength
PDP		12	16	%	0.15V_e changing with depth and doping of guard ring
Afterpulse probability		32		%	At nominal dead time
Breakdown voltage	10.28	10.4	10.43	V	
Wavelength range	360		800	nm	

Table-1. Summary of experimental results. All measurements were conducted at room temperature.

4. CONCLUSION

The new SPAD reported in this paper, to the best of our knowledge, is the first fabricated in 90nm standard CMOS technology; it comprises a multiplication region and a guard ring to prevent premature edge breakdown, all implemented using standard layers. The breakdown voltage of the SPADs is well-controlled and in a range of 10.28V to 10.43V, while the dark count rate (DCR) tops 16 kHz at room temperature but it can be reduced significantly by cooling. A maximum photon detection probability (PDP) of 16 % was measured while a 398ps FWHM of jitter was achieved in the standard temperature range (-20^{o}C ~ +60^{o}C). Applications include time-of-flight 3D vision, fluorescence lifetime imaging microscopy, fluorescence correlation spectroscopy, and time-resolved gamma/X-ray imaging.

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