JINGCHUN XIANG

Master Thesis

Low Voltage AC-DC Converter Systems for Fast Charging Stations for Electric Vehicles

TU Delft

Master Thesis

Low Voltage AC-DC Converter Systems for Fast Charging Stations for Electric Vehicles

By

Jingchun Xiang

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Abstract

Fast charging technology has accelerated the growth of the electric vehicle (EV) market and attracted significant attention from the industry. Two-stage AC/DC converter system is one of the traditional fast-charging architectures consists of the front-end converter and back-end converter. Numerous researches have developed IGBT-based medium-voltage converter or MOSFET-based low-voltage applications. In this work, a two-stage IGBT-based converter system is proposed in consideration of power switch costs and magnetic component loss.

Three-level T-type converter (3LT^{2}C) has a feasible performance on the switching loss compared with the two-level converter (2LC) and the other three-level topologies for low-voltage applications. Hence, it is suitable to serve as a bidirectional rectifier in the front-end stage. Moreover, the phase-shifted full bridge PWM converter is widely used for high power transformation as the DC/DC converter with galvanic isolation in the back-end stage. The significant advantage of the PSFB is that active switches in the rectifier stage are replaced with diodes which results in low costs of switches and fewer driver circuits. Another strength of the PSFB is that it can operate under zero voltage switching conditions. The design of the AC/DC converter system for EV fast-charging station is presented based on the theoretical calculation. Furthermore, the design procedure and simulation results are introduced and discussed in this thesis.

Key words: ZVS, fast charging, 3LT^{2}C, PSFB

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List of Symbols

P_{ch}	The charging power supplied by the fast-charging station
t_{ch}	The charging period
R_{bat}	The internal resistance of a battery pack
$v_{\text{bat}}(t)$	The voltage of a battery pack
η_{ac}	The efficiency of AC-DC converter
η_{dc}	The efficiency of AC-DC converter
P_{g}	The input grid power
$P_{\text{ch,eff}}$	The effective charging power
$P_{\text{ch,eff}}$	The charging loss power
E_{strc}	The total energy delivered from the storage
T_{strc}	The charging period
m_a	The modulation index
V_{dc}	The DC-link voltage
U_{ref}	The reference voltage vector
T_s	The switching period
$\overrightarrow{SV}$	The switching state vector
$\vec{I}$	The current space vector
P_{cond}	The conduction loss
P_{sw}	The conduction loss
$S_{a,b,c}$	The three-phase switch state
$i_{d,q}$	The current in the dq frame
ω	The angular frequency
$i_{a,b,c}$	The three phase current
D	The duty cycle

D_{eff}	The effective duty cycle
D_{loss}	The duty cycle loss
$N_{p,s}$	The number of windings of the transformer
f_s	The switching frequency
A_c	The cross-section area of the core
V_{core}	The volume of the transformer core
$I_{\mathrm{p1,p2,p3}}$	The characteristic value of the primary current
L_{out}	The inductance of the output filter
t_d	The dead time
i_p	The current of the primary transformer
$I_{p\mathrm{RMS}}$	The RMS value of the primary current
Δi_{out}	The peak-to-peak current in the output inductance
L_r	The leakage inductance
V_{CE}	The forward voltage drop
C_{oss}	The parallel capacitance
B_{PP}	The peak-to-peak flux density
δ_0	The skin depth
σ	The conductivity
μ	The permeability

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Chapter 1

Introduction

1.1 Motivation

Over the past few years, the researches and investigations on climate warming carried out by scientists and governments has gained global attentions significantly. The fossil-fuel-based transportation infrastructure is the main cause of greenhouse emissions which brings out environment impacts such as the melting of the glaciers and climatic anomalies. The internal combustion engines vehicles (ICEV) dominate the transportation market and results in high emissions of carbon dioxide and other greenhouse gases. The static report form Carbon Dioxide Information Analysis Center (CDIAC) indicates that annual global carbon emissions are still increasing dramatically as shown in the Fig1.1 from 1900 to 2015 [1]. The carbon emission originating from liquid fuel takes the second largest share of the global emission around 3000 million tons from 2000.

In order to mitigate the environmental effects caused by carbon emissions, increasing the utilization of renewable energy sources including solar and wind energy are thought to be a sustainable and most effective solution currently. Automobile manufacturers have developed their first modern electric models and enter the stage of commercial operation, proving that electric drives are technically feasible, environmentally friendly, and affordable. Electric vehicles (EV) are promoted by automotive manufacturers and government policies successfully in the last decades. The global electric vehicles market passed 100,000 sales milestone in the spring of 2012, and the battery-electric vehicle sales reach 800,000 in 2017 worldwide [2]. High engine efficiency and less noise emission are the main features that help the share of EVs in global markets to grow rapidly. A list of available EV products with their driving range, the capacity and voltage of the battery is shown in Tab1.1. The battery equipped in most products are lithium-ion technique from Nissan with a typical capacity of 24kWh [3].

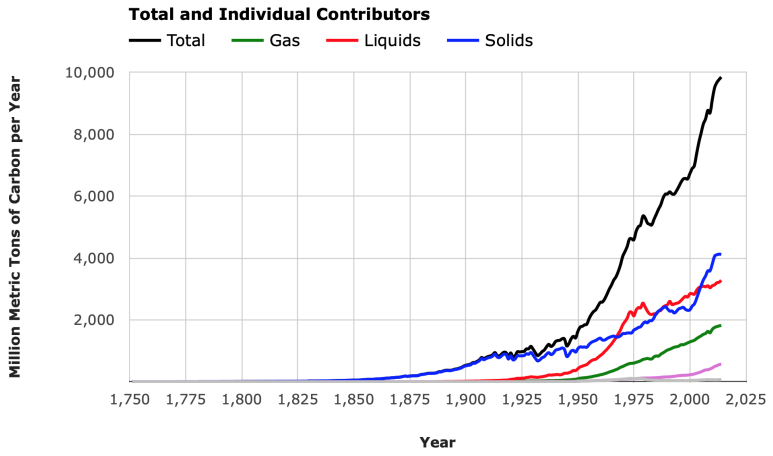


Figure 1.1: Global carbon emission per year in million tons from 1750 to 2016[1].

Table 1.1: The available electric vehicle products in 2019 with the typical features : driving range, the capacity and voltage of battery.

Model	Range	Battery Capacity	Battery voltage
BMW i3	190 km	19 kWh	360V
Fiat 500 e	210 km	24 kWh	360V
Nissan Leaf 2018	400 km	40 kWh	360V
Tesla Model S 70D	442 km	70 kWh	375V
VW e-Golf	190 km	24 kWh	320V
Chevy Spark EV	144 km	21 kWh	330V
Mitsubishi i-MiEV	185 km	22 kWh	350V
Think City 2011	160 km	24 kWh	320V
Kia Soul EV	210 km	27 kWh	360V
Ford Focus Electric	150 km	23 kWh	320V

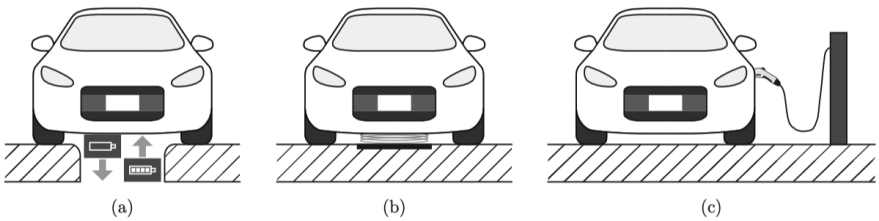


Figure 1.2: State-of-the-art charging methods for an EV: (a) battery swap, (b) inductive charging, (c) conductive charging with AC or DC current[4].

Table 1.2: The table of EV charging level summarizes the charging speed and AC/DC charging voltage and connectors[5].

Charging level and types of charging equipment		
LEVEL1-AC	LEVEL2-AC	DC FAST CHARGING
Slow charging	Medium charging	Rapid charging
120V	208V/240V	200V-600V
1 hour charging= upto 4.5 miles	1 hour charging= 12 miles	10 minutes=up to 40 miles
SAEJ1772 Connector	SAEJ1772 Connector	CHAdeMO, SAE Combo Connector
1.4kW-7.4kW	4-19.2kW	40kW-150kW

Three major charging methods developed by the manufactures to charge an EV are shown in Fig1.2, namely battery swap, conductive charging and inductive charging [4]. The battery swapping technology has been applied with the Renault Fluence Z.E and Telsa Model S for over five years but has not gain as much as public attention as the other two charging technology. Inductive charging methods is a contactless way that gained the public interests successfully. The main reason limits the realization of inductive charging is that it requires an receiver coil for wireless power transfer. The implementation of the coils will decrease engine efficiency at the same. Thus it is hard to promote to the customers. Currently, conductive charging is the most common-used method that requires external connectors to charge an EV with alternating current (AC) or direct current (DC).

The conductive charging can be classified into on-board charging and off-board charging based on the power level and charging currents as shown in Tab1.2. The AC charging enables the EV to be charged by power from the AC grids directly with a charger installed inside the drives. The total weight of the EV is increased and the total engine efficiency will be decreased as well. The DC-fast charging is also called off-board charging that requires an external charging port which provides the galvanic isolation between the AC grid and the EVs and high DC currents to feed the EV battery. Moreover, DC fast-charging technology plays a significant role that mitigates the driving range anxiety of EV, which is concerned by most customers. The main features of the DC-fast charging over the on-board charging are high engine efficiency of the EV and less charging time.

The DC fast-charging stations are normally installed in the public infrastructure in the metropolitan with medium-voltage (MV) gird like charging stations near the highway and commercial buildings. Manufactures and researchers nowadays propose concepts for fast-charging stations with an energy storage system for MV gird application as shown in Fig 1.3. The storage units are generally fed by renewable power sources such as solar energy generated from the photo-voltaic(PV) panels.

However, the number of fast-charging stations in the urban regions is not

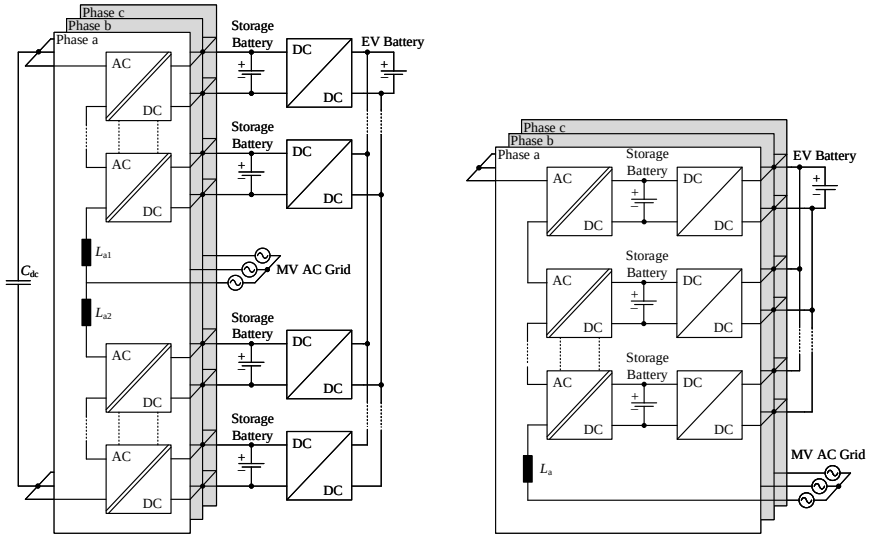


Figure 1.3: Fast charging station based on a split battery energy storage system for medium voltage application

enough which limits the penetration of EVs. A practical method to solve the problem is to launch more fast-charging stations in public areas. One reason that influences the installation of fast-charging stations is that the cost of the external DC charging piles. The cost of the charging piles is determined by the switching frequency and the type of power device used in the circuit. The low switching frequency below 16 kHz will bring noises to the public and require high-cost sound barrier material to build the container of the piles.

The power switch IGBTs or MOSFETs applied in the circuit is another cause. In general, the cost of MOSFETs for high-power application is over four times the cost of IGBTs from the available products in the markets. Several papers depicted the designs which are mainly MOSFET-based without the consideration of losses of passive magnetic components in [5-8]. The loss of the magnetic components including input and output inductor are related to the switching frequency and should be considered for the whole system design. Thus the project motivates to develop a high-efficiency IGBT-based fast-charging stations for EVs with low-voltage (LV) gird.

1.2 Objective

The project focuses on the design of the fast-charging station for EV with low voltage grids in urban areas. The infrastructures and design aspects for EV charging are investigated and defined. Two-stage AC/DC converter system

which consists of the front-end AC/DC converter and back-end DC/DC converter is selected for the fast charging design. Several available circuits including two-level converter (2LC), three-level neutral clamped converter (3LNPC^2) and three-level T-type converter(3LT^{2}C) are investigated and to find a suitable topology for the converter system. The operations of phase-shifted full bridge DC/DC converter with galvanic isolation to achieve zero voltage switching (ZVS) is also studied.

One of the main challenges in this project is the analytical loss models for devices in the three-levels rectifier with space vector pulse width modulation (SVPWM). It is solved by inducing an averaged power loss matrix and and expressed in terms of switching states and current space vectors. The averaged switching and conduction loss model can be calculated by the integrating eclectic angles and elements in the average power loss matrix.

Another challenge of this thesis is to design a highly-efficient converter system. The analytical models and operation points for magnetic components and active power devices are determined. Additionally, the automatic design procedure with inner optimization algorithms is introduced to realize high efficiency. MATLAB and Simulink are used for computation and theoretical models are built to verify the specifications of the design. The losses of power switches are simulated in the software PSIM.

The objectives of this thesis are listed as below

- Investigate the social insight of the electric vehicles, and introduce different charging methods of EV.
- Define the design aspects, specifications of the fast-charging stations with low-voltage-applications and select the charging infrastructure.
- Compare and determine the topologies for a non-isolated bidirectional AC-DC converter and an isolated unipolar DC-DC converter.
- Compare different modulation schemes and apply to the three-level T-type converter, and determine the analytical loss models for power semiconductors.
- Investigate the operation principles and realize soft switching in the phase-shifted full bridge PWM converter
- Realize an automatic design procedure with an optimization algorithm to achieve high-efficiency and high-power-density converter
- Design the control scheme for the power factor correction to realize a unity power factor operation.
- Build Simulink models in MATLAB to verify the performance of fast-charging stations for EV with LV grids.

- Compare the theoretical results generated from the analytical models with the simulation results from PSIM software.

1.3 Outline of the thesis

Chapter 1 describes the motivation and the objective of this thesis.

Chapter 2 defines the design aspects including the charging scenarios and the utilization, charging time and galvanic isolation, as well as the battery capacity of EVs. The state-of-the-art charging architectures and the focus of the work are introduced.

Chapter 3 investigates the merits of widely-used topologies for the fast-charging station for LV applications. The two-stage non-modular topologies is selected which consist of the $3LT^2C$ converter and the PSFB converter. These topologies are compared in terms of control and system complexity, power density, power loss as well as components cost.

Chapter 4 studies the switch commutations and modulation methods of $3LT^2C$. In addition, the implementation of the SVPWM and the averaged loss models are described. A simple control scheme including the inner current control loop and the outer voltage control loop is designed to realize the unity power factor.

Chapter 5 presents the phase shift control and realization of ZVS for a PSFB PWM converter. The design procedures and the loss models of devices and operation points are indicated.

Chapter 6 shows the comparison and analysis of the theoretical results computed from analytical models and simulation results from MATLAB and PSIM.

Chapter 7 summarizes the thesis work and gives the future work for development.

Chapter 2

Fast-Charging Station for Low Voltage Grids

The requirements and specifications must be evaluated first according to the reserved application area, during the design of a fast charging station for the low voltage grid. The number of electric vehicles to be charged during a specific time, the average battery capability of an electric vehicle as well as time to recharge per unit are the main design aspects for manufacturing. The concept of realizing the fast-charging station can be generated in light of the above aspects.

2.1 Design aspects

There are several aspects considered during the design process for the realization of a fast charging station including

- the number of electric vehicles to be charged during a specific time
- the average battery capacity of an electric vehicle
- the required time to recharge per unit
- complying with standards for the galvanic isolation of the EV battery

The desired power delivered from a fast-charging station to the EV is defined by the first three aspects. The fourth one is required to guarantee the safety and reliability of the design. Based on the intended application area, the scales of fast-charging stations are divided into two types: The large fast-charging station is located at highway rest stops, and normal stations are placed in urban infrastructures. The battery capacity is assumed to be higher for EVs charging at the highway because their driving distance is longer than urban fast-charging EVs.Table 2.1 shows the summary of the scenarios for fast charging stations.

Table 2.1: Two scenarios of fast charging station [5]

Parameter	Large station at highway rest stop	Normal station in urban infrastructure
EVs per day	200	44
EVs charging in parallel	6	1
Battery capacity	48kWh	24kWh
Charging rate	1.6kWh	0.8kWh/min
Charging power per unit	96kW	48kW
Total charging power	576W	48kW

2.1.1 Utilization

Monte Carlo methods are performed to simulate fast charging stations in different scenarios [5]. According to the traffic density distribution in Switzerland, the utilization varies from 30 to 220 electric vehicles per day [5,10]. It is assumed that the typical utilization of large and normal charging stations is 44 and 200 EVs per day.

2.1.2 EV battery capacity

The typical battery capacity of midsize EV is set as 24kWh, which allows traveling around 200km. The median of the EVs launched on the market in early 2015 was chosen for this assumption according to Table 1.1. These EVs are mainly used in urban cities because of the limited driving range. Increasing the battery energy content of EVs could provide consumers with a higher range to travel long distances. As shown in Table 1.1, the battery capacity of 70kWh enables Telsa Model S 70D to become the only one available EV with the driving range over 400km currently. For EVs charged at large stations near highway, the typical battery capacity is set as 48kWh since driving distance is longer. As stated by the New European Driving Cycle (NEDC), the average consumption of these electric vehicles is considered to be 12 kWh/100km [9].

2.1.3 Charging time

The maximum power of the DC charging method is up to 63kW defined by the CHAdeMO standard [10]. The voltage and current are limited to 500V and 125A, as which is stated in mode 4 based on the IEC 61851-1 standard [11,12]. The EV battery can be fully recharged in 30 minutes with a 50kW CHAdeMO charging point. Furthermore, EVs and charging stations offered by most manufacturers are in compliance with the CHAdeMO standard.

There are over 32,000 CHAdeMO fast charging stations installed globally [10].

This work focuses on DC fast charging, which means reducing the charging time of a typical 24kWh EV battery to 30 min. This results in a charging rate of 48 kW for a lossless charging process. This is the solution considered for normal charging stations in urban regions. It is assumed that the charging time for the EV battery is 30 minutes and the capacity is doubled to 48kWh for large charging stations. Thus, the effective charging power is doubled to 96kW.

2.1.4 Galvanic isolation

Galvanic isolation is required for EV chargers to comply with standards for safety reasons, which is located between the AC distribution grid and the battery DC bus. In a non-isolated system, people might be electric shocked when touching the AC line and vehicle chassis, as indicated in [13]. The isolated charger is for protecting ground loops and occupants' safety. Furthermore, isolation requirements were defined in IEC 61851-23 to accomplish "protection against electric" for conductive EV charging in 2014. Integrating transformers with converters is one method to achieve galvanic isolation for a DC fast charging system. The transformer could be either low-frequency placed in the front-end converter or high-frequency integrated in the back-end converter.

2.2 The state-of-the-art charging architectures

Two achieved architectures for fast charging station infrastructure are proposed as follows, which are both in the common DC-bus configuration. The first one is generalized for large charging stations near the highways. As shown in Fig 2.1, the station is primarily composed of two stages, namely, isolated AC-DC rectifier and a DC-DC converter. The low frequency transformer and input filter are employed to provide galvanic isolation and reduce harmonic current, respectively. The isolated AC-DC grid interface is used for coupling the DC bus, which regulates the power factor and provides a constant input voltage for the DC-DC converter.

Moreover, the AC-DC converter provides bidirectional power flow between the AC distribution grid and the DC bus. The unipolar DC-DC converter transfers energy to charge the EV battery. Various renewable sources are coupled to the DC bus to provide sufficient power for charging. Thus storage units play a significant role to maintain the stability of the grid.

Several energy storage units including flywheel and battery storage systems are able to coupling to the DC bus directly by connecting non-isolated DC-

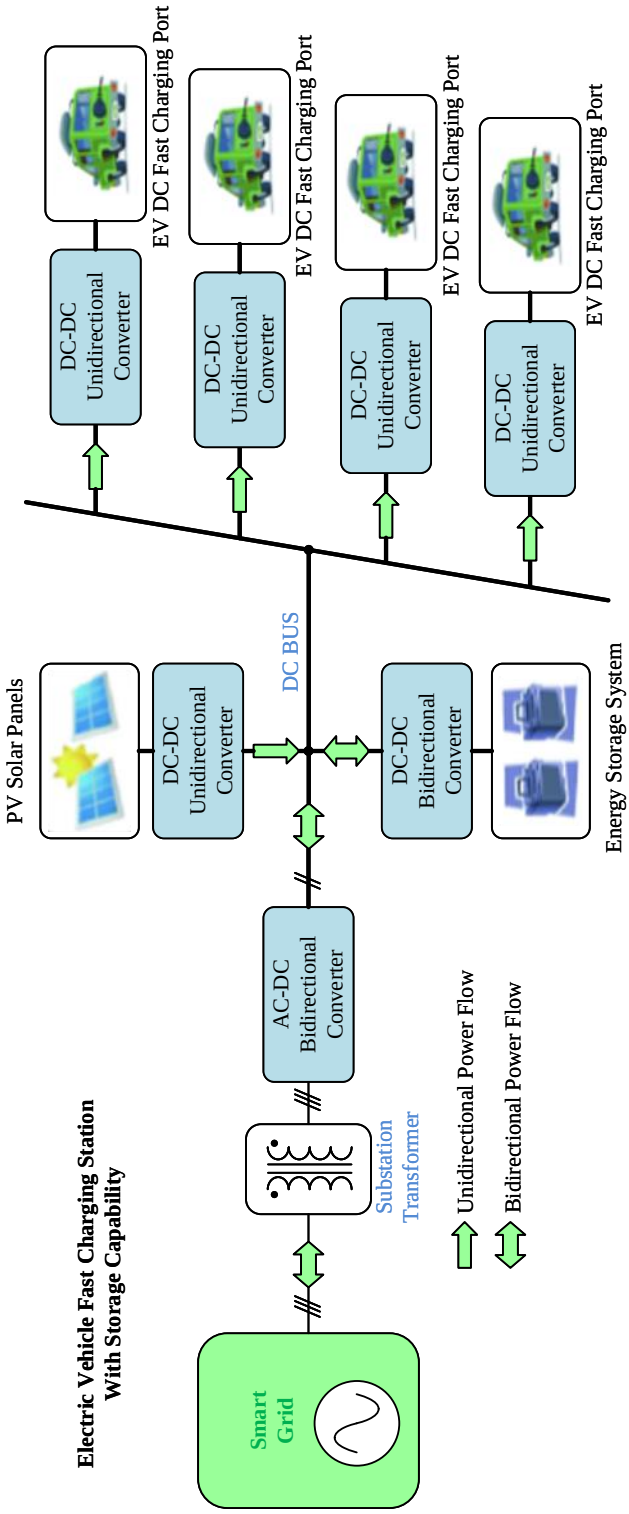


Figure 2.1: Architecture for large DC fast charging stations with MV distribution grid near the highway.

DC converters. Renewable power sources such as photovoltaic panels are able to be integrated to provide energy for EVs as well. Moreover, MV AC distribution grid is always utilized in this architecture, for which high storage and generation units are integrated with large power DC fast charging stations.

The architecture for a DC fast charging station suitable for urban areas is shown in Fig 2.2. The station comprises a nonisolated AC-DC grid interface and an isolated DC-DC energy transfer unit. The power flows bidirectionally between the LV AC grid and the bus DC through the AC-DC converter. The isolated DC-DC converter transfers unidirectional energy from the LV DC bus to EV battery, because of none vehicle-to-grid (V2G) applications. The high-frequency transformer induced in the DC-DC converter provides galvanic isolation between the EV battery and the DC bus. Furthermore, an extra DC-DC energy transfer interface can be added to the LV DC bus for integration of battery storage unit.

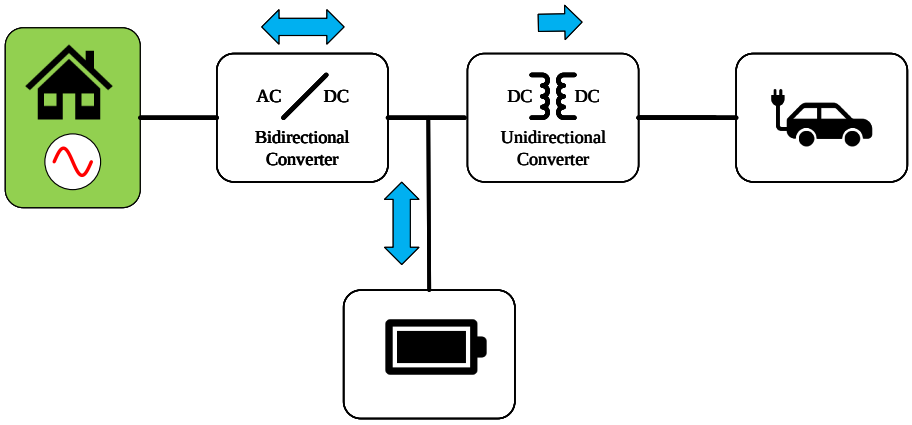


Figure 2.2: Urban DC fasting station with low voltage grid

2.2.1 Focus of the work

Compared to combustion engines (ICE) vehicles, limited driving distance and long time of recharging EVs, the penetration rate of EV is still considerably slow. In urban cities, the EVs are usually charged for a longer time at home or workplace during parking, and the driving distance is relatively short as well. This increases the electric mobility of EV and market interest. An increasing number of charging infrastructures are constructed in metropolitan areas for the coming years. Thus, the demand for fast charging of EVs will increase.

Therefore, this work concentrates on DC fast charging in urban regions as shown in Fig 2.2. Topologies and modulation schemes are selected for the converter system, then the design is developed and optimized to present a high power density and cost-effective fast charging station. Decreasing the number of conversion stages is one essential point to reduce system loss, which is realized by integrating galvanic isolation with the up-to-date converters.

2.3 Specifications and requirements

During the charging process, the resistive loss caused by the internal and contact resistance of EV is required to be covered by the charging power. In this section, the power dissipated by the battery pack is simplified as $i_{\mathrm{ch}}^2 R_{\mathrm{bat}}$. The voltage v_{bat} and internal resistance R_{bat} of a battery pack are generally contingent on the state of charge, which are also non-linear variation depending on the charging pattern. The required charging period is defined as t_{ch}, therefore the required charging power supplied by the converter system is shown as

$$P_{\mathrm{ch}} = \frac{1}{t_{\mathrm{ch}}} \int_0^{t_{\mathrm{ch}}} v_{\mathrm{bat}}(t) i_{\mathrm{ch}}(t) + i_{\mathrm{ch}}(t)^2 R_{\mathrm{bat}}(t) \mathrm{d}t \tag{2.1}$$

The grid power P_{g} input to the fast charging station is

$$P_{\mathrm{g}} = \frac{P_{\mathrm{ch}}}{\eta_{\mathrm{ac}} \eta_{\mathrm{dc}}} \tag{2.2}$$

where η_{ac} and η_{dc} represents the efficiency of AC-DC and isolated DC-DC converter respectively.

Specifications and requirements of the AC-DC converter system for metropolitan fast-charging stations with integration of battery storage units are discussed in detail. These are necessary for selecting power electronics circuit topology and system design to be in compliance with industrial standards.

The rated power and peak value of the input voltage of the converter system are 50kW and 311V. The 230V low-voltage AC distribution grid with three-phase connection meets the IEC 60038 voltage standard. Additionally, the actual charging power could be less than the rated power shown in Table 2.2, because of the possible integration of battery storage units. The extra energy transfer interface is not designed and considered in this work. The energy content size of storage unit is determined by charging power, as well as the charging power is assumed to be the same as the rated power. For the purpose of sizing the battery storage, the losses inside the battery pack are calculated to determine the entire charging power. The charging power simplifies from (2.1) to

$$P_{\mathrm{ch}} = V_{\mathrm{bat}} I_{\mathrm{ch}} + I_{\mathrm{ch}}^2 R_{\mathrm{bat}} = P_{\mathrm{ch,eff}} + P_{\mathrm{ch,loss}} \tag{2.3}$$

Table 2.2: Specification and requirements of the AC-DC converter system for metropolitan fast-charging stations with integration of battery storage units.

	Parameter	**Value**
Converter system	LV AC grid voltage	230V
	Nominal output power	50kW
	Galvanic isolation	Required
	Bidirectional power flow	Required
Battery storage	Storage capacity	100kWh
	Battery technology	Lithium-ion
	Battery voltage	400V

on the assumption that the battery internal resistance R_{bat}, output charging current I_{ch} as well as open-circuit battery voltage V_{bat} kept nearly constant during the charging period.

The desired charging power contains of two parts, where $P_{\text{ch,eff}}$ represents the effective power delivered to the battery pack as well as $P_{\text{ch,loss}}$ is the power covered by the dissipation loss in the battery. The battery pack contains several strings of series-connected cells which are connected in parallel. The resistance of battery cell R_{cell} is specified by the manufacturer, and the resistance of the battery pack R_{bat} is given by

$$R_{\text{bat}} = \frac{N_{\text{cell,s}} R_{\text{cell}}}{N_{\text{cell,p}}} \tag{2.4}$$

where $N_{\text{cell,s}}$ is the number of series-connected cells, and $N_{\text{cell,p}}$ is the number of strings in parallel connection. The Nissan Leaf battery pack is selected as a typical EV battery energy storage unit, the corresponding data are given by the manufacturer AESC [15], with the parameters $R_{\text{bat}} = 125m\Omega$,$N_{\text{cell,s=96}}$, $N_{\text{cell,p=2}}$.

As summarized in Table2.3, the effective charging power $P_{\text{ch,eff}} = 50kW$ mentioned in Table2.1, and the open-circuit battery voltage V_{bat} is 400V. Thus the current through the DC battery charging I_{ch} cable is 125A. The charging loss $P_{\text{ch,loss}}$ and total charging power P_{ch} are calculated to be 2kW and 52kW, which results in a charging efficiency $P_{\text{ch}} = 97\%$. The results and parameters are on the assumption that the temperature of battery pack maintains within $0 \sim 40^{\circ}C$.

2.3.1 Energy Storage

The power delivered from the AC distribution grid P_{g} and power supplied from the battery storage composes charging power P_{ch}. The power of the battery storage unit is determined by the energy E_{s} transferred during the

Table 2.3: Parameters of a typical EV battery pack built with lithium-ion polymer cells.

Open-circuit voltage	V_{bat}	400V
Internal resistance	R_{bat}	125mΩ
Charging current	I_{ch}	125A
Effective charging power	$P_{\text{ch,eff}}$	50kW
Charging loss	$P_{\text{ch,loss}}$	1.9kW
Charging power	P_{ch}	52kW
Charging efficiency	P_{ch}	97%

charging time t_{ch}. With the conversion efficiency of the AC-DC converter η_{ac} and the efficiency of an extra energy transfer DC-DC interface η_{dc}, the charging power $P_{\text{ch}}$is derived as

$$P_{\text{ch}} = \eta_{\text{dc}} \left(\eta_{\text{ac}} P_{\text{g}} + P_{\text{s}}\right) = \eta_{\text{dc}} \left(\eta_{\text{ac}} P_{\text{g}} + \frac{E_{\text{s}}}{t_{\text{ch}}}\right) \tag{2.5}$$

It is assumed that both grid power P_{g} and the numbers of EVs charged per day at the station N_{ev} are fixed, consequently the total energy E_{strc}delivered from the storage media can be presented as

$$E_{\text{strc}} = N_{\text{ev}} E_{\text{s}} = N_{\text{ev}} \left(\frac{P_{\text{ch}} t_{\text{ch}}}{\eta_{\text{dc}}} - \eta_{\text{ac}} P_{\text{g}} t_{\text{ch}}\right) \tag{2.6}$$

The energy stored in the battery pack will be empty without refilling, and the period $T_{\text{strc}}$where no EV charging at the station are available to recharge the storage unit

$$T_{\text{strc}} = 24\text{h} - N_{\text{ev}} t_{\text{ch}} \tag{2.7}$$

The constraint equation for recharging storage is

$$E_{\text{strc}} \leq \eta_{\text{ac}} \eta_{\text{dc}} P_{\text{g}} T_{\text{strc}} = \eta_{\text{ac}} \eta_{\text{dc}} P_{\text{g}} \left(24\text{h} - N_{\text{ev}} t_{\text{ch}}\right) \tag{2.8}$$

which guarantees the storage unit could be fully recharged in 24h. The number of EVs N_{ev} recharged at station reaches to the maximum, as well as the time to restore the energy storage unit T_{strc} comes to the minimal when the constraint is equal.

For the 230V AC low voltage grid, the gird power is set $P\text{g} = 40kW$ and the charging power $P\text{ch} = 52kW$, and the conversion efficiencies are assumed as $\eta_{\text{ac}} = \eta_{\text{ac}} = 96\%$. As listed in Table2.1 the charging time $t_{\text{ch}} = 30min$ and the number of EVs N_{ev} charged per day, thus the desired size of the energy storage unit $E_{\text{strc}} = 74kWh$.

Chapter 3

Converter Topologies

Proper topologies of AC-DC power converter system are evaluated for a fast charging stations with integration of battery energy units as shown in Fig2.2.In this work, it is assumed that the grid power is higher than the DC charging station and no requirements for extra integrated energy storage unit. As previously discussed, the converter system contains a non-isolated bidirectional AC-DC converter and an isolated unipolar DC-DC converter, therefore this section focuses on the selection of suitable power electronic converters. The specifications are:

- connection with three phase low voltage AC grid
- galvanic isolation integrated with DC-DC converter
- bidirectional power flow from the DC bus to the AC grid
- unipolar energy transfer from the LV DC bus to the DC output

The possible low-voltage converter topologies are classified based on their phase modularity, number of conversion stages, and the interconnection type of the modules in the modular topology. The main focus of this thesis is on non phase-modular two-stage converter topologies.

3.1 Non-modular topologies

In LV applications the use of conventional two-level or three-level three-phase AC-DC rectifier/inverter systems is quite common. Their inherently given non-modular structure does not allow a series connection of converters at the AC side to share the voltage across several terminals. In the case of a connection to a LV AC grid, suitable high power semiconductors have to be employed in such designs.

The general topologies with galvanic isolation are described in Fig 3.1, which are two-stage and single-stage non-modular AC-DC converters. For two-

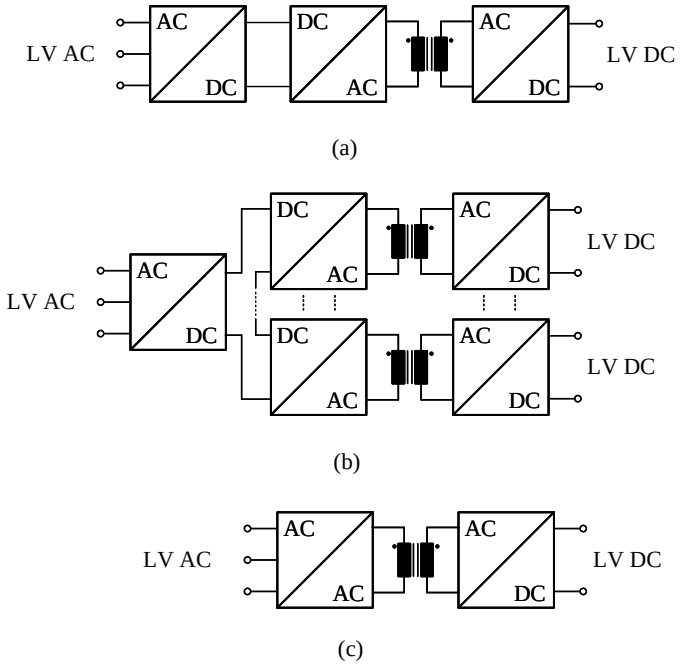


Figure 3.1: Three-phase non-modular isolated AC-DC topologies:(a) Two-stage AC/DC converter, (b)Two-stage AC/DC converter with multiple LV DC outputs,(c) Single-stage AC/DC converter

stage converters, an AC-DC rectifier and an isolated DC-DC converter are connected in series with LV AC input and LV DC output. Two isolated DC-DC converter connected in parallel with the DC side of the AC-DC rectifier and offer two split LV DC outputs. The parallel connection is the one that allows higher current LV DC output series increase voltage. A three-phase single-stage isolated AC-DC converter with LV DC output is also presented.

3.1.1 Single-Stage topologies

The main advantage of the three-phase single-stage converter with galvanic isolation is the high-power density because the number of passive components is reduced. The single-stage topology requires less number of power switch and the volume of magnetic components including transformer and output filter inductance.

The main drawback of the single-stage topology for the high-power charging with low voltage grids is that the control of the converter and the transformer design will be quite complex. Furthermore, the single-stage AC/DC converter is still thought to be as a state-of-art solution which are

not common-used in EV charging.

3.1.2 Two-stage topologies

Two-stage conversion systems are quite commonly used in high power transfer applications. The first stage couples the LV AC grid to the DC bus, where a non-isolated AC-DC converter is employed, also called the front-end converter. The second stage couples the DC bus to the EV. The galvanic isolation is integrated in the isolated DC-DC converter, which is also named as back-end converter. Several advanced non-modular topologies for AC-DC rectifier and isolated DC-DC converter are researched in this chapter.

Non-isolated AC-DC converter

The AC-DC converter with low-voltage application serves as a power factor correction interface, which couples to the AC grid and supplies with the sinusoidal current input. Several suitable power electronic topologies have their specific strengths and weaknesses, which are discussed in this section. This design concerns their characteristics, including costs, efficiency and complexity.

Converters for LV applications face enormous cost pressures. The circuit with the simplest structure and a competitive price which meets all constraints is generally applied. Therefore, constraints are defined based on their basic properties. The features including unidirectional or bidirectional power flow, operation frequency range, and future targets are considered for selection. The future targets such as efficiency optimization not just restrict the behaviors of itself, but can also restrain the interactions of surrounding components. Correspondingly, it is even more complicated to determine the cost of a selected converter topology, due to the taking surroundings into consideration, such as the size and cost of filters.

In this section, the work is concerned with converter efficiency, semiconductor loss as well as the chip area for semiconductors and compares between different suitable topologies.

Though Vienna and Swiss rectifier though perform as a power factor corrector and provide with sinusoidal current inputs, they are not considered for the reason that they are unidirectional interface topologies. There are several types of bidirectional converters including two-level or three-level and multilevel converters as states in [14,15].

It is fairly difficult to compare these widely used converters with features. Therefore, taking the applicability of low-voltage applications and their specific requirements into consideration, this work gives a brief qualitative assessment in order to preselect the topology. Finally, the three most competitive topologies for the LV grid are selected for a more in-depth comparison.

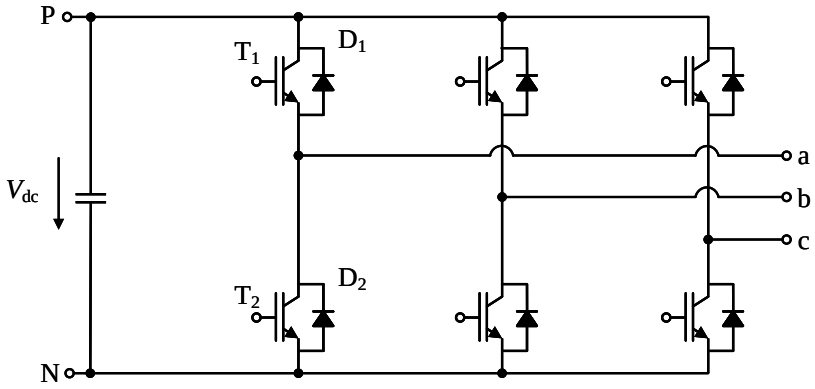


Figure 3.2: The schematic of a two-level (2LC) converter

This work is based on the summary of the three-phase toplologies for LV applications are given by M.Schweizer in [16].

3.1.3 Two-level converter(2LC)

The schematic of the 2-level converter is shown in Fig 3.2. The 2LC is a generally applied as a rectifier at the LV grid side to perform a function of PFC [14].

The 2-level converter consists of 6 parts, and one IGBT is usually integrated with a diode in each part. Therefore, the number of power semiconductors is only 12, which indicates that its simplicity is one major strength. If the all IGBTs in the lower lag $T_{a,b,c}$ are set with same voltage, only four isolated power supplies for all gate drivers, which reduces the expense of the converter. Thus, the 2LC is also considered as a low-cost industry solution for a bidirectional three-phase voltage interface.

Nowdays, manufacturer are still focus on the development of high performance IGBTs, therefore system loss will be considerably decreased and the efficiency of the topology increased. Discontinuous pulse-width-modulation or SiC Schottky diodes can be applied to reduce the switch losses. Turn-off losses are closely to zero for SiC Schottky diodes, and turn-on losses of IGBT can be reduced by 30% because there is no effect of the diode reverse recovery [16,17]. However, the price of SiC Schottky diodes are much more expensive compared to the other diodes with the same power and application.

Another drawback is that the loss might be increased for its surroundings, because the harmonic contents of a two-level voltage waveform will cause

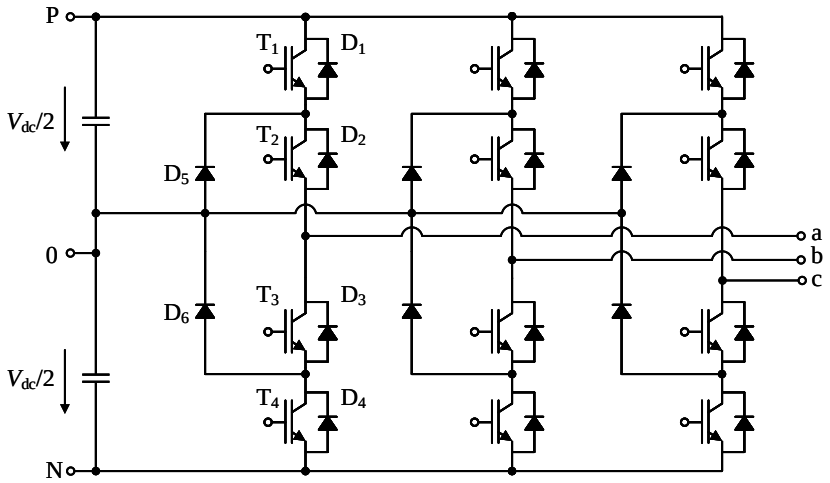


Figure 3.3: The schematic of a three-level (3LNPC) converter

extra losses in passive components.

3.1.4 Three level neutral point clamped converter (3LNPC^2)

The topology of a three-level neutral point clamped converter is shown in Fig 3.3, which are commonly applied in both MV and LV grids. The topology was generated based on the 2-level inverter. As shown in the schematic, the number of capacitors in the DC side increases to 2, and the number of power switch in each phase leg increases from 2 to 4, and two clamping diodes are implmented in each phase. Therefore, the output voltage levels increased from 2 (positive and negative) to 3 (positive, zero and negative). For the reason that the blocking capacity of the power device can not reach to a higher DC-link voltage in the high power applications [16]. Therefore, two semiconductors are series connected to share the block voltage which plays an important role for the medium voltage grid.

The blocking voltage is limited to $V_{dc/2}$ by implement of the clamp diodes $D_{5,6}$, and the diodes are in series connection and also play the function of balancing voltage.

For power devices including IGBT, MOSFET, and diodes, the switching loss is defined to be roughly linear with its commutation voltage. The switch loss will be reduced for a lower commutation voltage, and also reduced for a lower power rating circuit. In addition, based on power semiconductor characteristics, the rated blocking voltage will reduce, which results in decreasing switching loss as well. Therefore, if the 1200 V devices are re-

placed with 650 V for a low-voltage application, the switching losses will be reduced up to five times as observed in [16,17].

Apart from the switching losses, the conduction loss decreases as well. For a fixed current rating circuit, the forward voltage drop of 650 V semiconductor is lower than 1200 V device, and thus the conduction loss will be reduced. However, there is two devices in series carrying the impressed AC current which will have higher conduction losses then the 2L converter when IGBTs and Diodes are used.

In the high frequency operation mode where switching frequency is higher than 10kHz, the switching losses of power devices are dominant, which mainly determines the efficiency of the topology. The increase of conduction loss is compensated by the reduction of switching loss, therefore the losses of semiconductors of 2LC are higher than those of the 3LNPC^2. Furthermore, the harmonic content of two level is higher than 3-level topology, the losses of passive components are higher for 2LC. Therefore, the efficiency of the 3LNPC^2 is higher than 2LC.

It is similar to the 2LC, the reduction of switching losses of 3LNPC can be realized by replacement of 600V SiC Schottky diodes [16]. However, the effect of reverse recover effect does not performance a big difference on a conventional 650V device and on a SiC diode, which means the reduction of switching losses and increment of efficiency are both small. Moreover, considering the material expense of the topology, it is not very advantageous to replace the standard Si diodes devices with 1200V SiC devices. The focus of reducing of switching losses moves to cut down conduction losses, which is a strength of the three-level T-type converter, which is discussed in the later section.

Comparing with 2LC, the topology of 3LNPC^2 is more complex and the total number of power semiconductors increased form 12 to 30, which is its main drawback. Apart from the power devices, the number of gate drivers also increased to 12, which means the material expense also increases.

In comparison with the 2LC, the power semiconductor in the 3LNPC^2 could be replaced with one with a smaller rated current. Since the distribution of converter losses is over a higher number of devices, it results in a smaller rising in junction temperature. Thus the semiconductor chip areas can be reduced as well [14,17]. In consideration of the energy savings caused by a higher converter efficiency and less loss in the passive devices, manufactures might prefer 3LNPC^2 rather than 2LC.

In summary, because of the low switching losses and less harmonic contents in three-level voltage outputs, the 3-level neutral clamped converter is consider to be a suitable choice for LV applications.

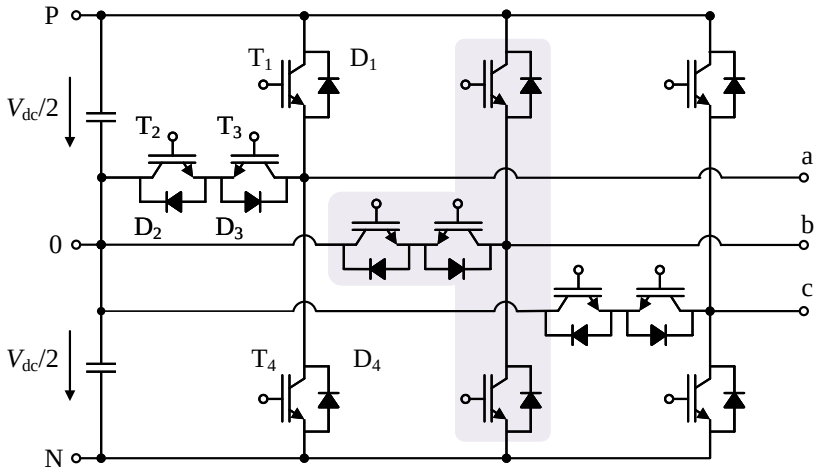


Figure 3.4: The schematic of a three-level T-type converter

3.1.5 Three-level T-type converter($3LT^2C$)

The topology of the three-level T-type converter was generated in the late 1970s as shown in the Fig 3.4 [16,19]. The $3LT^2C$ is developed based on the 2LC, and each phase is connected with a bidirectional switch to the midpoint of the DC link. Since the $3LNPC^2$ has successfully dominated the market of low-voltage and medium-voltage applications [20]. The $3LT^2C$ gained widespread attention until the late 1980s and widely used after the year of 2008 to develop high-efficiency converters for solar systems [18,20].

The positive side switch and negative side switch are usually both employed with 1200 V devices to block the full voltage of the DC link V_{dc}. Because the bidirectional switches are connected to the DC-link midpoint, the block voltage cut down to half $V_{dc}/2$. Therefore, two 600V IGBTs with antiparallel diodes are implemented on each phase, which is served as a bidirectional switch. It is similar to the previous discussion, though two devices are series-connected in each phase, the low switching losses and conduction losses are reduced considerably because of the lower rated voltage.

There are no series-connected devices on both positive and negative sides to block the full DC-link voltageV_{dc}. The output of the topology is connected to the positive and negative ports. The forward voltage drop only occurs on one device rather than two series-connected devices in the $3LNPC^2$, which achieves a reduction of conduction losses [21].

Compared with the $3LNPC^2$, the switching losses is higher because there is a 1200V device switching. As mentioned before, the switching loss of a power

device is defined to be generally proportional to its commutation voltage. In this case, the blocking voltage is reduced to $V_{dc}/2$ compared to the full voltage V_{dc} in the 2LC, thus it reduced the switching losses [17]. Both 1200V and 600V devices are implemented in the topology, the switching losses can be approximately calculated according to the datasheets. The switching losses of a device are specified for different rated voltages.

Another strength of implement of 1200V devices is that, the full DC-link voltage could be directly transited between the positive and the negative during the switch transitions. The clamping diodes limits the blocking voltage of the DC- link to $V_{dc}/2$ in the 3LNPC^2. However, for two semiconductors in series connection, the direct transition of full DC-link voltage from positive to negative are normally neglected [20,21]. The problem of voltage balancing might occur when the two series-connected IGBTs turn off simultaneously. This adverse effect not exists in the topology of 3LT^{2}C, which makes it a suitable solution for the low-voltage applications.

3.1.6 Multilevel Converter (MMC)

A series connection of power semiconductors in each phase to block the high dc-link voltage are developed for a multilevel converter. The number of voltage increased as the number of series connected switch. For a high power system for medium-voltage applications, it requires a high blocking voltage which can be increased by employing series-connected high power semiconductors. The gated drivers supply control signals to several switches to extend a higher blocking voltage.

The number of voltage levels can be increased by decreasing the number of power devices in the multilevel converter. Therefore, the MMC will offer a better sinusoidal voltage level waveform than three-level converters and its total harmonic distortion will be lower. Therefore the losses of the passive components such as filtering inductors from the grid side will be reduced.

Two common types of generalized multilevel converter topology are shown in Fig 3.5, which are namely diode-clamped MMC and capacitor-clamped MMC (also named flying-capacitor MMC). The five-level converter is presented for instance, one phase leg structure of the two topologies are presented in Fig 3.5(a) and Fig 3.5(b).

As the number of voltage levels increased, the system will become more complex and the total cost will rise with the number of power semiconductors, gate drivers and capacitors. For a rated voltage level, the reduction of switch losses can be realized by the employing low voltage switches [22]. Through the implement of lower rated voltage switches, the switching speed is faster and the switching losses are lower compared to the three-level converter and two-level converter. The conduction will be reduced as well because of

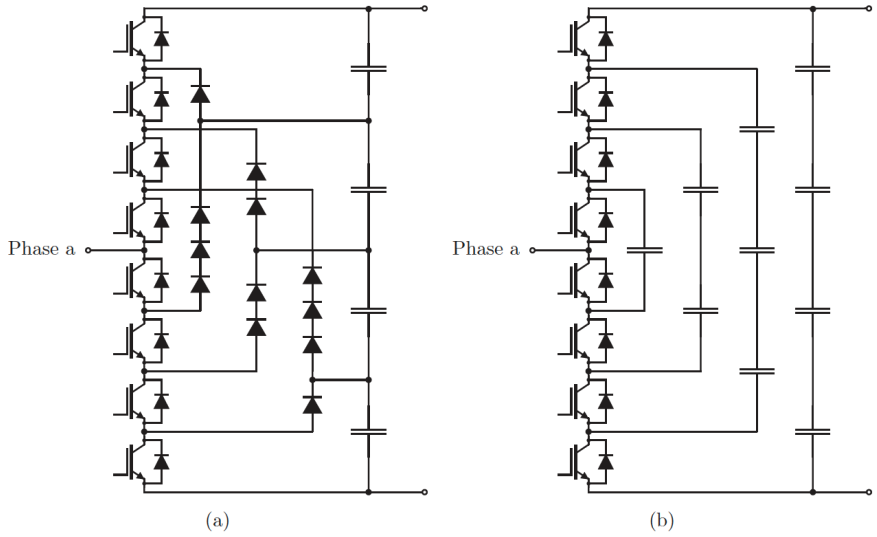


Figure 3.5: The schematic of a 5-level MMC converter

a lower the forward voltage drop in case LV MOSFETs are used. However, for the converter design, it will increased the complexity in the process of selecting power switches.

3.2 Isolated DC-DC converter

The isolated DC-DC converter is necessary to provide galvanic isolation for safety issues. An overview of galvanically isolated DC-DC converters is depicted in Fig 3.7. The topologies are classified based on the structures of converters into single switch, half-bridge, full bridge as well as multi-phase structure.

Dual active bridge converters are widely used for high power transfer, which convert the DC bus voltage down to the output voltage. The schematic of an isolated DC-DC dual half bridge with a single-phase transformer is shown in Fig 3.7(a), and the dual full bridge converter with a single-phase transformer is shown in Fig 3.7(b), a three-phase DAB converter with a three-phase converter is displayed in Fig 3.7(c). The series resonant converter and the parallel resonant converter are generated by adding a series or parallel resonant inductor and capacitor to the converter.

In addition, a modular approach is applied for low-voltage and medium voltage isolated DC-DC conversion [23]. The DAB serves as a module for a 3kW 700V to 400V converter, the modules are in series connection with the input and connected in parallel at the output. The modular multilevel

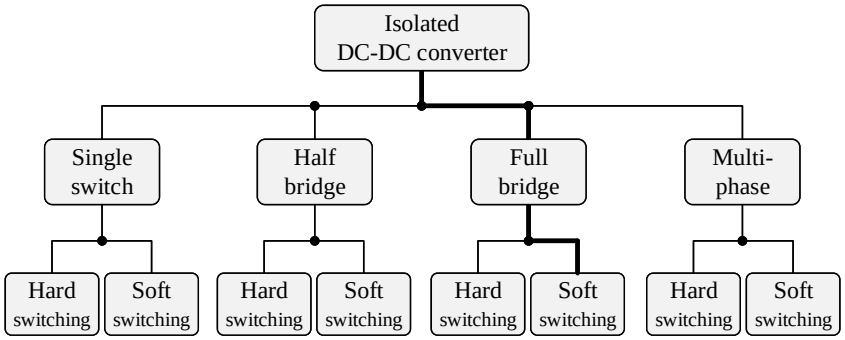


Figure 3.6: Overview of galvanically isolated DC-DC converters

converter is another realization of modular DAB approach as presented in [24].

Isolated DC-DC converters which transfer unidirectional power from the DC-bus input to the DC side output are preferred. Nevertheless, several works present the application of the bidirectional converters with advanced controls for the low-voltage side to improve the efficiency of the system. Beside the vehicle-to-grid application is not considered, due to the increased number of power semiconductors and gate drivers, as well as a more complex control method, the suitable bidirectional topologies are not investigated in the following. The following work to investigate the state-of-the-art isolated DC/DC converters is according to the overview of telecom DC-DC converters given by U.Badsubner [25].

Flyback and forward converters are typical isolated single-switch converters widely used for low-power conversion. The low complexity and a smaller number of power components are the strengths of single-switch converters for low-power applications [20]. Additionally, auxiliary circuits are used to achieve soft switching for the basic hard switching converters, which increase the number of components and complexity for the system. In the consideration of reliability, the single switch topology is not considered. It is not practicable for a high-power converter because of the massive magnetic components [26]. Both the size and weight of the transformer in the forward converter or winding inductors in the flyback converter make it not attractive to high power and high efficiency applications. Furthermore, the number of available power devices is reduced because the blocking voltage of switch is twice the input voltage. The blocking voltage of switch is minimum to 1kV for high power application, compared to the other toplogies, for example in a full bridge converter, 600/650V IGBT and MOSFET are suitable for a high performance system. Thus, the isolated single-switch DC-DC

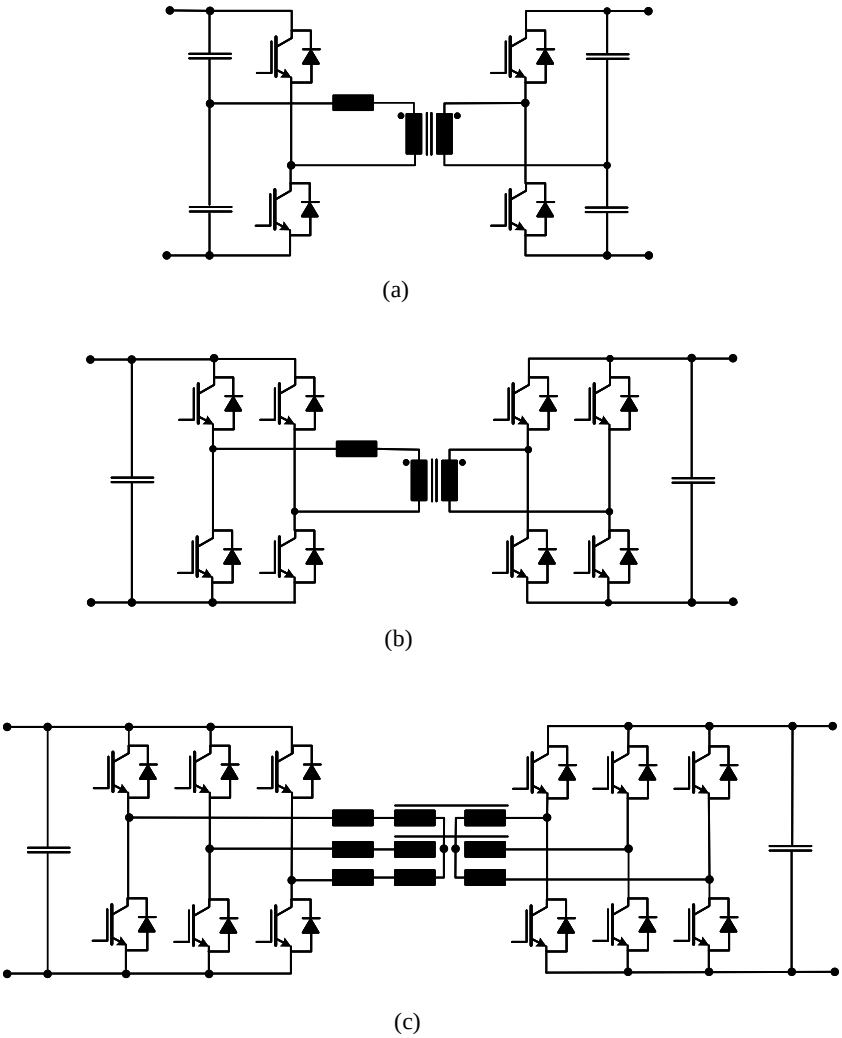


Figure 3.7: Isolated DC-DC dual active bridge converters: (a) the DHB with a single-phase transformer (b), and the DFB converter with a single phase transformer (c) the three-phase DAB converter with a three-phase transformer.

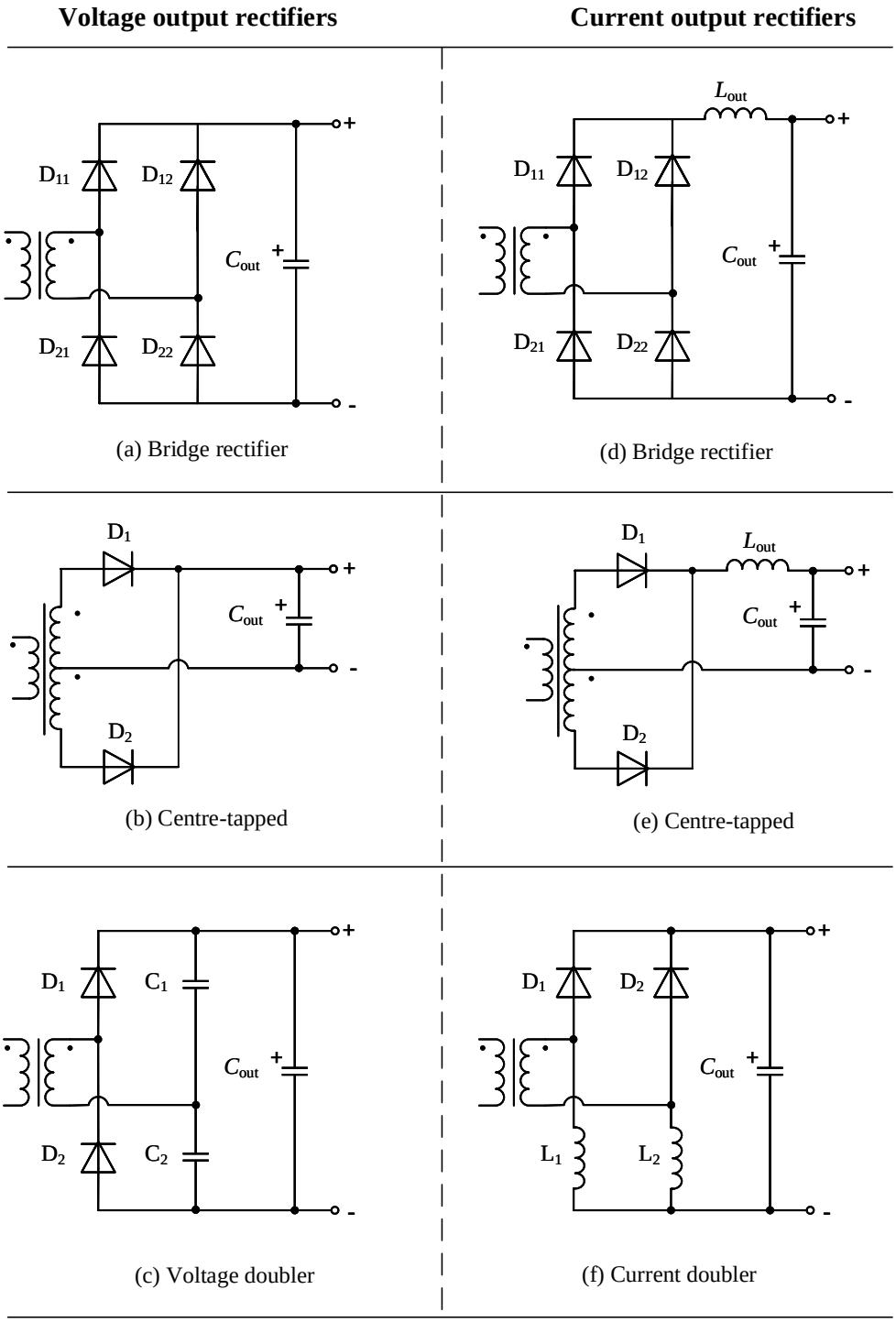
converters are not considered in the following investigation.

There are several applicable topologies in the rectifier stage able to be connect with both the resonant and PWM two-stage inverter topologies. Based on the outputs of the topologies, these are divide into the voltage output rectifiers and current output rectifiers. The basic full-wave rectification stage shown in Fig 3.8 is briefly described in the following. Due to the bidirectional magnetization of the transformers, several types of full-wave rectifiers are developed for both the half and full bridge converters, which are shown as Fig3.8.

Full-wave rectifier stage The bridge rectifier is invented by Leo Graetz, and it is the most common used full-wave rectifier as presented in Fig 3.8(a). According to the polarity of the input voltage, which is applied to the transformer, the two diagonal diodes in the H-bridge will conduct when the output voltage of the filter C_{out} is higher than the input voltage. Omitting the voltage drop over line resistances and parasitic inductances, the output capacitor voltage is clamped by the blocking voltage of the diode. One weakness of the topology is that two of four semiconductors are conducting at the same time, which results in high conduction losses. Another drawback is that there is no inductor in the secondary side circuit, thus it requires a sufficient large inductor to limit the slope of the primary side current. Moreover, the magnetic flux in the transformer is usually high for the high-power application. Therefore, it results in a high capacitor, and there will be a trade-off between component volume and losses.

The are only two diodes in the rectifier stage for a full wave centre-tapped converter as shown in Fig 3.8(b). The number of switch device and conduction losses are both reduced for high-power applications, compared with the bridge rectifiers. The main drawback of this topology is that the transformer design and selection process becomes much more complex due to the two series-connected windings. Moreover, the leakage inductance exists in the two windings which will inluences the current flow in the rectifier [27]. Therefore, the voltage rings will be larger because of the commutation of current is not ideal in the rectifier stage. Another drawback is that it requires a higher the voltage rating compared with the bridge rectifier. It is the sum of the output voltage V_{out} and the voltage of the primary side in the transformer. The slopes of current and voltage are required to be decreased in the inverter stage.

The structure of the voltage doubler is similar to the centre-tapped rectifier. There are also two diodes and two extra capacitors as well as a single secondary winding in the topology. It combines the advantage of a single design of transformer from the full-bridge converter and the strength of centre-tapped with less power devices. One capacitor is recharged in and another one blocks the voltage in each half-wave. The output capacitor C_{out}



(a) Bridge rectifier

(d) Bridge rectifier

(b) Centre-tapped

(e) Centre-tapped

(c) Voltage doubler

(f) Current doubler

Figure 3.8: Full-wave rectifier topologies for the half or full bridge the DC-DC converter. The diodes can be other power switch IGBTs or MOSFETs for bidirectional power conversion. Gate drivers can be connected to the switch with controllable signals.

in the filter is usually small or can be removed for the design. For high-power application, the current flow in the rectifier stage is always high and continuous, and the energy charge in the capacitor is quite high at the same time. Therefore, it requires a large bulk capacitor to achieve a standard output voltage ripple [28]. This limits the voltage doubler topology to be a suitable choice for the low-voltage design for EV charging.

The output inductor L_{out} is applied in the output filter as shown in Fig 3.8 in a bridge rectifier. The utilization of the inductor increases the system losses and total component volume. The filter inductor serves to limit the slope and ripple of the output current, and it influences the primary side current in the inverter stage. In addition, the implementation of the inductor also requires a higher blocking voltage of the diodes due to the voltage drop over the inductor. Another advantage of the LC output is that the current measurement in the inverter stage can be omitted and provide a high quality current output. Though by extending the full bridge topology with an output inductor the converter becomes more complex, the current output converter is a precise choice for high-power applications.

Fig 3.8(e) presents the centre-tapped converter extended by the output inductor. The drawback of the topology is similar as previous presented, the voltage rating is increased; thus, there are less applicable power devices for system design. It is preferred for the high smooth current output applications. In addition, it combines both the strengths and the drawbacks of the LC output filter and the centre-tapped rectifier. The complex transformer design and less applicable semiconductors limit its utilization. The current doubler rectifier stage as shown in Fig 3.8(f) has the same problem as the voltage doubler, the desgin of transformwer will be more complicated and will increase the total volume of the system [29].

These full-wave rectifiers presented can be worked with the resonant PWM full-bridge inverter to compose a full-bridge DC/DC converter. Thus the energy can be transferred form the DC-link in the inverter stage to the output. As previous discussed, the voltage output of the converter is assumed to be constant, thus the left column voltage output is preferred for control [29]. The drawback of the voltage output converters can be eliminated by implying an output inductor in the filter to smooth the current.

Under the consideration of the complexity of transformer design , power components loss, that full bridge converter as shown in Fig 3.9 is the wise choice for the back-end converter with galvanic isolation. PWM modulations can be employed to achieve the soft switching to reduce the power loss during switch transitions. Thus the fullbridge PWM converter is a popular choice that for high-power applications as states in [25-26]. The full bridge PWM converter with phase-shifted control is called phase-shifted full bridge converter (PSFB) and a detailed description is presented in Chapter 5.

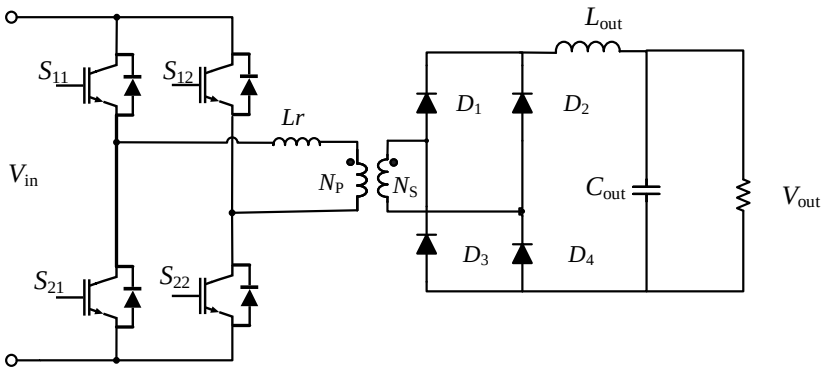


Figure 3.9: Full bridge PWM DC/DC converter

3.3 Summary

It can be concluded that the 3LT^{2}C is the proper choice for high-power applications with low voltage grids. The main advantages of the 3LT^{2}C are the high quality output waveform, more available power devices for system design, good compromise between conduction and switching losses over the comparison to the 2LC and 3LNPC^2. Thus it is applied as the front-to-end converter that allow bidirectional power follows between the AC gird-side and DC-link output. The PSFB converter serves as an back-end converter that provides galvanic isolation and high DC current output to the battery. The topology of the two-stage AC/DC converter system consists of the 3LT^{2}C converter and the PSFB converter is shown in Fig 3.10.

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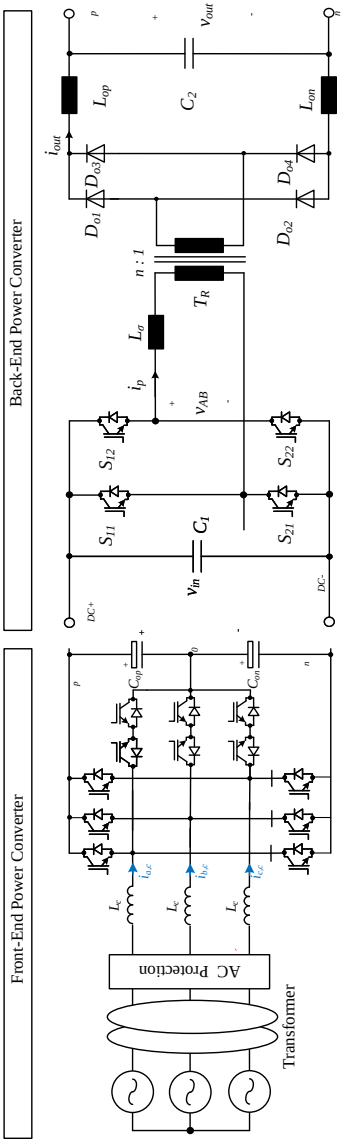


Figure 3.10: Topology of a two-stage AC/DC converter system: The 3LT^{2}C converter is selected as the front-end converter and the full-bridge DC/DC (PSFB) converter serves as the back-end converter.

Chapter 4

Three-Level T-type Converter

In this section, the switch commutation and the modulation methods of the 3LT^{2}C are discussed in detail. The analytical loss models for active power devices are determined and the control method to achieve high power factor operation is applied.

4.1 Switch Commutation

The switching states and commutations are studied in depth for the 3LT^{2}C. As explained in Chapter 3, the output of the three-level converters are three states namely the positive (P), neutral (O) and the negative (N). Due to the symmetry of the circuit topology, one phase bridge-leg is selected to investigate the switch states and the output of the DC-link voltage. The direction and path of the current output and switch transitions are shown in Fig 4.1. As it is shown, the positive output (P) can be obtained by simple turn on the switch T_1, and for the negative output (N) can be achieved by turning on T_4 while keeping T_2 and T_3on will give the neutral (O) state. This commutation strategy depends on the direction of the output current and it is relatively complex.

One simple strategy is to keep two switches conducting and the other two open in each switching state. There is one switch always kept on and another two switch commutating during the switching transition. Thus the current will switch to the other correct branch during the switch transitions [16]. A small turn on delay is required that guarantees the positive and negative branch will not conduct at same time which might result in the short circuit of the DC-link. The summary of the DC-link output voltage and switching states is given in Table 4.1. The positive output voltage (P) $+V_{dc}/2$ can be obtained by keeping the switch T_1 conducting and T_2,T_3, T_4 off. And the neutral (O) output can be achieved by turning on the switch T_2,T_3 and

Table 4.1: The DC-link voltage output and switching states

State	V_{out}	T_1	T_2	T_3	T_4
P	$+V_{dc}/2$	on	on	off	off
0	0	off	on	on	off
N	$-V_{dc}/2$	off	off	on	on

turning off T_1,T_4. In the same manner, closing the switch T_1,T_2 and keeping T_3,T_4 off will deliver the negative output (N) $-V_{dc/2}$.

For instance, the output voltage is $+V_{dc}/2$ and the negative output current flows into the the positive (upper) branch as shown in Fig 4.1(b). The switch T_1,T_2 are closed, that the current will naturally flow through the diode D_1 to the positive pole. The switch T_1 turns off and the current is not able to flow in the upper branch. The switchT_3 starts conducting after a simple turn-on delay. The negative current will commutate from the positive branch to the neutral branch through the IGBT/MOSFET in T_3 and the diode D_2 in T_2. Thus the switching state transits from positive to neutral P $\rightarrow$ 0.

If the transition states switch back from neutral to positive 0 $\rightarrow$ P for a negative output current, then the T_3 is turned off and the T_1 is closed after the turn-on delay. Thus the current will commutate from the mid branch to the positive branch. As shown in Fig 4.1(c,d), the positive phase current passes through the IGBT/MOSFET and the negative current flows into the diodes in the switch T_1 of the upper branch. The operation principles applies to all switching commutations.

4.2 Modulation

Three level T-type converter is a suitable choice for the high power-application voltage source inverter as described in Chapter 3. Compared with the three-level neutral point clamped converter and two level converter, the main advantages of the 3LT^{2}C include a high quality output waveform, low switching losses and lower value of total harmonics distortion, as well as the high power capacity [30]. Furthermore, the power switches have less voltage stress and there are more available semiconductors on the market for the high power application.

The applicable modulation for the three-level converter is shown in Fig 4.2, which are classified to fundamental switching frequency and high switching frequency PWM. The 3LT^{2}C is normally operated in high switch frequency (f_s > 10kHz) for high power application [31-33]. Thus, the space vector PWM and sinusoidal PWM are considered for the off board EV charging

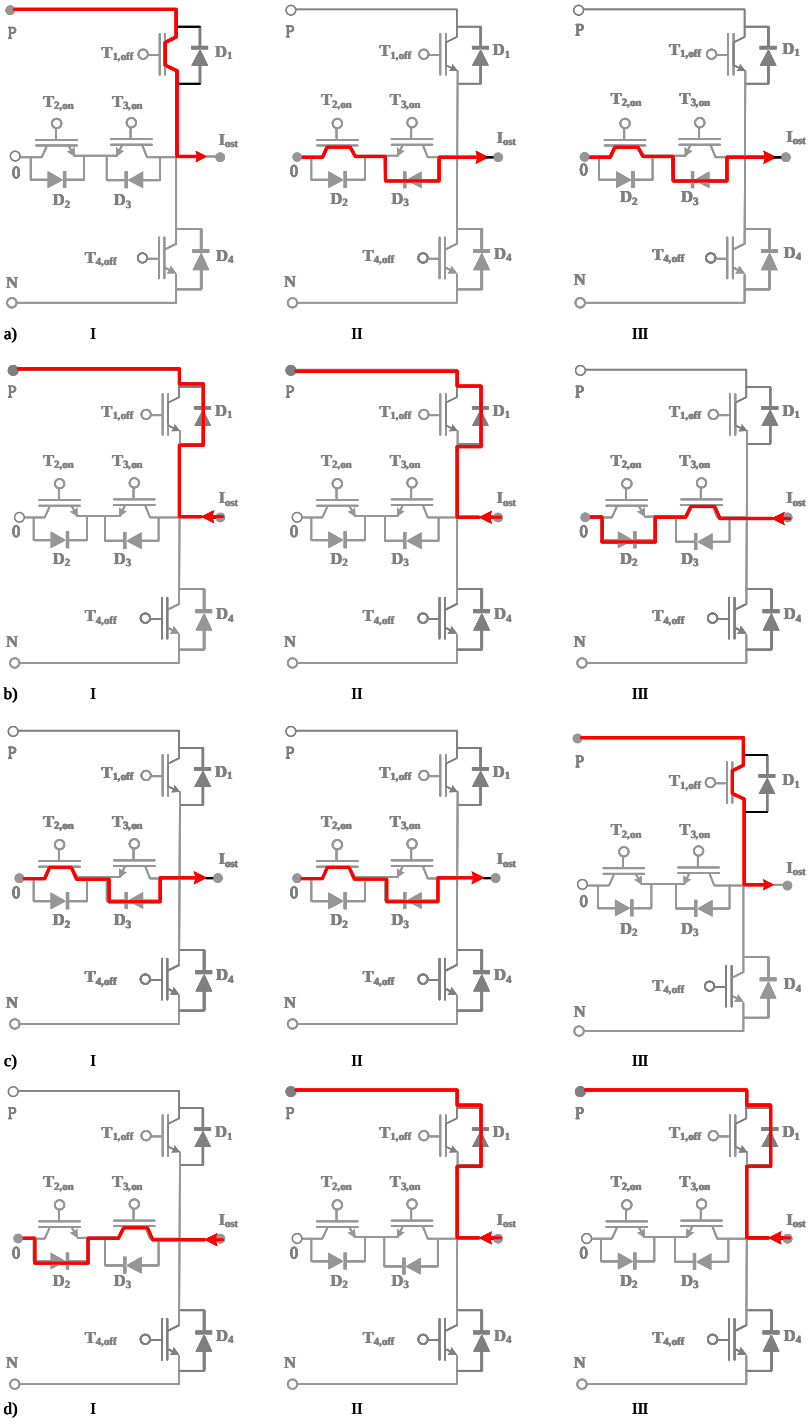


Figure 4.1: Switch commutation in the 3LT^{2}C: (a) the positive output current from ($P \rightarrow 0$) (b)the negative output current from ($P \rightarrow 0$) (c)the positive output current from ($0 \rightarrow$ P) (d)the negative output current from ($0 \rightarrow$ P).

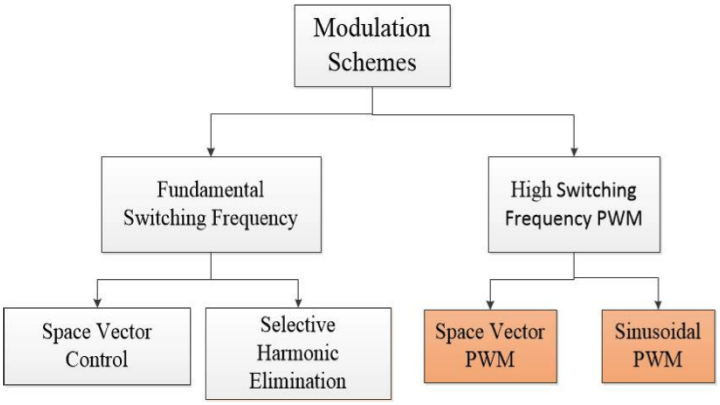


Figure 4.2: Classification of Modulation Schemes

design. In next section, the SPWM and SVPWM are researched in the following.

4.2.1 Sinusoidal Pules Width Modulation

SPWM is the most widely-used and simplest modulation scheme for inverters with high switching frequency operations [30]. The realization of SPWM for the 3LT^{2}C can be achieved by comparing three modulating signals with two carriers with different phases. For a single-phase converter, the gate signals or switch signals are produced by comparing a high frequency triangular signal to a sinusoidal modulating signal. When the carrier signal is higher than the modulating signal, the output is set to be high (1), and otherwise it is set zero. The Fig 4.3 shows the scheme of the SPWM and the output gate pulses. The frequency of the sinusoidal modulating signal is normally same as the grid frequency (50Hz or 60Hz), which is called fundamental frequency [30]. The modulation index m_a is defined as the ratio of the amplitude of the modulating signal V_m to the amplitude of the triangular carrier signal V_C.

$$m_a = \frac{V_m}{V_C} \tag{4.1}$$

Region $0 < m_a < 1$, where the line-to-line or phase voltage increases with the modulation index linearly is defined as the linear region. The region where $m_a > 1$ is defined as the over-modulation region, where the slope of output voltage decreases non-linearly as the modulation index increases [31].

For the three phase converter such as the 3LNPC^2, three sinusoidal modulating signal with 120° phase-shift between them are compared to the carrier signals. The fundamental frequency of the output voltage is the same as the

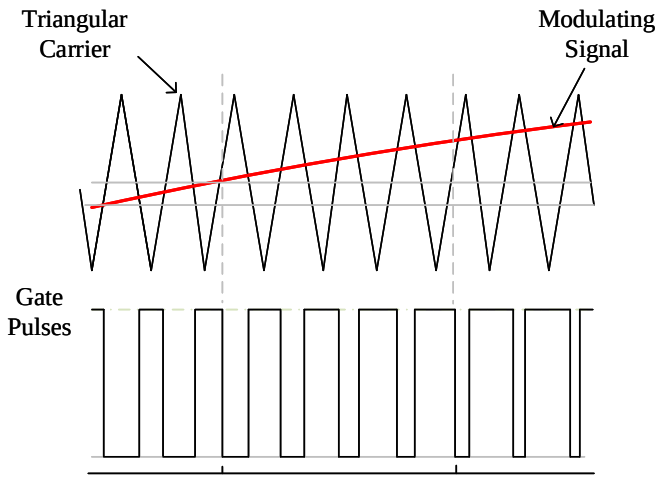


Figure 4.3: Sinusoidal Pulse Width Modulation

Figure 4.3: Sinusoidal Pulse Width Modulation

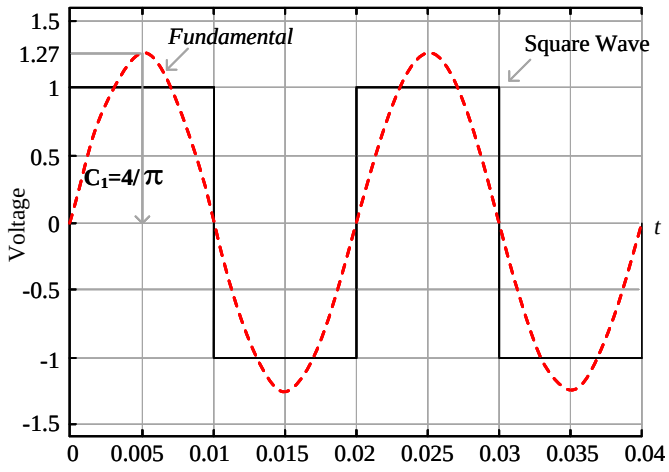


Figure 4.4: Unit square wave and its fundamental sinusoidal wave

fundamental frequency and the amplitude of the waveform is determined by the modulation index. Modulation index m_a can reach up to $4/\pi$ in the overmodualtion region derived from the fourier series expansion [31]. The Fig 4.5 shows the unit square wave and its fundamental sinusoidal wave and the modulation index. To analyze the output of the SPWM, the modulation

index is presented as

$$m_a = \frac{\hat{V}_{ph,1}}{0.5 * V_s} \quad \text{for } (0 < \mathrm{m_a} \leq 1) \tag{4.2}$$

where $\widehat{V}_{ph,1}$ is defined as the peak value of the output phase voltage, and $\mathrm{V_s}$ is the DC-link voltage of the converter. The amplitude of the carrier signal is $0.5{*}V_s$. Thus the maximum phase voltage will be 0.636 times of the DC link voltage.

$$\begin{aligned} \hat{V}_{ph,1} &= \frac{40.5 * V_s}{\pi} \\ \frac{\hat{V}_{ph,1}}{V_s} &= 0.636 \end{aligned} \tag{4.3}$$

The principle of SPWM for the three phase inverter works as the single phase converter as well. One phase of the three-level voltage waveform and its fundamental modulating sinusoidal signal is shown in Fig 4.5. Thus, the peak phase voltage of the fundamental wave signal is

$$\begin{aligned} \hat{V}_{ph,1} &= \frac{6 * \frac{0.5 * V_s}{3}}{\pi} = \frac{2V_s}{\pi} \\ \hat{V}_{ph,1} &= 0.318 V_s \end{aligned} \tag{4.4}$$

Therefore, the maximum of the phase output voltage in the linear modulation region ($0 < m_a < 1$)of SPWM scheme is derived as:

$$\begin{aligned} \hat{V}_{ph,1} &= \frac{0.318}{0.636} * m_a * V_s \\ \hat{V}_{ph,1} &= 0.5 * m_a * V_s \\ m_a &= \frac{\hat{V}_{ph,1}}{0.5 * V_s} \end{aligned} \tag{4.5}$$

Thus the amplitude of output phase voltage is half of the DC-link voltage.

$$\hat{V}_{ph,1}(\max) = 0.5 * V_s \tag{4.6}$$

4.2.2 Space Vector Pulse width Modulation

SVPWM is commonly used for the three-phase rectifiers because of the low switching losses and a lower THD compared to other modulation schemes. Another advantage of the SVPWM is that it is better for the utilization of the DC bus [32,33]. SVPWM is a three-phase simultaneous modulation that uses the reference vector formed by the different switching states of the inverter

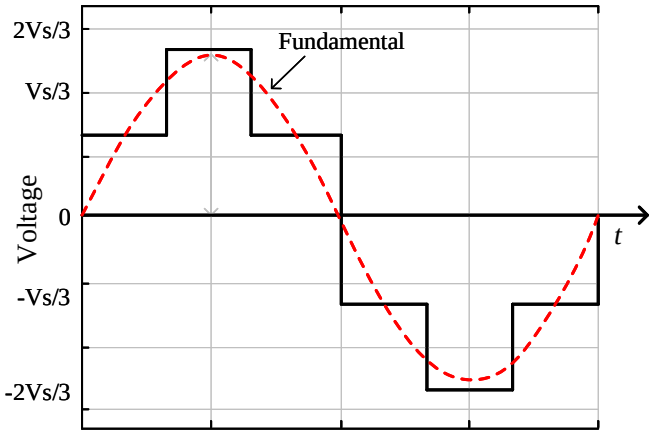


Figure 4.5: Three-level voltage waveform and its fundamental sinusoidal waveform

to approach the spatial vector formed by the grid phase voltage to determine the switching state of the switches and to generate the PWM waveform. The number of the switching states are 27 in the 3LT^{2}C including 24 active voltage vectors and 3 zero voltage vectors. The active vectors consist of small voltage vectors, medium voltage vectors and large voltage vectors.

Three-level Reference Vector For a three-phase balanced system, when a uniform three-phase sinusoidal voltage is applied to the stator of a motor, the composition of the three-phase voltage vectors produces a magnetic vector Ψ rotating at a synchronized speed ω with a standard circular path in the $\alpha \sim \beta$ coordinate system [32]. Thus it generates a circular rotating magnetic field and which results in a constant torque. The three-phase sinusoidal voltage applied to the stator terminal is

$$\begin{cases} u_{A(t)} = U_d \cos(\omega t) \\ u_{B(t)} = U_d \cos(\omega t - 2\pi/3) \\ u_{c(t)} = U_d \cos(\omega t + 2\pi/3) \end{cases} \tag{4.7}$$

The coordinated system is transferred from the three-dimensional ABC plane to the two-dimensional $\alpha\beta$ plane to represent the reference vector as shown in Fig 4.6, in which the phase A is aligned with the α-axis.

The reference vector $U_{ref}(t)$ is composed of three phase voltage vector $u_A(t), u_B(t), u_C(t)$ is

$$U_{ref}(t) = \frac{2}{3}\left[u_A(t) + \rho u_B(t) + \rho^2 u_c(t)\right] \tag{4.8}$$

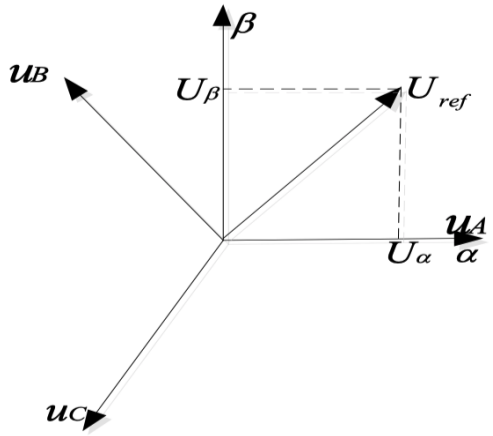


Figure 4.6: The reference vector in the $\alpha\beta$ two-dimensional plane.

where ρ is the complex number called rotation factor and it is given by $\rho = e^{j2\pi/3}$.

The outputs of one phase leg of the three-phase converter are $V_{dc}/2, 0, -V_{dc}/2$, and they are defined as positive(P) level, zero(0) level and negative level(N) respectively. If the switching state of each phase bridge arm is defined by S_a, S_b, S_c, then the phase voltage can be expressed by the following formula.

$$U_A = \frac{1}{2}V_{dc}S_a, U_B = \frac{1}{2}V_{dc}S_b, U_C = \frac{1}{2}V_{dc}S_c \tag{4.9}$$

where $S_x = \begin{cases} 1 & \text{the positive level output of the x phase} \\ 0 & \text{the zero level output of the x phase } (x \in a, \mathrm{b}, c) \\ -1 & \text{the negative level output of the x phase} \end{cases}$

Thus the reference space vector can be defined as:

$$\begin{aligned} u_\kappa &= \frac{1}{3}V_{dc}\left(S_a + \rho S_b + \rho^2 S_c\right) \\ &= \frac{1}{6}V_{dc}\left[(2S_a - S_b - S_c) + j\sqrt{3}\left(S_b - S_c\right)\right] \end{aligned} \tag{4.10}$$

The magnitude and the direction of each reference vector are determined by the equation(4.10), and the distribution of reference vectors for the three-level SVPWM is shown in Fig 4.7. The vectors are classified by the magnitude of the voltage vectors and defined as

- Zero Voltage Vectors $|u_K| = 0$
- Small Voltage Vectors $|u_K| = V_{dc}/3$
- Medium Voltage Vectors$|u_K| = \sqrt{3}V_{dc}/3$

- Large Voltage Vectors $|u_K| = 2V_{dc}/3$

There are 3 zero voltage vectors, 6 small voltage vectors, 12 medium voltage vectors and 6 large voltage vectors, are shown in Fig 4.7. Both zero vectors and small vectors are named redundant vectors, and the small vectors are always generated in pairs. For instance, OPO and NON are small vectors and they are redundant vectors to each other [33].

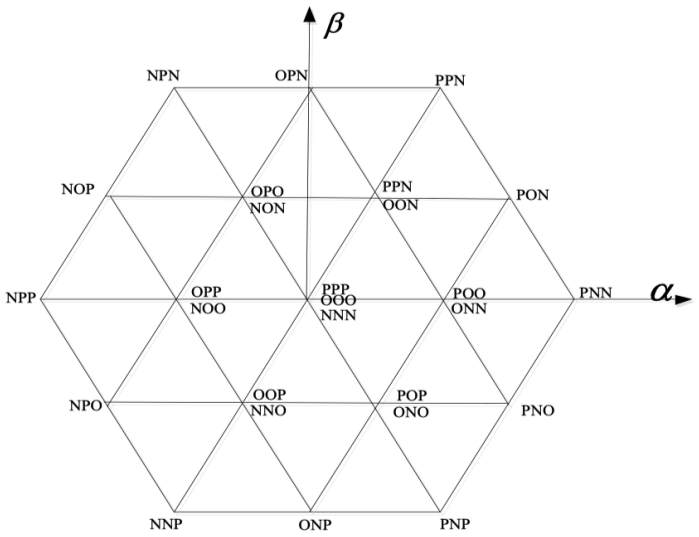


Figure 4.7: Three-level space vector diagrams.

The modulation index of the SVPWM is given by

$$m_a = \frac{V_{ref}}{\frac{2}{3} * V_s} \tag{4.11}$$

As presented in Fig 4.5, the longest length of the vector inside the hexagon is $\frac{2}{3}$. The length of the reference vector directly determines the magnitude of the phase output voltage. The largest circle inside the hexagon is the linear region for the SVPWM where the output increases linearly with the reference voltage.

$$\begin{cases} 0 < m_a < 0.866 & \text{linear modulation region} \\ m_a > 0.866 & \text{overmodulation region} \end{cases} \tag{4.12}$$

It is assumed that V_{a0}, V_{b0}, V_{c0} are the three phase voltage in a balanced system.

$$V_{a0} + V_{b0} + V_{c0} = 0 \tag{4.13}$$

The vectors converted through Clarke transformation are expressed as

$$\begin{array}{l} V_\alpha = \frac{2}{3}\left(V_{a0} + V_{c0} * \cos\frac{2\pi}{3} + V_{b0} * \cos\frac{4\pi}{3}\right) \\ V_\beta = \frac{2}{3}\left(0 + V_{c0} * \cos\frac{\pi}{6} + V_{b0} * \cos\frac{5\pi}{6}\right) \end{array} \tag{4.14}$$

The solution is given as (4.15) by solving the equations (4.13,4.14)

$$\begin{aligned} V_\alpha &= V_{a0} \\ V_\beta &= \frac{1}{\sqrt{3}} (V_{c0} - V_{b0}) \end{aligned} \tag{4.15}$$

The voltage vector V_α reaches to the maximum when $V_{a0} = 2/3V_s$ and thus $V_\beta = 0$, the phase voltage can be represented as

$$V_{a0} = \frac{2}{3} * m_a * V_s \tag{4.16}$$

The relation between the DC-link voltage and maximum phase voltage for SVPWM is derived as:

$$V_{a0}(\max) = 0.577 * V_s \tag{4.17}$$

Based on (4.6) and (4.17), the ratio of the output voltage of the three phase converter with SPWM and SVPWM is derived as:

$$\frac{V_{a0}(\max)}{\hat{V}_{ph,1}(\max)} = \frac{0.577 * V_s}{0.5 * V_s} \tag{4.18}$$

$$\frac{V_{a0}(\max)}{\hat{V}_{ph,1}(\max)} = 1.154 \tag{4.19}$$

It can be concluded from (4.19) that the output of the SVPWM is higher than the SPWM.

Time Duration As previously discussed, the SVPWM has a better output quality and is more suitable for the utilization of the DC bus in the three-level converter. The implementation of SVPWM is described in this section. In general, the distribution of three-level SVPWM voltage reference vectors are separated into six sectors by every 60 degrees based on the large voltage vectors [33]. Each contains 4 small regions as shown in Fig 4.8. The sectors are denoted by I, II, III, IV, V, VI, and the small regions by 1, 2, 3, 4. For instance, III1 presents the first small region of the third sector. Therefore, the position of the reference voltage vector can be determined by the angle θ between the reference voltage vector U_{ref} and the α-axis. It is assumed that [X] is the integer-valued function, $\theta \in [0^\circ, 360^\circ]$, then it is given that

$$\begin{aligned} [\theta/60] &= 0, \quad \mathrm{N} = 1 \\ [\theta/60] &= 1, \quad \mathrm{N} = 2 \\ [\theta/60] &= 2, \quad \mathrm{N} = 3 \\ [\theta/60] &= 3, \quad \mathrm{N} = 4 \\ [\theta/60] &= 4, \quad \mathrm{N} = 5 \\ [\theta/60] &= 5, \quad \mathrm{N} = 6 \end{aligned}$$

where N stands for the sector of the reference voltage vector. Unlike the two-level SVPWM, the number of vectors in the three-level SVPWM increases,

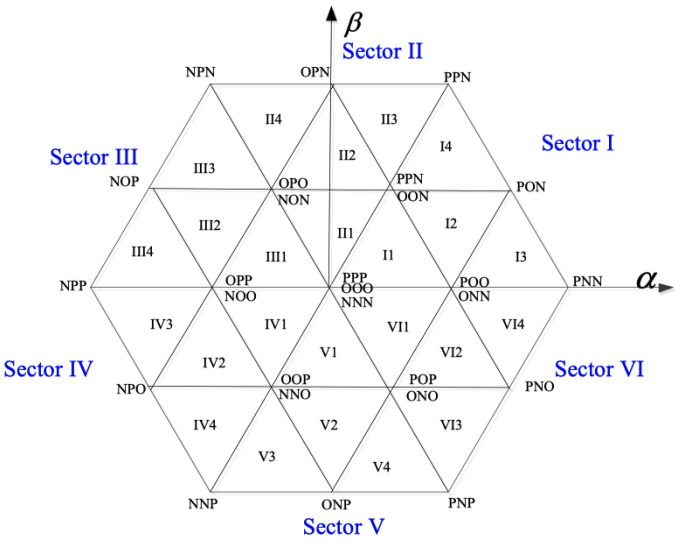


Figure 4.8: Sectors and regions distribution of the space vector diagrams.

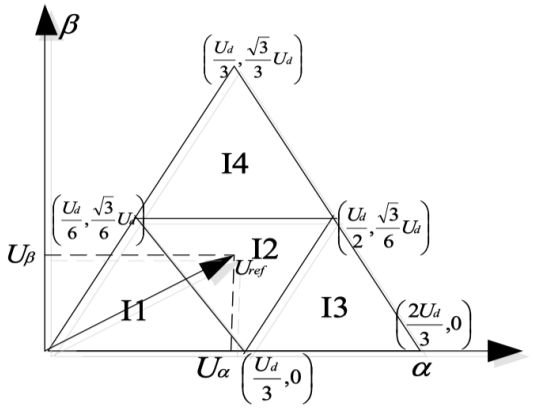


Figure 4.9: The small region judgment algorithm.

so that the basic vectors involved in the integration of the reference voltage vector cannot be completely determined by figuring out the large sector in which the reference vector is located [32,33]. In this matter, the small region where the reference vector U_{ref} located should also be determined. The sector I is selected as an example as displayed in Fig 4.9.

The coordinates of the vertices of each small triangle region are shown above. Based on the geometric relationship, a linear equation formed by the vertices determines which small triangle region the reference vector lies in-between. For example, a linear equation formed by $\left(\frac{U_d}{6},\frac{\sqrt{3}}{6}U_d\right)$, $\left(\frac{U_d}{3},0\right)$ the coordi-

Table 4.2: Criterion Table

Small region	Criteria I	Criteria II	Criteria III
1	✓	——	——
2	×	×	×
3	——	✓	——
4	——	——	✓

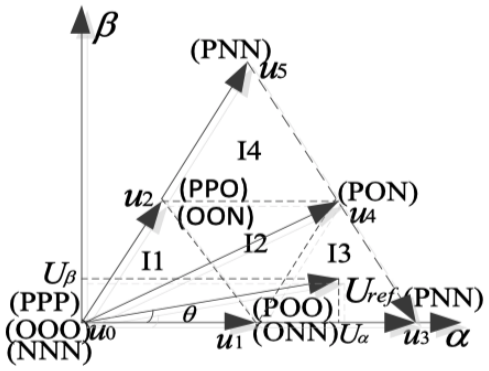


Figure 4.10: Time expressions of voltage vectors in sector I.

nates of the vertices would be $U_\alpha + \frac{\sqrt{3}}{3}U_\beta = \frac{U_d}{3}$. The criterion is generated by three similar line formulas for region selection as:

$$\begin{aligned} &U_\alpha + \tfrac{\sqrt{3}}{3}U_\beta - \tfrac{U_d}{3} < 0 \quad \text{Criteria I} \\ &U_\alpha - \tfrac{\sqrt{3}}{3}U_\beta - \tfrac{U_d}{3} > 0 \quad \text{Criteria II} \\ &U_\alpha - \tfrac{\sqrt{3}}{6}U_d < 0. \quad \text{Criteria III} \end{aligned}$$

The listed criterion for small regions is shown as Table 4.2.

The three nearby basic vectors u_1, u_2, u_3 involved in the composition of the reference vector U_{ref} can be known when its position is determined. According to the volt-second equilibrium principle based on spatial voltage vector synthesis, the following equation are derived.

$$u_1 t_1 + u_2 t_2 + u_3 t_3 = U_{ref} T_s \tag{4.20}$$

$$t_1 + t_2 + t_3 = T_s \tag{4.21}$$

where t_1, t_2, t_3 indicate the action duration of u_1, u_2, u_3, and T_s represents a modulation period. As shown in Fig 4.10, the reference voltage vector located in the small region I3 and the basic vectors nearby are u_1, u_3, u_4.

From the equation (4.10), the vectors are given as

$$\begin{aligned} u_1 &= \frac{1}{6}U_d\left[(2S_a - S_b - S_c) + j\sqrt{3}\,(S_b - S_c)\right] \\ &= \frac{1}{6}U_d[(2-0-0) + j\sqrt{3}(0-0)] \\ &= \frac{1}{3}U_d \end{aligned} \tag{4.22}$$

$$\begin{aligned} u_3 &= \frac{1}{6}U_d\left[(2S_a - S_b - S_c) + j\sqrt{3}\,(S_b - S_c)\right] \\ &= \frac{1}{6}U_d[(2-(-1)-(-1)) + j\sqrt{3}((-1)-(-1))] \\ &= \frac{2}{3}U_d \end{aligned} \tag{4.23}$$

$$\begin{aligned} u_4 &= \frac{1}{6}U_d\left[(2S_a - S_b - S_c) + j\sqrt{3}\,(S_b - S_c)\right] \\ &= \frac{1}{6}U_d[(2-0-(-1)) + j\sqrt{3}(0-(-1))] \\ &= \frac{1}{2}U_{d+j}\frac{\sqrt{3}}{6}U_d \end{aligned} \tag{4.24}$$

Substituting the equations (4.22-23,2.24) to the equation (4.20-21) gives

$$\frac{1}{3}U_{dt1} + \frac{2}{3}U_{dt2} + \left(\frac{U_d}{2} + j\frac{\sqrt{3}}{6}U_d\right)t_3 = \left(U_\alpha + jU_\beta\right)T_s \tag{4.25}$$

The solution of (4.25) is given as

$$\begin{cases} t_1 = 2T_s - \frac{3T_s\left(U_\alpha + U_\beta/\sqrt{3}\right)}{U_d} \\ t_2 = \frac{3\left(U_\alpha - U_\beta/\sqrt{3}\right)T_s}{U_d} \\ t_3 = \frac{2\sqrt{3}U_\beta T_s}{U_d} \end{cases} \tag{4.26}$$

by expanding the equations in real and imaginary parts. When the reference vectors are located in the other small regions of sector I, the time duration can be derived in the same way. Table 4.3 shows the action duration of each fundamental voltage vector of sector I.

Sequences of switching states For a three-level converter circuit, each phase bridge arm has three output states: P, O, and N. When the P state transits directly to the N state, two power switches have to operate simultaneously, which not only increases the operating frequency of the switch device, but also has a high probability of turning on both upper and lower switches of this phase bridge arm simultaneously, which results in the damage to the power semiconductors. Therefore, the principle that only one switch of one

Table 4.3: Time duration of voltage vectors in sector I

Small region	t_1	t_2	t_3
1	$\frac{3T_s\left(U_\alpha - U_\beta/\sqrt{3}\right)}{U_d}$	$\frac{2\sqrt{3}T_sU_\beta}{U_d}$	$T_s - \frac{3T_s\left(U_\alpha + U_\beta/\sqrt{3}\right)}{U_d}$
2	$T_s - \frac{2\sqrt{3}T_sU_\beta}{U_d}$	$T_s - \frac{3T_s\left(U_\alpha - U_\beta/\sqrt{3}\right)}{U_d}$	$-T_s + \frac{3T_s\left(U_\alpha + U_\beta/\sqrt{3}\right)}{U_d}$
3	$2T_s - \frac{3T_s\left(U_\alpha + U_\beta/\sqrt{3}\right)}{U_d}$	$\frac{3\left(U_\alpha - U_\beta/\sqrt{3}\right)T_s}{U_d}$	$\frac{2\sqrt{3}U_\beta T_s}{U_d}$
4	$2T_s - \frac{3T_s\left(U_\alpha + U_\beta/\sqrt{3}\right)}{U_d}$	$\frac{3T_s\left(U_\alpha - U_\beta/\sqrt{3}\right)}{U_d}$	$\frac{2\sqrt{3}T_sU_\beta}{U_d} - T_s$

bridge arm is active at the same time must be observed. As seen in the previous analysis, there are redundant states for the small and zero vectors, which means that each small and zero vector has two or three switch combinations correspondingly. This enables to optimize the sequences of switching states, which means the switching frequencies and switching losses are reduced [31,33].

In order to facilitate the control method and reduce the harmonic content of the output voltage, the fundamental vector is usually kept symmetrical during each control cycle [32]. The reference voltage vector in section I as shown in Fig 4.10 is analyzed for instances. According to the vector transition principle as previously mentioned, the positive small vectors are used as the initial vectors, the O state is applied as the transition state, the next basic vector is selected according to the principle that only one switch can be operated in each phase arm. Then it returns to its original path according to the symmetry principle, and finally reach to the initial vector. In Fig 4.10, the vector sequences act in the following order: POO $\rightarrow$ PON $\rightarrow$ PNN $\rightarrow$ ONN $\rightarrow$ PNN $\rightarrow$ PON $\rightarrow$ POO. Thus it is called center symmetrical seven-segment waveform, and duration time of the basic vector corresponds to the switch state for U_{ref} in the region 3 of sector I is displayed as Fig 4.11.

4.3 Analytical Model

The conduction losses and switching losses are the major concern for the three-level T-type converter. Due to the application of the SVPWM scheme, the switching states and transitions in each modulation period should be determined for each bridge leg devices based on the current commutation as displayed in Fig4.1. In this section, the general analytical losses model for converters with SVPWM technology is illustrated based on [16,34].

As shown in the previous section, the output phase are determined by each fundamental space vectors which consist the reference vectors $\overrightarrow{V_{ref}}$. Thus the

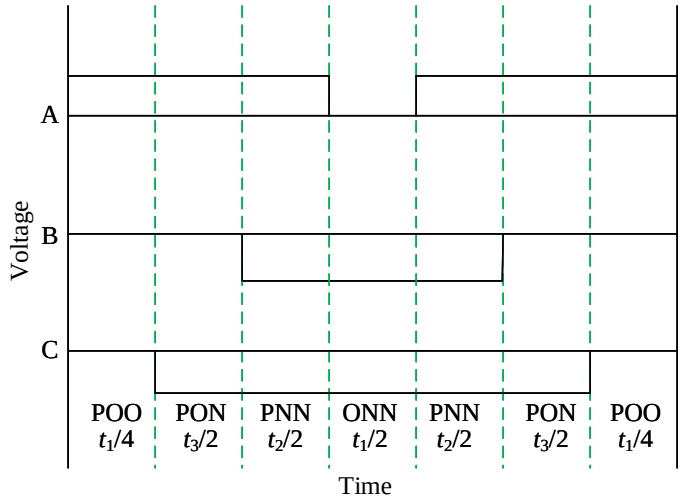


Figure 4.11: Waveform showing sequence of switching states for region 3 in sector 1.

voltage space vectors are defined and can be expressed by the 27 switching states, the direction of current following in the bridge legs are determined at the same time .

Thus the conduction loss of the power switch is determined by its switching state and the commutation current. A summary of the conduction losses of the devices according to the current direction and its path is presented in Table 4.4. For instance, as for the switch T_1 in phase A, the conduction loss only occurs when the phase current is positive and the switching state is positive (P) as

$$P_{\mathrm{c,T1a}} = \begin{cases} P_{\mathrm{cond,T1}}\ (i_{\mathrm{a}}) & i_{\mathrm{a}} \geq 0 \& S_{\mathrm{a}} = \mathrm{P} \\ 0 & \text{otherwise} \end{cases} \tag{4.27}$$

Here the switch states is given by the switching state vector $\overrightarrow{SV} =$

$$\overrightarrow{SV} = [S_{\mathrm{a}} \quad S_{\mathrm{b}} \quad S_{\mathrm{c}}] \tag{4.28}$$

Where $S_{\mathrm{a}}S_{\mathrm{b}}S_{\mathrm{c}}$ are the switching states of the a, b, c phase. When $S_{\mathrm{a}}S_{\mathrm{b}}S_{\mathrm{c}}$ are all positive, the switching state is (PPP).

Moreover, the current space vector $\vec{I}$ can be described in terms of the each phase current as

$$\vec{I} = \begin{bmatrix} i_{\mathrm{a}} & i_{\mathrm{b}} & i_{\mathrm{c}} \end{bmatrix} \tag{4.29}$$

Then the conduction loss of each power device depends on the current space vector $\vec{I}$ and the switching state vectors $\overrightarrow{SV}$ and expressed as

$$P_{\text{cond}}\left(\overrightarrow{SV},\vec{I}\right)=\begin{pmatrix} P_{\text{c,T1a}} & P_{\text{c,D1a}} & \cdots & P_{\text{c,xa}} \\ P_{\text{c,T1b}} & P_{\text{c,D1b}} & \cdots & P_{\text{c,xb}} \\ P_{\text{c,T1c}} & P_{\text{c,D1c}} & \cdots & P_{\text{c,xc}} \end{pmatrix} \tag{4.30}$$

The conduction loss matrix contains all the loss of power device in the topology. The conduction loss of the IGBT T_1 can be expressed as the function of the forward drop v_{CE} voltage and the equivalent output resistance r_o and the current i as

$$P_{\text{cond, T1}}(i)=v_{\text{CE,T}_1}\cdot i+r_{\text{o,T1}}\cdot i^2 \tag{4.31}$$

Here, the forward drop voltage is assumed to be linearly increased with the commutation current [16,33,35].

The switching state vectors and the switching sequences of these vectors can be found when the position and magnitude of the reference voltage space vector $\overrightarrow{V_{ref}}$ is given. Thus the time of on-state actions for switching states vectors in one switching cycle and the averaged conduction loss can be determined.

As shown in Fig 4.10, the reference space voltage vector is located in the region3 of the sector I. The three space vectors nearby is (PNN), (POO) and (PON). Moreover the time duration of the space voltage vectors are given in Table 4.3. The full expression of the sector I contains 4 small regions and it is not necessary to calculate by hand, which could be solved by MATLAB. This method can be used for the 2LC with SVPWM and select the sector II as an example, that the vector (PPN), (NPN) and (PPP) are numbered as $\overrightarrow{SV_2}$, $\overrightarrow{SV_3}$ and $\overrightarrow{SV_7}$

$$\begin{aligned} P_{\text{cond, avg}}\left(\vec{V},\vec{I}\right)=&t_3\cdot P_{\text{cond}}\left(\overrightarrow{SV_3},\vec{I}\right)+t_2\cdot P_{\text{cond}}\left(\overrightarrow{SV_2},\vec{I}\right) \\ &+t_7\cdot P_{\text{cond}}\left(\overrightarrow{SV_7},\vec{I}\right) \end{aligned} \tag{4.32}$$

The switching loss of the power device consists of the energy loss during the turn-on and turn-off period. Thus one more factor is required to determine the switching loss of the components. The phase current and voltage during the transitions determine the switch loss of the semiconductors. Two switching state vectors are introduced to determine the energy loss during switch transition. The switching state vector $\overrightarrow{SV_o}$ is the previous state before the switch commutation and $\overrightarrow{SV_n}$ presents the new state after the commutation [16,35]. Thus the matrix representation for switching loss of all power switch in a certain topology is

$$E_{\mathrm{sw}}\left(\overrightarrow{SV}_{\mathrm{o}}, \overrightarrow{SV_{\mathrm{n}}}, \vec{I}\right) = \begin{pmatrix} E_{\mathrm{s,T1a}} & E_{\mathrm{s,D_1a}} & \cdots & E_{\mathrm{s,xa}} \\ E_{\mathrm{s}}, \mathrm{T_{1b}} & E_{\mathrm{s,D1b}} & \cdots & E_{\mathrm{s,xb}} \\ E_{\mathrm{s}}, \mathrm{T_1c} & E_{\mathrm{s,D_1c}} & \cdots & E_{\mathrm{s,xc}} \end{pmatrix} \tag{4.33}$$

In the 3LT^{2}C, the IGBT T_1 will be turned on when the switching state changes from neutral (0) to positive while the phase current is positive. For the turn-off loss of T_1, it will occur when the state changes from positive(P)to neutral while the phase current is positive as well. Thus the switching loss of the T_1 is given as

$$E_{\mathrm{s,T1a}} = \begin{cases} E_{\mathrm{T1,off}}\left(i_{\mathrm{a}}\right) & S_{\mathrm{a,o}} = \mathrm{P} \& S_{\mathrm{a,n}} = 0 \& i_{\mathrm{a}} \geq 0 \\ E_{\mathrm{T1,on}}\left(i_{\mathrm{a}}\right) & S_{\mathrm{a,o}} = 0 \& S_{\mathrm{a,n}} = \mathrm{P} \& i_{\mathrm{a}} \geq 0 \\ 0 & \text{otherwise} \end{cases} \tag{4.34}$$

The switching state transitions and the energy losses of the power switches in the 3LT^{2}C are displayed in Table 4.5. The energy loss during switch commutations of the power switch can be derived from the datasheet and it is assumed to be approximately linear with the commutation voltage V_{CE}. The turn-on energy loss of the IGBT T_1 is

$$E_{\mathrm{T1,on}(i)} = \frac{E_{\mathrm{T1,on,}}}{V_{\mathrm{CE0}} I_{\mathrm{CE0}}} \cdot V_{\mathrm{c}} \cdot i \tag{4.35}$$

where V_{CE0} and I_{CE0} are the initial voltage and current shown on the datasheet.

Thus, the averaged switching loss of a symmetric 7-segment sequence ($\overrightarrow{SV_A} - \overrightarrow{SV_B} - \overrightarrow{SV_C} - \overrightarrow{SV_D} - \overrightarrow{SV_C} - \overrightarrow{SV_B} - \overrightarrow{SV_A}$) from SVPWM can be expressed as

$$\begin{aligned} P_{\mathrm{sw,avg}}(\vec{V}, \vec{I}) = & \frac{1}{T_{\mathrm{sw}}} \cdot \left(E_{\mathrm{sw}}\left(\overrightarrow{SV_A}, \overrightarrow{SV_B}, \vec{I}\right) + E_{\mathrm{sw}}\left(\overrightarrow{SV_B}, \overrightarrow{SV_C}, \vec{I}\right) \right. \\ & + E_{\mathrm{sw}}\left(\overrightarrow{SV_C}, \overrightarrow{SV_D}, \vec{I}\right) + E_{\mathrm{sw}}\left(\overrightarrow{SV_D}, \overrightarrow{SV_C}, \vec{I}\right) \Big) \\ & \left. + E_{\mathrm{sw}}\left(\overrightarrow{SV_C}, \overrightarrow{SV_B}, \vec{I}\right) + E_{\mathrm{sw}}\left(\overrightarrow{SV_B}, \overrightarrow{SV_A}, \vec{I}\right) \right) \end{aligned} \tag{4.36}$$

The *ABCD* here just describes the switch state vectors in a switching sequence for an undetermined space voltage reference vector.

Finally, the conduction loss and switching loss of the power components over a fundamental frequency can be expressed by integrating the power loss with electric angle α as

$$\overline{P_{\mathrm{cond}}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} P_{\mathrm{cond,avg}} \cdot d\alpha \tag{4.37}$$

$$\overline{P_{\mathrm{sw}}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} P_{\mathrm{sw,avg}} \cdot d\alpha \tag{4.38}$$

Table 4.4: Conduction losses of devices and switching in the 3LT^{2}C

Switching States	Conduction Losses
$I_{out} \geq 0$	
P	$P_{cond,T1}$
0	$P_{cond,T2}$, $P_{cond,D3}$
N	$P_{cond,D4}$
$I_{out} < 0$	
P	$P_{cond,\ D1}$
0	$P_{cond,\ D2}$, $P_{cond\ ,T3}$
N	$P_{cond,\ T4}$

Table 4.5: Energy losses and switching transitions in the 3LT^{2}C

Switching Transition	Loss Energies
$I_{out} \geq 0$	
$P \rightarrow 0$	$E_{T1,off}$, $E_{D3,on}$
$0 \rightarrow P$	$E_{T1,on}$, $E_{D3,off}$
$N \rightarrow 0$	$E_{T2,on}$, $E_{D4,off}$
$0 \rightarrow N$	$E_{T2,off}$, $E_{D4,on}$
$I_{out} < 0$	
$P \rightarrow 0$	$E_{T3,on}$, $E_{D1,off}$
$0 \rightarrow P$	$E_{T3,off}$, $E_{D1,on}$
$N \rightarrow 0$	$E_{T4,off}$, $E_{D2,on}$
$0 \rightarrow N$	$E_{T4,on}$, $E_{D2,off}$

4.4 Control Scheme

The diagram of control blocks for the three-phase converter with space vector pulse width modulation is shown as Fig4.12. The 3LT^{2}C operates as a rectifier to provide a constant DC output to the back-end converter. Thus a simple voltage source converter (VSC) controller consisting of the current control as well as the voltage control is illustrated in this part.

In the control design, the voltage drops across the line resistance and active power components are neglected, and the three phase voltage at the terminal of the 3LT^{2}C is

$$v_{x,1} = v_x - L\frac{di_x}{dt} \tag{4.39}$$

where x represents the phase A,B,C. Clark transformation is applied to trans-

fer three phase current i_{abc} into the dq domain as i_d, i_q. Subtitling the equation to the dq-system yields :

$$v_{d1} = v_d - L\frac{di_d}{dt} + \omega L i_q \tag{4.40}$$

$$v_{q1} = v_q - L\frac{di_q}{dt} - \omega L i_d \tag{4.41}$$

where $\omega L i_{d,q}$ are the coupling terms generated in the dq frame. Moreover, the reference voltages of the AC grid terminal expressed in dq system are :

$$v^*_{d1} = v_d + \omega L i_q - v_{Ld} \tag{4.42}$$

$$v^*_{q1} = v_q - \omega L i_d - v_{Lq} \tag{4.43}$$

where $v_{Ld,q}$ are derived form the PI compensator in the current control loop.

Current Control The proportional-integral (PI) controller is adopted in the current control loop to compensate the grid-side current. The output voltage of the current control loop is the reference of the terminal voltage of the $3LT^2C$.

Voltage control The PI controller is used in VSC converter to control the DC-link voltage. The output of the outer loop is the reference input of the inner current controller.

The real and reactive power can be expressed with dq terms directly shown as

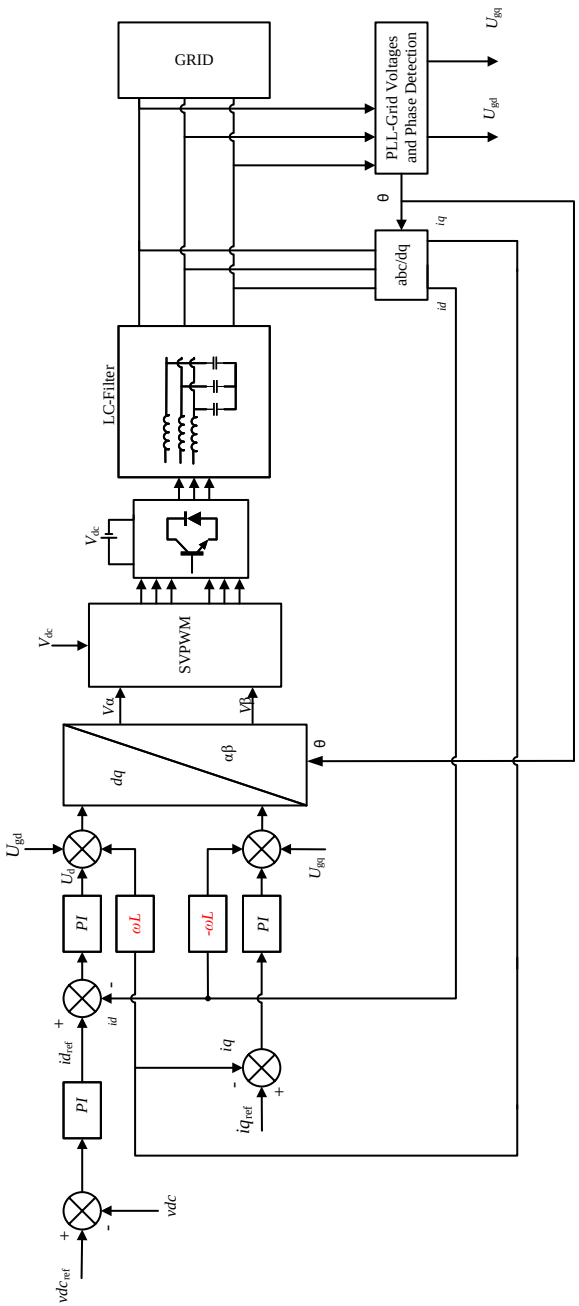
$$P = v_d i_d + v_q i_q \tag{4.44}$$

$$Q = v_d i_q + v_q i_d \tag{4.45}$$

because d-axis is aligned with the grid voltage so v_d is constant and v_q equals to zero. Thus, the active power can be controlled by adjusting the current i_d, i_q

Furthermore, the reactive power Q can be controlled by the current i_q, and for power factor control, the reference current i^*_q is set to be zero, thus there will be no reactive power and deliver a rectifier with the power factor PF $=$ 1.

Figure 4.12: Control diagram



Chapter 5

Phase-shifted Full Bridge Isolated Converter

The operation modes of the PSFB converter are introduced in this section. The analytical loss models of power devices and the magnetic components are determined. The optimization procedure to achieve a high efficiency galvanically-isolated DC-DC converter is presented.

5.1 Phase shifted control

The four power switches are driven by the gate signals with 50% duty cycle, and the upper switch $S_{11,12}$ and lower switch $S_{21,22}$ in each bridge cannot conduct simultaneously, and the difference of the gate signals in each leg is 180° phase shift [36,37]. The switching signals for the right leg switches $S_{12,22}$ are shifted with a controllable phase in respect of the signals for the left switches $S_{11,21}$. The phase angle decides the the overlap of the input voltage V_{in} and the secondary side output voltage vs, and thus it determines the energy transferred to the output.

The phase shift control method enables ZVS soft switching of the power device, which is utilized by the resonance of the capacitance in the primary side circuit during the dead time of the gate signal in one bridge leg [36,37]. When one of the power switch is turned off, the current in the primary side is resonant charging its parallel (parasitic) capacitance and resonant discharging the output capacitance of the other switch in the same bridge leg. When the capacitance discharged to zero, the other switch turns on with zero-voltage switching [39]. The power switches paralleled with the capacitors to achieve soft switching in the isolated PSFB converter is shown in Fig 5.1.

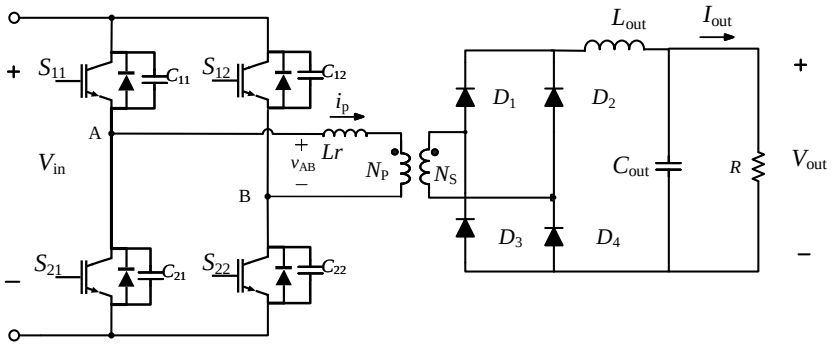


Figure 5.1: Topology of the PSFB converter with ZVS conditions

5.2 Operation modes

There are four operating modes as shown in Fig 5.2, the powering state and the free-wheeling state cycle sequentially in one switch cycle. The characteristic waveforms including gate signals to drive the switches and the voltage applied on the primary side of the transformer, the output inductor current and the voltage of secondary-side transformer are presented as well.

Duty Cycle loss $t_0 \leq t \leq t_2$

The converter operates in the powering states from t_0. As presented in the previous section, the switch S_{11} is turned on under the ZVS condition. The parallel or parasitic capacitors is completely discharged during the dead time t_d and the energy is stored in the leakage inductor L_r. The voltage across the transformer v_{AB} is clammped to the input voltage V_{in} and applied on the leakage inductor L_r in the primary transformer. The current in the the primary side i_p increases linearly from the negative value $-I_{p3}$ to the positive value I_{p1} and its slope is determined by the primary inductance. The primary current transits from the negative value to the positive one at t_1. It is shown that there is no overlap between the primary voltage v_{AB} and secondary voltage v_s, and thus there is no energy delivered to the secondary side during this period, which means that no power is transferred form the input to the output.

The current in the output inductor i_{out} still decreases form during $t_0 \leq t \leq t_2$ that the it will turn to increase from $t = t_2$. As the output current is kept positive and the secondary voltage is clammped to zero, thus the four diodes in the rectifier stage are conducting and the diodes D_2, D_3 are forced to turn off under the hard switching condition at $t = t_2$.

Power delivery $t_2 \leq t \leq t_3$

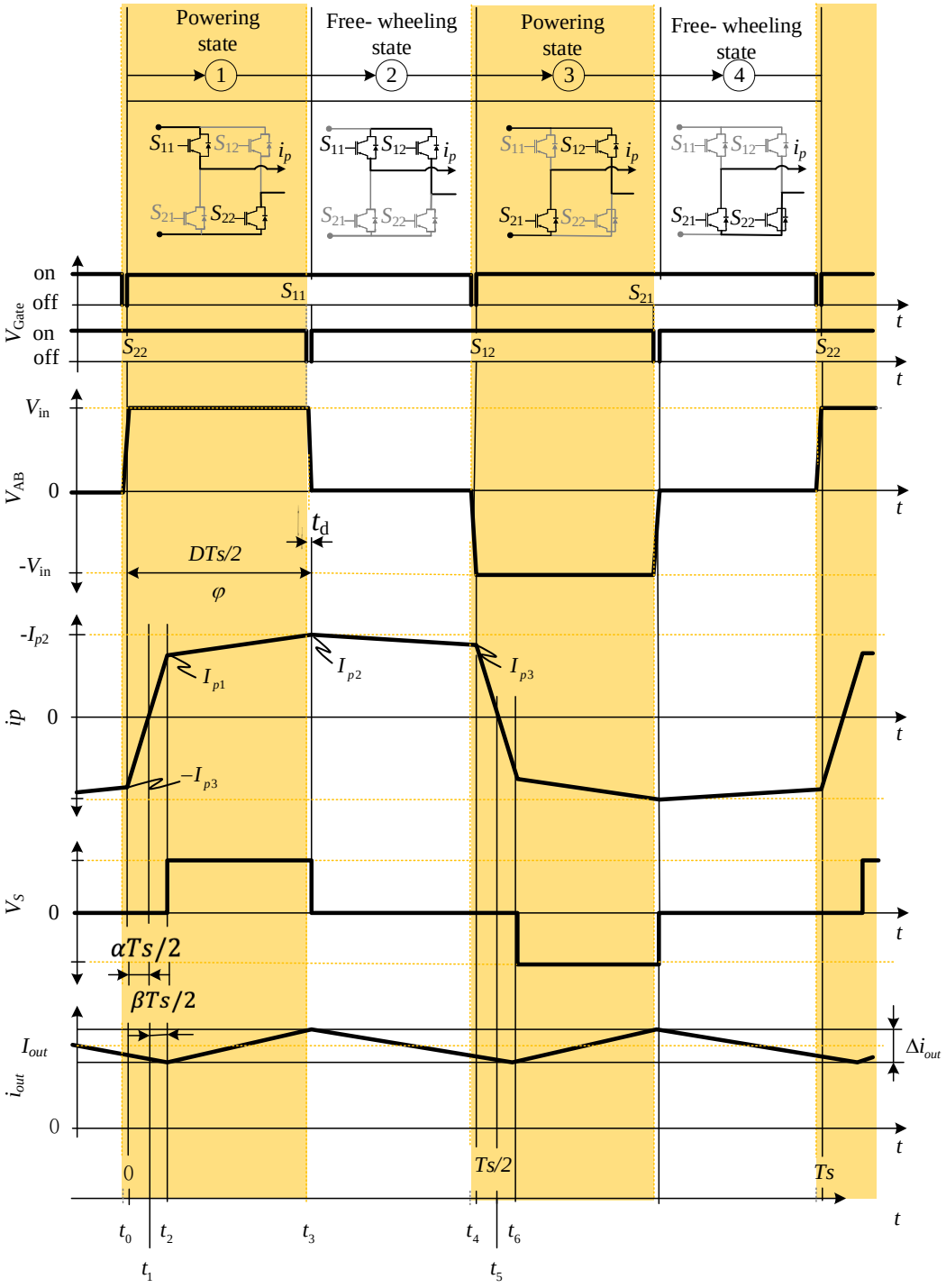


Figure 5.2: The steady-state waveform of characteristic currents and voltages in the PSFB DC/DC converter.

The converter operates the powering states as well and the voltage of the secondary transformer v_s is clammped to a constant voltage as $V_{\text{in}}\, N_{\text{s}}/N_{\text{p}}$ instantaneously. The diodes D_1, D_4 are forward biased to conduct and the secondary current raise from I_{p1} to I_{p2} and the slope of the output current is V_{out}/L_{out}. This period $t_2 - t_3$ is called effective phase duty cycle where the converter transfer energy from the input to the output.

During the dead time t_d before t_3, the IGBT S_{22} is turned off and the primary current charges the parallel capacitance C_{22} of switch S_{22} while discharging the capacitance C_{12} of switch S_{12}. The capacitance C_{12} is fully discharged during t_d and voltage drops from $+V_{in}$ to zero. The anti-paralleled diode in switch S_{12} will conduct, thus S_{12} will be turned on with ZVS conditions at $t = t_3$.

Freewheeling mode $t_3 \leq t \leq t_4$

The converter operates in the freewheeling states from t_3 to t_4. The switch S_{12} is turned on under the ZVS condition and the primary current i_p is freewheeling in upper switches S_{11} and S_{12}. Additionally, the voltage of the primary transformer v_{AB} and secondary voltage v_s are both clammped to zero. The primary current decreases linearly from I_{p2} to the positive value I_{p3}, and the diodes D_2, D_3 starts to conduct as well because there are no voltage applied on the secondary transformer, thus four diodes in the rectifier stage are all in on states.

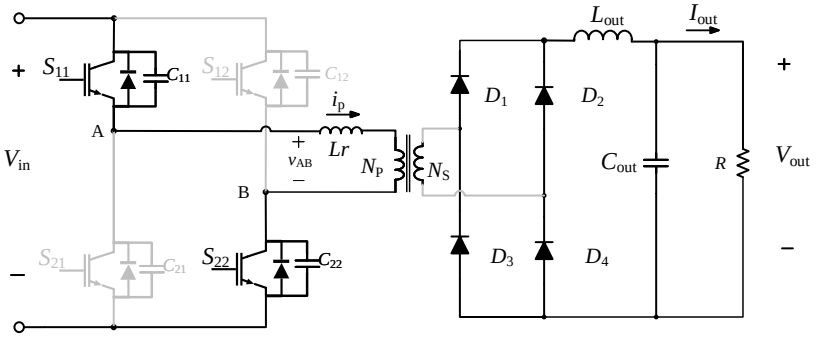
In the period of the dead time t_d before t_4, the IGBT S_{11} is turned off and the primary current charges the parallel capacitance C_{11} of switch S_{11}, and discharges the capacitance C_{21} of switch S_{21}. The capacitance C_{11} is fully discharged during t_d and the voltage drops from zero to the negative value $-V_{in}$. The anti-paralleled diode in switch S_{21} will conduct, thus S_{21} will be turned on with ZVS conditions at $t = t_4$.

The above switching modes during the first half cycle are described as above. The analysis of the second half cycle similar to that of the first half cycle and this is not presented in this section.

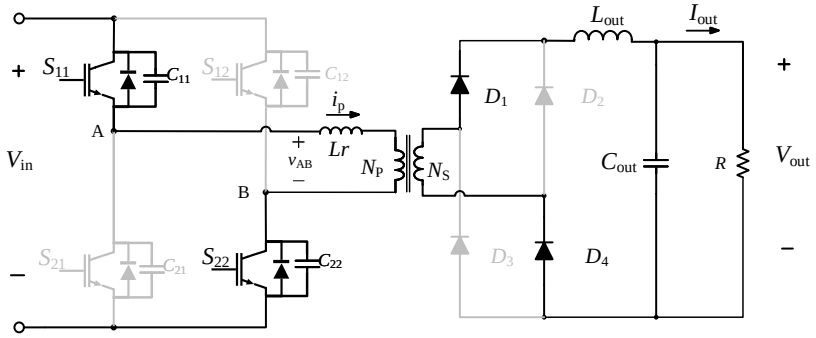
5.3 Optimization Procedure

The flow chart of the design procedure and the optimization algorithm to realize a high-efficiency and high-power density phase-shifted full bridge DC/DC converter with galvanic isolation is shown in Fig 5.4. The design sequences and assumptions are clearly illustrated in the following.

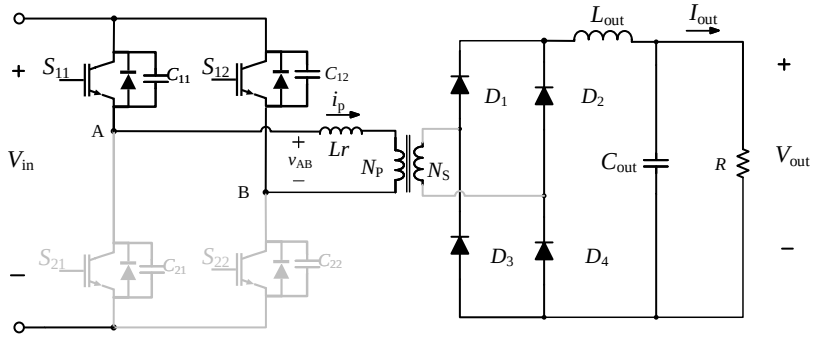
Step 1 The parameters and specifications are fixed based on the consideration of industry standards and applications []. The electrical parameters and limitations are elaborated in Chapter 2 including the input and output voltage. The selected magnetic materials and power devices are based on



(a) $t_0 \leq t \leq t_2$



(b) $t_2 \leq t \leq t_3$



(c) $t_3 \leq t \leq t_4$

Figure 5.3: Switching states of the PSFB converter and current path in a half-cycle: (a) duty cycle loss mode (b) power delivery mode (c) freewheeling mode.

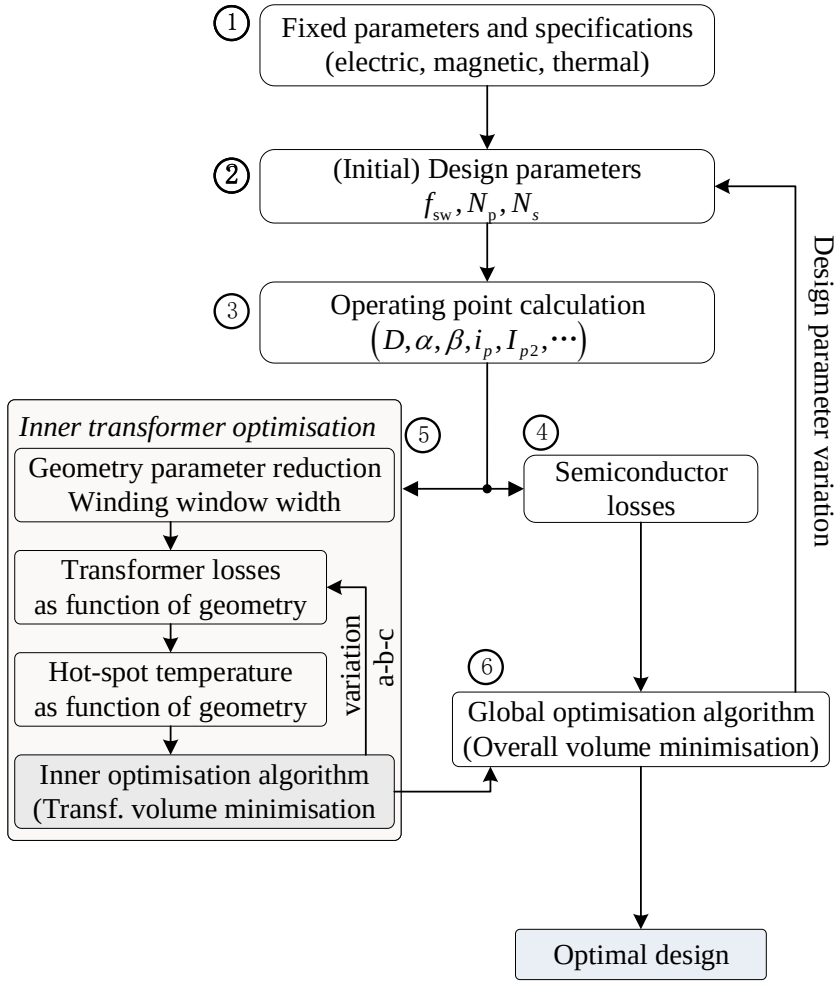


Figure 5.4: Automatic design procedure with an optimization algorithms for high efficiency system design.

the products available on the market. Thermal aspects such as the temperature of the surrounding environments and ambient junction temperatures as well as the requirements of the cooling system or heat-sink are not taken into consideration in this step.

The cost of power devices is the major concern for the system design as previously described. The prices of high-power switches with low loss such as Cool-SiC MOSFETs from Infineon are several times higher than the IGBTs. Therefore, the limitation of switching frequency can be determined as 16kHz $\leq f_s \leq$ 25kHz according to their power behaviors versus frequency.

Step 2 The values of initial design parameters are selected from past empirically which will significantly reduce the computation time of the optimization algorithms.

In this step the switching frequency f_s and the number of turns of the primary N_p and secondary N_s transformer are determined. The operating frequency is same as the operating frequency of the phase-shifted PWM control. The number of turns are to be selected based on the ratio of the input voltage and the output voltage. These parameters mainly denote the volume and the power loss of the magnetic components namely the transformer and the inductor.

Step 3 The operating points are determined by the duty cycle, and the duty-cycle loss, as well as the transformer currents. The characteristic values of the primary current $I_{\mathrm{p1}}, I_{\mathrm{p2}}, I_{\mathrm{p3}}$ are determined by the duty cycle-loss $\alpha + \beta$ and the duty cycle D, as well as the power delivered to the output. The RMS-current in the primary transformer can be calculated by the turn-off current of the IGBTs, which will be used in the further steps to calculate the power loss of the power devices and magnetic components in step4 and step5.

Step 4 The switching losses and conduction losses are determined based on the waveforms of the steady-state current and voltages as well as the operation modes. The analytical equations for losses are introduced in the next sections. The losses models are expressed as the function of the RMS value of the current I_{RMS} and the switching frequency f_s.

Step 5 Transformer geometry and the volume of the transformer are determined in this step. The power losses are expressed as the function of the volume of transformer V_{core} and the cross-section area A_c. There is an inner optimization loop to design the transformer with minimum loss and volume.

Step 6 The results from step5 and step6 determine the power density and efficiency of the phase-shifted DC-DC converter design for parameters set in step2. The determined results are forward to the optimisation algorithms

and the design parameters are verified to the step2 to start a new computation turn.

The optimization principles mentioned in this part are described in detail and the analytical expression of loss and volume of power components are given in the next section.

5.4 Analytical Model

The switching modes are described in the previous section and here the analytical expressions to determine the operation points are presented. The loss models of power devices and transformer are given based on the steady-state waveforms.

In this section, the positive primary current i_p during $t \in \langle t_1, t_5 \rangle$ is analysed in detail and its RMS-value are given as following:

As shown in the Fig 5.2, the primary current i_p can be expressed in piecewise linear equations:

$t_1 \leq t \leq t_2$ The voltage applied on the primary transformer is positive v_{AB} and same as the input voltage $+V_{in}$. The primary current rises linearly form zero to the positive value where the diodes $\mathrm{D}_2, \mathrm{D}_3$ are hard switched off at $I = I_{\mathrm{p1}}$ and the slope of the current is $+V_{in}/L_r$, where L_r is the leakage inductance. The primary current $i_{\mathrm{p,t12}}$ during this period is

$$i_{\mathrm{p,t12}}(t) = \frac{I_{\mathrm{p1}}}{\beta \frac{T_{\mathrm{s}}}{2}} \left(t - \alpha \frac{T_{\mathrm{s}}}{2} \right) \tag{5.1}$$

The switching frequency is f_s and the switch period is $T_{\mathrm{s}} = 1/f_s$. In this duty-cycle loss mode, there is no energy transferred to the output during D_{loss}. The phase α and β is given as

$$\alpha = t_1 - t_0 \quad \text{and} \quad \beta = t_2 - t_1 \tag{5.2}$$

$$D_{\mathrm{eff}} = D - (\alpha + \beta) \tag{5.3}$$

$$D_{\mathrm{loss}} = (\alpha + \beta) \tag{5.4}$$

Where the power is delivered in the effective duty cycle D_{eff}.

Moreover, the secondary voltage v_s is zero and no current follows through the secondary transformer, thus the four diodes are all in on state. Thus the secondary will conduct when the primary current reaches to the reflected output inductor current at $t = t_2 = (\alpha + \beta) T_{\mathrm{s}}/2$

$$i_{\mathrm{p}}(t_2) = I_{\mathrm{p1}} = i_{\mathrm{L_{out}}} N_{\mathrm{s}}/N_{\mathrm{p}} \tag{5.5}$$

In the power delivery mode of the powering state, ($t_2 \leq t \leq t_3$) that the primary current $i_{p(t)}$ increases linearly to I_p2 and can be represented as

$$i_{p,t23}(t) = \frac{I_{p2} - I_{p1}}{(D - (\alpha + \beta))\frac{T_s}{2}} \left(t - (\alpha + \beta)\frac{T_s}{2} \right) + I_{p1} \tag{5.6}$$

$$i_{p,t23}(t) = \frac{I_{p2} - I_{p1}}{(D - (D_{eff}))\frac{T_s}{2}} \left(t - D_{eff}\frac{T_s}{2} \right) + I_{p1} \tag{5.7}$$

The IGBT S_{22} is turned off and the capacitance C_{22} discharges completely in the dead time t_d before t_3, the parallel capacitance C_{12} is charged to guarantee that the upper switch S_{12} will turn on with ZVS at $t = t_3$.

In the freewheeling state $t_3 \leq t \leq t_4$, the voltage of secondary transformer is clamped to zero and the primary current decreases linearly from I_{p2} to I_{p3} and it is given as

$$i_{p,t34}(t) = \frac{I_{p3} - I_{p2}}{(1 - D)\frac{T_s}{2}} \left(t - D\frac{T_s}{2} \right) + I_{p2} \tag{5.8}$$

Similarly, the IGBT S_{11} is turned off and the capacitance C_{11} discharges completely in the dead time t_d before t_4, the parallel capacitance C_{21} is fully charged. Thus the upper switch S_{21} will be turned on at ZVS conditions when $t = t_4$.

The PSFB converter switches to operate in the duty-cycle loss mode of the powering state during the interval $t_4 \leq t \leq t_5$. The voltage applied on the primary transformer v_{AB} is negative $-V_{in}$, and the primary current falls to zero from I_{p3}.

$$i_{p,t45}(t) = -\frac{I_{p3}}{\alpha\frac{T_s}{2}} \left(t - \frac{T_s}{2} \right) + I_{p3} \tag{5.9}$$

The current waveform in the primary transformer in the next half cycle is the same as the first cycle but with an inversed signs which are not presented in section.

The RMS value of the primary current can be driven from (5.1) and (5.5)-(5.9) and the analytical equation is given as

$$\begin{aligned} I_p^2 = \tfrac{2}{T_s}[&\textstyle\int_{\alpha T_{s/2}}^{(\alpha+\beta)T_{s/2}} \left(i_{p,t12}(t)\right)^2 \mathrm{d}t + \int_{(\alpha+\beta)T_{s/2}}^{DT_{s/2}} \left(i_{p,t23}(t)\right)^2 \mathrm{d}t \\ &+ \textstyle\int_{D}^{T_s/2} \left(i_{p,t34}(t)\right)^2 \mathrm{d}t + \int_{T_s/2}^{(1+\alpha)T_{s/2}} \left(i_{p,t45}(t)\right)^2 \mathrm{d}t] \end{aligned} \tag{5.10}$$

The duty cycle D is presented as (5.3)-(5.4) and can also be expressed as a function of the number of turns of the transformer

$$D = \frac{V_{out}}{V_{in}}\frac{N_p}{N_s} + (\alpha + \beta) \tag{5.11}$$

where $V_{\text{in}}, V_{\text{out}}$ represent the input and output voltage of the converter. In addition, it can also be expressed as a function of the characteristic value of primary current I_{p1}, I_{p2} and I_{p3} as

$$I_{p\text{RMS}} = \sqrt{I_{p\text{RMS1}}^2 + I_{p\text{RMS2}}^2} \tag{5.12}$$

$$I_{\text{pRMS1}} = \sqrt{D\left[I_{\text{p1}} \times I_{\text{p2}} + \frac{\left(I_{\text{p2}} - I_{\text{p1}}\right)^2}{3}\right]}. \tag{5.13}$$

$$I_{\text{pRMS2}} = \sqrt{(1-D)\left[I_{\text{p2}} \times I_{\text{p3}} + \frac{\left(I_{\text{p2}} - I_{\text{p3}}\right)^2}{3}\right]}. \tag{5.14}$$

The average output of the converter is defined as the ratio of the output power and voltage

$$I_{\text{out}} = \frac{P_{\text{out}}}{V_{\text{out}}} \tag{5.15}$$

The value of peak-to-peak current Δi_{out} in the inductance of the output filter is calculated as

$$\Delta i_{\text{out}} = \frac{V_{\text{out}}}{L_{\text{out}}}(1 - D + \alpha + \beta)\frac{T_{\text{s}}}{2} \tag{5.16}$$

where L_{out} is the output inductor. Moreover, the characteristic values of current in the primary transformer can be calculated graphically according to the Fig 5.2.

$$I_{\text{p1}} = \frac{N\text{s}}{N_{\text{p}}}\left(I_{\text{out}} - \frac{\Delta i_{\text{out}}}{2}\right) \tag{5.17}$$

$$I_{\text{p2}} = \frac{N\text{s}}{N_{\text{p}}}\left(I_{\text{out}} + \frac{\Delta i_{\text{out}}}{2}\right) \tag{5.18}$$

In the free-wheeling state, the voltage of primary and secondary transformer are both clammped by the upper switches [36,38]. Thus the output inductance L_{out} is in series with the referred leakage inductance $L_r^{'}$ where

$$L_r^{'} = (\frac{N_{\text{s}}}{N_{\text{p}}})^2 L_r \tag{5.19}$$

Thus, the primary current I_{p3} when the switch S_{21} is turned on with ZVS at t_4 is determined

$$I_{\text{p3}} = I_{\text{p2}} - \frac{N_{\text{s}}}{N_{\text{p}}}\frac{V_{\text{out}}}{L_\sigma\left(N_{\text{s}}/N_{\text{p}}\right)^2 + L_{\text{out}}}(1-D)\frac{T_{\text{s}}}{2} \tag{5.20}$$

The relationship between phase α and β can derived by equations (5.16)(5.17) and (5.20) shown as

$$\frac{\beta}{\alpha} = \frac{I_{\mathrm{p1}}}{I_{\mathrm{p3}}} \tag{5.21}$$

Thus the duty cycle can be expressed as the function of switching period T_{s} and the characteristic current values

$$D_{\mathrm{loss}} = \alpha + \beta = \frac{L_r}{V_{\mathrm{in}} T_{\mathrm{s}}/2} \left(I_{\mathrm{p1}} + I_{\mathrm{p3}}\right) \tag{5.22}$$

Semiconductor Loss
The losses in the power semiconductors are mainly two parts: the conduction losses and switching losses. The conduction loss of IGBTs are mainly caused by the turn on resistance $R_{\mathrm{CE,on}}$ and the current in the primary transformer I_p. Though the DC/DC full bridge converter with phase-shifted control can turn on the power switches under zero-voltage-switching conditions, the switching loss still exists inside the power semiconductors. The parasitic or the parallel capacitance C_{oss} serves as the snubber and it is a necessary part in the resonant circuit for the soft switching methods. The gate-driver also brings the switching loss to the power switch, the gate-charge Q_{G} will be charged or discharged in the capacitance between the gated and the emitter. The conduction losses in the IGBTs can be driven from

$$P_{\mathrm{cond}} = V_{\mathrm{CE,on}} I_{\mathrm{pavg}} \tag{5.23}$$

where the $V_{\mathrm{CE,on}}$ is the common-to-emitter voltage of an IGBT and I_{pavg} is the averaged primary current in the transformer. In addition, the loss caused by the gated-driver circuit is determined as

$$P_{\mathrm{drive}} = V_{\mathrm{GE,on}}\, Q_{\mathrm{G}}\, f_{\mathrm{s}} \tag{5.24}$$

for a single IGBT, $V_{\mathrm{GE,on}}$ represents for the gate-emitter voltage when the power switch is in on state [39,40].

As discussed in the section 5.2, the power switch is normally supposed to be turned on with ZVS -conditions. One parasitic capacitance of the IGBT is discharged completely, and one capacitance of the switch in the other bridge-leg is fully charged during the dead time. The leakage inductance L_r and the output or parallel capacitance C_{oss} of the IGBT as well as the dead time t_d are the three main factors that determine the resonant charging mechanism. The switching loss might occur when the converter is working the the light-load mode or the part-load mode,where the energy stored in the leakage is less than the energy to charge or discharge the capacitance [41,42]. Thus the residual voltage remains on the bridge arms which will bring out the switching loss when the IGBT is turned on.

To calculate the switching loss with the part-load or light-load conditions, the energy stored in the capacitor can be given by

$$E_{\mathrm{C}} = \int_0^{V_{\mathrm{in}}} v_{\mathrm{CE}} C_{\mathrm{oss}} \left(v_{\mathrm{CE}}\right) \mathrm{d}v_{\mathrm{CE}} \tag{5.25}$$

$$E_{\mathrm{C}} = C_{\mathrm{oss}} \int_0^{V_{\mathrm{in}}} v_{\mathrm{CE}} \mathrm{d}v_{\mathrm{CE}} = \frac{1}{2} C_{\mathrm{oss}} V_{\mathrm{in}}^2 \tag{5.26}$$

Thus the power of switching loss $P_{\mathrm{sw,p}}$ caused by the output capacitance in one single switch is expressed as the function of switching frequency and the residual voltage $V_{\mathrm{CE,on}}$.

$$P_{\mathrm{sw,p}} = E_{\mathrm{c}} \left(V_{\mathrm{CE,on}}\right) f_{\mathrm{s}} \tag{5.27}$$

In this section, IGBT modules are generally used for a high power system, and there is no available output capacitance shown in the datasheet and the switching loss caused by the capacitance of the IGBT module is neglected[]. Therefore, the snubber capacitance are parallel connected to the IGBT modules to achieve the ZVS operation.

For the loss in the rectifier stage or in the secondary stage, the power loss of an single diode can be expressed as

$$P_{\mathrm{D}} = V_{\mathrm{CE}} I_{\mathrm{pavg}} + R_{\mathrm{D}} {I_{p\mathrm{RMS}}}^2 \tag{5.28}$$

where R_D is thought to be a constant value and indicated in the datasheet.

Transformer Model
The loss model of core and winding are presented in this section, which is given by analytical equations as the function of geometry. As the picture shown in Fig 5.5 that the the shell core transformer is built up with one pair of E-cores and the foil windings are arranged around the mid-leg. The results of the models are forward into the inner optimization algorithms to obtain a high-power density converter system. The volume of the transformer can be reduced by adjusting the height of winding window d.

The expression of the optimized foil thickness is given as

$$d_{\mathrm{opt}} = \frac{1}{\sqrt[4]{\Psi}} \sqrt{\frac{\omega I_{w12}}{I'_{w12}}} \delta_0 \tag{5.29}$$

are induced by Hurley that presented in [39], that the influence of skin effect and foil ratio are analytically determined, where Ψ is given as the function of then number of turns N.

$$\Psi = \frac{5N^2 - 1}{15} \tag{5.30}$$

where δ_0 represents the skin depth and is the function of the fundamental frequency f, here σ is the conductivity and μ is the free-space permeability

$$\delta_0 = \frac{1}{\sqrt{\pi f \sigma \mu_0}} \tag{5.31}$$

and the ω is the angular frequency. In addition, I_{w12} is the RMS value of the current in the windings, and the derivative of the current is I'_{w12}.

The effective resistance $R_{\text{eff}}|_{\text{opt}}$ can be approximately linear to the DC resistance of the windings shown as

$$R_{\text{eff}}|_{\text{opt}} = \frac{4}{3} R_{\text{DC}}\Big|_{\text{opt}} \tag{5.32}$$

The DC-resistance of windings is presented as follows that σ_{Cu} is the conductance of copper foil and l_{w12} is the total length of windings and b is the geometry height of the windings.

$$R_{\text{DC}}|_{\text{opt}} = \frac{N l_{\text{w12}}}{\sigma_{\text{Cu}} b d_{\text{opt}}} \tag{5.33}$$

Therefore the loss of copper foils can be expressed as

$$P_{\text{w}} = R_{\text{DC}}|_{\text{opt}} I_{\text{rms}} = \frac{N l_{\text{w12}}}{\sigma_{\text{Cu}} b d_{\text{opt}}} I_{\text{rms}} \tag{5.34}$$

The peak-to-peak flux density B_{pp} of the transformer is given as

$$B_{pp} = \frac{V_{\text{in}}\, D T_{\text{s}}/2}{N_{\text{p}} A_{\text{c}}} \tag{5.35}$$

The core loss of the transformer can be calculated through the improved general Steinmetz equation methods (IGSE) [37,41] as follows:

$$P_{\text{Core}} = p_{\text{core}} V_{core} \tag{5.36}$$

where the p_{core} is the power loss of the transformer core per unit volume, and it is defined as

$$p_{\text{core}} = 2^{\beta+\alpha} D^{1-\alpha} K_i f^{\alpha} B_{pp}^{\beta} \tag{5.37}$$

the parameters here K_i, α and β are the the Steinmetz parameters for the core material.

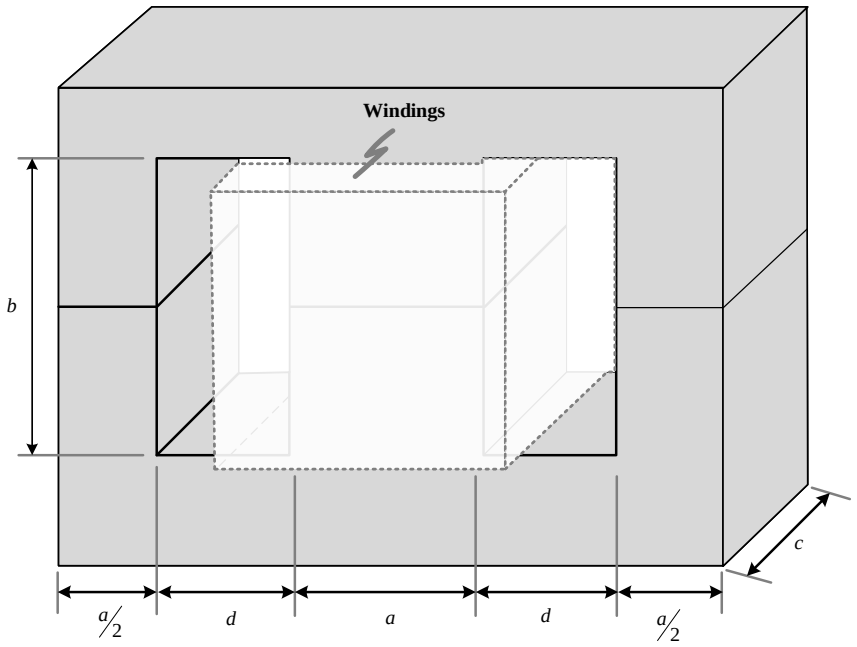


Figure 5.5: Geometry model of a shell-core transformer for phase-shifted full bridge converter with galvanic isolation.

Chapter 6

Simulation and Analysis

In this chapter, the simulation and analytical results for the two-stage AC/DC converter system for 50kW electric vehicle fast-charging stations with low voltage grid is presented. The Simulink models are constructed in the MATLAB and the loss model is then built in the PSIM.The selection of devices is based on the the products available from major manufactures. Finally, the theoretical and simulation results are discussed to verify the design of the fast-charging system.

6.1 Parameters and power components

The simulation of charging system carried out through MATLAB is constructed based on the topology schematics of 3LT^{2}C and PSFB shown in Fig 3.4. A version in detail of the model with implementation of the SVPWM scheme and phase-shifted PWM scheme as well as the control methods is presented in the Appendix A shown as Fig A.2. The three-phase input voltage source with the peak value of 327V and the grid frequency is set to be 50Hz. The inductance and capacitance of the grid input LC filter is 0.6mH and 10.5μF.

The control of the three-phase converter contains the current control and the voltage control. The comparator produce an error voltage signal to the proportional-integral (PI) compensator, which worked as the speed controller as shown in Fig A.2 and produce the reference current i_d^* in the dq frame in the output. The reference current i_q^* as previously described in Chapter 4 is 0 to obtain the unit power factor for the system.

The waveform of the grid-side voltage current are depicted in in the Fig 6.1 and Fig 6.2. The line-to-line voltage V_{ab} and the current in phase as presented in Fig 6.3 shows the achievement of the three-level waveform which means the simulation design is successful. The Fast Fourier Transform (FFT)

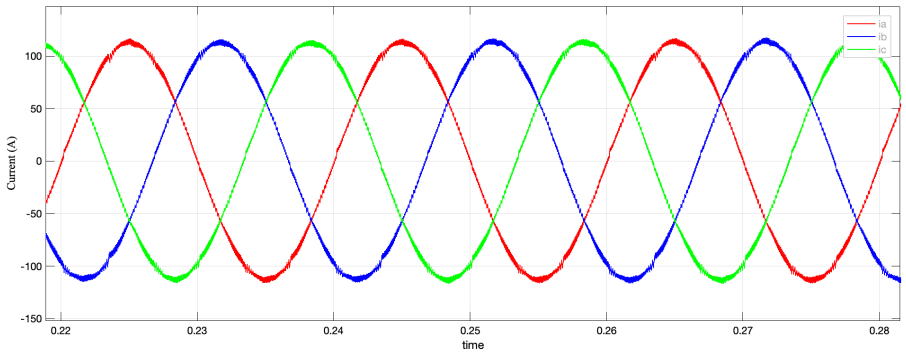


Figure 6.1: The grid-side current waveform

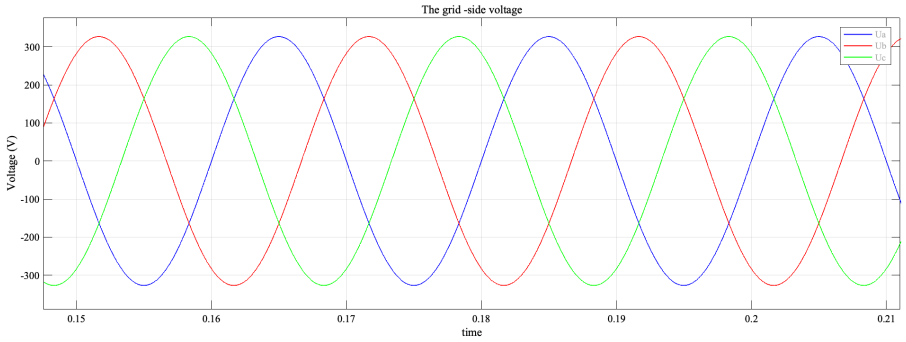


Figure 6.2: The grid-side voltage waveform

Table 6.1: Specifications of the 3LT^{2}C

Parameter	Symbol	Value
Input voltage	V_{grid}	327V
Output voltage	V_{dc}	750V
Nominal power	P_{rec}	50kW
Switching frequency	f_s	16-25kHz
Peak-to-peak voltage	V_{pp}	14V

is applied to analysis the THD of the three-phase AC/DC rectifier. As shown in the Fig 6.4, the fundamental frequency is 50Hz same as the grid-side frequency and the THD equals to 1.98% which is compliant with the standard IEC61851. The line-to-line voltage V_{ab} and the current in phase as presented in Fig shows the achievement of the three-level waveform which means the simulation design is successful as well. The output of the 3LT^{2}C varies around the voltage 750V with a peak-to-peak value 10V less than 5%. Through the simulation model from Simulink, the design meets the specification of the 3LT^{2}C as shown in Table6.1.

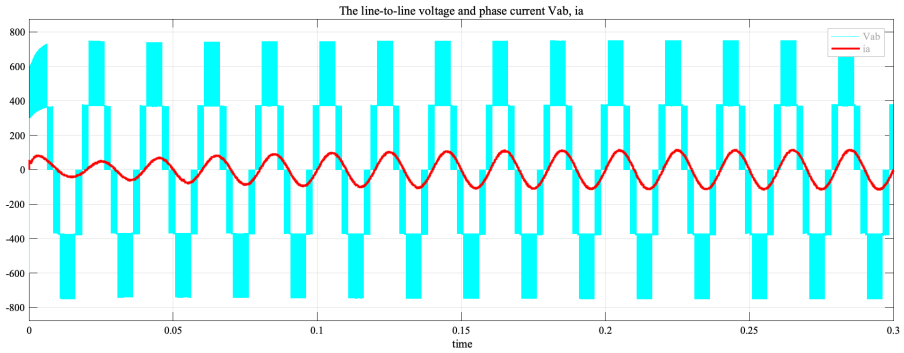


Figure 6.3: The line-to-line voltage and the phase current.

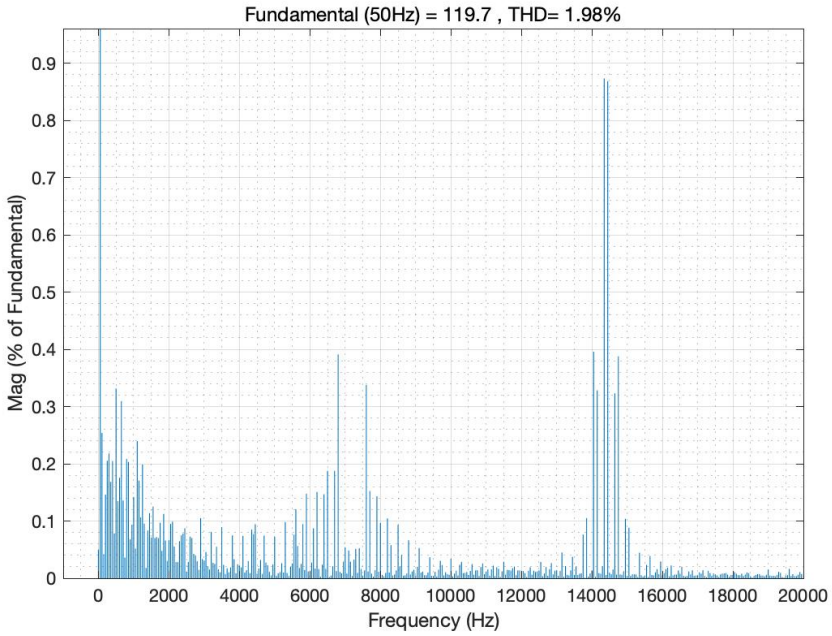


Figure 6.4: The THD of the 3LT^{2}C*converter*.

Table 6.2: Typical features of 600V, 1200V IGBTs

IGBT	Conditions ($T = 125^\circ$) $R_g = 4$ ohm	Eon [mJ]	Eoff [mJ]	V_{CE} (V)
600V FS200R07N3E4R	$V_{CE} = 300V$ $I_C = 200A$	1.7	9	1.7
1200V FF200R12KS4	$V_{CE} = 600V$ $I_C = 200A$	12	18	2.6

The structure of the topology is symmetrical thus four power semiconductors are analysis for the active component losses. The typical features including switching losses and forward voltage drops of selected 1200V device IGBT FF200R12KS4and 600V IGBT FS200R07N3E4R from Infineon are shown in the Table6.2. The typical values are calculated from the datasheet based on the characteristic curves of the devices. The switch energy loss is assumed to be the function of the commutation current and the voltage drop. The forward voltage drop in simulation is linear with the commutation current or IGBT collector current as given

$$v_{CE} = V_{CE0} + \frac{V_{CERA} - V_{CE0}}{I_{CR}} i_c = V_{CE0} + r_0 \cdot i_c \tag{6.1}$$

wherev_{CE} represents for the voltage drop and the V_{CER} is the typical voltage drop given from the datasheet at the rated current I_{CR}. The slope of the voltage-current curve is considered as the constant, which represents for the equivalent resistance r_o.

As discussed in the Chapter 3, it is assumed that the switch loss of the power device is proportional to the commutation voltage. Thus, the turn-on and turn-off energy loss of the power devices is presented in the formula of a quadratic equation with the current i_c.

$$E_{\text{switch}} = \left(A_0 + B_0 \cdot i_c + C_o \cdot i_c^2\right) \cdot \frac{v_{CE}}{V_{CER}} \tag{6.2}$$

The coefficients A_0, B_0, C_0 are determined from the characteristics figures through the curve-fitting methods in MATLAB which describe the relationship between the switch loss and commutation current i_c.

As previous discussed, the averaged switching loss can be calculated according to the switching transition and switching states of the SVPWM method. The averaged conduction and switching loss models presented in Chapter 4 are utilized for calculation in MATLAB.

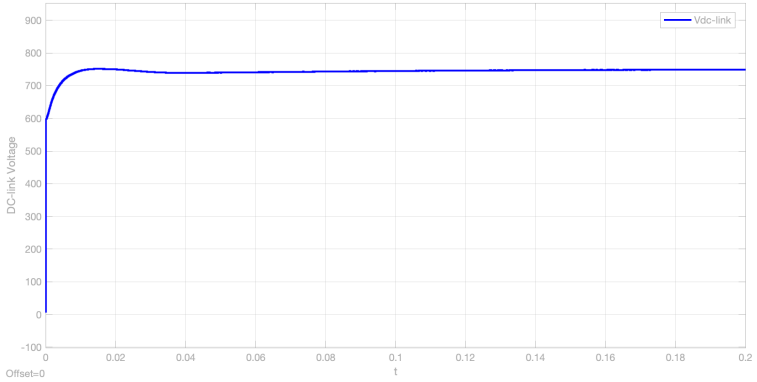


Figure 6.5: The DC-link voltage at the output of the 3LT^{2}C

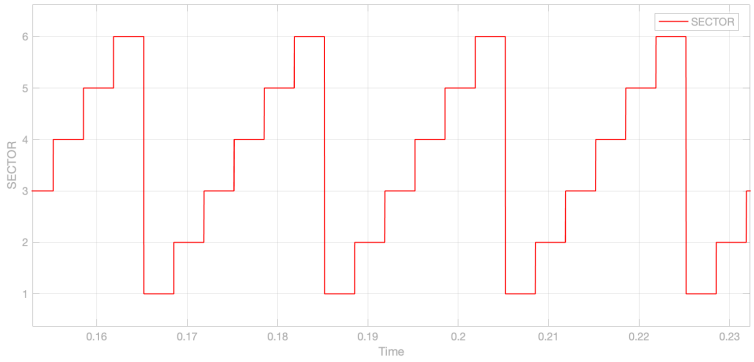


Figure 6.6: SVPWM Sector waveform

In Fig 6.6, the energy loss distribution of the power devices in each phase bridge leg from 100% power load to 20% power load are presented. T_2 and T_3 are the 650V IGBT power device, the 1200V IGBT is paralleled with the 1200V diode, D2 and D3 are 1200V fast diodes as well. The conduction loss and switch energy loss for each components are shown in Table. The output DCV-link voltage remains 750V as shown in Fig6.5. Moreover, the sector judgement graphs for SVPWM is shown as Fig6.6.

Table 6.3 shows a summary of the simulation results carried out by PSIM and theoretical results from the general loss model shown in the previous chapter. The conduction loss and switch loss are compared in each bridge-leg components as well as the total energy loss difference between the simulation and calculation results are listed. The power loss distribution of the 3LT^{2}C with 100%, 50%, 20% power level in one phase is depicted in Fig 6.8. The efficiency calculated from the simulation software is 98.5% which is higher than the calculation results 97.9 % in the 100% power operation mode.

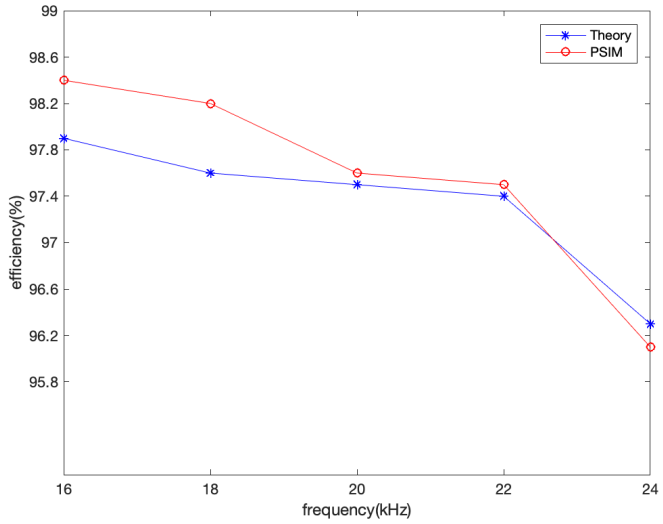


Figure 6.7: The relationship between the rectifier efficiency and switching frequency in the 3LT^{2}C

Table 6.3: The loss distribution of 3LTC from PSIM model and theoretical model

	Simulation		Theotical		Difference
Device	P_{cond} [W]	P_{switch} [w]	P_{cond} [W]	P_{switch} [w]	Percent%
T1	8.2	28.6	10.2	32.7	−16.7
D1	53.5	104.2	62.9	121.5	−15
T2	15.8	52.7	16.3	53	–
D2	15.8	13	16.3	17	0.8
T3	15.8	52.7	16.3	53	0.8
D3	15.8	13	16.3	17	8
T4	8.2	28.6	10.2	32.7	–
D4	53.5	104.2	62.9	121.5	−15

The relation between switching frequency and converter efficiency is shown as Fig 6.7.

PSFB simulation

The specifications of the PSFB converter is given as Table 6.4 as well as the design parameters are listed in Table 6.5.

To operate under the ZVS condition, the energy stored in the leakage inductance must be higher than the resonant charging or discharging the paralleled capacitance of the IGBTs during the dead time. In this design that the

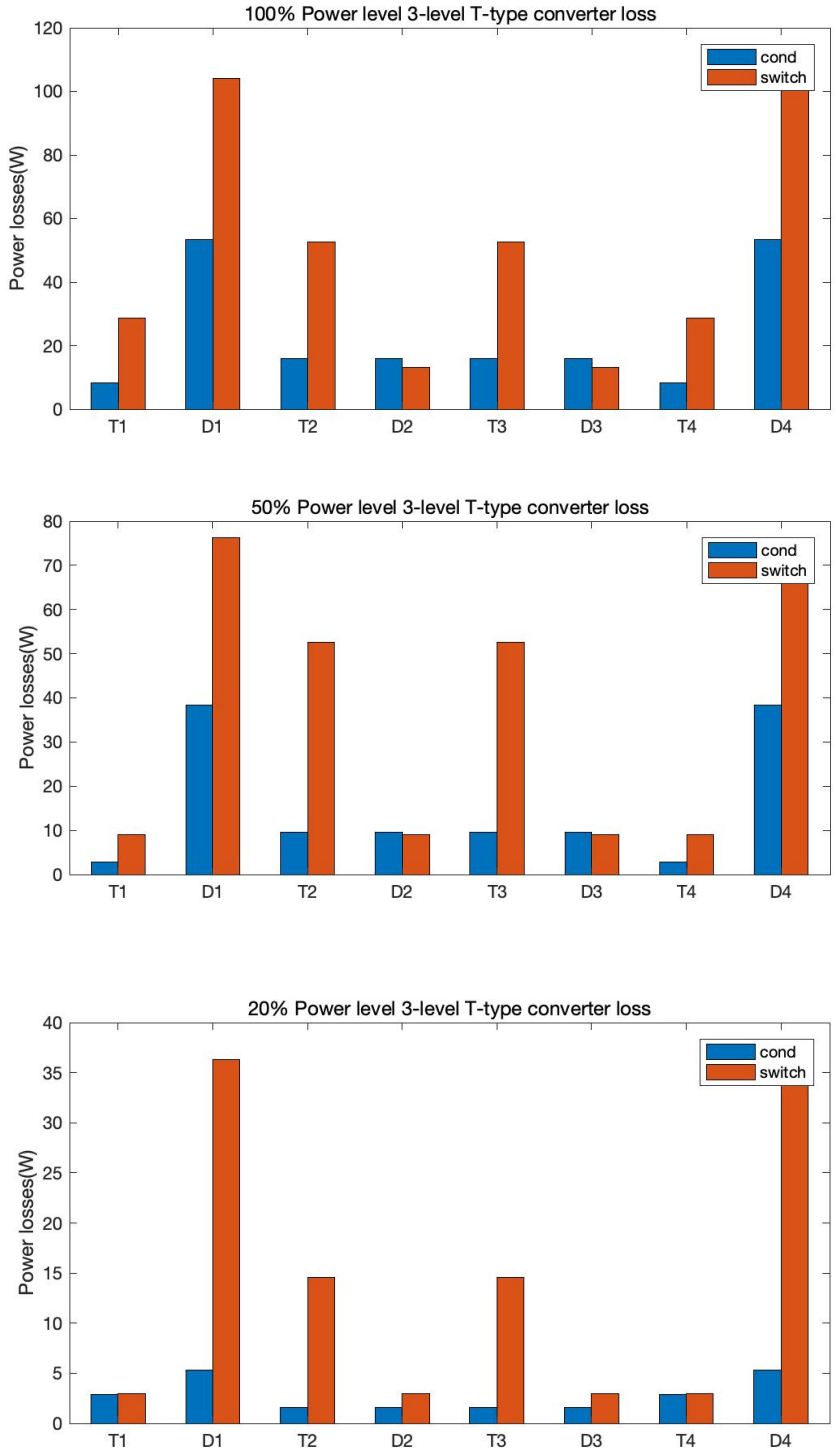


Figure 6.8: 100,50, 20% power loss distribution of the 3LT^{2}C

Table 6.4: Specifications of the PSFB converter

Parameters	Symbol	Value
Input voltage	$\boldsymbol{V_{dc}}$	750V
Output voltage	$\boldsymbol{V_o}$	$280-420$V
Nominal Power	$\boldsymbol{P_T}$	50kW
Switching frequency	$\boldsymbol{f_s}$	$16-24$kHz

Table 6.5: PSFB design parameters

Parameter	Symbol	Value
Output capacitor	C_{oss}	$2nF$
Leakage inductor	L_R	$1\mu H$
Output filter	L_F	$100\mu H$
Output capacitor	C_o	$33\mu F$

leakage inductance is working as the resonant inductor and no other inductance exists in the primary side. The energy stored in the leakage inductance E is

$$E = \frac{1}{2}L_r I_p^2 > \frac{4}{3}C_{oss}V_{dc}^2 + \frac{1}{2}C_T V_{dc}^2 \tag{6.3}$$

where L_r is the leakage inductance of the primary side transformer, C_{oss} is the parallel capacitance, C_T represents for the winding capacitance of the primary transformer, I_p is the primary current of the transformer.

As described in the previous Chapter that the dead time should be enough large to guarantee that the capacitance can be fully charged or discharged completely before the ZVS turn-on of the switches. Thus the minimum value of the dead time is

$$t_d > 2C_r V_{dc}/I_{p1} \tag{6.4}$$

The maximum dead time is set as

$$t_d < \frac{T}{4} = \frac{\pi}{2}\sqrt{L_r C_r} \tag{6.5}$$

where the resonant capacitance C_r is defined as

$$C_r = \frac{8}{3}C_{oss} + C_T \tag{6.6}$$

PSFB simulation Results

The material of the transformer core is made up with nanocrystalline in VITROPERM500F. One significant advantage of this material is that the winding

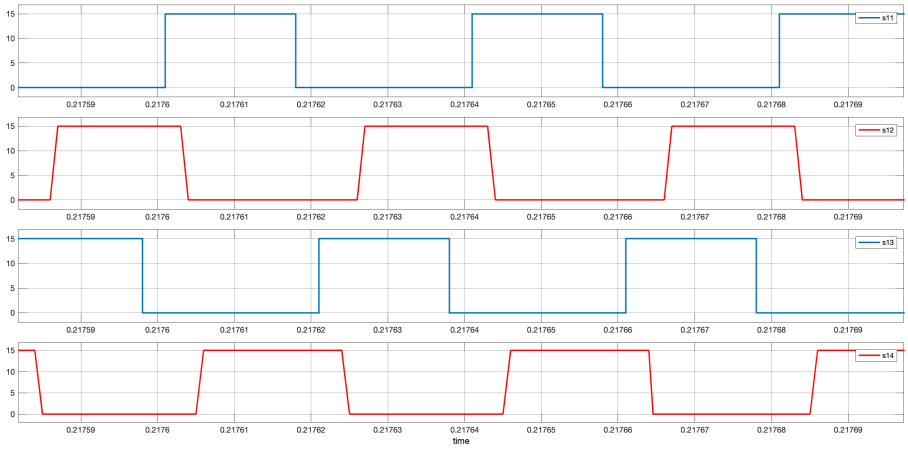


Figure 6.9: The waveform of the gate signals of the PSFB converter

capacitance is close to zero and thus the resonant inductance L_r will be reduced as well as the volume of magnetic components decreased.

The parameters are computed from the optimization algorithms described in Chapter5. The theoretical results are calculated from the equations (5.23-5.28)and (5.34-5.37) The power loss for 100% is given

Total losses consists of the losses of switches (conduction losses in the rectifier diodes (conduction loss) and transformer (core and copper losses). Therefore, the efficiency of the converter is expressed as

$$P_{\text{Loss}} = P_{sw} + P_{con} + P_d + P_{C_u} + P_{\text{Core}} \tag{6.7}$$

$$\eta = \frac{P_o}{P_o + P_{loss}} \tag{6.8}$$

The simulations results shown in Fig 6.9-12 verify the design of the PSFB is compliant with the design specifications. The current through the primary side of the transformer is shown in Fig 6.9. It is clear to see that the voltage changes from the zero to positive while the current is still remained as negative, which achieved the ZVS. The peak-to-peak ripple of the DC current output is 15A which is less than 20% and also in the working region for the inductors. The signals from driver circuit is shown as Fig 6.13.

The power device IGBT: FF200R12KT4 from Infineon Technologies and diodes MEK250-12DA from IXYS Corporation are selected for the system design. The distributions of power loss is described in Fig 6.14 for the converter with a full load of 50kW power, and the theoretical efficiency is 97.4%. The relationships among the converter efficiency, switching frequency as well as the power load are depicted in Fig 6.15.

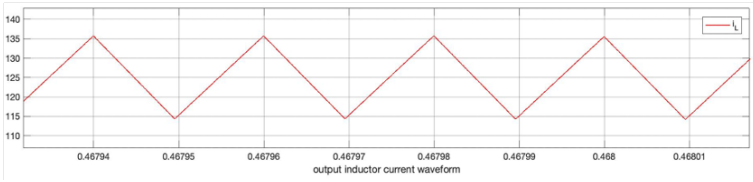


Figure 6.10: The DC current output of the charging system.

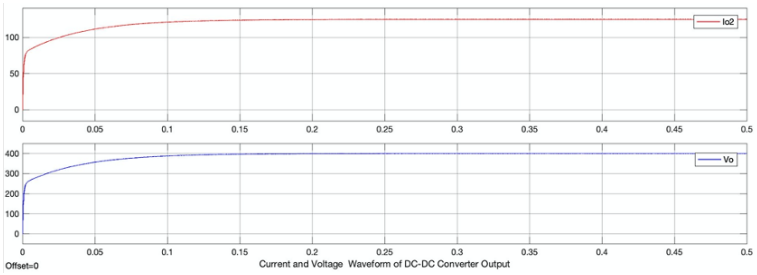


Figure 6.11: The waveform of output current and voltage of the PSFB converter

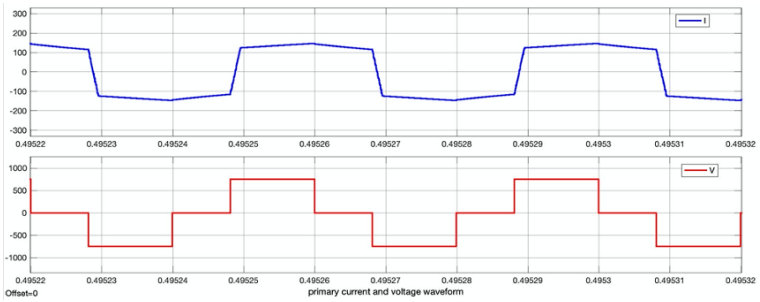


Figure 6.12: The voltage and current in the primary side transformer.

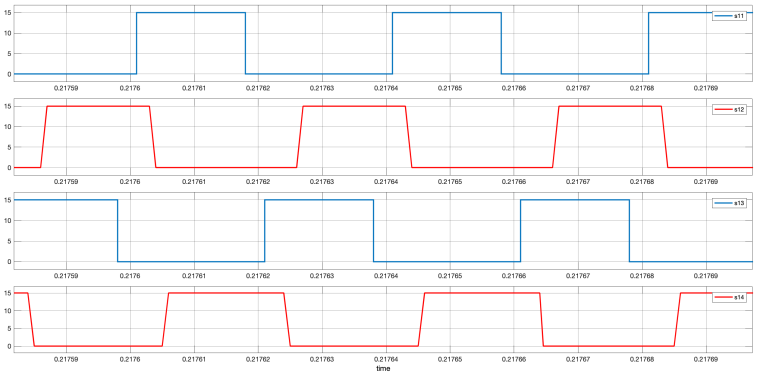


Figure 6.13: The waveform of the gate signals of the PSFB converter.

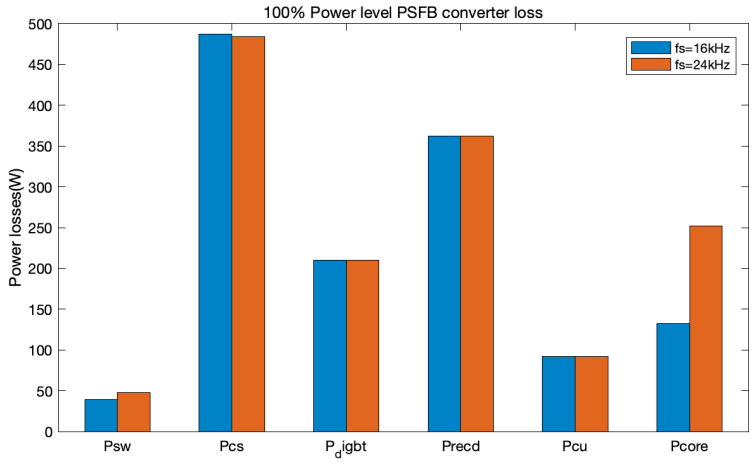


Figure 6.14: 100% power loss distribution

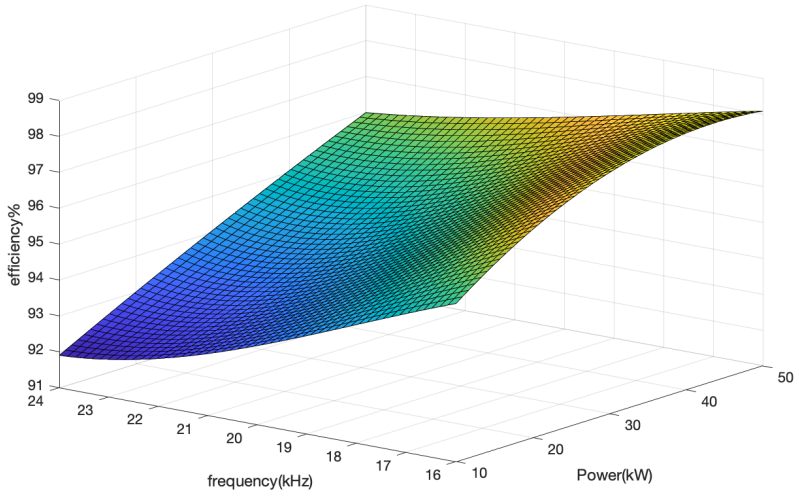


Figure 6.15: The 3D figure shows relationships the efficiency among the switching frequency and the power level.

6.2 Discussion

As the design of the three-level T-type AC/DC rectifier and the PSFB DC/DC converter is presented previously, the system for EV fast-charging station with LV grids gains a total efficiency 95.7% for the full-load test. The design is in compliance with the standards from IEC and the industry standards-CHAdeMO formed by major automakers. Thus the design can be considered by most charging infrastructure manufacturers for realization.

The difference between results from theoretical analysis and simulation models carried out by and MATLAB and PSIM is discussed in this section. There are two main reasons that the calculation power semiconductor losses in $3LT^2C$ is higher the simulation results. The major reason is that the parameters chosen for analytical models is not same as the value adjusted by software for simulation. The parameters including the forward drop voltage V_{CE} and switch energy loss $E_{on,off}$ chosen are under the assumption that the temperature of the devices is constant $T_j = 125^\circ$ and will not influenced by the surroundings. The software considers more characteristics of the power device such as transient thermal impedance and the thermistor-temperature characteristic. Thus, the simulation results could be slightly different.

Another reason that the difference occurs is, the sampling of software is not continuous and the loss results calculated by integral equations or methods might induce some errors. The PI compensators in the control part influence the quality of the waveform and dynamic response for sampling. This effect was found during the simulation and solved by optimizing the coefficient and limits in the controllers. Thus the errors might occur in the results generated from simulation solvers.

The results of energy loss from simulation indicates that the $3LT^2C$ works below $125^\circ C$ in the safe operating area. The passive cooling can be utilized for the system due to the simulation loss keeps constant. Therefore, the passive cooling method can be utilized for the system, which means that no extra devices are required that the total volume of the components will not be increased. The power density will be not reduced as well.

It is similar to the $3LT^2C$, the analytical energy losses are less than the simulation re in the PSFB converter. The main reason is that the thermal loss generated by the IGBTs are not considered in the analytical model. It can be concluded that the design is successful. Moreover, the chip-area consideration and thermal loss distribution are required for industry design in the future.

Chapter 7

Conclusion and future work

7.1 Conclusion

This thesis focuses on the fast-charging station for electric vehicles connected to the LV grid. The main challenge of the project is to develop a high-efficiency and high power-density off-board charging systems for LV applications. The background of EVs are investigated and a review of the state-of-the-art charging techniques for current available products of EV in the market is presented in Chapter 1. The DC off-board charging technology is most common-used for high power fast-charging of EVs. In Chapter 2, the realization and design aspects of the fast charging station are introduced. The bidirectional AC/DC converter and the unipolar power follow DC/DC converter with galvanic isolation are chosen for the final charging system structure. Through the literature view of non-modular topologies, the $3LT^2C$ converter and the PSFB converters are chosen for the two-stage AC/DC converter system for EV charging for low-voltage application in Chapter 3.

Moreover, the commutations of the $3LT^2C$ and implementation of SVPWM are presented in Chapter 4. The analytical model for active component losses is build by determining the power loss matrix. The power loss matrix is expressed in terms of the switching states vectors and current vectors. Thus the average loss of the power device can be calculated by integrating with the electric angle. In Chapter 5, the design procedure for efficiency optimization is developed by determining the operation points and duty cycle of the PSFB converter. In addition, the analytical loss models of power devices and passive components are determined as well. Finally, the design specifications and parameters for simulation models and theoretical analysis are listed in Chapter6. The design and selection of components are verified by both simulation and analytical results. As the shown in the results, the two-stage AC/DC converter system delivers 50kW to the full-load output with

the efficiency of 95.7% and THD 1.98%. Thus, it can be concluded that the project develops successfully a high-efficiency fast-charging 50kW station for electric vehicles with low-voltage grids that complies with the standards of IEC and CHAdeMO.

7.2 Future Work

There are several aspects to develop the thesis work in the future.

- The modulation method can be optimized to reduce the switching loss in the 3LT^{2}C converter. The 7-segment SVPWM can be replaced with discontinuous PWM (DPWM) scheme which contains 5 segments in each switching sequence. Thus, the total transition times of the power switches in each phase leg will be reduced which results in a lower switching losses.
- The losses of the other passive components including the output capacitance and inductance in the filter should be considered in the future work. The loss model of the output capacitance can be build to develop a higher power-density PSFB converter. In addition, the passive cooling system such as heat-sinks should be considered as well.
- The thermal models for power devices should be constructed to optimized the chip areas which will increase the total power density of the system.
- One disadvantage of the PSFB converter with phase-shifted PWM is that the converter operates in hard switching regions with light loads or partial-loads, where switching losses dominates the loss of power semiconductors. The other modulation methods such as triangular current mode modulation or trapezoidal current mode modulation can be applied to achieve soft switching in the full-range load.

Appendix A

Appendix

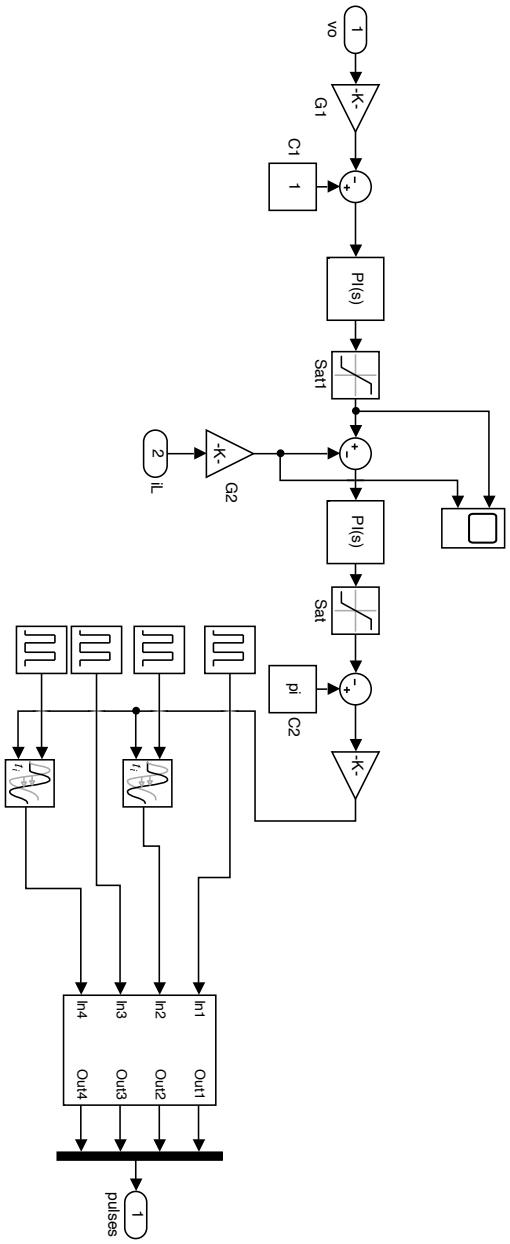


Figure A.1: PSFB control simulink

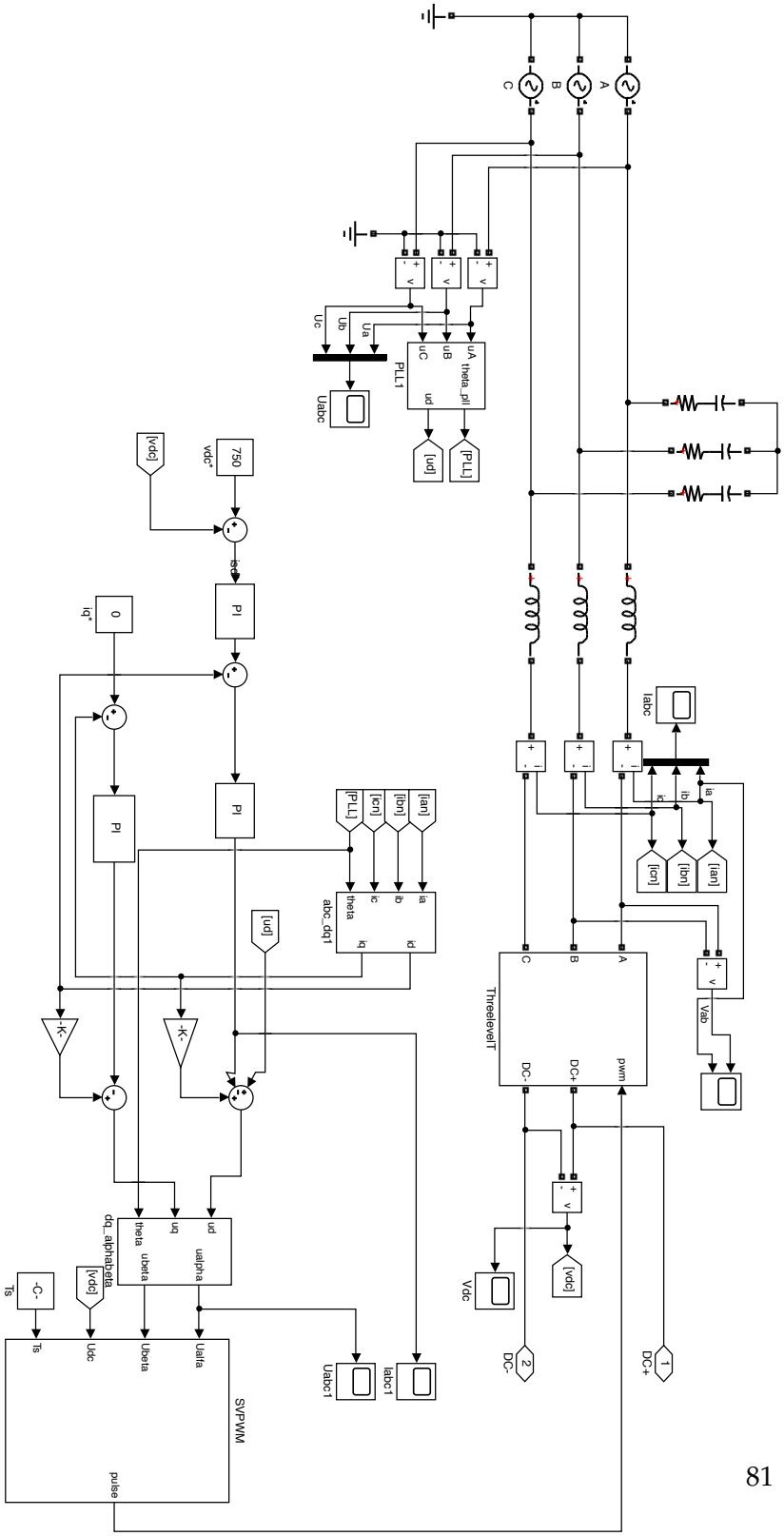


Figure A.2: Simulink model of 3LT^{2}C

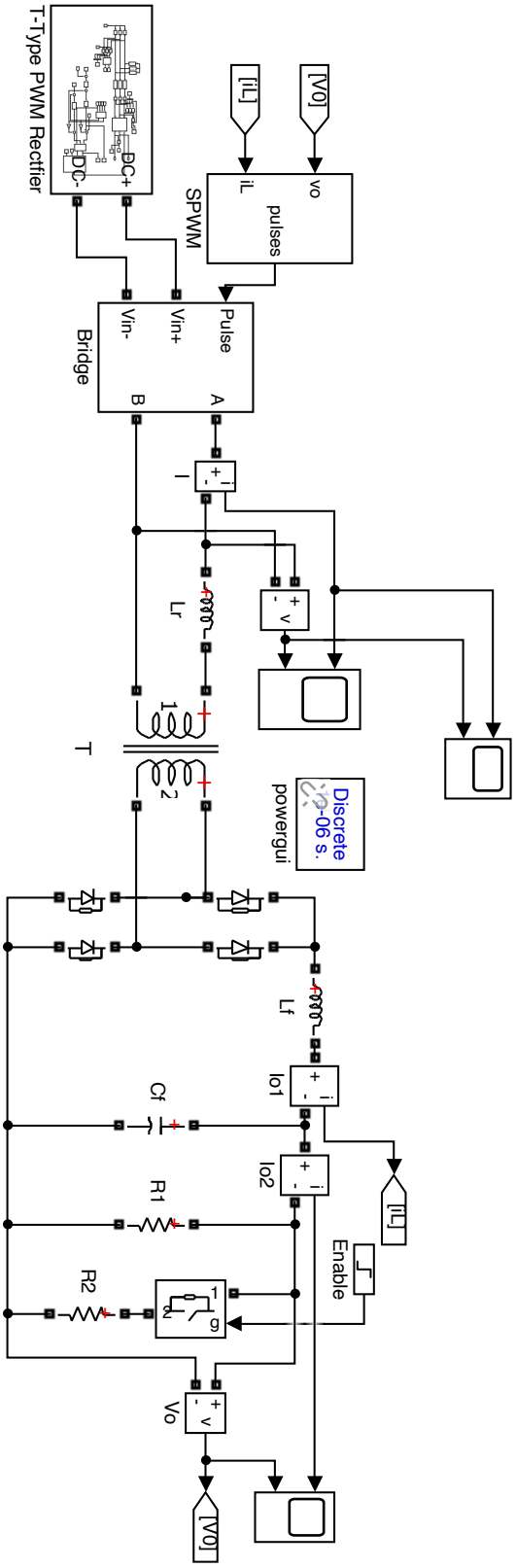


Figure A.3: Two-satge AC/DC converter

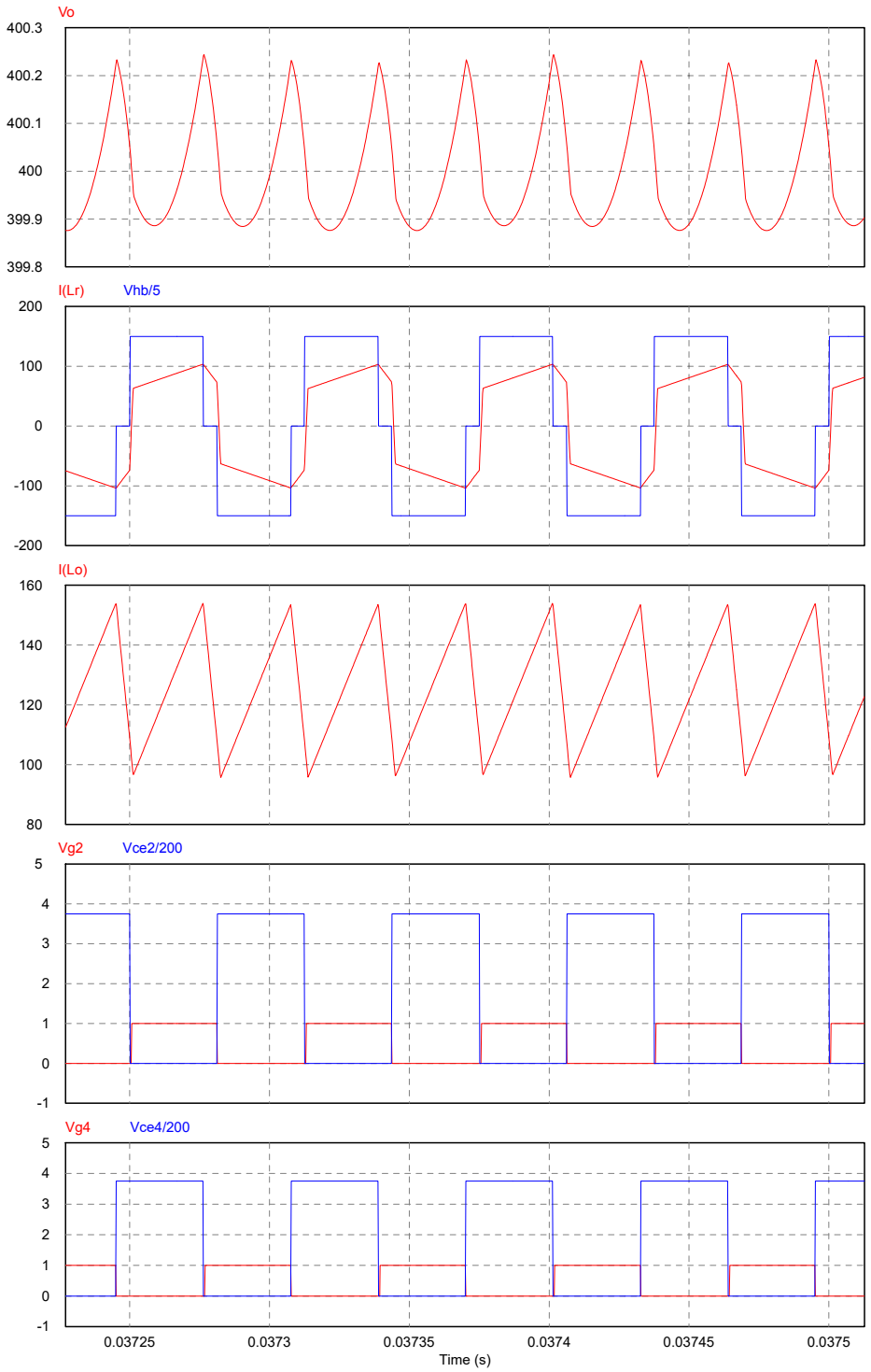


Figure A.4: The waveform of the PSFB converter(a) The output voltage V_o (b) The primary current in the leakage inductance and the the primary voltage(c)The output current (d) The gate signal and

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