Silicon-Based Integration of Groups III, IV, V Chemical Vapor Depositions in High-Quality Photodiodes

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Chapter 1

Introduction

While the backbone of the semiconductor industry is silicon technology with a clear CMOS dominance, III-V semiconductors are playing an increasing role as suppliers of optical functions and high-speed electronics. While the latter application is holding ground but must constantly compete with the continual speed advances made in CMOS, the photonic industry is one of today's fastest growing industries driven by a very wide range of potential applications. It is therefore not surprising that there is a vibrant interest in merging photonics with electronics. In Holland, this endeavor crystallized in 2006 in the large SmartMix program MEMPHIS "Merging Electronics and Micro and nano Photonics in Integrated Systems". This program supported the view that "our future lives will be changed by an ambient, intelligent, comfortable and safe environment, by continuous health monitoring, by personal communication and by early detection of threats from nature, technical failure and human activities". These developments require new complex miniaturized devices with vastly increasing functionalities against the lowest possible cost price which cannot be fulfilled with present micro-electronic technology alone. The limitations of present electronics require a new massive converging technology based on complementary characteristics of *micro-* and *nano-electronics* and *micro-* and *nano-photonics*, utilizing the best of both technology worlds. A low cost combination of the processing power of classical CMOS IC technology, the high frequency capabilities of modern High Frequency (HF) electronics and the large bandwidth offered by integrated photonics creates the technology for novel broadband miniaturized *"electronic-photonic devices"*. This will open the way to major new applications for the use of light: in medical diagnostics, for healthcare, entertainment, telecommunications, tracking and positioning. The MEMPHIS vision is illustrated in Figure 1.1.

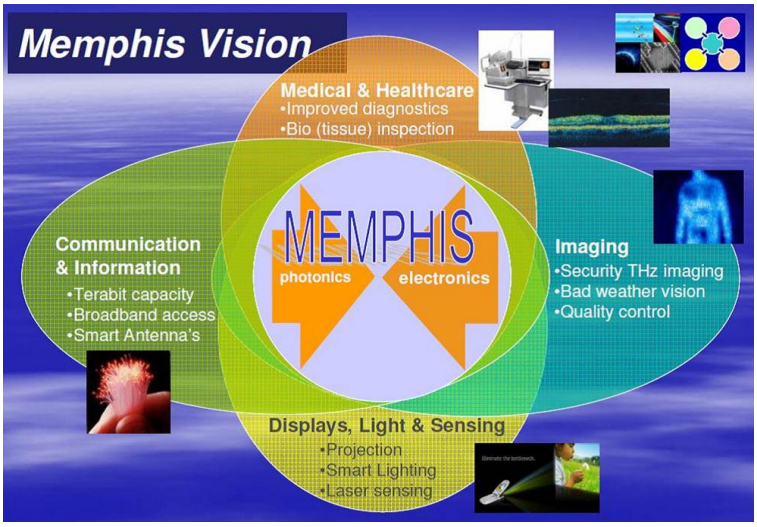


Figure 1.1: The MEMPHIS vision of the impact of merging electronics with photonics.

The work presented in this thesis has formed the part of the technology developments promoted in the MEMPHIS program. The focus was placed on the merging of III-V semiconductor technology with Si technology. It by no means represents the first attempts in this direction; on the contrary, since the early days of integrated circuits it has been one of the holy grails for the semiconductor industry to grow high-quality III-V materials on Si. Nevertheless, in many ways it remains an elusive goal towards which this thesis has made its own specific contributions. The experimental basis was the development of a new tool for chemical vapour deposition (CVD) of III-V materials with an initial focus on gallium arsenide (GaAs). Conventionally, CVD of these materials is achieved from high concentrations of gases, including metal-organics, in equipment referred to as Metal-Organic CVD (MOCVD) epitaxy systems. The high gas concentrations, particularly of the highly toxic gases arsine (AsH_3) and phosphine (PH_3), mean that severe safety precautions must be implemented when running MOCVD. For this reason, most MOCVD III-V materials fabricated today are produced in dedicated laboratories not directly connected to Si cleanroom facilities.

In the MEMPHIS project the growth of both III-V compounds and Si/SiGe was combined in one and the same CVD system: the ASMI Epsilon 2000, a commercial CVD system designed for Si and SiGe epitaxy. The tool was especially equipped for the growth of III-V compounds in a manner that did not exclude

the use of the system also for Si-based depositions. For this purpose, the system was extended with a TriMethylGallium (TMGa) bubbler and extra tubing to allow the deposition of GaAs as well as the standard Si and SiGe depositions. Good results were achieved for epitaxial growth of GaAs with a very low AsH_3 concentration: 0.7% as compared to the at least ten times higher values normally used in MOCVDs. The correspondingly low concentration of TMGa means that the contamination of the reactor chamber with gallium or arsenic is so low that standard high-quality low-doped Si and SiGe depositions can still be performed in the same chamber. Moreover, the low gas concentrations permit the system to be run with the same safety precautions that apply to a normal Si/SiGe reactor. Thus there is no issue with respect to adding this equipment to a CMOS cleanroom environment.

The crucial feature that made it possible to reach the results presented in this thesis was the new availability of gallium (Ga), boron (B), germanium (Ge), silicon (Si), arsenic (As) and phosphorus (P) in one and the same epitaxial reactor. Deposition cycles containing layers of different combinations of these III, IV, V elements could then be performed without vacuum break. This proved important not only for the growth of good quality Ge and GaAs but also for the formation of junction diodes in these materials. In particular, the formation of p^+n Ge-on-Si diodes of exceptional quality was facilitated by deposition of pure gallium (PureGa) and pure boron (PureB) to create the p^+-region. The ideas leading to this solution leaned strongly on the success of PureB depositions to form nanometer-shallow p^+n Si diodes. These are now extensively used as photodiodes for detecting beams that only penetrate a few nanometer into the Si such as vacuum-ultraviolet (VUV) light and electrons with energies below 1 keV [1, 2]. In the present work, similarly good results were achieved with PureGa deposition on Si to form p^+n Si diodes. In all these diodes formed by *pure dopant deposition*, PureB/Ga for Si diodes and PureGa plus PureB (PureGaB) for Ge-on-Si diodes, the excellent electrical characteristics have been ascribed to the creation of a very high hole concentration at the interface between the semiconductor and the bulk dopant material. This is not seen in other ultrashallow diodes produced by techniques that only aim at damage-free doping of the semiconductor, for example, epitaxy of doped Si or Ge, or doping from a gas [3]. Therefore the terms PureB/PureGa/PureGaB have been introduced to underline that a solid layer of pure dopant material has been deposited.

On the applications side, this thesis work has been directed towards the very challenging feat of fabricating Ge avalanche photodiodes (Ge APDs) on Si substrates. This was motivated by the good I-V characteristics obtained for the first

PureGaB Ge-on-Si diodes. Besides having a low dark current, they also displayed a clear breakdown curve that was proven to be suitable for infrared (IR) photon counting in Geiger mode. Compared to the PureB Si photodiodes, these Ge photodiodes are many times more complex to optimize. A new method was developed to grow high-quality, As-doped crystalline Ge in tens-of-micron large windows to the Si with only a 200 nm transition region to localize the misfit dislocations. However, both the Ge growth and the As-doping are subjected to strong CVD loading effects, i.e., the circuit layout will influence the geometry and doping distribution of the Ge-islands, which are factors that are decisive for the breakdown mechanism. Nevertheless, in view of the multitude of applications of sensitive infared detectors and imagers, gaining control of the Ge-on-Si growth is a very worthwhile endeavor and this thesis offers solutions to a number of the issues.

In the following, an overview on photonic materials and basics of semiconductor photodetectors is provided. Different photodiode technologies are reviewed with focus on their characteristics and special qualities. Also some of the unique properties and applications of Ge, which became the main vehicle for the work in this thesis, is studied with the focus on the processing and technological issues.

1.1 Fundamentals of photodetection

The science of photonics includes the generation, emission, transmission, modulation, signal processing, switching, amplification and detection/sensing of light and it covers the whole light spectrum from ultraviolet over the visible to the near-, mid- and far-infrared. A variety of applications from telecommunications to displays involves photonic semiconductors. Photodetection and light emission, however, have always been two of the largest and most interesting application areas. Both photodetection and light emission in semiconductors work on the general principle of the creation or recombination of electron-hole pairs upon exposure to light. According to Albert Einstein, who won a Nobel prize for the discovery of the photoelectric effect [4], anytime a photon hits a conductor it can excite electrons. The same phenomena happens in a semiconductor. When a semiconductor material is illuminated by photons of an energy greater than or equal to its bandgap, the absorbed photons promote electrons from the valence band into excited states in the conduction band, where they behave like free electrons able to produce electrical current in the crystal structure under the influence of an intrinsic or externally-applied electric field. In addition, the positively-charged

holes left in the valence band contribute to electrical conduction by moving from one atomic site to another under the effect of the electric field. In this way the separation of electron-hole pairs generated by the absorption of light gives rise to a photocurrent, which refers by definition to the fraction of the photo-generated free charge-carriers collected at the edges of the material by the electrodes of the photodetecting structure. The intensity of such a photocurrent at a given wavelength increases with the intensity of incident light.

On this level we can distinguish between two large categories of photodetectors based on the nature of the electric field, which causes the charge separation of photogenerated electron-hole pairs: (i) photoconductors, which consist of a simple layer of semiconductor simply with two ohmic contacts, where the electric field leading to the collection of the charge-carriers is provided by applying a bias voltage between the contacts at either end, and (ii) photovoltaic photodetectors, which use the internal electric field of a pn or Schottky (metal-semiconductor) diode to achieve the charge separation. This last term covers pn junction photodetectors (photovoltaic structures consisting of a simple pn junction, and pin photodetectors which include a thin layer of semiconductor material between the p- and n-regions which is not deliberately doped), as well as all Schottky junction photodetectors (Schottky barrier photodiodes and metal-semiconductor-metal (MSM) photodiodes) [5].

Other optical devices similar to photodetectors are solar cells which also absorb the energy of light and turn it into electricity by generation of electrical carriers; and light emitting diodes (LEDs) which are basically the inverse of photodiodes, instead of converting light to a voltage or current, it converts a voltage or current to light. In the following, some properties of photonic semiconductors are presented and then details of some well-known types of photodiodes are given.

1.1.1 Photonic semiconductor materials

The minimum energy of a photon that is required to generate an electron-hole pair in a semiconductor is defined as the work function and the number of electrons generated is proportional to the intensity of the light. The semiconductor photodetectors are made from different semiconductor materials such as Si, Ge and InGaAs. Each material has a characteristic bandgap energy E_g which determines its capability to absorb photons. The equation between E_g and cut-off wavelength λ_c is:

$$\lambda_c = \frac{1.24 \times 10^3 (nm)}{E_g(eV)} \tag{1.1}$$

Semiconductors with smaller bandgaps can absorb larger wavelenghts of light. Figure 1.2 shows the bandgaps of different semiconductors with their corresponding wavelengths with respect to the visible light. The information in Figure 1.2 is summarized in Table 1.1 for some prominent photonic materials, their bandgaps , and cut-off wavelengths λ_c at room temperature (300 K).

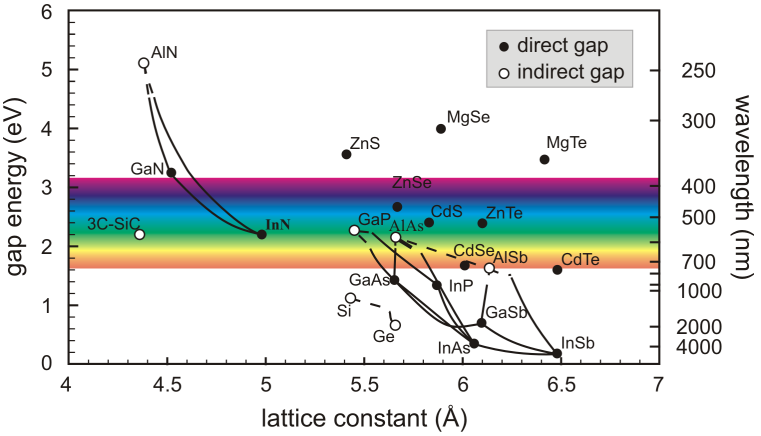


Figure 1.2: Bandgaps as a function of lattice constant and corresponding wavelengths of different semiconductors.

Table 1.1: Important photodetector semiconductors, the bandgaps and corresponding photon wavelengths [6].

Type	**E$_g$(eV)**	**λ_c (nm)**	**Band**
Si	1.12	1100	Visible
Ge	0.66	1800	Near-Infrared
GaAs	1.42	875	Visible
InGaAs	0.73 - 0.47	1700 - 2600	Near-Infrared
InAs	0.36	3400	Near-Infrared
InSb	0.17	5700	Medium-Infrared
HgCd	0.7 - 0.1	1700 - 12500	Near to Far-Infrared

One of the important terms in qualification of a photonic semiconductor is

the light absorption coefficient. In order to have a good photonic device with high quantum efficiency (QE), the absorption coefficient of the semiconductor should be high enough for the majority of the photons to be absorbed in the active detector region. Above the bandgap (or below the corresponding cut-off wavelength) the absorption increases rapidly. For semiconductors with direct bandgaps such as GaAs and InGaAs this is rather easily obtained. The difference between direct bandgap and indirect bandgap semiconductors is shown in Figure 1.3. Light induced electron-hole pair generation in semiconductors with indirect bandgap requires both photon and phonon assisted transitions [7].

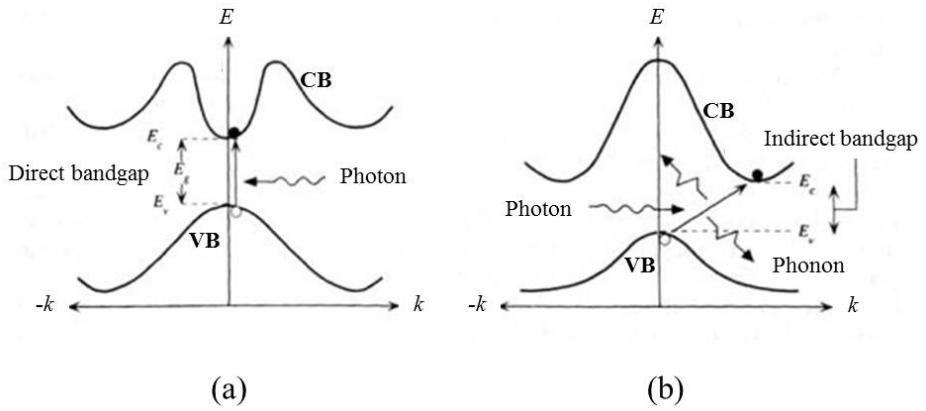


Figure 1.3: Photon absorption in semiconductors with a) direct and b) indirect bandgaps. Photon absorption in a semiconductor with an indirect bandgap requires phonon assisted transition.

Figure 1.4 shows the absorption coefficient and penetration depth of photons with different wavelengths for four different semiconductors. For GaAs and InGaAs, a penetration depth of 1 µm is obtained for wavelengths below 800 nm and 1400 nm, respectively. A penetration depth of 10 µm is found at 855 nm and 1850 nm, respectively.

Both Si and Ge are indirect semiconductors with a much weaker absorption directly above the bandgap. The corresponding cut-off wavelength for Si is 1100 nm. The 10 µm penetration depth is only reached in the red (800 nm) and the 1 µm penetration depth in the visible (550 nm). Despite this, Si detectors with good QE in the red and very near-infrared are fabricated with a large detector region and diffusion controlled carrier movement, but these detectors are inherently slower than III-Vs counterparts -depending on the design- and lack good responsivity in

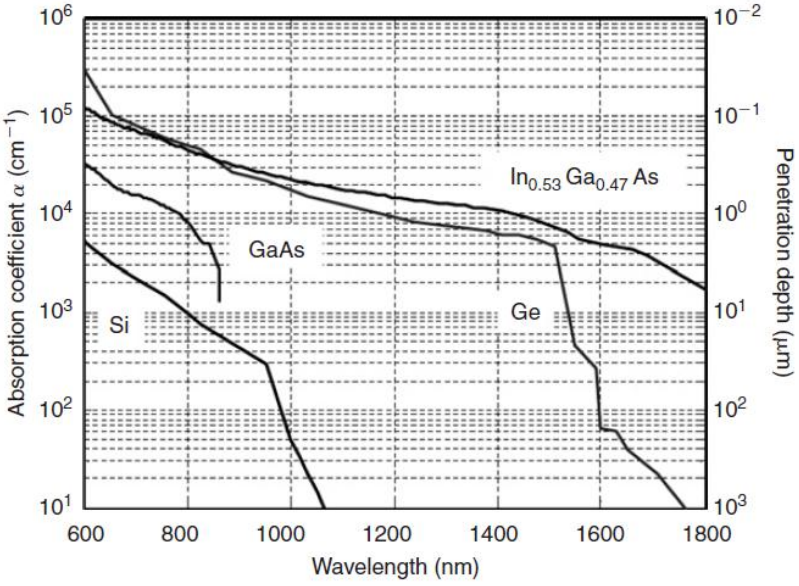


Figure 1.4: Absorption versus wavelength for two direct bandgap (GaAs, InGaAs) and two indirect bandgap (Si, Ge) semiconductors. [8]

the near-infrared wavelengths. Although Ge is also an indirect semiconductor its absorption curve looks very different. Below the cut-off at about 1800 nm a slight increase in absorption is seen as typical for the indirect bandgap but below 1600 nm a steep increase follows. This is a consequence of the lowest direct transition in Ge being slightly above (0.2 eV) the indirect transition (0.66 eV) whereas in Si the lowest direct transition (3.4 eV) is far above the indirect one (1.12 eV) [8]. One can distinguish three regions if we compare the absorption of Si and Ge. From the visible up to the very near-infrared (600-950 nm) the absorption in Ge is about 50 times stronger than in Si. That means that even in the visible, Ge is a superior detector material as compared to Si. In the near-infrared (950-1500 nm) the absorption in Si fades out (band edge at 1100 nm) and therefore the absorption in Ge is many orders of magnitude larger. Beyond 1500-1800 nm the absorption of Ge fades out which requires geometries to nevertheless absorb the light (resonant cavity, waveguide detector).

1.1.2 p-i-n photodiodes

A p-i-n photodiode, also called pin photodiode, is a diode with a wide, lightly doped near intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. The p-type and n-type regions are typically heavily doped because they are used for ohmic contacts. Compared with an ordinary pn photodiode, a pin photodiode has a thicker depletion region, which allows a more efficient collection of the carriers and thus a larger quantum efficiency, and also leads to a lower capacitance and thus to higher detection bandwidth. In a pin photodiode most of the photons are absorbed in the intrinsic region, and generated carriers can efficiently contribute to the photocurrent. The pin photodiode does not have any gain, and for some applications this may be a disadvantage. Despite this, it is still the most widely used form of photodiode, finding applications in audio CD players, DVD players as well as computer CD drives. They are also used extensively in optical communication systems.

The pin photodiodes generally operate in reverse-bias in order to deplete the intrinsic region. A high reverse-bias can introduce a noise current which reduces signal to noise ratio, but pin diodes always have better performance for high-bandwidth and high-dynamic range applications than standard pn diodes [9]. Figure 1.5 shows a typical pin photodiode. The illumination window for a pin diode is usually on the p-region because the mobility of electrons is larger than holes and it provides better frequency response. The larger breakdown voltage of pin photodiodes in comparison to the pn diode allows it to be used with a voltage bias of up to 100 V which results in a faster response time in the nanosecond range, depending on the design [10].

For all applications ranging from optical communications to infrared sensing, high sensitivity and low noise are two important properties of pin photodiodes which are enabled by a low dark current of the device. There has been many studies of the dark current for different types of pin photodiodes [11–15]. Basically, the dark current is the combination of three components: (1) diffusion current, (2) generation-recombination current and (3) tunneling current.

Diffusion current, is produced by the thermal generation of electron-hole pairs in the intrinsic region and their diffusion toward the depletion region [6]:

$$I_{diff} \propto e^{-E_g/KT} \tag{1.2}$$

where K is Boltzmann's constant and T is the ambient temperature. From Equation 1.2 it is clear that semiconductors with lower bandgap have higher diffusion. One effective way to reduce the diffusion current is cooling of the device.

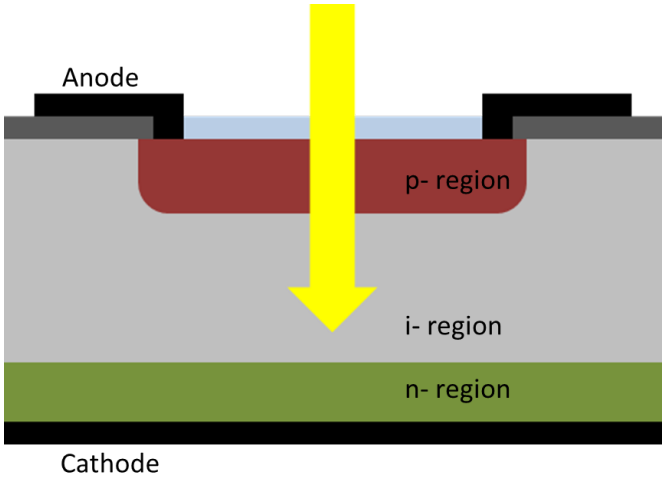


Figure 1.5: Schematic drawing of a pin photodiode. The blue layer is an anti-reflection coating.

Generation-recombination current, is the current produced due to presence of impurity trap levels inside the bandgap of semiconductor. Impurities and defects, form forbidden levels of energy inside the bandgap which induce the generation and recombination of carriers with energy smaller than E_g. This "trap-assisted" current is given by [6]:

$$I_{g-r} \propto We^{-E_g/2KT} \tag{1.3}$$

where W is the width of the depletion region. Equation 1.3, shows that the generation-recombination current is proportional to the depletion width and so it increases with reverse-biasing [16], whereas the diffusion current in Equation 1.2 is bias independent. From this, one can conclude that for semiconductors with bandgaps lower than 1.0 eV the current is dominated by the diffusion current at room temperature.

Tunneling current, is generated when the electric field is so high (e.g. exceeds 10^5 V/cm) that carriers can tunnel through the valence band to the conduction band [16]. Tunneling usually occurs over narrow energy barriers and is given by [6]:

$$I_{tun} \propto EVexp\left(\frac{-\Theta\sqrt{m}}{E}E_g^{3/2}\right) \tag{1.4}$$

where E is the applied electric field, m is the effective mass of electrons and Θ is a constant dependent on the tunneling barrier height. Semiconductors with

lower bandgaps have higher tunneling current. Tunneling is also dependent on the doping of the n- and p-regions while it has a weak dependency on the temperature with only a minor decrease in the breakdown voltage due to increase in E_g. Higher dopings of n- and p-regions results in narrower depletion widths and higher tunneling. In conclusion, the standard pin photodiodes that are fabricated based on semiconductors with low E_g (e.g. Ge and InGaAs) have higher dark current which is basically dominated by diffusion and tunneling currents while in pin photodiodes in high E_g semiconductors (e.g. Si and GaAs) the effect of generation-recombination current is higher and tunneling plays a less important role.

1.1.3 PureB Si photodiodes

As explained in Section 1.1.1, despite the indirect bandgap of Si, it can still be considered as a good photonic material. It is the most common semiconductor in the electronics technology and its compatibility with different industrial needs is always of high significance. Pure dopant deposition of B on Si, also known as "*PureB*" technology that was developed in "Silicon Device Integration" group of Delft University of Technology offers an advance technique to fabricate nanometer-shallow junctions on Si with a damage-free junction [17]. The basic advantage of such diodes is that the photosensitive region of the junction is very ideal and very close to the Si surface and as a result, they are highly applicable in detection of low-energy and low-penetration beams. PureB has been demonstrated in several cutting-edge applications where the integration of high-quality ultrashallow junctions offer a solution to the performance challenges of Si photodetectors. This technology is attractive for a variety of applications: large-area high quality Si diodes, high-linearity varactor diode technology [18], EUV/VUV/DUV photodiodes [19] and low-energy electron photodiodes [20].

At the moment PureB photodiode detectors are being used in EUV wafer-steppers for monitoring the 13.5 nm light entering the alignment system from the source and for effectuating the actual wafer alignment to the mask. These detectors are also a demonstration of flexible integration schemes that have allowed low parasitic resistance and capacitance as well as on-chip combination with other electronic elements. With 2 nm-thick as-deposited PureB-layers as only front-entrance window the photodiode has a responsivity of 0.266 A/W, which is practically that of an ideal lossless system, 0.273 A/W [21]. Moreover, the responsivity degradation is negligible under high-power exposure. Extensive characterization of the PureB photodiodes has also been performed in the whole VUV range, including the deep-ultra-violet (DUV) wavelength of 193 nm that is

in demand for state-of-the-art optical lithography systems. For this wavelength there is a less than 6 nm penetration depth in Si. For VUV photodiodes fabricated with 700°C PureB layers, it has been demonstrated that the very high hole gradient right up to the surface, without roll-off, is very important for securing low leakage currents and high responsivity. This gradient repels electrons from the surface where they would otherwise recombine. Even when the PureB layer is driven-in by thermal annealing at temperatures up to 900°C, a high gradient is maintained up to the surface and, together with the damage-free nature of this doping technique, a high responsivity is maintained [22]. In future, the lithographic wavelength of choice may become 6.8 nm [23]. As shown in Figure 1.6, The PureB photodiodes also display high responsivity at this wavelength as compared to commercial Si detectors [24].

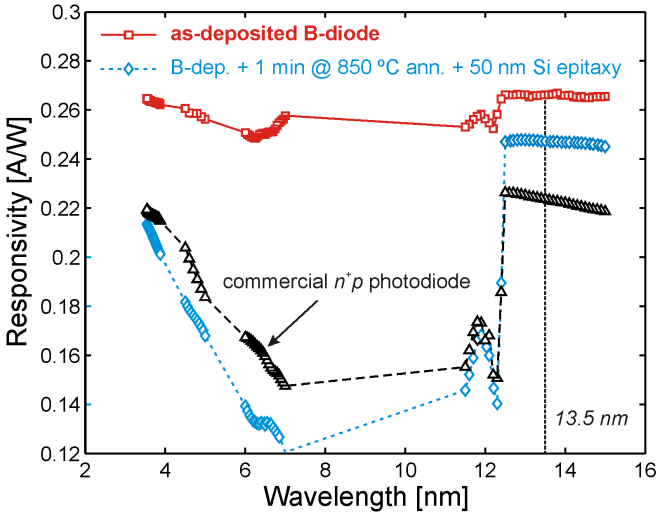


Figure 1.6: Measured EUV spectral responsivity of PureB diodes without and with a 1 min in-situ thermal anneal at 850°C and 30 nm epitaxial B-doped Si growth, compared to a commercial state-of-the-art n^+p photodiode [24].

Another example of the versatility with which the PureB diodes can be integrated in detectors is the low-energy electron detectors developed for SEM imaging. A schematic cross-section of such a detector is shown in Figure 1.7 [20]. The front-entrance window is formed with the photosensitive depletion layer only being covered by a nm-thin p^+-anode under an equally thin PureB layer. This has resulted in a record-high electron-signal-gain for electron energies below 1 keV down to 200 eV [25]. Figure 1.8 compares the performance of a PureB electron

detector with a commercially available back-scattered electron detector (BSE) and a low voltage high contrast detectors (vCDs) [20]. Going to lower deposition temperatures than the 700°C used in the applications up until now, is particularly interesting for increasing the integration flexibility. Below about 450°C it even becomes feasible to add the PureB to a fully processed CMOS wafer. Although equally good diode I-V characteristics have been obtained at temperatures down to 400°C there are more issues to be dealt with than for the 700°C deposition such as higher surface roughness, more pronounced loading effects, higher sheet resistance and probably also higher series resistance because effectively thicker layers must be used. Moreover, the optical responsivity and robustness as well as electrical degradation still need to be characterized.

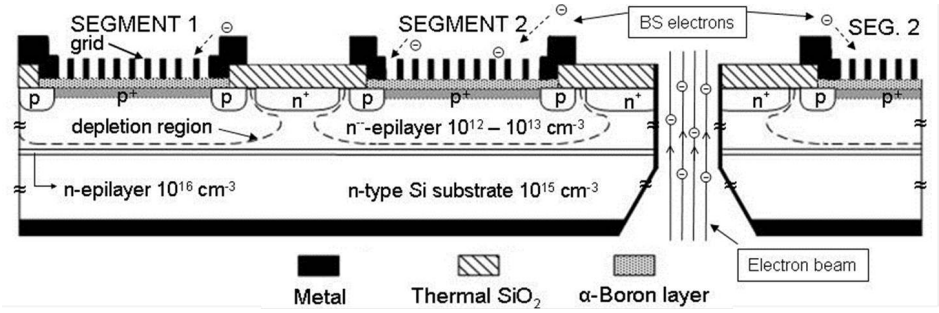


Figure 1.7: Schematic cross-section of two neighboring photodiode segments of a PureB back-scatter detector designed for use in SEM imaging with high scanning speed. A through-wafer hole has been etched to form an aperture for the electron beam. Low capacitance is achieved by depletion of a 40 μm deep n^--type epitaxial layer. To lower the series resistance a fine grid has been etched in Al metallization placed directly on the PureB layer covering the p^+ anode regions. This gives less than 2% loss of responsivity [20].

1.1.4 Avalanche photodiodes

High-speed avalanche photodiodes (APDs) are widely used for many applications such as photon counting, laser pulse detection [26] and fiber-optic communication. In spite of the high operating bias, APDs can be designed for low noise operation [27] and with gain-bandwidth (GB) products in excess of 100 GHz [28–32].

In principle, an APD is a highly sensitive photodiode that exploits the photoelectric effect to convert light to electricity by providing a built-in first stage of

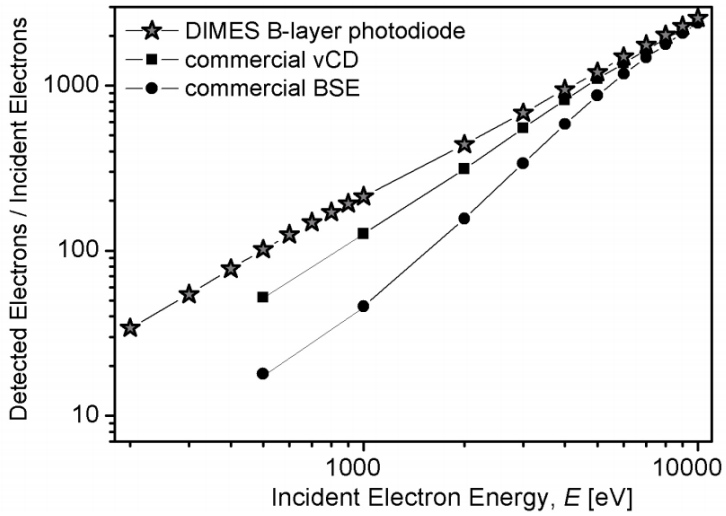


Figure 1.8: Measured electron signal gain for a PureB photodiode, a commercially available BSE detector and a low voltage high contrast detector (vCD) [20].

gain greater than unity through avalanche multiplication. This is obtained through the process of "*impact ionization*" by operating the photodiode at a sufficiently high reverse-bias voltage. The impact ionization process is illustrated in Figure 1.9. Under a localized electric field larger than about 10^5 V/cm [33], electron A gains sufficient kinetic energy to hit an atom in the crystal lattice and knock out an electron-hole pair $B - B'$. Electron A can move out and hit another atom and knock out electron-hole pair $C - C'$, while electron B also gains sufficient energy to hit an atom and produce electron-hole pair $D - D'$ and this process continues as an avalanche action.

In Figure 1.10 the schematic structure is given for operation of a high speed and low noise APD. The electric field in the near intrinsic absorption layer is high enough for carriers to travel at saturated velocities, yet it is below the field where significant avalanching occurs and the tunneling current is negligible. The photo-generated electron-hole pairs then reach the multiplication layer which is thinner and with higher doping. In the multiplication layer, the electric field is high enough to cause impact ionization and hence achieve an avalanche gain that exceeds unity. In heterostructure APDs, the multiplication layer is fabricated with a higher bandgap semiconductor to further increase the electric field.

In ideal APDs, the total dark current I_d is a function of the multiplication

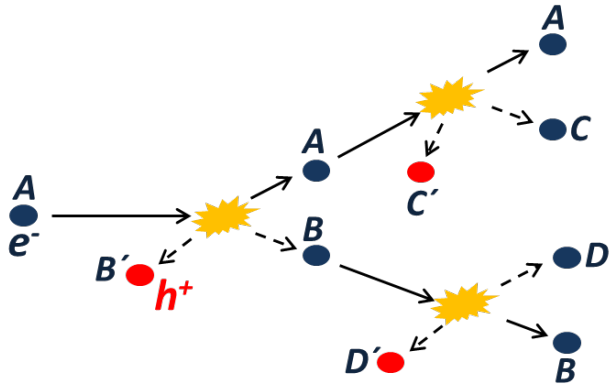


Figure 1.9: Impact ionization process

factor as follows [34]:

$$I_d = I_{dM} \times M + I_{d0} \tag{1.5}$$

where I_{dM} and I_{d0} are, respectively, the multiplied and the unmultiplied dark currents and M is the gain or avalanche multiplication factor. The multiplied dark current comes from the generation of carriers that takes place under the pn junction in the multiplication and transition regions where the electric field is high enough to generate impact ionization. While the unmultiplied dark current comes from the carrier-generations that are taking place at the absorption region, where the electric field is lower.

The gain or avalanche multiplication factor of an APD can be defined as the photocurrent of the diode generated by avalanche action divided by the unity gain photocurrent. At voltage breakdown of the APD, the multiplication factor M tends to infinity. An empirical relation between the multiplication factor M and reverse-bias V is given by [35]:

$$M = \frac{1}{1 - \left(\frac{V}{V_{br}}\right)^n} \tag{1.6}$$

where V is the applied reverse-bias and V_{br} is the breakdown voltage. The factor n is a constant depending on the semiconductor material and the temperature. Typical values for multiplication factors are in the order of at least 100 for Si APDs and 10-40 for Ge or InGaAs APDs [36].

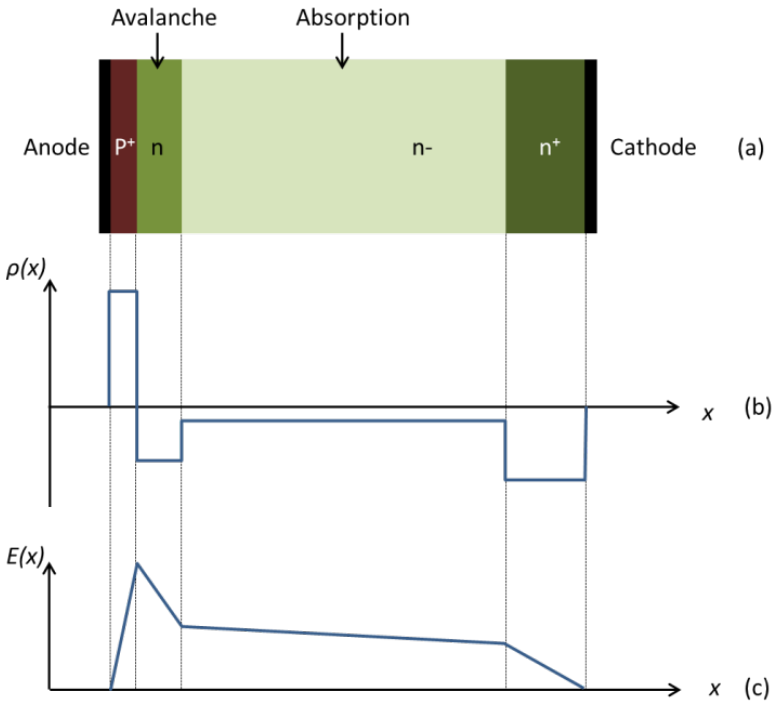


Figure 1.10: a) A schematic illustration of an APD, b) the net space charge density across the photodiode and c) the field across the photodiode and the identification of absorption and multiplication regions

1.1.5 Single photon avalanche photodiodes

Single photon avalanche photodiodes (SPADs) are identified as a class of APDs operating at a reverse-bias in which every single photon hitting the absorption region can generate an electron-hole pair that triggers an avalanche. In this operational mode, also known as *photon counting* mode, the APD is biased just above breakdown voltage where the avalanche multiplication factor is infinite, as a result the APD is able to detect very low intensity signals, in the scale of a single photon. Because the trigger nature of a photon counting APD, is similar to a Geiger-Muller counter of nuclear radiation, this mode of operation is also referred to as Geiger-mode operation [37]. It is important to note that in the photon counting mode when a photon is detected there is a dead-time before the next photon can be detected. For example, if 10^6 photons hit the detector at the same

time, only one pulse will be generated indicating that only 1 photon has been detected. However, if 10^6 photons were available for detection, photon counting would not be necessary, and a linear mode of detection would suffice. In other words, if there are a lot less photons (e.g. 25 photons per second), then photon counting would be required. Figure 1.11 shows the I-V characteristic of a SPAD in reverse-bias.

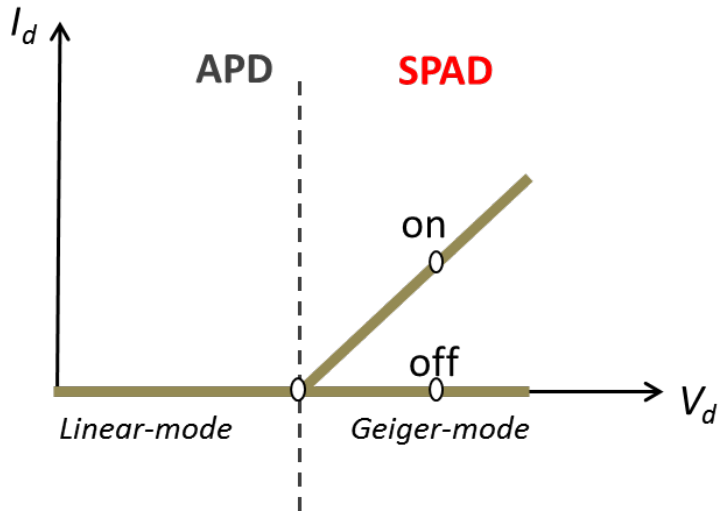


Figure 1.11: I-V characteristic of a photodetector in reverse-bias for APD and SPAD modes

The excess bias voltage V_e is defined as the voltage above breakdown that the detector is operating in Geiger mode:

$$V_e = V_{op} - V_{br} \tag{1.7}$$

At a given temperature, as the excess bias increases the probability of breakdown goes higher. This excess bias voltage causes high electric fields across the depleted region of the photodiode that may cause an avalanche current when the interaction of a photon or a thermal event creates electron-hole pairs. This current is then used to initiate an output pulse to indicate that a photon has been detected. In order to detect the next photon, the avalanche current must be quenched by pulling the SPAD bias voltage below breakdown again, and then resetting it at the excess bias voltage. The time it takes to reset the SPAD to its over-voltage is the *"dead-time"* [38]. Figure 1.12 shows a simple passive quenching circuit.

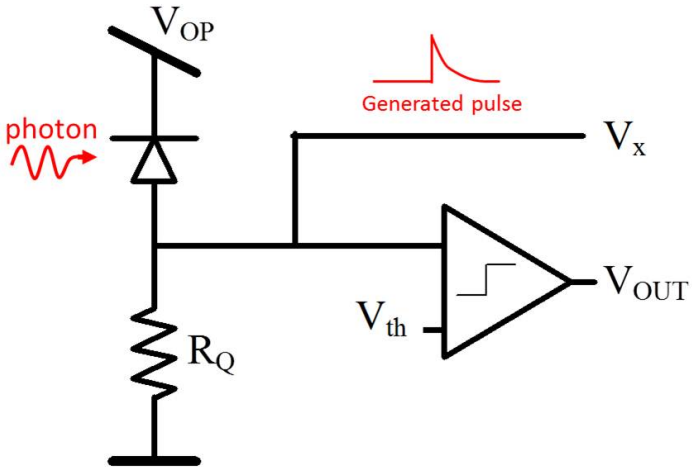


Figure 1.12: SPAD passive quenching circuit

In addition to photon-induced avalanche, thermally-generated carriers (through generation-recombination processes within the semiconductor) can also trigger the avalanche process. Therefore, it is possible to observe output pulses when the SPAD is in complete darkness. The number of these pulses generated in darkness per unit time is known as the dark count rate (DCR). The most fundamental trade-off in the operation of SPADs is between DCR and photon detection efficiency (PDE). Increasing the avalanche probability by operating at larger excess bias increases the probability that both photo-excited and dark carriers generate avalanche; therefore, both PDE and DCR increase. Moreover, if electric field-mediated dark carrier generation is significant at the operating conditions of interest, the DCR will exhibit a faster increase with excess bias than PDE [39, 40].

1.2 Properties of germanium

Germanium is a key material for many applications and it has always been of interest for semiconductor technology. Needless to say that world's first point contact transistor that was demonstrated by Shockley, Bardeen and Brattain in December 23rd, 1947 at Bell laboratories [41], was a Ge slab, into which a plastic wedge pressed two strips of gold foil (Figure 1.13). Recently Ge regained a lot of attention in the semiconductor industry because of its attractive properties

which can lead to solutions for some of the major roadblocks that Si technology is facing in the development of advanced nano-scale electronic devices. Today, Ge is a well-known material for its high mobility, low energy bandgap and for the match of its lattice constant with some of the III-V semiconductors such as GaAs. Ge is widely applied in infrared optoelectronics, as a substrate for epitaxy of III-V multi-junction solar cells, for SiGe alloying in state-of-the-art CMOS technology, in radiation-hard materials for the fabrication of nuclear-radiation detectors, and it is playing a major role in high performance fiber-optic systems. Also the transport properties of Ge are very favorable compared with other semiconductors because of its high hole mobility (Table 1.2). Just like any other semiconductor, most of the interesting properties of Ge stem from point defects and impurities which provide for the local resistivity, the doping type and density. In the following Sections some properties and applications of Ge that were major motivations for the works of this thesis will be described in more detail.

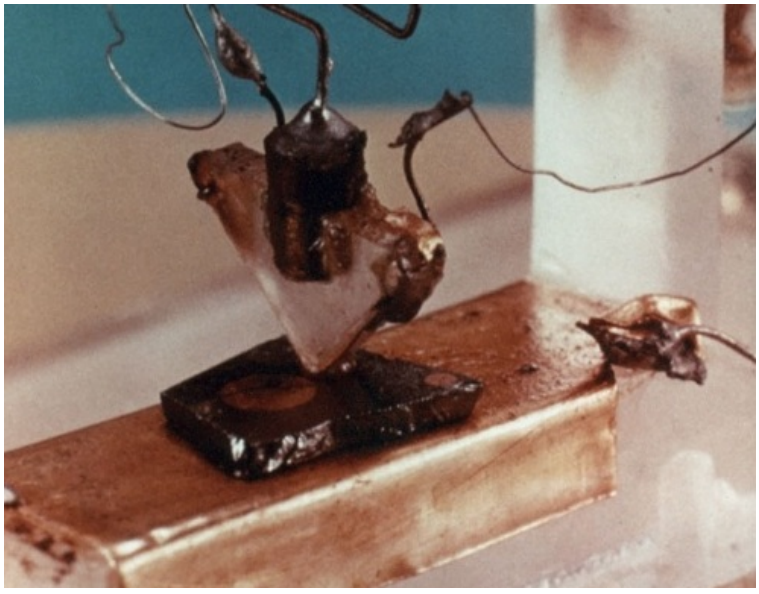


Figure 1.13: The first point contact transistor that was based on Ge (Bell Labs 1947) [41].

Table 1.2: Mobility of Ge, Si and GaAs in $m^2/V-s$

	Ge	**Si**	**GaAs**
Electrons (μ_n)	0.39	0.15	0.85
Holes (μ_p)	0.19	0.045	0.04

1.2.1 Infrared detection

One of the unique properties of Ge is its small bandgap as compared to most other semiconductors. The bandgap of 0.66 eV which corresponds to a cut-off wavelenghts of around 1800 nm makes Ge a very interesting photonic material for infrared applications. High absorption of light with wavelenghts from visible to near-infrared can be achieved if the detector is made of Ge.

For growing Ge on Si there are technological problems such as the lattice mismatch of Ge to Si and the lack of good Ge oxide. Nevertheless, there are plenty research areas on Ge-on-Si detectors, even as photon counters. Highly sensitive Ge detectors in near-infrared can be very interesting for applications such as clear night vision in absolute darkness. Ge photodetectors have also been shown to be operational in the far-infrared light spectrum [42]. The far-infrared part of the spectrum is crucial for the study of many astrophysically important objects.

1.2.2 Dopants in Ge

Doping in Ge- just like in Si- is normally achieved by Group III (p-type) or Group V (n-type) impurities, which are characterized by a high maximum solubility (S_{max}) up to a few times 10^{20} atoms/cm^3 [43]. Such dopants are especially useful as shallow-level dopants. Other impurities like the transition metals have a much lower S_{max} and generally act as generation-recombination centers in the semiconductor, forming deep levels in the bandgap. In other words, metal impurities can be centers of leakage current generation. For these and other reasons, both shallow and deep level impurities in semiconductors have been investigated in the fifties [44, 45]. The maximum equilibrium solubility of the common dopants in Ge and the expected sheet resistance for a diffusion (junction) depth x_j of around 100 nm are summarized in Table 1.3 [3]. This sheet resistance is an important technological parameter, which can be used to determine the suitability of dopants for shallow junction formation in Ge devices. Based on these data, Ga and P are the most promising dopants for Ge. Nevertheless, to better un-

derstand the doping behavior in Ge one has to study the diffusion of Group III (p-type dopants) and Group V (n-type dopants). Self-diffusion in Si and Ge is the slowest process. With respect to impurities, a distinction is made between slow diffusers, which are up to 100 times faster than self-diffusion and fast diffusers, which follow generally an interstitial mechanism. From Figure 1.14 it can be seen that Group III dopants are among the slow diffusers [46], while Group V impurities are typically 100 times faster. In the following, solubility and diffusivity of few famous dopants of Group III and V will be summarized.

Table 1.3: Maximum equilibrium solubility of common dopants in Ge and corresponding calculated sheet resistance for a junction depth indicated in the last column

Dopant element	**Max. solubility (at./cm^3)**	**R$_s$ (Ohm/sq.)**	**x$_j$ (nm)**
B	5.51018	315	140
Ga	4.91020	34	115
P	2.01020	42	92
As	8.11019	79	120
Sb	1.21019	163	100

Boron

B has an equilibrium solubility of around 5×10^{18} atoms/cm^3 at 850°C. Higher activated concentration of impurities up to around 5×10^{20} atoms/cm^3 -as the peak of electrically active concentration- is reported using rapid thermal anneal (RTA) steps [47]. However, recent studies confirm the low diffusivity of B in Ge, both under furnace anneal or RTA. B diffusion usually leaves a long diffusion tail in the profile inside Ge. The observed tail looks very similar to implanted B in Si where it is known that the predominant contribution to the tails is channeling rather than diffusion. However, radiation enhanced diffusion, can not be ruled out [48]. Such diffusion occurs when an ion-implantation is performed at elevated temperatures with an enhancement factor of several orders of magnitude, as compared with a room temperature implantation followed by an anneal at the same temperature. The enhancement is a result of higher than equilibrium concentration of vacancies under the higher temperature conditions.

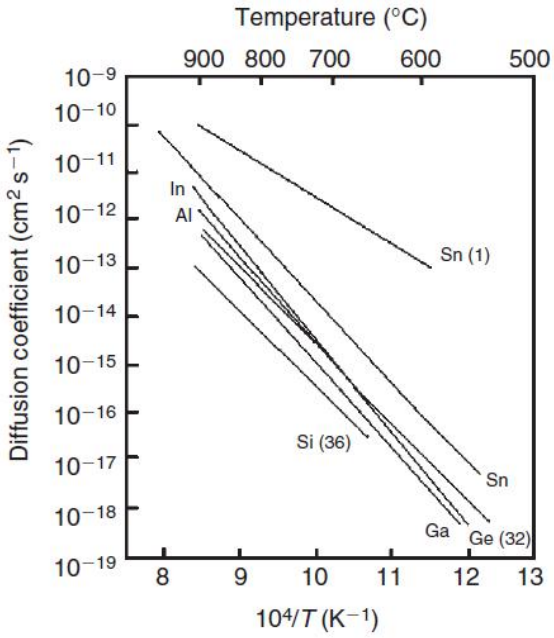


Figure 1.14: Diffusivities of impurities in Ge and Ge self-diffusion [46].

Aluminum

With a high solid solubility of around $4{\times}10^{20}$ atoms/cm^3, Al is known to be a suitable p-type dopant for Ge. Al profiles also suffer from tailing, although no radiation-enhanced diffusion has been noted in this case [49]. Another problem with Al is its strong out-diffusion behavior which makes it critical to avoid reactions with oxygen and formation of Al_2O_3.

Gallium

The maximum solubility of Ga in Ge is around $5{\times}10^{20}$ atoms/cm^3, which is higher than for both Al and B. The diffusion of Ga is slightly smaller than Al [50], however, it still suffers from tailing effect in the doping profile, when the annealing temperature is above 650°C [51]. In general, due to low diffusion coefficient and high solid solubility, Ga seems to be the most promising p-type dopant for formation of pn shallow junctions in Ge.

Arsenic

As has a high solubility of around 10^{20} atoms/cm^3 and therefore seems a suitable candidate for n-type doping. It has been shown that optimal n-type doping electronic performance can be obtained by As. Among P, As and Sb, only As shows up 100% activation at 500°C furnace anneal [52]. Also the tailing problem is less effective when forming the doping profile of As, as compared to other n-type dopants.

Phosphorus

The doping profile of P in Ge shows a tailing problem at annealing temperatures above 550°C, which is a drawback if shallow n^+p junctions are to be fabricated. The other problem with P as an n-type dopant is the out-diffusion during subsequent annealing [52]. A SiO_2 cap layer is usually utilized to prevent this from happening [52]. Diffusion of P in Ge increases significantly at large concentrations above 10^{19} atoms/cm^3.

Antimony

Compared to As, antimony (Sb) has serious disadvantages. It has smaller solubility than As (around 10^{19} atoms/cm^3) and a higher diffusivity than P or As [52] and also a high tendency to out-diffuse. All these make Sb less favorable as an n-type dopant in contrast with As and P.

1.2.3 Ge as III-V epitaxy template

Direct growth of GaAs on Ge can be used for many III-V applications. The lattice mismatch of only 0.07% between Ge and GaAs (see Figure 1.2), allows the epitaxial growth of high quality GaAs on Ge utilizing metal organic chemical vapor deposition (MOCVD) techniques. Ge substrates are highly preferable over GaAs substrates, because of high crystallographic perfection, high mechanical strength and better recyclability. These advantages have led to the major use of Ge as a substrate for GaAs/Ge solar cells for telecommunication satellites [53], as well as other GaAs related devices different from solar cells. Also the integration of Ge PMOS with GaAs NMOS is a very attractive replacement for fast Si CMOS structures [54]. Combining GaAs as a very high electron mobility n-channel with a Ge p-channel on the same Ge substrate would yield very high mobility

structures. Especially Ge-on-Insulator (GOI) wafers[1] in advanced semiconductor technology are of interest, not only to allow III-V integration to mature Si devices but also to provide novelties such as III-V and Ge on Si substrates.

In general, lattice mismatch does not significantly degrade the quality of GaAs/Ge epitaxy; however compound semiconductor growth on an elemental substrate presents a somewhat increased complexity compared to homogeneous growth. Here this is because of the polar nature of GaAs as compared to the non-polar nature of the Ge substrate [56]. Due to the inequivalence of two face-centered-cubic (fcc) sublattices, the zinc-blende crystal structure of GaAs and other III-V compounds possesses lower symmetry than the diamond cubic structure. As a result, when GaAs is nucleated on a Ge substrate, two sublattice orientations are possible, each rotated 90°C. When both GaAs orientations are nucleated on a Ge surface, distinct domains of each sublattice, separated by antiphase boundaries (APBs) may propagate into the GaAs epilayer as illustrated in Figure 1.15 [57]. These boundaries between two different antiphase domains consist of electrically very active Ga-Ga and As-As bonds, which act as strong scattering centers and inhibit the free charge carrier flow with high mobility. As a result, any effort to grow device quality GaAs/Ge, must overcome the challenge of antiphase disorder.

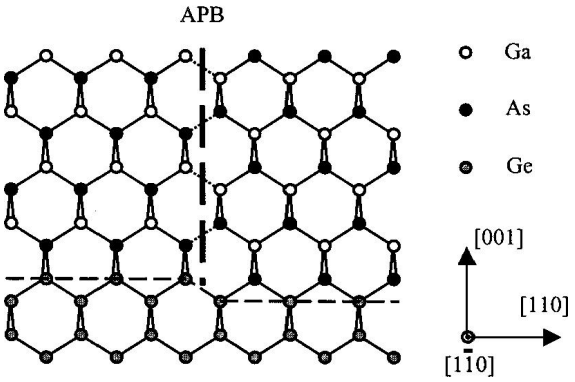


Figure 1.15: A GaAs APB nucleated by the sublattice displacement induced by a single atomic-layer step lying on the (001) Ge surface. The bold dashed line marks the wrong nearest-neighbor bonds lying on the plane of the APB [56].

[1]Germanium-on-insulator wafers are gaining attention as a high mobility material with the on-insulator advantages, potentially an ideal material platform to further boost the transistor performance. Its mechanical stability over fragile and heavy Ge bulk substrates is another practical advantage for processing in the current Si device lines [55].

1.3 Outline of this thesis

The work presented in this thesis is focused on technological development of a CVD system (ASMI Epsilon 2000) from depositions in groups III, IV and V of the periodic table. The main motivation for this research is to merge alternative semiconductors with standard Si technology. Such techniques are advantageous when special properties of a specific semiconductor is needed together with routine IC technologies such as CMOS. The goal here is to introduce methods that are applicable in electronics/photonics industry for fabrication of different high-quality photodetectors on Si substrates.

In the Introduction Chapter, firstly, the important properties and applications of different photonic materials are reviewed and important types of photodetectors as well as some basic theoretical explanations are delivered. In the second part, the focus is put on Ge, which is playing the most important role in this work. The properties and applications of Ge are discussed in details. The knowledge delivered in this part is highly useful throughout this thesis.

In Chapter 2, epitaxial growth of GaAs by CVD system is characterized. The ASMI Epsilon 2000 CVD reactor which was firstly a standard system for epitaxial growth of Si and SiGe is introduced in this Chapter. The reactor is further modified with extension of a TMGa bubbler system for deposition of GaAs. It is shown in this Chapter that this CVD reactor is applicable both for Si/SiGe and GaAs processing. The characterizations over epitaxial growth of intrinsic, Si-doped and Ge-doped GaAs is delivered in this Chapter.

Chapter 3, introduces a strong and applicable method to selectively grow crystalline Ge on Si substrates. Different characterizations are given over the quality, selectivity and uniformity of this method. It is shown that the quality of the grown Ge on Si is good enough for fabrication of high-quality electronic devices.

In Chapter 4, pure dopant deposition of pure boron (PureB) and pure gallium (PureGa) on Si substrates is studied. It is shown that both methods are highly useful in fabrication of advance pure dopant p^+n diodes on Si. Such diodes, with ultrashallow junctions and good-quality interface are proven highly useful in detection of low power and low penetration photonic signals. Both PureB and PureGa types of diodes are characterized in this Chapter and their exceptionally good electrical characteristics are presented.

In Chapter 5, the crystalline germanium growth technique of Chapter 3 and PureB/PureGa technologies of Chapter 4 were merged together to introduce a novel technique for fabrication of Si based ultrashallow Ge diodes. The idea is to first grow crystalline Ge selectively on Si substrates and then implement the pure

dopant junction by depositing both PureB and PureGa technologies. The term PureGaB is introduced in this Chapter for this method to create Ge ultrashallow junctions. It is shown that such Ge diodes can be used as high-quality photodetectors that works in infrared range of light spectrum. Ge single photon detectors are fabricated and a summary of their characterization is given in this Chapter.

Chapter 6 summerizes the main conclusions of this thesis and provides a number of recommendations for future work.

Chapter 2

Gallium arsenide epitaxial growth

For the experimental research in this thesis, a commercial Chemical Vapor Deposition (CVD) system, the ASMI Epsilon 2000 designed for Si and SiGe epitaxy, has, for the first time, been equipped for chemical vapor deposition of Ga compounds in a manner that does not exclude the use of the system also for Si-based depositions. With the new system, GaAs epitaxy has been achieved on GaAs substrate wafers by the decomposition of trimethylgallium (TMGa) and arsine (AsH_3) in the reactor at reduced pressure and at a temperature of 600°C. A low AsH_3 concentration, 0.7% in H_2, is used as one of the precursors, which permits the system to be operational with the same standard safety precautions.

In this Chapter, an overview is firstly given of the functions of the conventional Si/SiGe CVD reactor with modifications. Then details and conditions for the growth of high-quality intrinsic, Si-doped and Ge-doped GaAs epitaxy are provided. Finally, some brief experiments with GaAs epitaxy on Si substrates are described.

2.1 Introduction

GaAs is potentially of great importance for many high-speed electronics and optoelectronics devices [58]. It is recognized as a material with a large electron mobility that is suitable for high-speed electronics and with a direct bandgap that is perfectly applicable for fabrication of light emitting diodes (LEDs), laser diodes (LDs), photodetectors and waveguides. Now, GaAs is the basis of several billion dollar worldwide industry for high-frequency, high-speed electronics and

optoelectronics and GaAs epitaxial growth techniques are playing an important role in this industry. The use of such techniques allows more flexibility in the growth and placement of semiconducting layers and dopants than is achieved by other approaches such as bulk crystal growth, ion implantation and diffusion [59].

Metal-organic CVD (MOCVD) and molecular beam epitaxy (MBE) are the two major processes of GaAs epitaxial growth which can meet the extremely stringent material requirements of advanced designs. Both MOCVD and MBE produce high-quality materials with similar purity, mobility, and photoluminescence properties, but MOCVD is more suitable for large-scale production since MBE requires extremely low pressure and has low deposition rates. In addition, MOCVD appears to produce better heterojunction bipolar transistor structures. Nevertheless, MBE still has two advantages: better film-growth control and more abrupt interfaces [60].

In the last few years, different MOCVD methods for epitaxial growth have been developed to such high level that excellent thin GaAs layers can be grown with good quality and growth rate control [61–65]. However, all these methods use reactors that are specially designed for GaAs and other III-V families, and they are not compatible with Si processing. So, the ability of merging standard MOCVD techniques for III-V semiconductors and Si epitaxy in one single reactor is new and could be of great interest for integration of III-V materials and Si devices. For this purpose, a standard commercial Si/SiGe CVD system has been modified to allow the deposition of III-V semiconductors such as GaAs and GaN in addition to the standard Si and SiGe depositions.

2.2 Metal-organic CVD system

MOCVD is a specialized area of CVD techniques. The first reported use of MOCVD was in the 1960s for the deposition of indium phosphide (InP) and indium antimonide (InSb). The early experiments demonstrated that deposition of critical semiconductor materials could be obtained at lower temperature than conventional thermal CVD and that epitaxial growth could be successfully achieved. Metal-organics are compounds in which the atom of an element is bound to one or more carbon atoms of an organic hydrocarbon group. The term metal-organic is used somewhat loosely in CVD terminology, since it includes compounds of elements, such as Si, Ge, As and P that are not considered metallic. To conform to what appears to be a well-established tradition, such non-metal compounds will be included also as metal-organics [60].

The growth chamber of a conventional MOCVD system consists of four

zones: (1) precursor injection, (2) mixing, (3) boundary layer and (4) substrate surface. In the precursor injection zone, the precursor gases - including metal-organics - with the carrier gas are set with the proper flow and injected into the growth chamber or in the main manifold. In the mixing zone, the precursor gases are then mixed in the gas phase. It is important to have a uniform mixture of the gases without creating turbulent flow. If the mixing occurs in the chamber, the precursor gas stream experiences an abrupt change from the small cross-sectional area tubing in the lines to the large cross-sectional area and volume growth chamber during the mixing process. Therefore, mixing the gases in the manifold before injection to the reactor chamber can be advantageous. When the precursor gas stream enters the boundary layer zone, precursors are transferred mainly via diffusion onto the surface. In this zone, homogeneous reactions, such as vapor-phase pyrolysis, can also occur, possibly with a higher efficiency than in the mixing zone due to the higher temperature in this zone. Besides the diffusion of precursors onto the substrate surface, thermal convection can also occur, which can cause premature reactions and result in depleted precursor concentrations near the substrate surface. Such thermal convection-driven effects need to be minimized by careful reactor chamber design. On the substrate surface (the last zone) where surface reaction kinetics are important, the adsorption of pyrolyzed precursors, surface diffusion of atoms, chemical reactions and desorption of products occur to complete the crystal growth process [66].

The epitaxial growth procedure that is described here is carried out in the ASMI Epsilon 2000 CVD system, mainly used for the epitaxial growth of Si and SiGe alloys. It is a single-wafer (100 mm) system with a quartz chamber and a rotating graphite susceptor and is equipped with integrated heating lamps to grow layers at temperatures up to 1200°C at atmospheric and reduced pressures. The gas flow in the chamber is laminar, parallel to the surface of the rotating wafer. The schematic diagram of the CVD reactor is shown in Figure 2.1.

The standard precursor gases of the system for different epitaxial growth and doping are listed in Table 2.1. The important extension of the system is a trimethylgallium [$(CH_3)_3Ga$, TMGa] bubbler and an extra gas line to allow the MOCVD of Ga as well as III-V semiconductor compounds such as GaAs and GaN in addition to the standard Si and SiGe CVD. H_2 carrier gas is bubbled through the TMGa and the ratio of process and carrier gas is sensed and controlled by a state-of-the-art Lorex Piezocon binary gas concentration sensor. The system is also equipped with dilution setups which consist of additional mass flow controllers to further dilute the gas concentrations of the dopant precursor gases up to 20,000 times with H_2 gas.

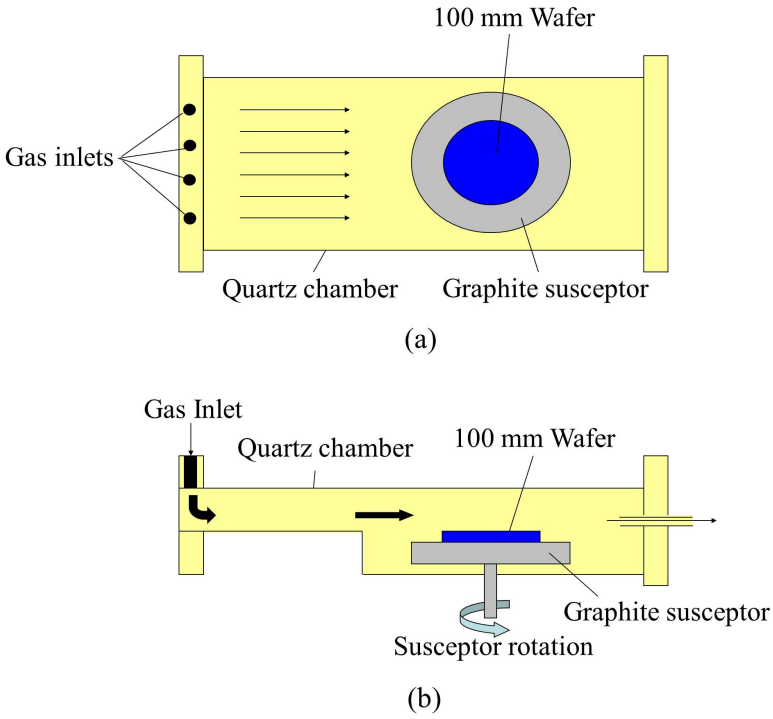


Figure 2.1: A schematic diagram of the (a) top view and (b) side view of the CVD reactor.

2.3 GaAs epitaxy

The precursor gases used for MOCVD of GaAs epitaxy in this research are TMGa and AsH_3. These two gases are known as the most popular precursor gases for GaAs epitaxial growth with MOCVD [60]. The chemical reaction during the growth of intrinsic GaAs is:

$$(CH_3)_3Ga + AsH_3 \rightarrow GaAs + 3CH_4 \tag{2.1}$$

The crystal quality of the GaAs layers was anaylized by differential interference contrast microscopy (DIC). From this analysis, it appears that defect-free epitaxial GaAs on GaAs substrates is achieved. Also Si and Ge doping profiles of the GaAs during epitaxy are attainable by using the methylsilane (CH_3SiH_3) and germane (GeH_4) gas lines that are already standard accessories of the MOCVD equipment. In this Section, the general description is given of the conditions for

Table 2.1: Precursor gases of the ASMI Epsilon 2000 CVD system with their molecular formulas, concentrations and deposition material.

Precursor	Molecular formula	Concentration	Deposition
dichlorosilane	SiH_2Cl_2	100%	Si
germane	GeH_4	2%	Ge
diborane	B_2H_6	0.02%	B
phosphine	PH_3	0.5%	P
arsine	AsH_3	0.7%	As
methylsilane	SiH_3CH_3	0.2%	C/Si
TMGa bubbler	$(CH_3)_3Ga/H_2$	-	Ga

growing intrinsic, Si-doped and Ge-doped GaAs and the characterization of these layers.

2.3.1 Characterization

For the GaAs epitaxial growth here, a low AsH_3 concentration is applied: 0.7% as compared to the at least ten times higher values normally used in MOCVD equipment. This has the advantage that the severe safety precautions usually associated with MOCVD systems need not be implemented. The obvious effect of using a very low AsH_3 concentration is the correspondingly low growth rate. Nevertheless, GaAs growth rates of 0.5 to 5 nm/min have been achieved, with the growth rate increasing as the TMGa and AsH_3 concentrations are increased. Such values are acceptable for many of today's device applications for which layers in the 100 nm range are required.

GaAs epitaxial growth on GaAs substrates is performed at a pressure of 107 mbar (80 Torr) and at a temperature of 650°C. First, a baking step at 650°C is carried out in H_2 ambient for 4 minutes in order to remove the native oxide. Then the mixture of the TMGa and AsH_3 from the main manifold is injected into the chamber with AsH_3/TMGa ratios from 20 to 40 in the gas phase.

In order to make the ASMI Epsilon 2000 CVD reactor applicable for both GaAs- and Si-related processes, after several GaAs growth cycles, the system can be cleaned by performing a few HCl cleaning steps[1]. Si epitaxy with dopant

[1]Each HCl cleaning step is performed by first depositing a thin Si layer on the susceptor using SiH_2Cl_2 as precursor gas and then introducing HCl gas to the reactor chamber at 1050°C for 20 seconds to etch the coatings on the sidewalls as well as the deposited Si layer.

concentrations as low as 10^{15} atoms/cm^3, is then possible to be grown. An example of a situation where the ability to grow Si and GaAs layers in the same system can be of advantage, is the growth of GaAs on Si substrates by using an intermediate Ge or SiGe buffer layers. Since the wafers can remain in the same reactor during the SiGe/GaAs growth sequence, there is no need for cleaning steps in between the two layers to remove the native oxide.

The AsH_3/TMGa ratio was found not to be very critical. Figure 2.2 shows the plots from typical SIMS analysis carried out on GaAs epitaxial layers on GaAs substrates. The layers have been deposited with different AsH_3/TMGa ratios. Ratios of 20, 30 and 40 have been investigated which proves that values from 20 - 40 in the gas phase all gives stoichiometric GaAs growth. However, different ratios still result in different growth rates. In all samples, a Ge marker has been used before commencing the GaAs growth so that the interface between the substrate and the epitaxial layer is accurately monitored by the SIMS. For this reason, In the beginning of each layer growth process, a 2-second pulse of low flow GeH_4 is introduced together with GaAs precursor gases which forms a delta doping in the GaAs epitaxy at the interfaces.

An experiment in which the AsH_3 and TMGa concentrations were varied while the AsH_3/TMGa ratio was kept constant is shown in Figure 2.3. Three layers were grown consecutively. A Ge marker indicates where a decrease in concentration is implemented as going towards the surface. The first layer with the highest gas flows has a growth rate of 5 nm/min; the second and third layers have rates of 3 nm/min and 0.5 nm/min respectively. The AsH_3/TMGa ratio was set to be 30 and the stoichiometry of Ga and As, as shown in Figure 2.3, is still perfect for all three cases with different gas flows and growth rates.

2.3.2 Doping profiles

For doping in GaAs, two possibilities are available in the ASMI Epsilon 2000 reactor: Si and Ge. They both are well-known n-type impurities for GaAs. Their incorporation in GaAs when epitaxial growth is mainly based on replacing Ga atoms in the lattice, which leads to n-type doping in GaAs [67, 68]. Both Si and Ge-doped GaAs epitaxial layers have been achieved in this research, using 0.1% CH_3SiH_3 and 2% GeH_4 gases respectively, in addition to the main GaAs precursors. The lines for these two gases are part of the standard equipment of the reactor.

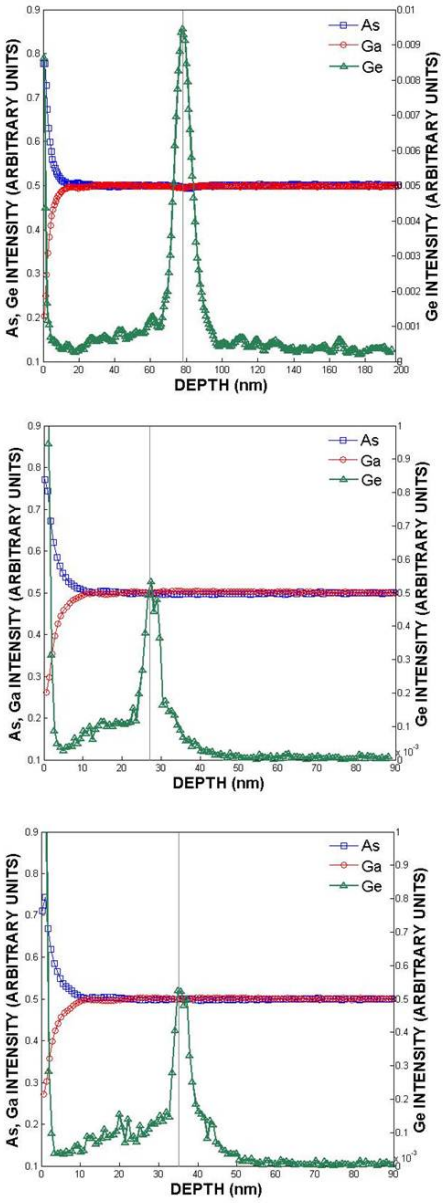


Figure 2.2: SIMS plots for GaAs epitaxial growth with AsH_3/TMGa ratios of (a) 20, (b) 30 and (c) 40 in the gas phase with perfect stoichiometry at a temperature of 650°C.

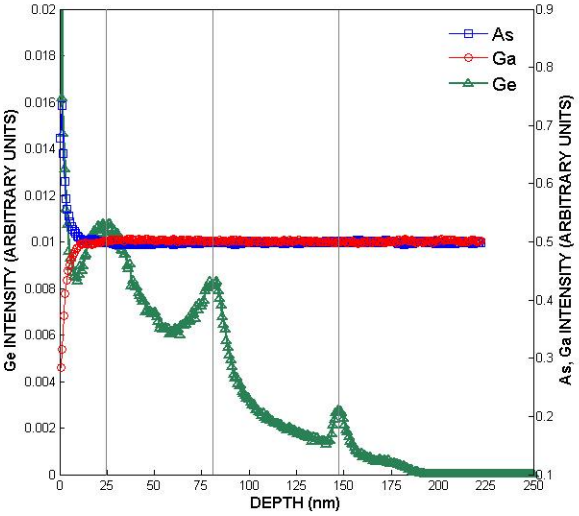


Figure 2.3: SIMS profile of three intrinsic GaAs epitaxial layers at a temperature of 650°C with growth rates of 5, 3 and 0.5 nm/min, respectively. The Ge markers have been introduced for the determination of interfaces between layers. The same concentration of As and Ga indicating good stoichiometry in the deposited layers.

Si-doped GaAs

Figure 2.4 shows a SIMS profile of a 100 nm Si-doped GaAs epitaxy with a dopant concentration of 2 $\times 10^{19}$ atoms/cm^3. It is interesting to note that the carbon (C) concentration in the GaAs epitaxy is lower than that of the substrate, in spite of the fact that methylsilane decomposition results in an introduction of the same amount of Si and C. Consequently methylsilane can be considered to be a good alternative for silane (SiH_4), the standard dopant precursor for Si-doped GaAs epitaxy.

The Si spike at the interface in this and other SIMS plots is most probably caused by the coating of the susceptor: before loading the GaAs wafer, a thin Si coating is applied on the susceptor[1]. It is possible that this coating causes a Si spike at the interface. The C spike, visible in some of the SIMS plots, is most probably due to insufficient cleaning of the surface before the deposition starts.

[1] Si coating on the susceptor is part of the standard HCl cleaning step before each deposition.

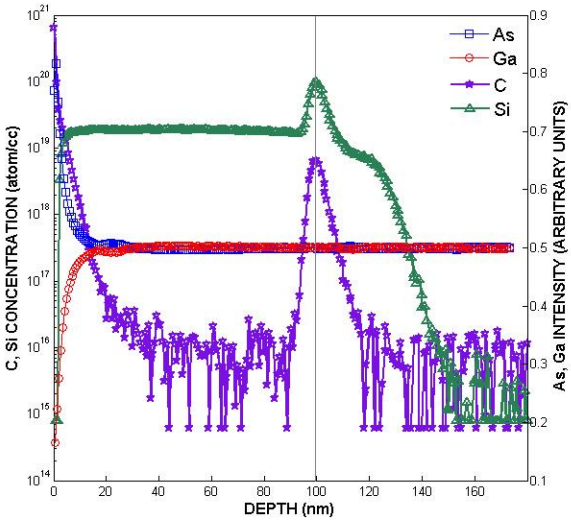


Figure 2.4: SIMS profile of a 2 $\times 10^{19}$ atoms/cm^3 Si-doping in a stoichiometric GaAs epitaxy at a temperature of 650°C.

Using the reactor's dilution system, the concentration of the impurity precursors can be reduced, giving rise to dopant concentration control over several orders of magnitude. This is illustrated in Figure 2.5, which shows a staircase doping profile of three Si-doped GaAs epitaxial layers with average levels of 8×10^{19} atoms/cm^3, 1×10^{19} atoms/cm^3 and 5×10^{17}, respectively. However, the doping profile at the layer interfaces is not abrupt. This is because of the rather high diffusion coefficients of Si in GaAs above 600°C. As is clearly visible, considerable diffusion has taken place. Not only are the changes in concentration far from abrupt, but also the Si has diffused past the original interface into the substrate.

Ge-doped GaAs

Very high Ge-doped GaAs epitaxial layers with a uniform dopant concentration of 10^{22} atoms/cm^3 have been obtained, as shown in Figure 2.6, while the stoichiometry of GaAs epitaxy is still ideal. At this high concentration, well over 20%, the Ga and As concentrations still seem to be equal, within the SIMS accuracy. Hence, Ga and As are approximately equally replaced by Ge in this high concentration regime. On the other hand, using the reactor's dilution system,

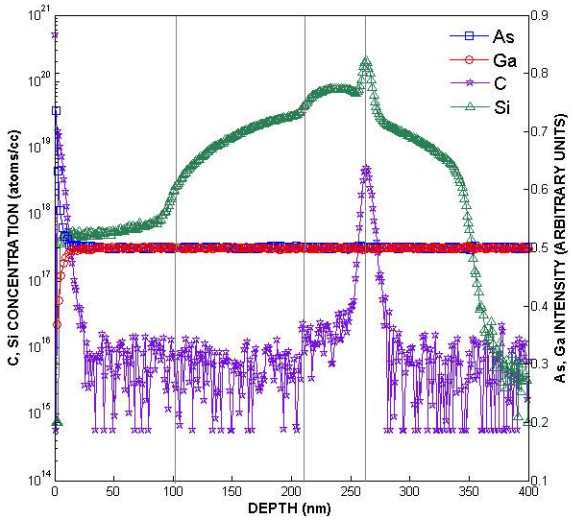


Figure 2.5: SIMS plots for Si-doped staircase GaAs epitaxial layers at a temperature of 650°C with average levels of 8×10^{19} atoms/cm^3, 1×10^{19} atoms/cm^3 and 5×10^{17}, respectively.

achieving lower Ge concentrations are also possible. Figure 2.7 shows the profile for three Ge doping levels with averages of approximately 1×10^{19}, 5×10^{19} and 5×10^{20} atoms/cm^3, respectively. It is also clear from Figure 2.7 that Ge - just like Si- suffer from high diffusion in GaAs at temperatures above 600°C. It is also clear that the deeper layers have suffered more from diffusion as they have been exposed to a higher temperature budget.

2.4 GaAs on Si substrates

Due to the lattice mismatch of around 4.2% between GaAs and Si crystals, GaAs growth on Si is a big challenge and the compound nature of GaAs makes it further critical for crystalline growth on the Si substrate. In order to study the selective MOCVD of GaAs on Si, first 700 nm LPCVD SiO_2 was deposited at a temperature of 700°C on 100 mm n- or p-type Si wafers. The SiO_2 is patterned to open windows to Si with different sizes afterwards. The patterned wafers are then loaded in the MOCVD reactor for GaAs deposition after they are dip-etched in HF for 4 minutes and dried with Marangoni. The conditions used for GaAs

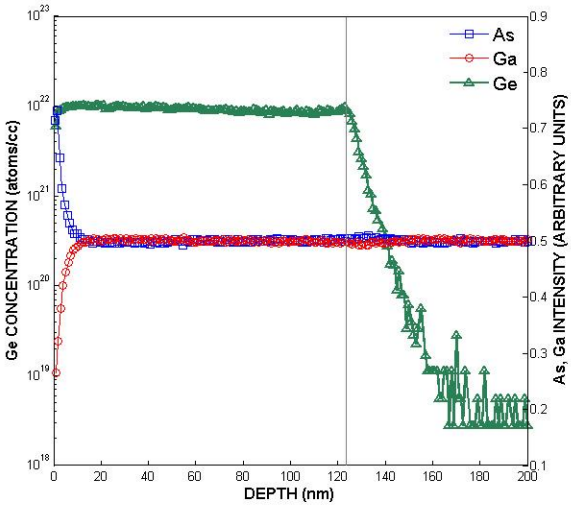


Figure 2.6: SIMS profile of a Ge doped GaAs epitaxial layer. At this high concentration Ge tends to replace Ga and As equally, at least within the accuracy of the measurement.

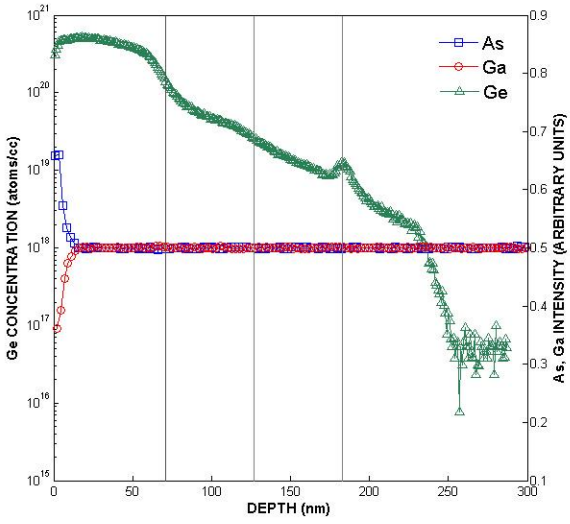


Figure 2.7: SIMS plots for Ge-doped staircase GaAs epitaxial layers with averages of 1×10^{19}, 5×10^{19} and 5×10^{20} atoms/cm^3, respectively.

growth on Si here is the same as described in Section 2.3.1 except for the baking step which is 4 minutes at 850°C to ensure a native-oxide-free Si surface. Figure 2.8 shows secondary electron microscopy (SEM) pictures of GaAs growth on Si. Early results show rather rough surfaces of GaAs that is more like a poly crystal, even though good selectivity over SiO_2 is observed.

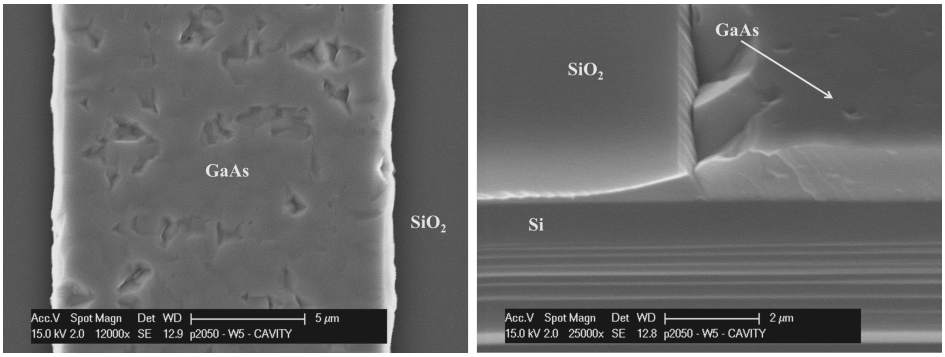


Figure 2.8: top-view (left) and cross-sectional view (right) SEM images of selective GaAs growth on Si.

To better understand the quality of GaAs growth on Si, cross-sectional transmission electron-microscopy (TEM) is performed on a selective MOCVD of GaAs-on-Si with lateral overgrowth on SiO_2 as shown in Figure 2.9.

The GaAs layer thickness in Figure 2.9 is more than 5 μm and as can be seen the further the GaAs growth is from the Si interface, less defects are observed. On the other hand, the lateral overgrowth of GaAs on SiO_2 is reasonably good and as the TEM image shows. No additional defects are produced in the area where GaAs overgrowth from either sides of SiO_2 joins to each other. However, the amount of defects in the body of GaAs, especially at thicknesses of less than 1 μm, is still considerably high for any electronics and optoelectronics application. In Section 1.2.3, it was mentioned that Ge is a good candidate for a sacrificial layer between the Si substrate and GaAs to achieve better crystallinity. This is the motivation of an approach to crystalline Ge growth on Si which is the topic of the next Chapter.

2.5 Conclusions

In this Chapter the MOCVD of GaAs epitaxy in a commercial Si/SiGe CVD reactor (ASMI Epsilon 2000) has been reported. The demonstration of this process

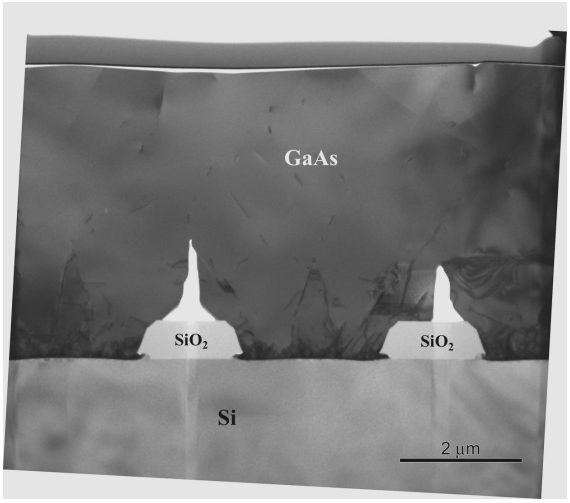


Figure 2.9: A cross-sectional TEM image of GaAs growth on Si substrate with lateral overgrowth on SiO_2.

is in a manner that is compatible with the standard Si/SiGe epitaxy. Based on DIC microscopy and SIMS analysises it appears that good quality and stoichiometric GaAs is obtained for a wide range of deposition parameters and at useful growth rates. The background doping level of the reactor can quickly be returned to the range that is compatible with Si processing with standard cleaning methods. Moreover, doping with Si or Ge is readily obtained from standard gas sources.

Selective GaAs growth on Si substrate is also studied. The early results show good selectivity for GaAs growth and rather smooth layers of GaAs on Si is achieved.

Chapter 3

Crystalline germanium growth on silicon

In the previous Chapters, a description was given over the standard Si/SiGe ASMI Epsilon 2000 reactor that was modified for CVD of both GaAs and Si epitaxy in one system. The conditions and mechanisms to achieve intrinsic and doped GaAs epitaxy was explained in detail and the challenges of GaAs epitaxial growth on Si substrates were described: the challenge related to the lattice-mismatch can be overcome by replacing the Si substrate with Ge according to the lattice-mismatch of only 0.07% between Ge and GaAs.

In this Chapter, the focus is on the utilization of the ASMI Epsilon 2000 system to develop crystalline Ge growth on Si substrates (Ge-on-Si) with low threading dislocation and defect densities. For this purpose, a novel method to grow good quality crystalline Ge within a layer thickness of approximately 1 μm on different window sizes up to hundreds of μm^2 is introduced. A 2% diluted GeH_4 gas is used as the main precursor gas for Ge growth; and AsH_3 and B_2H_6 precursor gases for As and B doping, respectively. Plan-view and cross-sectional transmission electron-microscopy (TEM) and atomic-force microscopy (AFM) analyses were performed on Ge-on-Si to confirm the quality and selectivity of the process as well as the crystallinity of the Ge-on-Si.

3.1 Introduction

At present, single-crystals of Ge grown by the Czochralski technique provide the closest to perfect material. However, the desire to merge Ge with Si to lower the price and for better compatibility with Si CMOS technology has led to development of a variety of techniques to grow crystalline Ge on Si substrates [69–71]. For this purpose, many studies have aimed at overcoming the lattice-mismatch of 4.2% between Ge and Si and some reports of good quality Ge-on-Si have appeared for approaches such as those using SiGe buffer layers [72, 73], lateral overgrowth [74] and aspect ratio trapping (ART) by growth in high aspect ratio trenches [75, 76]. However, Ge epitaxial growth on SiGe buffer layers that can be as thick as a micron or so, still results in some degree of dislocations degrading the quality of the Ge [77], and the lateral overgrowth and ART techniques developed up until now are dependent on critical nano-scale patterning and selective growth over window sizes in the 100 nm range.

In contrast, the method presented in this Chapter uses a CVD technique for selective growth of Ge-on-Si substrates that results in low defect crystalline Ge in tens of microns large window sizes. With this method most of the defects that are generated due to the lattice-mismatch are localized at the interface and disappear within the first 200 nm of growth. The process is performed in the ASMI Epsilon 2000 CVD reactor for Si/SiGe deposition. Since the system was modified for merging GaAs and Si epitaxies in one reactor (see Chapter 2), the integration of good-quality crystalline intrinsic and doped layers of GaAs on Ge could be accomplished directly after the Ge growth.

The quality of Ge-on-Si is investigated by plan-view and cross-sectional transmission electron-microscopy (TEM) and atomic-force microscopy (AFM), not only of the Ge-islands themselves but also of GaAs deposited on the Ge in the same growth cycle. It is shown that the inter-diffusion of Ge and Si at the interface at a deposition temperature of 700°C leads to a sub-200 nm transition with a low threading dislocation density and crystalline Ge is achieved within a thickness of less than 1 μm. Also lateral overgrowth of Ge over SiO_2 has been studied. With this method, the Ge lateral overgrowth from both sides joins perfectly on top of the SiO_2 without any defect formation at the interface. This is specifically promising for fabrication of Ge-on-insulator wafers with Si as the substrate.

3.2 Experimental procedures and analysis

For deposition of Si and Ge, the ASMI Epsilon 2000 is equipped with SiH_2Cl_2 and GeH_4 gas lines as main precursors. The system is also equipped with: B_2H_6, PH_3, AsH_3 and SiH_3CH_3 gas lines for different dopings, an extension of a TMGa bubbler system to allow the deposition of Ga and GaAs in addition to the standard Si and SiGe depositions, and integrated heating lamps that allow the reactor temperature to set controllably up to 1200°C (see Section 2.2). To study the Ge growth on Si substrates, 100 mm n- or p-type Si wafers were used as the starting material. Experiments were performed with less than 1 μm LPCVD SiO_2 first being deposited on the surface of the wafers at a temperature of 700°C, and the areas where Ge deposition is desired are opened by plasma etching to the Si with soft landing[1]. The deposition is inhibited by any oxide, even few atomic layers of native oxide, and any particle contamination or residues on the surface. Therefore, before loading into the reactor, samples were immersed in a diluted HF (0.55%) solution for 4 min to remove native oxide and H-passivate the surface against native oxide formation. This is followed by Marangoni drying[2], which is an effective substitute for spin rinse drying as the formation of drying spots is avoided. After drying the samples are immediately put in the load-lock of the reactor where they are continuously purged by oxygen-free N_2 gas. As an extra measure to assure an oxygen-free surface, a 4 min H-bake at 850°C was performed before the deposition. Then diluted GeH_4 gas is introduced into the reactor chamber and crystalline Ge is grown by the following reaction:

$$GeH_4 \rightarrow Ge + 2H_2 \tag{3.1}$$

Growth of crystalline Ge-on-Si depends strongly on the growth conditions used. The temperature needs to be high enough to allow the chemical reaction to take place and to allow Ge atoms to arrange in a single crystal manner. Also, in order to get a better quality of Ge-on-Si, low pressure growth is needed. The GeH_4 gas flow concentration can be used to increase the growth rate of the layer. Here, a pressure of 27 mbar (20 Torr) and growth temperatures from 550°C to 700°C were found to render best quality Ge-on-Si with good selectivity.

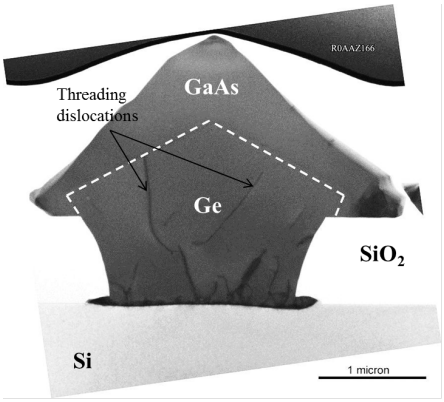
[1] The last 50 nm of the SiO_2 is etched with lower plasma energy to have more control on the etching process and eliminate over etching of the Si substrate.

[2] In Marangoni drying the substrate to be dried is withdrawn from a rinse bath (water) while at the same time N_2 gas with a trace of an organic vapor is led along its surface. The organic vapor dissolves in the water and introduces a surface tension gradient in the wetting film on the substrate, causing the water film to quickly drain backwards into the rinse batch (a Marangoni effect) [78].

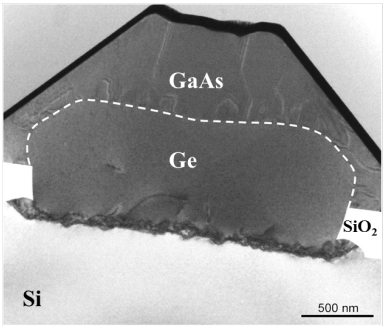
3.2.1 Crystallinity and quality analysis

Due to the inter-diffusion of Ge and Si that occurs at a deposition temperature of 700°C, most of the lattice-mismatch defects are trapped within the first 200 nm of Ge growth and hence, good quality crystalline Ge can be achieved within a layer thickness of approximately 1 µm on window sizes up to hundreds of μm^2.

In order to better investigate the quality of Ge-on-Si and its potential as a template for GaAs epitaxy, in some cases GaAs was deposited after the Ge growth. In Figure 3.1 TEM pictures are shown of Ge growth on a Si substrate with patterned LPCVD SiO_2, at deposition temperatures of 550°C and 700°C and covered with a top layer of GaAs deposited at 650°C. At 700°C a smooth and defect-free surface



(a)



(b)

Figure 3.1: Cross-sectional TEM images of Ge-on-Si growth at temperatures of (a) 550°C and (b) 700°C, followed by in-situ growth of a GaAs layer at a temperature of 650°C, in line-shaped windows with a width of 2 µm.

of Ge is obtained after only growing a thickness of 1 µm. From the TEM, it is also clear that as the deposition temperature is increased, Ge faceting along the [311] planes is reduced and there is rounding off of the final surface of the Ge-island. On the other hand, the facetted surface of the Ge-island grown at 550°C appears to be a better substrate for GaAs growth since the only dislocations observed in the GaAs are a continuation of those seen at the interface with the Ge. At 700°C the Ge is dislocation-free at the interface, but numerous new dislocations are generated by the GaAs deposition. This can be due to some degree of stress built into the Ge at this higher temperature as a result of the increased diffusion of Si into Ge.

The very smooth surface of the Ge grown at 700°C is underlined by the SEM images shown in Figure 3.2 where the growth of Ge in large windows to the Si is illustrated for sizes up to 200×200 µm^2. It is plausible that with the same depo-

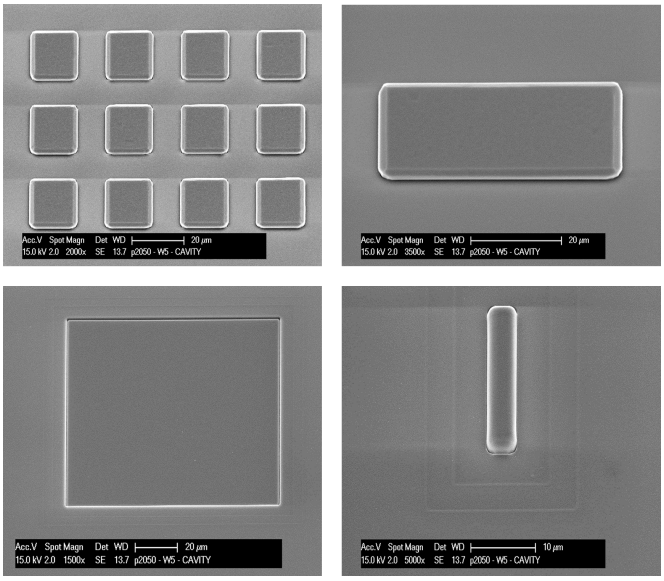


Figure 3.2: SEM images of crystalline Ge grown in large-area windows to Si. the sizes of the windows for Ge growth are: 15×15 µm (top left), 40×20 µm (top right), 100×100 µm (bottom left) and 2×20 µm (bottom right).

sition conditions, different thicknesses are achieved on the different geometries. This phenomenon is caused by surface diffusion of deposited material from the SiO_2 surface to the windows, which is a well-known loading effect. The loading effect generally induces variable deposition rates and epitaxial composition

over the wafer, which are related to variations in surface topography and patterning. As the size of the windows shrink, the influence of surface diffusion on the growth procedure increases and this results in an enhancement of the Ge growth rate.

The smoothness of the Ge grown at 700°C is supported by AFM imaging as shown in Figure 3.3 for the Ge-on-Si growth in window sizes of 30×30 μm^2. The Ge thickness is around 1 µm. A surface roughness of 0.43 nm RMS by AFM indicates a smooth surface of Ge and high quality of the growth. Most of the roughness is observed at the sides of the grown Ge while the center of the surface is considerably smoother.

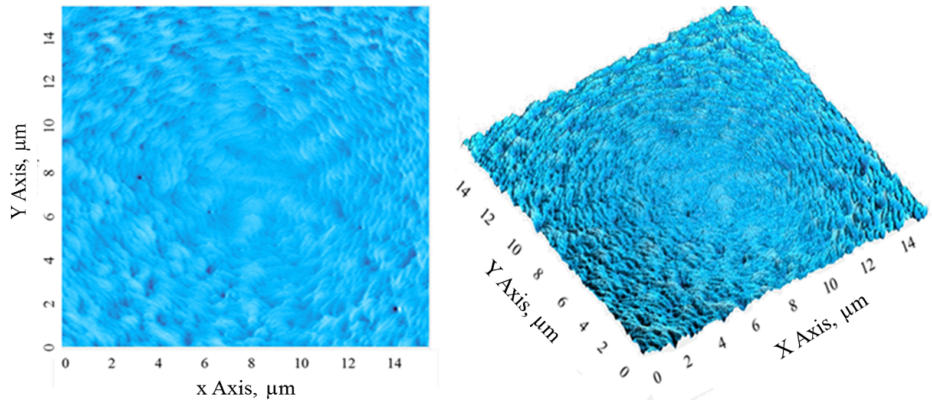


Figure 3.3: AFM (left) and 3D AFM (right) surface scan of a 30×30 μm^2 Ge-island grown on Si. The surface roughness is 0.43 nm RMS and 2 nm peak to peak.

3.2.2 Selectivity

As the growth temperature increases, more Ge nuclei start to form on large SiO_2 areas that are far from deposition windows. While at 550°C, the Ge nuclei formation on SiO_2 is negligible, at 700°C the amount of Ge nuclei may cause problems in further processing the wafers, such as short circuiting the electronic devices. The selectivity, however, can be very well controlled by proper pattern design on SiO_2. Experiments show that the surface diffusion length of Ge on LPCVD SiO_2 surface at the temperature of 700°C is more than 400 µm. This means that if the spacings between desired Ge-on-Si regions are more than 800 µm, the Ge nuclei start to form on SiO_2 surface. Therefore, to avoid nuclei formation and achieve

complete selectivity at 700°C, large size sacrificial regions are designed on the pattern within periodic distances of 800 µm around desired Ge-on-Si regions. The goal of such regions are to accumulate the Ge nuclei and help to keep a clean SiO_2 surface after Ge growth. Figure 3.4.a and b show optical microscopic pictures after selective Ge growth with two different pattern design without and with sacrificial regions, respectively. It is clear from Figure 3.4.b that complete selectivity is achieved while the sacrificial regions gather all the Ge nuclei and this guarantees a clean area around desired Ge-on-Si epitaxy for further processing.

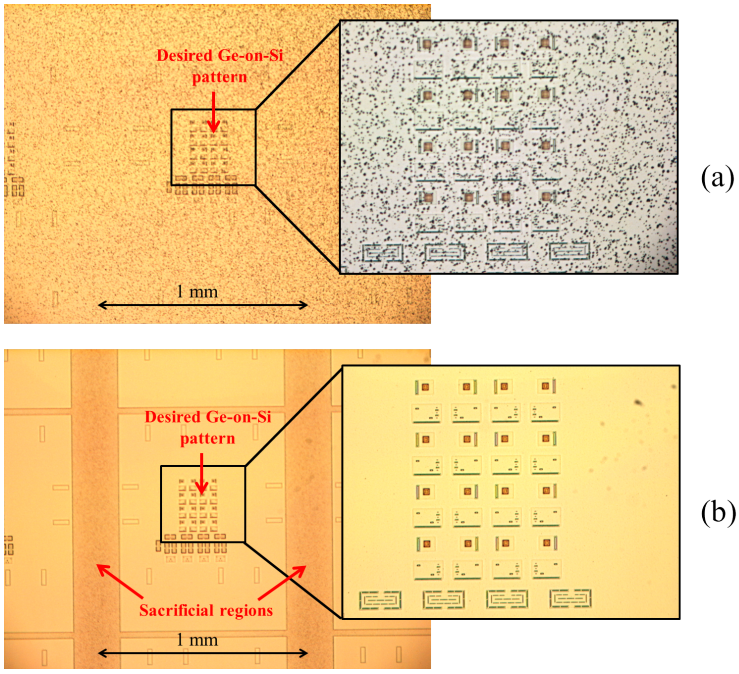
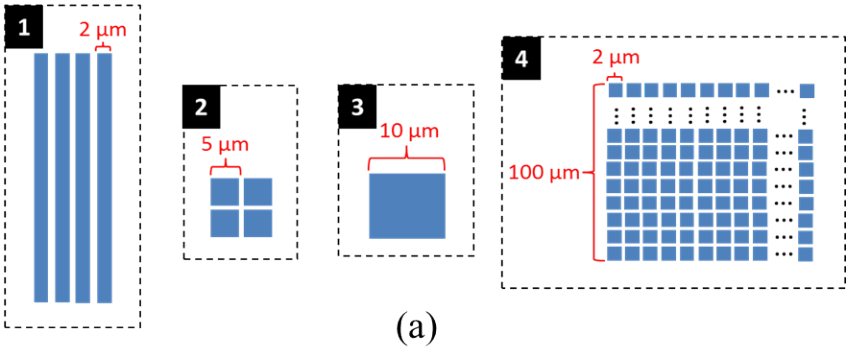


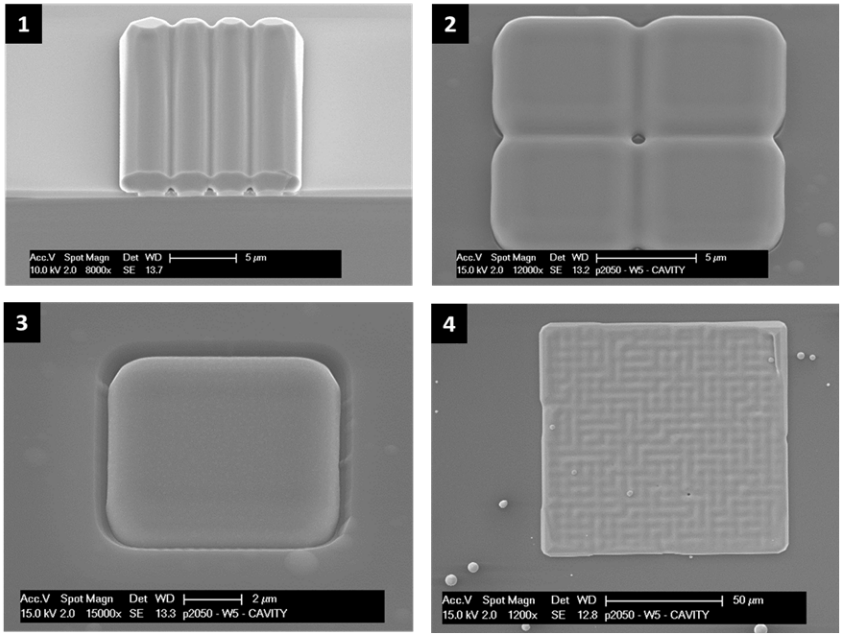
Figure 3.4: top-view optical image of selective Ge-on-Si (a) without and (b) with sacrificial regions. Complete selectivity can be achieved by using periodic sacrificial regions with spacings of 800 µm.

3.2.3 Ge lateral overgrowth

In another study on growth and overgrowth of Ge-on-Si, different patterns were designed in the SiO_2 masking layer. Figure 3.5.a illustrates the schematic top view of four different pattern designs that were studied, while Figure 3.5.b shows the SEM images of selective Ge-on-Si growth in the corresponding patterns at



(a)



(b)

Figure 3.5: (a) Layout of the patterns where Ge was grown on Si and (b) SEM images of the Ge on Si as grown in those patterns. All the spacings between the windows in #1, 3 and 4 are 1 µm.

a growth temperature of 700°C. For simplicity, these four patters are referred as sample #1, 2, 3 and 4, labeled accordingly in Figure 3.5. The spacings between opening windows in #1, 2 and 4 are all 1 µm. From samples #2 and 3 in Figure 3.5, one can observe a very smooth surface of the Ge-on-Si at 700°C even for the large size of 10×10 μm^2 while samples #1, 2 and 4 show that the Ge lateral overgrowth from different sides appears to join perfectly on top of the SiO_2. From Figure 3.5 it is also evident that again due to surface diffusion of the material deposited on SiO_2 surface, for the same deposition conditions different thicknesses are achieved on the different geometries. As a result, the larger open Si areas display a lower growth rate.

Plan-view and cross-sectional TEM imaging was used to get a better picture of the quality of Ge-on-Si with overgrowth and the quantity of threading dislocations. Figure 3.6 shows a plan-view TEM image taken from sample #4. The

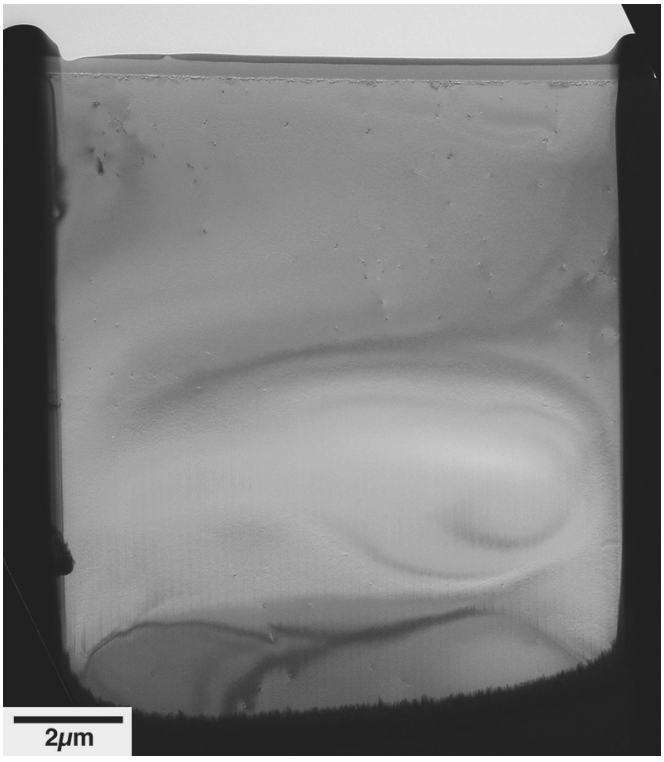


Figure 3.6: Plan-view TEM image of sample #1 with lateral overgrowth of Ge over SiO_2. The threading dislocation was counted to be $10^7 cm^{-2}$.

threading dislocation density was counted to be 10^7 cm^{-2} within an approximately 26 μm^2 large area which is comparable with the state-of-the-art Ge-on-Si growth techniques using aspect ratio trapping (ART) [79] or additional thermal anneal steps [80]. The TEM covers both grown and overgrown areas without any visible interface, while defect density is believed to be higher in the center of the patterns and lower in the overgrown areas. From Figure 3.6 it is confirmed that the overgrowth from different sides can join and cover the SiO_2 without generating defects at the interface.

Another investigation on lateral overgrowth of Ge over SiO_2 is delivered by cross-sectional TEM imaging of sample #1 and shown in Figure 3.7. From Figure 3.7.a, it is once again evident that Ge lateral overgrowth from both sides joins perfectly on top of the SiO_2 without any defect formation at the interface. This is specifically promising for fabrication of Ge-on-Insulator wafers with Si as substrate. In Figure 3.7.b a lattice image of the crystalline Ge after 500 nm of growth on Si is shown.

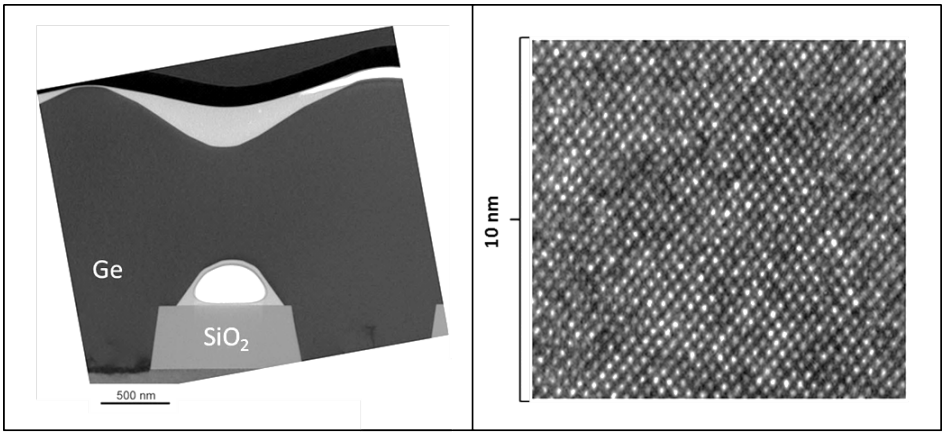


Figure 3.7: (a) Cross-sectional TEM image of selective Ge-on-Si with lateral overgrowth on SiO_2 and (b) a high-resolution TEM image of the Ge crystal at a thickness of 500 nm after growth on Si.

3.3 Doping profiles

To investigate the in-situ As and B doping concentrations in Ge, SIMS analysis was performed. For this purpose, alternating layers of As- and B-doped Ge were grown. The results are shown in Figures 3.8.a and 3.8.b for two samples grown

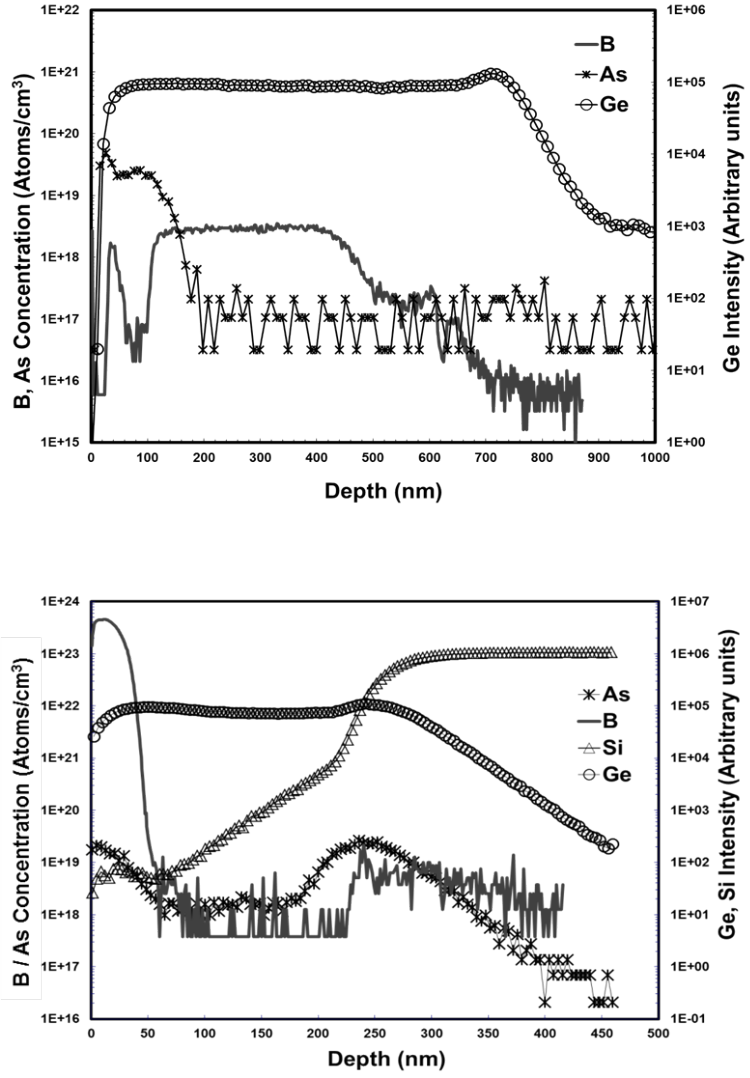


Figure 3.8: SIMS profiles of As- and B-doped Ge-on-Si for deposition temperatures of (a)550°C and (b)700°C.

at 550°C and 700°C, respectively. For n-doping of the Ge during growth, 0.7% AsH_3 is utilized. Taking advantage of the dilution system of the reactor, AsH_3 is further diluted to allow a wider doping range. Due to the solid solubility limit of As in Ge, the maximum n-type doping achieved at both temperatures is not higher than 2×10^{19} atoms/cm^3 (see Section 1.2.2). The background As doping of the reactor for nominal intrinsic Ge growth at both temperatures is below the SIMS level of measurement. At 700°C, As tends to segregate at the surface, giving a rise in As doping density at the Ge surface as compared to the bulk values. Moreover, it is concluded that at 700°C, As doping does not affect the growth rate while it is decreased significantly, depending on the AsH_3 flux, at 550°C. Also the SIMS analysis of the selective Ge-on-Si composition shown in Figure 3.8.b, illustrates that in a region of about 200 nm from the interface there is a substantial inter-diffusion of Si and Ge. This is no doubt the effect that helps to keep the dislocation defects from propagating out of this very limited transition region.

The B doping of Ge is achieved by using B_2H_6 gas. The maximum B doping measured for 550°C growth is 3×10^{18} atoms/cm^3 which is related to the low solid solubility of B in Ge (see Section 1.2.2). The high peak of the B doping profile at the surface of Ge as shown in Figure 3.8.b is a solid B layer that is deposited as a barrier layer; the use of which will be discussed in details in the following Chapters.

3.4 Conclusions

In the ASMI Epsilon 2000 CVD reactor, Ge selective growth on patterned Si substrates was developed with a transition region of less than 200 nm and smooth, flat and defect-free surfaces of Ge were achieved at a deposition temperature of 700°C. At a lower deposition temperature of 550°C, a slightly poorer quality crystal is achieved because the defects grow further into the Ge and the growth is limited along the [311] Ge planes. On the other hand, such facetted structures appear to provide a better substrate for subsequently growing in-situ crystalline GaAs. It is also demonstrated that lateral overgrowth of Ge over SiO_2 can be made to join from different sides without any defects at the interface. This process can particularly be applicable for the fabrication of low defect density Ge-on-Si and/or Ge-on-insulator substrates.

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Chapter 4

Pure dopant deposition for ultrashallow Si junctions

Obtaining an abrupt and accurate doping profile in semiconductor substrates is a challenging process, as the results of diffusion and ion implantation are limited by the thermal processing applied for dopant incorporation and activation. The work presented in this Chapter is the dopant deposition of pure boron (PureB) and pure gallium (PureGa) for fabrication of nanometer-shallow p^+n Si diodes. The PureB technology was already well-developed at the start of this thesis work and it is reviewed here as the basis of the work performed on PureGa. Both dopant types have also played an important role in the development of the Ge-on-Si diodes presented in Chapter 5.

Focus is placed here on the special properties that have put these technologies in a class apart: their attractive electrical behavior together with their electrical, optical and chemical robustness have led to the cutting-edge application as photodiodes for detecting low penetration depth beams, as for example in EUV lithography and low-energy electron SEM imaging (see Section 1.1.3). Of key importance is the effectively large number of impurity charges per unit area, which is expressed by *Gummel number*, of the p^+-region that provides low saturation currents despite the shallowness of the junctions. Based on experimental evidence, it has been proposed that this is related to the formation of a practically complete surface coverage of acceptor states as an interface property of PureB and PureGa on Si surface.

4.1 Introduction

The last half decade has seen a rapid development and adaptation in production of PureB photodiode technology for application in extreme-ultraviolet (EUV) lithography[1] and in Scanning Electron Microscopy (SEM) systems using low-energy (down to 200 eV) electron detection [81]. In this technology, CVD of pure boron (PureB) is used to create the p^+-region of shallow, less than 10 nm deep, silicon p^+n junction diodes. In the first applications, a nanometer-thin amorphous B (PureB) layer is deposited selectively on Si through openings in an oxide isolation layer at a temperature of 700°C. This technology has several attractive properties: the junction formation is damage-free, the PureB layer is chemically robust in many situations, there is a high compatibility with Si IC processing, and the diodes have saturation currents almost as low as that of conventional deep diodes. The fabricated detectors surpassed the performance of other existing technologies on points such as internal/external quantum efficiency, dark current, and degradation of responsivity. For example, for the detection of the above mentioned beams that only penetrate a few nanometers into the Si, 2 nm-thick PureB layers have reliably been implemented as the front-entrance window (see Section 1.1.3).

As a further development of the PureB work, the last couple of years have seen investigations on more low temperature processes, down to 400°C, by using pure gallium (PureGa) depositions. This was made possible again by the availability of the ASMI Epsilon 2000 CVD reactor. As explained in previous Chapters, this reactor was specially equipped for merging GaAs, Si and Ge CVDs all in one system. The main goal has been to develop new processes that would be compatible with CMOS, preferably in a fully-processed form.

In all these PureB/Ga Si diodes, the excellent electrical characteristics can be ascribed to an effectively high Gummel number of the p^+-region. The injection of electrons from the n-region into the p^+-region is suppressed resulting in a low saturation current. This is not seen in other ultrashallow diodes produced by techniques that only aim at damage-free doping of the semiconductor, for example epitaxy of doped Si, or doping from a gas [82]. Therefore the terms PureB/PureGa have been introduced to underline that a solid layer of pure dopant material has been deposited.

[1] PureB photodiodes are applied in the monitoring of the light from the EUV source and for the mask alignment to the wafer in ASML EUV lithography systems.

4.2 Pure dopant vs. conventional pn junctions

In order to understand the special properties and characteristics of the junction formed by the pure dopant deposition of B/Ga on a semiconductor, it is useful to compare three types of diodes: (1) Schottky junction formed by metal deposition directly on a n-type semiconductor, (2) shallow p^+n junction and (3) pure dopant junction formed by deposition of a nanometric pure p^+ dopant layer on a n-type semiconductor. Detailed analysis of the I-V characteristics for these types of diodes, including an analytical model that unifies the standard Schottky and pn diode formulations are explained in [83]. Here an overview is given:

(1) Schottky junction: the diode current is dominated by the injection of the majority carriers (electrons in this case). At the same time, a negligible current of minority carriers (holes) is also injected.

(2) Shallow p^+n junction: the junction depth varies from few nanometers to few tens of nanometers and the maximum doping concentration is defined by the solid solubility of the dopant in the semiconductor. As a result, under reverse and even small forward-bias, the p^+-region can be fully depleted. The current in reverse-bias is then dominated by electron injection and increases toward a Schottky-like level. The Schottky barrier height (SBH) is higher in this case and the total current is much lower than the pure Schottky case and also the hole current is much higher. At a high enough forward-bias voltage where the p^+-region is not fully depleted anymore (depending on the junction depth and doping concentration), the junction behaves like a conventional deep pn junction with higher hole current level comparable to electron current.

(3) Pure dopant junction: the unique feature of the pure dopant deposition from group III on an n-type semiconductor surface is the better ability to tune the current level of the resulting p^+n junction. The nanometric p-type pure dopant layer on the surface of the n-type semiconductor creates a very large amount of holes at the interface that are not readily depleted. Hence, the current is dominated by the injection of holes and the hole current is much higher than for fully-depleted shallow p^+n junction and Schottky junctions. The pure dopant junctions have been found to be ultrashallow with a depth of only few nanometers -depending on the dopant properties and deposition conditions- which, together with the low saturation/dark current, makes them very attractive for optoelectronics applications in detection of ultra-low power signals.

In principle, for a p^+n junction, the Gummel numbers of either n- and p^+-region governs the hole and electron injection into these respective regions. The term, Gummel number can in the simplest approximation be defined as the number of impurity charges per unit area. For a p^+n junction shown in Figure 4.1, it

then follows that:

$$G_n \propto N_D W_n \tag{4.1}$$

and

$$G_{p^+} \propto N_A W_p \tag{4.2}$$

where G_n and G_{p^+} are the Gummel numbers of n- and p^+-regions, respectively, N_D and N_A are the impurity concentration and W_n and W_p are the impurity concentration and the junction width of the n- and p^+-regions as shown in Figure 4.1. By solving the electron and hole current densities according to diffusion theory one can extract the total electron injection current J_n and hole injection current J_p as [84, 85]:

$$J_n \approx -\frac{qn_{i0}^2}{G_{p^+}} \{exp(qV/kT) - 1\} \tag{4.3}$$

and

$$J_p \approx \frac{qn_{i0}^2}{G_n} \{exp(qV/kT) - 1\} \tag{4.4}$$

Both Equations 4.3 and 4.4 show that higher G_{p^+} or G_n, will result in either lower electron current J_n or hole current J_{p^+} respectively.

Different electrical measurements on pure dopant diodes, especially on PureB diodes show Gummel numbers of p^+-region that are even decades higher than Gummel numbers of shallow p^+n diodes that are fabricated by diffusion of B in the n-type Si at a fabrication temperature of 700°C. This effect is due to the interface properties of the pure dopant rather than that of bulk. Such a high Gummel number suppresses the electron injection described by Equation 4.3 to very low values that are comparable with conventional deep p^+n junctions. This is essentially important in reverse-bias where the dominating term of the saturation current is the hole drift current from the n- to p^+-region. The presence of the pure dopant layer reduces the saturation current decades lower than Schottky or bulk-doped ultrashallow p^+n junctions, which is demonstrated experimentally as described in the following Sections.

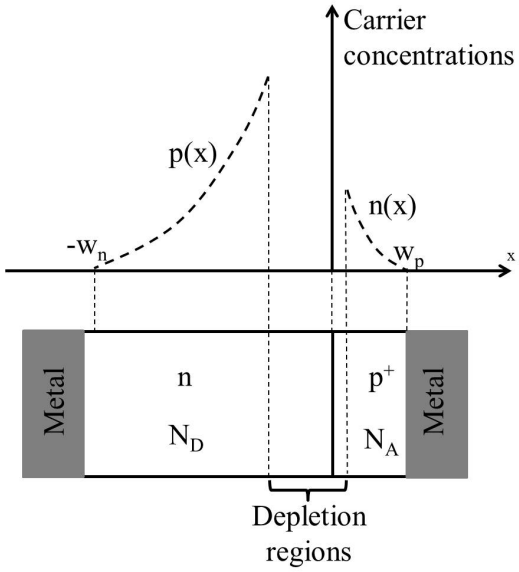

Figure 4.1: Carrier distribution in a p^+n diode with homogeneous doping profile.

4.3 PureB on Si

The details and different applications of PureB technology has already been published extensively and it has in the past been suggested that the bulk properties of the PureB layer should be responsible for the high Gummel number [17, 25, 82, 86–89]. However, the overall experimental evidence that now is available, suggests that it is in fact a property of the interface between the pure dopant layer and the underlying semiconductor. In this Section, an overview for the characterization of PureB technology with the focus on the properties of the interface with Si will be delivered.

4.3.1 Deposition conditions

The basic chemical reaction for PureB deposition with B_2H_6 gas as precursor and H_2 as the carrier gas is as following:

$$B_2H_6 \rightarrow 2B + 3H_2 \tag{4.5}$$

Characterization of PureB Si diodes has been previously performed for a deposition temperature of 700°C and at atmospheric pressure. As it turns out, this

now appears to be the ideal conditions for achieving extremely uniform, reproducible layers. For example, it has been possible to control pattern dependency and loading effects to such a degree that 2 nm-thick layers can be deposited uniformly with less than 1 nm variation in thickness over a 100 mm wafer and roughness of the order of 0.1 nm [88]. The diffusion lengths of the B on both SiO_2 and Si surfaces are found to be in the order of centimeters which means that the loading effect in micron-sized windows will not lead to thicker layers than those deposited in the larger windows. In this respect PureB can also be attractive for use in small dimension devices such as CMOS transistors. For lower deposition temperatures, down to 400°C, investigations have shown that as the temperature decreases the deposition rate and also the mobility of B along the surface decreases. This entails an increase of the surface roughness up to less than 1 nm. As illustrated by Figure 4.2, the deposition rate increases significantly by switching to N_2 as carrier gas but here the much lower concentration of H_2 at the surface lowers the B mobility and also gives a less smooth surface [90].

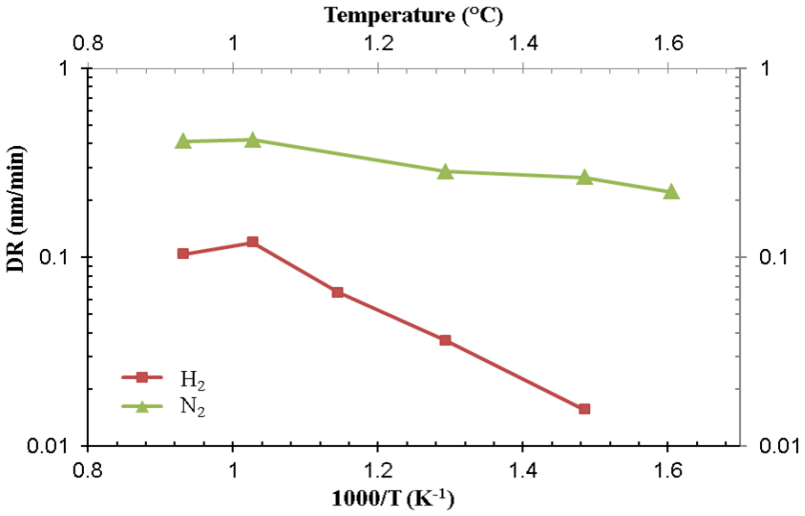

Figure 4.2: Deposition rate (DR) of PureB layers on B-covered Si as a function of temperature for a carrier gas of either H_2 or N_2 [90].

4.3.2 Electrical behavior

Electrical measurements that show the very low saturation current of PureB diodes are displayed in Figures 4.3 and 4.4. From the bipolar measurements it can be

concluded that the electron injection currents are as low as a few 10-20 A/μm^2 which is comparable to those achieved in deep heavily-doped junctions [86]. This corresponds to a Gummel number of the order of 10^{14}-10^{15} atoms/cm^2 for the p^+-region, which is decades higher than what would be expected of nanometer-shallow junctions formed by bulk doping of the Si [83]. In the 700°C PureB diodes the actual doping of the Si substrate is very limited by the low solid solubility and diffusivity of the B and gives a contribution to a Gummel number of about 10^{12} atoms/cm^2, as is documented in [86]. In diodes that are formed solely by such a doping of the Si substrate, the total current would approach Schottky-diode-like values and abnormalities often appear in the I-V characteristics due to depletion of this thin, lightly-doped p-region [91]. From the Figures 4.3 and 4.4

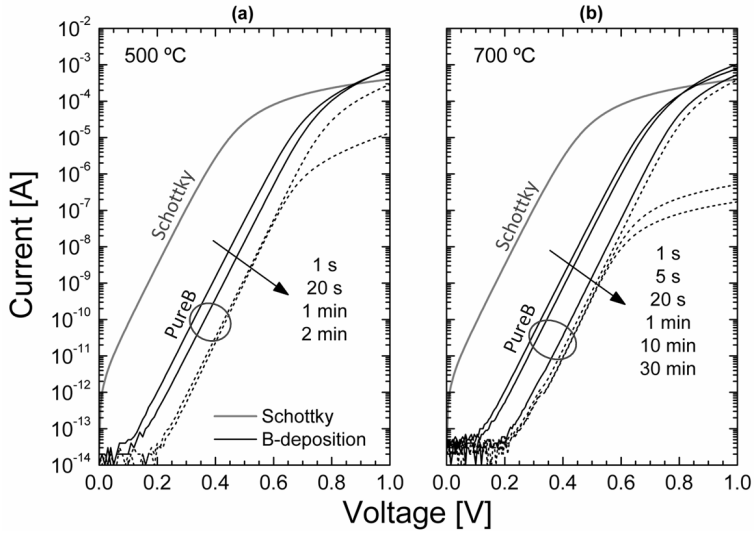

Figure 4.3: PureB diode I-V characteristics for various deposition times at either (a) 500°C or (b) 700°C. The anode area is 2×1 μm^2. For comparison, the I-V curve of a Schottky diode is also included [92].

it is seen that the PureB current levels are decades lower than those of the corresponding Schottky diodes and they decrease somewhat as the deposition time, i.e. PureB thickness, is increased. In earlier work on the PureB technology, it was suggested that the increasing PureB layer thickness was directly responsible for this behavior. Bulk properties of the amorphous B layer itself that could explain the suppression of the electron injection include (i) a very short electron diffusion length and low electron mobility that could cause quenching of the electron

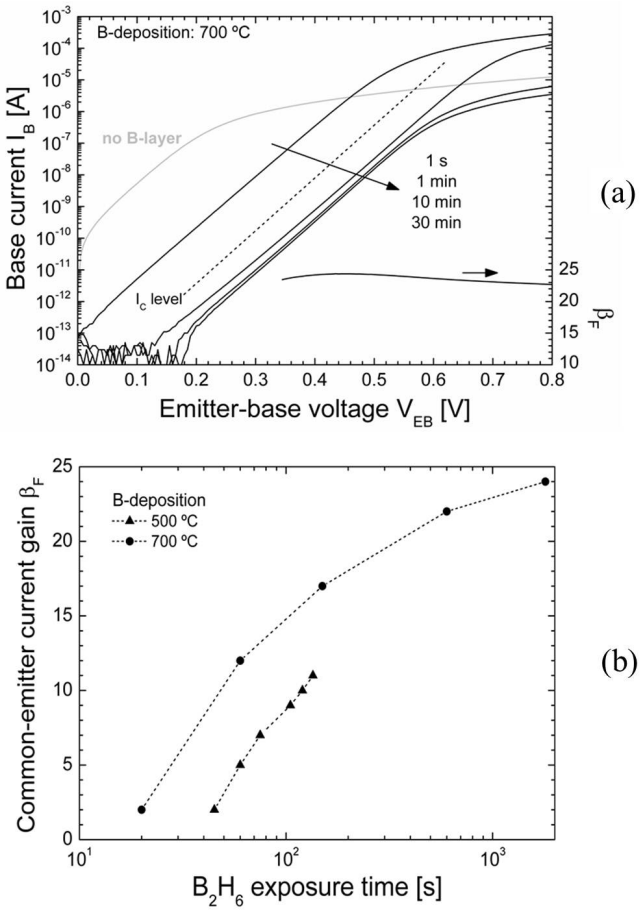

Figure 4.4: Electrical characteristics of pnp bipolar transistors with PureB p^+-emitters deposited at either 500°C or 700°C for different deposition times. (a) Gummel plots showing the base current for each deposition time. The collector current level is also shown as a reference. The common-emitter current gain (right axis) is reported for a device formed with a 30 min deposition time. The emitter area is 40×40 μm^2. (b) The common-emitter current gain as a function of deposition time at V_{EB} = 0.45 V for an emitter area of 40×10 μm^2 [86].

transport [86] or (ii) a wider bandgap than the Si as proposed and supported by simulations in [89] (also see Section 4.2). However, even for a 1 second of PureB deposition where not even a monolayer of B is deposited, an equally high hole injection is observed both for 700°C and 500°C depositions and abnormalities in the I-V characteristics have not been found. Also, the PureGa results described and discussed in the next Section do not support the idea that the bulk properties should be playing a decisive role. All in all, it seems much more plausible that high hole concentration is related to properties of the interface between the pure dopant layer and the Si substrate that induce the creation of acceptor states. For Gummel numbers in the 10^{14} - 10^{15} atoms/cm^2 range this would fit well with the picture that most of the dopant atoms at the interface are activated since monolayer coverage corresponds to about 6.78×10^{15} atoms/cm^2. The increasing Gummel number with increasing PureB could plausibly be related to several effects that increase the hole concentration: the progressive doping of the Si up to the solid solubility level (2×10^{19} atoms/cm^3 at 700°C but much lower at 500°C) or the activation of more and more acceptor states at the interface. Both effects will set the depletion region edge further from the surface to also give a lower influence of the surface recombination of injected electrons.

For photodiode applications it has also been demonstrated that the very high hole gradient right up to the surface, without roll-off, is very important for securing low leakage currents and high responsivity [21]. This gradient repels electrons from the surface where they would otherwise recombine. Even when the PureB layer is driven-in by thermal annealing at temperatures above 700°C, a high gradient is maintained up to the surface and, together with the damage-free nature of this doping technique, a high responsivity is maintained.

4.4 PureGa on Si

Ga is a group III metal, third in line after B and Al. As explained in previous Sections, CVD of the pure dopant on Si can be a powerful technique for the formation of ultrashallow (only a few nanometer deep) p^+n junctions. With the PureB technique, the first high-performance detectors for very low-penetration depth radiation and charged particles have been fabricated [81]. For Ga, the reaction temperature with Si is lower than Al and much lower than B. Therefore, to lower the deposition and associated doping temperature, Ga becomes an attractive option for replacing PureB, which preferably is deposited at 700°C to achieve the most reliably uniform layer [86].

In the past, both MBE [93] MOCVD [94, 95] methods have been used for

depositing Ga and they mostly have been investigate as a way of improving the metal contact to Si or in assisting with deposition of III-Vs [96–99]. In the present research, quite different conditions are used with considerably low controllable concentrations of precursor gases. In general, Ga is difficult to work with in many situations because it takes the liquid form already at 24°C and also readily reacts with many materials such as Si and Al. One of the most commonly used interconnect materials in Si technology is Al, which, in its pure form, also reacts with Si at quite low temperatures. Al is usually used together with a barrier layer such as titanium nitride (TiN) in order to prevent spiking during alloying, normally performed around 400 - 500°C. Similar alloying behavior is observed at even lower temperatures between Si and Ga. For Al the spiking is also often prevented by depositing an alloy of Al and $1\%Si$ (Al/1%Si) instead of pure Al to pre-saturate the system with Si.

This Section presents the CVD of Ga (PureGa) on Si with the AMSI Epsilon 2000 reactor that was equipped with a bubbler system and extra TMGa gas tubing with the purpose of enabling the deposition of GaAs (see Section 2.2). PureGa depositions are investigated at reduced pressure and for deposition temperatures from 400°C to 650°C with the purpose of achieving a selective deposition on Si. In particular, the p^+n junction formation with n-type Si is examined electrically and it is found to behave in a manner similar to PureB but is formed at much lower deposition temperatures.

4.4.1 Fabrication process

A schematic of the basic process flow is given in Figure 4.5. The starting material is n-type monocrystalline (100) Si wafers with a resistivity of 2-5 ohm-cm and a thickness of 525 μm. An isolation layer of 30 nm thermal and 300 nm LPCVD SiO_2 is first deposited at 760°C on the wafers and the areas where PureGa deposition is desired are opened by plasma etching to the Si. Soft landing of the etch-step is applied to limit the damage to the Si surface. Just before PureGa deposition, the native SiO_2 is removed by a 4-min HF dip-etch. In the ASMI Epsilon 2000 reactor a 4-min baking step at 850°C is performed in order to obtain a surface free of native oxide. In principle, due to the low deposition temperature, this high-temperature step can be omitted if precautions are taken to achieve a sufficiently good pre-cleaning of the wafer. Then TMGa is bubbled into the reactor and decomposed at a temperature of 400°C and a pressure of 27 mbar (20 Torr), by the following chemical reaction:

$$2(CH_3)_3Ga + 3H_2 \rightarrow 2Ga + 6CH_4 \tag{4.6}$$

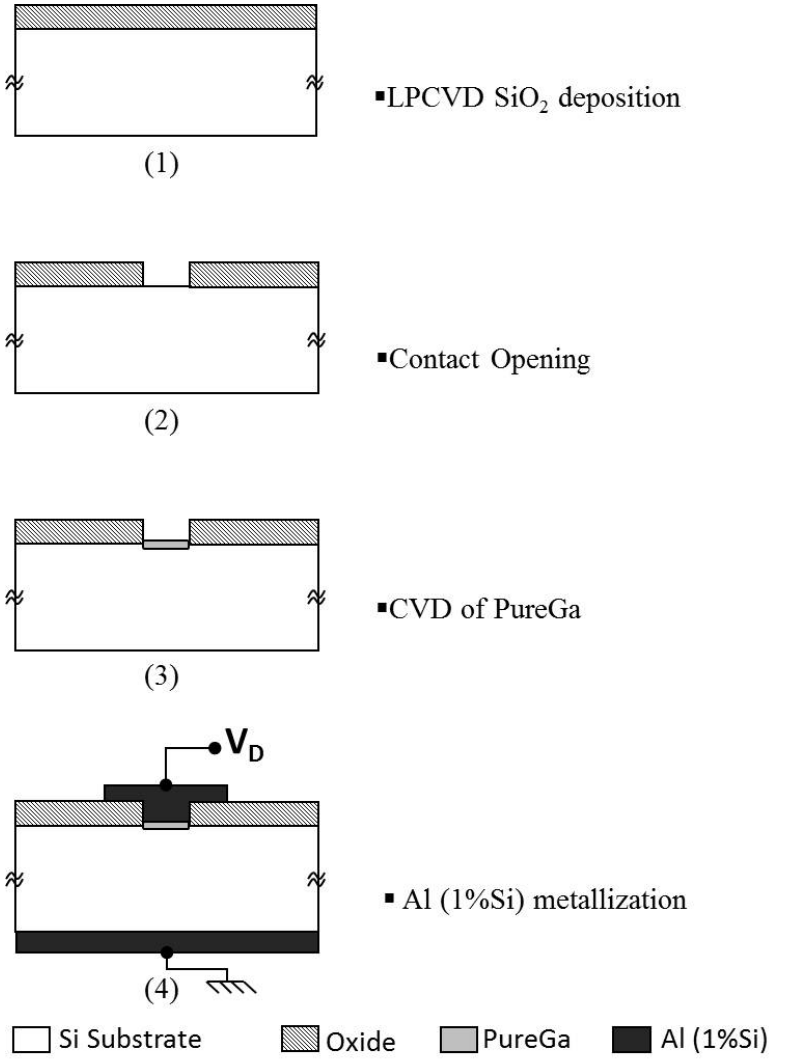

Figure 4.5: Schematic process flow for the fabrication of PureGa p^+n diodes with Al contacting.

Figure 4.6 shows a cross-sectional TEM image of PureGa deposited on the surface of Si at deposition temperature of 400°C. Under this condition, PureGa deposition is uniform over Si and the thickness is approximately 1 nm. In order to minimize the oxidation of the deposited PureGa, wafers are taken immediately from the ASMI Epsilon 2000 CVD reactor to a sputter coater for a 675 nm Al/1%Si deposition. Also the backside of the wafer is coated with Al for contacting of the n-type Si substrate. The Al/1%Si on the front of the wafer is then patterned around the PureGa-deposited windows. The quality of the diodes obtained with and without this deposition, is evaluated by electrical measurements of the I-V characteristics. As will be described in the following, On the basis of all electrical I-V characterizations, it is concluded that the PureGa gives an alternative pure dopant diode behavior on Si at a temperature of 400°C and the resulting p^+n junctions are near-ideal.

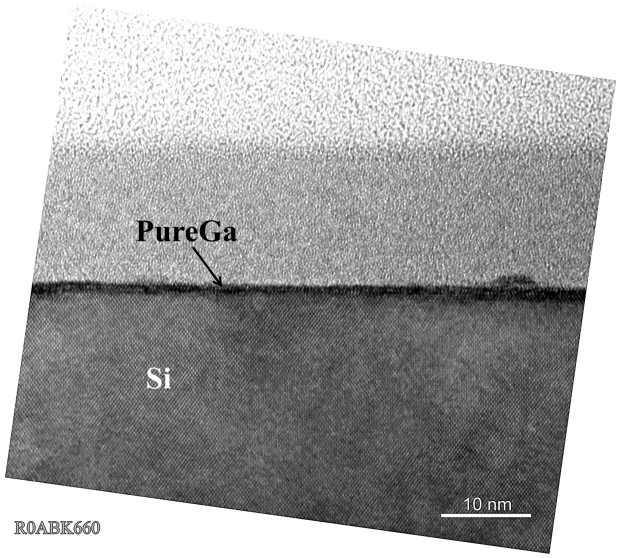

Figure 4.6: Cross-sectional TEM image of PureGa on Si. The coverage is uniform and the thickness is 1 nm.

4.4.2 Electrical behavior

In Figure 4.7 the I-V measurements of diodes deposited with a thin PureGa layer at a temperature of either 400°C, 500°C or 650°C on n-type Si are compared to that of a sample without PureGa deposition. In all cases near-ideal diodes are

obtained with ideality factors of around 1.05. For the Al directly on Si a Schottky junction is formed, which can have a Schottky barrier height (SBH) as low as 0.66 V, depending on the exact surface conditions. Since this is a majority carrier device the corresponding current level, i.e., the saturation current (I_s), can be decades higher than for deep pn junctions. From Figure 4.7 it can be seen that the I_s for the 4 different diodes spreads over 4 decades. For the PureGa deposition at 400°C the I_s is about 2 decades lower than for the Al Schottky diode, which indicates a significant suppression of electron injection that corresponds to high Gummel number of PureGa at 400°C. When going to a 500°C deposition, the I_s increases to about a decade lower than the Al Schottky level, which could indicate that the balance between Ga adsorption and desorption is shifted so that less PureGa is deposited to induce pure dopant interface or that the deposited PureGa preferably dopes the Si and the junction formed is closer to the conventional p^+n. For the 650°C deposition, the I_s is very high and the SBH appears to be lower than for the Al-Schottky case. It is speculated that This could be the result of a completely segregated layer of solid Ga, the SBH of which is lower than that of Al and also formation of defects at the interface similarly to Al spikes. In general, the interesting fact about PureGa is that unlike PureB it does not increase the contact resistance since Ga is a metal with low resistivity.

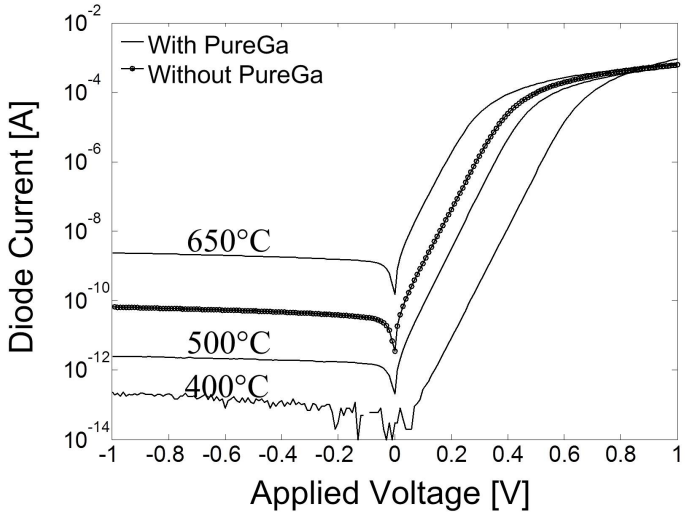

Figure 4.7: I-V characteristics of the diodes formed with deposition of PureGa at three temperatures of 400°C, 500°C or 650°C and a Schottky diode (without PureGa). The diode areas are 140 μm^2 for all cases.

4.4.3 Perimeter and area current analysis

The p^+n junction character of the PureGa on Si can be substantiated by analysis of the area to perimeter current of the diodes. As explained in Section 4.2, the current in Schottky diodes is entirely dominated by majority carrier injection, electrons in this case, from the n-type Si to the metal in forward-bias, and therefore it scales predominantly with the area of the contact. When the contact is sufficiently p^+-doped with a high Gummel number, the electron injection is suppressed and hole injection into the substrate dominates the diode current. Since the lateral hole injection at the perimeter of the contact can be very large, this will have a significant influence on the current level. The area/perimeter current analysis is performed by measuring the I-V characteristics of a large number of diodes with different rectangular geometries varying from 2×1 to 40×40 μm^2 and applying the relationship for the diode current I_d:

$$I_d = I_A A + I_P P + I_C \tag{4.7}$$

where I_A, I_P and I_C are the laterally-uniform area-component, the perimeter-component and the corner-component of the diode current, respectively, $A = L \times W$ is the area of the diode region in which the current is laterally uniform and P is the perimeter of this region. While I_A can be determined exactly from the measurements, I_P can only be estimated by defining the size of A. It is assumed here that the length, L and width, W of the diode region are both 0.3 μm smaller than the on mask dimensions, which is an underestimation of the actual situation for p^+n diodes because of the very extensive current spreading around the diode into the 525 μm thick substrate shrinks the laterally-uniform current region. Nevertheless, the results compiled in Table 4.1 are clear: perimeter current I_P for the PureGa diode fabricated at 400°C is almost ten times higher than area current I_A, which is as would be expected for a p^+n diode. For the 500°C and 650°C depositions of PureGa the values become comparable as expected for Schottky-type diodes.

4.4.4 PureGa lateral pnp transistor

Simple lateral pnp bipolar transistors can be fabricated with PureGa technology by placing some of the contacts within 5 μm of each other. The size of each contact is 1 ×40 μm^2. Figure 4.8 indicates the schematic cross-section of the fabricated lateral pnp. From measurements of the Gummel plots of these transistors, it is possible to separate the hole injection from any p^+ emitter region from the electron current by collecting the hole current at the collector terminal. This is

Table 4.1: Overview of the measurement results for diodes with and without PureGa.

Dep. Temp.(°C)	**Ideality Factor**	**I_s[A]**	**I_A[A/µm^2]**	**I_P[A/µm]**
Al-Sch	1.11	3.7e-11	3.8e-10	4.4e-10
400	1.05	5.5e-15	5.7e-11	3.1e-10
500	1.04	2.1e-12	2.1e-9	1.1e-9
650	1.11	1.8e-9	4.9e-9	3.7e-9

seen in Figure 4.9. A high collector current I_C is observed for the case of PureGa deposition at 400°C, corresponding to a high hole injection from the emitter region, which again proves an emitter with a considerably high Gummel number. At 500°C the hole injection is much lower but still significant, suggesting that there is still substantial PureGa or just Ga doping but the doped layer is apparently so lightly doped and/or thin that it is largely transparent for the electron injection from the substrate to the metal contact. This accounts for the high I_s and Schottky like behavior [83]. At 650°C the measured I_C is low and not discernible from the individual diode (leakage) currents, i.e., there is no measurable p-doping of the emitter.

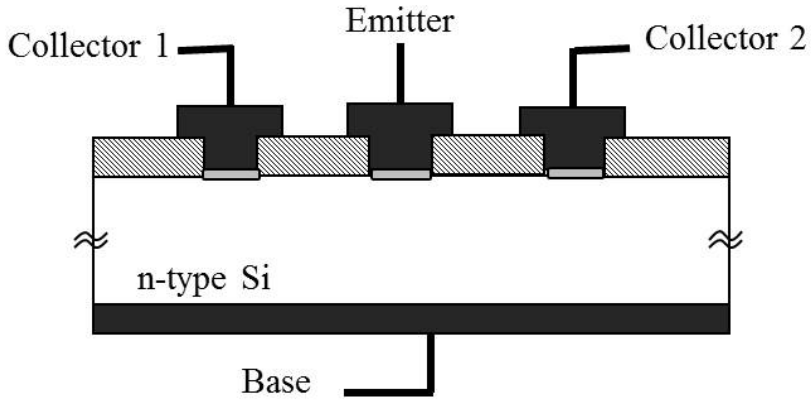

Figure 4.8: Schematic cross-section of the fabricated lateral p-n-p transistors

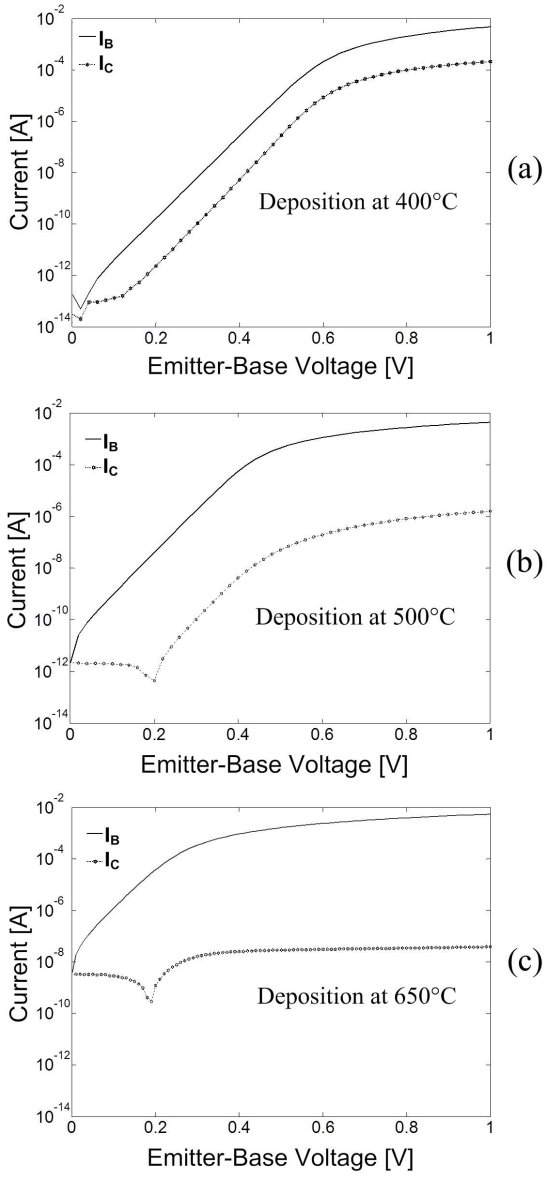

Figure 4.9: Gummel plots measured on lateral pnp transistors with Ga deposition at either (a) 400°C, (b) 500°C or (c) 650°C.

4.5 Conclusions

The combination of precursors for growing both Si/SiGe and GaAs doped layers in a single ASMI Epsilon 2000 CVD reactor have provided a powerful tool for forming pure dopant p^+n junctions. The originally investigated PureB deposition, performed at 700°C and in H_2 carrier gas, has been very extensively studied and is optimized for integration in photodiode detectors for low penetration depth beams. Besides the attractive electrical characteristics, the layer itself excels in physical properties like uniformity and robustness during processing and optical exposure. The door to many more applications has been opened by introducing low-temperature deposition, down to 400C, of either PureB or PureGa, both of which have been demonstrated to deliver Si diodes with the equally good electrical characteristics. This fact has led to the proposition that the effectively high Gummel number of the resulting p^+-region is related to the creation of acceptors states at the interface rather than being a property of the bulk dopant material. Also the very low processing temperature of PureGa makes it potentially very attractive for many device applications including CMOS ultrashallow source/drain fabrication.

Chapter 5

Ge-on-Si photodiodes

In the previous Chapters, Si based integrations of Ge (from group IV of periodic table) and B and Ga and As (from group III and V of periodic table) by CVD techniques have been presented for different applications. Utilizing such techniques have led to epitaxial growth of GaAs in Chapter 2, crystalline growth of Ge-on-Si, despite the lattice mismatch in Chapter 3 and fabrication of ultrashallow Si junctions by pure dopant deposition of B and Ga in Chapter 4. In this Chapter, a novel fabrication method of ultrashallow "Ge" junctions is introduced by merging the techniques presented in previous Chapters. With the growth technique of crystalline Ge-on-Si in ASMI Epsilon 2000 CVD reactor, an As-doped Ge is first grown selectively at the temperature of 700°C where most of the lattice mismatch-defects are trapped at the interface of Ge and Si and vanish within the first 200 nm of Ge growth (see Chapter 3). Then, for the implementation of the ultrashallow junction, the process is followed in the same reactor with a sequence of PureGa and then PureB depositions (see Chapter 4), to form a pure dopant junction on As-doped Ge-islands. The term "PureGaB" is introduced for this technology. The I-V and C-V characterizations of the diodes that are presented in the following, illustrate ideality factors of less than 1.1 and reliably low saturation currents. The doping levels are shown to be such that the depletion over the diodes falls within the Ge defect-free region. PureGaB Ge-on-Si diodes are then presented as a promising approach to fabrication of CMOS compatible APDs that are highly sensitive to infrared (IR) wavelengths above 1 μm in avalanche and Geiger modes.

5.1 Introduction

State-of-the-art Ge APDs that are operational in telecom band at 1.55 μm, generally require the use of III-IV compounds and alloys, such as InGaAs/InP/InAlAs. The literature on this class of materials is vast; see [100, 101] as an example. Devices commercially available today based on these technologies can reach quantum efficiencies higher than 50% and dark count rates of less than 100 Hz but they are usually cooled to operate at cryogenic temperatures. Photomultiplier tubes (PMTs) are the oldest technology available but they are still used thanks to their good timing resolution and ease to use, but they are bulky and do not operate in strong magnetic fields, thus limiting their applications in some medical imaging fields. Ge APDs have existed for decades but their sensitivity in the telecom band is limited and they exhibit high noise in a wide frequency band, even when operated cryogenically.

All these technologies share a fundamental incompatibility with standard CMOS processes and are thus not indicated for low-cost photon counters and large photon counting pixel arrays with and without on-chip processing. Si photomultipliers (SiPMs) and CMOS single-photon avalanche diodes (SPADs), whose bandgap enables the detection of shorter than 1.1 μm wavelengths, cannot be used in the telecom band, unless upconversion techniques are used [102]. However, such techniques are extremely inefficient and inappropriate in most applications.

In the work presented in this thesis, a novel processing procedure was developed for the fabrication of pure dopant p^+n Ge diodes on Si substrates, where the p^+-region is created by a sequence of nanometer-thick PureGa and PureB depositions. Unlike the Si case, where PureB depositions can be used to create high-quality ultrashallow p^+n diodes (see Section 4.3), a similar exposure to B_2H_6 gas will not create the necessary pure dopant junction on the Ge surface. This function can be achieved here by exposure to TMGa, which results in a PureGa. However, PureGa does not produce a reliable contact; therefore, the process is followed by a PureB deposition that functions a chemically resilient barrier layer to the Al interconnect layer being used. The term PureGaB is introduced for this PureGa/PureB layer stack.

The I-V characterization of the fabricated p^+n diodes gives a clear confirmation that the quality of the Ge grown by this method is excellent. The perimeter/area analysis of the diodes confirms the ultrashallow p^+-region and hole injection to n-type Ge from PureGaB, and no extra perimeter isolation techniques were necessary for obtaining good p^+n Ge diodes. The diode characteristics are uniform over the wafer for different sizes and have low series resistance, as well as exceptionally low saturation current and ideality factors. Further development

of this process lead to fabrication of Ge-on-Si APDs without having to introduce extra process steps to obtain good diode characteristics with suitable avalanching behavior.

5.2 PureGaB on Ge

5.2.1 Device fabrication

The selective crystalline Ge growth on Si substrates was explained in detail in Section 3.2: the starting material is n-type Si (100) wafers with a resistivity of 2-5 ohm-cm. Experiments were performed with around 1 μm SiO_2 first being formed on the surface of the wafers and the areas where Ge deposition is desired are opened by plasma etching to the Si with soft landing. Just before loading in the CVD reactor a HF dip-etch and Marangoni drying are performed, while in the reactor a 4-min baking step at 850°C is used in order to ensure that the surface is free of native oxide. Then 2% diluted GeH_4 gas is led into the reactor chamber together with AsH_3 at a pressure of 20 Torr and temperature of 700°C as the precursor gas for the growth of As-doped Ge.

In order to form the pure dopant junction on the surface of Ge then TMGa and B_2H_6 are used for deposition of the so-called PureGaB layer. Both these precursors have in the past Chapters been shown to be suitable for creating pure dopant junctions on Si. Based on this experience, it was expected that high p-doping levels could be introduced at the Ge surface by deposition of a thin layer of PureB at 700°C. However, while this procedure results in a very high effective p^+ doping on Si surfaces (see Section 4.3), it does not appear to be efficient on Ge, which could be connected to the much lower solid solubility of B in Ge as compared to Si. In contrast to PureB depositions, PureGa depositions do create an effective p^+ doping of the Ge surface. However, adding PureB is proved to be highly useful. The advantages of adding this PureB layer on Ge are twofold and its special properties have enabled the implementation of a straightforward metallization scheme using only sputtered Al. For the first, the surface of Ge covered with PureGa is very prone to oxidation and the resulting oxide not only affects the surface effective p^+ doping (pure dopant) but also needs to be removed before metallization. The PureB layer does not oxidize to any measurable degree, and the Al can therefore be deposited directly after the CVD processing. Secondly, the PureB layer acts as a barrier for Al diffusion into the Ge which otherwise readily gives spiking that can short-circuit the junction.

The basic process flow for the fabrication of Ge-on-Si PureGaB diodes is il-

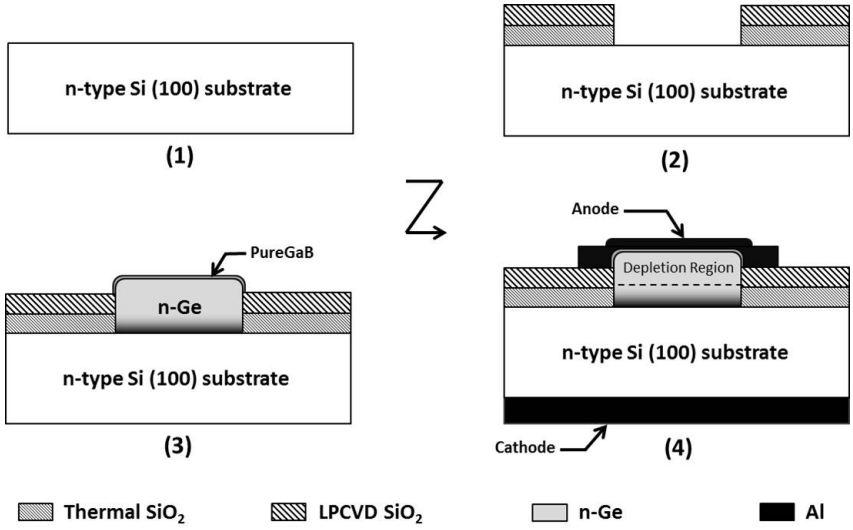

Figure 5.1: Schematic process flow for the fabrication of PureGaB p^+n Ge diodes.

lustrated in Figure 5.1. The covering oxide layer on Si substrate is a stack of 300 nm thermal and 700 nm LPCVD SiO_2. In one deposition cycle first around a 1 µm-thick n-type Ge is grown at 700°C on the exposed Si. Then PureGa is deposited to form the ultrashallow p^+-region and finally a PureB layer of almost 2 nm in thickness is deposited on the Ge surface. In Section 4.4 it was shown that PureGa deposition was most effective at a temperature of 400°C and the same conditions have been applied here to create a surface p^+ doping of the Ge. Subsequent exposure to B_2H_6 creates a PureB layer on the surface at temperature of 700°C. The junction formed by this PureGaB and the crystalline n-type Ge-on-Si must have a doping so large that the depletion will fall in the defect-free region of Ge. For this reason, the growth mechanism is designed to achieve n-type Ge with doping of around 10^{18} atoms/cm^3 at the desired deposition temperature of 700°C. Such doping concentration guarantees a depletion depth of less than 0.5 µm at room temperature which is formed totally inside the defect free area of the grown Ge. The doping concentration of Ge is also dependent on the window sizes where the growth occurs and for the smaller window sizes, a higher doping concentration is achieved as will be discussed in Section 5.2.2. Figure 5.2 shows top-view SEM images of two fabricated Ge-on-Si PureGaB diodes, before metallization, with the sizes of 10 ×10 µm^2 and 20 ×40 µm^2.

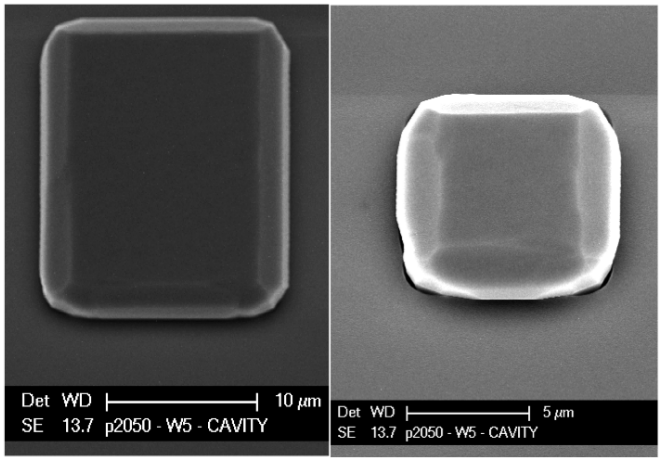

Figure 5.2: Top-view SEM images of Ge-islands grown on a Si substrate with the PureGaB layer on top as described in the APD flowchart given in Figure 5.1, taken before metallization.

After the deposition cycle of Ge-on-Si and PureGaB in the ASMI Epsilon 2000 CVD reactor, wafers are loaded immediately into a sputter coater for deposition of a 675 nm Al/1%Si. The samples are exposed to air during transfer from the CVD reactor to sputter coater, but nevertheless the PureGaB layer protects the Ge surface from oxidation. Also the backside of the wafer is coated with Al/1%Si for contacting of the n-type Si substrate. The metal on the front-side of the wafer is then patterned to cover and contact the individual Ge-on-Si PureGaB diodes. Diodes with different sizes are characterized electrically by I-V and C-V measurements.

5.2.2 Electrical behavior

Current-voltage characteristics

For better analysis of the PureGaB technology, two types of diodes have been electrically characterized by I-V and C-V measurements: (i) Schottky diodes with Al sputtered directly on n-type Ge-on-Si, and (ii) Ge-on-Si PureGaB diodes contacted by Al. The resulting I-V diode characteristics of both cases are shown in Figure 5.3 for different diode area sizes going from 1×1 μm^2 to 40 ×40 μm^2. As it is summarized in Table 5.1, a low saturation current (I_s) of less than 20 pA (with an I_{on}/I_{off} ratio of 10^9) is found for all PureGaB diodes at a reverse-bias

voltage of 2 V while the saturation current of Ge Schottky diodes with the same bias voltage and for the same geometries are about two decades higher than that of PureGaB diodes. This is in accordance with the fact that Schottky diodes are majority carrier devices, the current levels of which can be decades higher than p^+n diodes with a high Gummel number of the p^+-region.

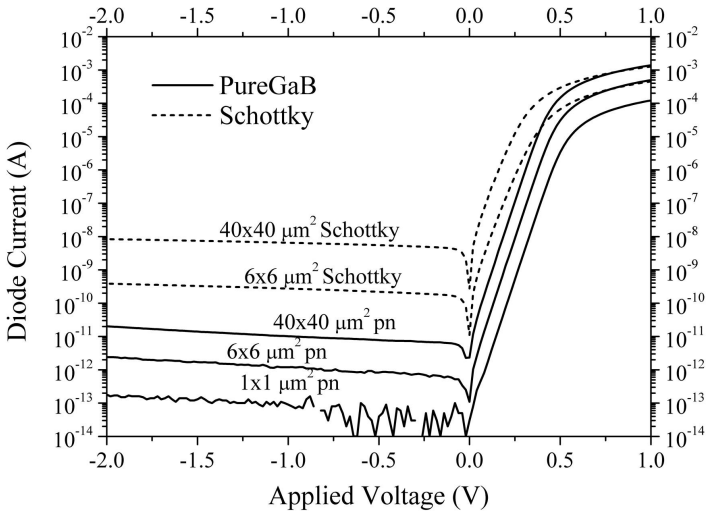

Figure 5.3: I-V characteristic of Ge-on-Si PureGaB diodes for geometries of 1×1 μm^2, 6×6 μm^2 and 40×40 μm^2 together with Ge-on-Si Schottky diodes for geometries of 6×6 μm^2 and 40×40 μm^2.

Table 5.1: Ideality factors and saturation currents (I_s) at 2 V reverse-bias of Ge-on-Si Schottky and PureGaB diodes with different geometries, measured at 27°C.

	1×1 μm^2 (PureGaB)	6×6 μm^2 (PureGaB)	6×6 μm^2 (Schottky)	40×40 μm^2 (PureGaB)	40×40 μm^2 (Schottky)
Ideality factor	1.03	1.05	1.22	1.04	1.24
I_s [A]	1.82e-13	2.39e-12	3.86e-10	2.03e-11	8.36e-9

For all the PureGaB diodes the ideality factors are around 1.05. This indicates that both peripheral and area components of PureGaB diodes are nearly

ideal without any major influence of defects. In addition, the series resistance is not higher than the resistance of about 100 ohm that is present when measuring through the whole Si substrate. These excellent diode characteristics are measured over the whole wafer as it is shown in Figure 5.4 for the diode sizes of 1×1 μm^2 and 40 ×40 μm^2. The observed spread is considered particularly low because no special attempts were made to passivate the Ge to SiO_2 interface at the diode perimeter.

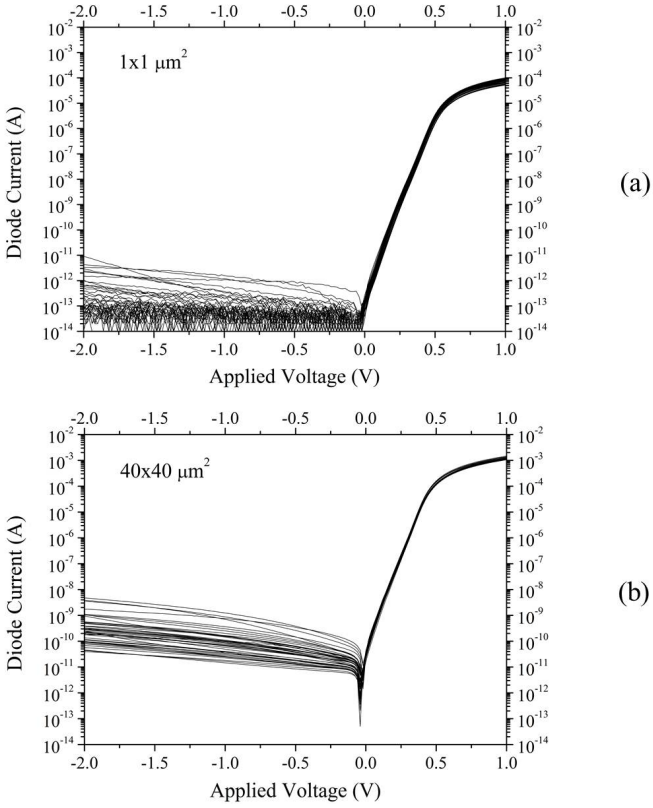

Figure 5.4: characteristic of Ge PureGaB diodes over the wafer for geometries of a) 1×1 μm^2 and b) 40×40 μm^2.

Capacitance-voltage characteristics

C-V characterization is carried out on different sizes of Ge-on-Si Schottky and PureGaB diodes to gain information on the doping concentraion of the Ge. The

C-V profile of the junction was extracted using the equations

$$C = \frac{dQ_s}{dV} = qAN_D(W)\frac{dW}{dV} \tag{5.1}$$

$$C = \frac{K_s \epsilon_0 A}{W} \tag{5.2}$$

$$N_D(W) = \frac{C^3}{qK_s\epsilon_0 A^2 \left[d\left(1/C^2\right)/dV\right]} \tag{5.3}$$

where, K_s is the relative permittivity of Ge of 16.0, W is the depletion width, V is the applied reverse-bias voltage and $N_D(W)$ is the concentration of donors for a junction with the area A. The C-V measurements are shown in Figure 5.5 for four Schottky and four PureGaB diodes with geometries of 40×40 μm^2, 40×20 μm^2, 40×10 μm^2 and 20×10 μm^2 at reverse-bias voltages of 0 to 20 V. Also measured capacitance versus junction area is shown in Figure 5.6 for a given bias voltage of 0 V where the differentiation of capacitance is maximal.

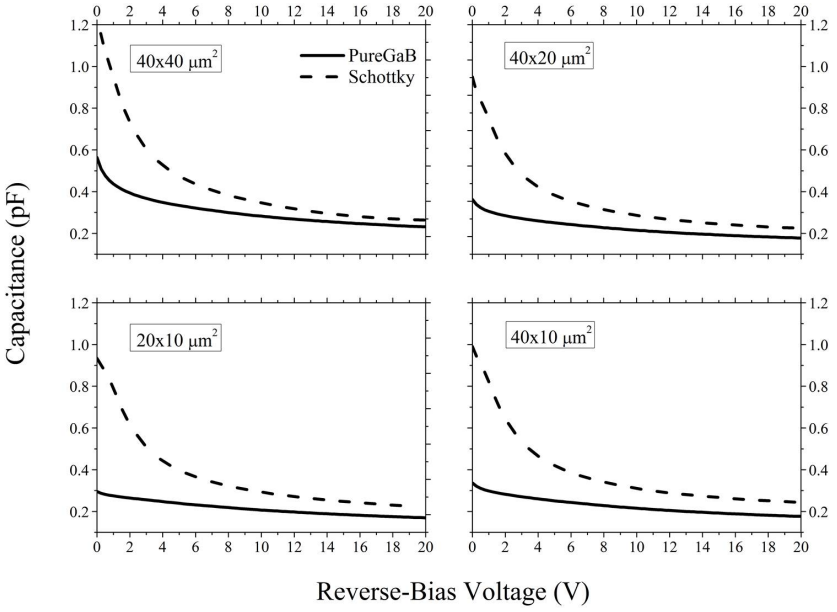

Figure 5.5: Capaticitance as a funtion of reverse-bias voltage and for 4 different geometries of Ge-on-Si Shottky and PureGaB diodes.

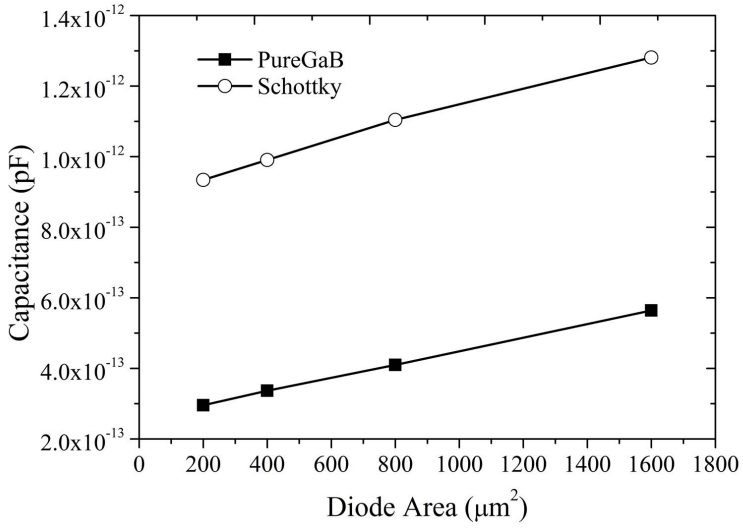

Figure 5.6: Capacitance as a function of junction area for both Ge Schottky and PureGaB diodes.

From Figure 5.6 one can conclude that capacitance is increasing much slower with area than would be expected if the Ge-islands were evenly doped. This is plausibly due to a non-uniform doping of each island caused by a loading effect combined with a low diffusivity of the As atoms across the Ge surface. The peripheral region of the Ge islands then receives and maintains more dopant atoms during growth and hence becomes more highly doped than the more central regions. This results in a peripheral capacitance that is higher per unit than the bulk capacitance. Therefore, the corresponding C-V profiles using the total island capacitance values, will reflect an average doping of the island. Since the loading effects are sensitive to the overall surroundings of the oxide windows in which the Ge is grown, it is not possible to correctly distinguish perimeter/area doping by differential measurements in the present experiment.

In Figure 5.7 the extracted n doping concentrations are displayed for Ge-on-Si Schottky and PureGaB diodes with different geometries. The calculation using equations 5.1 to 5.3 assumes a laterally uniform doping which is not correct in this case. Therefore the resulting doping is an average doping of the peripheral and bulk regions. It is clear from Figure 5.7 that the doping concentrations of both Schottky and PureGaB diodes match well for each geometry. Due to the lower

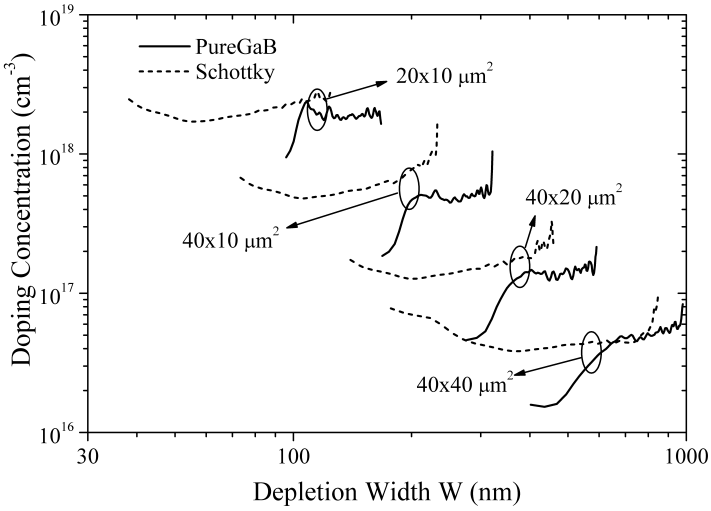

Figure 5.7: C-V doping profiles for the n doping of Ge grown in different window sizes measured on either Schottky or PureGaB diodes. The doping profiles indicate a concentration variation from 2×10^{18} atoms/cm^3 to 4×10^{16} atoms/cm^3 for a factor of 8 change in area from 20×10 μm^2 to 40×40 μm^2.

built-in voltage across the Schottky diodes it is possible to profile closer to the surface with these devices than with the PureGaB diodes. This confirms the p^+n nature of the PureGaB diodes as well as the reliability of the doping concentrations within the crystalline Ge-on-Si with and without PureGaB processing. As expected from the C-V measurements themselves, the extracted doping level is strongly related to the area of the junction and decreases significantly as the bulk area of the diode becomes large. Besides the loading effects on the As doping, the contribution of Ge species will also increase as the geometry of the windows are reduced due to surface diffusion across the oxide. This phenomenon, however, has more impact on the amount of As atoms available for dopant incorporation than on the amount of Ge being grown. Therefore, higher doping levels are achieved for smaller geometries of Ge-islands. For the diode areas used in Figure 5.7, a factor 4 increase in area leads to less than two decades difference in doping going from 2×10^{18} atoms/cm^3 to 4×10^{16} atoms/cm^3. For a very large window of 300×300 μm^2 the extracted doping goes down to 10^{15} atoms/cm^3 which means that the large bulk region is so lightly doped that the Si substrate doping is being measured.

5.2.3 Perimeter and area current analysis

The p^+ doping character of the PureGaB layer can also be substantiated by analysis of the area to perimeter current of the Ge diodes in forward bias. For this case, both Ge Schottky and PureGaB diodes with square-shaped geometries have been measured and analyzed. In a Schottky diode at forward bias, the current is dominated by majority carrier injection which in this case is electrons from the n-type Ge to the metal. In contrast, for p^+n junction diodes, the majority carrier injection is presumably suppressed and minority carrier injection, holes in this case, from PureGaB to n-type Ge, will dominate.

As explained in Section 4.4.3, the diode current can be modeled as

$$I = I_A A + I_P P + I_C \tag{5.4}$$

where I_A, I_P and I_C are the laterally-uniform area-component, the perimeter-component and the corner-component of the diode current, respectively. For square-shaped geometries, $A = L \times L$ is the area of the diode region in which the current is laterally uniform and $P = 4 \times L$ is the perimeter of this region when L is the on-wafer length of the junction. To evaluate the importance of the perimeter component of the current in p^+n junction diodes, a number of square-shaped Ge-on-Si Schottky and PureGaB diodes with an on-mask length L_m of 6 µm, 7 µm, 8 µm, 9 µm, 10 µm, 11 µm and 12 µm have been electrically characterized. The on-wafer L and on-mask L_m junction length are related by

$$L = L_m + \Delta L \tag{5.5}$$

where the length mismatch ΔL is related to the entire fabrication process. Here we assume ΔL to be constant and independent of the on-mask junction length, L_m for both Schottky and PureGaB diodes. Hence, it can be derived from equation 5.4 that [103]

$$\frac{I_j - I_i}{L_{m,j} - L_{m,i}} = I_A \left(L_{m,j} + L_{m,i}\right) + 2I_A \times \Delta L + 4I_P \tag{5.6}$$

where $L_{m,j}$ and $L_{m,i}$ are junction lengths of two different geometry diodes i and j, and I_j and I_i are the corresponding diode currents, respectively. Now the I_A of both Ge-on-Si Schottky and PureGaB diodes can be determined directly by applying equation 5.6 at a fixed forward-bias voltage in the exponential region and plotting the values as shown in Figure 5.8. For the Schottky case, a quite good linear behavior is obtained while the PureGaB values are more disperse. This can be related to the fact that Schottky diodes are majority carrier devices where the

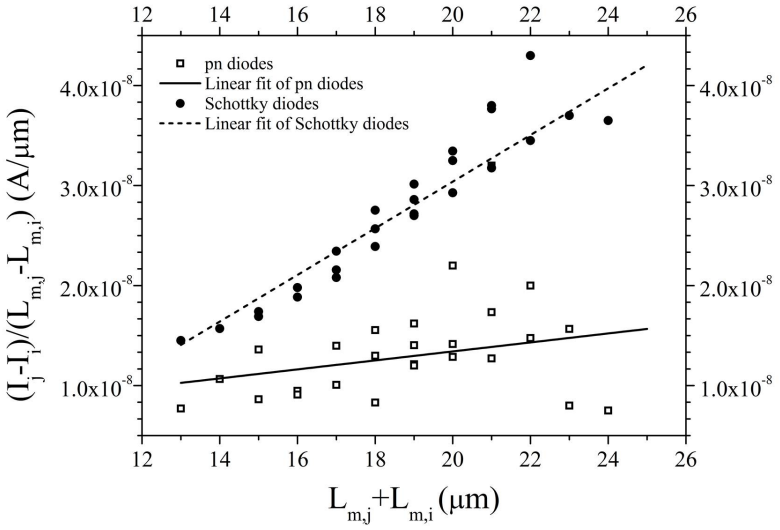

Figure 5.8: Measured diode currents as a function of different deposition window lengths for either Ge Schottky or PureGaB diodes, used to determine the area current component I_A from equation 5.6.

electron injection from the n-type Ge dominates the current. Given that the Al contacting is uniform over the Ge surface, this means that the current should predominantly scale with the area. It can then be assumed that the perimeter current of the Schottky diodes is zero. By applying this assumption to equation 5.6 we find the ΔL to be approximately 1 μm which is a reasonable value considering the window size enlargement due to wet oxide etching of the windows to the Si surface. On the other hand, the PureGaB p^+n diode current should be dominated by minority carrier hole injection from the p^+-region into the n-type Ge, in which case the Gummel number, i.e., doping, of the Ge is decisive. In view of the C-V profiling results that show the doping is geometry dependent and much higher at the diode perimeter, it is not surprising that there is a significant spreading of the PureGaB values in Figure 5.8. Nevertheless, the ΔL value found from the Schottky case is applied to extract an I_P from equation 5.6 for these diodes. The final area and perimeter characterization is summarized in Table 5.2. The extracted I_P is only 3 times higher than the I_A in the PureGaB case. Overall, this analysis supports the conclusion that there is no excessive perimeter leakage dominating the total current of these Ge-on-Si diodes.

Table 5.2: Extracted forward-bias perimeter and area current densities for Ge Schottky and PureGaB diodes, measured at 27°C.

Diode	**V_D [V]**	**I_A [A/µm^2]**	**I_P [A/µm]**	**I_P/I_D[%](10×10 µm^2)**
Schottky	0.18	2.33e-9	0	0
PureGaB	0.3	4.45e-10	1.35e-9	54.8

5.3 Ge-on-Si APDs by PureGaB

Photodetection is considered to be the most evident application of PureGaB technology. The advantages of the PureGaB ultrashallow junctions with the Ge-on-Si growth techniques presented in this thesis, leads to a promising approach to fabricate CMOS compatible Ge-on-Si APDs. In the following the prototype of such photodiodes is delivered. The measurements show high sensitivity of the APDs to infrared wavelengths above 1 µm in avalanche and Geiger modes.

5.3.1 Fabrication process

The APD fabrication flow is shown in Figure 5.9. The starting material is p-type Si (100) wafers with a resistivity of 2-5 ohm-cm. First a buried n^+-layer is implanted and capped with a 0.5-µm-thick Si epitaxy. Then n^+- and p^+-plugs are implanted for contacting the buried n-region and p-type substrate, respectively. An isolation layer of 1 µm LPCVD SiO_2 is then deposited and those regions where Ge growth is desired are opened by plasma etching to the Si with soft landing. In the next step, Ge-on-Si PureGaB diode is grown in the ASMI Epsilon 2000 CVD Si/SiGe system as described in Section 5.2.1. For the metallization, physical-vapor-deposited (PVD) Al/Si(1%) is used to contact the n-type Si and the anode of the p^+n Ge diode. Arrays of diodes with different areas, as large as 40 ×40 µm^2, were fabricated. They all displayed good I-V characteristics and the smaller ones could be operated in Geiger mode. In the following, two APDs with areas 2×2 µm^2 and 2×20 µm^2 are characterized.

5.3.2 Optical/Electrical behavior

The current-voltage (I-V) characteristics of photodiodes with two different sizes are shown in Figure 5.10. The breakdown voltages V_{br} are found to be respectively 13 V and 9 V for the 2×2 µm^2 and 2×20 µm^2 devices and the corresponding ideality factors are 1.15 and 1.35. The dark currents at 1 V reverse-bias are as

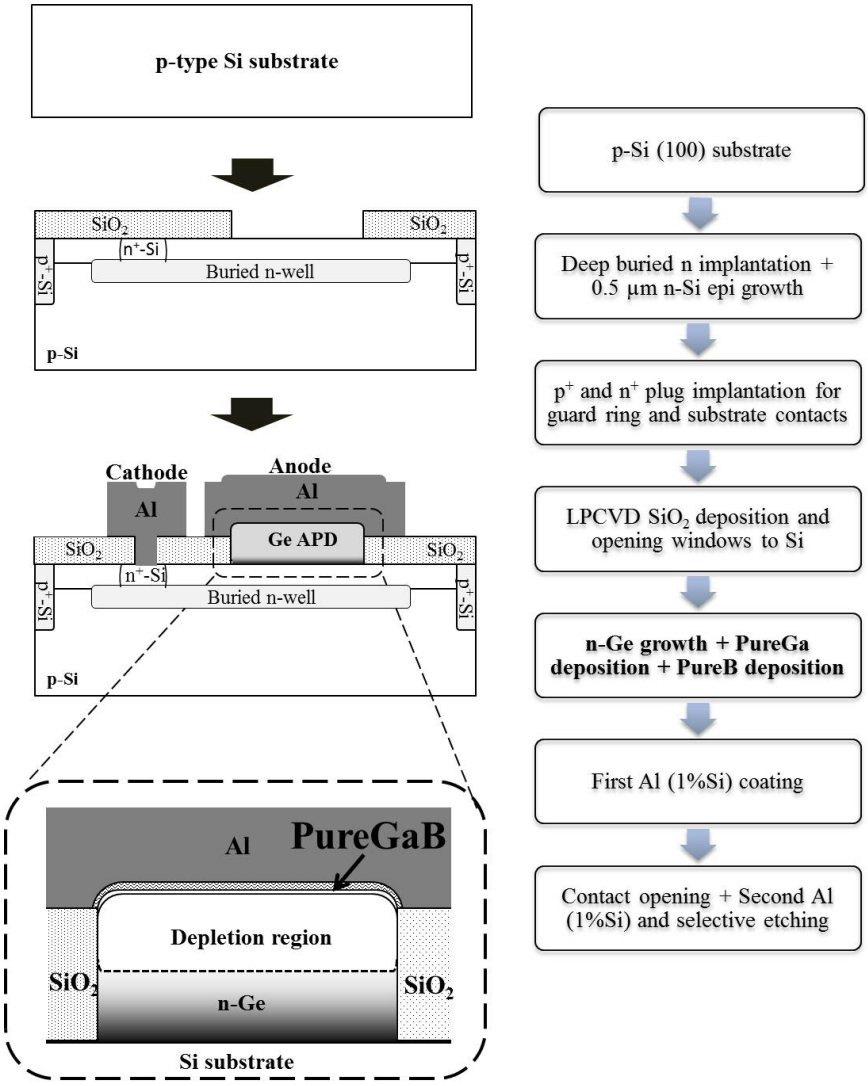

Figure 5.9: APD fabrication flowchart.

low as 2 pA and 20 pA for the 2×2 μm^2 and 2×20 μm^2 devices, respectively, and increase to hundreds of micro-amps past the breakdown.

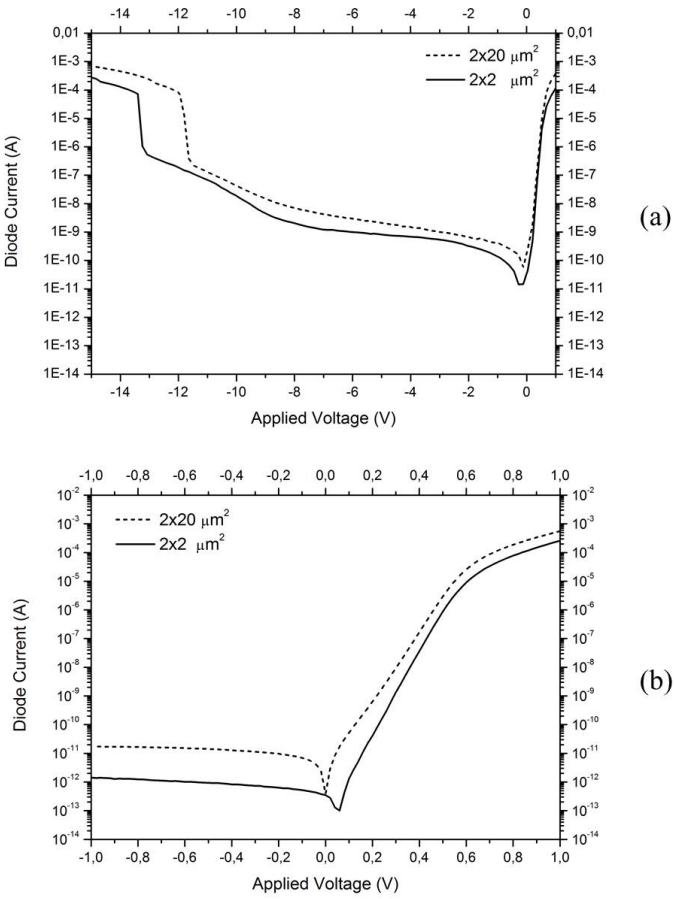

Figure 5.10: I-V characteristics of APDs with areas of 2×2 μm^2 and 2×20 μm^2. The breakdown is shown in (a) and the ideality factors are, respectively, 1.15 and 1.35.

In Figure 5.11 a schematic is shown of the circuit used to operate the APD in Geiger mode with passive quenching and passive recharge via a ballast resistor. The APD is biased above V_{br} by a voltage known as the excess bias V_e, The total voltage is $V_{op} = |V_{br}| + V_e$. The range of V_e is from 0 to 4 V. This high operational voltage causes high electric fields across the depleted p$^+$n junction that may cause

an avalanche current when the interaction of a photon or a thermal event in the Ge creates electron-hole pairs.

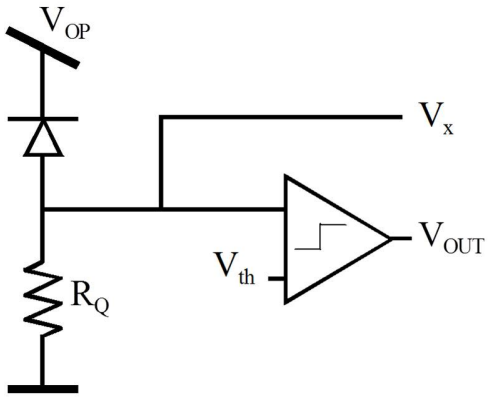

Figure 5.11: The APDs were biased above breakdown using the above circuit, so as to operate in Geiger mode. The ballast resistance RQ is used to perform passive quenching and passive recharge. $V_{op} = |V_{br}| + V_e$, where V_e is the excess bias voltage and V_{br} is the breakdown voltage. The comparator, with an appropriate threshold voltage V_{th}, was used to convert Geiger pulses to digital signals.

The p^+-anode of the APD is connected to the ballast resistor. Whenever a photon reaches the APD, a Geiger pulse is generated, and the ballast resistor quenches the device to be ready for the next event. The avalanche current going through this resistor builds up to a sharp voltage pulse, known as a Geiger event (see Section 1.1.5). Geiger events are converted to digital pulses by using a comparator with an appropriate threshold voltage V_{th}.

Besides photon-generated pulses, in the dark, carriers can be generated due to generation-recombination processes inside and near the multiplication region (see Section 1.1.5). This results in dark counts, characterized by the parameter dark count rate (DCR), or the mean frequency of dark counts. In order to visually observe the DCR, the V_X of the circuit in Figure 5.11 was connected to an oscilloscope while applying the V_{op} right above breakdown. Figure 5.12 is the oscilloscope photo of the pulses that are generated from the 2×2 μm^2 device in absence of any light and represent the DCR of approximately 6.5 kHz. DCR is more aaccurately mesasured as a function of excess bias voltage using a pulse counter and the results are plotted in Figure 5.13 for the 2×2 μm^2 and 2×20 μm^2 devices.

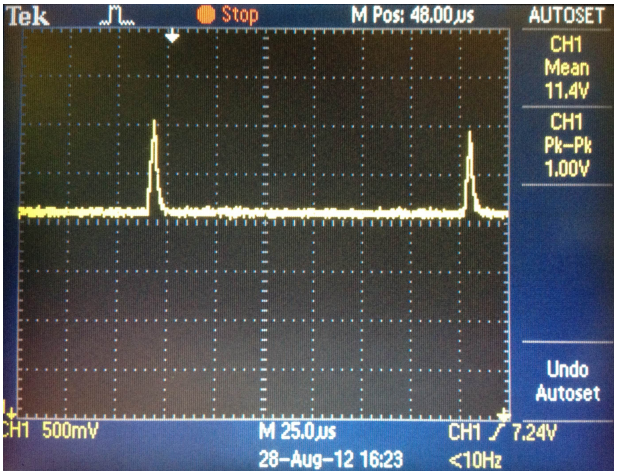

Figure 5.12: Pulses that are generated in the V_x of circuit shown in Figure 5.11 in the absence of any light. The device size is 2×2 µm^2 and the corresponding DCR in this case is approximately 6.5 kHz.

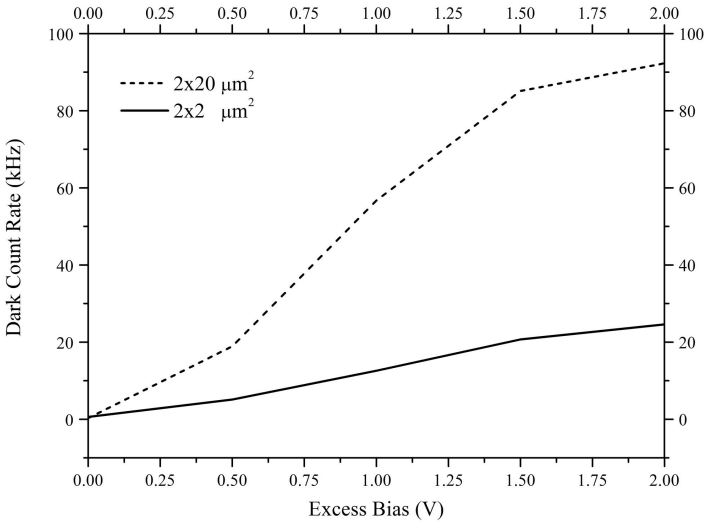

Figure 5.13: DCR as a function of excess bias voltage V_e, at room temperature.

In Figure 5.14 the photo-response is given for the 2×20 μm^2 detector in sub-Geiger mode (both in linear and proportional APD modes). The breakdown voltage is near 11 V and the current after breakdown (100 μA) is 500 times bigger than proportional APD mode current of 200 nA. The infrared-induced current is higher than that induced by visible light which confirms that these Ge photodiodes are more sensitive in the infrared region.

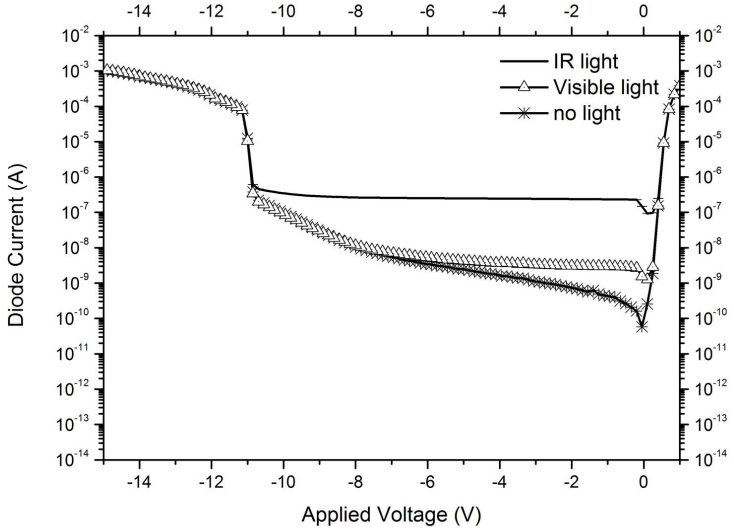

Figure 5.14: Photo response of the 2×20 μm^2 APD as a function of reverse-bias when exposed to a wide-band 800 nm source.

To evaluate the sensitivity of photon detection in avalanche and Geiger mode, the photocurrent I_d of the 2×20 μm^2 diode is measured at different wavelengths by illumination with a light-source spot that is much larger than the diode area. The diode photocurrent I_d is compared with the photocurrent measured on a reference photodiode I_{ref} with an area larger than the spot size for which the quantum efficiency (QE) is known for all wavelengths of interest. The ratio I_d/I_{ref} is plotted as a function of wavelength in Figure 5.15 for the bias voltages of 3 V and 9 V (below breakdown) and 14 V and 15 V (Geiger mode). The 25% peak at an infrared wavelength of 1100 nm in Geiger mode is measured for excess bias voltages of 3 V and 4 V. This gives a conservative indication of the high avalanche current obtainable with the PureGaB diodes.

The timing response is plotted in Figure 5.16 for the APD when exposed

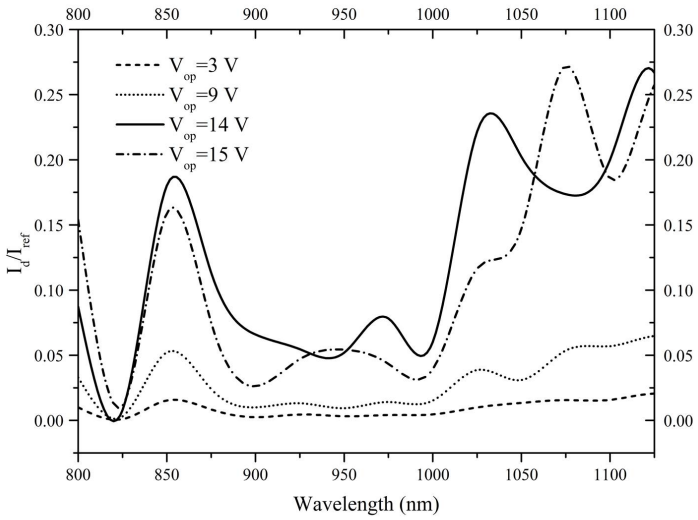

Figure 5.15: I_d/I_{ref} of the 2×20 μm^2 APD in the NIR spectrum for various bias voltages V_{op}.

to a pulsed laser that was centered at 637 nm (Advanced Laser Diode Systems GmBH, Berlin, Germany) with an excess bias voltage of 1 V. The measurement was obtained using the embedded time discriminator of a LeCroy WaveMaster 8600 A. This jitter performance was measured for the 2×2 μm^2 APD with a pulse width of 80 ps. The full width at half maximum (FWHM) jitter was measured to be approximately 900 ps.

Finally, the performance characterization of the photodiodes in three modes of operation (linear, APD, and Geiger) is summarized in Table 5.3. The devices can be fabricated with a range of breakdown voltages that can be accurately controlled from a minimum of 9 V to a maximum of 13 V. The excess biases of 0 to 4 V were applied to the APDs for DCR measurements.

5.4 Conclusions

In this Chapter PureGaB technology was introduced for the fabrication of pure dopant p^+n Ge-on-Si diodes. All doping is achieved in-situ by As doping during the Ge growth and then p^+ pure dopant from a PureGa deposition followed by

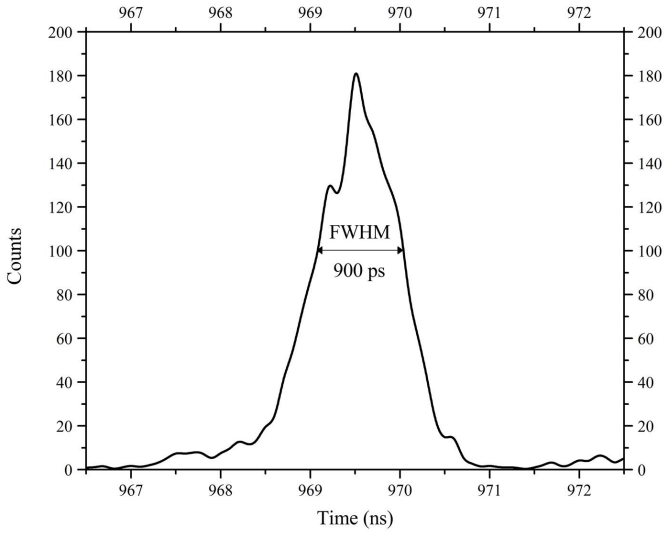

Figure 5.16: Jitter performance of the 2×2 μm^2 APD when operated in Geiger mode. The measured FWHM jitter was approximately 900 ps.

Table 5.3: Summary of performance measurements for linear mode, APD mode, and Geiger mode of operation.

Performance (APD/linear mode)	**Min.**	**Typ.**	**Max.**	**Unit**
Dark current at 1 V reverse-bias	2		20	pA
Active area	4		40	μm^2
Breakdown voltage	9	11	13	V
Performance (Geiger mode)	**Min.**	**Typ.**	**Max.**	**Unit**
DCR at V\subse = 1 V	10		60	kHz
I_d/I_{ref} at V_e=3 V			25	%
FWHM Time jitter			900	ps
Excess bias voltage	0		4	V

a PureB deposition (PureGaB) to form a barrier layer to the Al metallization. To the knowledge of the author, the resulting I-V characteristics have uniquely low values of saturation current, series resistance and ideality factors as well as good uniformity over the wafer. The lack of extra processing to isolate the p^+-region and/or passivation for the Ge sidewalls as well as the quite planar surface after Ge growth make this an attractive and straightforward add-on to standard Si technology. Moreover, the PureGaB technology is in general an attractive method of fabricating diodes on Ge, which could, for example, also be applied in source/drain processing of devices such as Ge PMOS transistors.

PureGaB technology was used to design and implement Ge-on-Si APDs that can be operated both in proportional and in Geiger mode. The fabricated Ge-on-Si APDs exhibit relatively low dark counts and high sensitivity at room temperature. This correlates well with the fact that the I-V characteristics have, uniquely low values of saturation current, series resistance and ideality factors.

Chapter 6

Conclusions and recommendations

In this thesis, CVD techniques for deposition of different materials from group III, IV and V elements were studied. First epitaxial deposition of GaAs in a standard Si/SiGe CVD reactor (ASMI Epsilon 2000) was characterized with details of intrinsic and doped layers. The CVD reactor was then utilized for crystalline growth of Ge on Si substrates with uniquely good quality. Also dopant deposition of PureB and PureGa on Si substrates were studied in order to fabricate ultrashallow pure dopant Si junctions. The techniques of crystalline Ge growth on Si substrates were merged together with PureB and PureGa technologies to develop a new method for fabrication of high-quality Ge-on-Si photodiodes. In this Chapter, specific conclusions of the work presented in this thesis is summarized together with recommendations for any related future work.

6.1 Conclusions

Merging standard Si/SiGe CVD with MOCVD of Ga/GaAs

For all the different chemical vapor depositions described in this thesis, one single system was used: ASMI Epsilon 2000 CVD reactor. The reactor was designed for epitaxial growth of Si and SiGe and for this research it was extended with a TMGa bubbler system to allow deposition of Ga and GaAs. With such a system, depositions of epitaxial GaAs on GaAs substrates and Si on Si substrates as well as crystalline growth of Ge-on-Si and various depositions of pure dopants are possible all in one reactor. Precursor concentrations are kept so low that critical

contamination issues are avoided and after each deposition of materials such as GaAs, the background doping level of the reactor can quickly be returned to the range that is compatible with Si processing by using standard cleaning methods. Moreover, especially the low concentration of AsH_3 gas, only 0.7%, which is considerably lower than the concentration used in most other similar CVD techniques, no sever extra safety precautions need to be implemented.

Selective and large area crystalline Ge on Si substrates

A method for selective growth of crystalline Ge on Si substrates at a temperature of 700°C has been developed. The results were characterized by different techniques such as cross-sectional and plan-view TEM and AFM analysis. These indicate a good quality and crystallinity of the Ge-on-Si with a transition region of less than 200 nm as well as smoothness and flatness on the Ge surface. At a lower deposition temperature of 550°C, the defects grow further into the Ge and the growth is limited along the 311 Ge planes. However, such faceted structures prove to be better suited for subsequent in-situ crystalline GaAs growth. Also solutions were introduced for perfect selectivity on Si over SiO_2 as well as Ge lateral overgrowth.

Chemical vapor pure dopant deposition

It was already proven in the previous work that pure dopant deposition of B (PureB) is a potent solution to fabricate ultrashallow junctions on Si with applications in photodetection of low power and low penetration beams. PureB technology was reviewed shortly in this thesis as the basis for the introduction of Ga (PureGa) deposition as another pure dopant for ultrashallow junction formation on Si. Having a deposition temperature of 400°C makes this technology very interesting for low temperature processes. The electridal characterization of ultrashallow Si junctions fabricated by PureGa are proven to have high-quality and ideality. All in all, the first results of both PureB and PureGa show great potential of both technologies in applications such as Si-integrated APDs and source/drain engineering in advanced CMOS.

Ultrashallow Ge diodes on Si substrates

The combination of both PureB and PureGa technologies were utilized for fabrication of pure dopant ultrashallow p^+n junctions on Ge-on-Si. The p^+ region is formed by in-situ PureGa deposition right after crystalline Ge growth and then

it is followed by in-situ deposition of PureB to form a barrier layer to the metallization. The term PureGaB was introduced for this combined pure dopant deposition. To the knowledge of the author, the I-V characteristics of PureGaB Ge-on-Si diodes have uniquely low values for saturation current, series resistance and the ideality factors. The process is uniform over the wafer and repeatable. The lack of extra processing to isolate of the p^+-region as well as the quite planar surface after Ge growth makes this an attractive and straightforward add-on to standard Si technology.

High-quality Ge-on-Si photodiodes

PureGaB is very attractive for fabrication of high-quality and highly sensitive photodiodes. The PureGaB Ge-on-Si diodes were tested for infrared photodetection and it was shown that they operate both in proportional and in Geiger mode. Such photodiodes (also known as avalanche photodetectors) exhibit low dark counts and high sensitivity to infrared light at room temperature.

6.2 Recommendations for future work

Merging standard Si/SiGe CVD with MOCVD of Ga/GaAs

ASMI Epsilon 2000 CVD reactor has the potential to be further extended for deposition of more compound semicondutors, two most interesting of which are InGaAs and GaN. For InGaAs another bubbler system of trimethylindium ($In(CH_3)_3$) is necessary while for GaN, no extra gas lining is needed. However, for GaN it is probable that a special injector and showerhead are needed. This would be a major operation to change and operate the system accordingly.

Selective and large area crystalline Ge on Si substrates

The method introduced in this thesis for crystalline growth of Ge on Si substrates can be further improved. The main consideration is the control over the loading effect of Ge growth with respect to the opening window sizes as well as the loading effect of the dopant. In order to fabricate many types of devices on the Ge-on-Si especially a fine and sensitive control is needed for arsenic-doping.

Chemical-vapor pure dopant deposition

While PureB technology has become well-established over the last years, more characterization is to be done for PureGa. Not only with respect to its ability to

fabricate Si-based photodiodes but also for its use in standard IC processing. In particular the introduction of a pure dopant on Si surface after metallization made possible, by the low temperature of PureGa depositions. Also the author believes that the same method to fabricate pure dopant p^+n Si diodes can be achieved by other dopants of group III. Aluminum especially can be the next pure dopant candidate to further expand this type of technology. The challenge here is to control the layer thickness and condition to avoid spiking and most importantly the calibration of the deposition temperature.

High-quality Ge-on-Si photodiodes

The electrical and optical characteristics of the Ge-on-Si photodiodes can be further improved by reduction of the DCR. This goal can of course only be achieved by having a good control over the arsenic-doped Ge growth on Si substrates. Also the design of the APDs can be further modified for better sensitivity. The advantage of PureGaB as a good barrier layer can make it also a good etch-stop and protector for Ge-on-Si. As a result a strategy could be developed to remove the aluminum, to have good access to the detector during front-side illumination.

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List of abbreviations

Al	aluminum
AFM	atomic force microscope
APD	avalanche photodetector
ART	aspect ratio trapping
As	arsenic
B	boron
C-V	capacitance-voltage
CMOS	complementary metal oxide semiconductor
CVD	chemical vapor deposition
DCR	dark count rate
DUV	deep ultra-violet
EUV	extreme ultra-violet
FWHM	full-width half-maximum
Ga	gallium
GaAs	gallium arsenide
GB	gain bandwidth
Ge	germanium
HgCd	mercury cadmium
I-V	current-voltage
InAs	indium arsenide
InGaAs	indium gallium arsenide
InSb	indium antimonide
IR	infrared
LD	laser diode
LED	light emitting diode
LPCVD	low pressure chemical vapor deposition
MBE	molecular beam epitaxy
MOCVD	metal-organic chemical vapor deposition
MSM	metal semiconductor metal

P	phosphorus
PDE	photon detection efficiency
PMT	photomultiplier tupe
QE	quantum efficienc
RMS	root mean square
RTA	rapid thermal anneal
Sb	antimony
SBH	Schottky barrier height
Sch	Schottky
SEM	scanning electron microscopy
Si	silicon
SIMS	secondary ion mass spectroscopy
SiPM	silicon photomultiplier
SPAD	single-photon avalanche detector
TEM	transmission electron microscopy
TMGa	trimethylgallium
UV	ultra-violet
VUV	vacuum ultra-violet

Summary

Heterogeneous integration of III-V semiconductors with silicon (Si) technology is of interest for giving on-chip access to both high-speed *photonic* and *electronic* devices. While Si still remains the dominant material for high-speed electronics, other semiconductors with more attractive photonics functionalities (III-Vs, Ge,) are playing an increasingly important role in the photonics industry. The work presented in this thesis was predominantly initiated to reach the goal of merging III-V semiconductor technology with Si technology. The focus was initially placed on the development of a Si-compatible tool for metal-organic chemical vapor deposition (MOCVD) of gallium arsenide (GaAs). For this purpose, a Si/SiGe CVD reactor, the ASMI Epsilon 2000, was extended with a TriMethyl-Gallium (TMGa) bubbler system and extra tubing to allow the deposition of GaAs as well as the standard Si and SiGe depositions. Conventionally, CVD of GaAs is achieved with high concentrations of gases. The high gas concentrations, particularly of the highly toxic gases arsine (AsH_3) and phosphine (PH_3), mean that severe safety precautions must be implemented when running the MOCVD system. The key in this research was to apply a very low AsH_3 concentration: 0.7% as compared to the at least ten times higher values normally used in MOCVDs. The correspondingly low concentration of TMGa means that the contamination of the reactor chamber with Ga or As is so low that standard high-quality low-doped Si and SiGe depositions can still be performed in the same CVD reactor chamber. In view of this, the research took the unique direction of creating devices where the merging of depositions of gallium (Ga), arsenic (As) and boron (B), all in one reactor with Si and Ge, proved indispensable.

The most mature III-V semiconductor is GaAs, which is the basis of several billion dollar worldwide industry for high-speed electronics and photonics technologies. Epitaxial growth techniques are playing a very important role in this industry. In this thesis work, GaAs epitaxy in a Si/SiGe CVD reactor is presented for the first time. Considering the low concentration of the AsH_3 gas, the main challenge was the stoichiometry of Ga and As. By precise control over precursor

gas flows as well as deposition temperature (650°C) and pressure (107 mbar) perfect stoichiometric intrinsic and doped GaAs epitaxy was achieved with a growth rate as high as 5 nm/min. For doping the GaAs, two available possibilities in the ASMI Epsilon 2000 CVD reactor are Si and Ge, both of which are well-known n-type impurities for GaAs. It was possible to grow Si-doped and Ge-doped GaAs epitaxy with doping in the range from 5×10^{17} atoms/cm^3 to almost 10^{20} atoms/cm^3 and from 10^{19} atoms/cm^3 to 5×10^{20} atoms/cm^3, respectively. One of the goals of establishing a process for stoichiometric GaAs epitaxy was to develop a method for growing crystalline GaAs on Si. However, due to the lattice mismatch of 4.2% between GaAs and Si crystals, and the compound nature of GaAs, GaAs epitaxy on Si is a major challenge. The early results were found to have rough surfaces of GaAs that appeared to be polycrystalline in nature, even though good selectivity of growth on Si masked by SiO_2 is observed when growing on patterned Si substates.

To create regions with a better lattice match to GaAs, the selective growth of Ge on Si was investigated. This is not a compound material so the growth conditions are less critical than for GaAs. Moreover, the Ge itself is an interesting photonic material being widely used in infrared (IR) optoelectronics. The quality of the crystalline Ge-on-Si that can be grown depends strongly on the chosen growth conditions. The temperature needs to be high enough to allow the desired chemical reaction to take place and to allow Ge atoms to arrange in a single crystal manner. A pressure of 27 mbar and growth temperatures from 550°C to 700°C were found to render good quality Ge-on-Si with high selectivity. The results of Ge-on-Si growth were studied with plan-view and cross-sectional transmission electron-microscopy (TEM) and atomic-force microscopy (AFM). At 550°C the selective growth forms Ge-islands on Si with faceting along the [311] planes and some dislocation defects are observed inside Ge. In contrast, at 700°C most of the lattice-mismatch defects are trapped within the first 200 nm of Ge growth and with this process good quality crystalline Ge (defect density of 10^7 cm^{-2}) can be achieved with a smooth and flat surface (surface roughness of 2 nm peak to peak) within a layer thickness of approximately 1 μm on window sizes up to hundreds of μm^2. The doping of the Ge was achieved with in-situ As and B doping up to concentrations of 2×10^{19} atoms/cm^3 and 3×10^{18} atoms/cm^3, respectively. Moreover, in order to study the potentials of this Ge-on-Si as a template for GaAs epitaxy, selective growth cycles designed to grow GaAs immediately on the Ge-on-Si islands were studied and found to result in a good quality of the GaAs epitaxy.

Besides the semiconductor depositions of GaAs and Ge, the fabrication of

ultrashallow junctions using pure dopant depositions was also studied where the option to deposit pure Ga was a new feature offered by the extension of the ASMI Epsilon 2000 with a TMGa source. Obtaining an abrupt and highly-doped ultrashallow profile in semiconductor substrates is challenging, since the results of standard doping methods such as diffusion and ion implantation, are limited by the thermal processing applied for dopant incorporation and activation. The deposition of pure boron (PureB) has in the past been shown to be an attractive approach to fabricate ultrashallow (nanometer-shallow) p^+n junctions with uniquely good electrical behavior together with electrical and optical robustness. Here, the deposition of pure Ga (PureGa) at 400°C on Si substrates was shown to give equally good electrical results. Based on the overall experimental evidence it has been proposed that both PureB and PureGa form a practically complete surface coverage of acceptor states on Si as an interface property. The resulting p^+n Si diodes that are a few nm shallow show ideal behavior with saturation currents as low as those typical of deep junctions. Of key importance is the effectively large Gummel number of the PureB and PureGa regions which can be interpreted as a large number of holes per unit area. This provides low saturation currents despite the shallowness of the junctions. The PureB photodiodes were already well developed by the Silicon Device Integration group in Delft University of Technology for a variety of applications: large-area, high-linearity varactor diode technology, deep ultraviolet (DUV), extreme ultraviolet (EUV) and vacuum ultra-violet (VUV) photodiodes and low-energy (less than 1 keV) photodiodes. PureGa, however, was developed in the context of this thesis. The basic advantage of PureGa as compared to PureB is the lower reaction perature with Si (400°C). Therefore, PureGa becomes an attractive option for replacing PureB, which preferably is deposited at 700°C to achieve the most reliably uniform layer. The I-V characteristics and perimeter/area current analysis of PureGa diodes as well as the Gummel plots of fabricated lateral pnp transistors with PureGa emitters/collectors all display a high hole injection from the PureGa region into the n-Si. This electrical behavior closely resembles that of the PureB diodes, which, together with the fact that it occurs at low temperatures where no diffusion into the Si is expected, suggests that it is solely related to the property of the interface between the Si and the pure dopant deposition.

On the applications side, this thesis work has been directed towards the very challenging feat of fabricating Ge avalanche photodiodes (Ge APDs) on Si substrates. The ability of growing crystalline Ge-on-Si together with the pure dopant deposition technology both in one single ASMI Epsilon 2000 reactor has generated the idea of merging the above techniques to fabricate high quality ultra-

shallow junctions on Ge-on-Si: in one deposition cycle first 1 μm of As-doped Ge is grown selectively on Si. Then, for the implementation of an ultrashallow junction, the process is followed by a sequence of PureGa and then PureB depositions, to form a pure dopant junction on the n-type Ge-islands. Early studies show that PureGa itself is enough to form the ultrashallow junction; however, it doesn't guarantee a reliable contacting after metallization. In contrast, PureB does not create an effective p^+-region on Ge as it does on Si, but it is useful here for creating a barrier layer on top of Ge junction that protects the Ga/Ge from oxidation when exposed to air and form aluminium spiking during metallization. The term PureGaB is introduced for this PureGa/PureB layer stack. The I-V characterization of the fabricated p^+n diodes (with uniquely a low saturation current and clear breakdown) gives a clear confirmation that the resulting diode quality is suitable for implementation of Ge-on-Si photodetectors that can be operational in avalanche or even single-photon avalanche modes. The prototype of the Ge-on-Si photodiodes show good sensitivity to infrared light as compared to visible light and also show dark count rates (DCR) of less than 80 kHz when biased in breakdown for single photon counting (Geiger mode).

Samenvatting

Heterogene integratie van III-V halfgeleiders met silicium (Si) technologie is van belang om on-chip de voordelen van zowel *fotonische* als *elektronische* hoge-snelheidscomponenten te kunnen gebruiken. Terwijl Si nog steeds het dominerende materiaal is voor het gebruik in hoge-snelheidselektronica, spelen de aantrekkelijkere fotonische functionaliteit van andere halfgeleiders (III-Vs, Ge,) een steeds belangrijkere rol in de fotonica-industrie. Het werk dat gepresenteerd wordt in deze thesis is voornamelijk genitieerd met het doel de III-V halfgeleider technologie met Si technologie samen te brengen. De focus werd aanvankelijk gelegd op de ontwikkeling van een met Si verenigbaar gereedschap voor Metal Organic Chemical Vapor Deposition (MOCVD) van galliumarsenide (GaAs). Hiervoor is een Si/SiGe CVD reactor, de ASMI Epsilon 2000, uitgebreid met een TriMethyl-Gallium (TMGa) bubblersysteem met extra buizen om de depositie van zowel GaAs als de standaard Si en SiGe deposities toe te staan. Voor de conventionele CVD van GaAs worden er hoge concentraties gassen gebruikt. Deze hoge concentraties, met name de uiterst giftige gassen arsine (AsH_3) en fosfine (PH_3), geven aanleiding tot het handhaven van strenge veiligheidsvoorschriften voor het gebruik van een MOCVD systeem. Van groot belang was het toepassen van een hele lage arseenconcentratie (AsH_3): 0.7%, een minstens tien keer zo lage hoeveelheid als gebruikelijk in MOCVDs. De bijbehorende lage concentratie van TMGa betekent dat de vervuiling van de reactor kamer met gallium of arseen zo laag is dat de standaard hoge kwaliteit van laaggedoteerd Si- en SiGe-deposities nog steeds kan worden behaald met dezelfde CVD reactorkamer. Hierdoor nam het onderzoek een unieke richting om devices te creren waar de samenvoeging van materialen zoals gallium (Ga), arseen (As) en boor (B), met Si en Ge, in een enkele reactor, een onmisbare factor is.

De meest volwassen III-V halfgeleider is GaAs, wat de basis vormt van een wereldwijde industrie ter grootte van enkele miljarden dollars voor hoge-snelheid elektronische en fotonische technologien. Epitaxie groeitechnieken spelen een belangrijke rol in deze industrie. In deze thesis wordt voor het eerst de GaAs epi-

taxie in een Si/SiGe CVD reactor gepresenteerd. Gezien de lage concentratie van het AsH_3 gas, lag de grootste uitdaging bij de stoichiometrie van Ga en As. Door de precieze controle van de gasstroom, de depositietemperatuur (650°C) en de druk (107 mbar) werd een uitstekend stoichiometrisch intrinsieke en gedoteerde GaAs-epitaxie bereikt met een groeisnelheid van 5 nm/min. Twee mogelijkheden voor het doteren van GaAs binnen de ASMI Epsilon 2000 CVD reactor zijn Si en Ge, beide zijn welbekende n-type onzuiverheden voor GaAs. Het was mogelijk om Si-gedoteerde en Ge-gedoteerde GaAs epitaxieaal te groeien met de doteringshoeveelheid van respectievelijk $5{\times}10^{17}$ atomen/cm^3 tot bijna 10^{20} atomen/cm^3 en van 10^{19} atomen/cm^3 tot $5{\times}10^{20}$ atomen/cm^3. Een van de doelen voor het opzetten van een proces voor stoichiometrische GaAs epitaxie was een methode te ontwikkelen voor het groeien van kristallijn GaAs op Si. Dit is een grote uitdaging vanwege de roosterongelijkheden tussen GaAs en Si kristallen en het samengestelde karakter van GaAs. De eerste resultaten lieten ruwe oppervlakken van polykristallijn GaAs zien, zelfs wanneer een goede selectiviteit van de groei op Si, gemaskeerd door SiO_2 werd geobserveerd in het geval van met patroon voorziene Si substraten.

Om gebieden te creren met een betere GaAs roosterovereenkomst is de selectieve groei van Ge op Si onderzocht. Ge is geen samenstelling van meerdere materialen, dus de groeicondities waren minder critisch dan voor GaAs. Ook is het Ge zelf een fotonisch interessant materiaal dat veelal wordt gebruikt in infrarood (IR) opto-elektronica. De kwaliteit van het kristallijn Ge-op-Si dat gegroeid wordt is sterk afhankelijk van de gekozen condities. De temperatuur moet hoog genoeg zijn om een chemisch wenselijke reactie toe te staan, hetgeen ervoor zorgt dat de Ge atomen samenkomen in een enkel kristal. Een druk van 27 mbar en groeitemperaturen van 550°C tot 700°C zorgden voor een goede kwaliteit Ge-op-Si met hoge selectiviteit. De Ge-op-Si resultaten zijn bestudeerd door middel van plane-view en cross-sectional transmission electron-microscopy (TEM) en atomic-force microscopy (AFM). Op 550°C zorgt de selectieve groei voor de formatie van Ge-eilanden op Si, met facetten langs het [311] vlak, en een aantal dislocatiedefecten werd geobserveerd binnen het Ge. Hiertegenover worden op 700°C de meeste roostermisplaatsingdefecten gevangen binnen de eerste 200 nm van het Ge groeiproces en daarom is kristallijn Ge van goede kwaliteit (defectdichtheid van 10^7 cm^{-2}) met een glad en plat oppervlak (oppervlakte ruwheid van 2 nm piek tot piek) binnen een laagdikte van ongeveer 1 μm in openingen tot honderden μm^2. De dotering van het Ge was bereikt met in-situ As en B dotering met respectievelijk maximale concentraties van $2{\times}10^{19}$ atomen/cm^3 en $3{\times}10^{18}$ atomen/cm^3. Hiermee, om de potentie van Ge-op-Si te kunnen bestud-

eren als een onderlaag voor GaAs epitaxie, zijn selectieve groeicycli ontwikkeld om GaAs direct te groeien boven op de Ge-op-Si eilanden en werd hiermee een goede kwaliteit GaAs epitaxie bereikt.

Behalve de halfgeleiderdeposities van GaAs en Ge, is ook het fabricatieproces van zeer ondiepe juncties met pure doteringsmiddeldeposities bestudeerd waar de optie om puur Ga te deponeren een nieuwe mogelijkheid biedt door de uitbreiding van de ASMI Epsilon 2000 met een TMGa bron. Het verkrijgen van een abrupt en hoog-gedoteerd ultra ondiep profiel in halfgeleider substraten is lastig, aangezien de resultaten van standaard doteringsmethodes zoals diffusie en ion implantatie gelimiteerd zijn door de toegepaste thermische behandelingen voor doteringsinbouw en -activatie. De depositie van puur boor (PureB) is in het verleden een interessante manier gebleken om zeer ondiepe (nanometer dikte) p^+n juncties met uitstekende elektrische eigenschappen gecombineerd met elektrische en optische robuustheid te verkrijgen. De depositie van puur Ga (PureGa) op 400°C op Si substraten heeft tot even goede elektrische resultaten geleid. Gebaseerd op het experimentele bewijs wordt er aangevoerd dat zowel PureB als PureGa een praktisch complete oppervlaktedekking van acceptortoestanden op Si als een interface-eigenschap wordt gevormd. De resulterende p^+n Si-diodes die een paar nm diep zijn, laten een ideaal gedrag zien met verzadigingsstromen van zo laag als die typerend zijn voor diepe juncties. Van essentieel belang is het effectieve hoge Gummelgetal van de PureB en PureGa gebieden, wat kan worden genterpreteerd als een grote hoeveelheid gaten per volume-eenheid. Dit zorgt voor lage verzadigingsstromen ondanks de geringe diepte van de juncties. De PureB fotodiodes waren zodanig ver ontwikkeld door de Silicon Device Integration groep van de Technische Universiteit Delft voor een scala aan toepassingen: groot oppervlakte, zeer lineaire varactor diode technologie, deep ultraviolet (DUV), extreme ultraviolet (EUV) en vacuum ultra-violet (VUV) fotodiodes en lage-energie (minder dan 1 keV) fotodiodes. PureGa, daarentegen, was ontwikkeld in de context van deze thesis. Het fundamentele voordeel van PureGa vergeleken met PureB is de lagere reactietemperatuur met Si (400°C). Daarom wordt PureGa een aantrekkelijk alternatief voor PureB, wat bij voorkeur wordt gedeponeerd op 700°C om the meest betrouwbare uniforme laag te verkrijgen. Zowel de I-V karakteristieken en omtrek/oppervlakte stroomanalyse van PureGa-diodes als de Gummel plots van gefabriceerde laterale pnp-transistoren met PureGa emitters/collectors laten allemaal een hoge gat-injectie van het PureGa-gebied in het n-Si zien. Dit elektrisch gedrag lijkt erg op dat van PureB-diodes, die, samen met het feit dat het optreedt bij lage temperatuur waar geen diffusie in het Si wordt verwacht, erop duiden dat het enkel is gerelateerd

aan de eigenschap van het interface tussen het Si en de pure doteringsdepositie.

Aan de kant van de toepassingen is deze thesis gericht om de zeer uitdagende verrichting om Ge avalanche-fotodiodes (Ge APDs) te fabriceren op Si substraten. Het vermogen om kristallijn Ge-op-Si te groeien samen met de pure doteringsdepositietechnologie in een enkele ASMI Epsion 2000 reactor heeft het idee gegenereerd om de bovenstaande technieken samen te voegen om zeer ondiepe juncties op Ge-op-Si van hoge kwaliteit te fabriceren. In een enkele depositiecyclus wordt eerst 1 m As-gedoteerd-Ge selectief gegroeid op Si. Daarna, voor de implementatie van een zeer ondiepe junctie, wordt het proces gevolgd door een reeks van PureGa en dan PureB deposities om een pure doteringsjunctie te vormen op de n-type Ge-eilanden. Eerdere studies wijzen uit dat PureGa op zichzelf genoeg is om een zeer ondiepe junctie te vormen. Echter, het garandeert geen betrouwbaar contact na metallisatie. PureB, daarentegen, creëert geen effectief p^+-gebied op Ge zoals het wel doet op Si, maar het is hier nuttig om een protectielaag te vormen bovenop de Ge-junctie die het Ga/Ge beschermt tegen oxidatie wanneer het wordt blootgesteld aan lucht en het vormen van aluminium pieken tijdens metallisatie. De term PureGaB is gentroduceerd voor deze PureGa/PureB-opeenstapeling. De I-V-karakterisering van de gefabriceerde p^+n-diodes (met een unieke combinatie van een lage verzadigingsstroom en een duidelijke breakdown) geeft een duidelijke bevestiging dat de resulterende diodekwaliteit bruikbaar is voor de implementatie van Ge-op-Si fotodetectoren die kunnen werken in avalanche of zelfs single-photon avalanche modes. Het prototype van de Ge-op-Si fotodiodes laat goede gevoeligheid voor infrarood licht zien in vergelijking met zichtbaar licht en laat ook dark count rates (DCR) van minder dan 80 kHz zien wanneer het wordt aangestuurd in breakdown voor het tellen van enkele fotons (Geiger modus).

List of Publications

Journal papers

- L. K. Nanver, **A. Sammak**, V. Mohammadi, K. R. C. Mok, L. Qi, A. Šakić, N. Golshani, J. Derakhshandeh, T. M. L. Scholtes and W. B. de Boer "Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices", *Electro-Chemical Society (ECS) Transactions*, vol. 49, No. 1, pp. 25-33, sept. 2012.

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