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Voltage Balancing in Series-Connected GaN Devices Using Scalable Transformer-Coupled Gate Driver

SOHRAB GHAFOOR [1] (Student Member, IEEE), REZA MIRZADARANI [1] (Student Member, IEEE), HITESH DIALANI [1] (Student Member, IEEE), PETER VAESSEN [1,2] (Member, IEEE), AND MOHAMAD GHAFFARIAN NIASAR [1] (Member, IEEE)

[1]Delft University of Technology, CD 2628 Delft, The Netherlands
[2]KEMA Laboratories, DE 6812 Arnhem, The Netherlands

CORRESPONDING AUTHORS: SOHRAB GHAFOOR; MOHAMAD GHAFFARIAN NIASAR (e-mail: s.ghafoor-1@tudelft.nl; M.GhaffarianNiasar@tudelft.nl).

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ABSTRACT This article presents a scalable transformer-coupled open-loop gate-driving technique that enables voltage balancing across series-connected GaN devices. High-voltage pulse generation with short rise times at kilovolt levels is a significant challenge. Conventional solid-state devices such as insulated-gate bipolar transistors and SiC metal–oxide–semiconductor field-effect transistors, though capable of high blocking voltages, are limited in switching speed and cannot reach the nanosecond regime. Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) due to their lateral structure offer low gate charge and ability to switch faster than 50 V/ns, are an attractive potential candidate. However, due to their lateral architecture, GaN HEMTs also have limited voltage-blocking capability, with most commercially available GaN power devices rated up to approximately 650 V, limiting their direct use in fast high voltage waveform generation at kilo-volts level. Series-connecting GaN devices can overcome this limitation but introduces severe voltage-balancing challenges, as even minor gate-signal mismatch at nanosecond timescale can cause destructive imbalance. Conventional closed-loop balancing methods, are difficult to implement at GaN switching speeds due to feedback latency. This article presents a simple open loop technique for driving GaN devices in series with a transformer-coupled gate driver. The proposed gate drive ensures simultaneous turn-ON/OFF with identical gate signals across all devices. An ultrafast full-bridge GaN based inverter excites wideband gate-drive transformers designed to preserve the ultrafast transition speeds of individual devices, while providing high-voltage isolation and near-equal voltage sharing establishing a scalable solution. Experimental results with two series-connected GaN HEMTs confirm nearly balanced voltage sharing at 1 kV across varying loads and currents.

INDEX TERMS High-voltage switch, isolated gate driver, nano pulse generation, series-connected gallium nitride (GaN), voltage balancing.

NOMENCLATURE

2DEG	Two-dimensional electron gas.
AlGaN	Aluminum gallium nitride.
C_r	Compensation capacitance.
C_{iss}	Input capacitance of FET ($C_{gs} + C_{gd}$).
C_{oss}	Output capacitance ($C_{ds} + C_{gd}$).
C_{rss}	Reverse transfer capacitance.
DUT	Device under test.
dV/dt	Rate of voltage change.
di/dt	Rate of current change.
FET	Field effect transistor.
GaN	Gallium nitrite.
HEMT	High electron mobility transistor.
H-Bridge	Full-bridge switching circuit topology.

IGBT	Insulated-gate bipolar transistor.
k	Coupling factor.
kV	Kilovolt.
L_{xx}	Transformer self-inductances
M_{xx}	Transformer mutual inductances.
MOSFET	Metal–oxide–semiconductor field-effect transistor.
PWM	Pulsewidth modulation.
SiC	Silicon carbide.
TVS	Transient voltage suppressor.
V_{gs}	Gate-to-source voltage.
V_{ds}	Drain-to-source voltage.
$V_{gs(\text{th})}$	Threshold gate voltage.
V_B	Breakdown voltage.
ΔV	Static voltage imbalance.
WBG	Wide bandgap (semiconductor technology).

I. INTRODUCTION

Solid-state devices like IGBTs and MOSFETs are widely used in high-voltage pulse generators, offering longer lifetime, lower losses, compact size, high repetition rates, and improved control compared to traditional spark-gap switches [1]. However, these switches have relatively slow rise times, preventing the generation of ultrafast high voltage nano pulses. Wide-bandgap (WBG) devices are being increasingly adopted in power electronics because of their superior electrical and thermal performance, reduced switching and conduction losses, and higher efficiency [1]. Among them, GaN HEMTs, owing to their lateral device structure offering six times lower gate charge than SiC and nearly fifty times lower than Si power devices [2], [3], [4] can enable the generation of high-voltage arbitrary waveforms with ultrafast rise times. GaN HEMTs offer a practical alternative to Si/SiC MOSFETs in high-power-density applications, enabling MHz-range switching, smaller device size, higher power density, and improved efficiency through lower switching energy and reduced reverse recovery losses. However, Their low gate threshold and maximum voltages (typically below 6–10 V), channel-based reverse conduction, extremely small input capacitance, and high dv/dt capability demand precise, low-delay gate drivers for reliable high-speed operation [5], [6].

Structurally, Si and SiC MOSFETs employ a vertical current conduction mechanism, whereas GaN HEMTs utilize a lateral device structure in which current flows through a 2DEG formed at the AlGaN/GaN interface [5], [6], [7], as illustrated in Fig. 1. This unique structure enables high charge density and electron mobility, resulting in superior switching performance. However, it also inherently limits the voltage rating of commercially available GaN devices to approximately 650 V [8], [9].

Although various approaches have been explored to extend the voltage capability of GaN HEMTs beyond this limit, such as the use of field plates and other structural modifications, these solutions typically introduce additional parasitic capacitances and increased switching losses, thereby compromising the intrinsic advantages of GaN technology [10]. While future developments may enable higher voltage GaN devices, such designs may not fully exploit the key benefits of GaN, including ultrafast switching and low on-resistance.

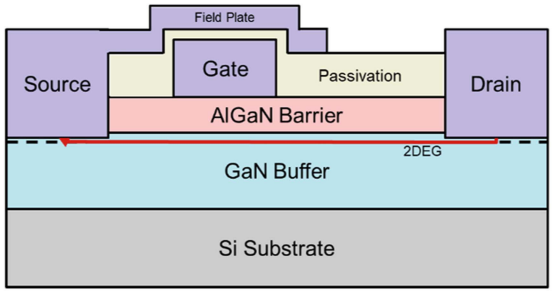


FIGURE 1. Basic lateral structure of a GaN FET [6].

Consequently, the same device structure that provides GaN with its superior performance also constrains its voltage blocking capability, limiting its direct applicability in generating ultrafast, nanosecond-scale high-voltage pulses in the kilovolt range capabilities that are essential for advanced high-voltage testing of grid assets. This need of fast voltage rise is further emphasized by standardized immunity tests, such as Electrical Fast Transient/Burst (EFT/B, IEC 61000-4-4) and Electrostatic Discharge (ESD, IEC 61000-4-2), which involve voltage transients with nanosecond-scale rise times, thereby underscoring the growing demand for ultra-fast high-voltage switching solutions.

A. TRANSFORMER COUPLED GATE DRIVING OF SERIES-CONNECTED GAN DEVICES

The exceptional switching speed of GaN devices, combined with their limited voltage blocking capability, motivates the series connection of multiple low-voltage GaN HEMTs to enable ultrafast, high-voltage pulse generation using cost-effective, commercially available devices [11]. Prior studies show that series-connected devices can achieve lower on-resistance and higher current density than a single high-voltage switch [12], while the specific on-resistance of power devices increases sharply with breakdown voltage ($R_{DS(\text{on})} \propto V_B^{2.3-2.5}$), limiting the practicality of high-voltage SiC MOSFETs for medium-voltage, high-power application [13].

A major challenge of series-connected topologies is unequal voltage sharing, which can cause inefficient utilization or catastrophic device failure. Voltage imbalance arises from parasitic mismatches, external capacitive coupling differences, and, most critically, mismatched gate signals [14]. Even a few nanoseconds of gate delay can result in severe imbalance, with delays as small as 4 ns causing up to 40% voltage deviation [15], [16]. While static imbalance can be mitigated using high-value resistors across each device [17], dynamic imbalance is more complex and strongly influenced by asynchronous gate driving, including both timing delays and differences in dV_{gs}/dt slopes [14]. These effects are particularly severe in GaN HEMTs due to their extremely small

parasitic capacitances and very fast switching speeds exceeding 50 V/ns [5].

Conventional gate-driving approaches for series-connected GaN switches suffer from significant limitations. Isolated DC–DC supplies become impractical as the number of stacked devices increases, introducing propagation delays and synchronization issues [18]. Bootstrap-based nonisolated drivers reduce hardware complexity but still suffer from level-shifting delays and vulnerability to high-voltage transients that can exceed diode ratings [19].

To overcome these challenges, transformer-coupled gate-driver architectures have been proposed to synchronously drive series-connected devices using magnetic isolation [17], [20], [21]. This approach is highly scalable, as it eliminates complex level shifting and ensures synchronized gate currents across the stack. Scalability is primarily constrained by insulation requirements between the high-voltage secondary side and the low-voltage primary side, especially as stack voltages reach several kilovolts. Advanced dielectric materials such as polyimide, PTFE, and XLPE enable compact transformer designs while maintaining high isolation strength. However, conventional pulse-transformer drivers are inherently frequency-dependent and cannot support arbitrary duty cycles or long on/off durations, limiting their suitability for applications requiring precise pulse control, such as high-voltage testing [2], [22].

To address this limitation, this work extends the dual-transformer concept introduced in study [23], enabling user-programmable switching frequency and duty cycle while maintaining synchronized and fail-safe operation of series-connected GaN HEMTs. Furthermore, achieving high-speed operation requires careful optimization of the transformer-coupled gate driver. The achievable rise time is dominated by the primary-side switching frequency, transformer inductances and coupling coefficient, compensation capacitance, and the fixed intrinsic gate capacitance of the GaN devices [24], [25]. Instead of complex resonant excitation schemes such as E-class oscillators [26] this work employs a simple GaN-based full-bridge primary stage to generate ultrafast square pulses, combined with optimized transformer design and compensation networks to preserve sharp voltage transitions on the secondary side.

Overall, optimized transformer-coupled gate drivers with GaN-based ultrafast excitation enable scalable, compact, and efficient high-voltage switching solutions while retaining the intrinsic speed advantages of low-voltage GaN devices.

B. PAPER CONTRIBUTION

Unlike conventional Si or SiC devices, GaN's lateral structure offers superior switching speed and efficiency but limits its voltage blocking capability. To overcome this limitation while preserving GaN's high-speed advantages, a scalable, magnetically isolated gate-driving scheme is developed to synchronize gate currents across multiple series-connected devices.

This article presents a simple open loop transformer-coupled gate driver architecture enabling the nearly even voltage distribution across the series connection of low-voltage GaN HEMTs for fast high-voltage pulse generation.

Contrary to the complicated high frequency oscillation circuits, the article has shown the utilization of a simple GaN-based full-bridge excitation circuit with an optimized L_3C_2 resonant compensation network, achieving minimal propagation delay and precise gate charge control.

The article identifies and analyzes the transformer parameters that must be optimized to effectively transfer the ultrafast switching capability of a GaN based excitation circuit from the primary to the secondary side. Using an L_3C_2 equivalent circuit framework supported by comprehensive MATLAB/Simulink simulations based on a mutual-inductance model with one primary and four secondary windings, the study has elaborated the dual resonant behavior of the transformer circuit and derives the resonance conditions and leakage-inductance relationships that define the impedance plateau and operational bandwidth. The results further illustrate the influence of each resonant element (L_1–L_5, C_r, C_{iss}, and coupling) on circuit behavior, ultimately establishing practical design guidelines that ensure operation within the impedance plateau so that the gate capacitance of series-connected GaN HEMTs can be fully charged within the first pulse.

Furthermore, the article has highlighted that probe compensation is critical for normal gate drive operation and reproducibility of the experimental results. Moreover, high-bandwidth probes and appropriately rated oscilloscopes are necessary to accurately capture the nanosecond-scale rise times and MHz-range switching of series-connected GaN devices.

The article has also addressed the switch overshoot problem which is very prominent with ultrahigh switching speed of GaN by minimizing the loop inductance and utilizing the noninductive nonwire wound thick film resistors [27].

The article has shown experimental validation confirming nearly even voltage sharing among two series-connected GaN HEMTs up to 1 kV with different loads and associated currents, demonstrating open-loop transformer coupled gate driver's effectiveness in driving series connected GaN Devices.

The proposed method establishes a practical path for extending GaN's high-speed, high-efficiency performance into the kilovolt regime, enabling simple, compact and cost-effective solid-state switches for future pulsed power systems, dielectric testing, and advanced power electronic applications.

To provide a structured overview, this article is organized into several sections. Section II summarizes the advantages and limitations of the voltage balancing techniques for series connected switching devices. It briefly discusses previously employed techniques to achieve voltage balancing across series connected GaN devices in particular. Section III provides a comprehensive description of the transformer-coupled gate driving technique with the high-frequency excitation circuit to

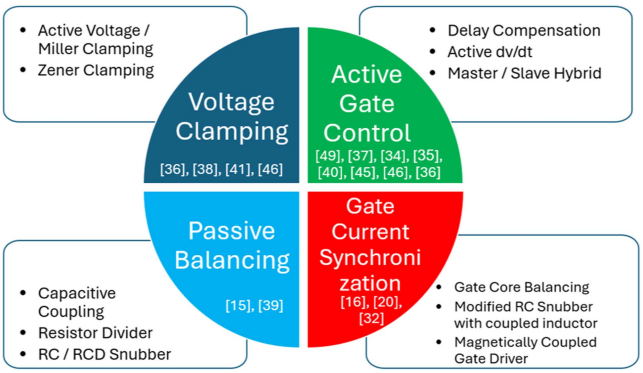


FIGURE 2. **Overview of voltage balancing techniques.**

drive series connected GaN devices. Section IV presents simulation results illustrating the impact of gate-signal mismatch and intrinsic device capacitance variations on dynamic voltage sharing. It further analyzes the translation of the GaN half-bridge switching voltage to the transformer secondary-side gate voltage. In addition, the section examines the influence of transformer parameters on switching speed and provides explicit design guidance on the selection of the resonant compensation capacitor and the choice of switching frequency for reliable operation across the transformer, along with detailed transformer design considerations. Section V focuses on the experimental setup, the measurements performed, and the analysis of the obtained results, along with key observations drawn from the experiments. Finally, Section VI offers a concise summary of the findings and concludes the research, emphasizing the contributions and implications of this work.

II. VOLTAGE BALANCING TECHNIQUES FOR SERIES CONNECTED DEVICES

A detailed review of the literature on voltage-balancing strategies [15], [17], [18], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45] indicates that optimization techniques for both static and dynamic balancing can generally be classified into four major groups: voltage clamping, passive balancing, active gate control, and gate current synchronization. Fig. 2 attempts to consolidate these approaches.

A. VOLTAGE CLAMPING METHODS

Voltage clamping methods [32], [34], [37], [42] employ auxiliary components such as clamping diodes, varistors, or snubber circuits to restrict the voltage stress across individual devices. These methods are relatively simple to implement and cost-effective since they require no additional isolation circuitry. However, they suffer from inherently high switching losses because the clamping elements repeatedly absorb excess energy. Moreover, their response time to fast transients is limited, making them less effective in applications requiring precise dynamic voltage balancing.

B. PASSIVE BALANCING METHODS

Passive balancing methods [15], [35] typically rely on resistors or RC snubber networks to equalize voltage sharing among series devices. Similar to clamping methods, these techniques do not provide galvanic isolation and therefore have limited flexibility in high-voltage applications. They also introduce additional static and dynamic power losses, which reduce system efficiency. On the other hand, passive balancing offers a relatively good transient response, making it useful in certain medium-voltage, moderate-speed switching scenarios .

C. ACTIVE GATE CONTROL METHODS

Active gate control methods [30], [31], [32], [33], [36], [41], [42], [46] improve upon the limitations of passive techniques by dynamically adjusting the gate signals of the series-connected devices. This approach provides good isolation, low switching losses, and excellent dynamic balancing performance. Nevertheless, the control strategy is significantly more complex, requiring high-speed feedback loops, advanced driver circuitry, and precise coordination of multiple gate signals. Furthermore, as the number of series devices increases, the complexity and cost of the system grow disproportionately, making scalability a key drawback.

D. GATE CURRENT SYNCHRONIZATION METHODS

Gate current synchronization methods [17], [28], [44] represent a promising solution for series-connected wide-bandgap devices. By magnetically or capacitively coupling the gate drive currents, these methods inherently synchronize the switching transitions of all devices in the stack. They offer strong isolation, very low switching losses, and excellent dynamic response. In addition, the control strategy is comparatively simple, and the method scales efficiently to a large number of devices, making it attractive for ultrahigh-voltage applications. The primary challenges lie in designing high-quality coupling elements and ensuring insulation reliability at extreme voltage levels, but overall, this approach combines the benefits of efficiency, scalability, and robustness better than the other groups.

A brief comparison chart of these techniques is shown in Table 1. From the comparative evaluation, it is evident that voltage clamping and passive balancing methods are attractive for their simplicity and low cost, but their lack of isolation and inherently high switching losses limit their use to relatively low or medium voltage applications. Active gate control, while capable of delivering precise dynamic balancing with reduced switching losses, introduces significant control complexity and poor scalability, restricting its practicality to systems with only a few devices operating at high frequency. The most recent advancements in GaN dynamic voltage balancing have been reported in [47] and [48]. These approaches rely on closed loop active gate current control techniques for balancing, offering a promising solution for improved dynamic performance.

TABLE 1. Comparison Chart of Voltage Balancing Methods for Series-Connected MOSFETs

	Voltage Clamping	Passive Balancing	Active Gate Control	Gate Current Synchronization
Principle	Limits voltage stress using energy-absorbing components	Equalizes voltage via passive networks	Dynamically adjusts gate signals for each device	Synchronizes gate drive currents to align switching transitions
Typical Components	Clamping diodes, varistors, snubber circuits	Resistors, RC snubbers	Active gate driver with feedback, variable gate voltage or impedance	Magnetic or capacitive coupling between gate drives
Isolation	None	None	Yes	Yes
Switching Losses	High (Energy dissipation in clamping elements)	High (Static & Dynamic losses)	Low	Very low
Dynamic Response	Moderate	Moderate to Good	Excellent	Excellent
Control Complexity	Low	Low	High (Requires coordination and feedback loops)	Low
Scalability	Moderate	Moderate	Limited (Grows complex with device count)	High
Key advantages	Low cost and easy to implement	Simple, stable, decent transient behavior	Precise control, efficient, good isolation	High efficiency, strong isolation, easy scalability
Main Limitations	Poor transient response, energy losses, limited to moderate voltage	Inefficient at high frequency, limited voltage scalability	High cost, complexity, synchronizati on required	Design of coupling components and insulation reliability is critical
Best suited applications	Low voltage & low frequency systems where cost is main concern	Medium voltage and moderate speed converters	High frequency converters with small number of devices	High voltage multi kV systems

However, the techniques remain iterative in nature and are therefore unable to guarantee instantaneous voltage balancing across devices. This limitation can lead to scenarios where, if the time or current resolution is insufficient, a control failure can occur, resulting in uneven device stress leading to one or more device failure. Furthermore, neither study sufficiently addressed the problem of voltage overshoot, which is critical in high-speed GaN switching due to the devices' low capacitances and extremely fast transient response. Thus, while these methods represent significant progress, few challenges remain to be addressed before they can be adopted as robust solutions for developing high-voltage switch using series-connected GaN devices.

In contrast, open-loop gate current synchronization techniques offer the most balanced tradeoff combining high isolation, low losses, simple control, and excellent scalability making them a very prominent candidate for driving GaN devices connected in series. A comparative analysis of different gate-driver topologies presented by the authors in study [24] demonstrates that magnetically isolated drivers offer a cost-effective and straightforward option for high-frequency operation (2.5–50 kHz) at voltages above 8 kV, especially in cases involving a large number of series-connected devices.

III. PROPOSED BALANCING TECHNIQUE

A. CIRCUIT DESCRIPTION

To address the limitations of existing voltage balancing techniques across series connected GaN HEMTs, a programmable open loop gate current synchronizing driver is designed with a transformer-coupled system to achieve matching gate signals and high-voltage isolation. Fig. 3 illustrates the block diagram of the proposed gate driver architecture, which is categorized into primary-side and secondary-side sections. On the primary side, two single-turn, high-voltage insulated loops are employed for turn-ON and turn-OFF operations, each driven with ±24 V bipolar pulses generated by GaN based high-frequency full-bridge excitation circuits. These coils operate in complementary fashion to ensure proper switching action. The secondary side incorporates a gate charging and discharging circuit, enabling flexible switching functions for the series-connected GaN HEMTs.

For each GaN device in the series stack, two dedicated secondary coils are provided, one for turn-ON and the other for turn-OFF along with the gate charging and discharging control. The GaN-based full-bridge excitation circuit utilizes a 12V DC supply to power up its control circuitry, while the primary switching action is driven by a 24V DC input applied across its DC bus terminals, providing the necessary excitation voltage for the transformers.

It is pertinent to mention that the proposed open loop method is not intended to restore voltage balance once an initial imbalance has already occurred. Instead, it prevents the development of dynamic voltage imbalance during switching transients by minimizing gate signal and gate current mismatch among the devices, thereby maintaining stable voltage distribution under normal operating conditions.

B. CIRCUIT OPERATION AND TIMING SEQUENCE

The circuit operation starts with the user signal of turn on/off which is turned into streams of mutually exclusive digital gate pulses for turn on and turn off signal by the microcontroller. These streams of digital pulses then subsequently drive the high frequency GaN H Bridge to generate 24 V nearly square high frequency bipolar pulses on the primary side of the transformer. This produces around ±24 V bipolar pulses across either the turn-ON or turn-OFF single-turn loops, with only one coil active at a time. On the secondary side, a gate charging and discharging circuit is built with small-signal MOSFETs controlling the switching frequency and duty cycle of the series-connected GaN HEMTs, independent of the transformer's operating frequency. The detailed schematic

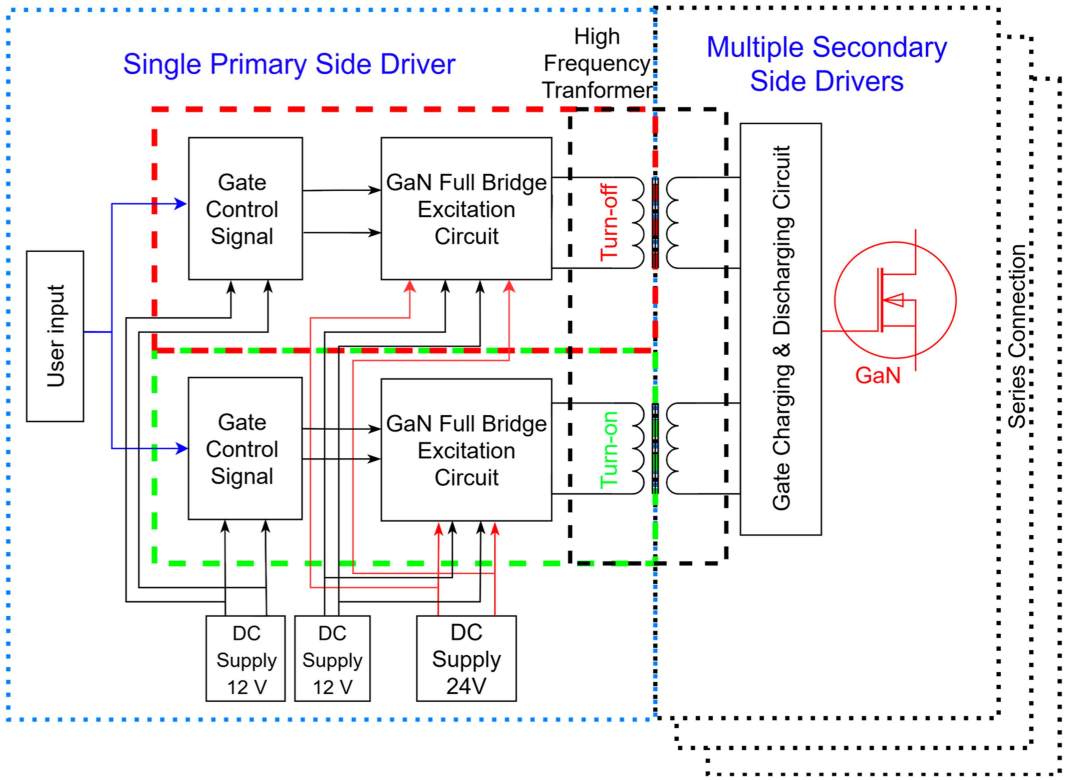


FIGURE 3. **Block diagram for the proposed scheme.**

is shown in Fig. 4 and its corresponding timing diagram is shown in Fig. 5.

During turn-on, the first rising voltage pulse charges the GaN's gate capacitance C_{iss} through Schottky diode D_3 to turn it ON. At the same time, the same pulse charges the small signal MOSFET M_2 which discharges the gate of MOSFET M_1 to turn it OFF. The turn OFF coil remains inactive during the turn on operation. Although fast dv/dt switching in the presence of gate-loop parasitic inductance can, in general, lead to gate-voltage overshoot and ringing, this effect is effectively mitigated in the experimental prototype. A TVS diode, which has faster response than typical Zener diode, is placed directly across the gate–source terminals to clamp the gate voltage during high dv/dt transitions, thereby limiting overshoot and suppressing oscillations induced by parasitic inductances. As a result, despite the presence of unavoidable gate-loop parasitics, the measured gate-voltage waveforms exhibit stable and well-controlled switching behavior.

For turn-OFF cycle, the turn OFF transformer is excited with fast bipolar pulses from GaN H bridge, which in turn generates a fast voltage pulse on the secondary side turning the small signal MOSFET M_1 on, immediately discharging the GaN gate capacitance C_{iss}, turning it effectively OFF. The turn ON coil remains stalled during the turn off operation cycle. In this way the secondary windings ensure rapid charge and discharge of relevant switch gates ensuring triggering of the series-connected GaN devices as per user defined digital input and preventing any false turn ON/OFF.

C. GATE CHARGING AND DISCHARGING MECHANISM FOR SERIES-CONNECTED GAN DEVICES

Fig. 6 illustrates the turn-ON operation of the switch, emphasizing the components responsible for activating the series-connected GaN HEMTs. The blue measurement probes correspond to the timing sequence presented in Fig. 5. During the positive half cycle, the signal passes through diode D_3 and is clamped by TVS Z_3 at +10 V, thereby charging the input capacitance C_{iss} of the GaN switch (GaN_1) to the gate voltage V_{gs3}, as shown in Fig. 6(a). When the input voltage falls below V_{gs3}, the diode D_3 becomes reverse-biased, halting current flow through the gate–source path as depicted in Fig. 6(b). The diode remains reverse-biased throughout the negative half cycle and resumes conduction once the input voltage exceeds V_{gs3} again. Throughout this interval, GaN switch remains in the on state. Simultaneously, the positive pulse from the transformer activates the small-signal MOSFET M_2, which discharges the gate of M_1 to maintain it in the off state. Once the gate capacitance of GaN_1 switch is fully charged, the device is completely turned ON, and the gate capacitance behaves as an open circuit.

Fig. 7 presents the components active during the turn-OFF phase of the series-connected GaN HEMTs. In this mode, the positive half cycle of the secondary is clamped by TVS Z_1 at +10 V, charging the gate capacitance C_{iss} of the small-signal MOSFET M_1 to gate voltage V_{gs1}, as illustrated in Fig. 7. The drain–source path of M_1 then discharges the gate charge of the GaN Switch (GaN_1), ensuring its rapid turn-off.

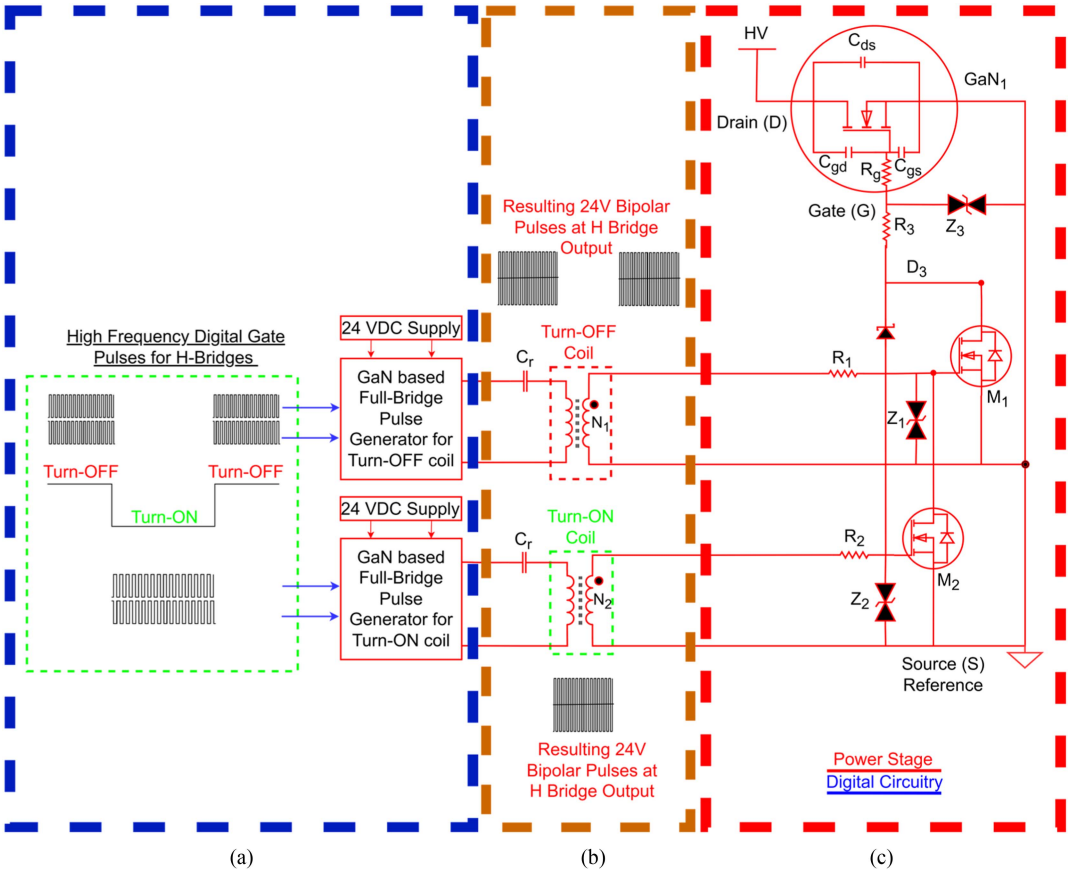


FIGURE 4. GaN based high-frequency excitation gate current synchronization driving circuit with programmable frequency and duty cycle. (a) Gate Drive and Control. (b) Transformer. (c) Gate Charging and Discharging Circuit.

This process occurs synchronously across all series-connected GaN devices, ensuring uniform gate voltages and simultaneous switching, which results in an even voltage distribution among all devices.

D. TRANSFORMER CORE DESIGN

The transformer toroidal core can be selected based on equations for core area (A), maximum magnetic flux density (B_m), and inductance (L), considering parameters like voltage (E), frequency (f), current (I), and the number of turns (N_p) using the following equations:

$$A = \frac{E}{k\, f\, B_m N_p} \tag{1}$$

$$B = \frac{LI}{NA} \tag{2}$$

$$L = \frac{BNA}{I}. \tag{3}$$

Reducing the number of transformer turns lowers leakage inductance; therefore, a single turn is used for the primary coil, with minimal turns for the secondary coils. The coupling coefficient is then calculated as follows [49]:

$$k = \sqrt{1 - \frac{L_1\,(S.C.L_2)}{L_1\,(O.C.L_2)}} = \frac{M}{\sqrt{L_1.L_2}} \tag{4}$$

Simulation results reveal that the rise time of the gate signal is strongly influenced by the transformer's inductances, the coupling coefficient, and the gate capacitance of the GaN HEMT. The gate capacitance of GaN devices is inherently very small compared to Si and SiC technologies and is fixed by the device, so it cannot be adjusted. Consequently, the design focus shifted to parameters that can be controlled, i.e., the transformer coupling and inductances. Specifically, a lower leakage inductance, a smaller gate capacitance, and a higher coupling coefficient all contribute to a faster rise in the gate voltage, which is crucial for rapid switching performance. By minimizing leakage inductance and maximizing coupling, the circuit achieves a fast gate voltage rise time, ensuring efficient turn-ON of the GaN HEMTs even at high switching frequencies. This approach allows the circuit to fully exploit the fast-switching capabilities of GaN devices while maintaining stable and predictable gate-drive behavior.

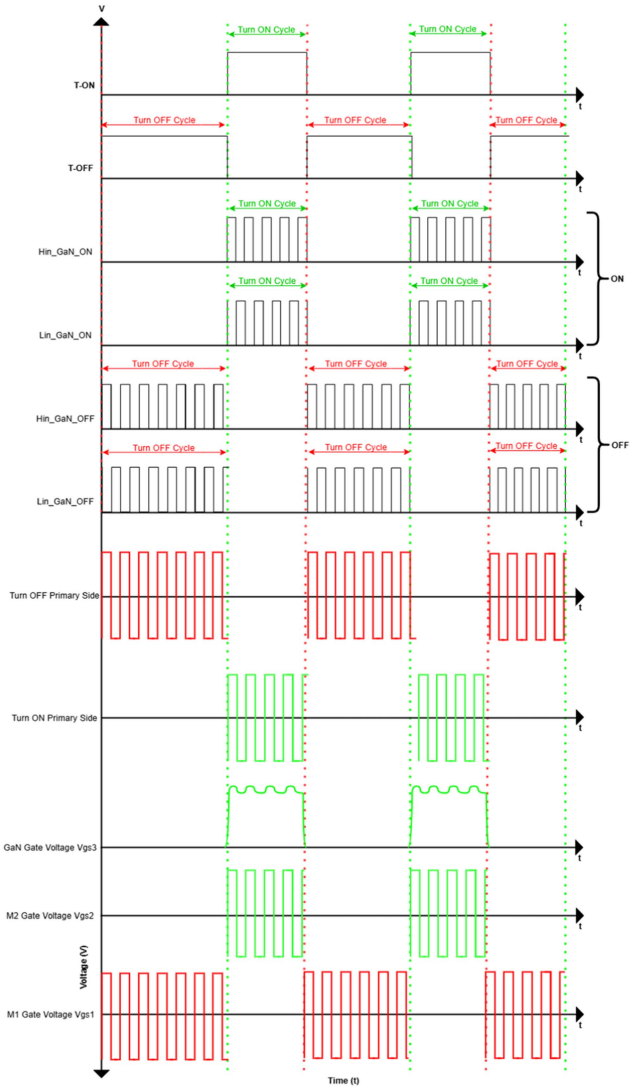


FIGURE 5. Detailed timing diagram for circuit presented in Fig. 4 where user defined on and off trigger signals are modulated into high-frequency complementary digital signals to drive the coil between the full bridge circuits.

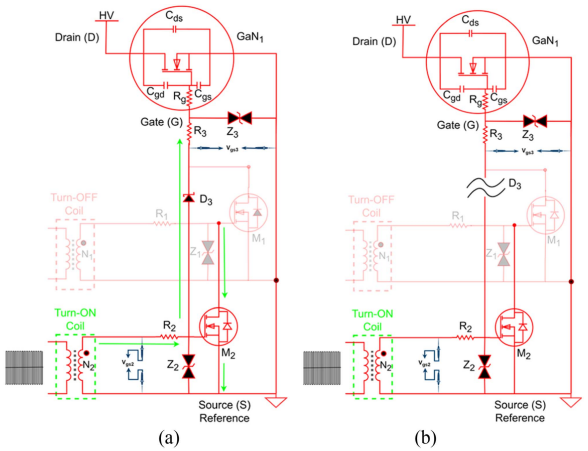


FIGURE 6. Turn-ON operation of series-connected GaN HEMTs showing M_2's synchronization with GaN_1 and control of M_1, with D_3 charging Ciss to turn GaN_1 ON (see timing diagram in Fig. 5). (a) Circuit during positive half voltage pulse. (b) Circuit during negative half voltage cycle.

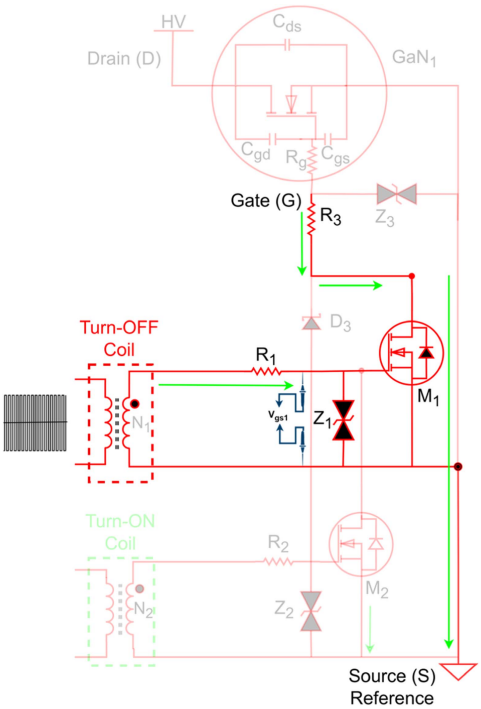


FIGURE 7. Active components in the secondary driver circuit during turn-OFF phase, illustrating operation as per timing diagram shown in Fig. 5.

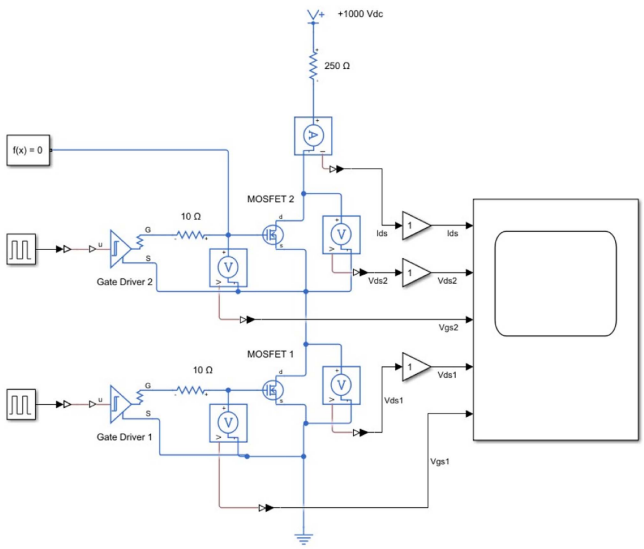
E. INTEGRATION AND FOOTPRINT OPTIMIZATION

The proposed transformer-coupled gate driver can be efficiently integrated by optimizing the transformer design, minimizing auxiliary components, and carefully arranging circuit tracks to reduce parasitic effects. These strategies have the potential to lower the overall footprint and manufacturing cost compared to conventional isolated power supply solutions, while preserving high-speed performance and synchronized gate signals.

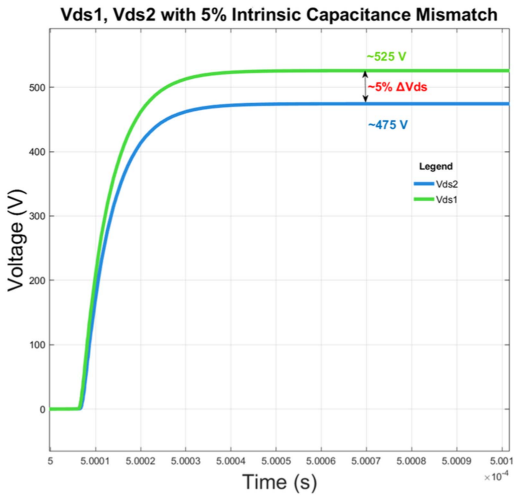
IV. SIMULATIONS

A. IMPACT OF INTRINSIC CAPACITANCE DIFFERENCE AND TIME DELAY ON DYNAMIC VOLTAGE IMBALANCE

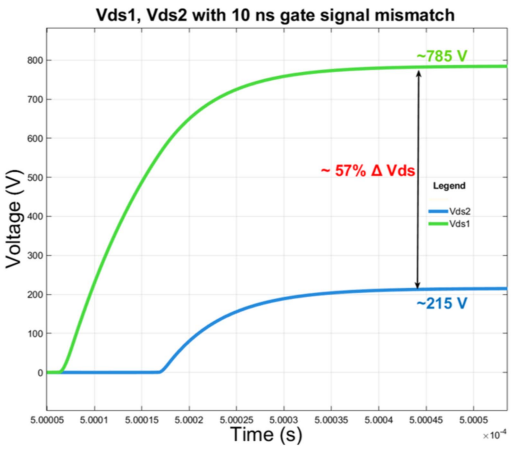
A simple MATLAB simulation shown in Fig. 8(a) is performed to elaborate the impact of intrinsic capacitance mismatch and gate signal mismatch on the dynamic voltage imbalance. It can be seen in Fig. 8(b) that with 5% difference in intrinsic capacitances, around 5% voltage imbalance occurs across two series connected devices. However, with a 10 ns delay among the series connected devices, a 57% voltage imbalance can be observed as shown in Fig. 8(c). These results demonstrate that gate signal timing mismatch has a far more severe impact on dynamic voltage imbalance than typical levels of intrinsic device parameter variation. In practice, intrinsic capacitance mismatch can be reduced by selecting devices from the same production batch [15].



(a)



(b)



(c)

FIGURE 8. (a) Simple MATLAB Simulink model to simulate the gate signal and intrinsic capacitance mismatch. (b) Voltage imbalance due to 10 ns gate signal mismatch. (c) Voltage imbalance due to 5% intrinsic capacitance mismatch.

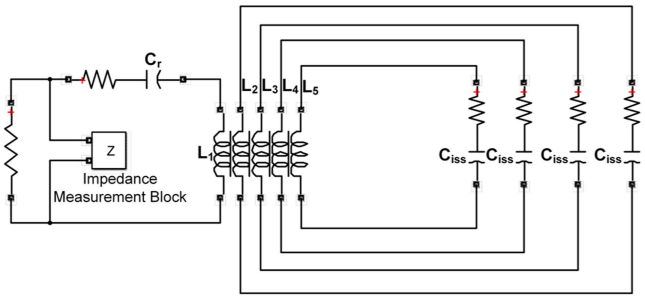


FIGURE 9. MATLAB Simulink model illustrating the primary-side impedance characteristics of a resonant transformer circuit.

The dominant source of dynamic voltage imbalance, gate signal mismatch is effectively mitigated by the proposed transformer-coupled gate driver, which provides highly synchronized gate-driving signals to series-connected devices.

B. L_3C_2 RESONANT NETWORK MODELING AND SIMULATION OF TRANSFORMER-COUPLED GATE DRIVERS

To mitigate transformer parasitics, a resonant compensation network is used [50], [51]. The primary side of transformer consists of a self-inductance L_1 in series with a capacitor C_r, while the secondary includes L_2, a rectifier diode, and the gate capacitance C_{iss} acting as the load. Together these elements form an L_3C_2 circuit with distinct resonant frequencies on both sides of the transformer. Fig. 9 shows the simplified compensation network and its equivalent L_3C_2 model. To analyze its behavior, a MATLAB simulation was designed using a mutual inductance model with one primary and four secondary windings. The study examined the resonant characteristics over a frequency range from a few kHz up to several MHz, with the diode modelled as a short circuit during conduction.

The transformer's mutual and self-inductances are represented in the inductance matrix L, initialized as follows:

$$L = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} & M_{15} \\ M_{21} & L_2 & M_{23} & M_{24} & M_{25} \\ M_{31} & M_{32} & L_3 & M_{34} & M_{35} \\ M_{41} & M_{42} & M_{43} & L_4 & M_{44} \\ M_{51} & M_{52} & M_{53} & M_{54} & L_5 \end{bmatrix}. \tag{5}$$

Here, L_1 denotes the self-inductance of the primary loop measured with the secondary side open, while L_2, L_3, L_4, and L_5 represent the self-inductances of the secondary windings, measured with the primary side open. Since the secondary toroidal cores are physically isolated and exert identical influence on the primary while having negligible coupling among themselves, the inductance matrix of the transformer can be simplified as follows:

$$L = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} & M_{15} \\ M_{12} & L_2 & 0 & 0 & 0 \\ M_{13} & 0 & L_3 & 0 & 0 \\ M_{14} & 0 & 0 & L_4 & 0 \\ M_{15} & 0 & 0 & 0 & L_5 \end{bmatrix}. \tag{6}$$

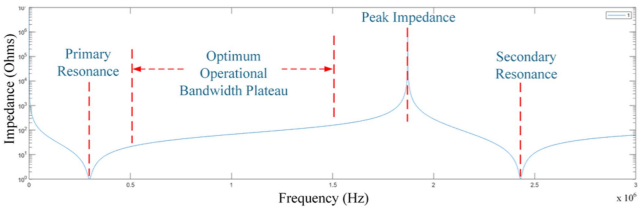


FIGURE 10. Simulated impedance response of the L_3C_2 circuit, exhibiting dual resonance peaks and indicating the optimal operating bandwidth.

The equivalent impedance of the L_3C_2 network, as derived in study [52], can be expressed as follows:

$$Z_{\text{eq}}(j\omega) = j\omega L_1 + \frac{1 - L_2 C_r \omega^2}{j\omega C_r (1 - \omega^2 L_2 C_{iss})}. \tag{7}$$

This representation highlights the dual-resonant nature of the circuit, where the primary and secondary sides resonate at different frequencies, producing a wide impedance plateau favorable for stable operation. The impedance response observed from the primary side, as shown in Fig. 10, reveals two distinct resonant frequencies. The primary resonance frequency is governed by the compensation capacitor C_r and the primary self-inductance L_1, and can be expressed as follows [52]:

$$f_p = \frac{1}{2\pi\sqrt{L_1 C_r}} \tag{8}$$

where f_p is the primary side resonance frequency, and L_1 denotes the self-inductance of the primary side.

On the secondary side, the circuit is connected to a capacitive load C_{load}, which represents the GaN's gate capacitance C_{iss}. Simulation results indicate that the secondary-side resonance frequency is governed by the interaction between the secondary leakage inductance L_{s-lk} and the load capacitance C_{load}, and is expressed as follows:

$$f_s = \frac{1}{2\pi\sqrt{L_{s-lk}\, C_{\text{load}}}}. \tag{9}$$

Due to the small gate capacitance C_{iss}, the secondary side exhibits a relatively high resonance frequency. The network shown in Fig. 11(a) can be simplified into the reduced L_3C_2 model illustrated in Fig. 11(b). For the case of a single secondary winding, the leakage inductance can be expressed as follows:

$$L_{s-lk-1} = L_2 - \frac{M^2}{L_1} \tag{10}$$

where $L_{s\text{-}lk\text{-}1}$ is the effective secondary leakage inductance with just one secondary winding, L_2 is the secondary side self-inductance, M is the mutual inductance between primary and secondary, and L_1 is the self-inductance of the primary side.

Adding each secondary winding changes the effective leakage inductance of the secondary according to the following

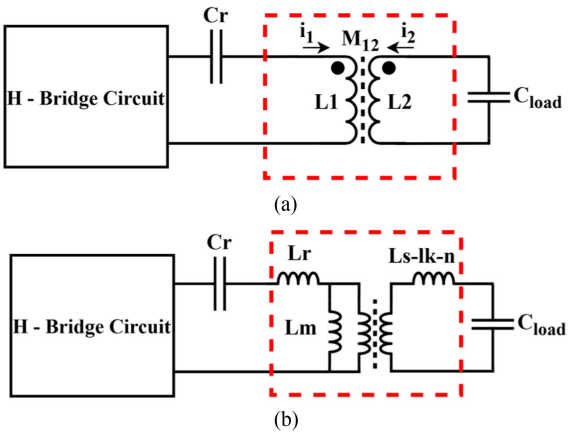


FIGURE 11. Simplified equivalent model of the resonant transformer circuit for analysis [51], [52]. (a) Resonant transformer showing self/mutual inductances, compensation, and load capacitors. (b) Equivalent circuit illustrating leakage and magnetizing inductances with associated capacitors.

relationship:

$$L_{s-lk-n} = L_2 - n\frac{M^2}{L_1} \tag{11}$$

where n is the number of secondary windings.

Equations (5) and (6) indicate that adding each secondary winding shifts the resonance frequency of the secondary side higher. They also reveal that the effective leakage inductance of the secondary which defines the resonance point of the secondary LC circuit is influenced not only by the mutual inductance but also by the self-inductance of the primary side.

It is pertinent to mention that the junction capacitance of the secondary-side diode and loop parasitic elements inevitably influence the secondary-side resonant frequency by modifying the effective circuit impedance. However, these effects primarily result in a shift of the resonant frequencies and do not alter the fundamental dual-resonant behavior of the transformer-coupled gate-driving circuit. Since the objective of the proposed approach is not to operate at a narrowly tuned resonant frequency, but rather to enable effective gate-charge transfer on the initial pulse within the broad linear operational bandwidth between the primary and secondary side resonances, these nonideal effects are neglected in the analytical model. This simplification allows the dual-resonant behavior and associated design insights to be presented clearly.

The quality factor, which characterizes the sharpness of the resonance, is given by the following:

$$Q = \frac{1}{R_{\text{eq}}}\sqrt{\frac{L_1 + L_2}{C_r + C_{iss}}}. \tag{12}$$

A high Q-factor indicates stronger resonance and reduced damping, enhancing voltage amplification but potentially introducing peaking effects if not properly tuned. Therefore, careful selection of C_r and transformer inductances ensures operation within the impedance plateau, avoiding excessive resonance while maintaining high dV/dt performance [53].

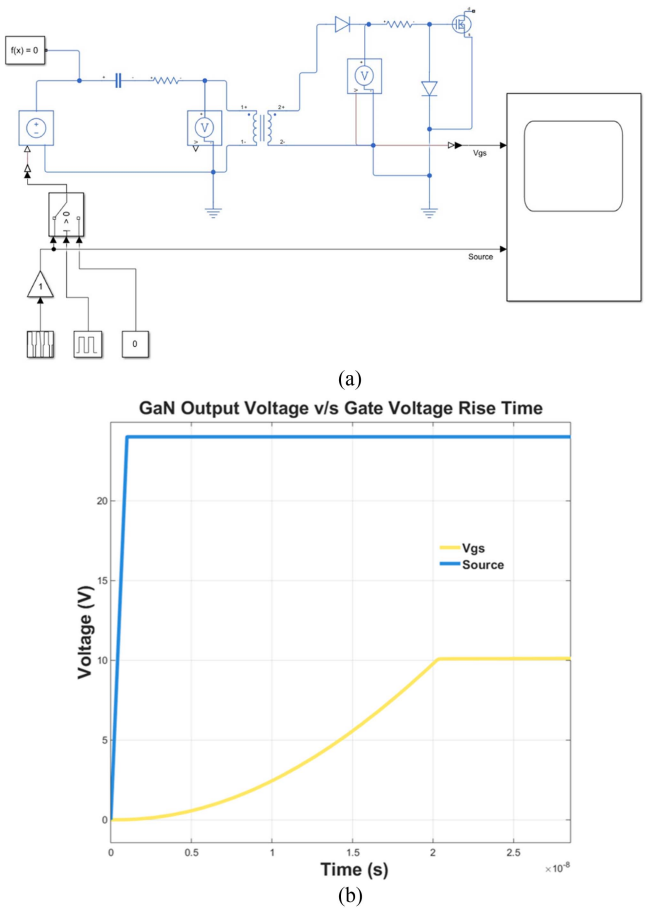


FIGURE 12. (a) Simulink model of GaN H-Bridge and transformer secondary / gate voltage output. (b) Voltage waveforms of GaN H-Bridge source and transformer secondary / gate voltage.

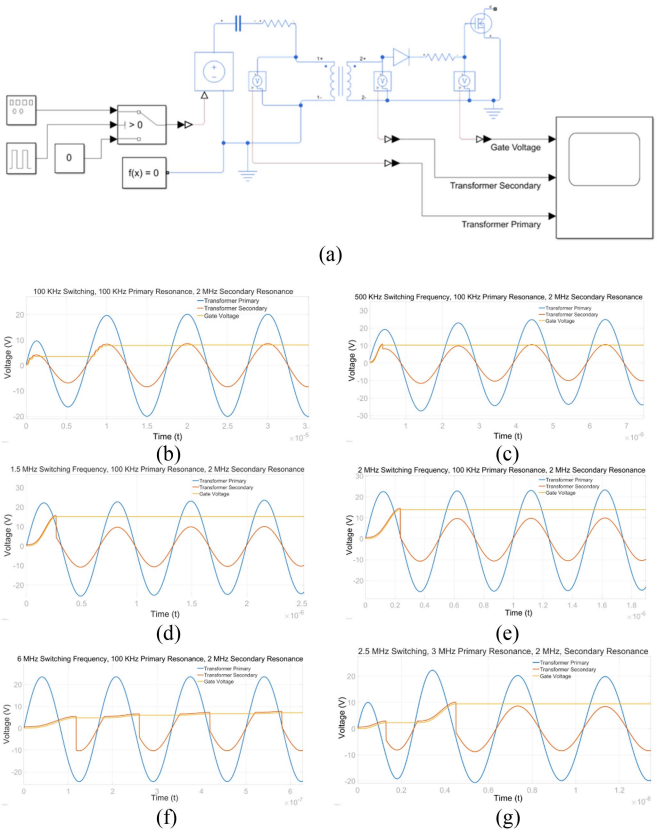


FIGURE 13. Simulink model and voltage waveforms of the resonant transformer showing effects of switching and resonant frequency variations. (a) Model. (b)–(f) Waveforms at 100 kHz–6 MHz. (g) 2.5 MHz case with higher primary resonance.

C. GAN HALF BRIDGE RISE TIME SIMULATION

A simple MATLAB Simulation was designed to establish the GaN half bridge output voltage waveform translation into secondary side transformer output voltage rise time as shown in Fig. 12(a). With primary side inductance of 12 μH, secondary side inductance of 26 μH and a coupling coefficient of 0.96, around 20 ns rise time was observed via voltage plot shown in Fig. 12(b). The simulation shows that in order to achieve fast rise time, the coupling coefficient plays the most crucial role. The higher the coupling the faster is the transformer secondary side gate voltage rise time. The results can be verified in Fig. 17 of the actual gate voltage where rise time around 20 ns can be observed.

D. SWITCHING FREQUENCY DYNAMICS

The primary resonance frequency can be tuned by choosing a suitable primary compensation capacitor C_r , enabling adaptation to the desired switching speed and other system requirements. Since the main purpose of the circuit is to charge the gate capacitance of the series-connected GaN HEMTs during the first pulse, using separate windings for turn-ON and turn-OFF, it does not require operation at a fixed resonance frequency. This tuning can be achieved by selecting an appropriate resonant frequency along with the corresponding primary compensation capacitor. The critical factor is the dV/dt of the rising edge of the driving pulse, rather than the entire waveform.

The impedance characteristics shown in Fig. 10 indicate that the impedance reaches its minimum near the primary resonance frequency. Operating close to this point results in increased current flow, which, due to transformer parasitics and source resistance, impedes voltage rise. Conversely, beyond the impedance plateau, the impedance magnitude increases, adversely affecting circuit performance. Beyond the secondary resonance, the system behaves as a second-order resonant converter, an operationally viable mode but one that introduces high-frequency challenges such as EMI and the need for extremely small passive components. Hence, the optimal operating region is within the impedance plateau between the primary and secondary resonance frequencies, as illustrated in Fig. 10. The primary resonance frequency can be adjusted to meet the desired high-voltage dV/dt requirements by appropriately selecting the compensation capacitor C_r .

A simple MATLAB simulation, shown in Fig. 13(a), was conducted to study the effect of different switching frequencies on the primary and secondary resonant frequencies. The primary resonance is determined by the compensation capacitor and primary inductance, while the secondary resonance

depends on the secondary inductance and the gate capacitance of GaN. With the primary resonance set at 100 kHz and the secondary at 2 MHz, results for a 100 kHz switching frequency [see Fig. 13(b)] show that the gate voltage does not build up during the first pulse. Since the circuit's goal is to charge the gate in the initial pulse, operating at the primary resonance frequency is unsuitable.

Fig. 13(c) shows that a 500 kHz switching frequency allows the peak gate voltage to develop within the first pulse. Similar behavior is observed at 1.5 and 2 MHz switching frequencies [see Fig. 13(d) and (e)]. However, at 6 MHz [see Fig. 13(f)], the gate voltage fails to reach its peak during the first pulse and requires multiple pulses to fully charge the gate capacitor. Fig. 13(g) presents results for a 2.5 MHz switching frequency, with the primary resonance set at 3 MHz and the secondary at 2 MHz.

The simulation demonstrates that when the primary resonance exceeds the secondary resonance, the peak gate voltage cannot be achieved in the first pulse. Therefore, the primary resonance should always be equal to or lower than the secondary resonance.

E. TRANSFORMER CORE CROSS COUPLING ANALYSIS

To verify the magnetic behavior and coupling assumptions of the proposed transformer structure, a finite-element method (FEM) simulation was conducted in COMSOL as shown in Fig. 14. The simulated model comprises a single-turn primary conductor passing through two toroidal magnetic cores, each incorporating a single-turn secondary winding driven at a switching frequency of 1 MHz. The cores have dimensions of 8 × 4 × 4 mm and are characterized by an inductance factor A_L of 5500 nH. The resulting magnetic flux density distribution indicates that, due to the high permeability of the core material, the magnetic flux is strongly confined within each toroidal core and follows the flux path established by the primary excitation.

Flux leakage into the surrounding space is negligible, and no appreciable magnetic interaction is observed between adjacent cores. These results confirm that cross-coupling between secondary windings is effectively suppressed in the proposed configuration. Consequently, the mutual coupling among secondary windings can be considered negligible, and the corresponding mutual inductances may be safely assumed to be zero in the circuit-level resonance analysis.

V. EXPERIMENTAL RESULTS

A. EXPERIMENTAL EQUIPMENT

The prototype board with 2 GaN HEMTs GAN111-650WSB in TO-247 package by NEXPERIA connected in series and driven by SGT120R65AL e-mode GaN HEMT by STM Electronics based full bridge inverter circuits is shown in Fig. 15. After verifying the prototype operation, the V_{ds} voltage of 1.0 kV is applied from a DC test source. V_{ds} and I_{ds} waveforms are captured using 100 MHz high voltage differential probes

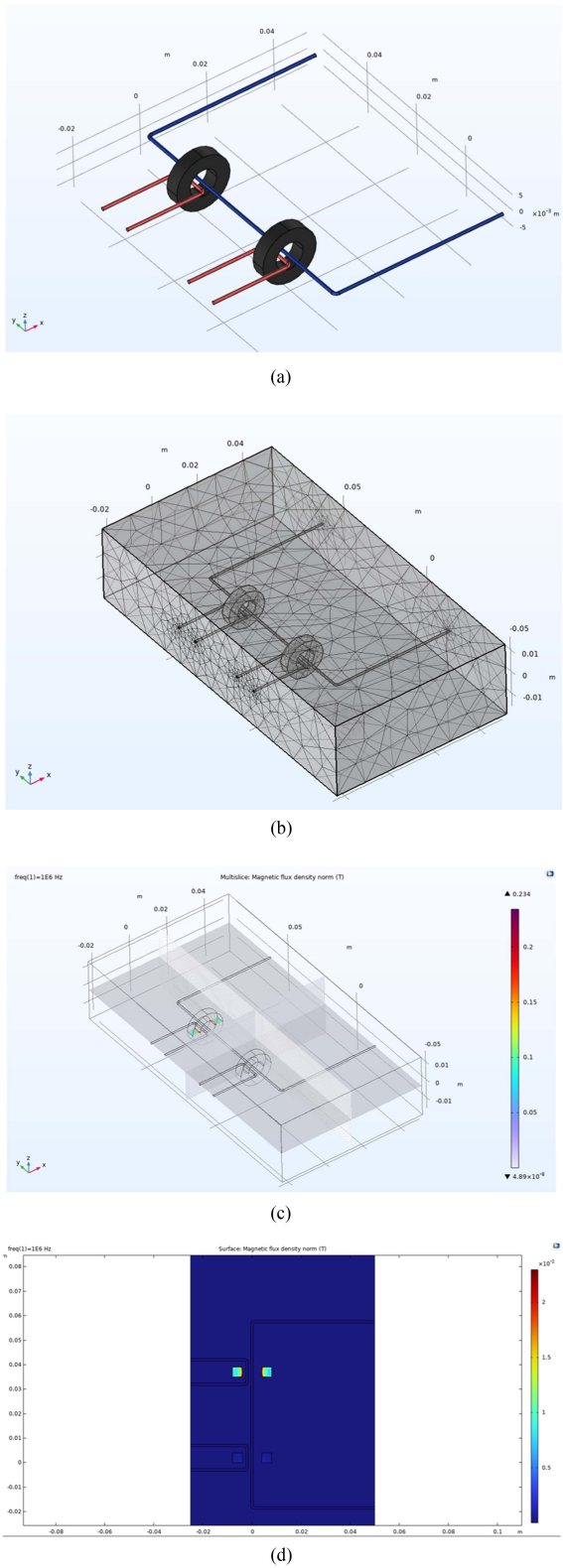


FIGURE 14. Magnetic flux density (T) distribution at 1 MHz obtained from COMSOL FEM simulation, illustrating flux confinement within the high-permeability toroidal cores and negligible magnetic interaction between adjacent secondary cores. (a) COMSOL Simulation. (b) Meshed simulation. (c) Isometric Plot showing magnetic flux density B (T). (d) Cut plot showing magnetic flux density B (T).

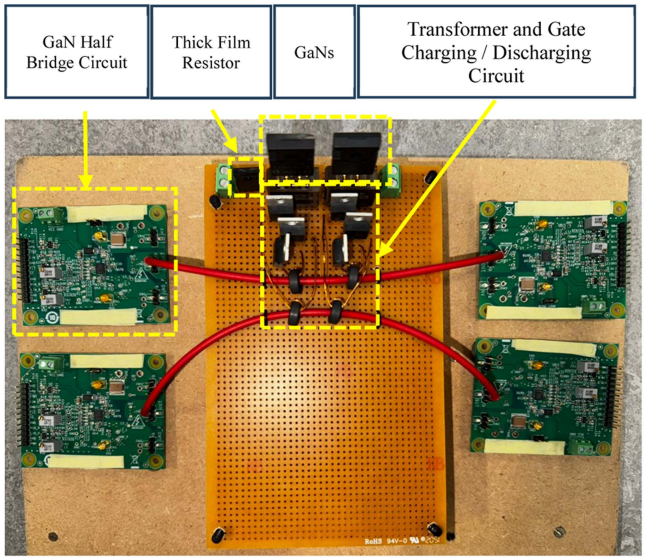


FIGURE 15. Prototype board showing HV turn-ON/OFF single-turn loops through toroidal cores, coupled to two series-connected GaN HEMTs via intermediate circuitry.

TABLE 2. Various Components Used in the Experimental Setup

S No.	Part Number	Description
1.	GAN111-650WSB	Through Hole GaN Switch, 650 V
2.	SGT120R65AL	GaN Switch, 650 V
3.	STDRIVEG610	GaN Half Bridge Gate Driver
4.	IRFZ14	Small Signal MOSFET
5.	AP851 390/100/25/10 R F 50PPM	Ohmite Thick Film Non Inductive Resistor
6.	B64290P0751X038	High Permeability Toroidal Core
7.	N2780B	Current Probe by Keysight
8.	TBS2000B	250 MHz Tektronix Oscilloscope
9.	CT4072	100 MHz, High Voltage Differential Probe by CAL Test Electronics
10.	Heinzinger PNC 6000 - 30	6 kV / 30 mA HV-DC power source
11.	MKP1W041007K00KS SD	1 μF 3000 V Film Capacitor

TABLE 3. V_{ds} Measurement Across Each Series Connected GaN HEMTs

S No.	Load	Drain–Source Voltage	Value Observed	ΔV
1.	*150* Ω	V_{ds1} (Bottom MOSFET)	512	~1.6 %
2.		V_{ds2}	496	~1.6 %
3.	*250* Ω	V_{ds1} (Bottom MOSFET)	520	~1.6 %
4.		V_{ds2}	504	~1.6 %
5.	*400* Ω	V_{ds1} (Bottom MOSFET)	512	~2.4 %
6.		V_{ds2}	488	~2.4 %

CT4072 by CAL Test Electronics, Current Probe N2780B by Keysight Technologies on a 250 MHz Tektronix TBS2000B Oscilloscope. The technical items utilized are summarized in Table 2. Table 3 summarizes the measured V_{ds} across each of the two series-connected GaN HEMTs under varying load conditions, along with the corresponding percentage voltage imbalance between the devices.

B. MITIGATION OF PARASITIC INDUCTANCE INDUCED VOLTAGE OVERSHOOT IN FAST GAN SWITCHING

When a power switch turns OFF very rapidly, the abrupt interruption of current interacting with circuit parasitics especially the stray inductance, produces a voltage overshoot according to $v = L\,\mathrm{d}i/\mathrm{d}t$. As the turn-OFF speed increases, the rate of change of current becomes extremely high, causing correspondingly large overshoot and ringing on the switching node.

This problem becomes significantly more severe with GaN HEMTs, which exhibit much faster switching transitions and higher di/dt compared to Si and SiC MOSFETs. Their ultrafast turn-OFF capability amplifies the effect of even small parasitic inductances, leading to substantial overshoot which can potentially overstress the device and lead to its failure.

To reliably evaluate the series-connected GaN devices, the test setup was carefully engineered to minimize parasitic inductances. Straight copper bars were used for the high-voltage DC bus connections to reduce loop inductance and maintain a low-impedance current path. It is pertinent to mention that conventional wire-wound or spiral-track resistors inherently exhibit parasitic inductance, which can introduce significant voltage overshoot when subjected to the extremely high di/dt produced by GaN devices. Therefore, nonwirewound thick-film resistors [27] specifically designed with nearly zero inductance were selected as the resistive load. These Ohmite thick-film elements help suppress overshoot and ringing by minimizing the inductive component of the load, enabling accurate characterization of the GaN device's switching behavior.

C. MEASUREMENT PROBES IMPACT ON VOLTAGE DISTRIBUTION AND MEASUREMENT ACCURACY

Ghafoor et al. [19] and Zhao et al. [38] have shown that the measurement probes can significantly distort voltage sharing in series-connected MOSFETs topology. So it is critical that the probe effects must be considered and compensated during measurement. Voltage probes and their leads add parasitic capacitance and impedance that alter the local capacitive coupling between devices and thus change both static and dynamic V_{ds} distribution. The compensation is not needed during normal experiments when no probe is employed for measurement. Since GaN device has very low gate capacitance, and very fast dv/dt and di/dt, the addition of probe impedances across its terminals can seriously disrupt the device normal operation. The impact is not limited to the V_{ds} voltage distribution across the series connected devices. It is observed that probe impedance if not properly compensated can also introduce ultra-high frequency resonance at the gate terminal of the series connected GaN devices which can distort the gate voltage signal thereby distorting the output voltage V_{ds}. The probe impact and its compensation is critical to be considered for reproducibility of the experimental results.

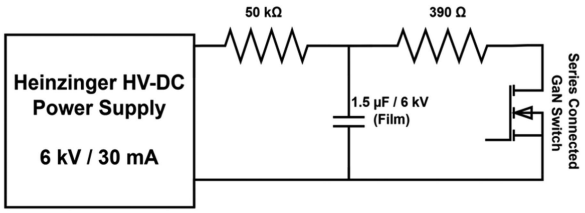


FIGURE 16. Block diagram of the test setup for high-voltage DC testing of the developed series-connected switch module.

Moreover, when characterizing ultrafast GaN switching with nanosecond scale rise times and dv/dt of tens of V/ns or more, probe sensitivity and bandwidth become critical. Probes with high input capacitance, long ground leads or limited bandwidth will slow the observed edge, introduce ringing or overshoot, and hide the true device performance i.e., a slow probe and or oscilloscope makes a fast GaN edge appear slow. For accurate capture of GaN transients high-bandwidth, low-capacitance (or active) differential probes and an oscilloscope whose bandwidth comfortably exceeds the frequency content of the edge is needed [54]. Practically, this means using properly rated high-frequency differential probes, minimizing ground-lead length and using matched impedance connections, characterizing and subtracting probe loading where possible. Failure to do so can lead to incorrect conclusions about device or balancing performance rather than limitations of the driving technique and DUT itself.

D. VOLTAGE BALANCING AT HIGH VOLTAGE

The block diagram of the developed high-voltage DC test setup is presented in Fig. 16. The control and monitoring station, placed outside the protective high-voltage Faraday cage, consists of a high frequency 4-channel oscilloscope (Model TBS2000B), a laptop for defining switching time, DC laboratory power supplies for energizing the PCBs, a protective interlock system, and a Heinzinger 6 kV / 30 mA HV-DC power source. Since the power supply is unable to deliver high current at high voltage, a capacitor bank is charged using the high-voltage supply, after which the stored energy is switched across the load to avoid tripping the supply due to high inrush current surges. The GaN-based high voltage switch module is energized through a capacitor bank charged by a Heinzinger HV-DC power supply. High frequency high voltage differential probes (Model CT4072 by CAL Test Electronics) were connected across the drain of each individual switch and its source terminal, while the current probe is placed in the drain path to monitor circuit current. The switching gate signals were programmed via an Arduino interface. To confirm proper gate drive synchronization and voltage sharing, the gate-to-source voltages V_{gs} of all devices were captured. High frequency probes (CT4072, 200:1 attenuation) were placed across the gate source terminals of each GaN HEMT. Identical V_{gs} waveforms with matched turn-ON and turn-OFF instants can be observed across both devices, reaching ∼10 V peak as shown in Fig. 17. The similarity in charging profiles of the input capacitance C_{iss} confirms uniform gate excitation. The GaN HEMT stack is fully turned on once the threshold voltage is exceeded.

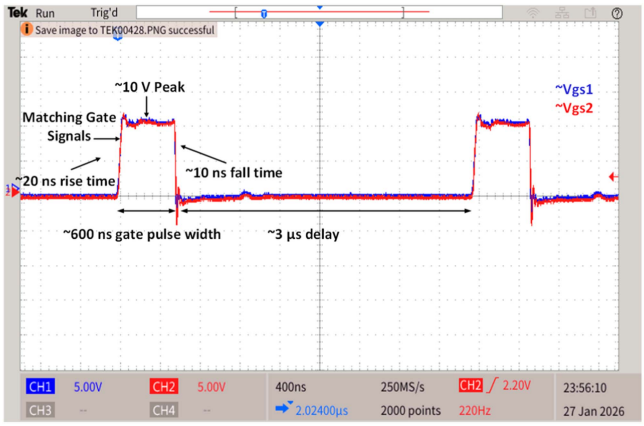


FIGURE 17. Gate to source (V_{gs}) voltage across 2 GaN HEMTs in series during turn ON and turn OFF.

A double-pulse test was performed in which the series-connected GaN devices were turned on for 600 ns, followed by a 3 μs off-interval. The off-interval allows the capacitor bank to fully recharge and restore the DC-link voltage to 1 kV prior to the subsequent switching event, ensuring reliable operation under current-limited conditions.

Subsequently, high-frequency differential probes (CT4072) were connected across the drain–source terminals of each GaN device to measure the individual device voltages V_{ds}. Fig. 18(a)–(c) present the double-pulse test results obtained with three noninductive resistive loads of 150, 250, and 400 Ω, corresponding to peak drain currents of 6.4, 4.00, and 2.512 A, respectively. In each figure, the blue and red traces represent the measured V_{ds} across the two series-connected GaN devices, while the magenta trace indicates the drain current flowing through the device stack.

With an approximately 1 kV DC-link voltage, the two GaN devices exhibit nearly even static and dynamic voltage sharing during both turn-ON and turn-OFF transients, confirming effective voltage balancing under all load conditions. The oscilloscope captured transition characteristics further show a clear dependence of rise time on load resistance. For the 400 Ω load, a rise time of approximately 67 ns and a fall time of approximately 26 ns were measured. With the load resistance reduced to 250 Ω, the rise and fall times decreased to approximately 44 and 19 ns, respectively. For the 150 Ω load, a much faster rise time of approximately 14 ns and a fall time of approximately 13 ns were observed, corresponding to the higher current level.

These results demonstrate that faster voltage transitions are achievable at the expense of increased current stress. Despite the variation in load and current, the transformer-coupled gate driver consistently maintains nearly balanced V_{ds} sharing across the series-connected GaN devices, validating

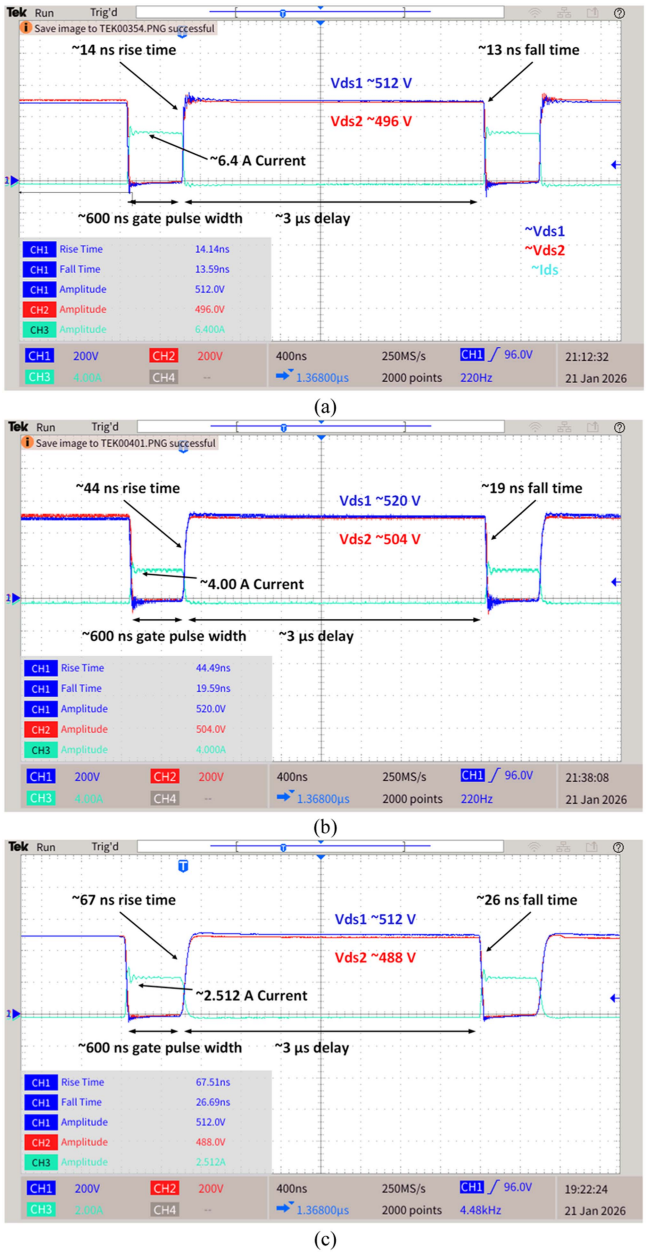


FIGURE 18. V_{ds} **voltage across 2 GaN HEMTs in series switching at 1 kV. (a) With 150 Ω Load. (b) With 250 Ω Load. (c) With 400 Ω Load.**

the robustness and effectiveness of the proposed gate-driving approach.

It is important to note that the measured rise and fall times are subject to the bandwidth limitations of the measurement setup. A 100 MHz differential voltage probe (CT4072) was used in conjunction with a 250 MHz oscilloscope. Based on standard bandwidth considerations (t_r0.35/BW), the corresponding rise-time limits of the probe and oscilloscope are approximately 3.5 and 1.4 ns, respectively. The combined system rise-time limitation, estimated using a root-sum-square approach, is therefore approximately 3.8–4 ns. Since the experimentally observed rise and fall times are significantly larger than this limit, the reported measurements capture the switching dynamics within the constraints of the probing arrangement. This clarification is provided to ensure transparency and reproducibility of the experimental results under high-dv/dt operating conditions.

VI. CONCLUSION

GaN devices, owing to their lateral device structure, exhibit excellent characteristics such as low gate charge, fast switching, and high dv/dt capability, making them superior to conventional IGBTs and SiC MOSFETs for ultrafast operation. However, the same lateral structure inherently limits their voltage blocking capability to about 650 V, restricting their direct use in kilovolt-level applications. Series-connecting GaN devices therefore emerges as the most viable solution to harness the advantages of GaN technology at higher voltages.

Efforts have been made quite recently to achieve voltage balance across series connected GaN devices using closed loop techniques. This work however demonstrates a scalable open-loop transformer-coupled gate driver that achieves nearly equal voltage sharing across series-connected GaN HEMTs. Using a simple GaN-based full-bridge driver, an optimized L_3C_2 resonant network, and a straightforward gate-charging/discharging circuit, the method delivers minimal signal mismatch and precise gate-current synchronization across series connected devices.

Detailed analysis of the transformer design parameters, supported by an L_3C_2 equivalent-circuit framework and comprehensive MATLAB/Simulink/FEM simulations with one primary and multiple secondary windings, identifies the resonance conditions and operational bandwidth plateau needed to ensure complete gate-capacitance charging within the first excitation pulse, an essential requirement for dynamic voltage balancing. The study also emphasizes the significant influence of measurement probe parasitics on gate and output voltage waveforms, demonstrating that proper probe compensation and high-bandwidth instrumentation are critical for accurate characterization of MHz-range switching transitions.

In addition, the work addresses the challenge of voltage overshoot commonly encountered with ultrafast GaN switching, showing effective mitigation through loop-inductance minimization with the use of noninductive thick-film resistors.

Experimental results confirm nearly balanced voltage sharing up to 1 kV with two series-connected GaN HEMTs with different loads and currents, validating the effectiveness of the proposed open-loop transformer-coupled gate-driving approach. These results demonstrate transformer-coupled gate driving technique as an effective method to extend GaN's performance benefits into the kilovolt regime. The proposed technique can realize the development of compact, cost-effective, high-frequency, high-voltage solid-state switches, enabling scalable and programmable systems capable of generating complex ultrafast arbitrary waveforms for advanced high-voltage testing of grid assets.

ACKNOWLEDGMENT

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SOHRAB GHAFOOR (Student Member, IEEE) was born in 1987 in Mirpur, Azad Kashmir, Pakistan. He received the bachelor's degree in electrical and electronics engineering from AJK University in 2009, and the master's degree from the National University of Science and Technology (NUST), Islamabad, Pakistan, in 2013. He is currently working toward the Ph.D. degree in the field of high voltage technologies from Delft University of Technology (TU Delft), Delft, The Netherlands.

He has worked on the development of various underwater sensor systems, ship degaussing systems, and power electronics projects and joined Delft University of Technology (TU Delft). His current research interests include isolated gate drivers, power electronics-based programmable power supplies, and high-voltage testing of renewable-rich power electronics-dominated grids.

REZA MIRZADARANI (Student Member, IEEE) was born in 1991 in Isfahan, Iran. He received the M.Sc. degree in power systems from the University of Kashan, Kashan, Iran, in 2018. He is currently working toward the Ph.D. degree in the field of high-voltage technologies from Delft University of Technology (TU Delft), Delft, The Netherlands.

He has worked on various high-voltage power electronics projects and joined the Delft University of Technology (TU Delft) to focus on the design of medium-voltage, medium-frequency transformers for solid-state transformers in green hydrogen production.

Mr. Mirzadarani is a winner of IEEE International Challenge in Design Methods for Power Electronics Excellent Innovation Award 2023.

HITESH DIALANI received the M.Sc. degree in electrical engineering from the Delft University of Technology (TU Delft), Delft, The Netherlands, in 2023.

He is currently working as a technician with the DC Systems and Energy Conversion & Storage (DCE&S) Group Lab, TU Delft, supporting research in medium-voltage power electronics and advanced gate driver circuits for wide-bandgap semiconductor devices. His professional research interests include high-efficiency power conversion systems, experimental validation of power electronics circuits, and laboratory development of medium-voltage testing setups.

PETER VAESSEN (Member, IEEE) received the M.Sc. degree (cum laude) in electrical power engineering from Eindhoven Technical University, Eindhoven, The Netherlands, in 1985.

In 1985, he also joined KEMA (now a CESI brand). In his 40-year career, he held the Research positions in the field of large power transformers and high voltage measurement & testing. He headed the Transmission & Distribution High Voltage Department and managed realization projects, among them construction of Dutch 400 kV substations and laboratory test facilities. As a Principal Consultant, he has 25 years' experience in (U)HVDC technology and Transmission & Distribution Grids with high shares of renewables. He is the Manager innovations with CESI and actively involved in the technology strategy. He is a part-time Professor Hybrid Transmission Systems with the Delft University of Technology, Delft, The Netherlands, where he teaches high voltage technology and HVDC.

Mr. Vaessen is the Chairman of the Board of the European Distributed Energy Resources Laboratories Association (DERlab) and a Member of several national and international working groups.

MOHAMAD GHAFFARIAN NIASAR (Member, IEEE) was born in Tehran, Iran, in 1984. He received the M.Sc. degree in electrical power engineering from the Sharif University of Technology, Tehran, Iran, in 2008, and the Ph.D. degree in electrical engineering from the Royal Institute of Technology, Stockholm, Sweden, in 2015.

He is currently an Associate Professor with the High Voltage Technologies Group, Delft University of Technology, Delft, The Netherlands. His main research interests include the ageing of electrical insulation, HVDC insulation system, partial discharges, high-frequency power transformers, power cables, and FEM modeling.