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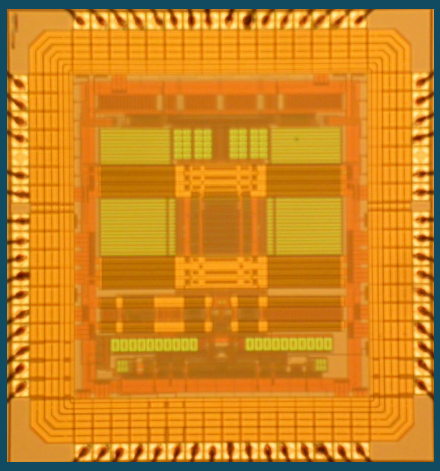

Sha Xia

High-Speed Interfaces for Capacitive Displacement Sensor

High-Speed Interfaces for Capacitive Displacement Sensor

Dissertation

for the purpose of obtaining the degree of doctor

at Delft University of Technology

by the authority of the Rector Magnificus Prof.dr.ir. T.H.J.J. van der Hagen

Chair of the Board for Doctorates

to be defended publicly on

Monday 11 November 2019 at 12.30 o'clock

by

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To my beloved parents and my wife Jie

致我亲爱的父母亲和钟洁

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Chapter 1

Introduction

1.1. Motivation

Capacitive sensors are one of the most widely used sensors today, as they offer a number of distinct advantages: compactness, simple principle of operation, and relatively low cost [1-13]. Capacitive sensors can achieve very high resolution due to the fact that, ideally, they consume no electric energy and therefore generate no electric noise [14,15]. A key application of capacitive sensors is position/displacement measurement. Over the last several years, interest in implementing capacitive sensors for measuring extremely small displacements in the sub-nanometer range has increased. For example, such sensors are now used as inertial sensors, accelerometers, and pressure sensors.

Capacitive displacement sensors are also used in high-precision mechatronic systems where the position/vibration of critical mechanical components must be dynamically stabilized with sub-nanometer precision. Any unwanted motion must be sensed in real time and be corrected for. For example, in the next generation extreme ultraviolet (EUV) lithography machines, the required precision in displacement/position measurement will be in the picometer range [16,17].

The correction of such small displacements/vibrations can be achieved with the help of a servo loop consisting of a displacement sensor and an actuator, as shown in Fig. 1.1. The performance of the servo-loop depends heavily on that of the displacement sensor. However, achieving sub-nanometer displacement measurement with a capacitive

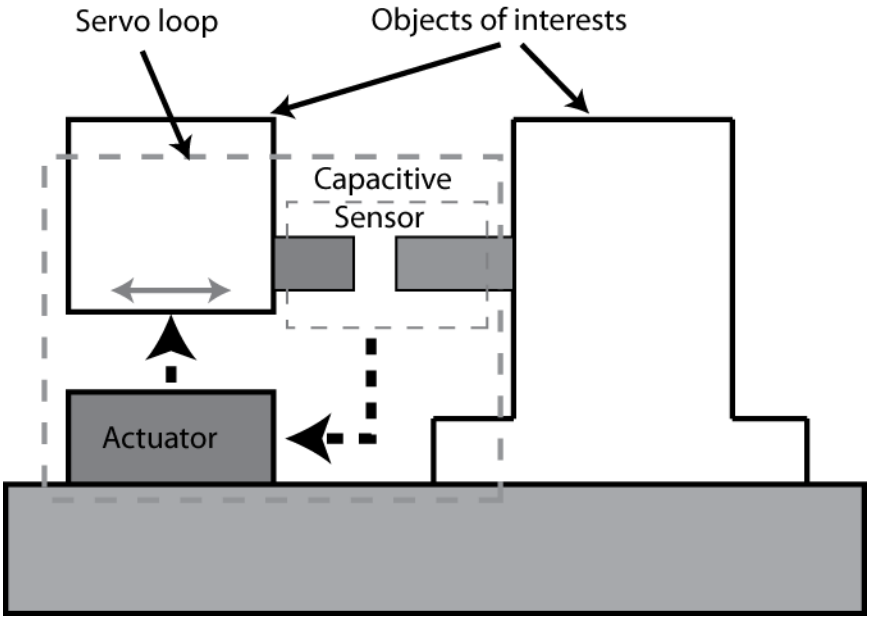

Fig.1.1: Lithography machine in which the wafer stage is dynamically aligned with the lens columns by measuring the small displacement.

displacement sensor is quite challenging, both in terms of the sensor design and the interface electronics. On the one hand, the sensitivity of a capacitive displacement sensor, which is determined by the mechanical structure of the sensor head, is limited by a number of non-idealities such as electrode surface roughness and tilt. On the other hand, the reduced sensitivity as a result of these non-idealities puts more pressure on the interface circuit, which must then compensate for the drop in sensor sensitivity.

This thesis will not address the sensor head design, the focus of this work is on the interface circuit. The interface circuit should have the following characteristics:

Precision

To digitize the capacitance C_{sen} of a precision displacement sensor, a precision reference is required, which can either be a physical reference capacitor C_{ref}, or an 'equivalent' reference capacitor derived from a combination of other references, such as resistors, inductors, time references, current references, and voltage references [18]. While most of the recently reported capacitance-to-digital converters (CDC) directly employ a physical reference capacitor and demonstrate good resolution, measurement speed, and energy efficiency, their precision is

ultimately limited by the quality of the capacitive reference used.

Speed

Because the result of the capacitive displacement measuring system is used in a servo loop, the measurement speed of the CDC is also very important. If it is too slow the servo loop will not have sufficient bandwidth to correct for errors, causing the correction to be insufficient. It can be seen as a feedback system with delay in the loop filter, in which excess delay can cause instability.

Power

High speed measurement often leads to high power consumption. In an precision mechatronics environment, low power operation is also vital. Excess power consumption generates heat, which leads to a rise in temperature. Since capacitive sensors can be used to sense a lot of physical quantities, it is also quite easy to get cross-sensitivity from temperature changes. In that case, the measurement system cannot distinguish if the change in sensor capacitance is from a displacement change or temperature change. Therefore, the power consumption of the CDC must be limited to a certain degree.

A broad literature study (chapter 2) has shown that most existing capacitive interface circuits have either a low conversion speed or low capacitive resolution, which has led to the conclusion that no existing solution demonstrates all of the above-mentioned properties at the same time. This is due to the fact that no prior applications require such a stringent set of specifications. An in-depth investigation of the limitations of capacitive displacement sensors will therefore provide valuable information that could expand the application territory of capacitive sensors even further, which is the motivation behind the research described in this thesis.

1.2. Main research question and research methodology

The main research question of this thesis is: can the capacitive sensor interfaces be designed to enable capacitance measurements with high resolution and short measurement latency in a power-efficient way, so that it becomes compatible with high-precision real-time servo systems operating in tightly controlled working environments. At the same time, the stability of the interface should be high enough to avoid the need for recalibration.

To be more specific, the goal is to find a way to realize picometer level resolution displacement measurement using capacitive sensors that have stand-off distance of several micrometers, with a measurement time in microseconds range. On top of this, the power consumption should be kept as low as possible.

To answer the research question, the research methodology described below has been followed:

The first step is to take an overall look from a system point of view and to identify the limiting factors in the system. This is needed to find an optimum capacitance measurement system, possibly consisting of multiple sub-systems, each addressing a certain aspect of the requirements. This step is necessary, since a single system that can achieve all the requirements may be too impractical to realize.

Next, state-of-the-art solutions for interfacing high-performance capacitive sensors are studied so as to evaluate the potential benefits for the target application. The investigation of capacitance measurement principles is geared toward their potential use in low-power, high-speed and high-accuracy applications.

The final step is to solve each of the challenges by proposing and implementing proper techniques. The validity of the proposed solution is verified with experimental results.

1.3. Organization of this thesis

The thesis is organized in the following way, in order to answer the main question:

Chapter 2 provides a detailed survey of state-of-the-art voltage-driven, also called "two-port" capacitance, measurement circuits. The result of the survey provides a solid understanding of the limitations of the existing solutions and the pros and cons of each circuit topology.

Chapter 3 introduces the baseline capacitance cancellation technique and the implementation of this in the context of displacement measurement using capacitive sensor.

Chapter 4 presents a reconfigurable low-power CDC that can be used to realize both zoom-in, high-resolution, high-speed capacitance measurement and high-resolution, large dynamic range, low-speed capacitance measurement. This is a circuit solution that can be used as the main CDC.

Chapter 5 presents an alternative solution that can be used to deliver a zoom-in, high-resolution, high-speed capacitance measurement with low power consumption. The pros and cons with respect to the work presented in Chapter 4 will be elaborated on.

In Chapter 6, a benchmark is provided that includes other recent works in this field. This chapter concludes the thesis and provides recommendations for future works.

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Chapter 2

Background Overview

2.1. Capacitive displacement sensors

This section focuses on the principle of operation and the main characteristics of a parallel-plate capacitive displacement sensor. An electrical model of the sensor is introduced, followed by a discussion on the challenges and limiting factors in high-performance applications.

2.1.1. Operating principles of capacitive displacement sensors

Capacitive displacement sensors come in a variety of structures. The parallel-plate capacitive sensor is however the most commonly utilized structure when high sensitivity is required for very small displacement measurements. As the name suggests, a parallel-plate capacitive sensor comprises two parallel electrodes with an overlapping area A and plate distance d. When d is much smaller than the plate dimensions, the electrical field can be considered to be perpendicular to the parallel plates, and the capacitance of the structure can be approximated as:

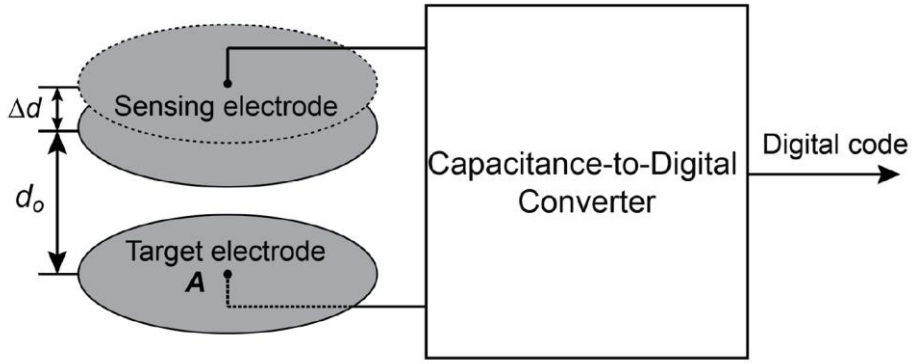


Fig. 2.1: Parallel-plate capacitive displacement sensor and the readout circuit.

$$C = \epsilon \frac{A}{d} \tag{2.1}$$

where ϵ is the dielectric constant of the material between the two plates. In a capacitive displacement sensor, variations in d result in a change in capacitance, therefore the displacement information can be obtained by means of capacitance measurement. For a small displacement Δd which satisfies $\Delta d \ll d$, we have:

$$\Delta C = \epsilon \frac{A}{d \pm \Delta d} - \epsilon \frac{A}{d} \approx \mp \epsilon \frac{A}{d^2} \cdot \Delta d \tag{2.2}$$

The term $\epsilon \frac{A}{d^2}$ is called the sensitivity of the capacitive displacement sensor. It describes how much capacitance C changes (ΔC) in response to a change in distance (Δd). It is clear that the capacitive displacement sensor is not linear and that the sensitivity is inversely proportional to the square of the plate distance d. From this relationship, it can be inferred that for higher sensitivity, the plate distance should be reduced.

A more insightful view can be obtained by looking at the relative sensitivity of the capacitive displacement sensor. If we divide Eq. 2.2 by Eq. 2.1, we can obtain:

$$\frac{\Delta C}{C} \approx \mp \frac{\Delta d}{d} \tag{2.3}$$

which suggests that the relative change in the capacitance is approximately proportional to the relative change in the plate distance. As the relative changes in capacitance directly translates into the resolution requirements of the sensor readout circuit, with Eq. 2.3 we can estimate the required nominal plate distance based on the target displacement resolution.

2.1.2. Electrical model of capacitive displacement sensors

Figure 2.2 shows an electrical model of a capacitive sensor. Besides the sensor capacitor C_S, also included in the model are two parasitic capacitors C_{P1} and C_{P2} at the two terminals of C_S. Parasitic capacitance is inevitable in the realization of capacitive sensors. It plays an important role in the performance of the capacitive sensor measurement systems, as it tends to increase their energy consumption. Therefore, minimizing the parasitic capacitance can be an important step toward building an energy-efficient capacitive sensor measurement system.

Capacitive sensors are high-impedance sensors, and so they are quite sensitive to electrical disturbances [1]. Therefore, the connection between such sensors and their interface circuits is often realized with coaxial cables, leading to a significant amount of parasitic capacitance to ground. The longer the cable, the larger the parasitic capacitance becomes. Minimizing the parasitic capacitance can be achieved by co-integrating the interface circuit with the sensor head in order to keep the distance as short as possible. This is also seen as one of the motivation for integrating capacitive sensors on the chip. In such realizations an interface circuit realized on the same chip or in the same package with the sensor can be an important way to improve the energy efficiency of the system.

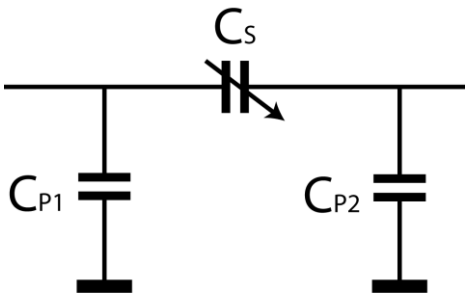


Fig. 2.2: Electrical model of the capacitive displacement sensor.

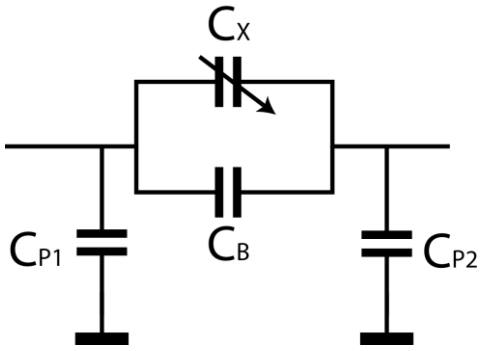


Fig. 2.3: Electrical model of the capacitive displacement sensor, splitting the sensor capacitance into baseline capacitance and varying capacitance.

The simple model shown in Fig. 2.2 does not fully describe how the measurand modulates the sensor capacitor C_S. For instance, due to displacement, only a fraction of C_S varies. This can be modelled by defining a mean, or baseline capacitance C_B and a varying capacitance C_X, as is shown in Fig. 2.3. A modulation index can be defined as in [2]:

$$C_B = \frac{C_{S,max} + C_{S,min}}{2} \tag{2.4}$$

$$\alpha = \frac{C_{S,max} - C_{S,min}}{C_B} \tag{2.5}$$

The modulation index α expresses the ratio of the capacitance variation range to the baseline capacitance, and is in most cases in the order of 0.1 or smaller. A low modulation index often means that a large portion of the dynamic range of the interface will be wasted

on the baseline capacitance, leading to low energy efficiency [3]. Therefore, it is important to find a way to increase the modulation index of the capacitive sensor.

The reason for a low modulation index is the stand-off distance between the two plates d, which is much larger than the maximum displacement of interest Δd_{max}. The reasoning behind this will be discussed in the next section.

2.1.3. Alignment of capacitive displacement sensors

As discussed in the previous sections, the stand-off distance between the plates of a capacitive sensor plays an important role, as it determines its sensitivity as well as the modulation index. In industrial applications, the stand-off cannot be smaller than a few hundred micrometers [4], due to mounting and machining tolerances, error from tilt. However, such a stand-off is a serious challenge for the readout electronics design.

This is especially true for the types of applications for which the solutions presented in this thesis are intended: the stabilization and vibration reduction of essentially static objects. Due to the fact that the objects to be measured are almost still, the variation in their displacement will often be smaller than the practically achievable stand-off distance between the target and the capacitive sensor head. This inevitably leads to low sensitivity and a low modulation index, and hence to wasted power in the capacitance measurement system [3,5].

In order to improve the alignment accuracy, several methods can be used. One method is to fabricate all the relevant parts with small tolerances. However, not only does this method significantly increases cost, but parts manufactured with micrometer accuracy are still not suitable for systems that need to be transported in an assembled state, because of the associated risk that accidental vibrations may destroy the sensor. Another method is manual alignment after the sensor assembly. However this leads to inefficiency, or may even be practically impossible. A better solution is to incorporate a self-alignment mechanism into the sensor head, as described in [6]. In that work, a thermally actuated auto-alignment

system called a “thermal stepper” is proposed. It is simple, cheap and reliable, and can achieve relatively precise alignment.

With a thermal stepper, the stand-off distance of the sensor head can be reduced to 10~20 μm, in practice. Consequently, for applications requiring nanometer sensitivity, modulation indexes are in the order of 0.01, in the best-case scenario.

2.1.4. Discussion

This section discusses the basic operating principles and the electrical modelling of a parallel-plate capacitive displacement sensors. It has been shown that the alignment challenges of capacitive displacement sensors lead to low sensitivity and a very low modulation index. These place large dynamic range requirements on the succeeding interface circuit.

Since, in the target application, the displacement measurement will be used in a servo-loop, the speed requirement of the interface circuit is also high. In the next section, the principles of interface circuits that convert capacitance into electrical signal will be addressed, including the possible structures and references used for the conversion.

2.2. Capacitive sensor interfacing approaches

Many principles have been investigated in the past to measure capacitance. For the purposes of this thesis, we can classify these principles in the following two categories.

1) Indirect capacitance-to-digital conversion

In many cases, the unknown capacitor is first converted into another unit, for instance a voltage, by a capacitance-to-voltage converter (CVC) [7-13] or into frequency (time period) by a capacitance-to-frequency converter (CFC) [14-27]. The capacitor is then converted into a digital code by either a conventional voltage-input analog-to-digital converter (ADC) or a time-to-digital converter (TDC).

2) Direct capacitance-to-digital conversion

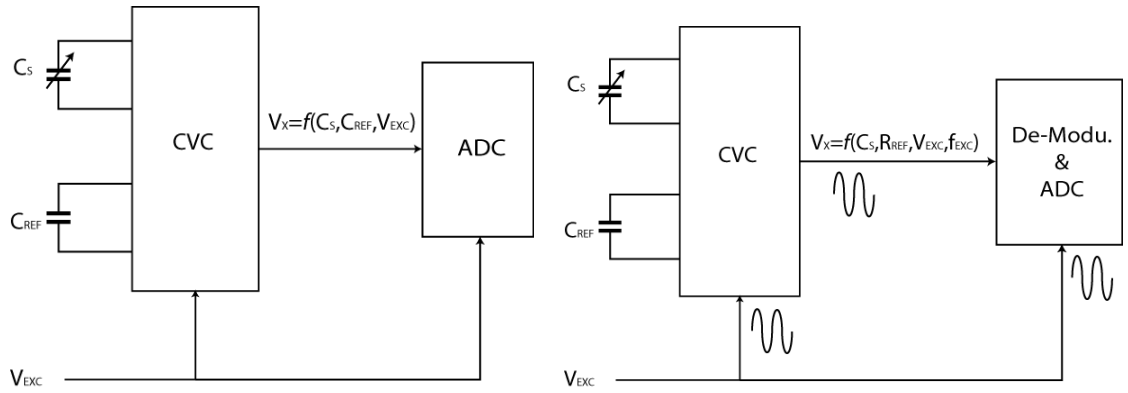
Many ADCs make use of switched-capacitor circuitry allowing them to be readily converted into a capacitance-to-digital converter (CDC) by using the capacitor bank as a reference capacitor C_{REF}. Examples of such designs include switched-capacitor sigma-delta ($\Sigma\Delta$) based CDCs [28-32] and successive approximation register (SAR) based CDCs [33-35]. These types of CDCs benefit from the charge-balancing/charge-redistribution nature of the corresponding ADCs and can achieve capacitance conversion. By applying the same reference voltage to both the sensor capacitor and the reference capacitor, the exact value of the reference voltage does not affect the conversion result. The output digital code is a representation of the ratio between the sensor capacitor C_S and the reference capacitor C_{REF}.

In the following sections, the operating principles of those capacitance conversion methods will be introduced, and the characteristics will be compared.

2.2.1. Capacitive sensor interface employing a CVC

A CVC converts an unknown capacitance into a voltage signal. This is usually done with either charge amplifiers or trans-impedance amplifiers. The most commonly used CVCs can be classified into two categories: switched-capacitor (SC) CVCs [7-10] and continuous-time (CT) CVCs with synchronous demodulation [11-13].

Figure 2.4 shows the block diagrams of such circuits. CVCs require an excitation voltage and other passive components, usually in the form of a fixed reference capacitance, to



(a) (b)

Fig. 2.4: CDCs based on a CVC followed by an ADC: (a) direct approach; (b) modulation approach.

convert the sensor capacitance into a voltage signal. In Fig. 2.4 (a), the output voltage of a CVC V_X can be expressed as a function of the unknown sensor capacitance C_S, the (equivalent) reference capacitance C_{REF}, and the excitation voltage V_{EXC}, as given in the following equation:

$$V_X = f(C_S, C_{REF}, V_{EXC}) \tag{2.6}$$

The applied excitation voltage V_{EXC} usually has either a sinusoidal or a square-wave shape. As shown in Fig. 2.4 (b), with a resistor reference and a sinusoidal excitation signal, the CVC (in this case usually realized as an active RC integrator) outputs a modulated output voltage signal the amplitude of which is a function of the excitation voltage amplitude V_{EXC}, the excitation frequency f_{EXC}, the reference resistor value R_{REF}, and the unknown sensor capacitance C_s, as given in the following equation:

$$V_X = f(C_S, R_{REF}, V_{EXC}, f_{EXC}) \tag{2.7}$$

This signal, together with the excitation signal, is fed into a demodulator. The demodulated signal is then converted by an ADC.

However, generating a sinusoidal excitation voltage is relatively complicated, as the extra sinusoidal-signal generation block makes the whole system power hungry [36]. It is therefore not often used, especially in chip-level solutions. On the other hand, square-wave

excitation can be implemented with just switches, which fits very well with CMOS technology and is hence very popular.

Using a CVC is one of the most popular methods for measuring capacitance and is often used as the signal-conditioning circuit in capacitive sensors. The advantage is that the signal conditioning and the AD conversion can be optimized separately, which can be useful in some cases.

2.2.2. Capacitive sensor interface employing a CFC

Another class of capacitive sensor interface circuits is based on a capacitance-to-frequency converter (CFC) which converts capacitance into frequency/time signals, as shown in Fig. 2.5. The unknown capacitor C_s modulates the output time signal, which can be measured by a time-to-digital converter (TDC). In its simplest form, a TDC can be realized with a counter. Examples of these types of circuits are period-modulators and duty-cycle modulators.

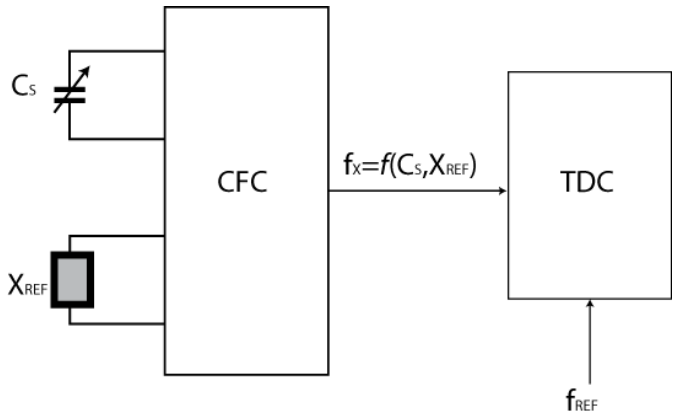


Fig. 2.5: CDCs based on a CFC followed by a TDC.

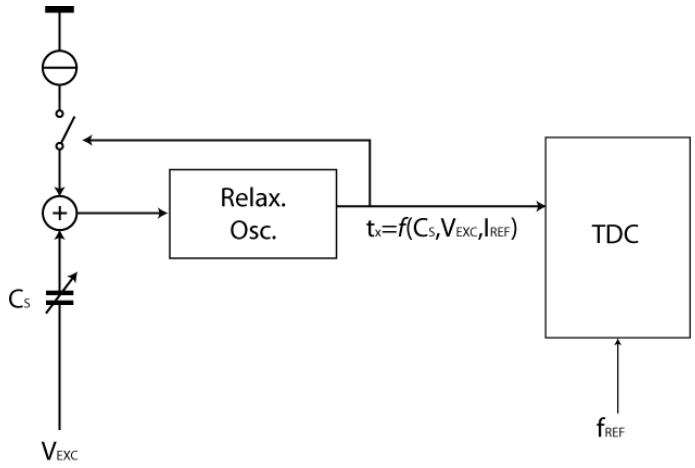


Fig. 2.6: CDCs based on a relaxation oscillator followed by a TDC.

In essence, a CFC is a type of oscillator which generates a time-domain signal (frequency, pulse-width or phase shift) that is proportional to the sensor capacitance C_s. A CFC can be realized as an RC relaxation oscillator [14, 15], current source relaxation oscillator [16-21], LC oscillator [22,23], or ring oscillator [24-27].

In the case of an RC relaxation oscillator, the capacitance value determines the time constant of the discharge process, and thus changing the oscillation frequency. The advantage of an RC relaxation oscillator is that it can be implemented with simple digital logic, which can be compact and low-power [15]. However, the oscillation frequency is highly dependent on the shunting capacitance and resistance. Therefore, they are used in applications where the power budget is limited, and the accuracy requirement is relaxed.

Instead of discharging the capacitor with a resistor, a current source can also be used, which is the case in [16]. The discharging current source is controlled by the output of the oscillator, as shown in Fig. 2.6. The charge associated when exciting the sensor capacitance results in a voltage jump which is detected by the relaxation oscillator. Once the voltage has crossed a certain threshold, the oscillator controls the current source to discharge the capacitor until the threshold is crossed again. Because the current source discharges the capacitor with a fixed current, the amount of time it takes for the capacitor to be discharged will be linearly related to the unknown capacitance. Recent work has shown that this measurement principle can achieve good capacitance resolution in an energy-efficient

manner. However, the operating speed of these circuits is generally on the low side, with conversion times in the order of a few milliseconds [16,21].

It is also possible to build an oscillator with a capacitance and an inductance, i.e. an LC oscillator [22]. The output frequency of an LC oscillator is a function of the sensor capacitance C_s and an inductance reference L_{REF}. The frequency signal produced by the LC oscillator can range from several hundred kHz to a few GHz. Because it is insensitive to the lossy component around C_s, it can be used for the measurement of sensor capacitor made from high loss materials [22]. This solution is favorable in chemical and bio-material applications, as many chemical properties show large sensitivity at RF/Microwave frequencies [23]. In industrial applications, where the physical changes such as displacement and acceleration must be detected, striving for very high frequency results in a waste of energy [5].

For very low-voltage and low-power applications, a ring oscillator can also be used. Two forms of circuits have been proposed. The unknown sensor capacitance C_s can be incorporated into the ring oscillator loop as a load capacitor, with which the output frequency of the ring oscillator will become a function of C_s [25]. Alternatively, the unknown charged sensor capacitance C_s can be used as a power supply for a ring oscillator. As time passes the ring oscillator discharges C_s causes the voltage to drop. During this process the oscillation frequency of the ring oscillator will also decrease accordingly over time. The time required for the ring oscillator frequency to drop down to a reference frequency will be a function of the sensor capacitance C_s [26,27], allowing it to be utilized to measure the sensor capacitance. One of the advantages of this approach is that the interface circuit is predominantly composed of digital circuit parts such as inverters and comparators, thus lending them very favorable for use in low-voltage operations and advanced technology nodes. It has also been shown that such interfaces can achieve superior energy efficiency [26]. However, this approach is highly sensitive to the parasitic capacitance to ground and to process variations, thus it is only suitable for relatively low-precision applications.

2.2.3. Capacitive sensor interface employing a ΣΔ-based CDC

One popular way of measuring the charge stored by the sensor capacitor is the so-called charge-balancing principle [28-32]. This principle is often used in normal switched-capacitor ΣΔ ADCs, where the input quantity is a voltage signal. Nevertheless, due to the charge-balancing nature of switched-capacitor ΣΔ ADCs, with a small modification, the principle can also be applied to capacitance measurement [29].

Figure 2.7 shows a block diagram of a ΣΔ-based CDC. The charge that is supplied by the unknown capacitor C_S is in the input branch, while the charge supplied by the reference capacitor C_{REF} is in the feedback path. The charge difference is integrated by the loop filter, which keeps track of the total amount of charge difference over time. The polarity of the loop filter output is determined periodically by a comparator. Depending on the output of the comparator, the charge supplied by the feedback path will also have a different polarity. Since the negative feedback loop keeps the output of the integrator bounded, over time the total charge supplied by the input branch will be balanced by the charge supplied by the feedback branch, hence the term "charge-balancing".

ΣΔ-based CDCs have many advantages. Because ΣΔ-based CDCs do not rely on component matching they can be used to realize high-resolution CDCs that also have a good linearity. The disadvantage, on the other hand, is their relatively low conversion speed due to their oversampling nature.

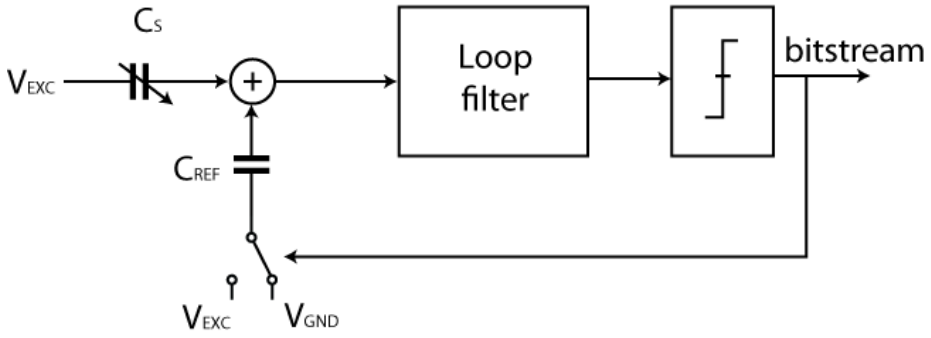


Fig. 2.7: CDC based on ΣΔ converters.

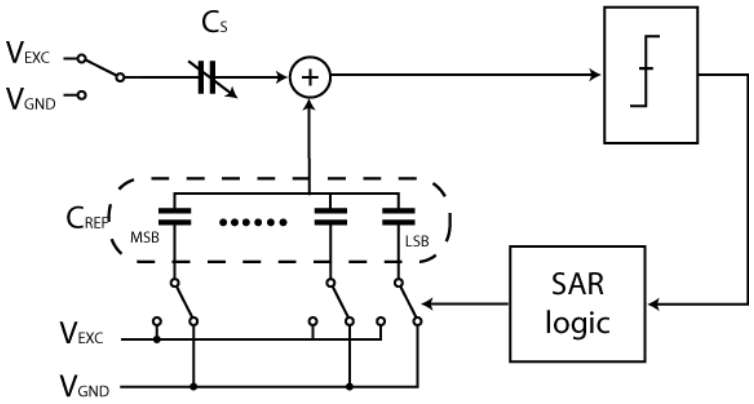


Fig. 2.8: CDC based on SAR converters.

2.2.4. Capacitive sensor interface employing a SAR-based CDC

Another way of measuring capacitance is with a SAR-based CDC. Figure 2.8 shows a block diagram of a SAR-based CDC. The binary-weighted capacitor bank normally used as a sampling capacitor in a SAR ADC will be used here as the reference capacitor C_{REF}. The SAR-based CDC works in two steps. The first step is the sampling step: The input of the comparator is shorted to ground (V_{GND}), (not shown in Fig. 2.8) and C_S is tied to the excitation voltage V_{EXC} while the reference capacitor array is connected to V_{GND}. The second step is the conversion step: The switch connecting the input of the comparator to ground (V_{GND}), (not shown in Fig. 2.8) is open. The switches connected to C_S and C_{REF} will be controlled by a SAR logic, which will compare C_S to the units of C_{REF} starting from the MSB element and ending with the LSB element. The input voltage V_X of the comparator will indicate the relative relationship between C_S and the compared capacitor because of charge conservation.

Depending on the sign of V_X, the corresponding digital bit is determined to be either '1' or '0'. If the bit is '1' the corresponding capacitor unit will be connected to V_{REF} in the remaining SAR conversion cycles. The conversion continues until the LSB is defined [34].

SAR-based CDCs can be made relatively fast, and due to their simple structure, they can be made very power-efficient as well. However, due to the limitations in component mismatch, the maximum resolution of this type of CDCs is limited to the low- or medium-resolution ranges, and so is the precision.

2.2.5. Comparison and Discussion

As can be seen from the discussions in this section, over the years a variety of interface principles for capacitive sensors have been developed. These solutions cover a wide range of application specifications. It is therefore important to compare the performance of different interfacing principles from different angles to be able to select the most suitable principles for use in building a capacitive displacement sensor interface system that can address the challenging specifications presented in Chapter 1. The performance of the prior art has been summarized below.

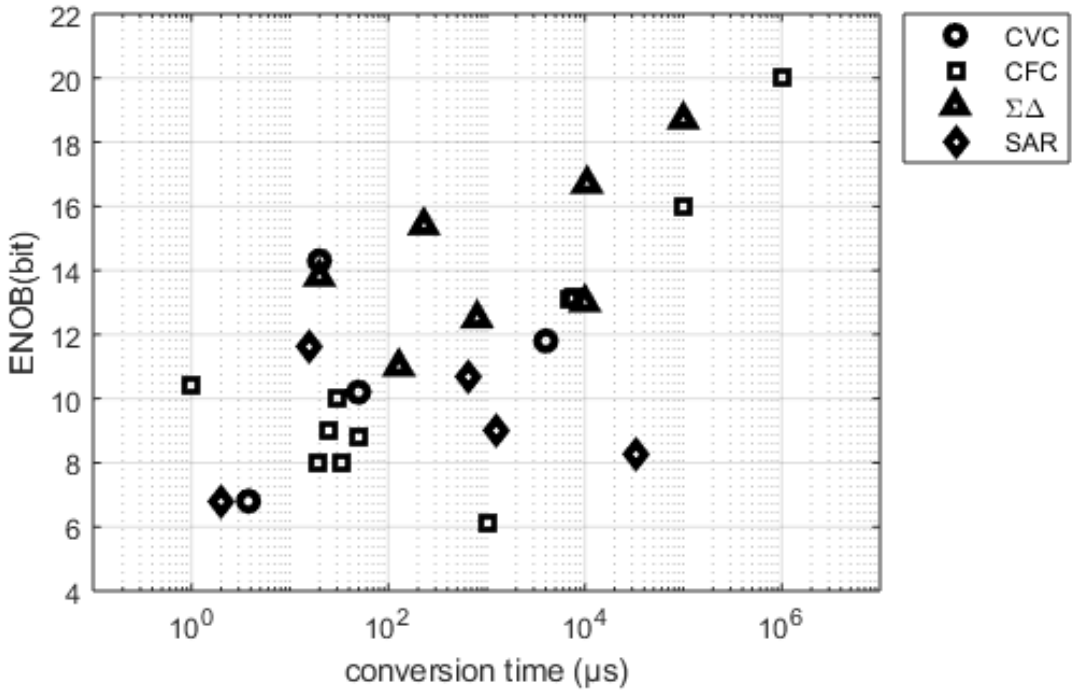


Fig. 2.9: Achievable ENOB and conversion time of various capacitive sensor interfaces

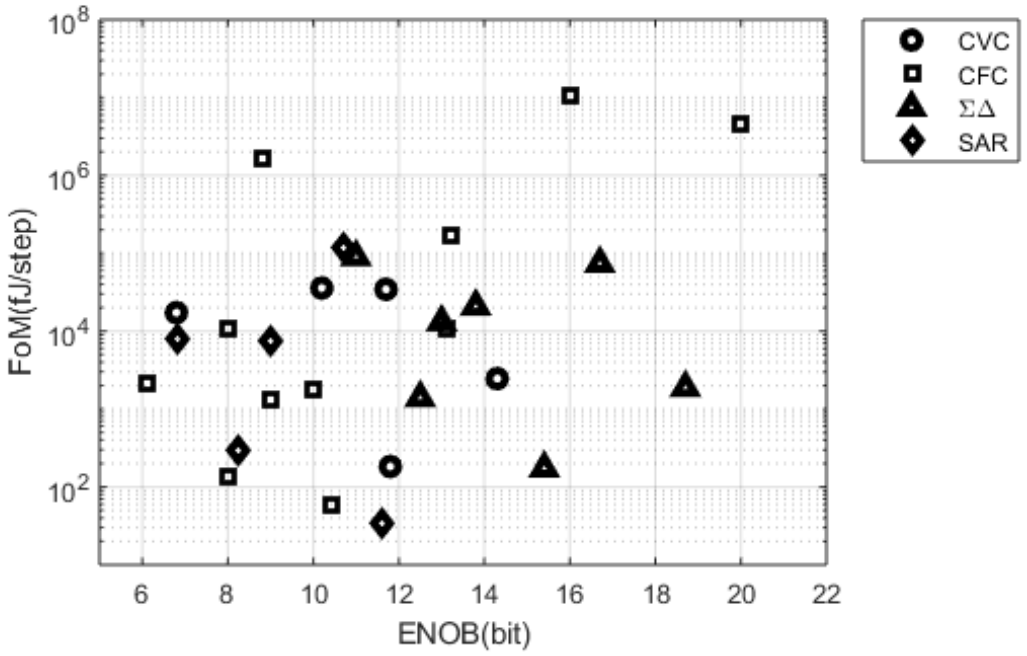


Fig. 2.10: Energy efficiency of different types of capacitive interface circuits.

The effective number of bits (ENOB) of an interface is a very important performance indicator as it not only captures the resolution of a circuit, but also its linearity. In Fig. 2.9, the ENOB achieved by various capacitance interfaces are plotted in relation to their conversion time.

Included in this survey are representative designs from recent years of CVC [8, 11-13, 37], CFC [15-17, 21 ,24 ,26, 27, 38-40], ΣΔ-based CDC [31, 32, 42-46], and SAR-based CDC [33-35, 47, 48]. It can be seen from Fig. 2.9 that generally speaking, the higher the resolution target, the longer conversion time is needed. The upper left corner in Fig. 2.9 stands for high-resolution, high-speed applications. Among those principles, only ΣΔ-based CDCs and CDCs based on a CFC with relaxation oscillator/period modulator realization have been able to achieve ENOBs greater than 13 bits. Both principles make use of the intrinsic linearity offered by the architecture and utilize oversampling to increase resolution [29,36]. However, CFC-based interfaces show speed disadvantages compared to their ΣΔ-based counterparts.

To facilitate the comparison of energy efficiency across interface circuits with different ENOBs, the figure-of-merit (FoM) is defined as:

$$FoM = \frac{Energy\ per\ conversion}{2^{ENOB}} \tag{2.8}$$

Figure 2.10 shows the energy consumption per conversion step of various CDC designs as a function of the ENOBs. For the same ENOB, the lower the amount of energy that is consumed per conversion step, the better the energy efficiency achieved. The unit of this FoM is energy/step. In Fig. 2.10, the designs situated closer to the bottom have better energy efficiency.

Generally speaking, the FoMs that can be achieved by CDCs are lower compared to those of ADCs. This is because unlike ADCs, the reported CDCs may operate under quite different circumstances. For example, CDCs often operate with large parasitic input capacitances, which influences power efficiency in a negative way, while lowering the resulting FOMs of the CDCs.

It is noticeable that SAR-based CDCs achieves the best FoMs. However, all the designs are in low to medium ENOB regions. CVC-based CDCs can also achieve good energy efficiency, because an optimal power budget can be made available for the CVC and the ADC separately. The CFC-based capacitive interface circuits cover a large spectrum of ENOB values ranging from low to high. On the low ENOB side, designs utilize relatively simple building blocks, thus facilitating good energy efficiency. When higher ENOBs are required, the energy efficiency drops.

It can also be seen that among designs that have achieved high ENOBs, ΣΔ-based CDCs achieve better energy-efficiency compared to CFC-based CDCs, while at the same time achieving a shorter conversion time. As we will see from the discussion in the next section, ΣΔ-based CDCs at the same time have a very versatile architecture that has the potential to further increase the conversion speed and energy efficiency.

2.3. Capacitance measurement systems

A capacitive displacement measurement system consists of a sensor head and an interface circuit, which also contains the reference. In order to achieve accurate displacement measurement, the accuracy of both the sensor head and the interface matters. For the interface circuit, the properties of the reference are also an important point of consideration. In the previous two sections the capacitive displacement sensor modeling and the capacitive sensor interface circuit principles were introduced. In this section, a system-level analysis will be presented.

2.3.1. Reference selection

For precision capacitance measurement, the interface circuit needs to provide accurate signal processing, for which the reference plays an important role. The reference quality includes: stability, aging, tolerances, all of which are important when it comes to precision capacitance measurement.

From the discussion in Section 2.2, it became clear that the capacitive interface circuit works by comparing the unknown capacitance with a reference capacitance, or an equivalent reference capacitance that is built from a combination of other references. The ultimate precision of the measurement is thus determined by the quality of the reference that is used in the system.

The selection of the reference used in a capacitive interface circuit is determined by the accuracy requirements of the targeted application. In most of the literature that we could find, the stability of the reference used in the capacitive sensor interface circuit was not separately discussed. The reason is that for most capacitance measurement systems, the absolute accuracy of measurement is often not that important. For instance, the capacitive humidity sensor discussed in [3] aims for an accuracy in the order of 1%, because the target humidity-sensing error after calibration is only in the order of 1%. In such cases, a reference capacitance is the natural reference choice, since a comparison with the unknown capacitance can be directly made.

However, capacitive references have limited accuracy, and even after calibration, show noticeable temperature drift and aging. In [5], a benchmark of possible capacitance references shows that the best available off-the-shelf capacitors have a roughly 30 ppm/°C temperature drift, 0.1 % tolerance and 300 ppm/year time drift (aging). The study also shows that the better the quality of the capacitor, the bulkier it is. For example, capacitive standards used in metrology have a thermal drift of only 2 ppm/°C, ±0.005% tolerance, and below 20 ppm/year aging [5]. However, those capacitance references are enormous in size and not practical.

The integrated capacitors have a comparable temperature coefficient. Both Metal-Insulator-Metal (MIM) and Polysilicon-Insulator-Polysilicon (PIP) capacitors report a nearly 30 ppm/°C temperature coefficient, while their long-term drift is often not reported.

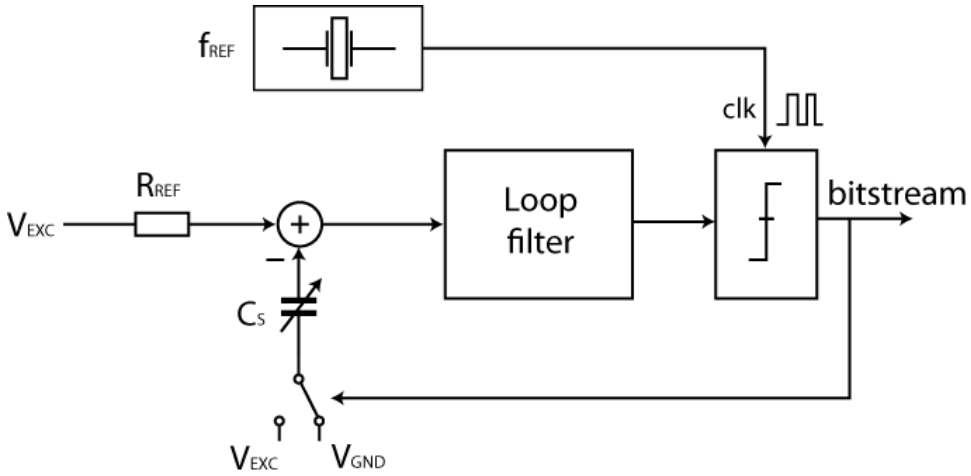


Fig. 2.11: Charge-balancing that measures a sensor capacitor with the combination of a precision resistor reference and precision frequency reference.

On the other hand, as was pointed out in [5], both resistive references and frequency/time references exist that have better accuracy and stability than practically available capacitive references. For instance, VPG VHA412Z metal foil resistors have a rated temperature coefficient of 2 ppm/°C and a long-term drift of 2 ppm/6 years [49], while commercially available temperature-compensated crystal oscillators provide accuracy up to 0.1 ppm while having a sub-ppm/°C level temperature coefficient [50]. Although both components are still off-chip, their sizes are much smaller compared to the primary capacitance standard.

Despite the added complexity of comparing an unknown capacitor with an equivalent capacitive reference, the design with a resistive and frequency reference has the potential of achieving better accuracy and long-term stability. By utilizing ultra-stable reference resistors and a crystal oscillator, the interface circuit in [5] achieves thermal stability of ± 7.5 ppm/°C, which also demonstrates good long-term stability.

2.3.2. Speed-accuracy trade-off

From the point of view of the measurement accuracy, it is clear from the last section that because of the better stability offered by resistive and frequency references, a capacitive interface based on these types of references could have both better thermal and long-term stability. However, since the comparison between an unknown capacitor and an 'equivalent' reference capacitor created by a reference resistor and a crystal oscillator is not a direct one, there are also limitations with respect to power efficiency.

The design in [5] employs a ΣΔ-based CDC with two charge balancing branches, as shown in Fig. 2.11. The unknown capacitor is used to create a switched-capacitor branch, just as in a conventional ΣΔ-based CDC. The reference resistor is first converted into current by a resistance-to-current converter, using a reference voltage V_{EXC}. Then, the combination of this current and a crystal-based time reference generates an equivalent reference charge. The sensor capacitor is incorporated into a switched-capacitor circuit which turns the sensor capacitance into a signal charge using the same reference voltage V_{EXC}. The modulator balances the signal charge against the charge supplied by the reference current. Since both the signal charge and the reference charge are proportional to V_{EXC}, the output is thus insensitive to the exact value and the drift of V_{EXC}, provided that the drift of V_{EXC} is much slower than the conversion time.

While this principle works reasonably well at lower speeds (clock frequency of 200 kHz in [5]), achieving the same level of performance while greatly improving the measurement speed is challenging, as two major limitations are present. First, the finite speed at which the switches turn the reference current, which has a continuous-time nature, on and off will create clock non-idealities. Second, the finite speed of the resistance-to-current converter also limits the maximum operating speed of this type of CDC [5].

It seems very difficult to find a single interface circuit that can achieve both high speed and high accuracy. However, from a system-level point of view, the problem can potentially be solved.

2.3.3. System-level solution

It is important to understand that solving all issues with a single design is not necessary. In fact, we can combine different designs to construct a capacitance measurement system, in which each design inside the system addresses one or several specific properties.

This idea is further illustrated in the block diagram shown in Figure 2.12. A high-speed, high-resolution, low-power CDC (main CDC) can be built by utilizing a good capacitor as its reference. Since no reference conversion is needed, by directly using a capacitor as the reference of the CDC the circuit solution can be quite straightforward. At the same time, being a switched-capacitor circuit, it is less prone to many circuit errors such as clock jitter, etc. [17]. To deal with the slow drifting of the capacitance reference value due to temperature and aging, an additional low-speed, low-power and high-precision CDC (auxiliary CDC) can be used to periodically calibrate the reference capacitor inside the main CDC. This auxiliary CDC does not require access to the reference capacitor inside the main CDC. Such a calibration can for instance be realized by consequently measuring the same capacitor with both the main CDC and auxiliary CDC, as shown in Fig. 2.12. The

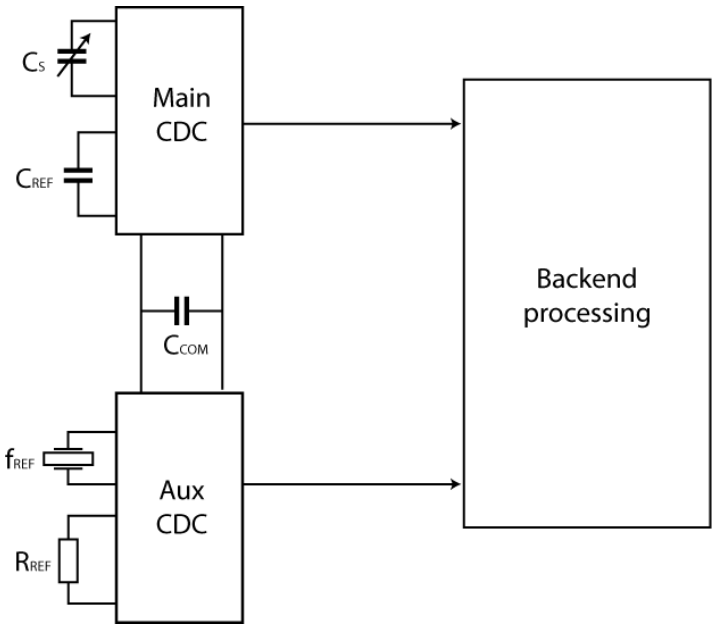


Fig. 2.12: Capacitance measurement system composed of a fast main CDC and a slow but high-precision auxiliary CDC.

results can then be compared, and the calibration can be applied to the main CDC. The periodicity of the calibration will depend on the application precision requirement and the drift of the capacitance reference. The main CDC only needs to guarantee that the drift is negligible within a relatively short time between two calibrations, which is much easier to achieve.

2.3.4. Placement of interface circuit

In some situations, the capacitive sensor is directly integrated on-chip where the interface circuit is located [3], whereas if the sensor fabrication technology is not compatible with that of the interface circuit, they are placed in the same package. The motivation here is to minimize the associated parasitic capacitance to ground, because excessive parasitic capacitance will not only degrade the achievable resolution of the interface circuit, but also loads the interface and causes extra energy consumption.

When interfacing an off-chip sensor, it is also the case that the best performance of an interface circuit can be achieved when it is integrated into the sensor head, thus avoiding the use of cables between the capacitive sensor and the interface circuit.

The sensor head of an advanced displacement sensor is very sensitive to variations in the environment such as temperature and humidity changes, because all these changes will affect the property of the sensor head. Therefore, it is important to keep the dissipation of the interface circuit from self-heating to a reasonable and constant level.

2.4. Conclusion

In this chapter, the background of capacitive displacement sensors and capacitance interface circuits is discussed. The discussion of the interface circuit is extended to the references used.

The biggest limiting factor on the sensor head is alignment, since stand-off distance must be minimized to maximize resolution. Advanced alignment techniques are required to bring down the stand-off distance, so that the dynamic range requirement of the interface circuit can be more realistic. Many interface principles for capacitive sensors are available, however, most of the interface circuits have relatively low precision and low stability, mainly due to the quality of the references used in those interface circuits. An alternative, more stable and more accurate reference struggles reaching a high conversion speed and good power efficiency.

A promising solution is to combine two interface circuits onto a single chip (a system-on-chip) or in a single package (system-in-package): (i) one fast, highly sensitive and energy-efficient interface operating continuously in real time, periodically calibrated by a (ii) second stable and accurate interface, which is "sleeping" between two calibrations and hence does not dissipate noticeable additional energy during normal operation.

The rest of the thesis presents an investigation of this approach with focus on the fast and energy-efficient interface. Methods are proposed, and implementations are reported which improve the conversion speed and the energy efficiency of the interface circuit using a capacitive reference. An accurate and stable, but relatively slow interface solution, which can be integrated with the solutions proposed here, is reported in [32].

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Chapter 3

High-Speed High-Precision Capacitive Sensor Interface with Baseline Capacitance Compensation

3.1. Introduction

As discussed in the previous chapter, capacitive sensor interface circuits based on a capacitive reference suffer from low stability, mainly due to the limited stability of the capacitive reference. On the other hand, circuits that utilize a more stable and more accurate reference have been shown to have difficulty in achieving a high conversion speed. Towards the end of Chapter 2, it was shown that it is possible to split the functionality of the capacitive sensor interface into two types of operation. The first is a real-time high-speed, high-resolution, low-power operation with the addition of an auto-alignment function in the sensor head (mechanical zoom-in), and the second is a low-speed, high-stability, high-precision and relatively low-power operation, to be used periodically for self-calibration. In this chapter, the focus will be on the investigation of a capacitive sensor interface with real-time high-speed high-resolution and low-power.

In order to build an interface circuit that can achieve a high speed, high resolution, and at the same time low power consumption, we can first try to determine the limiting factors

that impede this goal. From Chapter 2 we know that most capacitive sensors suffer from a small modulation factor which results in a relatively large baseline capacitance. This baseline capacitance increases the dynamic range requirement for the interface dramatically and limits the achievable energy efficiency of the interface circuit. Therefore, this baseline capacitance would need to be processed.

3.2. Baseline Capacitance Compensation Principle

The most significant limiting factor for increasing the sensitivity of a capacitive displacement sensor is the minimum amount of stand-off distance to the target which is necessary to compensate for any misalignment of the sensor plates [1]. Although with advanced alignment techniques the stand-off distance could be reduced to tens of micrometers [2], it would still be too large when a limited displacement needs to be measured in the nanometer range. As discussed in Section 2.1, this limit on the stand-off distance would result in a small modulation factor and lead to reduced sensitivity and increased demand on the dynamic range of the interface circuit. Eventually this would lead to energy being wasted, which in capacitive sentence interface circuits located close to the sensor head must be avoided due to stringent power consumption requirement. This section focuses on the circuit technique that can help increase the energy efficiency of a capacitive sensor interface circuit.

3.2.1. Baseline sensor capacitance

For all the capacitive interface principles illustrated in the previous chapter, the allowable variation range of the input capacitance can span from zero to a maximum value that is

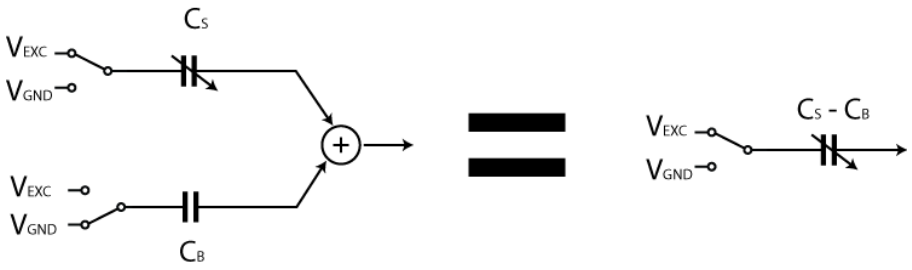


Fig. 3.1: Baseline capacitance compensation.

determined by the circuit parameters of the interface circuit. In the case of the charge-balancing principle, for instance, the maximum allowable sensor capacitance value should not exceed the value of the reference capacitor. The maximum input capacitance to be handled by the interface circuit is determined by the maximum expected value of the sensor capacitance, while the minimum detectable variation of the capacitance is defined by the interface resolution.

It is important to note than the measurement range of a capacitive sensor never starts from zero. In the case of a parallel-plate capacitive displacement sensor, zero capacitance translates into an infinite plate distance. When the displacement measurement range is specified, the capacitance variation range is also determined. In most cases, the full range of the capacitive interface circuit is not utilized in an optimal way, leading to a waste in energy consumption. The static part of the capacitance that makes up for the sensor capacitance is sometimes called baseline capacitance. Since for a capacitive sensor the interest is often in the variation component, it is desired to have the baseline capacitance removed.

One of the most commonly used methods to electrically cancel the baseline capacitor is shown in Fig. 3.1 [3,4]. Conceptually we can split the sensor capacitor C_S into the baseline capacitor C_B and the signal capacitance C_X. Since the baseline capacitance C_B contributes to a charge amounting to $V_{EXC} \cdot C_B$, if we create a charge that amounts to $V_{EXC} \cdot C_B$ and subtract that from the charge contributed by the sensor capacitor, it is then equivalent to removing the baseline capacitance. This can be realized by physically connecting another capacitor with a value equal to C_B, to the circuit and applying an excitation signal V_{EXC} with an opposite sign. Since the charge contributed becomes $-V_{EXC} \cdot C_B$, the net effect is

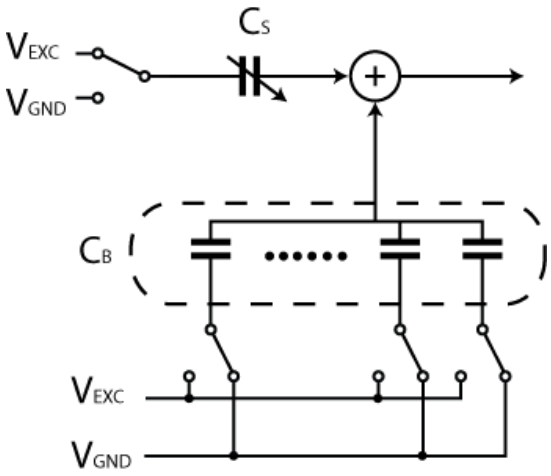


Fig. 3.2: Baseline capacitance compensation with adjustable C_B.

equivalent to C_B being removed from the sensor capacitor C_S in the transfer function of the interface circuit. The dynamic range of the interface circuit after the removal of the base capacitance needs only to cover the varying part of the sensor capacitance, which is often much smaller. The range of the capacitive sensor interface has been effectively zoomed in to the range of interest. We name the factor between the baseline compensation capacitor and the capacitance variation range of the interface circuit with baseline capacitor compensation the "zoom-in factor" α_Z [1]:

$$\alpha_Z = \frac{C_B}{C_{S-max} - C_{S-min}} \tag{3.1}$$

Baseline capacitance compensation can be applied to most of the capacitive sensor interfacing principles discussed in Section 2.2, with a few exceptions. Generally speaking, circuits that employ an active amplifier and have a virtual ground node are best suited for implementing the baseline capacitance compensation. Other than those circuits, a SAR-based interface with passive charge redistribution, as discussed in Section 2.2.4, can also incorporate baseline capacitance compensation, given that the parasitic capacitance to ground is small enough. Circuits where baseline capacitance compensation cannot be implemented include circuits based on ring oscillators and LC oscillators, where a charge subtraction cannot be facilitated.

In cases where the baseline capacitance is a fixed part of the sensor capacitor, C_B can be realized with an invariable capacitor. However, that baseline capacitance is also a subject to variations due to mounting tolerances and drift [5]. Moreover, the capacitor C_B can deviate from its nominal value due to process variations. This is especially a problem when the baseline capacitance takes up much larger portion of the sensor capacitance, compared to the signal-carrying part of the sensor capacitance. In this case a small change in the baseline capacitance will already be equivalent to the sensor variation range. In order to avoid out-of-range operation, the gain applied in baseline capacitance compensation must be limited, reducing the dynamic range advantage that could be gained with this technique.

This issue can be partially solved by making the baseline capacitor C_B adjustable [4], as shown in Fig. 3.2. In the initialization phase, an algorithm such as a successive approximation register algorithm can be used to determine the approximate value of the baseline part of the sensor capacitor by adjusting the value of C_B according to the relative size of C_B and C_S, which is available through a comparison algorithm similar to the successive approximation algorithm. This would also allow the interface circuit to cover a wider sensing capacitance variation range, while still maintaining a high zoom-in factor within each sub-range.

3.2.2. Circuit implementation issues of baseline capacitance compensation

Although there are many advantages of applying baseline capacitance compensation to capacitive sensor interface circuits, so far we have only discussed the benefits. However, it makes sense to also point out the implications of applying such a technique from a circuit design point of view, as these implications have a great impact on circuit performance, especially when the desired zoom-in factor becomes large.

We begin our analysis by first studying a typical switched-capacitor integrator stage as shown in Fig. 3.3. The circuit works in two phases. In Φ_1 the OTA is set to unity-feedback mode and the input capacitors are reset, while in Φ_2 the charge is transferred from the input capacitors onto the integration capacitor. The amount of charge that is transferred to the integration capacitor can be approximated as:

$$V_o = V_{EXC}\frac{C_S - C_B}{C_{INT}} \tag{3.2}$$

Here it is assumed that the OTA holds the virtual ground node still and that the voltage remains unchanged before and after the charge transfer. In reality, for various reasons, the virtual ground voltage will change slightly, which in turn leads to an error term in Eq. 3.2.

From the theory on feedback [6], we know that in reality, the transfer function deviates from the ideal shown by Eq. 3.2. There are three main charge-transfer error sources that contribute to the error in the output voltage change: static error ε_{static}, dynamic error $\varepsilon_{dynamic}$, and random noise $\overline{v_{no}^2}$. Specifically, the first two errors are deterministic in nature while the last one is classified as random error. Equations 3.3 to 3. summarize the nature of these errors.

$$\varepsilon_{static} \approx \frac{1}{T_{LG}} \tag{3.3}$$

$$\varepsilon_{dynamic}(t) = e^{-t/\tau} \tag{3.4}$$

$$\overline{v_{noT}^2} = \frac{kT \cdot N_f}{\beta \cdot (C_L + \beta C_{INT})} \tag{3.5}$$

T_{LG} is the loop-gain of the feedback amplifier and is expressed as $T_{LG} = A_{DC}\beta$; τ is the time constant of the feedback amplifier and is expressed as $\tau = \frac{C_{Leff}}{\beta g_m}$; while $\beta = \frac{C_{INT}}{C_{INT}+C_S}$ is the feedback factor of the feedback amplifier. N_f is the noise factor that is related to the OTA topology. It can be seen that the feedback coefficient β plays an important role in all three error sources. When β decreases, the loop-gain reduces, while the time constant and noise increase.

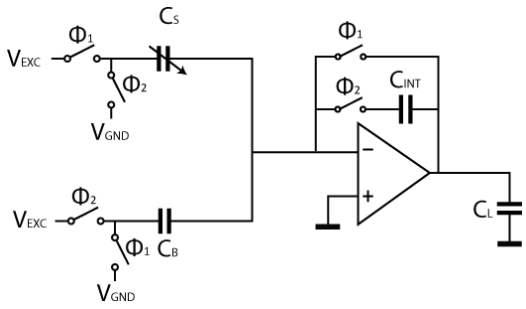
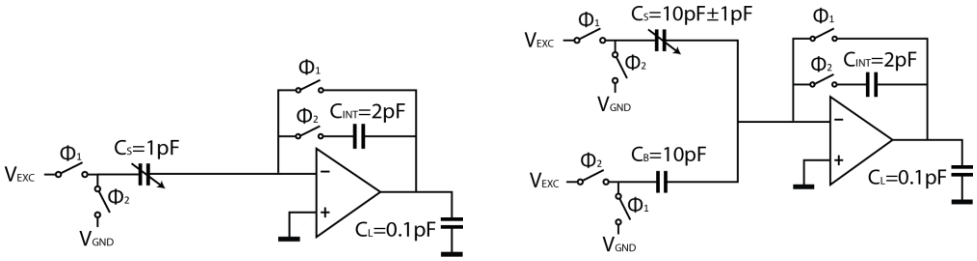


Fig. 3.3: Switched-capacitor integrator stage.



(a) (b)

Fig. 3.4: Switched-capacitor integrator stage with different zoom-in factors.

Consider then the two circuits with baseline capacitance compensation in Fig. 3.4, both of which have the same transfer function in terms of signal. The circuit in Fig. 3.4 (a) has a sensor capacitor of 1 pF without baseline capacitance compensation, while the circuit in Fig. 3.4 (b) has a sensor capacitor of 10 pF with baseline capacitance compensation. Suppose that in both cases, the value of the integration capacitor C_{INT} is chosen to be 2 pF. We can calculate that for the circuit in Fig. 3.4 (a), the feedback factor $\beta_1 = \frac{2}{3}$; while for the circuit in Fig. 3.4 (b), the feedback factor $\beta_2 = \frac{2}{23}$, which is almost 1/8 of β_1. As can be seen, realizing baseline capacitance compensation will inevitably lead to a decrease in the feedback factor β. Moreover, since the feedback factor β is linked to almost all the circuit performance parameters of the feedback amplifier, a decrease in β will affect all those parameters. Decreasing β will also reduce loop gain T_{LG}, which will in turn cause larger static error ε_{static} in the charge transfer process.

Decreasing β will also increase the time-constant of the feedback amplifier if nothing else changes. From another angle, in order to keep the time constant unchanged, the transconductance g_m of the amplifier needs to increase, which translates into a larger bias current requirement and hence higher power consumption. Last but not least, decreasing β

affects the thermal noise of the circuit. In fact, the reciprocal of β is often referred to as the noise gain of the circuit, as the smaller β is, the more noise there will be in the circuit. It is thus important to keep these effects in mind when designing an interface circuit that utilizes baseline capacitance compensation.

3.3. Displacement Measurement with a Capacitive Sensor Incorporating Baseline Capacitance Cancellation

In this section we will investigate aspects of displacement measurement using a capacitive displacement sensor that incorporates baseline capacitance cancellation. In particular, we will extend the idea of splitting the measurement task into three sub-tasks to produce a capacitance displacement measurement that is high-precision, high-resolution, high-speed and low-power. Here with the preceding information about capacitive sensor measurement principles we can allocate the suitable principles to the different sub-measurements.

3.3.1. System-level consideration

Since the desired quantity to be measured is the displacement, not the absolute distance, the measurand of interest is then the difference between two measurements. The value of the sensor capacitance C_S can be written as:

$$C_S = \frac{\varepsilon A}{d} \tag{3.4}$$

where ε is the dielectric constant of air, A is the area of the capacitive sensor plate and d is the distance between the plates. When the value of the distance is the same as the stand-off distance d_0, the value of C_S will be exactly the same as the baseline-compensation capacitor C_B:

$$C_B = \frac{\varepsilon A}{d_0} \tag{3.5}$$

When we use the baseline-compensating capacitance C_B as a reference, the displacement can be expressed as:

$$\begin{aligned} \Delta d = d_1 - d_2 = \frac{\varepsilon A}{C_{S1}} - \frac{\varepsilon A}{C_{S2}} = \frac{\varepsilon A}{C_B} \cdot \left(\frac{C_B}{C_{S1}} - \frac{C_B}{C_{S2}}\right) \\ = d_0 \cdot \left(\frac{C_B}{C_{S1}} - \frac{C_B}{C_{S2}}\right) \end{aligned} \tag{3.6}$$

The ratio of the baseline-compensating capacitance C_B and the sensor capacitance C_S cannot be obtained directly, since in the circuit their difference $C_S - C_B$ is measured in relation to a reference capacitor C_{REF}. In other words, the ratio $\frac{C_{S1}-C_B}{C_{REF}}$ and $\frac{C_{S2}-C_B}{C_{REF}}$ can be measured. If the ratio $\frac{C_B}{C_{REF}}$ can also be obtained, then we can indirectly calculate the ratio between C_B and C_S:

$$\frac{C_B}{C_S} = \frac{\frac{C_B}{C_{REF}}}{\frac{C_S - C_B}{C_{REF}} + \frac{C_B}{C_{REF}}} \tag{3.7}$$

Substituting Eq. 3.7 with Eq. 3.6 we reach:

$$\Delta d = \frac{\varepsilon A}{C_B} \cdot \left(\frac{\frac{C_B}{C_{REF}}}{\frac{C_{S1} - C_B}{C_{REF}} + \frac{C_B}{C_{REF}}} - \frac{\frac{C_B}{C_{REF}}}{\frac{C_{S2} - C_B}{C_{REF}} + \frac{C_B}{C_{REF}}} \right) \tag{3.8}$$

Thus, in order to extract displacement information from the capacitive sensor interface circuit incorporating baseline capacitance cancellation, three types of measurements are required. One is the absolute capacitance measurement of the baseline compensation capacitance C_B to determine d_0, while the other two are capacitance ratio measurements, namely $\frac{C_B}{C_{REF}}$ and $\frac{C_S - C_B}{C_{REF}}$.

Essentially the last measurement is the only one which involves the sensor capacitor C_S. Because of the baseline capacitance compensation technique used in this measurement, the resolution requirement of this measurement is relaxed in the view of quantization noise. The other two measurements still require relatively high resolution. However, they are measurements of static capacitances. Since we expect the drift of C_B and C_{REF} to be very slow, more measurement delay can be tolerated without causing noticeable error. Also, these two measurements do not need to be performed regularly but can be performed during the available calibration period.

3.3.2. System error budgeting

The total measurement error in displacement Δd of the measurement system described in the last section consists of the measurement errors from all three sub-measurements. To further quantify the allowable error in each measurement, let us take as an example a final displacement measurement error Δd below ±160 pm. Our task is to define how sensitive the obtained value for Δd is to the three sub-measurement results. For simplicity, we define:

$$d_0 = \frac{\varepsilon A}{C_B} \tag{3.9}$$

$$\alpha = \frac{C_S - C_B}{C_{REF}} \tag{3.10}$$

$$\beta = \frac{C_B}{C_{REF}} \tag{3.11}$$

$$\gamma = \frac{\beta}{\alpha + \beta} = \frac{C_B}{C_S} \tag{3.12}$$

In this way we can express the displacement with the following simplified equation:

$$\Delta d = d_0(\Delta\gamma) \tag{3.13}$$

The sensitivity of Δd to errors in d_0 and $(\gamma_1 - \gamma_2)$ can be calculated respectively as:

$$S_{d_0}^{\Delta d} = \frac{\partial(\Delta d)}{\partial d_0} = \Delta\gamma \tag{3.14}$$

$$S_{\Delta\gamma}^{\Delta d} = \frac{\partial(\Delta d)}{\partial(\Delta\gamma)} = d_0 \tag{3.15}$$

We can further express $\Delta\gamma$ as:

$$\Delta\gamma = \frac{C_B}{C_{S1}} - \frac{C_B}{C_{S2}} = \frac{C_B(C_{S2} - C_{S1})}{C_{S1}C_{S2}} \tag{3.16}$$

As the change in the sensor capacitance of interest is much smaller than the nominal value, and the baseline compensation capacitance is very close in value to the sensor capacitance, we can approximate Eq. 3.16 as:

$$\Delta\gamma \approx \frac{C_B(\Delta C_S)}{C_S^2} \approx \frac{\Delta C_S}{C_S} \tag{3.17}$$

In fact, $\Delta\gamma$ can also be written in terms of plate distance:

$$\Delta\gamma = \frac{\Delta d}{d_0} \tag{3.18}$$

Therefore, in the target system, $\Delta\gamma < \pm 2500$ppm, given that d_0 is around 10μm and Δd is less than ±25nm during normal operation. This means that to guarantee a maximum error for Δd below ±160pm, the maximum allowable error in d_0 must be below ±40 nm. From this we can conclude that the measurement of the absolute value of C_B does not have to be much more accurate than ±40fF out of a nominal capacitance of 10pF to fulfill the requirement. In [5] a CDC based on a precision resistor together with a crystal oscillator is employed to produce an equivalent high precision capacitive reference to achieve an absolute accuracy of greater than ±25fF, which is suitable for this measurement task.

On the other hand, the measurement error of $\Delta\gamma$ needs to be below ±16 ppm to guarantee a maximum error for Δd below ±160pm. This is necessary because the nominal value of d_0 is 10μm. Since $\Delta\gamma$ itself is a combination of two types of capacitance ratio measurements, it makes sense to break it down and find out the allowable error for each type of measurement. The following simplification can be made to the analysis:

$$\Delta\gamma = \frac{\beta}{\alpha_1 + \beta} - \frac{\beta}{\alpha_2 + \beta} = \frac{\beta(\alpha_2 - \alpha_1)}{(\alpha_1 + \beta)(\alpha_2 + \beta)} \approx \frac{\Delta\alpha}{\beta} \tag{3.19}$$

In the final step, the approximation is based on the fact that β, which is the ratio between the baseline-cancellation capacitor and the reference capacitor, is much larger than the ratio between the capacitance difference and the reference capacitor. We can then proceed to formulate the sensitivity of $\Delta\gamma$ to errors in $\Delta\alpha$ and β:

$$S_{\Delta\alpha}^{\Delta\gamma} = \frac{\partial(\Delta\gamma)}{\partial(\Delta\alpha)} \approx \frac{1}{\beta} \tag{3.20}$$

$$S_{\beta}^{\Delta\gamma} = \frac{\partial(\Delta\gamma)}{\partial\beta} \approx \frac{\Delta\alpha}{\beta^2} \tag{3.21}$$

The nominal value of β and the range of $\Delta\alpha$ both depend on the value of the reference capacitor C_{REF}. Suppose that C_{REF} is 100fF, which is sufficient to cover the variation range

of the sensor capacitance while leaving some margin. The nominal value for β is then equal to 100, and the maximum range of $\Delta\alpha$ will be ±0.5.

From these results, assuming that $\Delta\alpha$ is the only source of error, we can tolerate a maximum tolerable error of about ±1600 ppm in $\Delta\alpha$, if the error of $\Delta\gamma$ must be below ±16 ppm. Then the maximum tolerable error of β will be ±0.32. Considering that β has a nominal value of 100, this translates into a ±3200 ppm relative error in the measurement of β itself.

Although it seems that the measurement of β has a more relaxed specification than the measurement of α, the total error must be budgeted among all three error sources. As the measurement of β is the ratio of two constant capacitors, there are no stringent conversion time requirement for β measurement. In fact, β can be measured during calibration intervals. Therefore, in practice, the measurement of β should be given only a small fraction of the total error budget. The measurement of α directly involves the sensor capacitor and therefore determines the measurement delay. This measurement will have the largest impact on the total power consumption of the system, therefore a greater amount of the error budget should be allocated to the measurement of α.

3.4. Discussion and conclusion

In this chapter, we have focused the discussion on ways to reduce the impact of challenges posed by the large baseline capacitance of a capacitive sensor interface circuit. The electrical method of cancelling the effect of the baseline capacitance of the sensor helps to reduce the dynamic range requirement for the interface circuit and gives more flexibility to the design. However, this technique also brings some challenges that need to be addressed.

3.4.1. Appropriate interfacing principles

Based on the error budget calculation in the previous section, the most appropriate interfacing principles for all three sub-measurement tasks can be selected. Table 3.1 provides a summary of specification requirements for the three sub-measurements, respectively.

Table 3.1: Summary of requirements of sub-measurements.

Measurement	***Primary specification***	***Additional requirements***
d_0	Absolute accuracy	Excellent stability, low-power
$\frac{C_B}{C_{REF}}$	High resolution, linearity	Good stability, low-power
$\frac{C_S - C_B}{C_{REF}}$	High speed	Good stability, low-power

For the d_0 measurement, the most critical requirement is absolute accuracy. The reference used for this measurement should have a high absolute accuracy and a very low drift. As studied in [5], the most accurate and stable reference to date can be composed by combining an accurate resistive reference and a frequency/time reference. In order to limit other errors rising from the circuit non-idealities, a ΣΔ-based interfacing principle has been chosen. We know from the previous sections that ΣΔ-based capacitive sensor interfaces can achieve high resolution and high accuracy. The relatively limited conversion speed and energy efficiency of the ΣΔ-based capacitive sensor interfaces are not a limiting factor for the d_0 measurement, as the measurement speed requirement is not high.

For the C_B/C_{REF} capacitance ratio measurement, the important specifications are high resolution and high accuracy. The speed of this measurement can be low as stated before. Both ΣΔ-based capacitive sensor interface circuits and capacitive sensor interface employing capacitance-to-frequency converters (CFCs), such as interface circuits based on a period modulator, can achieve this requirement.

For the measurement of $(C_S - C_B)/C_{REF}$, the most critical specifications are high measurement speed and limited power consumption. Again, ΣΔ-based capacitive sensor interfaces with baseline capacitance compensation have shown good potential in achieving high conversion speed with reasonable energy efficiency. Alternatively, CVC-based capacitive sensor interfaces with baseline capacitance compensation could potentially also achieve high measurement speed. Combined with a general-purpose energy-efficient ADC, this solution also seems worthy to consider.

3.4.2. Conclusion

Based on the discussions in this chapter, an investigation of design techniques for high-speed capacitive sensor interface circuits will be presented in the following chapters. In Chapter 4, a high-speed capacitance measurement system will be discussed that strives to take full advantage of the zoom-in and baseline capacitance compensation techniques. Alternatively, in Chapter 5, another method, potentially suitable for realizing a high zoom-in CVC, is presented, and the additional steps to realize a complete high-speed capacitance measurement system will be analyzed.

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Chapter 4

Capacitive Sensor Interface Using a Charge-Balancing Principle

This chapter presents a high-speed high-precision capacitance-to-digital converter (CDC) using a charge-balancing ΣΔ modulator. It is demonstrated that with the same circuit, both a high-speed measurement and a lower-speed high-resolution calibration step can be realized. The combined result has the desired low-latency due to the fast measurement, while achieving high-precision as well.

4.1. Introduction

The charge-balancing principle combined with ΣΔ modulation is one of the most applied principles in capacitive sensor readout circuits. The basic operation principles of the ΣΔ modulator have been discussed briefly in Section 2.3 of Chapter 2, in which the major advantages, such as high achievable measurement resolution and high DC measurement precision have been reported. Because ΣΔ modulation makes use of oversampling, the increase in resolution comes ultimately at the cost of an increase in the oversampling ratio (OSR), which in turn leads to an increased measurement time. For most sensor readout circuits with a limited signal bandwidth, this increase is not a problem. However, applying this technique in high-speed low-latency circuits, used for example in servo-systems, is not so straightforward. In order to achieve larger than 50 kHz of signal bandwidth, which is our research target, a moderate OSR value of 256 would demand a modulator sampling clock of 12.8 MHz. For existing CDCs, such a high sampling clock frequency is not usual.

The direct disadvantage of using a high sampling clock frequency is the associated higher power consumption. As discussed in Section 2.4, a higher sampling frequency requires shorter settling time for the amplifier in each cycle, meaning that more bias current in the OTA is needed to charge the same load capacitances.

A high sampling frequency also brings other issues. When the sampling frequency increases, the on-resistance of the switches in the circuits needs to be reduced in order to prevent the time constant related to the RC network from limiting the settling time of the circuit. This would lead to the use of large switches. As the channel charge of MOS switches is proportional to the switch size, using large switches will inevitably lead to large charge-injection errors [1], which may limit the achievable accuracy. From both a power and accuracy point of view, increasing the sampling frequency should be avoided.

In the following sections, techniques that can be used to reduce the required sampling frequency of a CDC will be discussed.

4.2. System-level considerations

4.2.1. Overview

This section describes a capacitive-sensor interface circuit based on the charge-balancing principle as discussed briefly in Section 2.2.3 of Chapter 2. Since the goal here is to design a power-efficient capacitance-to-digital converter (CDC), the oversampling ratio (OSR) required to obtain a certain level of capacitance resolution should be minimized. The capacitance resolution in a CDC can be limited by both thermal noise and quantization noise. By increasing the OSR both thermal noise and quantization noise tend to reduce. The difference however is that thermal noise drops by only 0.5 bits per doubling of the OSR, while quantization noise, depending on the loop filter order, can drop at a much faster rate [2]. Generally speaking, the resolution of a CDC will be dominated by the quantization noise at a low OSR and by thermal noise at a high OSR. There will be a corner OSR at which the dominant noise source of the CDC will turn from quantization noise into thermal noise.

It has been shown in the noise analysis in Chapter 2 that the relationship between thermal noise and the OSR in a CDC depends on the total input capacitance value, to the first order. In most applications, the total input capacitance is directly linked to the size of the sensor capacitance. In this sense, the relationship between the OSR and the thermal-noise-limited

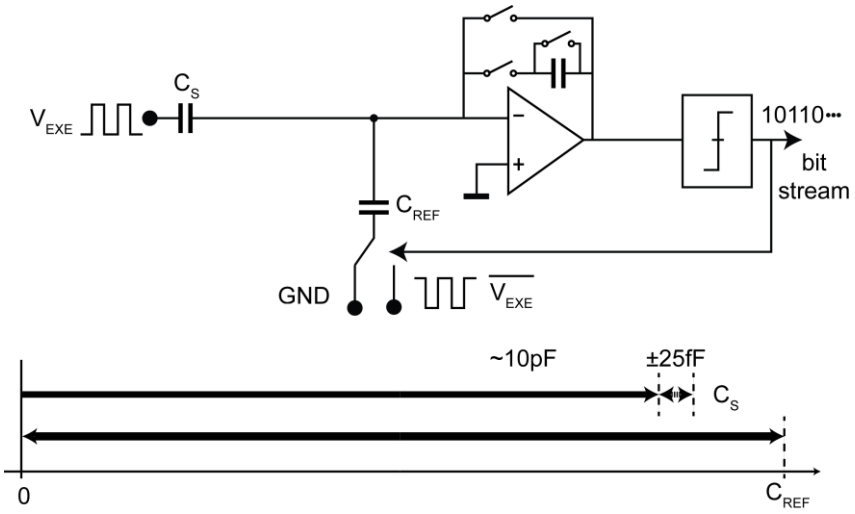

Fig. 4.1: Simplified block diagram of a CDC.

capacitance resolution cannot be easily influenced. Hence the minimum OSR required to bring the thermal noise level down, in order to achieve the target capacitance resolution, is in effect the minimum possible OSR required to achieve a certain target capacitance resolution. The CDC must be designed such that at the target capacitance resolution level, the CDC is thermal-noise limited. This involves bringing the corner OSR of the CDC to a level lower than the minimum OSR required by the thermal noise.

In the following sections, methods to bring down the corner OSR will be discussed, leading to a power-efficient CDC architecture.

4.2.2. Power-efficient capacitance-to-digital converter

A simplified block diagram of a CDC is shown in Fig. 4.1, in which the ΣΔ modulator is used to determine the ratio of the sensor capacitance C_S and a reference capacitance C_{REF}. In order to achieve charge balancing, the charge that is supplied by the input branch $Q_S = V_{EXC}C_S$ needs to be balanced by the same amount of charge with the opposite sign

supplied by the reference branch. The range of the compensating charge is from 0 to $Q_{REF} = V_{EXC}C_{REF}$, as can be seen in Fig 4.1. As is mentioned in Chapter 2, for high-precision capacitive displacement sensors, the variation in the sensor capacitance is much smaller compared to the nominal value. Therefore, it can be concluded that with this architecture a large part of the full-scale range of the CDC is used to accommodate the baseline capacitance of C_S. Assuming that the minimum required value of C_{REF} is 10pF, then a capacitance resolution of below 50aF translates into a resolution of 17.5 bits relative to the full-scale range of the modulator.

The minimum OSR required to achieve a quantization noise limited resolution at the 17.5-bit level depends on the order of the loop filter in the ΣΔ modulator. For a first-order ΣΔ modulator, a minimum OSR of 185364 is needed. This drops dramatically to about 512 for a second-order ΣΔ modulator and about 256 for a third-order ΣΔ modulator [2].

Although this trend suggests that applying a higher-order ΣΔ modulator is a good way to reduce the minimum required OSR for a CDC to achieve a certain level of resolution, practical incremental ΣΔ modulators with an order higher than three are rarely seen. One of the reasons for this is that for high-order ΣΔ modulators, not all of the signal input range can be used [2]. As the input reaches the full-scale range, the modulator may become unstable. Typically, about 75% of the full-scale input range for a second-order ΣΔ modulator is usable. For a third-order ΣΔ modulator this value reduces to 67% [3]. Moreover, the higher the loop filter order, the more difficult it is to design a stable ΣΔ modulator. The consequence is that a conservative degree of the noise-shaping will be required to guarantee better stability.

To further reduce the minimum OSR required to achieve a certain capacitance resolution, it is important to realize that the full-scale range of the modulator does not have to be as large as that of a sensor capacitance of 10pF. As briefly discussed in Chapter 2, the high-resolution requirement can be reduced if the baseline capacitance can be removed from the input of the modulator. This is shown in Fig. 4.2, where a programmable baseline-removal capacitance C_B , which can be tuned to close proximity to the value of the sensor capacitor C_S, is used to cancel the effect of the baseline capacitance of C_S. As is illustrated in the lower part of Fig. 4.2, removing the baseline part of the sensor capacitance can enable

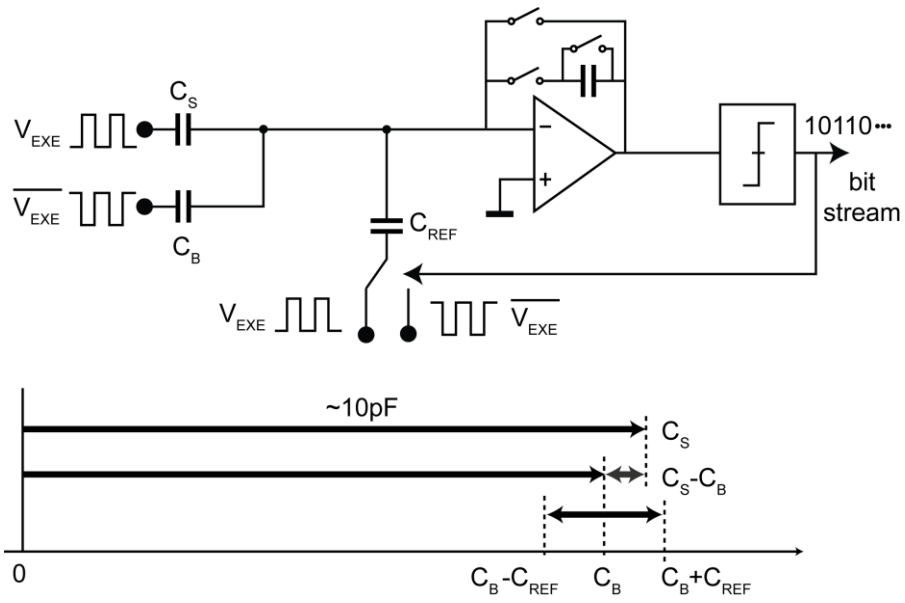

Fig. 4.2: Simplified block diagram of a CDC with baseline capacitance cancellation.

the use of a smaller reference capacitance in the charge-balancing operation. If the baseline capacitance removal can occur without any flaws, the reference capacitance size can be reduced to the sensor capacitance variation range, which is in our case only ±25fF and more than two orders of magnitude smaller than the nominal sensor capacitance of 10pF. This will considerably reduce the effort needed to resolve the changes in C_S. In this case, a capacitance resolution of below 50aF translates into a resolution of 10 bits relative to the full-scale range of the modulator, which amounts to only 50fF with the baseline part of the sensor capacitance removed. This is a very effective way of gaining capacitance resolution with limited OSR, especially when the baseline part of the sensor capacitance is large compared to its variation part.

The key benefit of baseline capacitance cancellation is that the required minimum OSR to reach the same level capacitance resolution can be reduced, leading to a reduced conversion

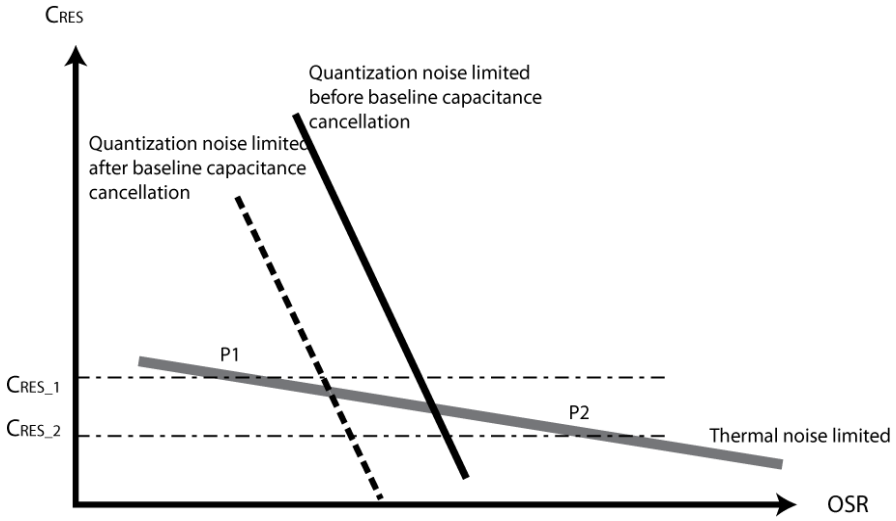

Fig. 4.3: Capacitance resolution of a CDC as a function of the OSR, due to both thermal noise and quantization noise limitations.

time for the same sampling frequency. From another perspective, the same conversion time can be achieved with a lower sampling frequency with baseline capacitance cancellation, and in turn lead to lower power consumption. However, the baseline capacitance cancellation will only reduce the quantization noise. The thermal noise is determined by the total input capacitance and circuits in Fig. 4.1 and Fig. 4.2, both of which have comparable total input capacitance values of about 20pF. It can therefore be concluded that first-order baseline capacitance cancellation will not change the minimum OSR that is required by the thermal noise.

The situation above can best be illustrated by Fig. 4.3, which shows the capacitance resolution as a function of the OSR. Both quantization noise-limited capacitance resolution and thermal noise-limited capacitance resolution become smaller as the OSR increases. However, the quantization noise limited capacitance resolution drops at a faster rate. As is shown by the dotted line, applying baseline capacitance cancellation will shift the quantization noise-limited capacitance resolution line down but will have almost no effect on the thermal noise-limited capacitance resolution.

Moreover, two situations are shown in Fig. 4.3. In situation one, the minimum required OSR, as determined by the quantization noise, is larger than the minimum OSR, as

determined by the thermal noise. In situation two it is the other way around. Since the baseline capacitance cancellation only reduces the minimum required OSR, as determined by the quantization noise, it is only effective in the first situation. From Fig. 4.3 it can also be seen that the baseline capacitance cancellation is effective for a limited range, as well. As soon as we move the dotted line beyond point P1, which stands for the minimum OSR determined by the thermal noise in the first situation, a further decrease in the modulator full-scale range will not result in power conservation, as the CDC resolution will become thermal noise-limited.

Both the order of the modulator and the degree of reduction in the full-scale range by means of applying baseline capacitance cancellation are design parameters that can be adjusted to reduce the minimum required OSR to reach the targeted capacitance resolution. Generally speaking, a high-order ΣΔ modulator needs less reduction in the full-scale range to achieve a target capacitance resolution compared to a lower-order ΣΔ modulator. Because for the same OSR a higher-order ΣΔ modulator can achieve a higher capacitance resolution compared to a lower-order ΣΔ modulator, the trade-off needed to reduce the full-scale range is smaller. This suggests that there are multiple combinations of design choices available. The disadvantage of using a high-order ΣΔ modulator is the increased design complexity and risk of running into stability problems that may potentially null the benefit of a high-order ΣΔ modulator in the form of a reduced stable input signal range [4]. The disadvantage of using a very high degree of reduction of the full-scale range of the modulator, on the other hand, is that the reduced full-scale range may become impractical in contrast to the variation range of the sensor, the adjustment resolution of the baseline cancellation capacitance, etc.

Therefore, from the thermal noise analysis, a minimum OSR of about 100 is needed to reach the target capacitance resolution. Given that the short-term variation range of the sensor is less than 50fF, if the full-scale range of the modulator after baseline capacitance cancellation is chosen to be 200fF, then reaching a capacitance resolution below 50aF translates into a resolution of 12 bits relative to the full-scale range. A full-scale range of 200fF leaves reasonable margins for non-idealities in the baseline capacitance cancellation such as finite adjustment resolution of the baseline cancelling capacitance. A system-level simulation shows that a third-order ΣΔ modulator requires a minimum OSR of about 66 to achieve 12-bit resolution, so the choice of a third-order loop filter would provide enough

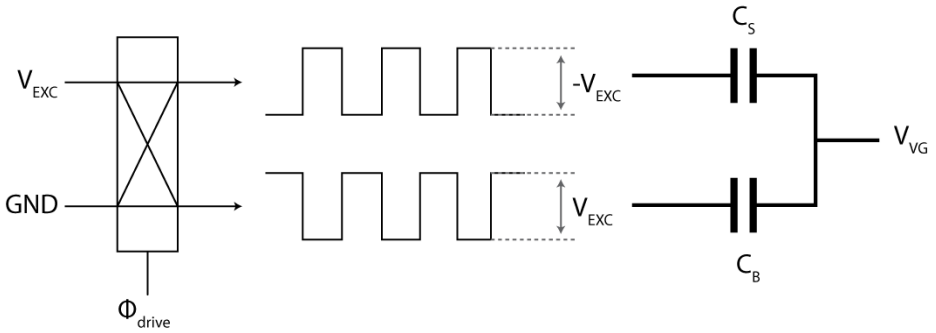

Fig. 4.4: Generation of excitation signals for baseline capacitance cancellation operation.

margin to guarantee that both quantization noise is reduced to sufficiently low levels and the CDC is thermal noise limited.

4.2.3. Charge-balancing operation

The introduction of the baseline cancellation capacitance means that in order to measure the sensor capacitance C_s, we also need to know the value of the baseline-removal capacitance C_B. In order to determine the baseline-removal capacitance C_B itself, the same charge-balancing operating principle and a large part of the hardware can be re-used.

The proposed capacitive-sensor interface circuit thus comprises two operation modes: (i) a standard fast capacitance measurement operation, with cancelled baseline capacitance; and (ii) a calibration mode, in which the baseline cancellation capacitance is measured. The detailed operations of both modes will be discussed next.

Baseline capacitance cancellation requires the application of a pair of opposite excitation voltages to the two capacitors connected, as shown in Fig. 4.4. The opposite excitation signals needed to drive the two capacitors are generated by applying a clock signal to a chopper, the inputs of which are connected to two different DC voltage levels. In this case

these two voltages are V_{EXC} and GND, respectively. Since the voltage difference is fixed, it can be guaranteed that the two excitation voltages generated at the output of the chopper will always have equal value with the opposite sign. The system works according to ratiometric principles, so that the exact value of V_{EXC} will not affect the measurement results. The system should, however, be stable enough for one conversion. However, since the conversion time is short, the stability of the excitation voltage source is relatively easy to achieve.

The total charge transferred in each clock cycle through the virtual ground node to the integration capacitor can be written as:

$$Q = V_{EXC} \cdot (C_S - C_B) + (V_{VG}(t2) - V_{VG}(t2)) \cdot (C_S + C_B) \qquad (4.1)$$

where V_{VG} stands for the virtual ground voltage of the amplifier.

From Eq. 4.1, it can be seen that having two opposite but equal voltage steps at the left side of the two capacitors is not enough to guarantee that the transferred charge is proportional to the capacitance difference. The voltage of the common-electrode at times $t1$ and $t2$ needs to be the same as well. This requirement can be achieved by connecting the common electrode node of the two capacitors to a virtual ground voltage created by the OTA.

In the simplified circuit diagram of the capacitive sensor interface circuit shown in Fig. 4.5 (ignore the C_{REF} branch for the moment) as Φ_{drive} toggles, the charge package

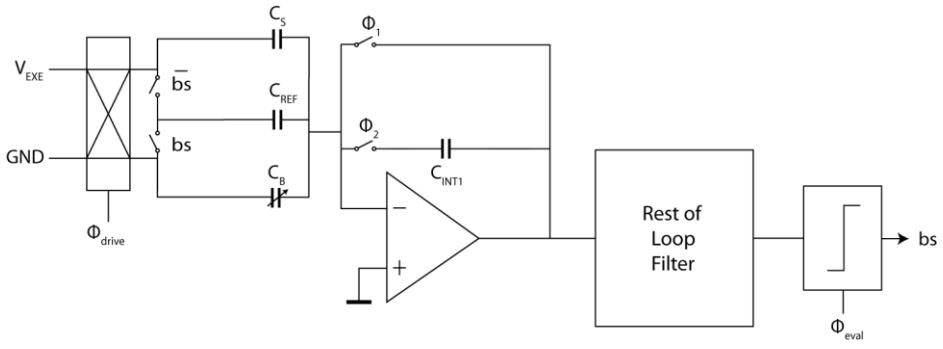

Fig. 4.5: Simplified circuit diagram of a CDC.

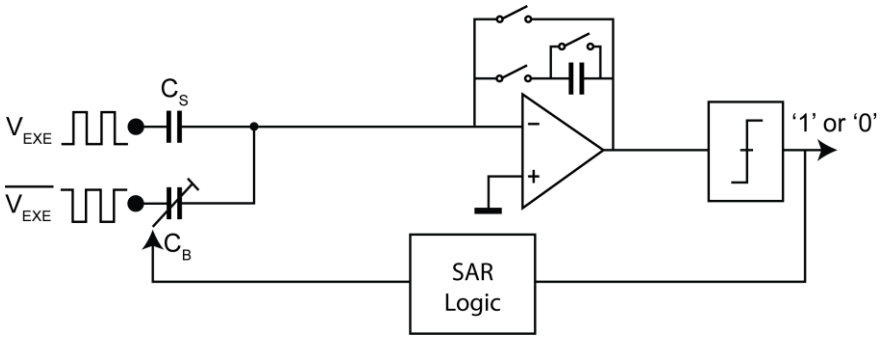

Fig. 4.6: Proposed CDC during CapDAC initialization.

proportional to C_S and C_B, but opposite in polarity, will be transferred into the integrating capacitor C_{INT1}. The net effect is that only the difference between C_S and C_B is seen by the interface circuit. Thus the baseline part of the sensor capacitor C_S is removed if C_B is tuned to be approximately equal to the baseline part of C_S.

To achieve this, C_B is realized as an adjustable capacitance bank, thus C_B functions as an offset-cancelling capacitive DAC (CapDAC). In order for C_B to effectively cancel the baseline part of C_S, an initialization phase where the appropriate value of C_B is found by means of a series of comparisons with C_S, should be performed. In this step, the reference capacitor is disconnected from the excitation voltages and connected to a fixed potential. The loop filter is configured as the preamp of the comparator and is reset after each comparison, as shown in Fig 4.6.

The output of the comparator provides information about the relative capacitance relationship between C_S and C_B. Based on the results, the value of C_B can be adjusted so that it approximates C_S. This searching process can for instance be controlled by a successive approximation algorithm. In view of the specification of the sensor capacitor value, C_B has been chosen to be able to vary between 8.4pF and 11.6pF in steps of 50fF nominally. The range is in line with the expected short-term capacitive variation range (±25fF), the long-term drift range (~ ±1pF), and the baseline capacitance (10pF) of the sensor capacitance C_S, with some margin. The input range of the circuit in this mode then

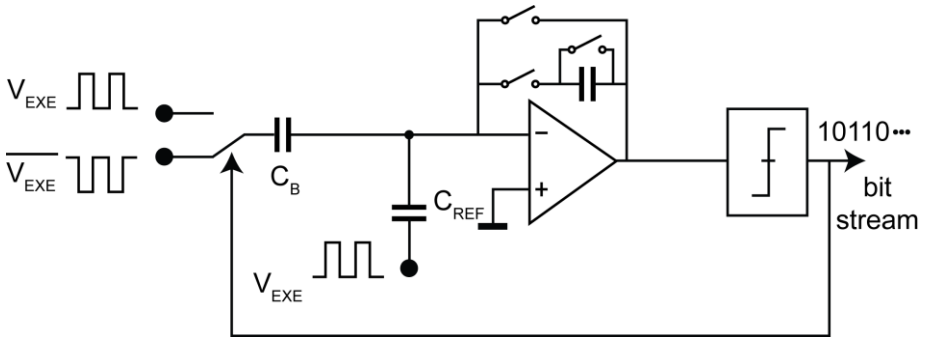

Fig. 4.7: Proposed CDC during CapDAC calibration.

spans from 8.4pF to 11.6pF, or an input capacitance range of 2.2pF. Although this choice stems from a system specification, C_B can in principle cover a full range from 0pF to 11.6pF.

After the correct C_B has been found, the relationship between C_B and the reference capacitor in the standard conversion phase C_{REF} is determined during a second CapDAC calibration step, as shown in Fig 4.7. During this step the sensor capacitance is disconnected from the input of the modulator. With some logic function modifications, C_B acts as the reference capacitor in the ΣΔ modulator in this CapDAC calibration phase to determine the ratio C_{REF}/C_B. This logic function inversion is necessary because in a ΣΔ converter, the input capacitance generally needs to be smaller than the reference capacitor. In practice this is realized by modifying the digital logic of the chopper CH_1 which is used to generate excitation signals for the CDC. Instead of driving the input chopper with Φ_{drive}, which is a square-wave signal as is shown in Fig. 4.5, in the CapDAC calibration mode this chopper is driven by the exclusive nor of bs and Φ_{drive}. This realization ensures that no extra switches are required to achieve the logic function inversion.

The aforementioned two steps, which are only occasionally necessary, are performed during the system calibration phases, the timing relation of which is illustrated in Fig 4.8. From time to time the system can be calibrated. For this reason, the initialization and calibration of C_B are not time-critical. Using a longer measurement time allows the resolution to improve by reducing the noise bandwidth, and eventually can help to reduce

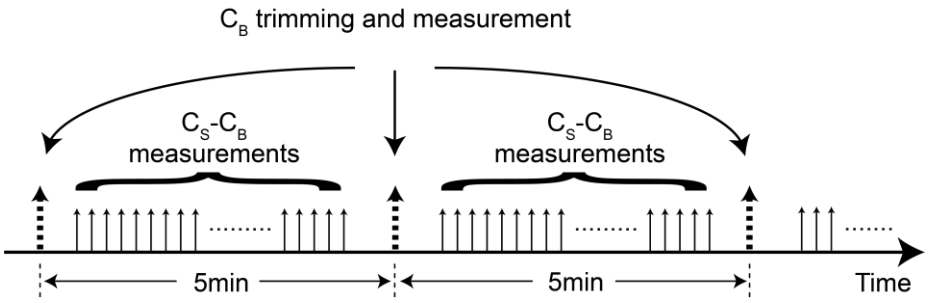

Fig. 4.8: Timing relation for various measurement modes of the proposed CDC.

the uncertainty of the calibration. The achievable accuracy of the calibration can thus be relatively high so that the error induced by calibration can be made negligible.

During standard operation, the nominal reference capacitor C_{REF} of 100fF is either connected to the excitation signal or the anti-phase excitation signal, depending on the bitstream bs of the modulator. This is shown in Fig. 4.9. The ratio between the small capacitance difference $C_S - C_B$ and C_{REF} is continuously determined by the ΣΔ modulator. The effective input range of the modulator during standard operation is thus ± 100fF, or 200fF. The conversion result is then combined with the CapDAC calibration result to obtain the desired low-latency ratio:

$$\mu = \frac{C_S}{C_B} = \frac{\frac{C_S - C_B}{C_{REF}}}{\frac{C_B}{C_{REF}}} + 1 \tag{4.2}$$

If the capacitance of $C_B$can be considered to be a constant value between calibrations, the measurement latency is in principle only determined by the measurement latency in the standard operation mode. Since the full-scale range in the standard operation mode is only ±100fF, it takes much less time to reach to the required capacitance resolution. If the time interval between calibrations is small enough, with a well-controlled operating environment, the assumption that C_B can be considered to be a constant value is valid.

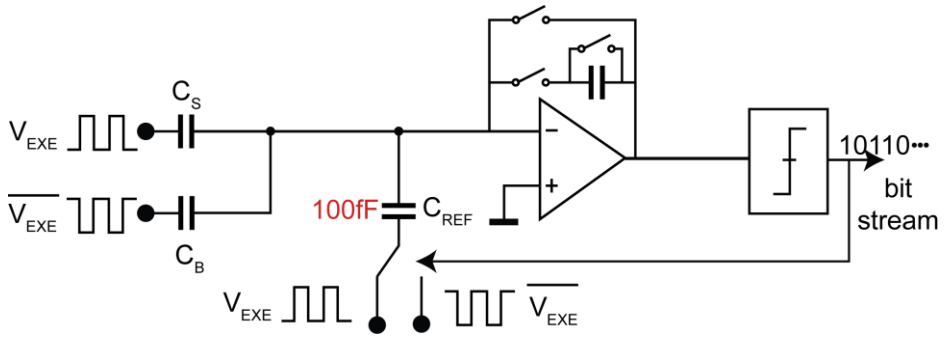

Fig. 4.9: Proposed CDC during standard operation.

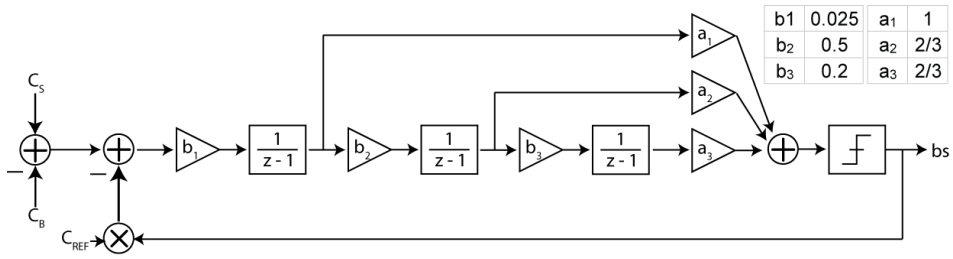

Fig. 4.10: Proposed CDC loop filter topology.

The full-scale input range in the standard operation mode chosen is four times that of the nominal step size of C_B. This ensures that not only a suitable measurement range is available even in the presence of an integral non-linearity (INL) error in the C_B, but that sufficient overlap between adjecent ranges is also available so that the difference between C_S and C_B can always be accurately digitized.

Figure 4.10 shows a loop filter topology of the proposed CDC. This design uses a third-order feedforward loop filter, since it provides improved modulator linearity [5,6]. Compared to the implementations proposed in [6], a direct feedforward path from the input to the quantizer is omitted, as the input of the CDC is still in the capacitive domain where such a direct feedforward path would not be practical to make. On the other hand, omiting this path does not significantly degrade the performance of the CDC either, especially when a single-bit quantizer is used, as is the case in this design.

There is, on top of all these, an additional advantage of using a feedforward structure without direct feedforward path. With this topology the same loop filter can be used in both the normal and the CapDAC calibration steps simply by adjusting the integration capacitors of the first integrator stage. The gain of the first integrator stage needs to be adjusted because of the large difference in the capacitance of C_{REF} and C_B, which act as reference capacitors in normal and CapDAC calibrations respectively. In this particular topology adjusting the gain of the first integrator affects all signal paths, and thus will not affect the loop stability. The modulator coefficient chosen leads to decent third-order noise-shaping in combination with a stable input range of about ±0.65 C_{REF}.

4.3. Circuit-level techniques

4.3.1. Overview

Following the system-level discussions in the previous section, the path has been laid to move to circuit-level details of the proposed approach. This is dealt with in this section of the thesis.

4.3.2. Third-order incremental ΣΔ capacitance-to-digital modulator

The circuit diagram of the proposed third-order incremental ΣΔ capacitance-to-digital modulator is shown in Fig. 4.11. Although the sensor is single-ended, a fully differential circuit is used to increase the robustness of the interface to charge-injection errors [1]. To this end, a replica capacitive input network, shown in grey in Fig. 4.11, is also implemented on-chip. This branch does not receive excitation signals and is only meant for cancellation of the charge-injection error.

In standard operation mode, for maximum resolution and maximum operation speed, C_S and C_B are driven by square waves with the same amplitude as the supply voltage, i.e. 3.3V. Since C_S and C_B are driven in the anti-phase, the first integrator does not slew because the signal capacitance $C_S - C_B \pm C_{REF}$, which is limited to below ±150 fF by design, is quite small compared to the total input capacitance $C_S + C_B + C_P + C_{REF}$, which amounts to

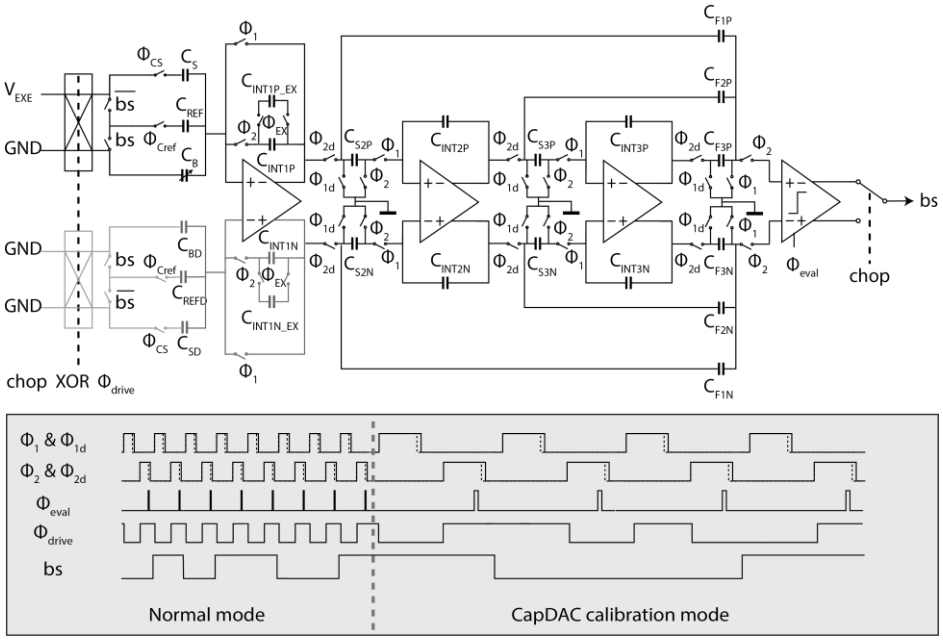

Fig. 4.11: Circuit diagram of the capacitive-sensor interface.

larger than 30 pF. As a consequence, the resulting voltage step at the OTA input terminals is quite small. Due to the absence of slewing, the clock frequency in standard operation mode can be determined by small-signal characteristics and thus is set to 5MHz. During CapDAC calibration, where the effective input capacitance $C_{REF} \pm C_B$ is relatively large compared to the total input capacitance, the system clock frequency thus needs to be reduced correspondingly to 1.25MHz to give the OTA more time to settle and hence prevent slewing-related errors.

During CapDAC calibration, the main requirement is precision and stability rather than speed and resolution. However, the modulator's precision and stability are limited by its offset and 1/f noise, respectively. To mitigate their effects, the first integrator employs correlated double-sampling (CDS). On top of this, the entire modulator is chopped at a much lower frequency to cancel out the residual error [3], as shown in Fig. 4.11. Chopping is digitally implemented first by swapping the polarity of the excitation voltages and the bitstream bs appropriately, and then by averaging the decimated conversion results obtained in each chopper state. In this way, no extra state-preserving chopper switches are required to chop the integration capacitors as in [3], thus reducing the layout complexity [4]. This step also eliminates the potential source of charge-injection errors which would

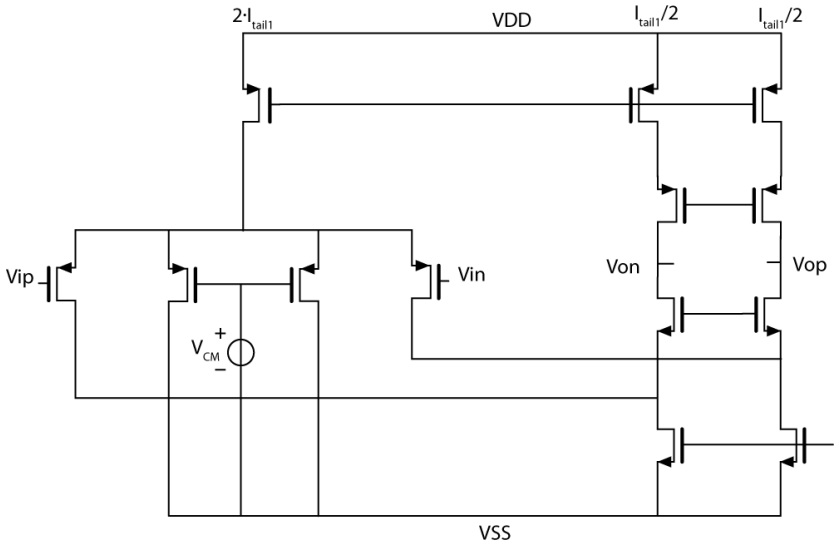

Fig. 4.12: Schematic of the first integrator OTA with input common-mode feedback.

otherwise result from the chopper switches. Compared to the analog implementation of system-level chopping in [3], here the effective number of clock cycles in each of the two sub-conversions is halved, and hence the quantization noise level will be higher. However, since the quantization noise has already been reduced to sufficiently low levels in the CapDAC calibration phase, there will be no visible penalty associated with this digital system-level chopping implementation.

4.3.3. Input stage design considerations

In this section the focus of discussion will turn to the design of the input stage, which directly interfaces the sensor capacitance C_S. This requires special attention because this stage is more critical in terms of noise and precision. As is discussed in the previous section, although the interface is designed for a single-ended sensor, a differential circuit is used to increase the robustness of the interface to charge-injection errors. For this purpose, the first

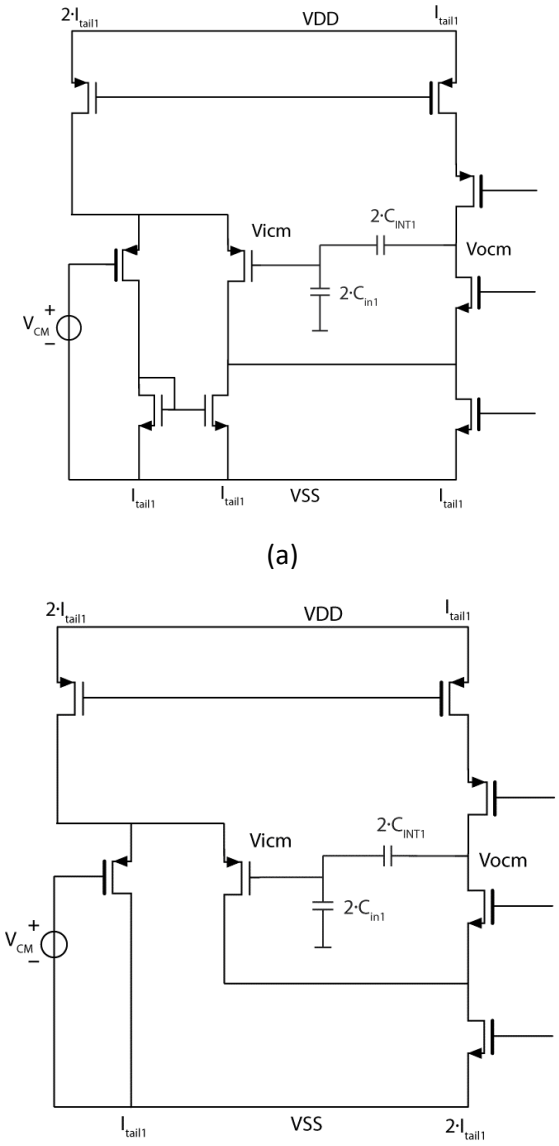

Fig. 4.13: (a) Input common-mode regulation; (b) input common-mode regulation with bandwidth doubler.

OTA employs a common-mode feedback (CMFB) loop stabilizing the common-mode voltage at the input, rather than the conventional way of realizing CMFB stabilizing the common-mode voltage at the output of an OTA.

The circuit diagram of the first OTA is shown in Fig. 4.12. From the schematic it can be seen that the input CMFB is realized by adding two extra transistors to the input differential pair of the OTA [7]. The common-mode feedback function only works when global feedback is available, as shown in Fig. 4.13, where transistors and capacitors in the differential paths have been merged to show only the common-mode signal path. In Fig.

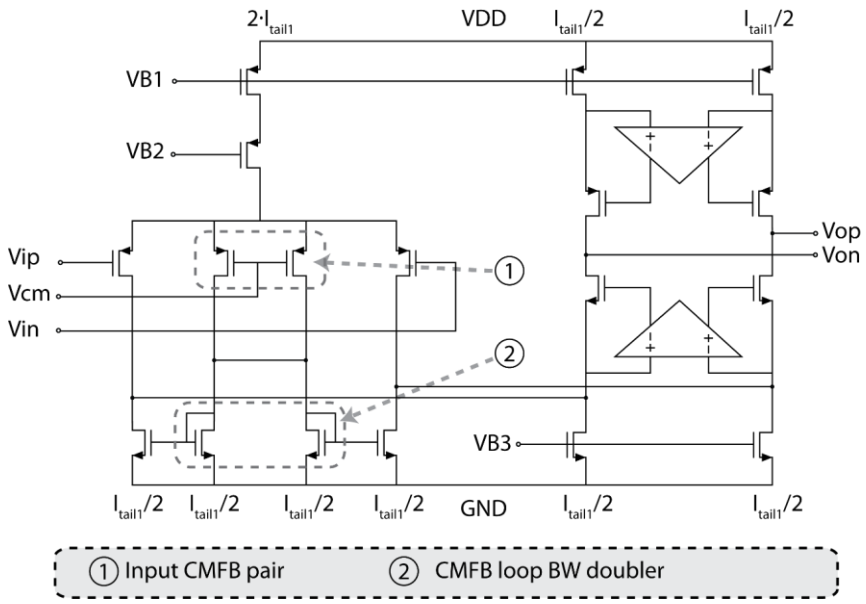

Fig. 4.14: Schematic of the first integrator OTA in more detail.

4.13 (a), the current of the common-mode feedback transistor has been dumped to ground. This in principle does not affect the functionality of the common-mode feedback, however, this would cause the bandwidth of the CMFB path to be only half of that of the differential signal path. In order to solve this, a current mirror is added to reclaim the signal current, as shown in Fig. 4.13 (b) [8].

The common-mode feedback input transistors added to the amplifier will, however, contribute additional noise. This can be solved by connecting the two added transistors together, as shown in Fig. 4.14. Consequently, the noise contribution of these transistors will only be visible in the common-mode path and hence will not affect the differential signal path. In reality, due to mismatches in the differential signal path resulting in limited common-mode rejection ratio (CMRR), part of the common-mode noise does leak to differential signal path. However, since thermal noise adds up in terms of noise power, even with 10% mismatch, the noise penalty will only be roughly 1% and can be ignored in practice.

The first OTA also incorporates gain-boosting techniques [9], where the loop gain is designed to be above 110dB in CapDAC calibration mode and above 90dB in standard

operation mode. The input common-mode feedback ensures that the interface of the modulator acts as a good virtual ground for both the differential and common-mode signals. In CapDAC calibration mode, simulations show that the modulator can achieve 18-bit precision even in the presence of 10% switch mismatch and up to 4pF (parasitic) capacitance mismatch between the differential inputs.

The following two integrator stages in the loop filter use simple folded-cascode OTAs with an output CMFB loop, as the errors are strongly suppressed by the gain of the first integrator functioning above 110dB at low frequency.

4.4. Realizations and measurement results

4.4.1. Layout

The designed capacitance-to-digital converter is fabricated in a standard 2P4M 0.35µm CMOS process. A chip photo of the realized design is shown in Fig. 4.15. The design occupies an active area of 2.6 mm^2. It draws 4.5 mA from a 3.3 V supply, of which over 3.1 mA is consumed by the first OTA to drive large input capacitances. The CapDAC and all other on-chip capacitors are realized with poly-poly capacitors, which is the best

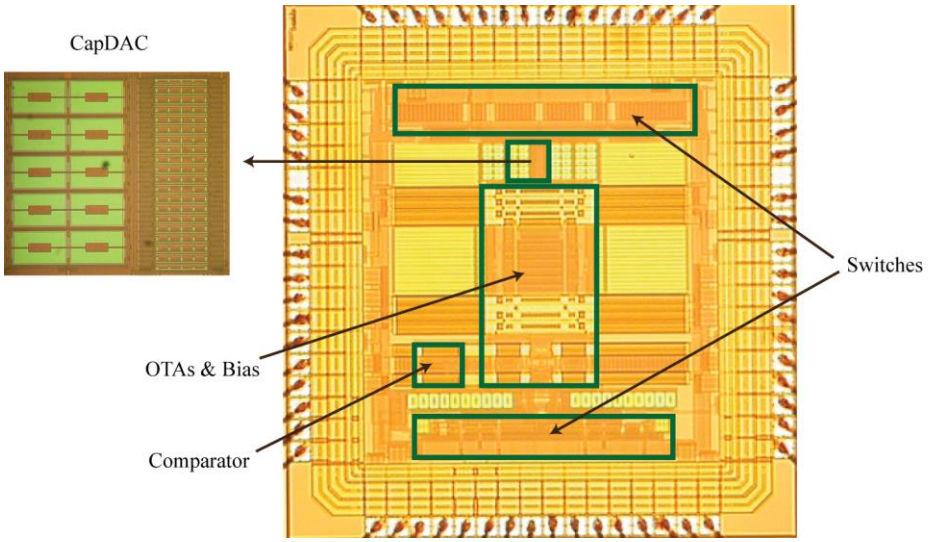

Fig. 4.15: Chip photo of the realized CDC.

available type of capacitor for this process in terms of linearity and stability. For flexibility, the control logic and decimation filter are implemented off-chip.

4.4.2. Measurement results

Measurements were conducted to characterize the performance of the CDC in various operation modes. In CapDAC calibration mode, the main requirement is accuracy and stability. To test the stability of the CDC in CapDAC calibration mode, the ratio of C_{REF} and C_B were continuously measured for up to six hours. During this period, because both C_{REF} and C_B are made of the same type of capacitance and are physically close together, the effect of drift in temperature would not show up in this measurement. Therefore, no special temperature control was applied. The measured decimated result is shown in Fig. 4.16, from which it can be observed that the measurement result without chopping applied contains offset in the order of about 1 LSB of 13 bits, which with chopping drops below 1 LSB of 20 bit. In the intended application the thermal drift of C_{REF} and C_B is negligible, since both the sensor and the CDC are designed to operate in a temperature-controlled environment with less than 10mK variations. Due to the nature of radiometric measurements, drift in the excitation voltages also does not contribute to the error. Together with the good stability of the CDC itself, the stability of the absolute capacitance measurement system between calibration intervals can be achieved.

As it is difficult to construct a CapDAC with very good linearity, the linearity of the CDC could not be directly evaluated. There is, however, a method with which the integral non-linearity of the CDC can be measured. If two input capacitances C_1 and C_2 are available, two measurements can be conducted with the CDC to obtain the following two ratios:

$$\mu_1 = \frac{C_1}{C_{REF}} \tag{4.3}$$

$$\mu_2 = \frac{C_2}{C_{REF}} \tag{4.4}$$

Furthermore, the parallel combination of the two capacitances can also be measured by the CDC the ratio of which will be:

$$\mu_3 = \frac{C_1 + C_2}{C_{REF}} \tag{4.5}$$

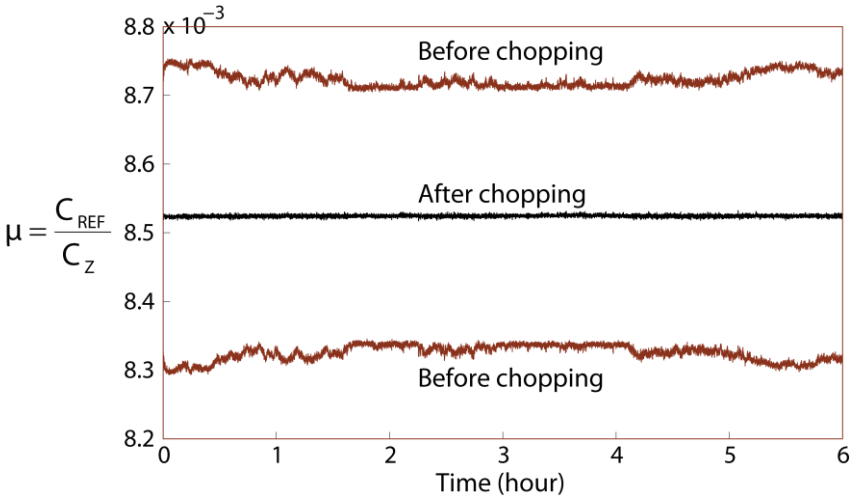

Fig. 4.16: Stability measurement results, with and without system-level chopping turned on.

If the CDC is perfectly linear, we should have $\mu_3 = \mu_1 + \mu_2$, and the difference between μ_3 and $\mu_1 + \mu_2$ will be a good indicator of the linearity of the CDC. Using this method, a perfectly linear CapDAC functioning as the input capacitor is no longer required.

There is, however, a small issue with the above-discussed measurement method: the offset of the CDC will affect the accuracy of the linearity measurement. This is because $\mu_1 + \mu_2$ contains twice the amount of measurement offset while μ_3 contains only one, causing the offset to affect the measurement result. Although the offset level is low for the CDC, we would still like to exclude its influence in the linearity measurement. Fortunately, this can be easily achieved with a small modification. With three different input capacitances C_1, C_2 and C_3, the following four measurements can be conducted:

$$\mu_1 = \frac{C_1}{C_{REF}} \tag{4.6}$$

$$\mu_2 = \frac{C_1 + C_2}{C_{REF}} \tag{4.7}$$

$$\mu_3 = \frac{C_1 + C_3}{C_{REF}} \tag{4.8}$$

$$\mu_4 = \frac{C_1 + C_2 + C_3}{C_{REF}} \tag{4.9}$$

If the CDC is perfectly linear, we should have $\mu_2 + \mu_3 = \mu_1 + \mu_4$. Since both sides of the equation contain twice the amount of offset of the CDC, the difference will not be affected by the offset and therefore will be a better indicator of the linearity of the CDC.

In the design, the C_{REF} actually consists of three capacitors: a CapDAC with C_{REF0}=100fF, C_{REF1}=100fF and C_{REF2}=200fF. These enlarge the input range of the standard operation phase if necessary. They can be utilized as discussed above to assess the CDC linearity. For each C_B setting, four measurements can be carried out with the following four different capacitance combinations as input:

$$\mu_1 = \frac{C_{REF0}}{C_Z} \tag{4.10}$$

$$\mu_2 = \frac{C_{REF0} + C_{REF1}}{C_Z} \tag{4.11}$$

$$\mu_3 = \frac{C_{REF0} + C_{REF2}}{C_Z} \tag{4.12}$$

$$\mu_4 = \frac{C_{REF0} + C_{REF1} + C_{REF2}}{C_Z} \tag{4.13}$$

As discussed before, $(\mu_2 + \mu_3) - (\mu_1 + \mu_4)$ will reflect the non-linearity of the CDC. Since this approach only gives a local estimate of non-linearity, measurements were conducted at each of the 64 available settings of the C_B, covering the range from 8.5 to 11.5pF. The result of this measurement is shown in Fig. 4.17, which shows that the non-linearity level of the CDC is below 1 ppm, which is commensurate with 20-bit performance.

In normal operation mode, the main requirements are speed and resolution rather than accuracy and stability. Figure 4.18 shows the 65,536-point power spectrum of the bitstream in normal operation mode with a 5MHz clock. The bitstream is obtained with DC input, and the DC term is removed digitally here by subtracting the bitstream with the bitstream average. Here 3rd order noise shaping ensures that the modulator is thermal noise limited

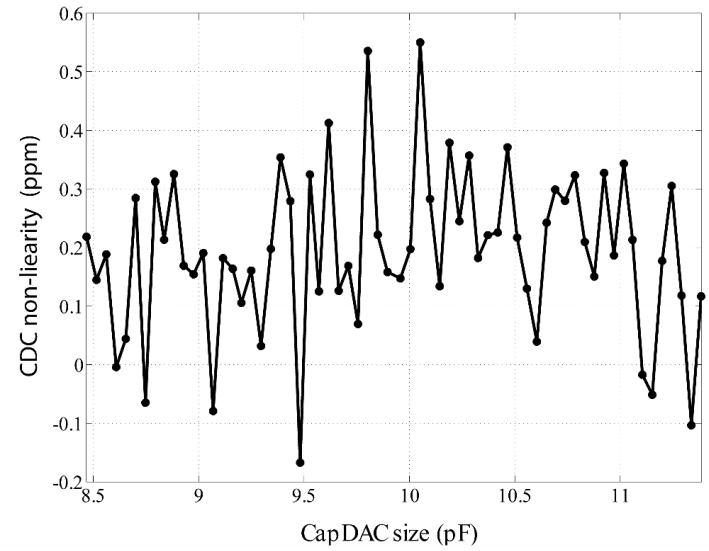

Fig. 4.17: Linearity measurement of the CDC.

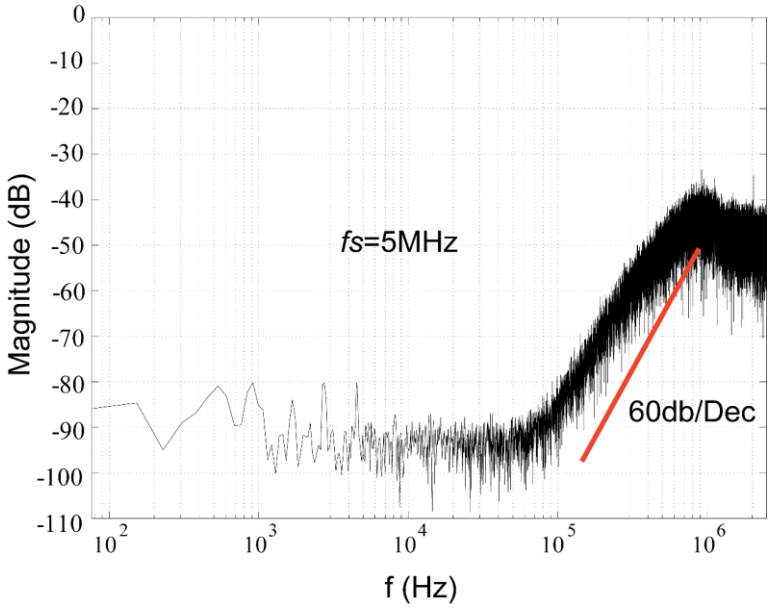

Fig. 4.18: Bitstream FFT of the CDC.

up to about 50kHz. The full scale corresponds to 200fF, while integrated noise within 50 kHz sum up to 60aFrms.

The performance of the CDC was further verified with an off-chip capacitive sensor using the test setup shown in Fig. 4.19. It consisted of a fixed electrode in close proximity to an electrode attached to a mechanical shaker. By driving the shaker with a function generator, small capacitance changes could be triggered. The CDC was connected to the electrodes via two short shielded cables, each of which contributed extra parasitic capacitance (roughly 10pF) to ground. The actual value of C_{REF} was found to be 91.8fF by calibrating it to an external 10.3pF SMD capacitor the value of which had been measured by a

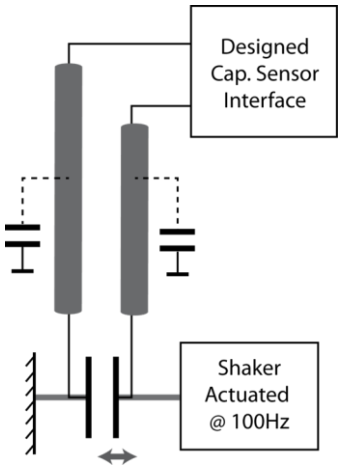

Fig. 4.19: Measurement setup to evaluate resolution of the CDC with an off-chip capacitive sensor.

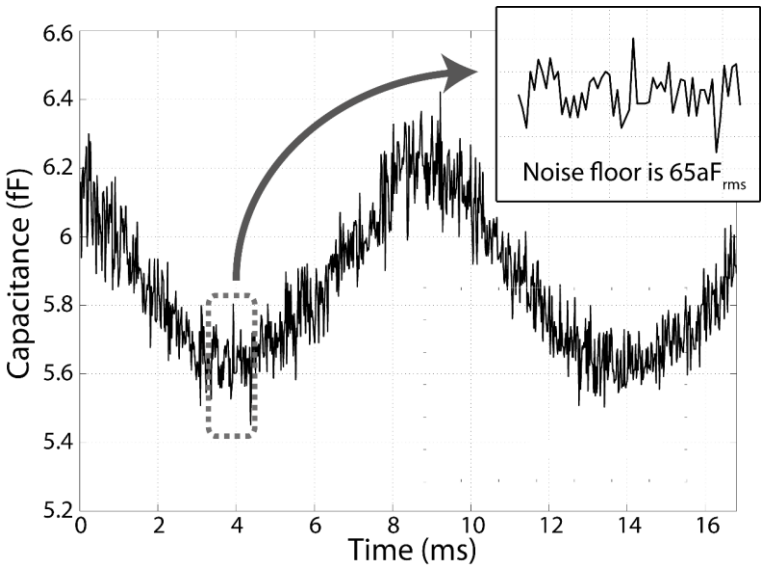

Fig. 4.20: Measured resolution of the CDC with an off-chip capacitive sensor.

HP4192A LF impedance analyser (±100fF inaccuracy). The small capacitance changes triggered by driving the shaker with a 100Hz square-wave are shown in Fig. 4.20. The capacitance change corresponds to 600aFpp while the resolution of the measurements corresponds to 65aFrms. When translating back to displacement resolution for the target capacitive sensor with d_0 of 10µm and a nominal capacitance of 10pF, the achievable displacement resolution is 65pmrms.

4.5. Conclusions

In this chapter, a capacitive sensor interface circuit based on the charge-balancing principle is described as an illustration of the proposed CDC design approach. In standard operation mode, it employs baseline capacitance cancellation to achieve an effective capacitance resolution of 65aFrms within 20μs. This is achieved with a power consumption of 15mW. Using the same charge-balancing principle, the relationship between the baseline capacitance and the reference capacitance can be determined using the same hardware with high accuracy, which can be done in the calibration steps. Greater than 17-bit precision has been demonstrated with excellent linearity.

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Chapter 5

Capacitive Sensor Interface Using Capacitance-to-Voltage Conversion

This chapter presents capacitive interface circuit based on a two-stage capacitance-to-voltage converter (CVC), where correlated double sampling scheme has been utilized to cancel sampling noise of the sensor capacitor. The result is a low-noise high-speed capacitive sensor front-end circuit.

5.1. Introduction

The variation of the capacitance in a capacitive sensor can be first turned into voltage change which can later be digitized. For instance, this voltage can directly be digitized with a conventional analog-to-digital converter (ADC). Figure 5.1 illustrates a block diagram of such a system in its simplest form, which is composed of a capacitance-to-voltage converter (CVC) and a conventional voltage-input ADC.

The output of a CVC is a function of the excitation voltage and the sensor capacitance. When the same excitation voltage is used as the reference voltage of the ADC, the entire capacitive sensor interface can be made insensitive to the exact value of the excitation voltage. This proves advantageous because the stability requirement on the excitation voltage becomes much less critical.

The CVC can be considered as a signal-conditioning circuit for the following ADC. The main function of a CVC is to transform the capacitance variation into a suitable voltage variation that can be handled by the ADC. This requirement, however, places some constraints on the CVC, including the output voltage range, output voltage resolution, driving capability, etc. The CVC thus plays an important role in a capacitive interface

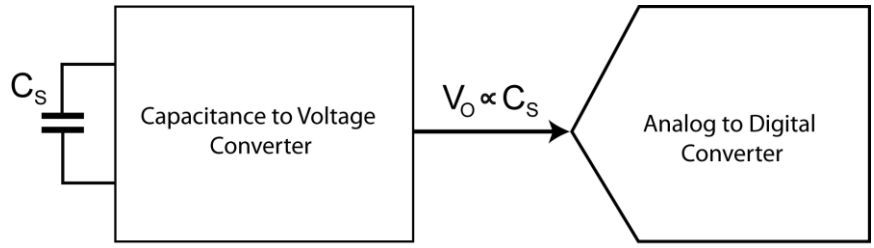

Fig. 5.1: Simplified block diagram of a capacitive sensor interface circuit comprising a capacitance-to-voltage converter followed by a standard analog-to-digital converter.

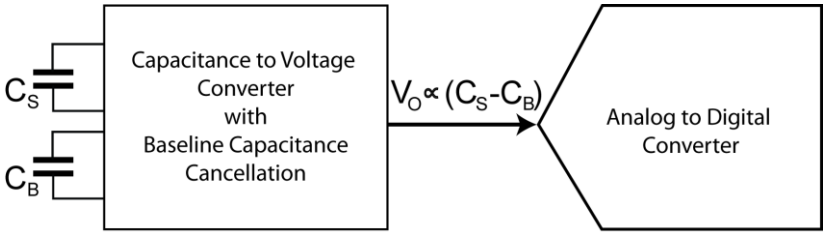

Fig. 5.2: Simplified block diagram of a capacitive sensor interface circuit comprising a capacitance-to-voltage converter with baseline capacitance cancellation followed by a standard analog-to-digital converter.

circuit. Given the large baseline capacitance size of the sensor, if the output range of the CVC is mapped to the total sensor capacitance of 10 pF, then the majority of the dynamic range at the output of the CVC will be wasted on the baseline capacitance.

By applying the baseline capacitance cancellation technique as discussed in Chapter 2, this problem can be mitigated. This is illustrated in Fig. 5.2. A baseline cancelling capacitance C_B is used to remove the baseline component of the sensor capacitance. With an appropriate signal gain, the output range of the CVC can be mapped to a limited capacitance variation range around the sensor baseline capacitance. With properly selected parameters, the dynamic range at the output of the CVC can be utilized in an optimum manner, such that the ADC which follows the CVC can have a relaxed specification.

In the following sections, the design of a CVC that fulfils the above-mentioned specifications will be discussed.

5.2. Operating principle

5.2.1. Overview

This section describes a capacitive sensor interface circuit based on the capacitance-to-voltage converter principle discussed in Chapter 2. The output of the interface is a voltage signal which needs to be further digitized with an analog-to-digital converter (ADC).

5.2.2. Capacitance-to-voltage converter

A CVC can be realized with a switched-capacitor amplifier, as is illustrated in Fig. . The circuit operates on a two-phase non-overlapping clock. During φ1, the sensor capacitor is connected between the ground and virtual ground created by the OTA, while the OTA is configured in unity feedback. During φ2, the sensor capacitor is connected to the excitation voltage V_{exc}. The voltage jump over the sensor capacitor will result in a voltage jump at the output of the OTA:

$$\Delta V_o = - V_{exc} \cdot \frac{C_S}{C_F} \tag{5.1}$$

The output voltage change will then be a measure of the sensor capacitance value, and as stated in the previous section, this voltage can be further digitized with a conventional voltage input ADC.

5.2.3. Baseline capacitance cancellation

The effect of the static component of sensor capacitance consumes the dynamic range of the CVC. This can be solved with the baseline capacitance cancellation technique discussed in Chapter 2. As illustrated in Fig. , the effect of the baseline capacitance of the sensor is cancelled by adding a baseline-cancellation capacitance C_B . Effective capacitance subtraction can be realized by inverting the excitation voltages on the baseline-cancellation capacitance C_B with respect to the sensor capacitance C_S. This way, the output voltage variation in the charge amplifier is:

$$\Delta V_o = - V_{exc} \cdot \frac{C_S - C_B}{C_F} \tag{5.2}$$

Removing the effect of the baseline capacitance of the sensor enables the use of a smaller feedback capacitance C_F to increase the gain of the frontend charge amplifier, thus increasing the signal level and relaxing the dynamic range requirement of the following stages [1].

Given the fact that the nominal sensor capacitance value is 10 pF, and that the specified sensor capacitance variation is less than ±25 fF, to fully utilize the output range, a very small feedback capacitor value should be chosen, in the order of 100 fF. This can however present high specifications for the amplifier, as the feedback factor to realize this gain, given by:

$$\beta = \frac{C_F}{C_S + C_B + C_P} \tag{5.3}$$

is as small as 1/300. Here the baseline cancelling capacitance and the parasitic capacitances of about 10 pF are both taken into account. As discussed in Chapter 2, this will result in a high requirement on both the DC gain and the bandwidth of the amplifier, making the specification difficult to achieve in practice. On top of this, the amplifier also needs to provide this DC gain level over a large output voltage swing, which again requires design trade-offs. A more practical alternative would be to distribute the total gain over a number of cascaded switched-capacitor gain stages. This proposal will be discussed in the next section.

5.2.4. Practical realization of the capacitance-to-voltage converter with baseline capacitance cancellation

A simplified circuit diagram of the proposed interface circuit is shown in Fig. 5.3. As can be seen, two amplification stages are used to realize the total required closed-loop gain of the zoom-in interface. The total closed-loop gain is then devided between two amplification stages. Correlated double sampling (CDS) [2] is implemented in the second amplification stage to cancel the offset of both stages [3].

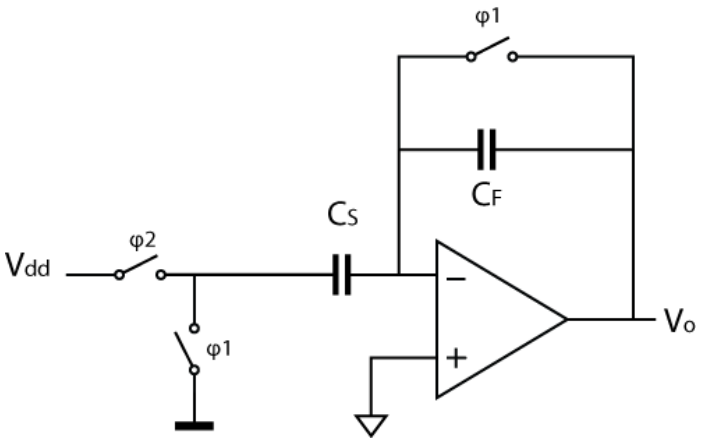

Fig. 5.3: Simplified circuit diagram of a capacitance-to-voltage converter.

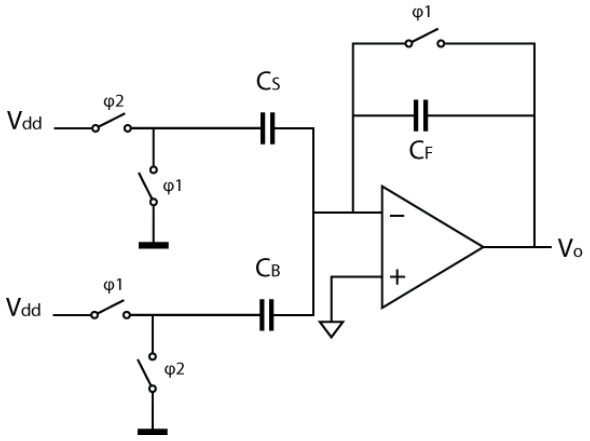

Fig. 5.4: Simplified circuit diagram of a capacitance-to-voltage converter with the zoom-in technique.

Before each conversion, the interface is reset by closing all switches controlled by P_{rst} and P_{oc}. Both amplifying stages are set in unity-gain feedback mode for reset. When the conversion starts, P_{rst} opens first, and the interface enters the offset-cancellation phase, when both the offsets of stage 1 and stage 2 will be cancelled by the CDS. The first amplifying stage utilizes offset cancellation at the output while the second amplifying stage utilizes offset cancellation at the input [3]. The amplified version of V_{os1}, which is the offset voltage of the first stage, will appear across capacitor C_H. This error will then be sampled on C_H when P_{oc} opens, no longer appearing at the output of the interface circuit. Similarly, the offset V_{os2} of the second stage is cancelled as described in [3]. The final output voltage at the output of the interface can be written as:

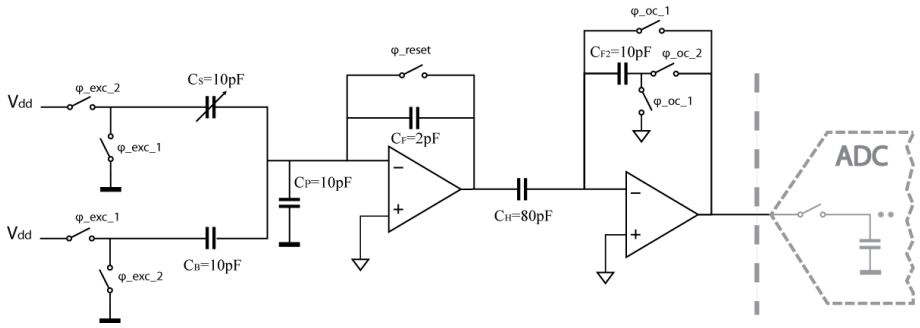

Fig. 5.5: Simplified circuit diagram of a capacitance-to-voltage converter with baseline capacitance cancellation. Here a two-stage implementation is shown.

$$V_o = -V_{exc} \cdot \frac{C_S - C_B}{C_F} \cdot \frac{C_H}{C_{F2}} \tag{5.4}$$

The value chosen for C_H limits the noise bandwidth of the first amplifying stage. From the derivation in Chapter 2, the total noise power at the output of amplifying stage 1 can be written as:

$$\overline{v_{noT}^2} = \frac{\gamma N_f kT}{\beta \cdot (C_H + \beta C_{IN})} \tag{5.5}$$

where γ denotes the noise factor of the MOS transistor, N_f denotes the noise factor which is determined by the structure and implementation of the OTA, k denotes the Boltzmann constant, T denotes the absolute temperature in kelvin, and $C_{IN} = C_S + C_B + C_P$ denotes the total input capacitance. The term βC_{IN} is the effective load capacitance of the capacitive feedback network comprising the series connection between C_F and C_{IN}. It can be seen that when C_H is much larger compared to the effective capacitance of the feedback network, the equation above can be simplified to:

$$\overline{v_{noT}^2} \approx \frac{\gamma N_f kT}{\beta \cdot C_H} \tag{5.6}$$

This shows that the noise is limited by the capacitance C_H, when C_H is much larger than the effective load capacitance from the feedback network. The noise contribution of the second stage will be suppressed by the closed-loop gain of the first stage. The noise of the interface can then be set by selecting a proper value for the capacitance C_H.

The proposed interface can handle capacitive loads and can therefore directly drive the input sampling capacitor of a capacitive-input ADC. Because the dynamic range requirement at the output of the interface is in the order of 10 bits, a fast and power-efficient

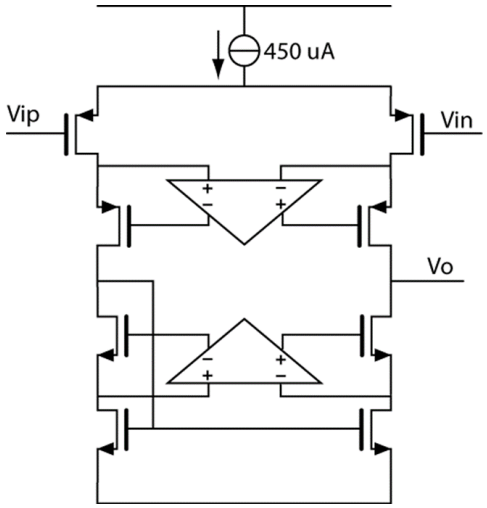

Fig. 5.6: Simplified circuit diagram of a telescopic OTA for the first amplifying stage.

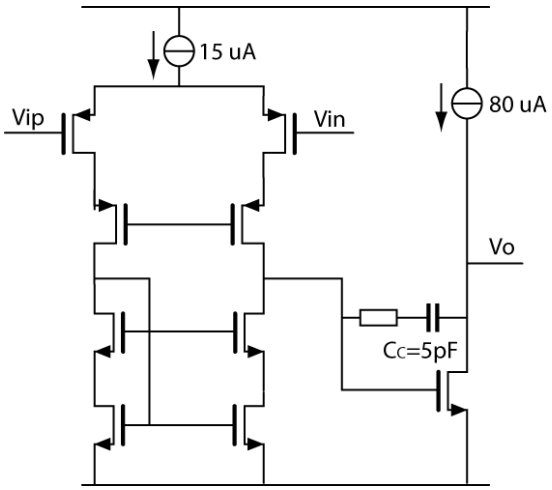

Fig. 5.7: Simplified circuit diagram of a two-stage OTA for the second amplifying stage.

Nyquist-rate ADC, such as a successive-approximation-register (SAR) ADC could be used. The time delay of the ADC will add to the time delay of the whole interface.

5.3. Circuit implementation

The output swing of the first amplifier in the interface circuit is relatively small, in the order of 200mV, because additional gain can be realized in the second amplifying stage. This makes it possible to use a telescopic OTA configuration, as shown in Fig. 5.6. This choice

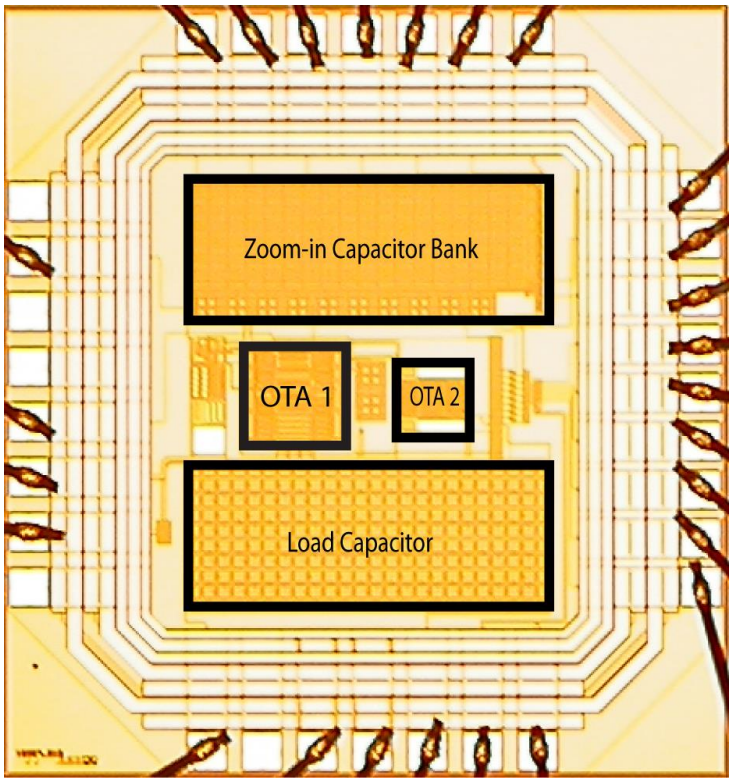

Fig. 5.8: Die micrograph of the realized interface circuit.

offers several advantages. First of all, a telescopic OTA has a high current efficiency. Secondly, because there are fewer noise-contributing transistors compared to other OTA topologies, such as the popular folded cascode topology, a telescopic OTA has a lower noise factor, which comes with the advantage of better interface circuit resolution. This again saves power, since according to formula (5.6), a smaller C_H can be used to reach the required resolution, hence less current is required to reach the same speed. In order to guarantee accurate charge transfer, the first OTA is gain-boosted [4] to provide a DC gain above 100dB over corners and output voltage swing.

For the second amplifier, the most important specification is that it can provide a large output voltage swing to enable use of the full input range of the following analog-to-digital converter stage. For this reason, a two-stage OTA configuration with Miller compensation has been chosen due to its large output swing. A simplified circuit diagram of the OTA in the second amplifying stage is illustrated in Fig. 5.7.

The zoom-in capacitor C_B is realized with poly-poly capacitors in the process. A back-to-back connection is used in the layout of C_B to cancel the first-order voltage dependency of

the zoom-in capacitor. The circuit is fabricated in a standard 0.35μm CMOS process. It consumes 2.4 mW from a 3.3 V supply. Figure 5.8 shows the chip photo and indicates various parts of the circuit.

5.4. Realizations and measurement results

A measurement setup including the realized frontend and DAQ board was used to measure the noise performance of the interface circuit. The DAQ facilitates the analog-to-digital conversion and acquires one result per cycle in the measuring phase. The standard deviation of the acquired results in a number of cycles shows the output-referred noise of the capacitance-to-voltage converter frontend. The input-referred capacitance resolution of the circuit can then be calculated from the measurement obtained and the transfer function. Figure 5.9 shows the measured samples of the frontend output voltage. When the excitation voltage is assumed to be 3.3V, which is the same level as the supply voltage, the input-referred capacitance resolution obtained from the measured standard deviation of the frontend output is 46 aF (RMS).

The output noise of the CVC was also measured against different input capacitance values. According to our analysis above, the output noise power should be proportional to the total capacitance connected to the amplifier inverting input, or $C_{IN} = C_S + C_B + C_P$. The measurement result is shown in Fig. 5.10, together with a linear interpolation. The interpolation line almost crosses the origin, which correlates well with the prediction shown in Eq. (5.6).

The linearity of the zoom-in frontend is also measured using the method described in [5]. In this method, the output voltage of the frontend of four different input capacitance values is measured, namely for C_{ref1}, C_{ref2}, $C_{ref1} + C_{ref3}$ and $C_{ref2} + C_{ref3}$. Supposing linear capacitance to voltage relationship, then the value of λ defined by the equation:

$$\lambda = \frac{V_{C_{ref\,2}+C_{ref\,3}} - V_{C_{ref\,1}+C_{ref\,3}}}{V_{C_{ref\,2}} - V_{C_{ref\,1}}} - 1 \qquad (5.7)$$

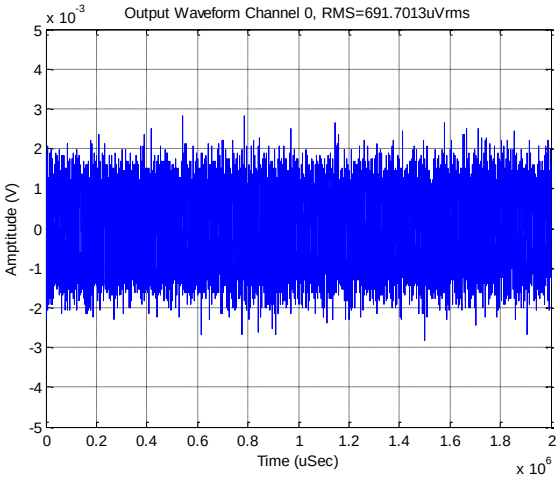

Fig. 5.9: Output noise power of the realized interface circuit. The standard deviation of those samples is calculated and given in the figure.

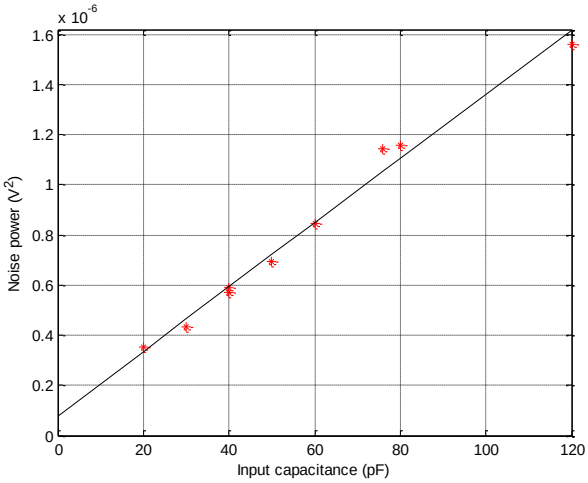

Fig. 5.10: Output noise power of the realized interface circuit measured at different values of total input capacitance.

should be zero. Any deviation of λ from zero can be defined as nonlinearity [5,6]. The on-chip binary-weighted capacitor bank used to realize the zoom-in capacitance is utilized to perform this measurement. The excitation voltage level is reduced, and the maximum capacitance variation is kept below 150 fF to prevent saturation of the output of the capacitance-to-voltage converter. Specifically, in this measurement, C_{ref1} is set to zero, so that only the parasitic capacitance is measured; C_{ref2} is set to $C_{B,LSB}$, or 50 fF; and C_{ref3} is consequently set to $C_{B,LSB+1}$, or 100 fF. The measured nonlinearity in this way is below 2.5×10^{-4} over a capacitance variation of 150 fF. Thus, the equivalent nonlinearity over this limited range of the capacitance-to-voltage converter is below 37.5aF, which is in line with its resolution.

5.5. Conclusions

In this Chapter, a frontend circuit for measuring small capacitance variation has been introduced. It utilizes baseline capacitance cancellation and provide high-resolution, high speed capacitance measurement.

In order to measure displacement, more information is needed. It can be seen from the ideal transfer function of the interface circuit in Fig. 5.5 that capacitors C_B, C_F, C_H and C_{F2} all affect the transfer function. As described in Chapter 2, calibration of those capacitors is needed. To be specific, the capacitive ratios C_F/C_B and C_{F2}/C_H need to be accurately determined, with the absolute capacitance of one of them known, in order for us to calculate the displacement information. The capacitance ratio measurements could potentially be conducted by using the existing hardware as shown in Fig. 5.5, where the sensor capacitor has been removed. However, this would not be a practical solution to reach the high accuracy requirement of the calibration measurement, as the Nyquist-rate ADC at the output of the interface would only be capable of up to 12-bit resolution.

A more practical way of realizing the additional measurements is to resort to the charge-balancing principle discussed in Section 2.4.3. Since the charge-balancing principle employs incremental sigma-delta conversion techniques, it can achieve the resolution requirements of the calibration measurements. The potential drawback of this approach, however, is that capacitors C_B, C_F, C_H and C_{F2} would need to be removed from the circuit and reconfigured to carry out the calibration measurement. This means those capacitors will see a different environment during the zoom-in measurement and calibration measurement, which could lead to extra error. For instance, the excitation voltage level will not be on the same order, so that error introduced by non-linearity of the capacitors will be present.

In the next chapter an overview will be made on the advantages and disadvantages of the designs in this work and the conclusion will be drawn.

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Chapter 6

Discussions and Conclusions

This final chapter presents a benchmark of capacitive sensor interface circuits. Then the main findings and contributions of this work will be summarized. Finally, a section will discuss the vision for the possible future improvements, from both circuit-level and system-level point of views.

6.1. Benchmark

Of the many performance parameters, the power-efficiency of a capacitive sensor interface circuit is the most often compared parameter. As the specifications of capacitive sensor interfaces differ greatly, in order to fairly compare the performance of capacitive sensor interfaces with different specifications, the so-called figure-of-merit (FoM) must be used to normalize the energy consumption of a design in relation to performance. For capacitive sensors, the FoM can be defined in a similar way to the Walden FoM often used for comparing the energy efficiency of general-purpose analog-to-digital converters (ADC):

$$FoM = \frac{Energy\ per\ conversion}{2^{ENOB}} \tag{6.1}$$

where the ENOB stands for effective number of bits, and is defined as:

$$ENOB = \frac{20 \cdot \log\left(\frac{C_{range}}{2\sqrt{2} \cdot C_{res}}\right) - 1.76}{6.02} \tag{6.2}$$

The performance results of state-of-the-art capacitive sensor interfaces published over the last decade with a variety of conversion principles have been summarized in Table 6.1, with the respective FoMs listed.

Table 6.1: Performance of state-of-the-art capacitive-sensor interfaces.

	Type	Tech.	Supply voltage	Current consum.	Meas. time	ENOB	FoM
[1]	CVC	0.18µm	1.2 V	0.13 µA	4 ms	11.8	183 fJ/step
[2]	CVC	0.18µm	1.8 V	85 µA	750 µs	11.7	34.5 pJ/step
[3]	CVC	0.35µm	1.8 V	460 µA	50 µs	10.2	35.9 pJ/step
[4]	CFC	0.7µm	5 V	1 mA	1 s	20.0	4.7 nJ/step
[5]	CFC	0.7µm	5 V	1.4 mA	100 ms	16.0	10.7 nJ/step
[6]	CFC	0.35µm	3.3 V	64 µA	7.6 ms	13.2	169 pJ/step
[7]	CFC	0.16µm	1 V	14 µA	6.9 ms	13.1	10.6 pJ/step
[8]	CFC	0.35µm	3 V	5 mA	50 µs	8.8	1.68 nJ/step
[9]	CFC	0.32µm	3 V	28 µA	33 µs	8.0	10.8 pJ/step
[10]	CFC	0.18µm	1 V	60 µA	30 µs	10.0	1.76 pJ/step
[11]	CFC	40nm	1 V	1.84 µA	19 µs	8.0	137 fJ/step
[12]	ΣΔ	0.35µm	3.3 V	436 µA	128 µs	11.0	89.9 pJ/step
[13]	ΣΔ	0.18µm	1.8 V	5.85 µA	10 ms	13.0	13.1 pJ/step
[14]	ΣΔ	0.18µm	1.2 V	8.60 µA	800 µs	12.5	1.4 pJ/step
[15]	ΣΔ	0.35µm	3.3 V	230 µA	10.5	16.7	74 pJ/step
[16]	SAR	N.A.	1.4 V	360 µA	2 µs	6.8	7.9 pJ/step
[17]	SAR	0.35µm	3.3 V	91 µA	650 µs	10.7	116 pJ/step
[18]	SAR	0.18µm	1.2 V	5.37 µA	16 µs	11.6	34 fJ/step
[19]	Zoom	0.18µm	1.8 V	19 µA	230 µs	15.4	174 fJ/step
[20]	Zoom	0.18µm	1.8 V	4.60 µA	100 ms	18.7	1.88 pJ/step
[21]	SAR+VCO	40nm	1 V	75 µA	1 µs	10.4	57 fJ/step
Ch. 4	**CVC**	**0.35µm**	**3.3 V**	**750 µA**	**20 µs**	**14.3**	**2.46 pJ/step**
Ch. 3	**ΣΔ**	**0.35µm**	**3.3 V**	**4.5 mA**	**20 µs**	**13.8**	**20.9 pJ/step**

In Table 6.1, it can be seen that the two designs presented in this thesis have achieved higher ENOB than state-of-the-art designs with similar conversion time. This illustrates one of the design goal of realizing fast capacitive interface circuits. Of course, the short conversion time is fuelled with larger current consumption, as can be seen from Table 6.1. It is therefore interesting to look at the energy efficiency of those designs against state-of-the-art capacitive sensor designs.

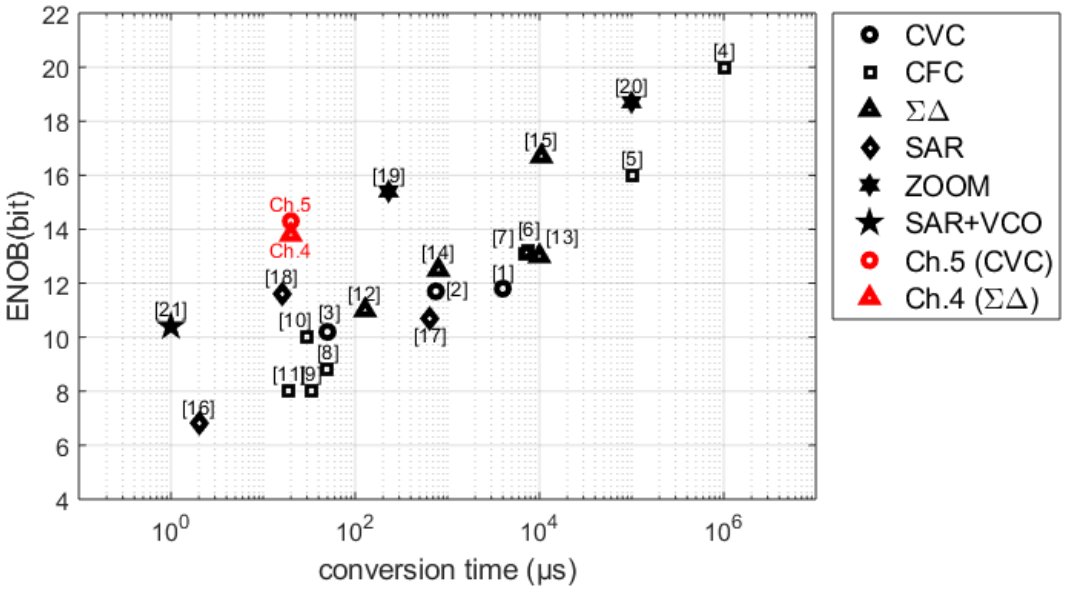

Fig. 6.1: ENOB of state-of-the-art capacitive sensor interface circuits versus their conversion time

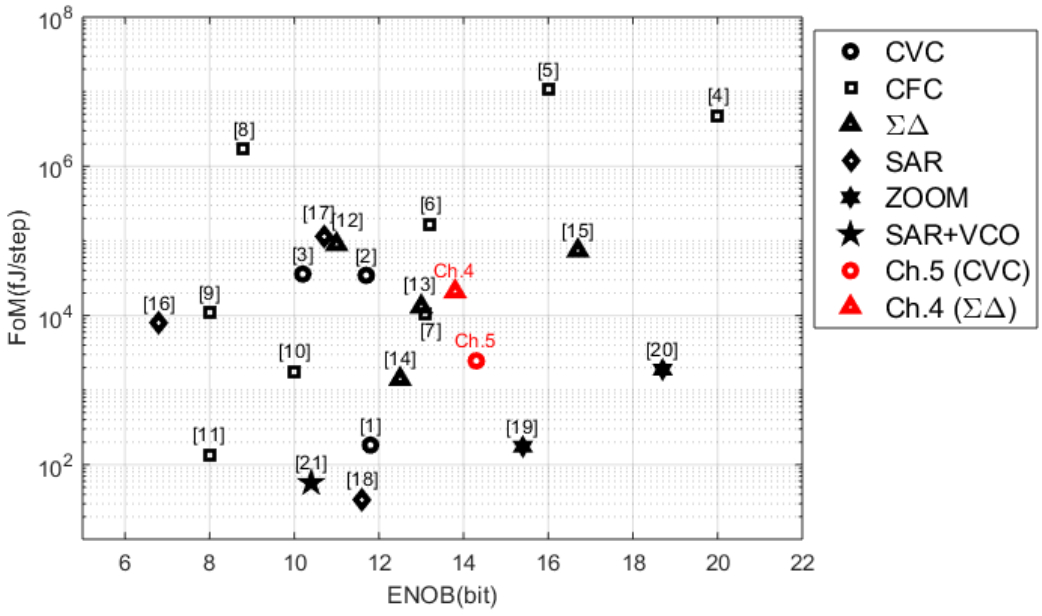

Fig. 6.2: Comparison of FoMs of state-of-the-art capacitive sensor interface circuits

In order to more easily visualize the relative energy efficiency performances the FoM of all those designs are plotted against their ENOB in Fig. 6.2. It can be seen that the two designs presented in Chapters 4 and 5 have achieved solid energy efficiency with FoMs of 20.9

pJ/step and 2.48 pJ/step, respectively. For capacitive sensor interface circuits with ENOB higher than 13 bit, the two designs presented in this thesis represent good energy efficiency especially for high-resolution capacitive sensor interface designs.

Although according to the ENOB definition given in Eq. 6.2 both designs are rated as ~14-bit CDCs, these designs could be easily modified to cover an input capacitance range from 0 pF to 12 pF without degrading the respective capacitance resolution performance. In other words, as general-purpose CDCs, the two designs could achieve higher ENOBs, equivalent to ~16-bit CDCs. Especially for the ΣΔ-based CDC in Chapter 4, if the design is used to interface a differential capacitive sensor instead of a single-ended one as in the application, it could gain 1 extra bit of ENOB. Furthermore, the superior 20-bit linearity also sets the ΣΔ-based CDC design apart.

Fig. 6.3 replots the data in Fig. 6.2 by highlighting with red rectangles the designs reported after 2011. It can be seen that in the last few years after the publication of the two designs in this thesis, drastic steps have been taken to achieve better FoM numbers for multiple interfacing principles. In [1,11,18,19,21], sub-pJ/step FoM numbers as low as 33fJ/step have been reported, which is more than two orders of magnitude lower than the designs presented in this thesis. These works are all very energy-efficient CDC designs that push the energy efficiency limits to new levels. However, the merits of a CDC should not be solely based on energy efficiency, as other specifications will have influence on architecture choices affecting the achievable FoM. Taking a careful look at those designs with remarkably low FoM numbers, we can see that most resolution levels targeted were not very high, both in relative and in absolute terms.

The CDC design in [1] is based on a CVC followed by an SAR ADC, which has an effective ENOB of 11.8 bits over an input range of 72.8 pF, and an absolute capacitance resolution of only 6 fF_{rms}. This design is very similar to the CVC-based CDC presented in Chapter 5 of this thesis and achieves a better FoM by operating in quantization-noise limited region.

The CDC design proposed in [11] is a highly digital alternative which uses a delay chain that gradually discharges the sensor capacitor, and controls the delay with the voltage across the sensor capacitor. This design can be classified as a CFC-based CDC, as the time taken for the delay in the inverter chain to catch up with the delay in a reference delay chain is proportional to the sensor capacitor. While this technique is highly energy-efficient, the

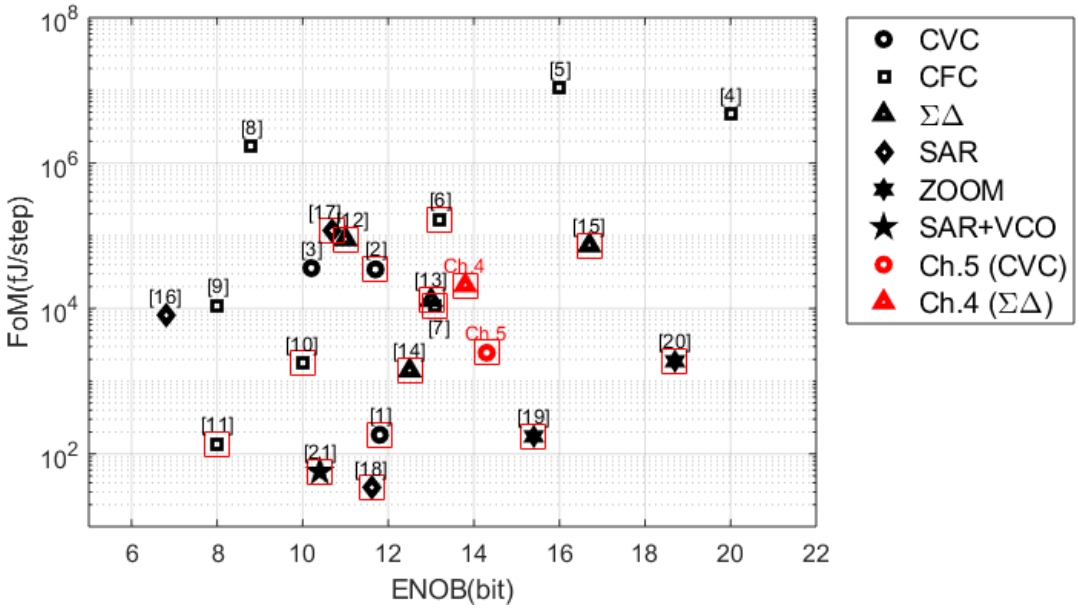

Fig. 6.3: Comparison of FoMs of state-of-the-art capacitive sensor interface circuits, with designs after 2011 high-lighted by red rectangular

resolution achieved is limited to 8 bits and the absolute capacitance resolution is 12.3 fF_{rms}. Therefore this technique is not suitable for sensing small capacitance changes.

The CDC designs in [18] and [21] can both be classified as SAR-based CDCs. Previous SAR-based CDCs generally use an operational transconductance amplifier (OTA) to perform the active charge transfer, which provides immunity to parasitic capacitances on the sensor node. However, OTAs are relatively power-hungry. In [18] the use of passive charge transfer in combination with a power-efficient inverter-based amplifier as the SAR comparator results in a very high energy efficiency and a FoM as low as 35 fJ/step. In [21] passive charge transfer is also used, while the SAR residual voltage is used to control a VCO for fine quantization on top of the SAR quantization, which also results in an impressive FoM of 55 fJ/step. However, both designs have a limited ENOB of ~10 bits, with absolute capacitance resolution of 1.1 fF_{rms} in both cases.

The CDC design in [19] is a zoom-based CDC. Since the first-stage SAR already performs coarse quantization, the resolution requirement for the fine conversion is reduced, and only a modest OSR is required, improving energy efficiency compared to a stand-alone CDC. This particular design employs a 9-bit SAR section, which has in total 512 unit reference capacitors. However, in order to obtain the optimal FoM value, an OSR of only 32 is used.

This means that the accuracy and linearity benefits of the zoom-based CDC could not be fully exploited as the dynamic-element-matching algorithm has too few clock cycles to achieve sufficient averaging. This can be observed by the ±150 ppm INL, which only corresponds to 11.4-bit linearity, while the design claims 15.4-bit resolution. The absolute capacitance resolution is 155 aF_{rms} while the input range is 24 pF.

The other zoom-based CDC presented in [20] has a more reasonable architecture with a 5-bit SAR section, or 32 unit reference capacitors. With an OSR of 3500 in the ΣΔ section, this work achieves an absolute capacitance resolution of only 2.5 aF_{rms} while the input range is 3.8 pF, or an ENOB 18.7 bits. Furthermore, a solid FoM of 1.8 pJ/step has been achieved. This design achieves excellent energy efficiency by using an energy-efficient current-reuse OTA that reaches current efficiency on par with that of an inverter-based OTA [20]. Inspired by this design, in section 6.3 discussions will be presented on possible ways to improve the two designs presented in this thesis.

6.2. Main findings and contributions

The main findings of this thesis are summarized below.

The background of capacitive displacement sensors and capacitance interface circuits is discussed. The discussion of the interface circuit is extended to the references used.

When measuring very small displacements with capacitive sensors, the baseline capacitance often comes as a trade-off in the sensor head design for other mechanical parameters. Unfortunately, a high precision capacitive sensor head also has relatively large baseline capacitance compared to its capacitance variation. In order to design a power-efficient interface circuit for such capacitive sensors, baseline capacitance cancellation technique is proposed.

Baseline capacitance cancellation techniques, however, introduce one additional capacitance which also needs to be calibrated. An error budget analysis showed that due to the limited sensor capacitance variation range, a trade-off exists with the selection of the zoom-in factor in the baseline capacitance cancellation and the accuracy requirement in the calibration steps. In order to avoid deterioration of the speed performance of the capacitance interface due to the calibration steps, a periodic calibration is proposed provided that good short-term stability can be achieved by the interface circuit.

A capacitance-to-voltage converter (CVC) is proposed, to be used to realize a signal-conditioning circuit for the capacitive sensor. A two-stage design yields a CVC that can deliver the required closed-loop gain and also maintain a near peak-to-peak output voltage swing to drive the following ADC stage. The required resolution is achieved by means of bandwidth limitation through a large capacitor, resulting in a state-of-the-art high-speed power-efficient capacitive-sensor interface based on capacitance-to-voltage conversion. This interface requires additional circuitry to carry out the calibration.

It has been proposed to use incremental ΣΔ modulators to realize the calibration as they can achieve high precision measurements. The baseline capacitance compensation can also be applied to capacitance-to-digital converters (CDC) based on the incremental ΣΔ modulation technique. It has been shown that the combination of baseline capacitance cancellation and use of high-order loop filters can help to achieve a good balance between quantization noise and thermal noise. The result is the realization of a state-of-the-art high-speed capacitive-sensor interface based on incremental ΣΔ modulation with good power efficiency. Above all, the same interface can be re-configured to realize the calibration measurement, where excellent precision and stability have been demonstrated.

6.3. Future research directions

Looking into the future, we see that the need for energy-efficient CDCs is still very strong. In quite a few application areas, the accuracy requirements for such CDCs are not very high, and many principles make use of OTA-less architectures to achieve good energy efficiency. However, there are also a number of applications where the required accuracy can only be met through active charge transfer with the help of OTAs. In those cases, the application of an energy-efficient OTA is the key to achieving good energy efficiency.

In order to improve the energy efficiency of the designs presented in this thesis, two approaches can be used. The first approach is to try to increase the capacitance resolution by reducing the noise of the CDC. The second approach is to employ more energy-efficient OTAs in the design. In the design of Chapter 4, a gain-boosted folded-cascode OTA topology was chosen whereas in the design of Chapter 5, a gain-boosted telescopic OTA topology was chosen. Generally speaking, energy-efficient OTAs often have simultaneously better noise performance, as can be seen from the analysis below.

The noise performance of different OTA topologies, when the feedback network is otherwise the same, can be captured by a parameter called noise factor N_f, generally defined as the sum of the transconductance of all noise-contributing transistors in the signal path divided by the transconductance of the input pair of the OTA:

$$N_f = \frac{\Sigma g_m}{g_{m,in}} \tag{6.3}$$

The energy efficiency of different OTA topologies, when the supply voltage is constant, can be compared by looking at the bias current efficiency factor γ, defined as the ratio between the realized transconductance g_m and the total bias current I_{tot}:

$$\gamma = \frac{g_m}{I_{tot}} \tag{6.4}$$

The circuit diagram of a conventional folded-cascode OTA is shown in Fig. 6.4. This topology has been quite popular mainly because it provides a reasonable output swing which is not affected by the input common-mode voltage, making it suitable for a wide range of applications. The downside of this topology, however, is that it has a high noise factor and is also not very power-efficient. As is shown in Fig. 6.4, apart from the input pair M1 and M2, the mirror current sources M3 and M4, and the top current sources M5 and M6 all contribute to noise. This is especially true for the mirror transistor, which carries

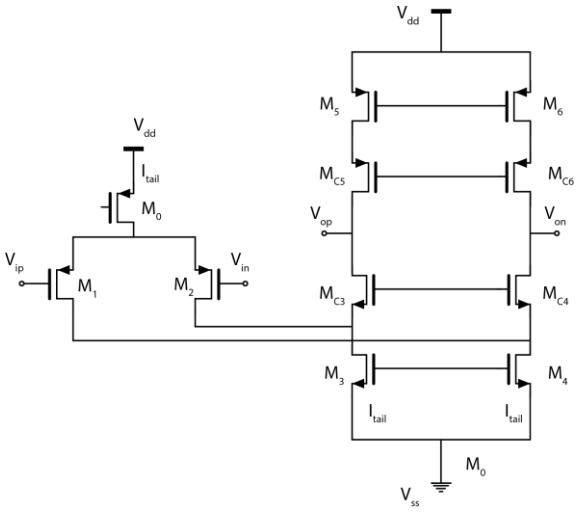

Fig. 6.4: Folded-cascode OTA.

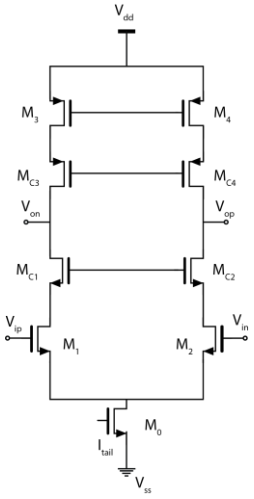

Fig. 6.5: Telescopic OTA.

twice the bias current as compared to the input transistor. The noise contribution from the cascode transistors can in general be ignored. The noise factor of a folded-cascode OTA can be expressed as:

$$N_{f\_fc} \approx 1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m5}}{g_{m1}} \tag{6.5}$$

Generally speaking, current sources are often biased to generate much less transconductance compared to input pair devices. Even so, because the mirroring current sources M3 and M4 carry twice the drain current compared to the input pair transistors M1 and M2, it is quite easy to obtain a noise factor close to two for a folded cascode OTA topology.

It normally requires a total bias current I_{tot} of two times I_{tail} (which is the bias current of the input differential pair). If we assume that the biasing point of the input pairs for all OTA topologies are made the same and that I_{tail} yields g_{m1}, for a folded-cascode OTA, the current efficiency is:

$$\gamma_{fc} = \frac{g_{m1}}{2 \cdot I_{tail}} \tag{6.6}$$

The circuit diagram of another frequently used topology, the telescopic OTA, is shown in Fig. 6.5. Here no mirror current source is present, all the transistors in the signal path are stacked vertically, and the structure consumes one times I_{tail} to generate the same amount of input pair transconductance g_{m1}. Thus the noise factor and current efficiency of a telescopic OTA are respectively:

$$N_{f\_te} \approx 1 + \frac{g_{m3}}{g_{m1}} \tag{6.7}$$

$$\gamma_{te} = \frac{g_{m1}}{I_{tail}} \tag{6.8}$$

It can be seen that the noise factor of a telescopic OTA can be reduced compared to that of a folded-cascode OTA, which can be quite advantageous in thermal-noise-limited designs. However, a major disadvantage of a telescopic OTA is the limited output swing, and the fact that a strong relation exists between the available output swing and the input and output common-mode levels.

In recent years, another class of OTAs which are called inverter-based OTAs have gained noticeable popularity among circuit designers, due to the superior current efficiency demonstrated. In fact, the inverter-based OTA shown in Fig. 6.6 outperforms the conventional OTAs in terms of current efficiency because both the PMOS and the NMOS transconductances contribute to the GBW of the OTA. If the PMOS and the NMOS transistors are biased to have the same amount of transconductance, the current-efficiency of an inverter-based OTA can be twice that of a telescopic OTA. Due to the omission of current-source transistors from the signal path, the inverter-based OTA will also have a noise factor close to unity:

$$N_{f\_inv} \approx 1 \tag{6.9}$$

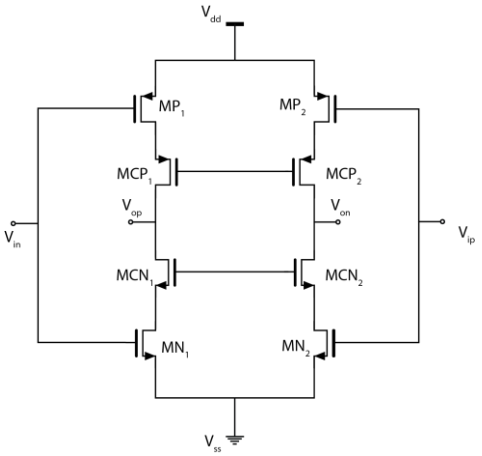

Fig. 6.6: Inverter-based OTA (biasing network not shown).

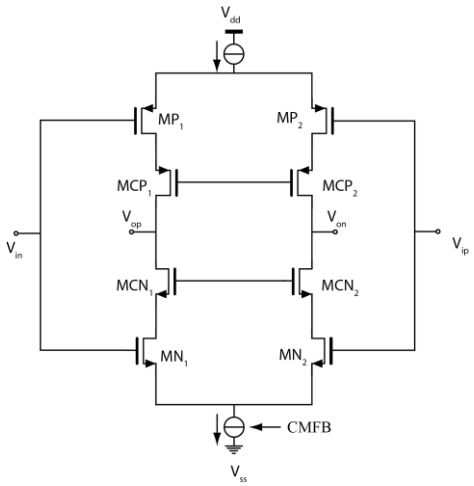

Fig. 6.7: Current-reuse OTA.

$$\gamma_{inv} = \frac{2 \cdot g_{m1}}{I_{tail}} \tag{6.10}$$

In contrast to an inverter-based OTA, which needs dynamic biasing in most cases, a current-reuse OTA topology has been proposed that is more similar to a conventional telescopic OTA. A circuit diagram of the current-reuse OTA is shown in Fig. 6.7. The current-reuse OTA can be understood as a telescopic OTA with output current sources that have been replaced by another differential pair. Here again, as in the case of the telescopic OTA, the output swing is limited. This topology also has the same level of current efficiency, all the advantages of inverter-based OTAs mentioned before, and it is at the same time a fully differential OTA as well. The noise figure of this topology is again close to unity, which is also very favorable:

$$N_{f\_cr} \approx 1 \tag{6.11}$$

$$\gamma_{cr} = \frac{2 \cdot g_{m1}}{I_{tail}} \tag{6.12}$$

However, the prior analyses have all ignored the noise contribution of the gain-boosting amplifiers. This was done to simplify the analysis. In applications that do not require high speed, long channel-length transistors can be used in the OTA designs such that even without gain-boosting, gains exceeding 90dB can be obtained. On the other hand, for high speed applications, short-channel-length transistors would have to be used to push the non-dominant poles of the OTA to higher frequencies and increase the obtainable unity gain bandwidth, so that gain-boosting techniques are needed for sufficient DC gain. The additional noise contributed should be accounted for.

From the above analysis, it can be seen that in order to increase the energy efficiency of the designs presented in this thesis, a more energy-efficient OTA topology such as a current-reuse OTA or inverter-based OTA should be used. DC gain should be obtained by means of longer channel devices instead of techniques such as gain-boosting. However, increasing the transistor channel length will decrease the non-dominant pole frequency of the OTA, thus posing a limit to the achievable maximum gain-bandwidth product of the amplification stage. Furthermore, as the zoom-in factor increases, and since the speed requirement is also

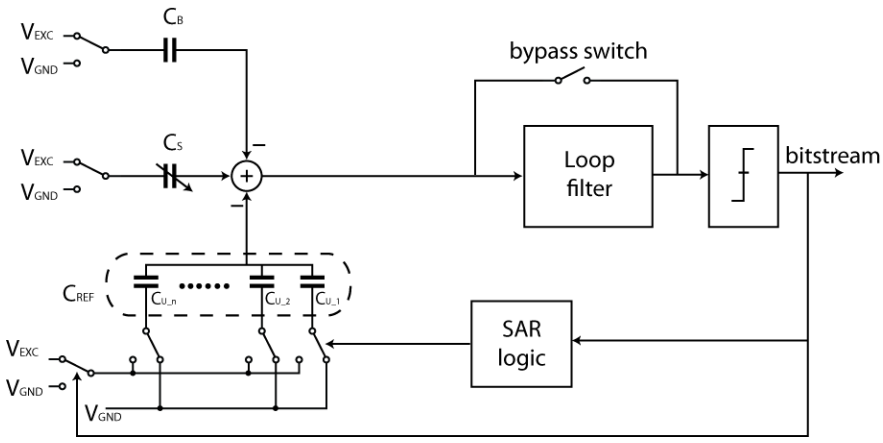

Fig. 6.8: Additional baseline capacitance compensation on top of a zoom-based CDC can help extend the measurement range.

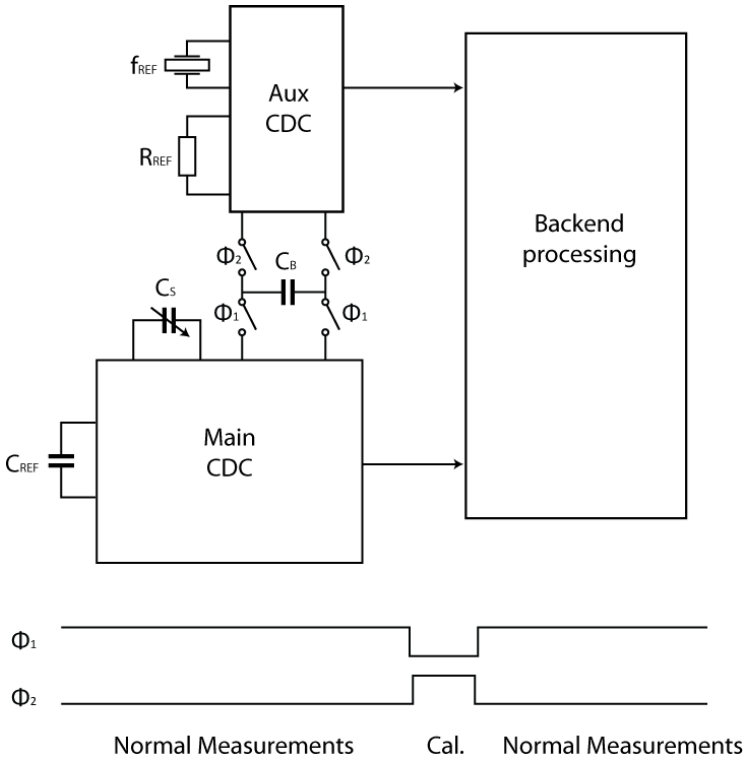

Fig. 6.9: Main CDC for fast real-time measurement and auxiliary CDC for calibrating the capacitance of the main CDC.

high, it will become difficult to achieve sufficient DC gain without using techniques such as gain-boosting.

Apart from this, zoom-based CDCs are more elegant in the sense that if the dynamic-element-matching algorithm has enough clock cycles to achieve sufficient averaging of the mismatch errors in the capacitive DAC (CapDAC), it would not be necessary to include the separate calibration step that is required to calibrate the ratio between C_{REF} and C_B. However, for high-speed, large zoom-in factor CDCs this requirement may still be difficult to fulfil, as the number of clock cycles N is limited while the required CapDAC elements are comparably large. However, this problem could be partially solved by using the combination of the zoom-based CDC with additional baseline capacitance cancellation, as is shown in Fig. 6.8. An additional baseline compensation capacitor C_B is added to the zoom-based CDC to compensate for the excess baseline capacitance that the C_{REF} CapDAC alone is not able to fully compensate for. With this solution, the ratio between C_{REF} and C_B still needs to be measured. However, in this case the effective input capacitance variation range, before the addition of another calibration step, is equal to the whole C_{REF} CapDAC

instead of just a unit of C_{REF} CapDAC capacitance. This can be a significant advantage especially when the sensor capacitance variation range is relatively large compared to the baseline capacitance. With this approach, large effective zoom-in factors can still be realized.

Finally, this research has focused on realizing a high-speed high-resolution capacitive sensor readout circuit capable of conducting low-latency capacitance ratio measurements. However, as discussed in Chapter 2, in order to measure displacement, the absolute capacitance needs to be known as well. Combining the high-speed high-resolution capacitive sensor readout circuit with a precision CDC to form a high-speed CDC system with backend reference sensor calibration will then result in a capacitance measurement system with which exceptional temperature and long-term stability can be achieved at the same time. One possible implementation of such a system is shown in Fig. 6.9. In parallel to the fast CDC, the slow but precise CDC [22] can periodically calibrate the capacitive reference of the fast CDC.

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Summary

This thesis describes the theory, design, and implementation of high-speed capacitive displacement sensor interface circuits. The intended application is to readout the capacitive displacement sensor used in a servo loop, where the measurement time needs to be low to ensure loop stability.

This thesis is organized as follows. After the introduction, Chapter 2 provides a detailed survey of the operating principles and the performance of state-of-the-art capacitance measurement circuits. The result of the survey provides a solid understanding of the limitations of the existing solutions and the pros and cons of each circuit topology. Out of this investigation, the mainly limiting factor for achieving high speed while guaranteeing the required accuracy is the relatively large baseline capacitance of the sensor capacitor.

Chapter 3 introduces the concept of baseline-capacitance compensation technique which can help reduce the dynamic range requirement for the interface dramatically and improve the achievable energy efficiency of the interface circuit. However, it also has its associated limitations and in this chapter ways to solve the associated problems with baseline-capacitance cancellation is analyzed.

Chapter 4 presents a reconfigurable low-power CDC based on ΣΔ converters that can be used to realize both zoom-in, high-resolution, high-speed capacitance measurement and high-resolution, large dynamic range, low-speed capacitance measurement. This CDC can be configured to realize baseline-capacitance cancellation and reach a high energy-efficiency and high conversion speed, and this mode is named standard operation mode. It can also be configured to measure the relative stable baseline capacitance with high accuracy, which is needed in relating the capacitive sensor variation to displacement. In standard operation mode, it employs baseline capacitance cancellation to achieve an effective capacitance resolution of 65aFrms within 20μs. This is achieved with a power consumption of 15mW. Using the same charge-balancing principle, the relationship between the baseline capacitance and the reference capacitance can be determined using

the same hardware with high accuracy, which can be done in the calibration steps. Greater than 17-bit precision has been demonstrated with excellent linearity.

Chapter 5 presents an alternative solution that can be used to deliver a baseline-capacitance-cancellated, high-resolution, high-speed capacitance measurement with low power consumption. However, to make the measurement system complete, the baseline-capacitance still needs to be calibrated against the reference capacitor. This could be done using the same charge-balancing principle presented in Chapter 4.

In Chapter 6, the presented capacitive-sensor interfaces in this thesis are compared to a survey of capacitive-sensor interfaces reported in the literature, which also cover many other interfacing principles. This comparison confirms the effectiveness of the approaches used in the designs described in this thesis. The last part of the thesis presents future research directions.

List of Publications

Book Chapters

S.Xia, and S. Nihtianov, "Capacitive Sensors for displacement measurement in the subnanometer range," in *Smart Sensors and MEMS: Intelligent Devices and Microsystems for Industrial Applications*, S Nihtianov, A. Luque, Woodhead Press, 2013.

Journal Papers

S. Xia, and S. Nihtianov, "Power-efficient high-speed and high-resolution capacitive-sensor interface for sub-nanometer displacement measurements," Instrumentation and Measurement, IEEE Transactions on, vol. 61, pp. 1315-1322, 2012.

Conference Papers

S. Xia, K. Makinwa, and S. Nihtianov, "A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International, 2012, pp. 198-200.

S. Xia, and S. Nihtianov, "Comparison of different methods to cancel offset capacitance in capacitive displacement sensors," in Instrumentation and Measurement Technology Conference Proceedings, 2012 IEEE International, 2012.

S. Xia, and S. Nihtianov, "Zoom-in front-end circuit for high-performance capacitive displacement sensors," in Conference of the IEEE Industrial Electronics Society (IECON), 2011, pp. 2657-2662.

S. Xia, and S. Nihtianov, "Capacitive sensor system for sub-nanometer displacement measurement," in SENSORS, 2011 IEEE, 2011.

S. Xia, and S. Nihtianov, “Zoom-in frontend for power-efficient high-speed and high-resolution capacitive sensor measurement system,” in Instrumentation and Measurement Technology Conference, 2011 IEEE International, 2011.

S. Xia, J. P. van Schieveen, S. Nihtianov, J. W. Spronck, “Concept evaluation of a high performance self-aligning capacitive displacement sensor,” in Conference on Industrial Technology, 2010 IEEE International, 2010, pp. 1575-1580.

S. Xia, F. Sarubi, R. Naulaerts, S. Nihtianov, L. Nanver, “Response Time of Silicon Photodiodes for DUV/EUV Radiation,” in Instrumentation and Measurement Technology Conference, 2008 IEEE International, 2008.

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Sha Xia

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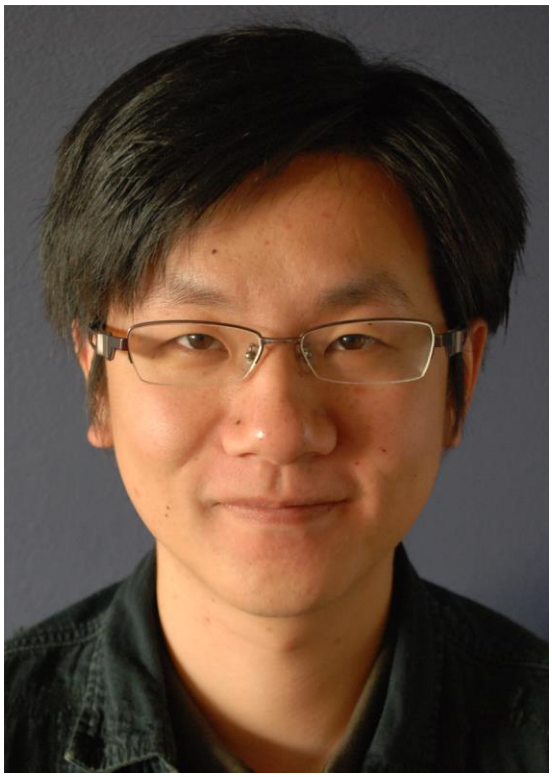
About the Author



Sha Xia was born in Wuhan, China, in March 1982. He received his B.Sc. degree from Wuhan University, Wuhan, China in 2004 and his M.Sc. degree (cum laude) in 2007 from Delft University of Technology, Delft, the Netherlands, where he was working on modelling and optimization of an electro-thermal filter (ETF).

From 2007 to 2012, he was working towards his Ph.D. degree at the Electronic Instrumentation Laboratory, from Delft University of Technology, Delft, the Netherlands. His work involved ASIC design for high-precision capacitive displacement sensor readout circuits. His research interest includes sensor conditioning circuits and data converters.

Since August 2012, he has been a senior analog circuit designer with NXP semiconductor, Eindhoven, the Netherlands, where he works mainly on the design of various high-accuracy smart temperature sensors in different technologies.

In his spare time, he likes playing guitar (mainly classic rock music and blues music). He also enjoys fitness, swimming and gardening.

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