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DC Fault Ride-Through and AC Grid Support

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Protection of Multiterminal HVDC Grids based on Modular Multilevel Converters

DC Fault Ride-Through and AC Grid Support

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. dr. ir. T.H.J.J. van der Hagen,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
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“ Ἐὰν μὴ ἔλπηται, ἀνέλπιστον οὐκ ἐξευρήσει,
ἀνεξερεύνητον ἐὸν καὶ ἄπορον.”
- Ἡράκλειτος ὁ Ἐφέσιος

Contents

Summary

High Voltage DC (HVDC) grids provide an efficient solution for the transmission of bulk power over long distances between the energy production and consumption centers. Up to now, most of the implemented dc connections are point-to-point, creating dc links to strengthen the existing, predominantly ac, electricity grid. However, to optimize the use of assets and energy harvest, multi-terminal HVdc grids are envisioned. Based on recent research and industrial trends, the Multilevel Modular Converter (MMC) technology will be the building block for the realization of these grids. Yet, as the grid structure becomes more complex, the protection of HVDC grids poses one of the most important challenges.

This dissertation proposes different ways to isolate and ride through dc faults, while maintaining controllability of the converters that can offer ancillary services to their respective ac grid, having as a main objective to reduce the downtime of the grid and the time in which assets are not utilised. More specifically:

- The characteristics of dc faults and the main parameters which affect the fault response are investigated.
- A dc breaker optimized design is proposed which allows equipment sharing, offering bidirectional isolation capability for multiple lines at the same time.
- In case MMC with fault-blocking capability is used, e.g. Full-bridge MMC, a methodology for dc fault ride-through is proposed. Moreover, a dc current controller is presented, ensuring that the MMC can continue its controlled operation towards the respective ac grid.
- Once the dc side is isolated, the MMC operation as STATCOM is studied. More specifically, a control structure is proposed to maintain internal balancing of the converter, while ensuring Low-Voltage-Ride-Through (LVRT).
- The capability of the MMC to operate as Active Power Filter (APF) is also investigated. A selective harmonics detection and control method is presented and experimentally verified for the mitigation of high-order current and voltage harmonics up to 13^{th} order.

Each of the aforementioned topics is dealt with in a respective Chapter of this dissertation and a more detailed summary is provided hereby.

DC fault characteristics

To handle dc faults, the dc fault development stages and the fault dynamics in dc connections are first analysed. These phenomena become complex once the converter station response is considered. Therefore, this dissertation establishes analytical expressions for the three main fault development stages, which are experimentally verified. The effect of the grid and fault parameters on the grid fault response, such as the dc grid configuration, the fault type, the fault impedance and the converter tripping, are explained using the experimental results. The obtained results are of great importance to the system designer in order to estimate the stresses anticipated on the dc cables, as well as on the converter components, and they can be used to determine the protection system design requirements.

Multi-line breaker design
After analysing the characteristics of dc faults, protection methods need to be established. A dc breaker arrangement is proposed that is highly modular in design and is able to protect multiple lines at the same time. This is achieved through the optimization of the number of the involved switching elements and conduction paths to allow bidirectional fault isolation capability. The performed study showed that the breaker operation (e.g. total interruption time, commutation times, fault current peak) is similar to other hybrid breakers, while offering a more cost-effective solution, especially for radial grids.

DC fault ride-through using Full-bridge MMC
In case Full-bridge MMC technology with fault-blocking capability is employed, dc breakers could be avoided. In this case, a step-by-step methodology is proposed to ride through dc faults. A dc current controller is presented, along with internal balancing controllers, to ensure that the MMC maintains controllability during dc faults. Therefore, it is able to provide ancillary services to the respective ac grid, while the dc fault or the maintenance of the faulty dc line is ongoing.

Low-Voltage-Ride-Through
While the MMC remains disconnected from the dc grid, it would be beneficial to provide ancillary services to the respective ac grid, taking advantage of its high controllability. To this end, the capability of the MMC to provide reactive power support and LVRT is investigated. While the MMC follows the LVRT grid requirements for different voltage sag types, it was observed that the MMC faces internal balancing problems which affect its operation and can lead to the converter tripping. This problem was solved by designing an arm and a leg energy balancing controller which are simple in implementation and help the MMC remain balanced. The tuning process of the controllers is presented and the effect of the controllers is experimentally verified, taking into account the non-linearities of the modulation and the delays of the system.

High-order harmonic mitigation
Another important application of the MMC could be as APF, mitigating harmonics resulting from non-linear loads connected to the ac grid. Recent grid codes require the filtering of high-order current and voltage harmonics. This dissertation proposes a selective harmonics detection and control method. Taking advantage of the high bandwidth of the MMC, while maintaining low effective switching frequency of each submodule, the obtained results prove that harmonics up to 13^{th} order can be effectively mitigated. Since, harmonic elimination cannot be proven in simulation using a simplified model, extensive experimental results are provided for both current and voltage harmonics, proving the effectiveness of the proposed detection and control methods.

Overall, this dissertation deals with the challenge of dc faults from different perspectives, showing that a more holistic approach is necessary in such studies. Most importantly, this work provides insights into the dc fault development, proposing solutions for its isolation and ride-through, while at the same time, it presents the possibilities of continued operation of the MMC, even when a dc fault affects the whole or part of a dc grid.

Samenvatting

High Voltage DC (HVDC) netwerken zijn een efficiënte oplossing voor de transmissie van grote vermogens over lange afstanden, bijvoorbeeld tussen de productie en consumptie centra. Tot nu toe zijn de meeste dc toepassingen van punt tot punt, hier worden dc-links voornamelijk gebruikt om het huidige wisselspanningsnetwerk te versterken. Echter om het gebruik van assets en energiewinning te optimaliseren heeft men multi-terminal HVDC netwerken voor ogen. Uit recentelijk onderzoek en industriële trends blijken dat de Multilevel Modular Converter (MMC) technologie één van de bouwstenen voor de realisatie van deze netwerken wordt. Niettemin, met de toenemende complexiteit van netwerkstructuren wordt de beveiliging van HVdc netwerken één van de belangrijkste uitdagingen.

Dit proefschrift stelt verschillende manieren voor om fouten te isoleren en af te schakelen, terwijl de controle over omzetters, die ondersteuning leveren aan het wisselspanningsnetwerk behouden blijft. Het belangrijkste doel is om de uitvaltijd van het netwerk en de tijd dat assets niet worden gebruikt te verminderen. Meer specifiek worden de volgende onderwerpen onderzocht:

- De eigenschappen van dc fouten en de belangrijkste parameters die invloed hebben op deze fouten.
- Een geoptimaliseerd gelijkstroomonderbreker ontwerp welke het functioneel delen van apparatuur mogelijk maakt en tevens geschikt is voor bi-directionele isolatie van meerdere lijnen.
- Een voorgestelde methodologie voor het doorstaan van een tijdelijk fout als een MMC met fout blokkerende capaciteiten wordt gebruikt (bijvoorbeeld een Full-bridge MMC). Verder, een gelijkstroom controller die toestaat dat de MMC een bijdrage blijft leveren aan het desbetreffende wisselspanningsnetwerk.
- De STATCOM werking van de MMC als de gelijkspanning kant geïsoleerd is. Meer specifiek een controle structuur, die de interne balancering van de omzetter in stand houdt terwijl Low-Voltage-Ride-Through (LVRT) gewaarborgd wordt.
- Het vermogen van een MMC om te opereren als een Active Power Filter (APF). Een selectieve harmonische detectie en controle methode wordt gepresenteerd. Deze methode is experimenteel geverifieerd voor de onderdrukking van stroom en spanning tot de 13^e harmonische.

Elk van de genoemde onderwerpen wordt besproken in een hoofdstuk in dit proefschrift, waarvan hieronder een meer gedetailleerde beschrijving wordt gegeven.

DC fout karakteristieken
Om met dc fouten om te kunnen gaan worden eerst de verschillende stadia van dc fouten en de foutdynamiek geanalyseerd. Deze fenomenen worden complex als rekening wordt gehouden met de respons van het omzetter station. Daarom worden er in dit proefschrift analytische vergelijkingen vastgesteld voor de drie belangrijkste stadia van fouten, welke

experimenteel geverifieerd worden. Gebruikmakend van de experimentele resultaten wordt aan de hand van het effect op het netwerk en foutparameters, het gedrag van de fout verklaard. De onderzochte typische foutparameters zijn: de netwerk configuratie, het type fout, de foutimpedantie en het trippen van de omzetter. De verkregen resultaten zijn van groot belang voor de systeemontwerper. Deze worden gebruikt voor het schatten van de verwachte belasting van de dc kabels, de onderdelen van de omzetter en het vaststellen van de vereisten voor het beveiligingssysteem.

Multi-lijn onderbreker ontwerp
Na de bestudering van de karakteristieken van dc fouten moeten de beveiligingsmethoden vastgesteld worden. Een modulaire rangschikking van dc onderbrekers wordt voorgesteld welke meerdere lijnen tegelijk kunnen beveiligen. Dit wordt bereikt door de optimalisatie van de hoeveelheid schakelende elementen en geleidende paden die zorgen voor bi-directionele foutisolatie. De resultaten laten zien dat de werking van de omzetter (bijvoorbeeld voor: de totale onderbrekingstijd, de commutatietijden en de piekstroom) vergelijkbaar is met andere hybride onderbrekers. Tevens is het kostenefficiënter voor radiale netwerken.

Bedrijfsvoering van een Full-bridge MMC tijdens dc fouten
Als de Full-bridge MMC technologie met fout blokkeringscapaciteit wordt toegepast, zijn dc onderbrekers in principe overbodig. In dit geval wordt er een stap-voor-stap methode voorgesteld om tijdens dc fouten in bedrijf te blijven. Om ervoor te zorgen dat de MMC beheersbaar blijft gedurende dc fouten, wordt er in combinatie met de interne balanceringscontrollers een dc stroom controller gepresenteerd. Hierdoor kan de MMC aanvullende diensten leveren aan het wisselspanningsnetwerk terwijl er een fout, of onderhoud gaande is aan de gelijkspanningslijn.

Low-Voltage-Ride-Through
Het is gunstig als de MMC aanvullende diensten kan leveren aan het wisselspanningsnetwerk, zelfs als deze niet verbonden is met het gelijkspanningsnetwerk. Daarom wordt er onderzocht of de MMC reactief vermogen en LVRT kan leveren. De observatie was dat, als de MMC de LVRT vereisten van het netwerk volgt, de MMC balanceringsproblemen heeft. Deze hebben effect op de operatie van de omzetter en kunnen tot loskoppeling leiden. Dit probleem werd opgelost door een speciale fase-tak en fase-arm balanceringscontroller te ontwerpen, welke eenvoudig geïmplementeerd kan worden en ervoor zorgt dat de MMC gebalanceerd blijft. Hoe de controllers afgestemd moet worden, wordt gepresenteerd en het effect van de controllers samen, is experimenteel geverifieerd. Hierbij is rekening gehouden met de niet-lineariteit van de modulatie en de vertragingen in het systeem.

Onderdrukking van hoge orde harmonische
Een andere belangrijke toepassing van een MMC zou een APF kunnen zijn. Hierbij zorgt de MMC voor de onderdrukking van hoge orde harmonische veroorzaakt door niet-lineaire belasting van het wisselspanningsnetwerk. Recente net-codes vereisen het filteren van hoge orde harmonische stroom en spanning. Dit proefschrift stelt een selectieve detectie en beheersingsmethode van harmonische voor. Gebruikmakend van de grote bandbreedte van de MMC, terwijl een lage effectieve schakelingfrequentie van sub-modules wordt gehanteerd, werd bewezen dat harmonische tot de 13^e orde effectief onderdrukt kunnen worden. Omdat de eliminatie van harmonische niet bewezen kan worden door simulatie met een ges-

implificeerd model zijn uitgebreide experimentele resultaten gegeven voor zowel de onderdrukking van stroom en spanning harmonische. Laatstgenoemde bewijst de effectiviteit van de voorgestelde detectie en controle methoden.

Dit proefschrift pakt de uitdaging van dc fouten aan vanuit verschillende perspectieven, waardoor het duidelijk wordt dat een meer holistische aanpak nodig is in dit soort onderzoek. Meest belangrijk, dit proefschrift biedt inzicht in het verloop van een dc fout en stelt oplossingen voor om de fout te isoleren en in bedrijf te blijven tijdens deze fout. Zelfs als deze fout betrekking heeft op het gehele of gedeeltelijke gelijkspanningsnetwerk.

Basic MMC Nomenclature

C_{sm}	Submodule capacitance
i_j	Output phase-j current
$i_{cj} = \frac{i_{uj}+i_{lj}}{2}$	Circulating current of phase-j
$i_{u,l}$	Upper, lower arm current
L_{arm}	Arm inductance
L_t	Transformer inductance
N	Number of submodules per arm
$N_{u,l}$	Number of submodules inserted in upper, lower arm
S	MMC apparent power
$v_{cj} = \frac{v_{uj}+v_{lj}}{2}$	Internal voltage of phase-j
v_{dc}	Pole-to-pole dc link voltage
$v_{dcp,n}$	Positive, negative pole-to-ground dc voltage
$v_{sj} = \frac{-v_{uj}+v_{lj}}{2}$	Output voltage of phase-j
v_{sm}	Submodule capacitor voltage
$v_{u,lj}$	Inserted upper, lower arm voltage of phase-j

1

Introduction

1.1. High Voltage Direct Current Systems

The changes in the global energy status quo and the grid penetration of a constantly increasing amount of renewable energy sources have affected the shape of the electricity grid. The distance between consumption and generation has increased significantly and it is expected to increase even more in the coming years, upgrading the role of the transmission system to a critical factor for the future. This fact is additionally corroborated by the increasing energy exchange between countries.

Many countries with a traditional energy mix, based on various forms of coal or oil, are forced by international treaties, such as the Kyoto Protocol and the Paris Agreement, as well as by regional agreements such as the 2020 Climate & Energy Package and the 2030 Climate & Energy Framework in Europe, to reduce their energy dependence on fossil fuels and introduce a more sustainable way to cover their energy needs. By creating energy pathways between countries and by interconnecting the national grids, sustainability goals can be achieved more easily and intermittency problems of renewable sources can be tackled. However, there are technological issues related to the transmission system that need to be resolved in order to materialize the vision of a transnational grid.

High-voltage ac (HVAC) electricity is preferred for transmission purposes mainly because higher voltages are easily achievable by means of a transformer, as well as electricity generation via three-phase synchronous generators is easier, cheaper and more efficient than using high-voltage dc (HVDC) converters. However, in some cases, it is not possible to use HVAC transmission technology, e.g. when networks are asynchronous or when long cables are involved. The limit in ac transmission distance is a result of voltage stability issues and the high transmission losses involved in ac lines [1]. The skin and proximity effects that exist in ac contribute to a non-uniform current distribution in conductors carrying ac, where most of the current is found in the conductor's outer layers [2]. As a result, the effective resistance of ac cables is higher than that of dc cables. Moreover, reactive power cannot be avoided when using alternating current and reactive power compensation is necessary at different points of the ac lines, especially for long distances. Consequently, HVDC appears to be an appealing and economically viable solution that allows the large scale grid expansion and the bulk power transfer from the renewable energy production sites to the big load consumption centers.

To utilize dc, a conversion step is necessary. The two main HVDC converter technologies are Current-Source Converters (CSC) and Voltage-Source Converters (VSC) [3]. A CSC station can be either Line-Commutated (LCC-CSC) or Forced-Commutated (FC-CSC) [4]. LCC-CSC, often referred to as HVDC Classic, is a mature technology that is used in most of the HVDC systems in operation nowadays. Most HVDC Classic transmission systems have distances between 180 and 1000 km, with voltages between 500 kV and 1000 kV and power ratings between 500 and 2500 MW [5, 6]. Moreover, power ratings up to 7.2 GW at 1600 kV are possible using Ultra-High Voltage direct current (UHVDC) technology [7].

One of the main advantages is that CSC stations are able to handle dc contingencies, as they do not allow the ac grid to feed the dc side fault. However, the fact that the HVDC Classic is line-commutated means it can control its active power flow but it always consumes reactive power. Depending on the thyristors firing angle, the reactive power compensation can be circa 50-60% of the converter rated power [8]. Their low switching frequency results in low converter switching losses, while the required filter size is high. Hence, HVDC Classic transmission systems require strong ac networks and capacitor banks capable of providing

the necessary reactive power, for proper converter operation, making LCC-HVDC not suitable for connection of offshore wind farms to the grid. As a consequence, research has recently focused on voltage-source converters (VSC) for the connection of weak ac grids, as well as for the expansion of point-to-point HVDC connections into grids [3].

VSC-HVDC converters utilize mostly insulated gate bipolar transistors (IGBT), which are controlled by pulse width modulation (PWM) controllers. The use of fully controllable switches allows the independent control of the active and reactive power, as well as control of the dc and ac side voltage level. In this way, the power quality is enhanced and the realization of multi-terminal HVDC networks is theoretically easier, as low coordination among the VSCs is required [3].

Regarding VSC technology, the two-level configuration has been widely used in the past. However, since 2003 when the multi-level modular converter (MMC) concept was introduced [9], all the main manufacturers have adjusted their production lines accordingly. The multi-level concept is easily adjustable facilitating transmission of high power at high voltage levels, while at the same time synthesising a high-quality sinusoidal voltage waveform by incrementally switching a high number of voltage levels, thus lowering the filtering requirements. Table 1.1 indicates the trend for MMC employment in VSC-HVDC installations for power transmission and grid connection of OWFs. However, as MMC is used in more projects, more research is required on the converter's system integration aspects.

Table 1.1: Overview of selected VSC-HVDC projects.

Project Name	**Year**	**Supplier**	**Power (MW)**	**Converter**
Gotland [10]	1999	ABB	50	2-level
Murraylink [11]	2002	ABB	220	3-level
Estlink [12]	2006	ABB	350	2-level
BorWin 1 (OWF) [13]	2009	ABB	400	2-level
Trans Bay Cable [14]	2010	Siemens	400	MMC
Caprivi Link [15]	2010	ABB	300	2-level
Skagerrak 4 [16]	2014	ABB	700	MMC
BorWin 2 (OWF) [17]	2015	Siemens	800	MMC
HelWin 1 (OWF) [18]	2015	Siemens	576	MMC
HelWin 2 (OWF) [19]	2015	Siemens	690	MMC
DolWin 1 (OWF) [20]	2015	ABB	800	MMC
SylWin 1 (OWF) [21]	2015	Siemens	864	MMC
INELFE [22]	2015	Siemens	2x1000	MMC
South-West Link [23]	2016	GE	1440	MMC
DolWin 2 (OWF) [24]	2017	ABB	916	MMC
NordBalt [25]	2017	ABB	800	MMC
DolWin 3 (OWF) [26]	2017–18	GE	900	MMC
BorWin 3 (OWF) [27]	2019	Siemens	900	MMC
Nemo Link [28]	2019	Siemens	1000	MMC
Cobra Link [29]	2019	Siemens	700	MMC

The MMC usually consists of three phase units. Each phase unit comprises two converter arms, each with several series-connected submodules and an arm reactor. The number of submodules per arm depends on the dc voltage rating of the HVDC grid, the semiconductors voltage rating, as well as the total energy storage need of the converter. As a result it is directly dependent on the application. Each submodule contains a number of power semiconductor devices as the switching elements which are placed according to the chosen topology. The two most commonly researched topologies are the Half-bridge and the Full-bridge, as presented in Figure 1.1. Although many different topologies have been proposed in the literature [30], these two can be considered generic. Apart from the semiconductors, a capacitor, as well as auxiliary electronics and a cooling system are included in a single submodule.

The Half-bridge topology is most commonly used due to its low losses and low cost. However, as all VSC topologies, in case of a dc fault, the submodule can only be bypassed via the antiparallel diode of the lower switch or via the thyristor and mechanical switch connected in parallel. As a result, it cannot contribute to the reduction or even blocking of the fault current. The Full-bridge submodule, which has been extensively used in cascaded converters for different applications [31], is an alternative to improve the dc fault blocking capability of the MMC station. This stems from the submodules capability to provide a counter voltage by directing the fault current through the capacitor, preventing the fault current flowing from the ac to the dc side [32].

Unlike other VSC topologies, the main advantage of this converter design is its modularity, which means that the conversion levels can simply be increased by connecting more submodules in series. Hence, the submodules are the elementary building blocks of the MMC system. In fact, the presence of N capacitors in one arm means that N respective voltage levels are available to synthetize the desired $N+1$-level ac voltage. Therefore, the ac voltage created has a shape close to a perfect sinusoidal and the filtering needs are mini-

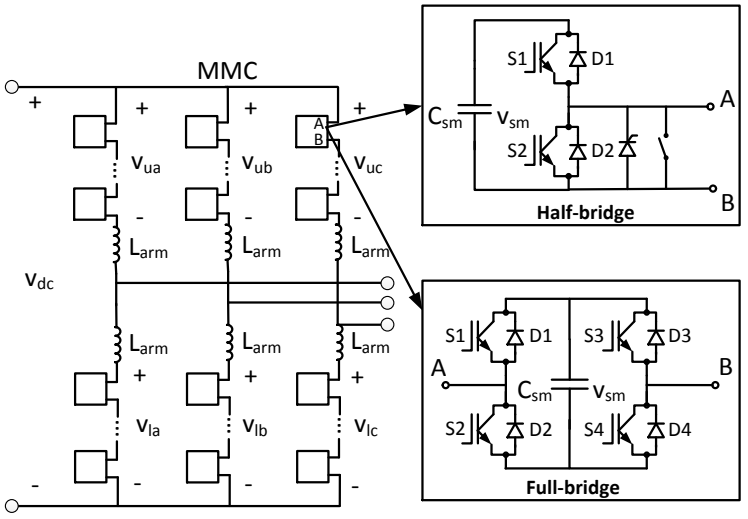

Figure 1.1: MMC structure and two types of submodule topologies.

mum. At the same time, the voltage derivative is very low, resulting in less stresses on the switches and on the arm reactor and less produced EMI.

Because of the presence of capacitors with controllable voltage levels in the arms, the MMC offers more degrees of control freedom compared to other converters. However, at the same time, its control becomes a complex task requiring both outer controllers, which are responsible for the control of parameters regarding the MMC interaction with the ac and dc side, as well as internal controllers, responsible for the energy balancing of the legs and arms of the converter and the handling of the circulating current to minimize the MMC losses and improve its harmonic content [32, 33].

1.2. Motivation

With the growth of offshore wind, the need for expansion of the existing offshore point-to-point connections arises, including transnational links to support an increase in cross-border electricity exchange. This expansion is also a pre-requisite for market integration towards a single, more efficient European electricity market, leading to cost price and emission reduction. The benefits of more interconnection capacity between North Sea countries, as well as coordinated offshore grid development, have been identified in several grid studies[1]. By building interconnections between offshore wind farms in different countries, the offshore electrical infrastructure can be used both for wind power export and for cross-border trade. The average load of dedicated offshore wind grid infrastructure, which is typically 40% to 50%, offers room for additional electricity transport and thereby more efficient asset utilization. Electricity can be traded to neighboring countries via the same infrastructure and for the offshore wind farms there is a redundant connection to shore. This helps to lower average electricity prices in Europe and could lead to a higher turnover of the wind farm and lower risk of power loss, reducing the necessary government support for offshore wind.

The electrical infrastructure connecting offshore wind farms to the onshore grid represents a large share of the total costs of offshore wind and a significant risk in terms of insurance claims [34]. Due to the increasing wind farm size and distance to shore, the technical and economic limits of existing solutions for offshore connections will be reached in the near future. In some cases, cost savings can be obtained in the design and realization phase from combining cabling routes and reducing the number of offshore platforms and converter stations [3]. To obtain an optimized design and efficient utilization of the wind farm connections, an integral approach is needed focusing beyond the boundaries of a single wind farm.

The TKI “Synergies at Sea" research project and more specifically the sub-project “Interconnector" studied the feasibility of a specific case, namely combining two offshore wind farms with an interconnection between the UK and the Netherlands. The feasibility study focused on economic, regulatory and technical aspects. The main conclusion is that ’integrated solutions’, where wind farms are connected to an interconnector are technically feasible, and in particular cases lead to significant societal benefits if regulatory issues can be overcome. All integrated solutions were compared with the respective ’stand-alone solutions’ in which the same amount of offshore wind is installed, but connected directly to the land network, and not to the interconnector. In total 17 scenarios were initially defined and

[1]Examples include OffshoreGrid: www.offshoregrid.eu, NorthSeaGrid: www.northseagrid.info and North Sea Transnational Grid (NSTG): www.nstg-project.nl.

evaluated. The feasibility also included a comparison between different rated capacities of the different sections of the offshore transmission system, considering transmission losses, reliability and effects on the connected markets. The aim was to determine the possible grid topologies and applicable technologies and secondly, to estimate the involved costs and assess the performance.

For the grid design, different combinations of HVDC and HVAC technologies in a multi-terminal topology were considered. From the long list of technical scenarios, two were identified as most favorable to be used as starting point for the system design. More specifically, the two scenarios which were found to be substantially beneficial for private investors as well as for society are presented in Figure 1.2:

1. Scenario 1: consisting of an HVDC connection between a 900 MW wind farm in the UK and the Dutch grid, and
2. Scenario 2: consisting of an HVDC connection between a 900 MW UK wind farm and a 900 MW Dutch wind farm.

Both scenarios apply HVDC technology in a multi-terminal configuration (MTDC). It has to be noted that in the specific case study, HVDC technology is required for at least one section of the interconnection, since the Dutch and UK grids are not synchronized.

Up to now, there are only 9 offshore HVDC point-to-point connections in place, under construction or commissioned, as shown in Table 1.1, most of which use the MMC technology. As a result, the MMC was selected as the building block of the HVDC grid.

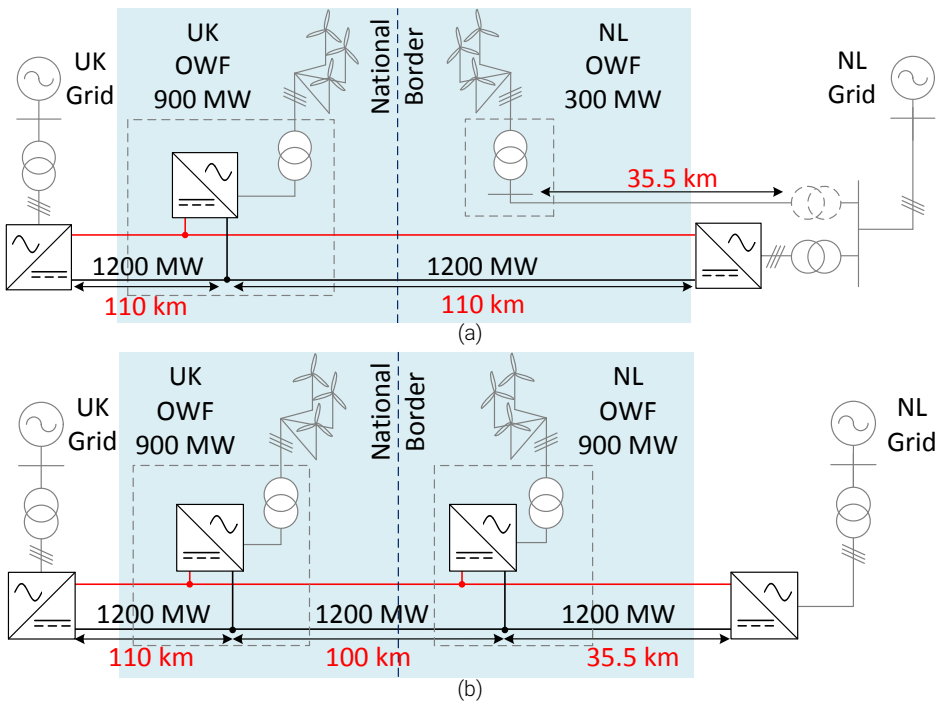

Figure 1.2: Schematics of (a) Schenario 1 and (b) Scenario 2.

1.3. Problem Definition

Although small HVDC projects have been proven to be technically feasible [35, 36], a number of technical challenges were identified as crucial for further research. More specifically, reliability and the risks associated with the protection of HVDC projects affect their economic feasibility. Among the sources of contingencies in an HVDC grid, faults on the dc lines are characterized as extremely challenging for HVDC grids [32, 37]. Due to the absence of a natural zero-crossing of dc current, the isolation of a fault on a dc line is more difficult than in case of faults in ac grids [38]. Very fast transients and high overcurrents, occurring in case of dc faults, are likely to damage the involved equipment and are more difficult to isolate [39].

Up to now, protection in point-to-point connections has been achieved through ac breakers [1]. Although this method might be sufficient for small grids, an important restriction stems from the power level limit the TSOs set for disconnecting at once in case there is a fault in the system. More specifically, National Grid determines 1320 MW as the normal limit, whereas 1800 MW can be considered as the limit for infrequent disconnections [40]. As a result, this method cannot be applied in high power grids, since it requires that the whole system is disconnected, in case of a dc fault in one line, before operation can be anew resumed. Therefore, as the trend is moving towards the realization of HVDC grids, selectivity in the fault detection and isolation is necessary, which can be realized by the development of dc breakers. Although several dc breaker designs have been theoretically proposed, cost of protection, which stems from the inefficient design of the different paths involved in the breaking process, still poses a significant challenge towards HVDC grids [41].

Apart from the dc breakers, different approaches on the MMC submodule design are able to contribute to the fault isolation, such as the Full-bridge submodule. In this case, the responsibility of the fault isolation is taken by the converter stations. However, the lack of standardization in the response of MMC stations to dc faults means that until now there is no fixed procedure to alleviate the fault impact on the converters and allow a fast post-fault recovery of the system. As a result, step-by-step fault-ride-through approaches are needed. To achieve that, the way the dc faults affect the MMC operation needs to be first investigated in depth, as the fast transients that develop during a contingency are likely to disturb the operation of the converters even after the fault is cleared.

Finally, during the dc fault ride-through operation or even after the successful fault isolation, it is important to consider the operation and controllability of the MMC with respect to the ac grid side. Until now, studies dealing with dc faults have only focussed on dc fault detection, isolation and recovery, without considering the control interaction of the MMC station with the ac side. If the MMC stations remain inactive at the disconnected terminals, it means that a big part of the 'healthy' grid assets remains unused compromising the operability of the grid. MMC stations are an essential and costly part of the grid with many degrees of control freedom, which can contribute to the support of the ac grid, either by providing reactive power support and ac voltage/frequency control or as an active filter for harmonic compensation. As a result, it is important to study the ancillary services the MMC stations can provide during a dc fault to maximize the utilization of the grid assets. If a converter station is 'isolated' from the rest of the dc grid either by means of a breaker or by means of control during a fault on the connected line, this station should be able to continue operation and provide support to the connected ac grid for as long as the line is repaired, until power flow can be restored.

1.4. Objectives & Research Questions

The main research objective of this thesis is to investigate different ways to protect an HVDC grid from dc faults according to the design choice of the MMC stations used at the grid terminals. DC faults and the lack of a protection system design are considered the main technical barrier that inhibits the realization of highly meshed HVDC grids. To this end, optimization of the dc breaker design on one hand and innovative dc fault ride-through techniques on the other hand are equally important. Moreover, new control techniques are to be obtained that can increase the uptime of the MMC stations, even during faults on the HVDC side, allowing them to provide ancillary services to their respective ac grids.

Considering these aspects, the main research question of this dissertation is:

How to protect an MMC-based multiterminal HVDC grid from dc faults without compromising the converter's ability to support the ac grid?

To answer the question above, the following key questions are considered:

1. *What are the main characteristics of dc faults?*
2. *What are the requirements for dc breaker design optimization?*
3. *What are the steps to ride through a dc fault without the use of dc breakers?*
4. *What ancillary services can the MMC provide during dc faults?*
5. *What are the MMC control requirements to support the ac grid during dc faults?*

1.5. Contributions

The main contributions of this thesis are:

1. Proposal of a novel dc breaker configuration concept with the aim to decrease the cost of necessary protection equipment;
2. Development of step-by-step dc fault ride-through techniques in multi-terminal HVDC grids using Full-bridge MMC;
3. Investigation of the operational capability of the MMC to support the ac grid during dc faults and design of a respective control structure.

1.6. Thesis Layout

This thesis is divided in three main parts: (i) DC Fault Analysis, (ii) DC Fault Ride-through, (iii) AC Grid Support during DC Faults. Figure 1.3 shows the parts of the HVDC grid on which each Chapter focusses, while the thesis layout is shown in Figure 1.4.

Part I. DC Fault Analysis
Chapter 2 answers the first key question by giving a mathematical analysis of dc faults in HVDC grids, identifying their main characteristics and evaluating their impact on the MMC operation using a developed experimental set-up. The set-up represents a scaled-down version of a point-to-point Half-bridge MMC-based HVDC connection. Different grid topologies are implemented and compared on their response to different types of performed dc faults.

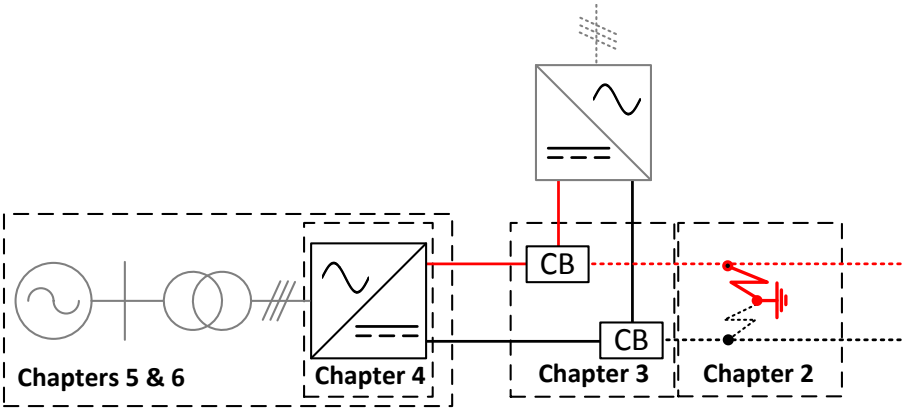

Figure 1.3: Chapters' focus points within an HVDC network.

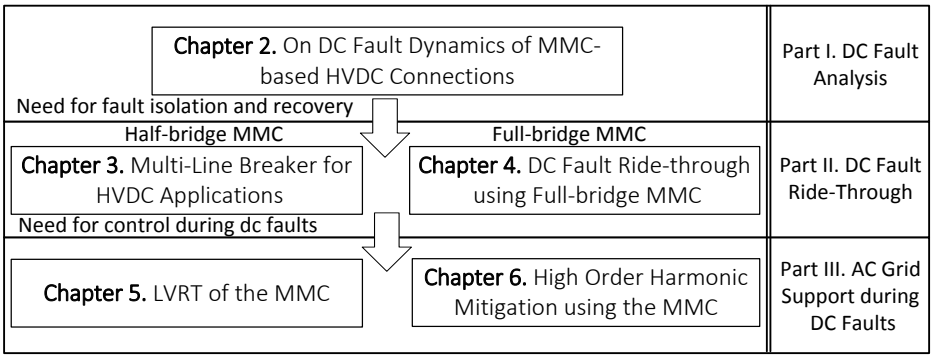

Figure 1.4: Thesis layout and interdependencies between Chapters.

Part II. DC Fault Ride-through

In general, two main dc fault protection approaches in HVDC grids can be identified: (i) Half-bridge MMC with dc breakers in both ends of each dc connection line and (ii) Full-bridge MMC with mechanical disconnectors on the dc side for faulty line isolation. This part of the thesis follows the same classification trying to address the two approaches in each of the related Chapters.

Chapter 3 addresses the second key question. In this Chapter, a novel concept of dc circuit breaker (CB) configuration, named the Multi-Line Breaker (MLB) is proposed with the aim to reduce the protection system cost and improve the dynamic fault response of an HVDC grid. The hardware and control implementation of the MLB is compared to the Load Commutation Switch - Mechanical Breaker (LCS-MB), as proposed by ABB under the name of 'proactive hybrid breaker'. Furthermore, the integration and the performance of the MLB in an HVDC grid are evaluated and compared to the LCS-MB breaker.

Chapter 4 covers the third key question. Considering the use of Full-bridge MMC, a dc fault ride-through technique is proposed and evaluated in HVDC grids. A controller is imple-

mented to bring the dc current to zero without tripping the converter, taking into account the characteristics of the submodule design.

Part III. AC Grid Support during DC Faults
During and after a dc fault is cleared, the MMC stations, depending on the submodule design (Half-bridge or Full-bridge), should be able to provide ac grid support. To this end, Chapters 5 and 6 deal with key questions 4 and 5.

Chapter 5 addresses the problem of internal balancing of the MMC while providing reactive power support to the respective ac grid. A generic control method is proposed, which can be implemented with adaptations in both Half-bridge and Full-bridge MMC.

More specifically, in case of Half-bridge MMC, the station should be able to operate as STATCOM once the dc line is disconnected from the converter station. The effectiveness of the method is proven experimentally using a Half-bridge based MMC prototype in an experimental set-up, while providing low-voltage-ride-through (LVRT) capability to the system. In this case, the method is evaluated using Matlab/Simulink models. In case of a Full-bridge MMC, as presented in Chapter 4, the station should be able to control the dc current to zero, while maintaining control of the reactive power during the fault and after the fault is cleared.

Chapter 6 investigates the use of a Half-bridge MMC as an active filter for the ac grid, proving the additional capabilities of an MMC even when it is disconnected from the dc grid. A harmonics detection method and a control structure for the harmonics elimination are proposed hereby. These are evaluated for both voltage and current harmonics in two different case studies and the results are experimentally validated for both cases.

Chapter 7 summarizes the results of this thesis and addresses each of the key questions independently drawing the final conclusions. Finally, recommendations for future research are presented.

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2

On DC Fault Dynamics of MMC-based HVDC Connections

This Chapter studies the dc fault development stages and analyzes the fault dynamics in a point-to-point MMC-based dc connection. First, the effect of the dc grid configuration on the normal operation was investigated by comparing an asymmetric monopole with metallic return and a symmetric monopole. Then, the main parameters that affect the dc fault response of a grid, such as the fault type, impedance and converter blocking, were examined. Compared to previous studies which are based on simulation results, the analysis is performed hereby both in theory, deriving the equations that describe the dc fault stages, as well as using experimental results obtained in the designed laboratory set-up. The set-up consists of two MMC terminals connected to two ac sources representing independent ac grids. These terminals are connected using a simple dc link based on pi-section equivalent of dc cables. The obtained results, which verified the theoretical analysis, can be used to determine the protection function thresholds of the MMC, as well as to estimate the developed stresses on dc lines during fault conditions and define the design requirements for dc breakers.

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2

2.1. Introduction

Towards multi-terminal HVDC (MTDC) grids, dc fault handling poses a main challenge due to the fast transients and the high developing currents [1]. Unlike H-bridge-based multi-level modular converters (MMC) and line-commutated converters (LCC), Half-bridge-based MMCs are unable to block fault currents by stopping their control operation. Therefore, to improve the dc fault response of dc grids, it is necessary to understand the dc fault characteristics. Many studies have focussed on the dc fault development stages for VSC [2, 3, 4] or MMC-based grids [5, 6], as well as on the different dc fault current contributions [7, 8].

Based on the dc fault characteristics, research has been conducted on dc fault detection and isolation methods to protect the converters and facilitate the fast isolation of the dc fault [9]. Studies have presented dc breaker designs with main objectives the low on-state losses and the low total interruption times [10, 11]. Moreover, converter designs have been proposed with inherent fault blocking capability [12, 13]. Finally, dc fault ride-through techniques are necessary to integrate the solutions on each fault development stage and give a step-by-step approach for dc fault handling [14, 15].

During a dc fault, some of the most important parameters which affect the grid response [16] and have been individually studied, are: (i) the grid topology (symmetric, asymmetric) [1], (ii) the fault type [17, 18], (iii) the fault impedance [2, 4] and (iv) the converter blocking [16]. However, most of the performed studies base their results on average-model-based simulations. Independent of the detail level of a simulation, there are many assumptions made and results still need to be tested in laboratory set-ups before they can qualify for real system applications. However, laboratory tests are difficult to be implemented since they require high safety control and measures must be taken to ensure the operation post-fault.

This Chapter's main contribution is the analysis of the aforementioned dc fault parameters (i)–(iv) in an integrated approach, compared to previous studies. This is done theoretically, as well as practically, using a developed laboratory set-up, which consists of two MMC prototypes connected through a dc link, representing a point-to-point HVDC connection.

The Chapter is structured as follows: Section 2.2 presents a theoretical analysis of the dc fault development stages. The laboratory set-up is presented in Section 2.3. Section 2.4 shows the results of normal operation in the connection, where the controllers are tested and power is being transferred between the two terminals for two dc grid topologies, namely asymmetric monopole with metallic return and symmetric monopole. The latter is further used for the dc fault analysis presented in Section 2.5. A pole-to-mid-point and a pole-to-pole dc fault are applied and two dc fault resistance levels are used to study their effect. Moreover, a comparison is made between the response of an MMC which keeps switching and an MMC which stops switching during the fault. Finally, Section 2.6 provides the main conclusions drawn from the performed tests.

2.2. DC Fault Dynamics

There are two main types of dc faults, i.e. (i) pole-to-ground dc faults and (ii) pole-to-pole dc faults. During a fault, MMCs can either stop switching for their protection or maintain it to allow faster recovery in case of temporary faults, as long as their protection is not at stake. In any case, the dc fault currents develop in three stages. Hereby a point-to-point connection is used as a reference for the analysis, as presented in Fig. 2.1(a).

During the first stage, the dc cable capacitance is discharged through the fault and the dc fault current only circulates through the dc ground path to the dc fault point. Approximating a

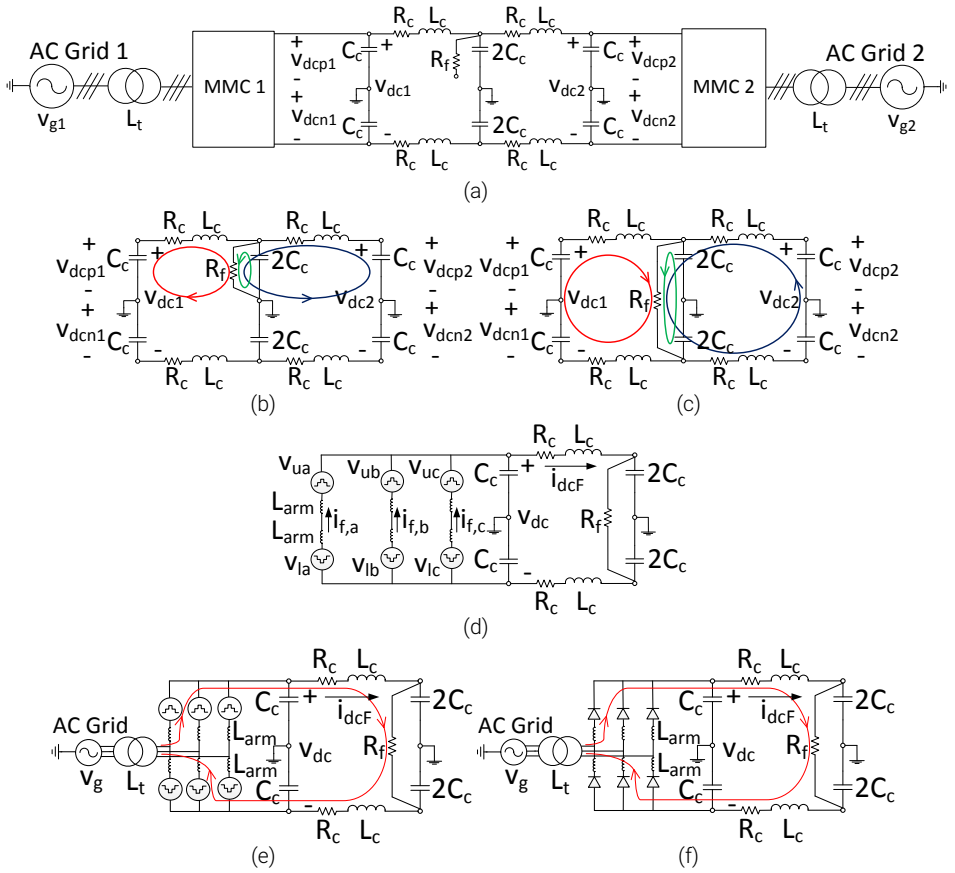


Figure 2.1: DC fault stages in a point-to-point dc connection with symmetric monopolar configuration as shown in (a): Stage 1: Capacitor discharge in case of (b) pole-to-ground and (c) pole-to-pole dc fault. Stage 2 (d): MMC submodule capacitor discharge through the fault. Stage 3: AC grid fault contribution in case switching (e) continues and (f) is blocked (uncontrollable diode conduction).

dc line using a pi-section equivalent, the circuit explaining this stage is presented in Fig. 2.1(b) for pole-to-ground fault and Fig. 2.1(c) for pole-to-pole fault. First, the capacitors at the point of the fault will get discharged through the fault resistance (indicated by green circle). As soon as the fault starts, the pole voltage v_{dcp} (pole-to-ground fault case) or the whole v_{dc} (pole-to-pole fault case), at the fault point, will be applied across the resistance R_f and the voltage will be estimated by:

$$v_{dcp} = -2R_f C_c \frac{dv_{dcp}}{dt} \tag{2.1}$$

$$v_{dc} = -R_f C_c \frac{dv_{dc}}{dt} \tag{2.2}$$

The dc fault current resulting from the dc capacitance discharge on either side of the dc

fault point (indicated by red and blue circles) can be estimated by the following equations, i.e. (2.3) for pole-to-ground and (2.4) for pole-to-pole dc faults:

$$L_c C_c \frac{d^2 v_{dcp}}{dt^2} + (R_c + R_f) C_c \frac{d v_{dcp}}{dt} + v_{dcp} = 0 \tag{2.3}$$

$$L_c C_c \frac{d^2 v_{dc}}{dt^2} + (2R_c + R_f) \frac{C_c}{2} \frac{d v_{dc}}{dt} + v_{dc} = 0 \tag{2.4}$$

In case of a pole-to-ground fault while the 'faulty' pole capacitors get discharged, the 'healthy' pole cable capacitance gets charged by the fault current until it reaches the nominal dc link voltage and operation can continue. On the contrary, the pole-to-pole fault is more severe and all dc link capacitances get discharged through the fault. Therefore, the analysis hereafter is focussed on pole-to-pole dc faults.

As soon as there is a voltage difference between sum of the voltages of the inserted MMC submodule capacitors and the dc side voltage ($(v_u + v_l) > v_{dc}$), the second stage begins and takes place along with the first stage. In the second stage, the fault current starts circulating through the MMC stations and thus, the submodule capacitors, when inserted, they discharge through the fault. In this stage, the submodules may block their operation leading to uncontrolled diode conduction or keep switching if no protection is violated. The natural response of the grid to the imposed low dc voltage generates high uncontrolled currents through the converter legs. Therefore, even if switching is taking place, the active/reactive power or dc voltage control is not possible. This stage is described by Fig. 2.1(d) and equations (2.5)-(2.8) describe the dynamics for phase-a:

$$u_{dc} - 2L_{arm} \frac{d i_{f,a}}{dt} - (v_{ua} + v_{la}) = 0 \tag{2.5}$$

$$2L_c \frac{d i_{dcF,a}}{dt} + (2R_c + R_f) i_{dcF,a} - v_{dc} = 0 \tag{2.6}$$

$$-\frac{C_c}{2} \frac{d v_{dc}}{dt} - i_{dcF,a} + i_{f,a} = 0 \tag{2.7}$$

$$i_{f,a} = -\frac{C_{sm}}{N} \frac{d(v_{ua} + v_{la})}{dt} \tag{2.8}$$

where $i_{dcF,a}$ is the contribution of phase a to fault current, while $i_{f,a}$ is the fault current circulating through phase leg a. In the third stage, the ac grid contributes to the fault current until a new steady-state is reached which primarily depends on the ac grid voltage level and the fault impedance. In case protection is triggered, the MMC acts as a diode-bridge rectifier with $v_u = 0$ and $v_l = 0$, whereas in case the switching is maintained, each arm continues to act as a voltage source which also reaches a new steady-state. Fig. 2.1(e)-(f) show the respective circuits and equations (9)-(12) describe this stage showing the contribution of v_{a-b}, for the time this is greater than the other two line-line voltages. In practice, as this is a three-phase system, there is commutation between the three phases depending on their magnitude at each moment of operation. The equations for the contributions of the other line-to-line voltages can be similarly obtained. Moreover, (12) is only valid when the switching operation of the MMC is maintained and does not hold for the case of uncontrolled diode operation. It has to be noted that in this case, it is assumed that the ac grid ground is isolated from the dc ground and there is no circulation of fault current through the ground path. This

assumption is made to match the experimental set-up which will be explained in Section III.

$$2(L_{arm}+L_t)\frac{di_{f,a-b}}{dt}+(v_{ua}+v_{lb})+v_{a-b}-v_{dc}=0 \tag{2.9}$$

$$2L_c\frac{di_{dcF}}{dt}+(2R_c+R_f)i_{dcF}-v_{dc}=0 \tag{2.10}$$

$$-\frac{C_c}{2}\frac{dv_{dc}}{dt}-i_{dcF}+i_{f,a-b}=0 \tag{2.11}$$

$$i_{f,a-b}=-\frac{C_{sm}}{(N_{ua}+N_{lb})}\frac{d(v_{ua}+v_{lb})}{dt} \tag{2.12}$$

where $i_{f,a-b}$ is the current that circulate through phase arm a and b, while v_{a-b} is the phase-to-phase voltage of the ac grid.

2.3. Hardware Implementation

2.3.1. MMC set-up

To verify the dc fault response of a point-to-point connection and test different operation modes of the MMC, two identical scaled-down MMC set-ups were built in the laboratory. Fig. 2.2(a) shows the MMC schematic, the central controller and measurement points, while Fig. 2.3(a) shows the laboratory prototype. As this study focusses on the dynamic performance of a dc connection between MMC converters during fault cases, the number of submodules does not affect the obtained results. In fact, as explained in Section II, the main parameters that affect the dynamic behavior of the system during the fault are the dc link and ac voltage rating, as well as the fault impedance and the employed arm inductors. Therefore, the developed set-up can be safely assumed to give a good overview of fault operation.

Each MMC set-up consists of:

- a 5V power supply to power the submodule boards;
- a Star-Delta transformer rated at 2.5 kVA for galvanic isolation with input of 3 x 230V and output of 3 x 400 V;
- an AC power supply (California Instruments MX-30);
- a LEM measurement box consisting of voltage transducers (LV 25-P) and current sensors (LA 25-P) with bandwidth of DC-200 kHz for measuring arm currents, DC voltage, input dc current and output voltage;
- two DS5101 interface cards for generating and sending PWM signals to the boards and DS4004 interface cards for capacitor voltage and temperature measurements;
- a DS2004 analogue to digital measurement board for measuring the signals (arm currents, ac and dc voltages and currents) from the LEM boxes with resolution frequency of 50 ns and 16 multiplexed channels;
- a PC equipped with dSPACE and Control Desk interface.

The submodule, as shown in Fig. 2.3(b), has a three-phase IPM rated at 600 V/15 A with thermal sensors. The design of the board includes capacitor voltage measurement along with overcurrent, overvoltage and overtemperature protection.

All the logic circuits are implemented in a Xilinx XC95144XL CPLD with an input clock of 35 MHz. The CPLD receives the PWM signals from the dSPACE simulator (one PWM input for each of the IPM legs) and introduces the required 1.25 us blanking time. After the

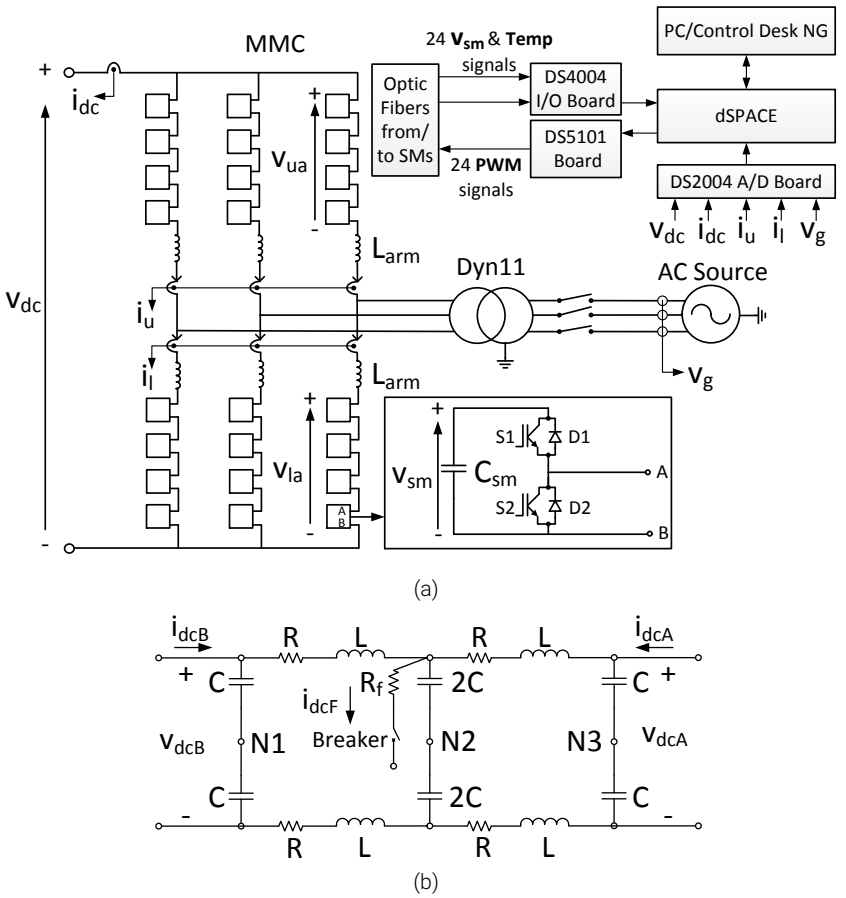


Figure 2.2: (a) MMC prototype and (b) DC link schematic.

conditioning of the PWM, six PWM signals are generated, one for each switch in the three legs. The operation status is signalled by two LEDs. The CPLD also receives an enable/reset signal from dSPACE and a fault signal which inhibits the generation of PWM signals in case one of the protection conditions is violated. Optic fibers were used for the communication between the dSPACE simulator and the submodules. Additionally, the control sampling frequency used was 10 kHz, while downsampling of 10 was necessary on the dSPACE Control Desk to depict the experimental graphs, due to memory limitations.

2.3.2. Point-to-point dc connection

To evaluate the performance of the MMC within a grid, a point-to-point dc connection was made between the two identical MMC set-ups. Two pi-sections with lumped elements were used for each pole to resemble the dc lines, as shown in Fig. 2.2(b). In fact, the lumped elements inductance and capacitance are chosen to represent an HVDC line of 20 km length

(a) (b)

Figure 2.3: (a) Laboratory prototype of MMC; (b) Submodule.

(0.2 mH/km and 0.22 uF/km respectively). The capacitors C are used to model the line susceptance, as parts of the pi-model and are not necessary for the MMC operation. To evaluate the dc fault response of the system, a 'fault' path was used consisting of an ABB breaker S201-C4 in series with a resistor resembling the fault resistance. The fault was always applied at the middle of the dc link. Depending on the connection of the 'fault' path, it was possible to perform both pole-to-pole faults as well as pole-to-mid-point dc faults. Once the point-to-point connection had been energized and control operation was stable, the fault was initiated by turning on the breaker and thus, creating a parallel path to the 2C capacitors. The fault was stopped by turning off the breaker. An overview of the complete set-up can be seen in Fig. 2.4. The MMC specifications along with the dc link parameters are summarized in Table 6.1.

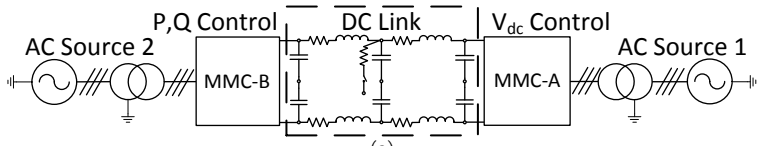
2.3.3. Control Model

In the laboratory set-up both MMCs use the same control architecture as presented in Fig. 2.5. The difference in the control strategy is that MMC-A is using V_{dc} control to provide a reference for i_d, while MMC-B is providing the reference through P_{ac} control. The outer controllers are tuned as presented in [20], while the circulating current control is tuned as presented in [21]. Additionally, Nearest Level Control (NLC) is used to provide the number of submodules that need to be inserted per arm at each switching instant. The main idea behind NLC is to approximate the reference signal with the nearest output voltage level. More specifically, the number of submodules to be inserted on each arm is determined by the following equations:

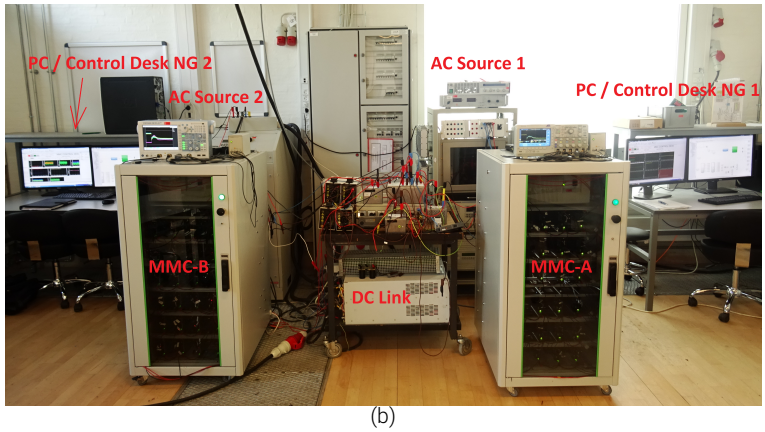
$$N_{u,l} = round\left(N \cdot \left(\frac{v^*_{u,l}}{v_{dc,rated}}\right)\right) \tag{2.13}$$

where round(x) function approximates x to the closest integer.

Once N_u and N_l for each phase j have been calculated, a simple capacitor balancing algorithm is employed to determine the gate signals for the submodules, as presented in [22]. In practice the submodules are sorted based on their capacitor voltage level and depending



(a)



(b)

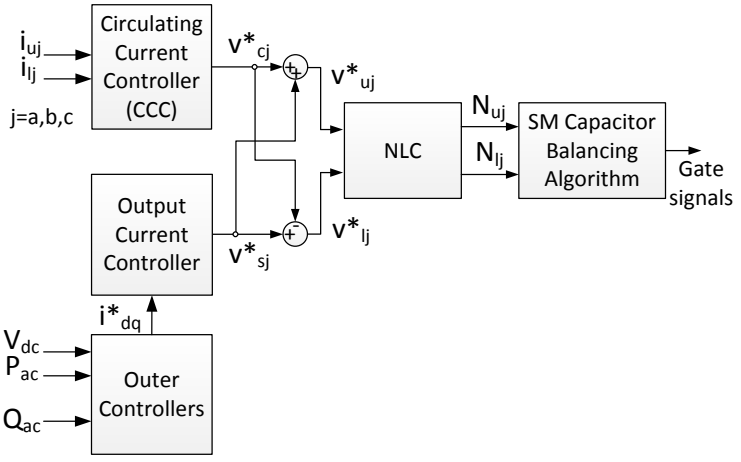
Figure 2.4: (a) Schematic and (b) laboratory implementation of complete set-up.

Table 2.1: Parameters of Experimental Setup

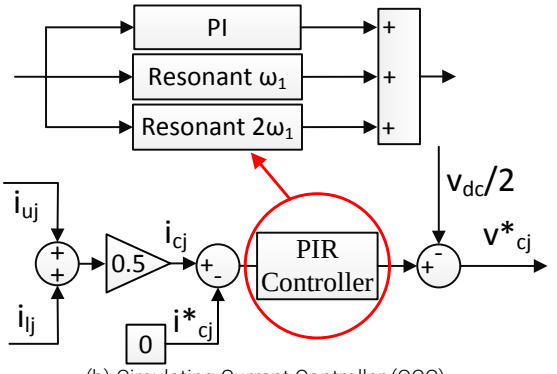
Description	Symbol	Value
MMC parameters		
Rated power (kVA)	S	2.5
Rated phase RMS voltage (V)	V_{ac}	230
Rated dc pole-to-pole voltage (V)	V_{dc}	400
Submodule's capacitance (mF)	C_{sm}	3.6
Arm inductance (mH)	L_{arm}	20
Number of submodules per arm	N	4
Transformer turns ratio	n	1:$\sqrt{3}$
DC link parameters		
Line resistance (Ω)	R	1.7
Line inductance (mH)	L	1.9
Line capacitance (uF)	C	2.2
DC fault resistance (Ω)	R_f	1.3 or 3

on the arm current direction, the submodules that need to be inserted are determined so that the capacitor voltages remain balanced in each arm. In this study, leg and arm energy balancing controllers are not used for the control of the dc and first fundamental frequency component of the circulating current [23]. As this study focusses on the fault response of

an MMC-based connection, it can be safely assumed that the energy controllers will not have an effect on it, since during a pole-to-pole dc fault, the energy of the MMC decreases, following the dc link voltage drop, faster than the time required for the energy controllers to act. Moreover, the stored energy in the MMC cannot be controlled since the tested converter uses Half-bridge submodules. As a result, the energy controllers are not affecting neither the transient nor the steady-state fault response of the connection. Additionally, the employed capacitor balancing algorithm is considered sufficient to maintain the internal balance of the converter within acceptable limits during normal operation. As a result, the structure of



(a) Overall control structure of MMC.



(b) Circulating Current Controller (CCC).

Figure 2.5: The v^*_s is determined by the outer control loop. The outer controllers are implemented as PI in the dq-frame. The d-component of the output current i is controlled by either P_{ac} or V_{dc}. The q-component is controlled by the Q_{ac}. This control structure is common in VSC converters and is presented in Fig. 12.7 of [19]. The reference of the i_{dq} is then transformed into $\alpha\beta$-reference frame and controlled using PR controller in the Output Current Controller block, as presented in Fig. 3.8 of [20]. The v^*_c is determined by the Circulating Current Controller (CCC). v^*_s and v^*_c are combined to provide the references for the upper and lower arm voltages v^*_u and v^*_l. Finally, Nearest Level Control (NLC) and a simple submodule capacitor balancing algorithm are used to determine the submodule gate signals.

the circulating current control is kept simple. The aforementioned controllers are loaded to dSPACE which in turn acts as the central control unit of the MMC.

2.4. Normal Operation

Two dc grid topologies were tested to compare their dynamic operation:

- Case (i): asymmetric monopolar with metallic return;
- Case (ii): symmetric monopolar.

In both cases the dc side was not firmly grounded, but the reference point for the voltage measurements differed. More specifically, in Case (i) the reference point was located at the return path, whereas in Case (ii) the mid-points of the capacitors (N1, N2, N3) were connected by cables creating a node, which served as the reference point.

The start-up sequence of the set-up included the controlled charging of the dc link at its nominal voltage through MMC-A control before control was enabled on the MMC-B set-up.

2.4.1. Case (i): Asymmetric Monopole with Metallic Return

In this case study, power was exchanged between the two terminals and step responses of the V_{dc}, P_{ac} and Q_{ac} were obtained to experimentally validate the MMC outer controllers. The used dc and ac voltage levels are presented in Table 2.2.

V_{dc} steps The dc link is charged at 300 V and ±10% step changes of V_{dc} are applied as shown in Fig. 2.6(a). The rise time of the V_{dc} is approximately 100 ms. For these step changes to take place, there is a respective positive or negative dc current flow from MMC-A into the dc grid (see Fig. 2.6(b)), which in turn flows into or out of MMC-B that is actively controlling its ac active and reactive power at zero. As soon as a new steady-state of the V_{dc} is reached, the current drops back to zero. The capacitor voltages are directly associated with the V_{dc} level and thus, any change in the V_{dc} is also reflected on the capacitor voltages as shown in Fig. 2.6(c)-(d).

P_{ac} steps In this case, the V_{dc} was increased to 400 V to allow for higher power exchange between the terminals. Steps of ±700 W were applied at MMC-B. The P_{ac} controller of MMC-B follows the reference with a rise time of 30 ms and the observed ripple is kept at $\pm 5\%$. However, there is a power mismatch when MMC-A delivers power to the dc grid as shown in Fig. 2.7(a), while Q_{ac} is controlled to zero (see Fig. 2.7(b)). The active power mismatch becomes apparent when comparing the P_{ac} at each MMC with the estimated power at the dc output. To estimate the P_{ac}, the dc voltage and current measurements of the MMCs are

Table 2.2: Voltage levels for normal operation tests.

Description	Symbol	Value
Phase RMS Voltage: AC Source 1 (V)	V_{ac1}	150
Phase RMS Voltage: AC Source 2 (V)	V_{ac2}	100
DC voltage for V_{dc} steps (V)	V_{dc}	300
DC voltage for P_{ac}, Q_{ac} steps (V)	V_{dc}	400

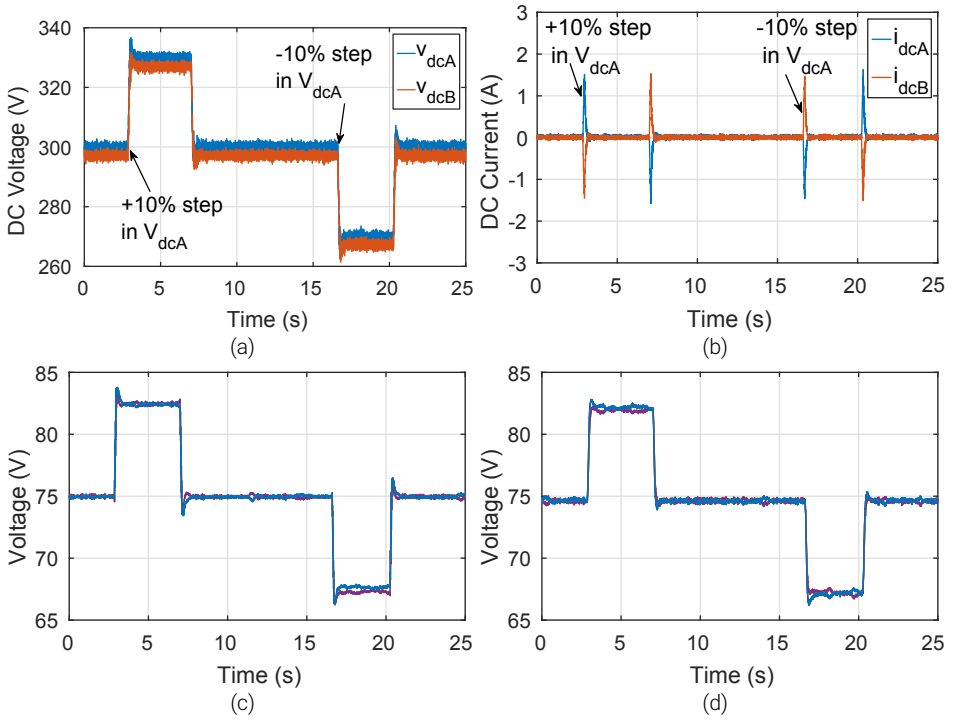


Figure 2.6: Asymmetric Monopole - V_{dc} steps: a) DC voltage, b) DC current, submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: c) MMC-A, d) MMC-B.

presented in Fig. 2.7(c)-(d). When MMC-B delivers power to ac grid 2, P_{ac} is almost equal to P_{dc} for MMC-A, whereas MMC-B has almost 500 W losses. On the other hand, when MMC-B delivers power to the dc grid, the P_{ac} levels are equal in absolute numbers and opposite as expected.

The submodule capacitor voltages on one leg of each MMC are depicted in Fig. 2.7(e)-(f). When power flow is zero, the arm voltages are maintained at the same level and the dc voltage is equally distributed among the submodule capacitors due to the balancing algorithm used. When there is power flow and depending on the direction, the upper and lower arm voltages are shifted since there is a dc component on the arm currents that charges/discharges the capacitors accordingly.

Q_{ac} steps In this case, the P_{ac} of MMC-B was controlled at 0 W at all times. Steps of ±6 A on the i_q were applied at both MMCs. The current steps result in different Q_{ac} levels, because the V_{ac} levels are different between the two MMCs. Although the P_{ac} and Q_{ac} controllers are decoupled, it was observed that when a change in the Q_{ac} took place, as shown in Fig. 2.8(b), the MMC-A would request active power (see Fig. 2.8(a)) to keep the capacitors charged and thus, keep the V_{dc} level steady. However, in this case, the active power does not appear on the dc side of the MMC-A.

When the steps are applied on MMC-B, a dc current flows from MMC-A to MMC-B as

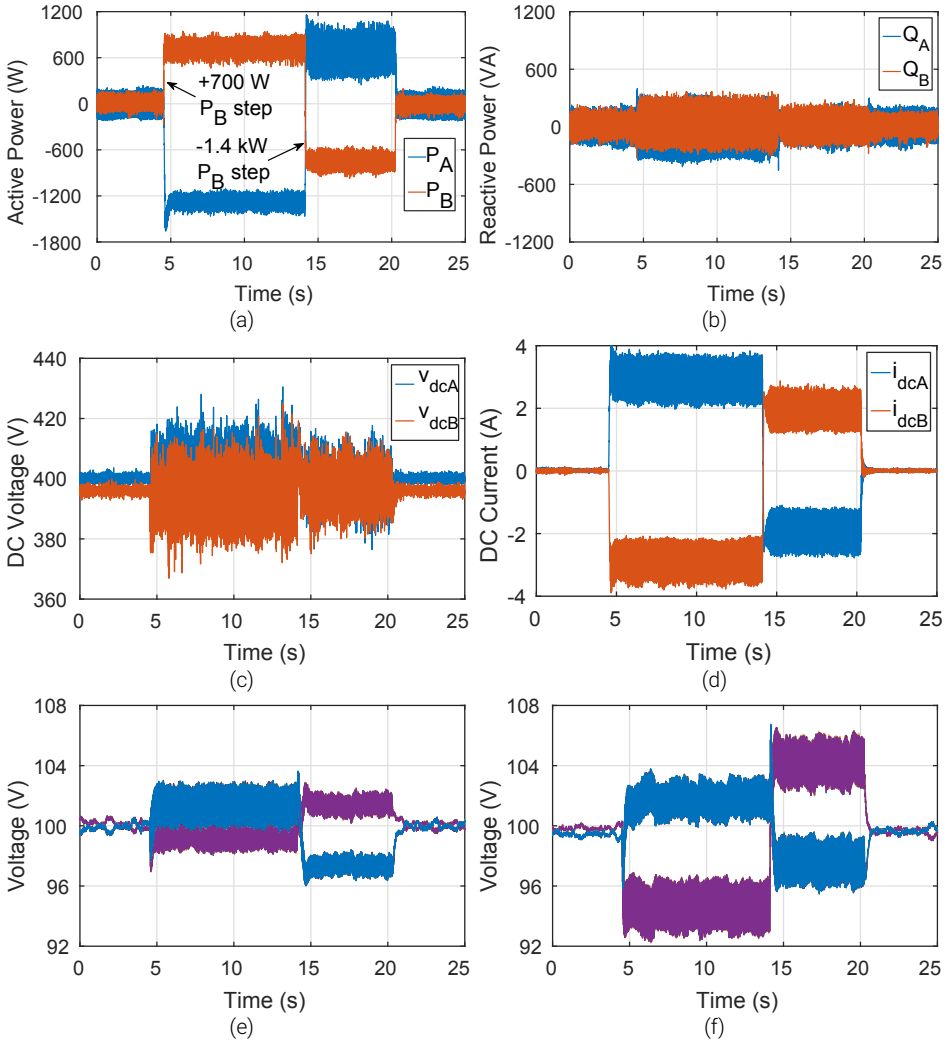


Figure 2.7: Asymmetric Monopole - P_{ac} steps: a) Active power, b) reactive power, c) DC voltage, d) DC current and submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: e) MMC-A, f) MMC-B.

shown in Fig. 2.8(d), while V_{dc} remains constant (see Fig. 2.8(c)). Active power does not appear on the ac side of MMC-B which means that the dc current circulates in the converters and the dc grid and does not depend on the reactive power flow. The dc current appears because MMC-A is responsible to provide active power to keep the capacitors of both MMCs and the dc grid charged at their nominal level. No change in the P_{ac} of MMC-B is observed because it is actively controlled to zero. Moreover, the Q_{ac} level of each converter is independent of the other station. Finally, the capacitor voltages remain at their nominal level with

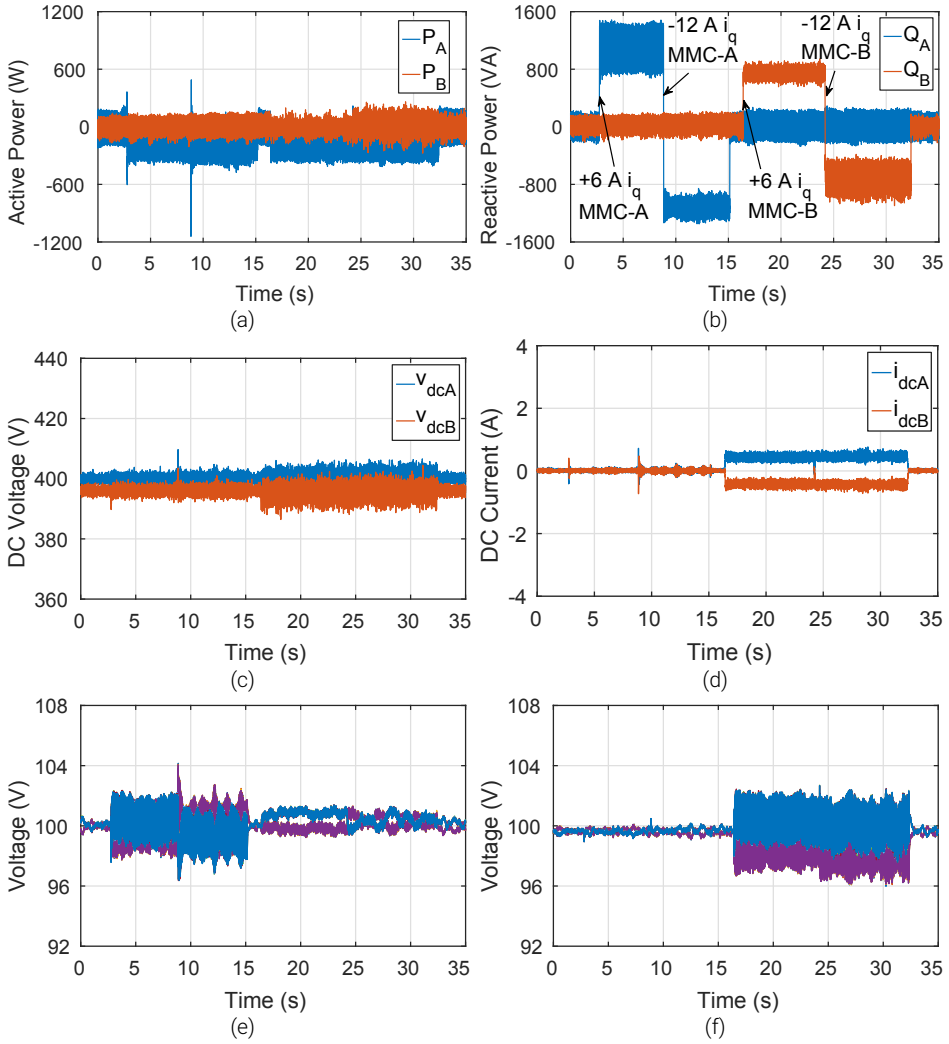


Figure 2.8: Asymmetric Monopole - Q_{ac} steps: a) Active power, b) reactive power, c) DC voltage, d) DC current and submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: e) MMC-A, f) MMC-B.

a maximum of 4% ripple, as presented in Fig. 2.8(e)-(f).

2.4.2. Case (ii): Symmetric Monopole

To allow a comparison between the two studied topologies, the V_{dc} was kept at $400\,V$. In the symmetric monopolar configuration, the voltage is split equally between two capacitors with a common mid-point used as reference point. As a result, the voltage is controlled at $\pm\,200$ V, as shown in Fig. 2.9.

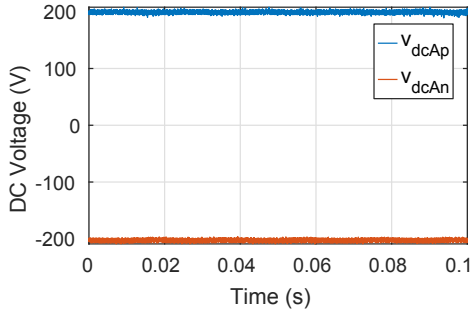


Figure 2.9: Pole DC voltage.

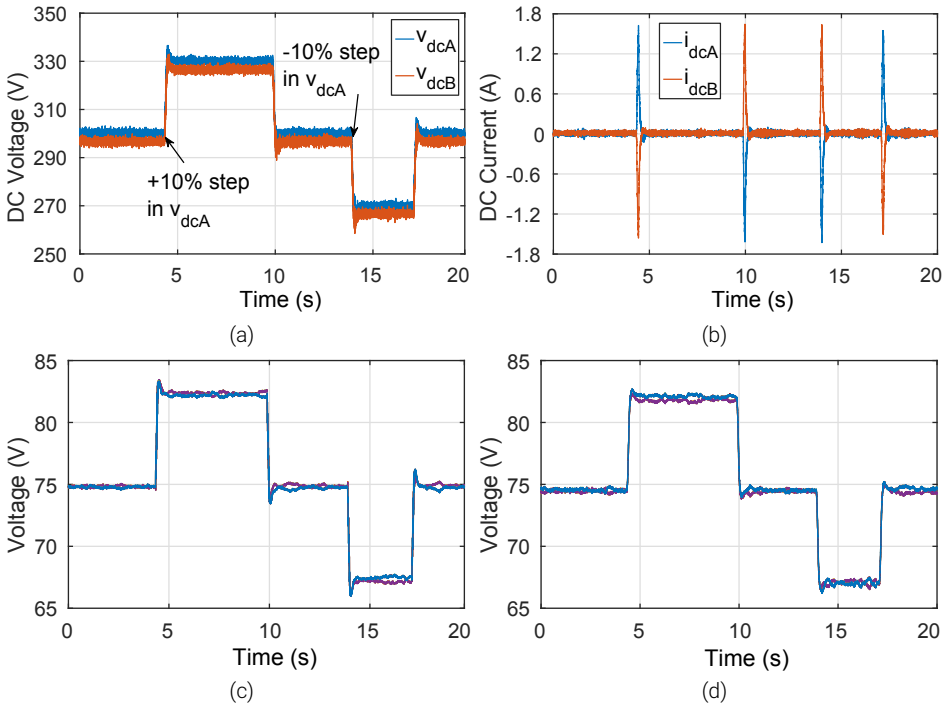


Figure 2.10: Symmetric Monopole - V_{dc} steps: a) DC voltage, b) DC current, submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: c) MMC-A, d) MMC-B.

V_{dc} steps For the dc voltage control evaluation, 300 V is used. The V_{dc} control is stable, which is evident from the dc voltage and current, which are presented in Fig. 2.10(a)-(b), while the capacitor voltages are presented for both set-ups in Fig. 2.10(c)-(d). It is observed that the capacitor voltage dynamics follow the V_{dc} control. Moreover, there is no change in the voltage dynamics between the two studied topologies and the rise time does not depend on the dc grid topology.

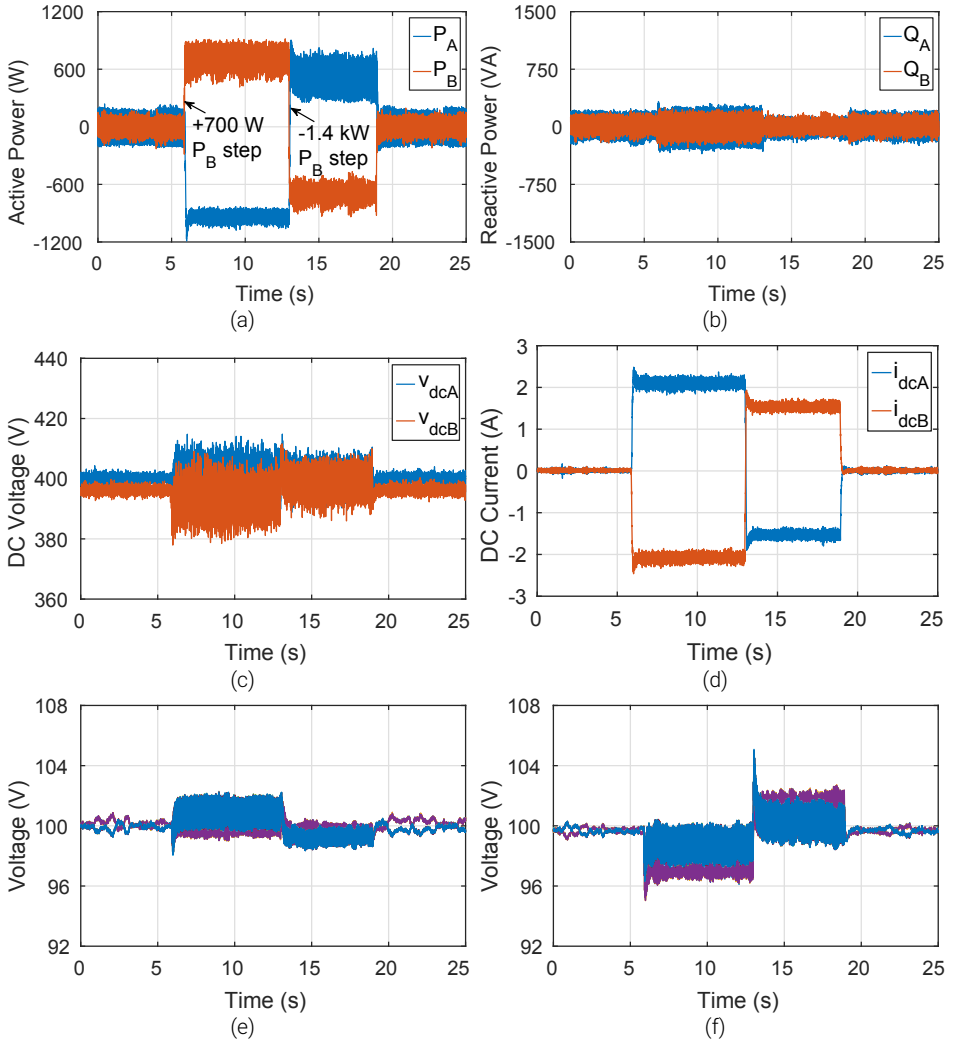


Figure 2.11: Symmetric Monopole - P_{ac} steps: a) Active power, b) reactive power, c) DC voltage, d) DC current and submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: e) MMC-A, f) MMC-B.

P_{ac} steps In order to evaluate the losses in the two MMCs, the P_{dc} is compared to the P_{ac}. The measured ac power levels and dc current and voltage are shown in Fig. 2.11(a)-(b) and Fig. 2.11(c)-(d) respectively. In this case study, the losses are approximately 80 W in inverter mode and 120 W in rectifier mode, resulting in 200 W difference between the P_{ac} levels at the ac grids. Moreover, due to the symmetry of the dc grid topology, the upper and lower arm capacitor voltages are maintained almost at the same level independent of the power flow, as seen in Fig. 2.11(e)-(f).

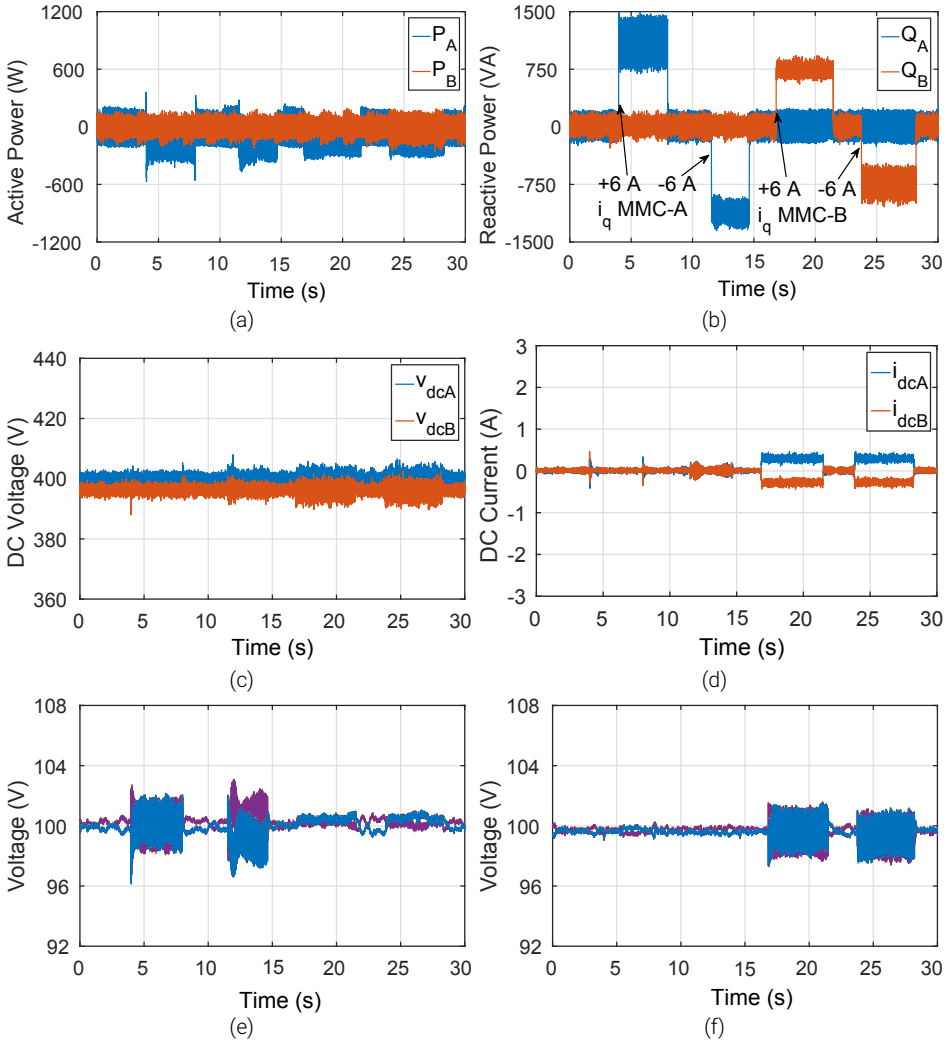


Figure 2.12: Symmetric Monopole - Q_{ac} steps: a) Active power, b) reactive power, c) DC voltage, d) DC current and submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: e) MMC-A, f) MMC-B.

Q_{ac} steps As theoretically expected, the dc grid topology does not play a role on the reactive power exchanged between the MMC and its respective ac grid. This is verified by comparing the results presented in Fig. 2.12 with the respective results of Case (i) in Fig. 2.8.

2.5. Fault Operation

The symmetric monopole was chosen and tested under dc fault conditions, as it is commonly used in VSC-HVDC connections and has shown a better dc fault response [1]. Low voltage and power levels were tested for safety reasons. The voltage levels used are shown in Table 2.3. In fact, if the pre-fault dc current value is higher or lower than zero then the dc fault current peak would be shifted higher or lower accordingly. Therefore, as the study focusses on the dc fault dynamics evaluation, which mainly depend on the converter and dc grid topology, and not on testing the set-up safety limits, all fault cases are studied at zero power flow. In this Section, four main case studies are presented to examine the effect of the dc fault type, dc fault resistance and converter tripping, namely:

- Fault case (i): Pole-to-mid-point dc fault without dc fault resistance;
- Fault case (ii): Pole-to-pole dc fault with 3 Ω dc fault resistance;
- Fault case (iii): Pole-to-pole dc fault with 1.3 Ω dc fault resistance;
- Fault case (iv): Pole-to-pole dc fault with 1.3 Ω dc fault resistance and MMC-A tripping.

Fault case (i) - Pole-to-mid-point dc fault

The dc link is charged at ±40 V. The dc fault is applied on the positive pole of the dc link at 4.1 s of the test. As expected, the positive pole is completely discharged within 0.7 ms

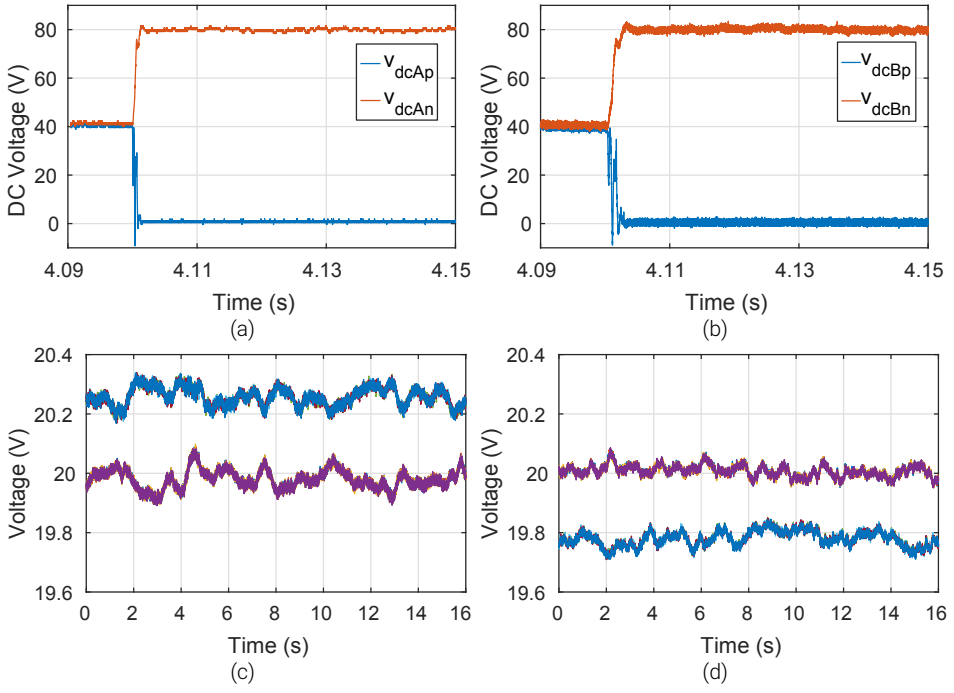


Figure 2.13: Fault case (i): DC voltage at a) MMC-A and b) MMC-B; Submodule capacitor voltage of upper (blue) and lower (purple) arms of phase-b at: c) MMC-A, d) MMC-B.

Table 2.3: Voltage levels for fault operation tests.

Description	Symbol	Value
Phase RMS Voltage: AC Source 1 (V)	V_{ac1}	40
Phase RMS Voltage: AC Source 2 (V)	V_{ac2}	40
DC voltage for Fault case (i) (V)	V_{dc}	80
DC voltage for Fault cases (ii)-(iv) (V)	V_{dc}	100

following the RLC dynamics of the dc grid, while the negative pole gets charged to the full dc link voltage, namely 80 V as shown in Figure 2.13(a)-(b). Since the fault transient is very fast, the positive pole capacitors are bypassed and the negative pole capacitors voltage reaches the nominal V_{dc} value as imposed by the MMC capacitor voltages. As a result, the V_{dc} control is maintained and operation can continue. Due to asymmetries in the dc grid resulting from the components used, the dc voltage at MMC-B is slower than at MMC-A. Because the V_{dc} reaches a new steady-state within 1 ms, no significant effect is observed on the submodule capacitor voltages in Figure 2.13(c)-(d).

Fault cases (ii)-(iv) - Pole-to-pole dc fault

Three different pole-to-pole dc fault cases are studied. The dc voltage and current for each case are presented in Figure 2.14-2.17. The three main stages, as described in Section II, can be distinguished.

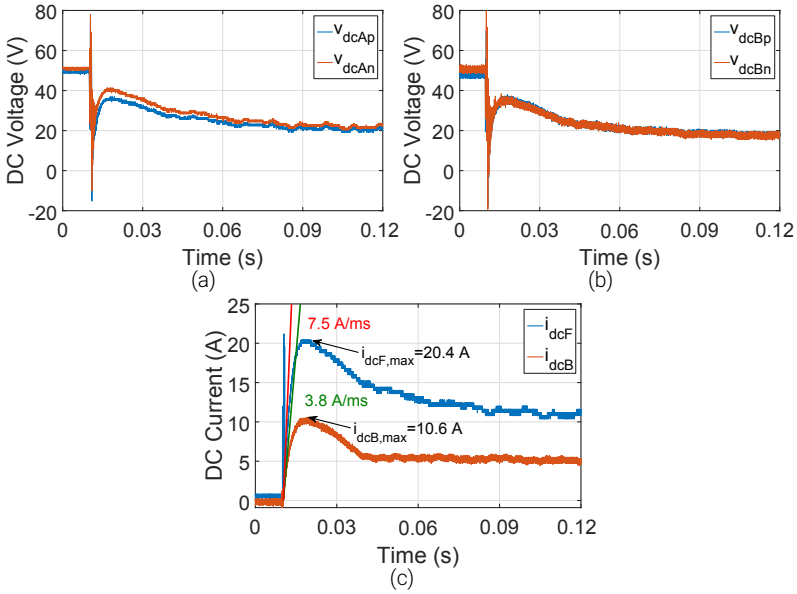


Figure 2.14: Fault case (ii): DC voltage at: a) MMC-A, b) MMC-B and (c) DC fault current. The red line indicates the di_{dcB}/dt as set by the arm inductors, while the green line indicates the max observed di_{dcB}/dt.

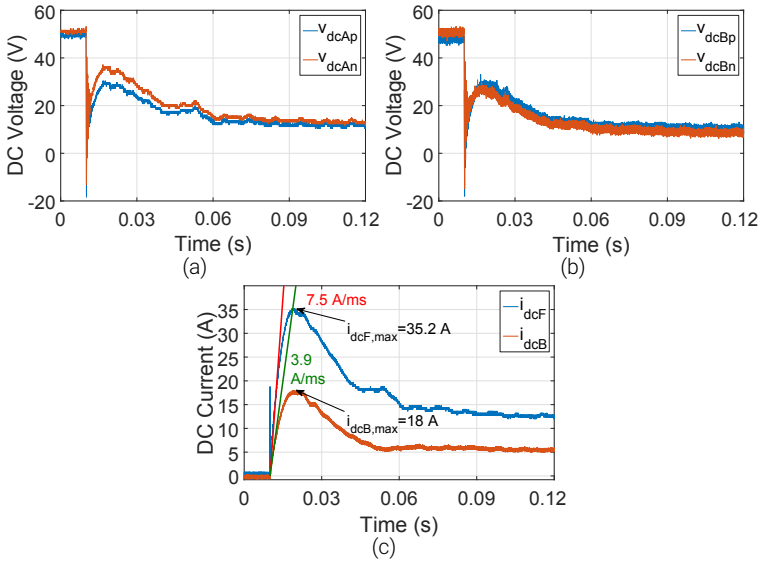


Figure 2.15: Fault case (iii): DC voltage at: a) MMC-A, b) MMC-B and (c) DC fault current. The red line indicates the di_{dcB}/dt as set by the arm inductors, while the green line indicates the max observed di_{dcB}/dt.

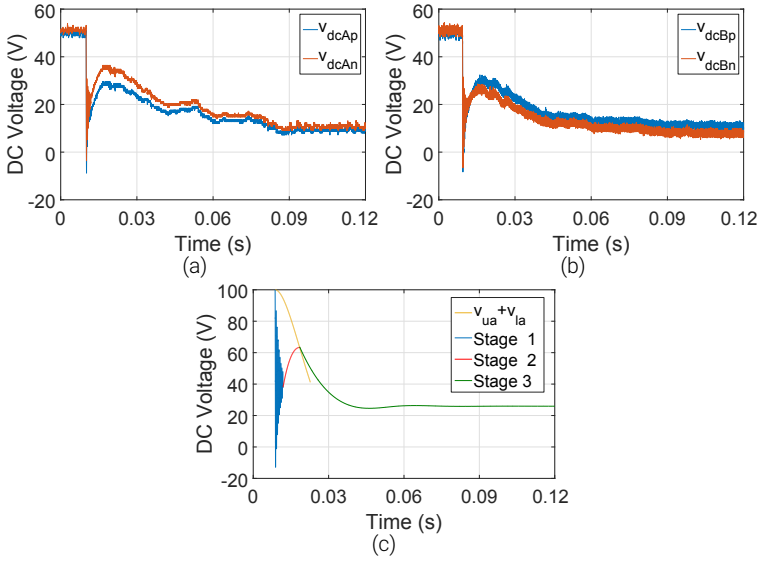


Figure 2.16: Fault case (iv): Pole DC voltage at: a) MMC-A, b) MMC-B. (c) MMC-A DC link voltage calculated solving equations of Section II. The sum $v_{ua}+v_{la}$ is plotted to signify the point at which Stage 3 begins.

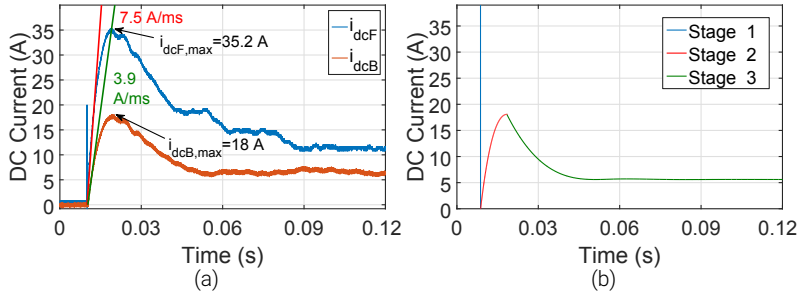


Figure 2.17: Fault case (iv): (a) DC fault current at fault point and at the output of MMC-B. The red line indicates the di_{dcB}/dt as set by the arm inductors, while the green line indicates the max observed di_{dcB}/dt. (b) DC fault current stages calculated solving equations of Section II. The first peak signifying Stage 1 refers to the discharge of the middle point capacitors through R_f, with a peak of $\frac{V_{dc}}{R_f}$ =76.9 A. In the experimental results, this peak was not sampled and thus, a value of only 20 A is displayed. Stages 2 and 3 refer to the current calculated at the output of MMC-B as shown in Figure 2.2(b).

DC capacitors discharge: In all cases the dc capacitors discharge first through the fault and this results in an almost immediate (<0.9 ms) initial voltage drop to zero.

MMC capacitors contribution: The steep dc voltage drop results in a voltage difference between the inserted submodule capacitors and the dc line. While the MMC switches are not blocked, the MMC capacitors get discharged and a high current peak is observed within 10 ms. The current stops increasing when the V_{dc} becomes equal to the inserted submodule capacitors voltage and a voltage peak is observed post-fault at that moment. The time this happens depends on the MMC capacitance and dv_{cap}/dt (in this design the di_{dc}/dt imposed by capacitor dv_{sm}/dt is lower than the di_{dc}/dt set by the 20 mH arm reactors (di_{dc}/dt = 7.5 A/ms)), whereas the current peak depends on the fault impedance. In case the converter was blocked, the time of the current peak would depend on the di_{dc}/dt limit set by the MMC arm reactors.

AC grid contribution: As described in Section II, from that point on, the V_{dc} follows the discharge of the MMC capacitors until a new steady-state V_{dc} level is reached. The new steady-state depends on the ac grid voltage and the fault impedance.

In this set-up, there is equal current infeed in the post-fault steady-state since the two set-ups are almost identical. As observed, higher fault currents are reached in case of lower fault resistance. Therefore, Fault case (ii) is not studied further.

Fault case (iii) Apart from the dc dynamics, the response of the MMC station and the ac dynamics need to be analysed. The circulating current follows the dc fault current reaching a peak point at 10 ms after the fault, as shown in Figure 2.18(c)-(d). At this stage, the ac side has not yet 'seen' the fault as the control dynamics are slow. Therefore, the fault current only circulates between the MMC legs and the fault. The current controllers react with the designed rise time. Therefore, the ac current and p_{ac} and q_{ac} have a rise time of 30 ms, as presented in Figure 2.18(a)-(b). Since there is a short-circuit, control cannot function properly and thus, there is both p_{ac} and q_{ac} on the ac side of each station. The p_{ac} is feeding the dc

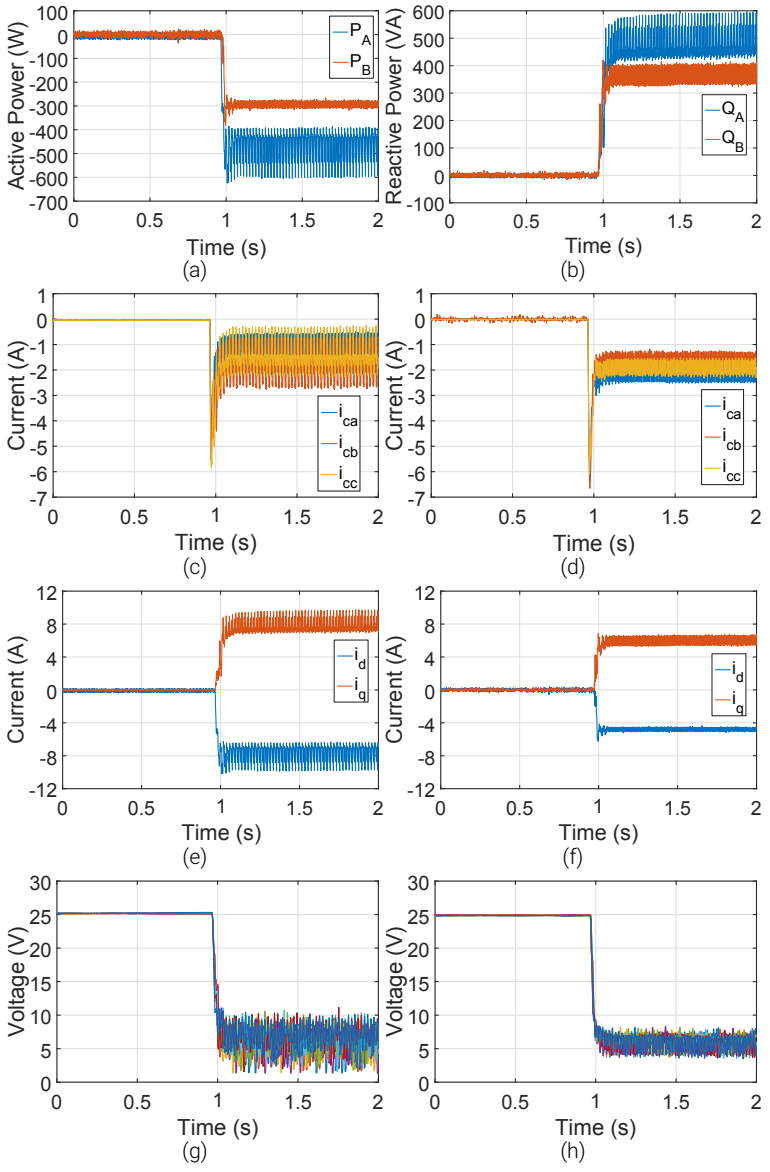


Figure 2.18: Fault case (iii): a) Active power, b) reactive power; circulating current at c) MMC-A, d) MMC-B; ac current in dq: e) MMC-A, f) MMC-B; submodule capacitor voltages of phase-b at: g) MMC-A, h) MMC-B.

fault and the q_{ac} flows to the respective ac grid. The ac power is given by:

$$p_{ac} = \frac{3}{2} v_d i_d \qquad q_{ac} = -\frac{3}{2} v_d i_q \tag{2.14}$$

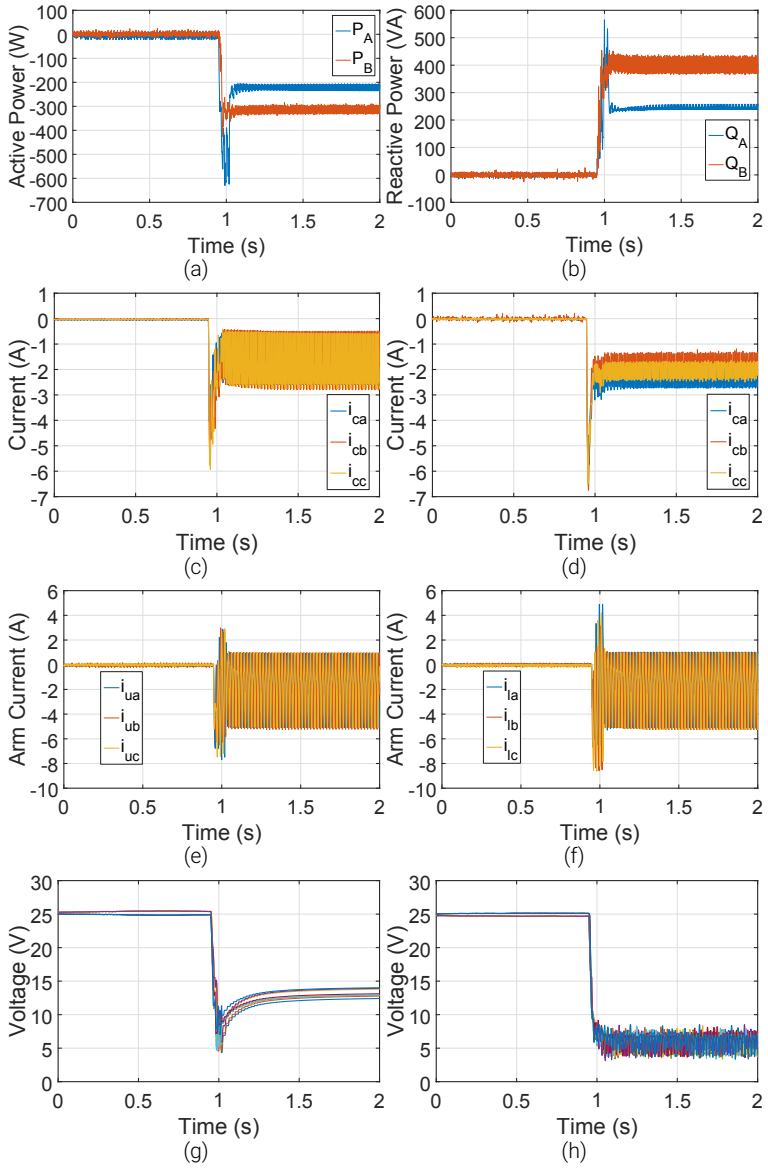


Figure 2.19: Fault case (iv): a) Active power, b) reactive power; circulating current at c) MMC-A, d) MMC-B; arm currents in MMC-A: e) upper, f) lower; submodule capacitor voltages of phase-b at: g) MMC-A, h) MMC-B.

where the dq ac currents are shown in Figure 2.18(e)-(f). Figure 2.18(g)-(h) shows that the discharge of the submodule capacitors depends on their capacitance. As a result, in both MMCs, the capacitor voltages exhibit the same fall time.

Fault case (iv) To study the case when the converter trips and switching stops, the overcurrent protection threshold is set at 8 A for the arm current. In this case, as MMC-A is trying to control the V_{dc}, the overcurrent threshold is surpassed 15 ms after the dc fault and at the next switching cycle a signal is sent to the submodule to inhibit the valve switching. It has to be noted that this is the only experimental fault case in which uncontrolled diode conduction takes place. This does not happen in MMC-B which continues its switching operation. The different response is evident in the submodule capacitor voltages of the two MMCs as presented in Figure 2.19(g)-(h), as well as in the circulating current in Figure 2.19(c)-(d). As soon as the submodules stop switching, the capacitors cannot discharge. However, since there is a positive part of the arm current, as shown in Figure 2.19(e)-(f), the capacitors slightly charge (see Figure 2.19(g)). Although the P_{ac} and Q_{ac} in MMC-B is the same as in Fault case (iii), the power levels of MMC-A change when it blocks its operation and a lower steady-state value is reached. MMC-A is no longer controlled to maintain a high ac current trying to raise the dc link voltage level as in Fault case (iii). This can be seen in Figure 2.19(a)-(b).

2.6. Conclusions

In this study a laboratory set-up for an MMC-based point-to-point dc connection was implemented. First, outer controllers were tested during normal operation for two dc grid topologies. The results showed that the dc voltage and reactive power control do not depend on the topology (symmetric or asymmetric monopolar). Moreover, energy balancing controllers are necessary in normal operation to reduce the arm voltage unbalances observed in case of asymmetric mainly, as well as symmetric monopolar configuration.

In case of faults, analytical expressions describing the three main dc fault development stages were derived and experimentally verified, while the effect of different fault types in the symmetric monopolar configuration were presented. As theoretically expected, the symmetric monopolar configuration has an inherent fault ride-through capability in case of a pole-to-mid-point fault, as a new steady-state is reached and control operation can continue within 1 ms. However, to achieve that, the dc lines need to be rated for the full dc link voltage.

On the contrary, in case of a pole-to-pole fault, which is the same independent of the monopolar configuration, the MMC cannot continue its control operation due to the imposed low dc link voltage level. The observed fault current peak value is determined by the fault impedance, while it was shown that the current stops increasing when the dc link voltage becomes equal to the inserted submodule capacitors voltage and a voltage peak is observed post-fault at that moment. The moment at which the fault current stops increasing depends on the di_{dc}/dt and thus, on the arm reactor inductance and the submodule capacitance, in case the MMC control operation is not blocked.

As long as the overcurrent threshold is not surpassed, switching operation can continue and could potentially facilitate a faster recovery in case of a temporary fault. However, if switching is not blocked, the MMC tries to control the ac currents and raise the dc link voltage, resulting in steady-state values even twice as high as in the blocked case. As a result, blocking the switching operation may be preferred. The steady-state dc fault current only depends on the ac grid voltage level and the dc fault impedance.

Regarding the developed set-up, this can be easily expanded to facilitate a multi-terminal dc network. Following the structure of the existing MMC set-up, additional converters need first to be developed, while the connection to the already existing dc link is possible through the use of one or more pi-sections. If more accuracy is necessary to study the way differ-

ent parts of the dc link cable discharge through the dc fault, more pi-sections or different configurations can be employed that resemble the cable structure more accurately.

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3

Multi-Line Breaker for HVDC Applications

This Chapter presents a breaker arrangement concept, the Multi-Line Breaker (MLB), for the protection of multi-terminal high voltage dc (MTDC) networks. Based on the design of a hybrid breaker, the MLB is an economically attractive solution for the protection of multiple dc lines in nodal connection using a single main breaker path. By using commutation units, the MLB directs the fault current through the main breaker in a unidirectional way, irrespective of the fault location. Hence, this study presents the design requirements for the MLB, regarding both hardware and control, and evaluates its operation within a grid. For this reason, a four-terminal Half-bridge MMC-based MTDC grid in radial configuration was used and pole-to-ground dc fault conditions were investigated. The dc fault response of the grid with one MLB at the central node is compared to the respective response of the grid when one hybrid breaker is employed at each dc line. The simulations show that the MLB is feasible and that the overall MTDC grid fault response for the two protection systems is very similar. As a result, the design advantages of the MLB make it a promising solution for the dc fault isolation in MTDC grids.

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3.1. Introduction

Due to the absence of a natural zero-crossing of dc current, the isolation of a fault on a dc line is more difficult than in case of faults in ac grids [1]. Very fast transients and high overcurrents, occurring in case of dc faults, are likely to damage the involved equipment and are more difficult to isolate [2]. To isolate dc faults, breakers need to be rated for high current (e.g. 12 pu) [3]. Moreover, there are high requirements for the dissipation of the energy stored in HVDC lines [4] and the time constraints are very stringent, especially when it comes to grid operation, where the dc fault needs to be isolated before it affects the operation of the 'healthy' part of the grid [5].

Many dc breaker topologies have been proposed to solve the protection problem in HVDC grids [6, 7, 8, 9]. Among them solid-state breakers and hybrid mechanical breakers, as proposed in the literature [10], appear to be the most promising technologies, mainly due to their low fault interruption times. Apart from the time response, on-state losses are also a very important issue [11]. Due to the large scale transmission of bulk energy, the system has to have high efficiency during normal operation. Hybrid breakers have a better performance, as they consist of the Nominal Current Path (NCP) with low resistance that is used during normal operation, the Current Commutation Path (CCP) and the Energy Absorption Path (EAP). In general there are several different hybrid breaker topologies proposed [12, 13, 14, 15], which can be grouped into two main types, i.e. one type uses Ultra-Fast Disconnectors (UFD), while the second type uses mechanical circuit breakers as the mechanical switching element. For the first type, there are different implementations, one of which can be described as Load Commutation Switch - Mechanical Breaker (LCS-MB), using an LCS/UFD in parallel with a stack of semiconductors, which can be controllably switched on and off. This principle was presented by ABB under the name 'proactive hybrid circuit breaker' [12]. The general structure of a hybrid breaker is presented in Figure 3.1.

Although it is claimed by HVDC manufacturers that circuit breakers are readily available, multi-terminal HVDC networks are not yet realised in large-scale, apart from two projects which were commissioned in the last two years in China, which do not have dc circuit breakers yet [16, 17]. Among other problems, cost of protection poses a significant challenge towards dc grids [18]. In case of hybrid breakers, the use and cost of the different paths involved in the breaking process needs to be optimized. Past studies have proposed different concepts in the direction of breaker design and possible implementation into networks, including the idea of component sharing[19, 20] to decrease the cost. However, more elaborate studies are necessary, which need to examine the hardware and control implementation of the dc breakers in MTDC networks, taking into account the boundary conditions that influence the fault interruption time requirements.

The idea to use a circuit arrangement to replace several circuit breaker at a dc node by only one, i.e. the Multi-Line Breaker (MLB), was presented in a patent of the authors[21]. This is realized by minimising the number of CCP and EAP paths needed and also the number of the involved switching elements within the breaker, while offering a bidirectional fault isolation capability. Based on the basic operation principle and path structure of proposed dc breakers, the MLB optimizes the use number of protection assets by using only one unidirectional CCP and one EAP for more than one dc line, as shown in Figure 3.2. To achieve that, two NCPs connected at each dc line are controlled to drive the dc fault current through the main breaking paths, whereas at normal operation they facilitate the bidirectional power flow in the dc grid. Unlike [20], the MLB design is simple and highly modular, facilitating the easy expansion to more interconnecting lines.

A dynamic analysis of the application of the same circuit arrangement as a bi-directional circuit breaker on a single line was presented in [22]. This is a special case that is also mentioned in [21]. However, in this case, the use of one individual circuit breaker on each line is proposed, instead of only one unidirectional main breaker to protect a complete node.

This Chapter's main contribution is the design and in depth analysis of the MLB based on the idea presented in [21]. This constitutes a generalized concept and is elaborated hereby with the structure of the LCS-MB. This Chapter goes beyond previous studies [21, 22], providing a thorough investigation of the hardware and control implementation of the MLB. More specifically, the switching actions of different switches in the breaker paths and the effect the timing has on the MLB operation are studied. Moreover, an economic analysis is provided, taking into account the relative costs of components and the scalability of the breaker to more lines, in order to quantify the advantages the new breaker arrangement brings compared to the use of individual breakers for each line. Additionally, this study presents a sizing methodology of the main breaker components for the chosen case study. Finally, the MLB performance is evaluated using an example of an MTDC grid and is compared to the performance of individual dc breakers for each dc line. Table I is used for quick reference of the most commonly used abbreviations in this Chapter.

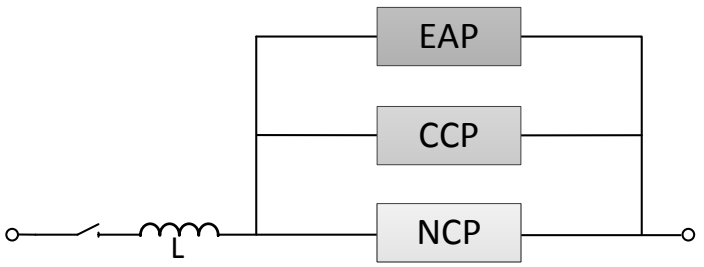

Figure 3.1: Hardware structure of a hybrid breaker.

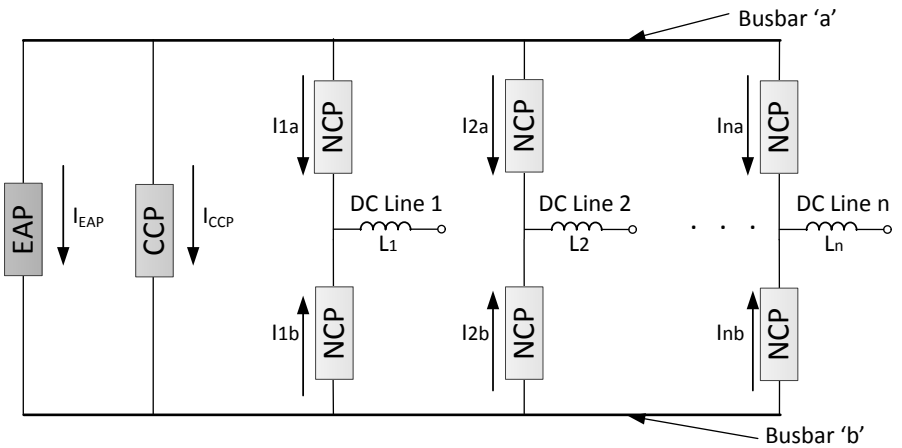

Figure 3.2: Hardware structure of a Multi-line breaker (MLB).

Table 3.1: Abbreviations of Common Terms.

LCS-MB	Load Commutation Switch - Mechanical Breaker
MLB	Multi-Line Breaker
NCP	Nominal Current Path
CCP	Current Commutation Path
EAP	Energy Absorption Path
LCS	Load Commutation Switch
UFD	Ultra-Fast Disconnector

The Chapter is structured as follows: Section 3.2 introduces the breaker concept, explaining the hardware and software implementation needs, analysing the cost of the protection system in comparison to a dc grid protected by hybrid circuit breakers. Section 3.3 presents the case study used to evaluate the effectiveness of the breaker, along with the specifications of the main grid assets. In Section 3.4, the results for the MLB fault response are compared to the results obtained using hybrid breakers and the main differences in the transient behavior are elaborated. Finally, in Section 3.5, conclusions are drawn on the feasibility of the proposed breaker concept.

3.2. Multi-line breaker concept implementation

3.2.1. Hardware Requirements

Based on the review analysis performed in [15], the LCS-MB, as proposed in [23] and shown in Figure 3.3, appears to be faster than other hybrid breaker concepts proposed in the literature, although probably more expensive. Therefore, in the present study, the LCS-MB is chosen as the reference case for evaluation of the proposed MLB concept.

Based on the LCS-MB design, the MLB uses an Ultra Fast mechanical Disconnector (UFD)

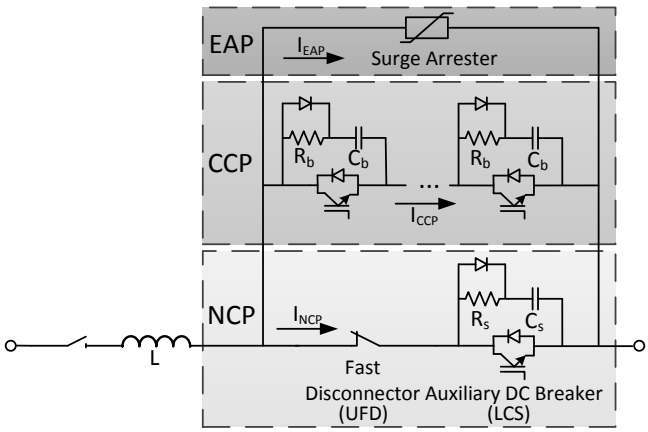

Figure 3.3: LCS-MB breaker with its three paths.

and a Load Commutation Switch (LCS), which constitute the NCP, to connect each line to each of the two busbars, which, hereafter, will be identified as 'a' and 'b', as shown in Figure 3.2. Busbars and connections can introduce stray inductances that affect the current commutation speed between branches. Hence, care has to be taken, when designing the circuit breaker. However, if the design is optimized for low stray inductance, the commutation time can be considered significantly smaller than the total operation time of the breaker. As a result, in this study, the busbar inductances are not considered in the analysis of the MLB. In this configuration, a single CCP and EAP is sufficient to break the dc fault current. It has to be noted that the system designer can decide to oversize the CCP and EAP ratings, based on the number of dc faults that the MLB needs to deal with simultaneously. A schematic of the implemented version of the MLB is presented in Figure 3.5.

The main difference between the proposed concept and existing breaker concepts is that it allows the protection of multiple lines at the same time. By using only one main breaker circuit in a unidirectional scheme, the MLB significantly reduces the number of switching elements needed and subsequently the protection system cost. It has to be noted that to isolate the dc fault in the proposed MLB arrangement, more individual switching actions are required than in case of the LCS-MB. However, as these occur in parallel, the total fault interruption time is not affected. Moreover, as this might affect reliability, it has to be taken into account, when specifying the requirements for UFDs for the MLB. Moreover, the necessary volume of the station, housing the protection system, is also reduced further bringing down the cost and the construction complexity of the project, which are more important in case of offshore constructions.

3.2.2. Control Requirements

In case of an LCS-MB the control sequence is straightforward, as shown in Figure 3.4. As soon as a fault is detected, the LCS of the NCP opens and the current commutates to the CCP. When i_{NCP} drops to residual current level, the UFD opens. Finally, when UFD is fully open and has established dielectric strength (approximately within 2 ms), the switches in the CCP are switched off and the current commutates to the EAP, where the energy is dissipated.

Based on the control sequence of the LCS-MB, the MLB control is designed. More specifically, Figure 3.5 shows the MLB control sequence in case of a three-line dc connection, when

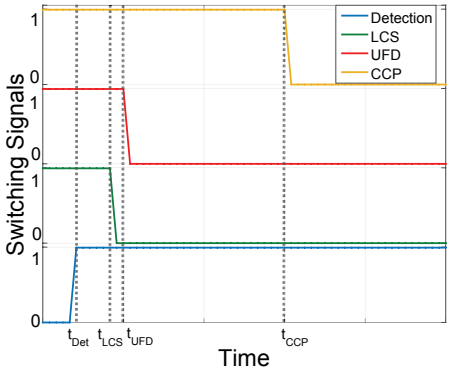

Figure 3.4: Switching sequence hybrid. '1' and '0' values indicate the 'on' and 'off' states respectively.

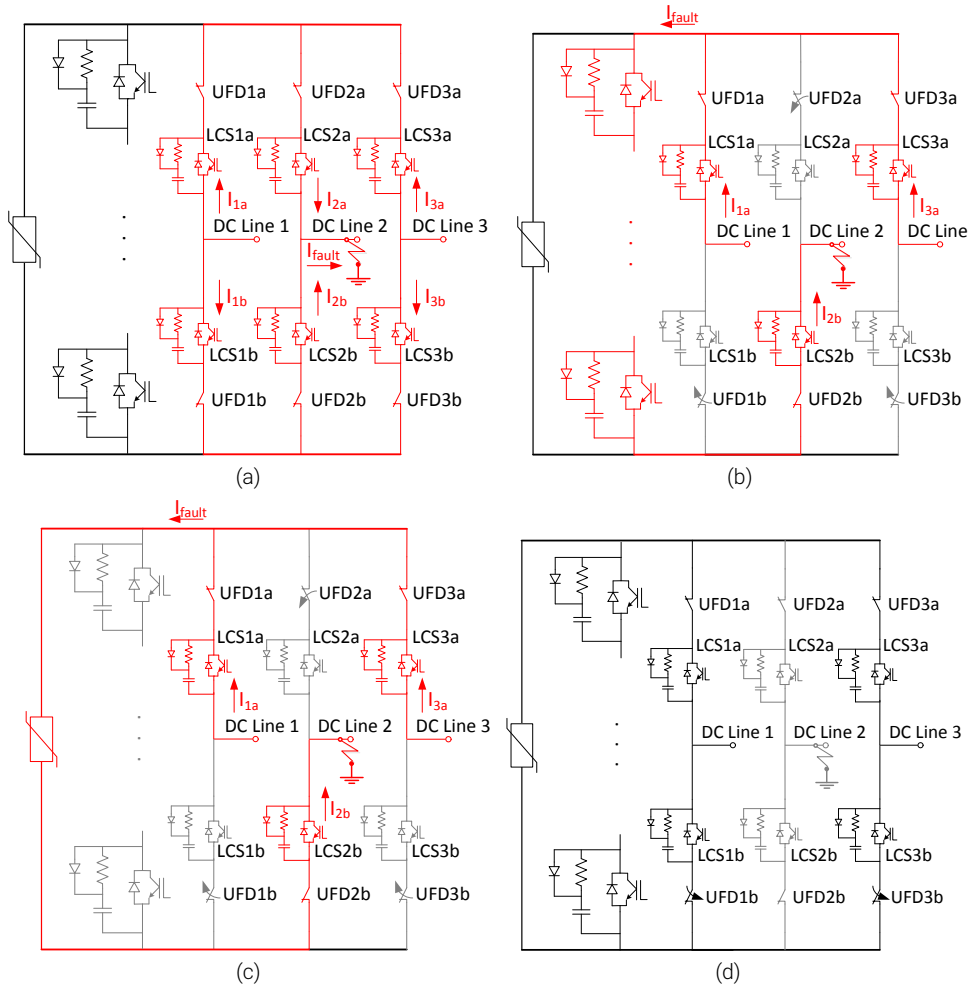

Figure 3.5: Control sequence of the MLB illustrated for a configuration with three attached lines.

the fault occurs on line 2. It has to be noted that in case of the MLB, a jitter of the UFD opening times will probably occur. As a result, a dead-time is required in the design, to allow the synchronization of the UFDs opening. Figure 3.6 presents the times on which control events occur. In the time symbols used in the following analysis, the subscripts 'f' and 'nf' denote the faulty and not-faulty line respectively, while the subscripts '(a)' and '(b)' indicate the bus to which the NCP unit is connected.

Four control steps can be distinguished for the dc fault ride-through:

1. Initially, all switches of the MLB are closed. As soon as a dc fault occurs on line 2, the capacitances of the healthy lines discharge through the fault. Therefore, there is a high overcurrent flowing from the connected healthy lines through the node into the

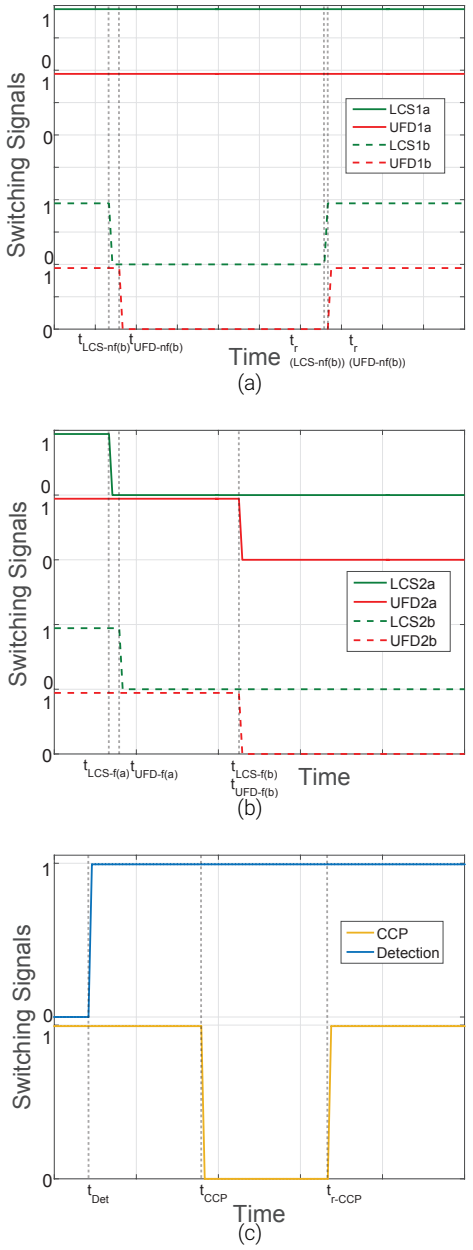

Figure 3.6: Pole-to-ground - Switching Sequence MLB1: (a) Healthy line path (1); (b) Faulty line path (2); (c) Main Breaker path and Fault signals. '1' and '0' values indicate the 'on' and 'off' states respectively.

fault, e.g. dc line 2 (I_{2a} and I_{2b}), as shown in Figure 3.5(a).

2. After the faulty line is detected at t_{Det}, the faulty line is disconnected from bus 'a' by opening the NCP unit (UFD2a/LCS2a) ($t_{LCS\text{-}f(a)}$ and $t_{UFD\text{-}f(a)}$), while the healthy lines are disconnected from bus 'b' by opening the respective NCP units (UFD1b/LCS1b and UFD3b/LCS3b) ($t_{LCS\text{-}nf(b)}$ and $t_{UFD\text{-}nf(b)}$). This commutates the complete fault current into the unidirectional CCP. This step is shown in Figure 3.5(b).
3. When the mechanical disconnectors on the NCP units, which were opened in the previous step, are fully open and have established their dielectric strength (~ 2 ms), the switches in the CCP open (t_{CCP}) and the current commutates to the surge arrester in the EAP path, where the energy is dissipated, as presented in Figure 3.5(c).
4. Once the fault current flowing to the faulty line drops to residual current level, the NCP unit (UFD2b/LCSb) opens ($t_{LCS\text{-}f(b)}$ and $t_{UFD\text{-}f(b)}$). In this way, dc line 2 is fully isolated from the rest of the network. At this moment, the NCP paths (UFD1b/LCS1b and UFD3b/LCS3b) connecting the 'healthy' lines to bus 'b' reclose ($t_{r(LCS\text{-}nf(b))}$ and $t_{r(UFD\text{-}nf(b))}$) and CCP recloses as well ($t_{r\text{-}CCP}$), as in Figure 3.5(d). In this way, normal operation is restored in the grid and the MLB is ready to isolate a possible fault in another line.

The aforementioned control strategy is independent of the number of lines interconnected through the MLB and therefore, the breaker is highly modular with minimum changes.

3.2.3. Economic considerations

Hereby, a comparative analysis of the costs of the different protection systems is made taking into account the cost of the involved paths. To allow the comparison, it is assumed that the paths that are used for the MLB are exactly the same as the ones used for the individual hybrid breakers, which is the worst-case scenario for the cost comparison. It is assumed that c_{NCP} is the cost of the nominal current path, c_{CCP} is the cost of the current commutation path and c_{EAP} is the cost of the energy absorption path. Assuming n is the number of interconnected lines, cases $n = 1$ or 2 refer to a point-to-point connection. Therefore, the following analysis is made for $n \geq 3$. The total cost of the LCS-MB breaker is calculated as:

$$\Sigma C_{LCS\text{-}MB} = n \cdot (c_{NCP} + c_{CCP} + c_{EAP}) \tag{3.1}$$

Respectively, the cost of the MLB is given by:

$$C_{MLB} = 2 \cdot n \cdot c_{NCP} + c_{CCP} + c_{EAP} \tag{3.2}$$

To make a comparison between the two costs for n lines, the fraction of the path costs is used. Assuming that:

$$\frac{c_{NCP}}{c_{CCP}} = a \tag{3.3}$$

and

$$\frac{c_{EAP}}{c_{CCP}} = b \tag{3.4}$$

As a result, the cost fraction $\frac{\Sigma C_{LCS\text{-}MB}}{C_{MLB}}$ of the two technologies depends on both n, a and b. In case the breakers have unidirectional breaking capability, the cost fraction is given by:

$$\frac{\Sigma C_{LCS\text{-}MB}}{C_{MLB}} = \frac{n(a+1+b)}{2na+1+b} \tag{3.5}$$

while assuming that LCS-MB has bidirectional breaking capability, this cost fraction becomes larger, as the c_{CCP} of the LCS-MB is double compared to the MLB, namely:

$$\frac{\Sigma C_{\text{LCS-MB}}}{C_{\text{MLB}}} = \frac{n(a+2+b)}{2na+1+b} \tag{3.6}$$

Figure 3.7 shows the trend of the costs for the technologies using unidirectional breaking capability. Assuming that the same CCP and EAP paths can be used in both breaker technologies, while only the number of involved NCP paths changes, the ratio between the cost of NCP and the combined costs of CCP and EAP becomes of value in the analysis and is calculated as:

$$\frac{c_{\text{NCP}}}{c_{\text{CCP}} + c_{\text{EAP}}} = \frac{a}{b+1} \tag{3.7}$$

The use of MLB is justified if the following conditions apply: (i) three or more lines are interconnected through the MLB and (ii) the cost of the NCP is lower than 0.6 of the combined cost of CCP and EAP. The more lines and the higher the cost ratio between the NCP and CCP+EAP, the higher the individual LCS-MB breakers capital investment is compared to the proposed MLB solution. It has to be noted that the comparison is theoretical, neglecting the details of the cost division between the different components involved. In case of bidirectional LCS-MB capability, the cost ratio of the two technologies would be higher.

3.3. MTDC Network Case study

The performance of the different circuit breaker concepts is evaluated in the present study using a four-terminal radially-connected MTDC network with Half-bridge MMC stations as presented in Figure 3.8. As shown, the MTDC network operates in asymmetric monopolar configuration with metallic return.

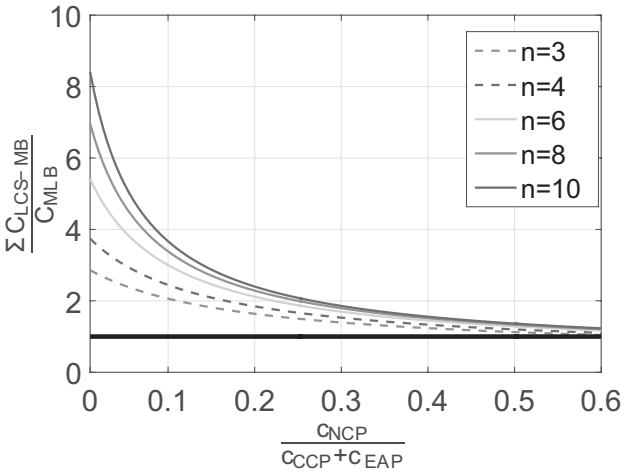

Figure 3.7: Sensitivity analysis of the cost of MLB over LCS-MB breakers and cost ratio between NCP and the combined cost of CCP+EAP, for different number of lines n. The thick black line, at y=1, indicates the break-even point between the two breaker costs.

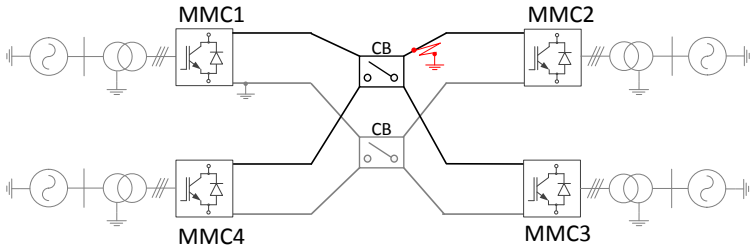

Figure 3.8: Layout of the analyzed radial MTDC network with 4 terminals with a pole-to-ground dc fault.

In normal operation, MMC1 is used to control the dc voltage operational level of the MTDC grid, while MMC2, MMC3 and MMC4 control their ac active power. The return path is grounded at the dc side of the MMC1 station. In case of the MMC station, no bulky capacitors are used on the dc side of the stations and thus, the dc fault currents exhibit lower initial peak [2, 3]. As a result, no large limiting reactors are necessary on the dc side of the MMC, as the MMC arm reactors are designed accordingly to limit the rate of rise of the current in case of terminal faults. However, limiting reactors are necessary on the node of the radial connection and thus, they are taken into account in the dc breaker design. The main MTDC network parameters are shown in Table 4.1.

3.3.1. MMC Model

This Chapter focusses on the protection of an MTDC network that is based on Half-bridge MMC converter stations, which do not have inherent fault current blocking capability. The aim of this study is to evaluate the proposed breaker concept and present a proof-of-concept. Therefore, 9-level Half-bridge MMCs are used in this study for simplicity purposes and their specifications are presented in Table 4.2. For the MTDC network analysis, a detailed simulation model which accounts for the MMC-HVDC stations switching behavior is implemented using the SimPowerSystems toolbox of Matlab/Simulink. All the converters share the same control structure, regardless of their control mode within the MTDC network, as presented

Table 3.2: MTDC network parameters.

Network parameters	**Unit**	**Value**
MMC rated power (S_{MMC})	MVA	1200/1200/600/600
MTDC voltage (V_{dc})	kV	320
DC cable resistance (R_{cable})	Ω/km	0.0195
DC cable inductance (L_{cable})	mH/km	0.2
DC cable capacitance (C_{cable})	nF/km	220
DC cable length (d1/d2/d3/d4)	km	50
Transformer voltage ratio (MMC1/MMC2)	kV	380/160 (Y_0-Δ)
Transformer voltage ratio (MMC3/MMC4)	kV	33/160 (Y_0-Δ)
Transformer rated power (S_{T})	MVA	1200/1200/600/600
Transformer leakage inductance (L_{T})	pu	0.05

Table 3.3: MMC parameters.

MMC specifications	Unit	Value
Submodule capacitance (C_{sm})	mF	4
Arm inductance (L_{arm})	mH	8
Arm resistance (R_{arm})	Ω	0.07
Number of SMs per arm (N)	-	8
Carrier frequency (f_C)	Hz	600
Sampling frequency (f_S)	kHz	20

in Figure 6.2 [24]. Moreover, the dc lines are modelled using cascaded pi-equivalent cable sections.

The converter valves are only tripped by the overcurrent protection which is implemented at each converter arm. As soon as one of the arm currents exceeds the defined current threshold, the fault signal is sent to the converter controller and the converter trips. The thresholds of the overcurrent protection function is defined at 2 pu [10] and its absolute value depends on the rating of each converter station.

3.3.2. Circuit Breaker Model

The circuit breakers used in this study are modeled using the SimPowerSystems toolbox of Matlab/Simulink. A simple selective fault detection method is used based on the current direction during a dc fault. A dc line overcurrent threshold is chosen equal to the threshold of the IGBT valves of the converter station, i.e. 2 pu. As soon as a fault occurs on a dc line, the line capacitance discharges through the fault. As a result, current from all lines flows towards the dc fault point, as it is shown in Figure 3.10. As soon as this current exceeds the defined protection threshold, the faulty line is identified and the actions for its isolation are initiated. In case of a breaker or bus failure, back-up protection can be provided either by disconnecting all the lines connected to the node using the breakers on the other ends of the lines or by operating the ac breakers at the converter terminals. However, this would result in a disconnection of the node, which would lead to a substantial power flow disturbance. Therefore, backup protection is an issue that has to be considered before building the grid

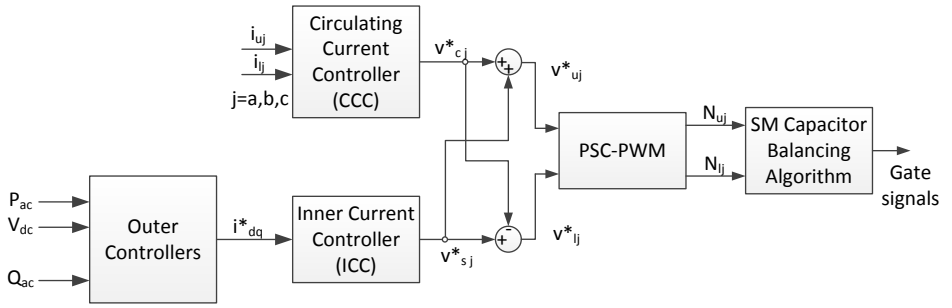

Figure 3.9: Control structure of the MMC station, where u, l indicate the upper and lower arm of the MMC respectively and j indicates the corresponding phase leg [24].

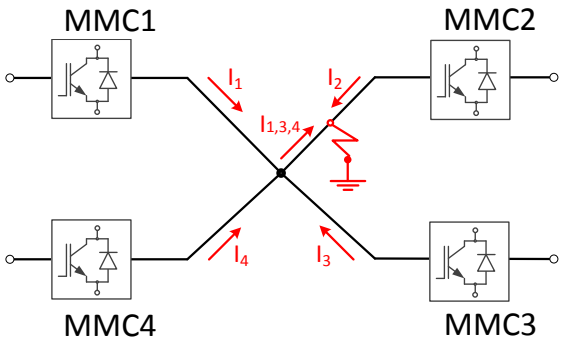

Figure 3.10: Current direction during a dc fault [24].

and has severe consequences for both MLB and LCS-MB schemes.

In the design of the circuit breaker, several parameters need to be taken into account. First of all, the LCS on each path is structured as a 3x3 IGBT array with 15 kV voltage rating and 15 kA current rating. The LCS RC snubber circuit parameters are selected based on these ratings to protect the LCS IGBTs at all instants of operation [25]. Moreover, the voltage drop across the UFD must remain very small until full contact separation, which is estimated at 2 ms. The design of the UFD and its contact motion characteristics affect the increase in dielectric strength during opening. In this study, for simplicity reasons, linear opening motion and homogeneous field conditions are assumed. This results in a linear increase of the dielectric strength of the UFD of 320 kV/ms. Finally, the CCP has 192 IGBTs grouped in 4 stacks.

The circuit breaker parameters for the two technologies under study are presented in Table 3.4. In addition to the dc circuit breaker, the ac side breakers of the respective MMC are tripped if a fault or overcurrent is detected.

Table 3.4: Circuit breaker parameters.

Parameters	**Unit**	**Value**
Nominal Path Forward Resistance (R_n)	mΩ	1.5
Comm. Path Forward Resistance (R_c)	mΩ	288
UFD opening time (t_c)	ms	2
Number of IGBTs in CCP (n_c)	-	192
LCS Snubber Resistance (R_s)	Ω	100
LCS Snubber Capacitance (C_s)	uF	4
Breaker Snubber Resistance (R_b)	Ω	5000
Breaker Snubber Capacitance (C_b)	uF	4
Limiting inductance ($L_{1,2,3,4}$)	mH	30
Residual voltage of SA @ 10kA	pu	2.2

3.4. Results

In this Section, the operational dynamics of the two breaker concepts and the effect on the post-fault operation of the interconnected stations are evaluated. A dc fault with a resistance of 7 Ω is applied at 0.3 s of the simulation [3]. The worst-case scenario for the protection system coordination is when the fault occurs as close as possible to the central node of the grid and to the breaker station, as identified in [10]. A pole-to-ground dc fault is investigated to compare and evaluate the performance of the two breaker technologies. The fault is applied on line 2 as shown in Figure 3.8 and Figure 3.10. Breakers are placed on both poles of the dc grid and their operation is triggered by the same fault detection signal to completely isolate the faulty part of the grid.

The currents and voltages are monitored during simulation at all crucial points of the grid. The most important results showing the transients taking place during the dc fault response are presented in Figure 3.11 and Figures 3.12, 3.13 for the LCS-MB and the MLB, respectively.

The current that the LCS-MB needs to interrupt, reaches a peak of 9.6 kA in the CCP. As soon as the LCS is turned off, a commutation voltage builds up across the LCS leading to the current commutation into the CCP. The UFD is opened and after current interruption, it has to withstand the transient interruption voltage (TIV) with a peak of 671 kV and a steady-state value equal to the nominal dc pole voltage. Although the current drops to zero after almost 3.6 ms, the voltage takes approximately 60 ms to reach a steady-state. This can be attributed to the LC parameters of the dc lines and the transient response post-fault, as shown in Figure 3.14.

In case of the MLB, the current and voltage stresses on the paths connected to the faulty line and one 'healthy' line are presented in Figure 3.12 and Figure, 3.13. The peak current on the main breaker path also reaches 9.6 kA, while the voltage on the surge arrester reaches a peak of 672 kV and a steady-state of 320 kV before dropping to zero when the faulty line is isolated and the main breaker is reset for later operation. The peak current is the same as in the case of LCS-MB, since the grid RLC parameters are the same. On the paths connected to the faulty line, the UFD takes up the voltage stress as in the case of the LCS-MB breaker, whereas the voltage across the LCS remains low. The respective path current drops to zero depending on the switching sequence of the MLB, as presented in Figure 3.6.

In the healthy path 1a, the LCS and the UFD remain closed at all instants. As shown in

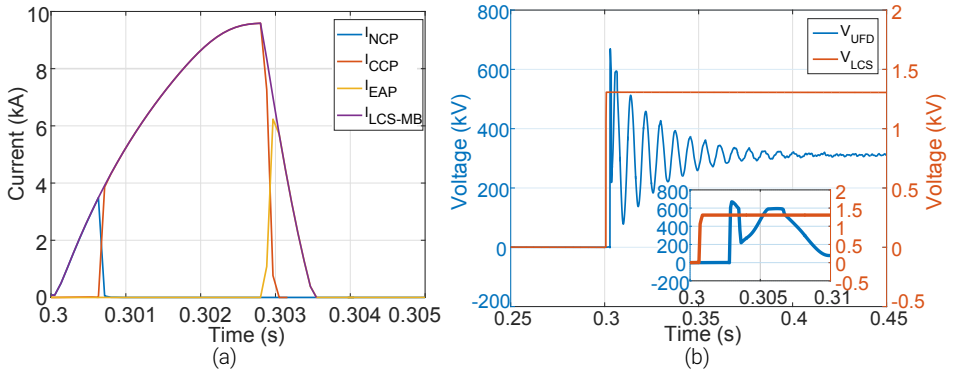

Figure 3.11: LCS-MB: (a) current on the breaker paths; (b) voltage stresses on the NCP switches.

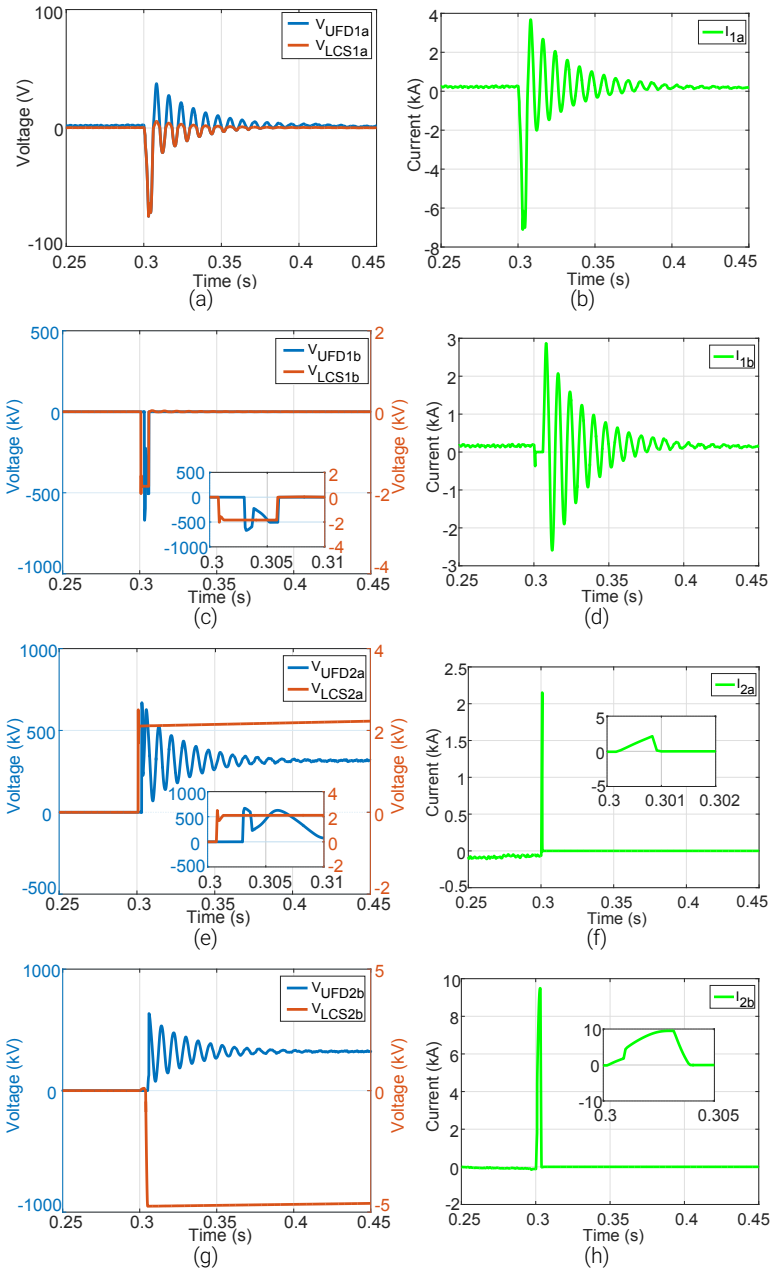

Figure 3.12: Current and Voltage at the paths of MLB1: (a) Voltages on 'healthy' NCP 1a; (b) current on 'healthy' NCP 1a; (c) voltages on 'healthy' NCP 1b; (d) current on 'healthy' NCP 1b; (e) voltages on 'faulty' NCP 2a; (f) current on 'faulty' NCP 2a;(g) voltages on 'faulty' NCP 2b; (h) current on 'faulty' NCP 2b.

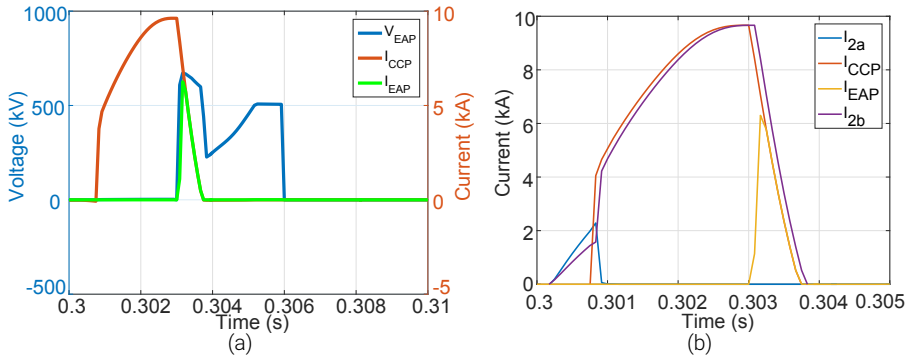

Figure 3.13: (a) Currents on CCP and EAP path; (b) Total breaker fault current.

Figure 3.12 (b), initially there is a surge current resulting from the discharge of the capacitance of line 1 towards the dc fault point. The current dynamics follow the dc voltage dynamics in the grid. On path 1b, the voltage across the UFD reaches a peak of 670 kV as the path is disconnected for a time period until the fault is isolated. The current characteristics are similar to path 1a.

The overall system response is better described by the main control variables. In this case study, these are the dc voltage at the output of MMC1, as well as the dc currents at all interconnected stations. From Figure 3.14, it becomes apparent that the voltage transients taking place in both case studies are very similar, as they depend on the fault interruption time and the LC parameters of the 'healthy' cables, which get anew charged to their nominal voltage level after the fault is isolated. From the zoomed subfigure in Figure 3.14, it can be seen that the voltage drop starts to recover at 3.1 ms and 3.2 ms for LCS-MB and MLB respectively, which is the time when the fault current is fully commutated to the surge arrester. In both cases the nominal voltage level reaches a new steady-state level post-fault after approximately 60 ms (t_{VSS}), while it is fully restored above 90% after 27 ms (t_{V90}).

For the case study under investigation, the switching sequence in the breakers is pre-

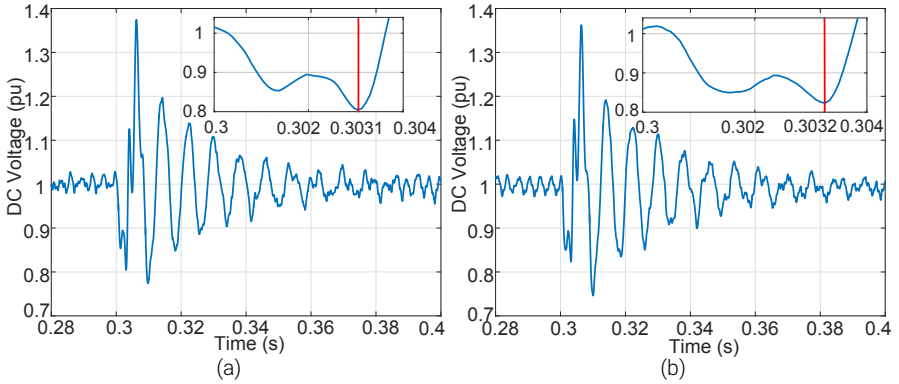

Figure 3.14: DC voltage at MMC1: (a) LCS-MB; (b) MLB. The red line indicates the time at which the dc voltage starts to recover in each case.

sented in Table 3.5, using the symbols introduced in Section II for the switching times. The fault detection time is the same for both systems, since it only depends on the grid and fault characteristics. Moreover, the total interruption time $t_{\text{Interruption}}$ for MLB is higher by 0.2 ms compared to LCS-MB. This difference can be attributed to the fact that in MLB the current in multiple NCP paths needs to drop to a residual current level before switching off the CCP.

Table 3.6 compares the most important aspects in the breaker operation. In fact, the LCS-MB and the MLB experience similar peak currents in the CCP (~9.6 kA). However, it has to be noted that a change in the current rating of the CCP can have a significant impact in the design of the breaker and its cost. Considering a case study in which the peak current would increase over 12 kA, assuming that the IGBTs have a current rating of 3 kA[26], a whole new stack of IGBTs needs to be added in parallel on the CCP path to withstand the peak current. As a result, 96 new IGBTs need to be added in the CCP path of the MLB, while this number is quadrupled in case of the LCS-MB, since the CCP path of the LCS-MB on each line needs to be rated for the new current peak.

On the other hand, 213.1% higher current peak is reached in NCP path 2b of MLB, as this needs to remain connected to the faulty line until the breaker operation has brought current to zero. Although there is a considerable difference in the relative change, the consequences are fundamentally different compared to the CCP case, due to the low voltage rating of the LCS. Because of the low current on the NCP path of LCS-MB, two parallel stacks of three series connected IGBTs are sufficient. On the contrary, the MLB needs four parallel stacks of three series connected IGBTs on each NCP. As a result, the number of additional IGBTs on the NCP of MLB has to be scaled by the number of parallel connected IGBTs and by twice the number of connected lines. As a result, the MLB needs in total 48 IGBTs (six on each of the eight NCPs) more than the LCS-MB. Hence, while still considerable, it is still a

Table 3.5: Switching Sequence Events.

Time	**LCS-MB**	**MLB**
t_{Det} (ms)	0.6	0.6
t_{LCS} (ms)	0.6	-
t_{UFD} (ms)	0.8	-
t_{CCP} (ms)	2.8	3
$t_{\text{Interruption}}$ (ms)	**3.6**	**3.8**
t_{Vss} (ms)	**60**	**60**
t_{V90} (ms)	**27**	**27**
$t_{\text{LCS-nf(a)}}$ (ms)	-	0.7
$t_{\text{LCS-f(a)}}$ (ms)	-	0.7
$t_{\text{LCS-f(b)}}$ (ms)	-	3.7
$t_{\text{UFD-nf(a)}}$ (ms)	-	0.9
$t_{\text{UFD-f(a)}}$ (ms)	-	0.9
$t_{\text{UFD-f(b)}}$ (ms)	-	3.7
$t_{\text{r(LCS-nf(b))}}$ (ms)	-	5.7
$t_{\text{r(UFD-nf(b))}}$ (ms)	-	5.8
$t_{\text{r-CCP}}$ (ms)	-	5.8

Table 3.6: Breaker Comparison.

Peak Values	LCS-MB	MLB	MLB-p Path	% Diff.
V_{LCS} (kV)	1.52	4.76	2b	213.1
V_{UFD} (kV)	670	670	1b	0
V_{EAP} (kV)	671	672	-	0.1
I_{NCP} (kA)	3.46	9.62	2b	178
I_{CCP} (kA)	9.6	9.62	-	0.2
I_{EAP} (kA)	6.19	6.26	-	1.13
$E_{absorption}$ (MJ)	1.33	1.39	-	4.5

minor increase compared to the number of additional CCPs (192 IGBTs each) of the LCS-MB configuration. It has to be noted that the design aspects are case specific (semiconductor selection, grid configuration, fault type etc.) and are hereby provided as examples of system designer considerations.

Finally, the energy absorption on the EAP path in the LCS-MB is similar to the MLB, since the fault current is the similar. As a result, the surge arresters have the same dimensioning. The advantage of MLB is that in case resizing is necessary, the cost and complexity of the task is lower, since only one EAP is used for each dc node. However, reduced lifetime of the surge arrester might be expected, as it is activated more often in MLB than in case of multiple LCS-MBs.

3.5. Conclusions

This Chapter analysed a breaker arrangement, named the Multi-Line Breaker (MLB), for the successful fault isolation in MTDC networks. The breaker can be used in dc nodes connecting multiple lines and was proven to be able to isolate faults bidirectionally in any of the interconnected lines using a single main breaker path in a unidirectional configuration. Due to the limited hardware requirements it is easy to implement using hybrid breakers as the basis for its design, while at the same time it constitutes a more cost-effective solution, especially in cases where a high number of lines is connected at the same grid node. The comparison between the proposed breaker concept and the use of hybrid breakers for each dc line, for different fault case studies, showed that the overall system dc fault response is similar and thus, the MLB is a promising alternative for the dc fault isolation.

While the proposed concept is not suggested for point-to-point connections, the MLB can be applied in all types of grid configurations, as long as there is a node in the network connecting multiple lines. The design of the breaker is highly modular with minimum control additions and can, therefore, easily accommodate the addition of future dc lines to an existing grid.

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4

DC Fault Ride-through using Full-bridge MMC

If no dc breakers are used, converters with fault-blocking capability offer an alternative to protect the grid assets from dc faults. This Chapter investigates a control structure to enhance the dc fault ride-through capability of a Full-bridge Modular Multilevel Converter (MMC) station, while ensuring a stable controlled operation as a STATCOM during dc faults without the need for fault isolation. Taking advantage of the switching states of a Full-bridge submodule, a dc current controller is proposed, which provides the dc voltage reference for the modulation when a dc fault is detected. By changing the outer controllers strategy from dc voltage or active power control to converter energy control during a fault, the decoupling of the converter operation from the dc side dynamics is realized. In this Chapter, the focus is laid on the control methodology at all times of operation and the evaluation of the STATCOM control during a fault. To this end, extensive simulations were performed on a three-terminal High Voltage Direct Current (HVDC) grid in radial configuration and a pole-to-pole dc fault case was investigated. The results showed that the ac voltage and current were controlled within limits at all times, while the Full-bridge MMC was able to provide reactive power support to the ac grid. Moreover, using the proposed control methodology, the transients at the operation transition points between STATCOM and inverter/rectifier operation were minimized and the stations were able to safely ride through the fault.

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4.1. Introduction

The dc fault characteristics, presented in Chapter 2, pose grid protection challenges which have steered research towards the design of innovative dc breaker concepts [1, 2] (see Chapter 3), as well as towards the design of different MMC submodules [3, 4], as adaptations to the main Half-bridge valve concept, with fault-blocking capability.

In case of dc faults, apart from the equipment protection, a grid needs to be designed in a way to ensure uninterrupted controllability of the MMC stations at all times. As a result, there is the need for operation isolation of the ac and the dc grid during faults. This becomes more apparent when weak grids, such as wind farms, need to be connected. In this case, it is necessary to be able to provide ac voltage support and reactive power compensation to the ac grid continuously.

Overall there are two prevalent concepts for dc fault ride-through in case of an HVDC network [5]: 1) combination of Half-bridge MMC with dc breakers; 2) Full-bridge MMC with simple mechanical disconnectors for the isolation of the dc fault part of the grid. In the first case, additional equipment, i.e. the dc breakers, need to be installed to protect the station. Unless the breaker total interruption time is lower than the dc fault travelling wave time from the fault point to to the converter station, the Half-bridge valves experience a high overcurrent and block their control operation for protection [6]. As a result, the MMC operates as a diode-bridge rectifier, losing its control capability. In the second case, no additional equipment is necessary. As soon as the fault occurs, the Full-bridge MMC is able to block the developing dc fault current in different ways, either maintaining [7, 8] or losing controllability [5, 9].

Several studies have investigated different aspects of the Full-bridge MMC response to dc faults using single stations or point-to-point HVDC connections as case studies. The coupling between capacitor voltage variation and the maximum modulation index for Full-bridge and hybrid MMC configuration was analysed in [7], while the relationship between ac/dc voltages and ac/dc side power, the arm current, as well as the capacitor voltage ripple in each submodule were investigated, in case the submodules adopt the negative voltage switching state. Moreover, in [8], the operation of different submodule topologies with fault-blocking capability was studied and a new leg capacitor energy balancing method by common-mode voltage injection was proposed. Alternate operation of the MMC arms between conducting and blocked mode when the dc voltage drops to zero, using clamp double submodules (CDSM-MMC), was proposed in [10]. However, in this case the dc current was not controlled to zero and thus, simple disconnectors could not be used for the fault isolation in case of permanent faults. Finally, a new control strategy to allow the operation of the MMC when the dc link voltage drops during different fault types was proposed in [11]. In this study the manipulation of insertion function dc bias to enable reduced dc voltage operation was presented. However, the energy balancing and STATCOM operation of the MMC during the fault were not investigated.

The main contribution of this Chapter is the proposal of a control structure of the Full-bridge MMC station to allow its operation as a quasi-STATCOM during a dc fault in an MTDC grid. Taking advantage of the four switching states it offers (positive voltage, negative voltage, bypassed and blocked), a dc current control method is proposed and explained in detail. In this way, the MMC is able to drive the dc current to zero in a controlled manner, as soon as the fault is detected, protecting the dc grid assets and enabling the dc fault isolation by means of simple mechanical disconnectors. At the same time, the MMC is able to operate as a STATCOM, in Full-bridge double-star (FB-DS) configuration, maintaining continuous control of the reactive power that it exchanges with the ac grid, providing reactive power compen-

sation and ac voltage support. Unlike previous studies [7, 8, 12, 11], this Chapter investigates the maintenance of the internal balance of the STATCOM as the most important aspect at this stage of operation. By using arm and leg energy balancing controllers, which are analytically presented hereby, the MMC stations manage to ride through the fault maintaining their energy at nominal level and limiting the transients at the transition between STATCOM and inverter/rectifier operation. Finally, as soon as the dc fault is cleared, the converters are able to resume operation at their pre-fault state, after the dc voltage is ramped up to its nominal level through the internal control operation of the MMC.

The Chapter structure is as follows: Section 4.2 presents the main characteristics of the Full-bridge MMC response during a dc fault and the proposed dc current controller is explained in detail. In Section 4.3, the developed MMC control structure is explained at the different stages of the dc fault, while Section 4.4 elaborates on the main controllers needed for the internal balance of the MMC. To verify the operation of the control, two case studies are described in Section 4.5, and the obtained results verifying the effectiveness of the proposed control structure are presented in Section 4.6. Finally, the most important findings are summarized and conclusions are drawn in Section 4.7.

4.2. Full-bridge DC Fault Operation

A Full-bridge-based MMC is primarily designed with focus on reliability. In normal operation, the Full-bridge submodules are modulated like Half-bridge submodules, with only two of the switch valves operating at each moment.

The main difference in operation appears in case of a dc fault. During a dc fault, high overcurrents develop on the dc grid. As soon as a dc fault is detected, the ac side can be isolated from the dc side by inhibiting the control operation of the submodules. Once the control operation is blocked, unlike the Half-bridge submodules, which are bypassed by the antiparallel diodes of the IGBTs or the thyristors and continue feeding the fault, the Full-bridge submodules are connected as shown in Figure 4.1. In this case, no dc fault current can circulate, as it is directed through the capacitors of the submodules, which are connected in series and in opposing polarity to the current direction. As the total series capacitor voltage is higher than the peak line-to-line voltage of the ac grid, the current drops to zero. However, the disadvantage of this method is that controllability is lost and therefore, the MMC station cannot provide support to the ac side.

The usable range of the insertion index of each arm in Half-bridge MMCs is limited to $0<n_{u,l}<1$. However, Full-bridge MMC has the capability to work in the region $-1<n_{u,l}<0$ as well, with its dc link voltage reversed [11]. Because of its structure, the Full-bridge submodule is capable of creating three voltage levels at any given moment of operation, i.e. $+v_{sm}$, 0 and $-v_{sm}$. To achieve that through modulation, two carrier signals are generated for each submodule as shown in Figure 4.2, controlling the two switch combinations (diagonal), which are switched on to produce the respective voltage level, depending on the arm current direction .

During a dc fault, it was observed that by changing the polarity of the voltage in the submodules through control of the modulation index, zero-crossings of the dc current (i_{dc}) were created. This polarity reversal is made possible through control of the dc voltage offset used to create the voltage reference signal for the modulation.

The PWM reference signals for the upper and lower arms of phase $j = a, b, c$ (v_{uj}^* and v_{lj}^*

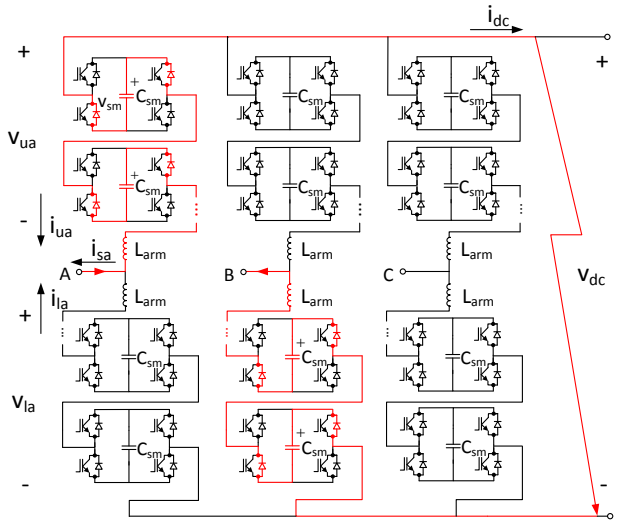

Figure 4.1: Full-bridge MMC in short-circuit dc fault [9].

respectively) are given by the following equations:

$$v_{uj}^{*} = \frac{v_{dc}^{*}}{2} - v_{sj}^{*} - v_{cj}^{*} \tag{4.1}$$

$$v_{lj}^{*} = \frac{v_{dc}^{*}}{2} + v_{sj}^{*} - v_{cj}^{*} \tag{4.2}$$

where v_{dc}^{*} is the dc voltage reference, v_{sj}^{*} is the output voltage reference and v_{cj}^{*} is the circulating voltage reference. Although, in normal operation the dc voltage is controlled by the outer dc voltage controller, during faults it can be controlled by the internal controllers of the MMC.

Hereby a controller is proposed to drive the i_{dc} to zero. In fact, the controller creates the

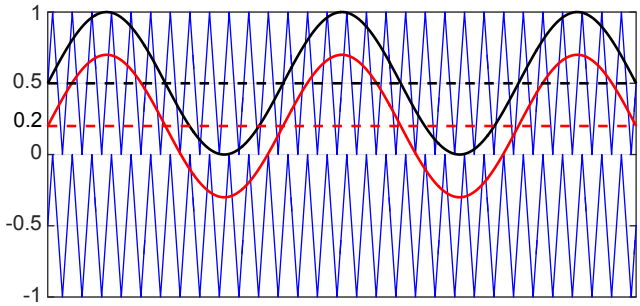

Figure 4.2: Carrier signals (blue) of one submodule and the continuous insertion index signals (black and red solid lines) at two dc voltage offset values (black and red dashed lines) for one arm.

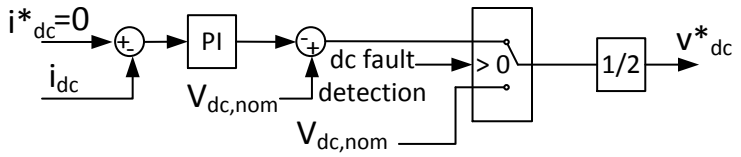

Figure 4.3: DC current controller.

dc voltage offset of the reference signal v_{dc}^{*} based on the i_{dc} measurement and is activated once the dc fault is detected. More specifically, the i_{dc} is compared to a zero reference and the error is driven through a PI controller, whose output determines the dc voltage offset. In normal operation, the dc voltage offset is set at 0.5 pu. Changing the dc voltage offset, the reference signal moves as shown in Figure 4.2 and the respective virtual v_{dc} is synthesized. Based on that observation, in case of a dc fault, the i_{dc} can also be controlled to zero by controlling the synthesized v_{dc}.

This controller needs to be fast to avoid a high overcurrent on the dc line and also on the valves, which would lead to the blocking of the control for their protection. Moreover, it needs to be accurate, as the i_{dc} needs to drop to zero before the faulty line can be successfully isolated by a common mechanical disconnector. Therefore, the tuning of the controller is made based on those two objectives. The i_{dc} controller is presented in Figure 4.3.

4.3. Control structure

In case of a dc fault, three time periods can be distinguished in the converter operation: 1) before the fault; 2) during the fault and 3) after the fault. In this Section, this chronological order is followed to explain the converter control modes and the transition between the different stages.

4.3.1. Before the fault

During normal operation the MMC is able to control either the v_{dc} or the p_{ac} through the outer controllers. Moreover, it can control the q_{ac} depending on the needs of the connected ac grid. At the same time, internally, a circulating current controller is used to suppress the second harmonic of the circulating current, while arm and energy balancing controllers ensure the internal balance of the converter. Finally, PWM modulation, in this case Phase-Shifted Carrier modulation (PSC-PWM), and a sorting algorithm are used to balance the submodule capacitor voltages, as shown in Figure 4.4.

4.3.2. During the fault

As soon as a dc fault occurs, overcurrents develop in the dc grid lines. The dc fault detection is triggered at a certain dc current threshold, usually at 2 pu [5]. If there is a short-circuit dc fault, the v_{dc} collapses to zero and the converter can no longer maintain control of the v_{dc} or p_{ac}. To avoid that the energy of the converter collapses, the following control actions need to be followed:

- First, the v_{dc} or p_{ac} control mode needs to change to converter energy (W_{conv}) control. Although the control of the v_{dc} is lost as it drops to zero, the voltage of the submodules v_c can be controlled independently. In fact, the control of the W_{conv} and the capacitor balancing algorithm which is used after the employed modulation technique, ensure

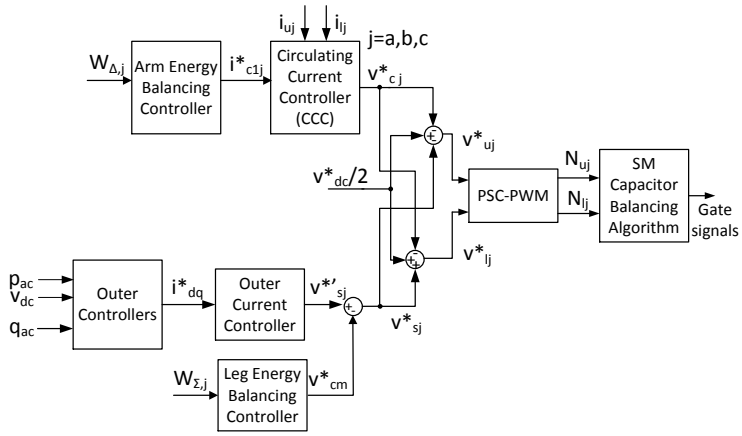

Figure 4.4: Basic Control Structure of MMC.

that the submodule capacitors remain charged at their nominal voltage level independent of the dc grid state of operation. By decoupling the dc grid voltage level from the submodule capacitor voltage levels, each arm can act as a virtual dc link even during a dc fault and thus, the MMC remains controllable [11]. In this way, the MMC is able to operate as STATCOM and provide reactive power support to the ac grid.

- Second, the i_{dc} controller described in Section 2 is necessary to drive the i_{dc} to zero and decouple the ac from dc side operation.
- Third, the arm and leg energy controllers are necessary for STATCOM operation and are explained in Section 4.

The control structure during STATCOM operation is shown in Figure 4.5, where the differences to the control structure employed in normal operation are highlighted.

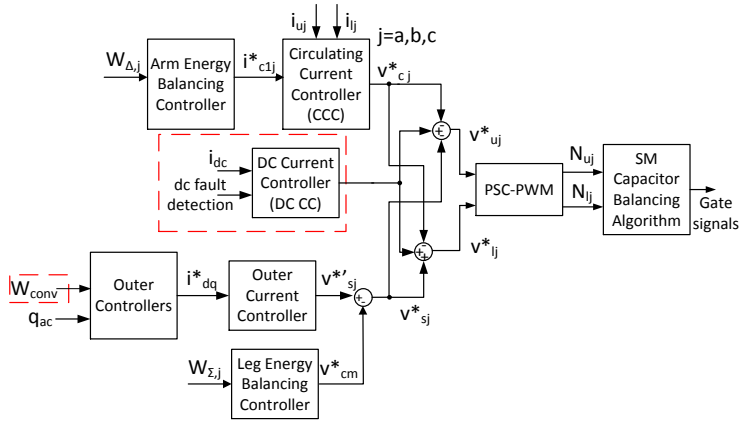

Figure 4.5: Control Structure of MMC in STATCOM operation.

4.3.3. After the fault

After the i_{dc} is brought to zero, simple mechanical disconnectors can be used to isolate the faulty line. However, if the MMC station is only connected to the grid through the faulty line segment, it cannot resume operation in the dc grid, until the line has been replaced. As a result, it is important that it keeps its controllability in order to continue supporting the ac grid. For the 'healthy' part of the grid, the MMCs need to return to their normal pre-fault operation control. This transition is made by slowly ramping up the v_{dc} level energising the dc grid lines, before active power can be exchanged. In this study, a rate of rise of 0.5 pu/1 ms was used.

4.4. Energy Balancing Controllers

The converter energy balancing is essential for the MMC, especially for STATCOM operation [13], not only for internal parameter mismatches, but mainly in case of ac and dc contingency cases which can create imbalances between the arms and legs of the MMC. For this purpose, two controllers are described hereby, which ensure the decoupled leg and arm energy balancing.

4.4.1. Leg Energy Balancing Controller

The leg energy balancing controller ensures that the total energy in the converter is equally distributed between its legs. From the mathematical analysis of the MMC operation, it can be deduced that the upper and lower arm power for phase $j = a, b, c$ are expressed as [13, 14]:

$$p_{uj} = i_{cj}\frac{v_{dc}}{2} - i_{cj}v_j + \frac{i_{sj}}{2}\frac{v_{dc}}{2} - \frac{i_{sj}}{2}v_j \tag{4.3}$$

$$p_{lj} = i_{cj}\frac{v_{dc}}{2} + i_{cj}v_j - \frac{i_{sj}}{2}\frac{v_{dc}}{2} - \frac{i_{sj}}{2}v_j \tag{4.4}$$

where i_{cj} is the circulating current in phase j, v_{dc} is the dc voltage, v_j is the phase j grid voltage and i_{sj} is the phase j output current.

From the sum of the arm power terms, the derivative of the phase j leg energy sum is calculated as follows, neglecting the oscillating terms:

$$\frac{\partial W_{\Sigma,j}}{\partial t} = i_{c0j}v_{dc} - \hat{v}_{sj}\hat{i}_{sj}cos(\phi_{ij}) \tag{4.5}$$

where i_{c0j} is the dc component of the circulating current in phase j, v_{sj} is the output voltage of phase j and ϕ_{ij} is the phase angle of the output current vector in phase j.

Usually, the dc component of the circulating current i_{c0j} is controlled to exchange active power between the converter legs. However, in case of a short-circuit dc fault, v^*_{dc} drops to zero driving the dc current to zero and thus, the first term of (5.1) is zero. Therefore, an adjustment to the $v^{*'}_{sj}$, which comes from the outer controllers, is needed to achieve leg energy balancing.

In [8], a method is proposed in which by controlling the common-mode voltage (CMV), the leg energies can be balanced. More specifically, the CMV in an MMC can be expressed as [15]:

$$v_{cm} = \frac{1}{6}\sum_{j\,=\,a,b,c}(v_{lj} - v_{uj}) \tag{4.6}$$

To get the reference for the CMV, each leg's energy is controlled to 1/3 of the total converter energy at each moment of operation using a PI controller. This gives a reference signal $p_{\mathrm{j}}^{\Sigma *}$, which is the sum of the active power that flows into upper and lower arm of each leg of the three-phase converter. The resulting $p_{\mathrm{j}}^{\Sigma *}$ is then tranformed into dq reference frame.

The reference for the CMV is given by [8]:

$$v_{\mathrm{cm}}^{*} = \mathrm{Re}\left\{ \frac{p_{\mathrm{d}}^{\Sigma *} + j p_{\mathrm{q}}^{\Sigma *}}{\frac{1}{2}(i_{\mathrm{ds}} + j i_{\mathrm{qs}})} \right\} \tag{4.7}$$

where Re is the real part of the expression between {}, $p_{\mathrm{d}}^{\Sigma *}$ and $p_{\mathrm{q}}^{\Sigma *}$ are respectively the d and q components of the sum of powers that flow into upper and lower converter arms.

The CMV reference is subsequently subtracted from the $v_{\mathrm{sj}}^{*'}$ reference resulting in a new reference as follows:

$$v_{\mathrm{sj}}^{*} = v_{\mathrm{sj}}^{*'} - v_{\mathrm{cm}}^{*} \tag{4.8}$$

4.4.2. Arm Energy Balancing Controller

The arm energy balancing controller ensures that the total energy of each leg is equally distributed between the upper and lower arm. To achieve this, the energy difference between upper and lower arms should be controlled to zero.

The difference of the arm power terms from (4.3) and (4.4) is equal to the differential of the arm energy difference. Neglecting the oscillating terms, for phase j this can be expressed as [13, 14]:

$$\frac{\partial W_{\Delta,j}}{\partial t} = -\hat{v}_{\mathrm{sj}} \hat{i}_{\mathrm{c1j}} cos(\phi_{\mathrm{cj}}) \tag{4.9}$$

where $\hat{i}_{\mathrm{c1j}}$ is the peak value of the first fundamental of the circulating current in phase j and ϕ_{cj} is the phase angle of the circulating current vector in phase j. Based on (5.3), it can be concluded that by controlling the injection of a fundamental component in the circulating current, active power can be exchanged between the arms of each converter leg. To achieve this, a simple PI controller is implemented.

To avoid the active power coupling between the arms of different legs, a decoupling method is used as explained in [13]. If an unbalance in phase-a is considered, an active current in phase with the voltage of phase-a should be applied, as shown in Figure 5.4. Assuming that there is no current flow to the dc side, the fundamental components of the circulating current should sum up to zero:

$$i_{\mathrm{c1a}} + i_{\mathrm{c1b}} + i_{\mathrm{c1c}} = 0 \tag{4.10}$$

To respect this condition, reactive current vectors in the other two phases are applied, as shown in Figure 5.4. The magnitude of the vectors of phase-b and phase-c to be applied is a result of basic trigonometry and the law of cosines and is estimated as $\sqrt{3}$ times smaller than the vector of phase- a.

Due to the high degree of symmetry, the results can be extended to all three phases. Therefore, using a simple PI controller, the final current references for all phases are given by the following equations [13]:

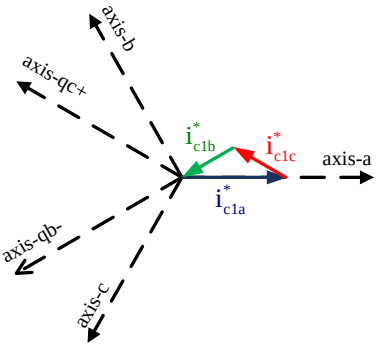

Figure 4.6: Arm energy balancing controller current vectors for decoupled operation [13].

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$$
\begin{aligned}
i^*_{c1a} &= (K_{p,arm} + K_{i,arm}\int dt)\left(e_a cos(\omega_1 t) + \frac{1}{\sqrt{3}} e_b cos(\omega_1 t + \frac{\pi}{2}) \cdots \right. \\
&\left. \cdots + \frac{1}{\sqrt{3}} e_c cos(\omega_1 t - \frac{\pi}{2})\right) \\
i^*_{c1b} &= (K_{p,arm} + K_{i,arm}\int dt)\left(e_b cos(\omega_1 t - \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} e_a cos(\omega_1 t - \frac{7\pi}{6}) \cdots \right. \\
&\left. \cdots + \frac{1}{\sqrt{3}} e_c cos(\omega_1 t - \frac{\pi}{6})\right) \\
i^*_{c1c} &= (K_{p,arm} + K_{i,arm}\int dt)\left(e_c cos(\omega_1 t + \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} e_a cos(\omega_1 t + \frac{7\pi}{6}) \cdots \right. \\
&\left. \cdots + \frac{1}{\sqrt{3}} e_b cos(\omega_1 t + \frac{\pi}{6})\right)
\end{aligned}
\tag{4.11}
$$

where e_a, e_b and e_c are the errors fed to the PI of each phase.

From the above equations, it becomes clear that an unbalance in the arm energies of phase a creates an error e_a and the controller commands the injection of a fundamental component of the circulating current in phase-a, as well as a fundamental component in the other two phases aligned with their reactive axes in order to eliminate the unbalance. It has to be noted that, since two PI controllers are cascaded (arm energy controller and circulating current controller), in order to avoid interactions between them, the energy balancing control loop is tuned with a high phase margin and a relatively small bandwidth for stability reasons (approximately 10 times lower than the bandwidth of the circulating current controller)[14].

4.5. Case Studies

To test the performance of the proposed control structure for the MMC station and the effectiveness of the fault ride-through methodology during a pole-to-pole dc

fault, two case studies were considered:

1. Case study (i): Single MMC station with a dc fault at its dc output;
2. Case study (ii): Three-terminal HVDC grid with a dc fault at the node of the radial connection.

A pole-to-pole fault, although rare, is the most severe dc fault case a dc connection can be subjected to. In this case, an almost solid pole-to-pole fault was tested with a fault resistance of 1 uΩ. The simulation models for the case studies were implemented in Matlab/Simulink.

In Case study (i) the Full-bridge MMC is subjected to a pole-to-pole dc fault at 1 m away from its dc connection point, as presented in Figure 4.7. This is the worst-case scenario for a converter station as the valves are directly subjected to high overcurrents. The dc cable on each pole is simulated as a single pi-equivalent section.

Case study (ii) includes the HVDC connection of three ac grids in radial configuration, as shown in Figure 4.8. The symmetrical monopole grid configuration is preferred as it is the most commonly used in HVDC connections. It has to be noted that the capacitors depicted at each station in Figure 4.7 and Figure 4.8 are part of

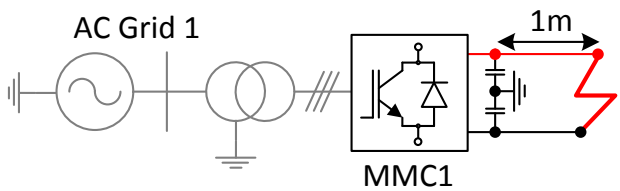

Figure 4.7: Case study (i) – MMC1 with a pole-to-pole dc fault at its dc output.

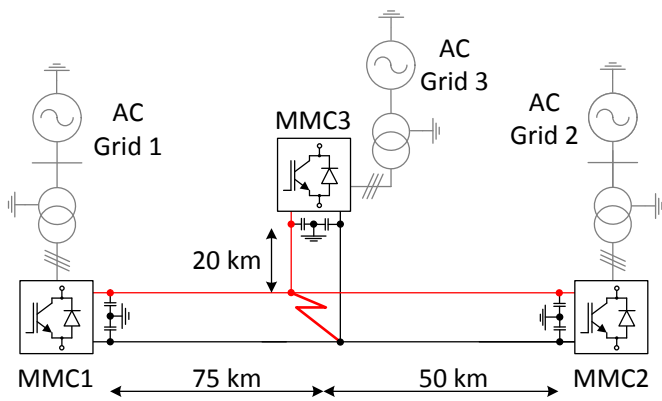

Figure 4.8: Case study (ii) – Layout of the analyzed radial MTDC network with 3 terminals.

Table 4.1: MTDC network parameters.

Network parameters	Unit	Value
MMC rated power (S_{MMC})	MVA	1200/1200/1200
MTDC voltage (V_{dc})	kV	±320
DC cable resistance (R_{cable})	Ω/km	0.0195
DC cable inductance (L_{cable})	mH/km	0.2
DC cable capacitance (C_{cable})	nF/km	220
DC cable length (d1/d2/d3)	km	75/50/20
Transformer voltage ratio	kV	380/160 (Y_0-Δ)
Transformer rated power (S_{T})	MVA	1200/1200/1200
Transformer leakage inductance (L_{T})	pu	0.05

Table 4.2: MMC simulation parameters.

MMC specifications	Unit	Value
Cell capacitance (C_{sm})	mF	5
Arm inductance (L_{arm})	mH	10
Arm resistance (R_{arm})	Ω	0.1
Number of SMs per arm (N)	-	8
Carrier frequency (f_{c})	Hz	600
Sampling frequency (f_{s})	kHz	20

the simulation pi-section model and are only shown to present the grounding points of the conductor shields.

All converter stations use Full-bridge MMC technology. The main parameters of the grid and the converter stations are summarized in Table 4.1 and Table 4.2 respectively. In normal operation, MMC1 controls the v_{dc}, while the other two stations directly control their respective p_{ac}.

4.6. Results

In this Section, the results for the two case studies are presented and the operation dynamics are explained.

4.6.1. Case Study (i):

In this case, a single MMC station, controlling the v_{dc} at its dc output, is subjected to a dc fault at a distance of 1 m. The short cable segment is used to introduce a small capacitance and a small impedance between the converter and the fault point. Table 4.3 presents the course of events.

As expected, once the dc fault occurs, the v_{dc} drops almost immediately to zero as presented in Figure 4.9(a). The high dc current is a result of the discharge of the dc cable capacitance through the fault and the voltage gradient between the

Table 4.3: Case study (i) timeline.

Time (s)	0.1	0.2	0.4
DC Fault	**Apply**	**x**	**x**
$\mathbf{q}^*_{\mathrm{ac}}$ **(pu)**	0	0.5	-0.8

equivalent leg voltage of the MMC and the fault point voltage. The fault current initially circulates through the legs of the MMC (see Figure 4.9(e)) and the ac grid does not experience high currents. As soon as the overcurrent threshold for the dc fault detection is surpassed, in this case 0.7 ms after the fault occurrence, the control changes as described in Section 3 and the dc fault current reaches its peak and stops increasing. Consequently, the i_{dc} is actively controlled below 1 pu within 8 ms and drops to zero within 19 ms, as shown in Figure 4.9(b), while the circulating current does not experience a dc offset during the fault as depicted in Figure 4.9(e).

When the fault is detected, the outer V_{dc} control strategy changes to W_{conv} control and the v^*_{dc} reference for the modulation is given by the i_{dc} controller as shown in Figure 4.9(c). The upper and lower arm voltages of each phase (v_{uj} and v_{lj}) follow the references as presented in Figure 4.9(d) for phase-a, exhibiting a fast response to the control change. An imbalance in the leg energies appears initially for 0.1 s after the fault and the effect of the CMV voltage reference on the v_{uj} and v_{lj} is evident, while trying to restore the balance. As shown in Figure 4.9(h), the leg energies manage to remain balanced during the fault, while the difference of the arm energies, presented in Figure 4.9(g), is kept at zero after the first transient. Moreover, the submodule capacitor voltages remain balanced at 1p̃u during the fault with only a short transient of ±2% at the moment of the fault. Therefore, the MMC station is able to operate as a FB-DS STATCOM. To test this operation, we apply steps in the reactive power exchange with the ac grid. It can be concluded that despite the dc fault, the dc side dynamics do not affect the ac side and therefore, the p_{ac} is kept at zero as shown in Figure 4.9(i), while Figure 4.9(j) shows that the reactive power reference (q^*_{ac}) is followed accurately. It has to be noted that at the moment of the fault the effect on the active and reactive power of the ac side is very small. This happens because the fault detection is fast and thus, the control mode change takes place before high transients are experienced on the ac side.

4.6.2. Case Study (ii):

In this case study, the response of three stations to a dc fault, their STATCOM operation during the fault and the return to normal operation post-fault are evaluated within the MTDC grid as shown in Figure 4.8. The timeline of Case study (ii) is presented in Table 4.4.

In this case, the v_{dc} at the dc output of each MMC drops slower than in case (i) because of the long HVDC lines, as shown in Figure 4.10(a). The travel time of the fault transient to the line ends depends on the LC parameters of the cables. Because of the dc cables, the fault detection occurs slower (e.g. 1.8 ms for MMC1

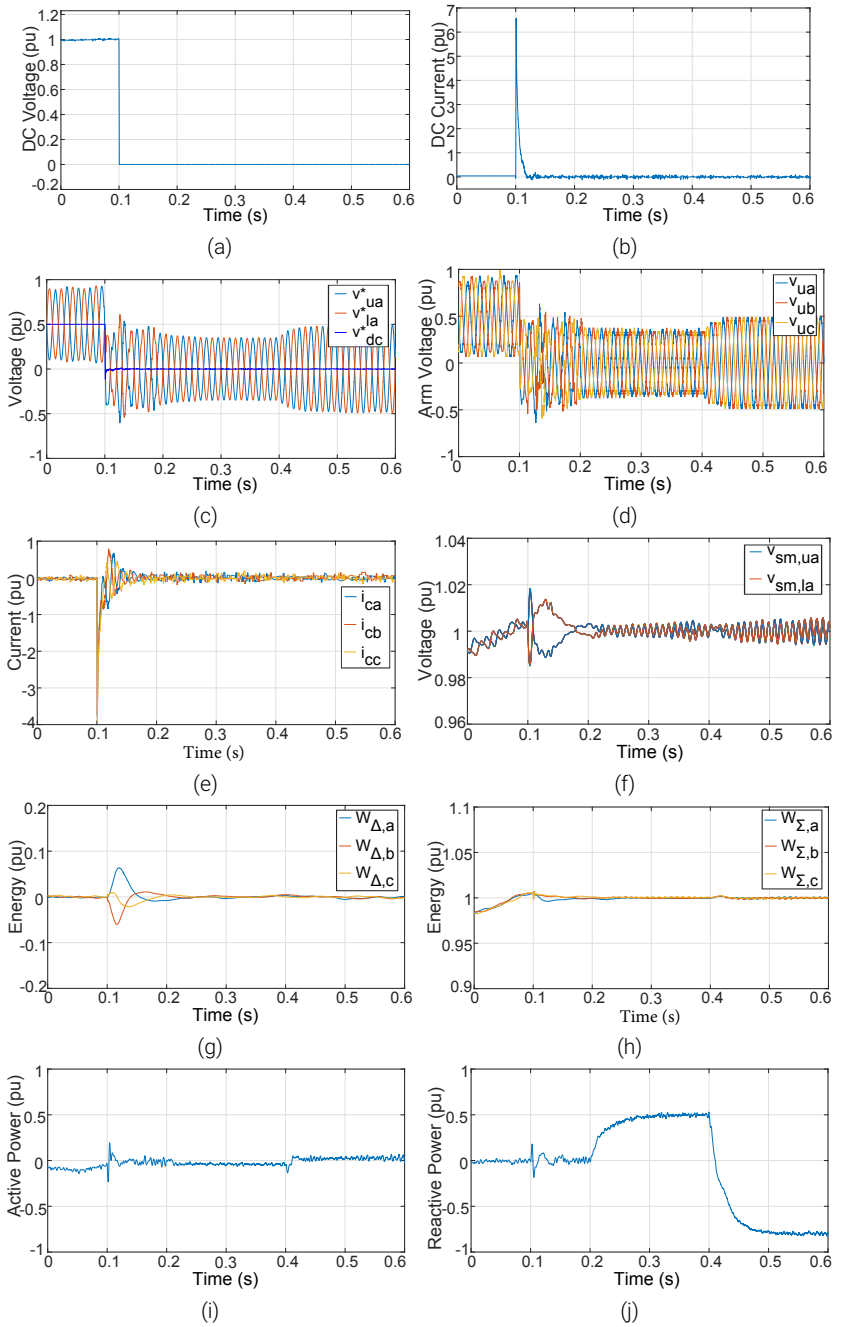

Figure 4.9: Fault operation – Case study (i): (a) DC voltage, (b) Positive pole dc current, (c) Voltage reference for modulation, (d) Upper arm voltage for phase-a, (e) Circulating current, (f) Upper and lower arm capacitor voltages for phase-a, (g) Energy difference between phase arms of MMC1 , (h) Leg energies, (i) AC active power, (j) AC reactive power.

compared to 0.7 ms in Case study (i)) and thus, the capacitors of the inserted submodules have more time than in case (i) to get discharged through the fault as shown in Figure 4.10(f). Moreover, the cable inductance affects the rate of rise of the fault current, while the added series RL impedance affects the peak fault current experienced at the dc output of each station. The dc current as measured at each MMC station is depicted in Figure 4.10(b). The highest i_{dc} peak is experienced at MMC3 which is located closer to the fault and for this reason the i_{dc} takes more time to drop to zero. The i_{dc} drops below 1 pu within 13 ms and to zero within 22 ms for all terminals, depending on the distance from the fault point.

The peak of the circulating current occurs at the same time as the peak of the dc current (3.3 ms after the fault for MMC1) (see Figure 4.10(e)). However, the ac side is not affected yet by the dc fault, as the fault current only circulates through the legs of the MMC. Once the dc fault is detected the control changes to STATCOM operation. The reference for the upper and lower arms of phase-a of MMC1 as well as the upper arm voltages of MMC1 are presented in Figure 4.10(c) and (d) respectively. The transient effect of the CMV voltage reference on the v_{uj} and v_{lj} is evident for 0.2 s after the fault occurrence in this case study, while the converter is trying to balance the leg energies. While the outer energy controller makes sure that the MMC energy remains constant, the arm and leg energy balancing controllers also make sure to keep the difference of the arm energies at zero and the leg energies at the nominal level as shown in Figure 4.10(g) and (h) respectively.

Because of the initial discharge of the capacitors, more current is necessary to increase the submodules energy to the nominal level and thus, a peak in the p_{ac} is observed at 5.5 ms after the fault (see Figure 4.10(i)). During the dc fault, the p_{ac} is maintained at zero in all MMC stations in Figure 4.10(i), while the q^*_{ac} (both positive and negative) is followed accurately in Figure 4.10(j). Based on this result, it can be concluded that the Full-bridge MMC is able to operate as STATCOM during a dc fault without the need to isolate the faulty line.

Assuming that the dc fault is cleared at 0.7 s, a control signal is sent to the stations and the v_{dc} is ramped up to its nominal level using a rate of rise limiter of the dc voltage reference (in this case study it was set at 0.5 pu/1 ms). In this way, overshoot of voltage is avoided, while at the same time the inrush dc current to the discharged dc cables is kept low. Once v_{dc} is restored, the stations return to their pre-fault control structure (MMC1 uses V_{dc} control, while MMC2 and MMC3 control

Table 4.4: Case study (ii) timeline.

Time (s)	0.1	0.3	0.5	0.7
DC Fault	**Apply**	**x**	**x**	**Clear**
MMC1 $\mathbf{q}^*_{\text{ac}}$ (pu)	0	0.7	-0.6	-0.6
MMC2 $\mathbf{q}^*_{\text{ac}}$ (pu)	0	0.3	-0.4	-0.4
MMC3 $\mathbf{q}^*_{\text{ac}}$ (pu)	0	0.5	-0.8	-0.8

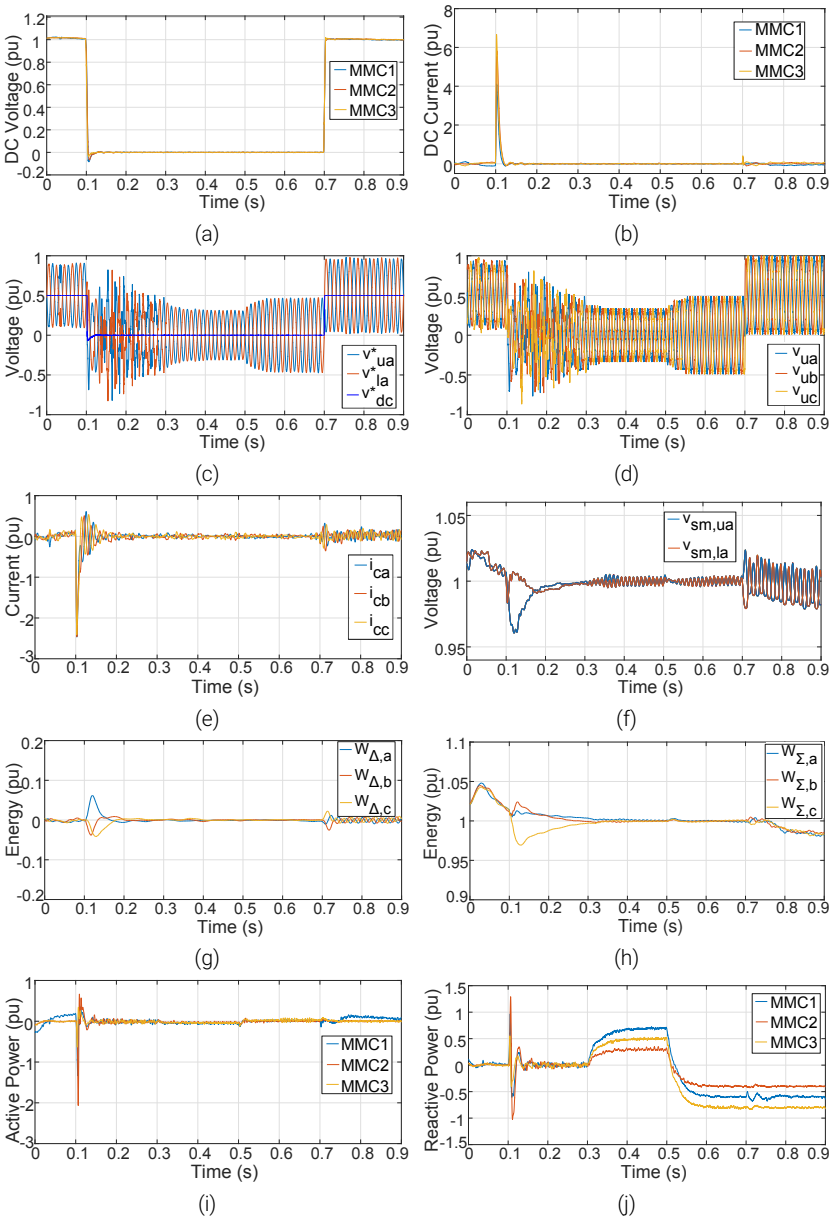

Figure 4.10: Fault operation – Case study (ii): (a) DC voltage, (b) Positive pole dc current, (c) Voltage reference for modulation at MMC1, (d) Upper arm voltage for phase-a of MMC1, (e) Circulating current of MMC1, (f) Upper and lower arm capacitor voltages for phase-a of MMC1, (g) Energy difference between phase arms of MMC1, (h) Leg energies of MMC1, (i) AC active power, (j) AC reactive power.

P_{ac}). The smooth transition to the new operating level is made sure by resetting the PI controllers.

The p_{ac} and the i_{dc} of MMC1 slightly increase post-fault, as it is the only station that is not actively controlling its p_{ac} and therefore, it is responsible to re-energize the dc cables post-fault and maintain the grid at its nominal voltage level. It has to be highlighted that each station is able to keep the control of the q_{ac} post-fault at the reference level it was operating during the dc fault. As a result, the reactive power support of the respective ac grid is not affected by the restoration process.

4.7. Conclusions

This Chapter presented a control structure to enhance the dc fault ride-through capability of a Full-bridge MMC, while operating as a STATCOM towards the respective ac grid, without the need to isolate the faulty line. During a dc fault the outer controllers change their control objective trying to maintain the MMC energy constant at nominal level. To achieve that the ac and MMC internal dynamics are also decoupled from the dc side using a controller to drive the dc current to zero.

The effectiveness of the proposed methodology was demonstrated using two case studies. In the first case, an MMC station was tested with a pole-to-pole dc fault at its dc output. Despite the severe fault and the high initial circulating currents, the MMC maintained controllability and was able to bring the dc fault current below the nominal 1 pu limit within 8 ms, while the ac side did not experience high transient currents. In the second case, more attention was paid on the HVDC grid response to the fault and on the post-fault grid recovery. In this case the fault detection at each station depended on the distance from the fault point. As a result, a network-based dc fault detection method would be recommended to detect the fault faster. The results showed that all stations were able to operate as STATCOM providing support to their respective ac grid, while they maintained their internal energy balance and the dc current was controlled to zero. Post-fault the dc voltage was ramped up to its nominal level within 2 ms using the dc current controller with a rate of rise limiter to ensure the smooth re-energization of the dc lines and to avoid high inrush dc currents and dc voltage overshoot. Overall, the main challenge is the control response at the transition moments between STATCOM and inverter/rectifier operation, i.e. when the fault is detected and when it is cleared. At these moments, the control of the MMC stations should be coordinated to maintain grid stability.

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Low-Voltage-Ride-Through of the MMC

Once a Modular Multilevel Converter (MMC) station is disconnected from the HVdc grid for dc fault clearance, it can continue operation as a Static Synchronous Compensator (STATCOM). In fact, in power systems, grid faults are common and can have a severe impact on the operation of the converters in the system. In this Chapter, the operation of an MMC-based STATCOM is investigated during grid faults. The study focuses on the challenging internal control of the converter to allow the independent control of the energy levels of each arm, with the goal to maintain internal balancing of the MMC during contingencies. Extensive experimental results highlight the need for a sophisticated internal control. Moreover, the experimental analysis verifies that, by using the proposed control structure, the MMC can effectively ride through a fault on the AC side without tripping, while injecting the necessary positive and negative sequence reactive current levels according to the most recent grid codes.

■ G. Tsolaridis, E. Kontos, S. K. Chaudhary, P. Bauer, and R. Teodorescu, "Internal Balance during Low-Voltage-Ride-Through of the Modular Multilevel Converter STATCOM," Energies, vol. 10, no. 7, 2017.

5.1. Introduction

Static Synchronous Compensators (STATCOMs) are used in applications where fast dynamic reactive current injection is needed. Mitigation of fast voltage variations due to grid faults or compensation of disturbances produced by rapidly varying loads, like arc furnaces, are conventional applications where STATCOMs are used [1].

Recently, the Multilevel Modular Converter (MMC) technology [2, 3, 4] has successfully replaced the conventional two-level topology in Medium- and High-Voltage DC (MVdc and HVdc) applications due to its superior performance in terms of efficiency, injected voltage harmonics, environmental footprint, modularity and fault tolerance. The topology with Full-Bridge (FB) submodules in Delta connection (FB-D) [5, 6, 7, 8] is well suited for STATCOM applications, as it allows the handling of positive and negative sequence current at the same time with a smaller initial cost [9]. Additionally, other proposals such as the FB submodules in Double-Star connection (FB-DS) have been reported [10, 11, 12]. However, the high number of power devices reduces the topology practicability.

Another attractive STATCOM configuration is the Double-Star (DS) topology of the MMC using Half-Bridge (HB) submodules [13, 14]. The DS-MMC was proven to be superior against the FB-D when the focus is laid on negative sequence current injection [15]. Nevertheless, high power quality is a major concern nowadays with the grid codes requiring efficient control of both positive-sequence and negative-sequence reactive current in a droop fashion as described in [16].

In an MMC-based STATCOM, the energy balancing within the converter is of utmost importance for its proper operation. Apart from the control of the total energy stored in the MMC [17], many studies have focused on the development of the decoupled leg and arm energy controllers to ensure internal balance both in the case of unavoidable internal parameter mismatches and most importantly for grid disturbances. More specifically, in [18], each arm capacitor voltage is controlled independently by applying a decoupling transformation of the quadratic voltages to define four power components, each one controlled by one current component. In other studies, it has been extensively shown that the DC component of the circulating current can be used to distribute power among the phase legs of the converter, thus achieving leg energy balancing, while the fundamental frequency component of the circulating current is responsible for exchanging power between the upper and lower arm of each phase leg [19, 20, 21, 22, 23, 24].

Based on this finding, a method was proposed in which one controller regulates the sum of the upper and lower arm stored energies, while a second controller regulates the difference between them [19]. This control approach can be carried out either using phase coordinates in a nonrotating reference frame [19] or by using a Decoupled Double Synchronous Reference Frame (DDSRF) current control technique to independently control the differential current active and reactive components separated into harmonics and sequences [25]. Moreover, to improve the dynamics of the energy balancing, feed-forward terms of the predicted components

can be used [26].

Although the energy balancing between legs is straightforward, the arm balancing is a more complicated task. As first noted in [27], the injection of current in one arm will inevitably affect the energy levels of the arms of the other two phases if no action is taken. The main idea of the decoupled arm energy balancing controller is the injection of active current in the unbalanced phase and reactive currents in the balanced phases so that the total average energy difference remains unaffected. However, the complexity of the solution in [27] is relatively high. More specifically, state-feedback control was employed for arm balancing. Apart from that, Linear-Quadratic Regulator (LQR) design was used to optimize the tuning of the state-feedback controller using the discretized state-space representation of the system in [27]. The method is known to provide very good response. However, it is usually employed along with a state observer, which increases the implementation effort and requires a precise model of the system, in order to operate as designed.

The same control idea has been extensively used in the literature for different MMC applications. In [28], the same approach is used for energy storage systems, where the MMC submodule capacitors are replaced by batteries. Compared to the capacitors, the batteries give higher flexibility in operation due to the higher available power in the converter. Moreover, this study does not consider AC grid unbalances, and the proof-of-concept is given only using simulations. In [29], where batteries are also used, the average State Of Charge (SOC) of the battery modules is used as a reference for the PI controller to change the power distribution of the three phases, and leg energy balancing is achieved through Zero-sequence Voltage Injection (ZVI). A hybrid power approach is used similar to the one proposed in [27], along with DC component Voltage Redistribution (DVR), fundamental current injection and ZVI, which complicate the control structure and its implementation and tuning procedure.

In the present study, a more intuitive method is used to decouple the arm energy controller, based on the idea introduced in [27], using PI controllers that are more easily implemented. The hereby used approach is very similar to the one implemented in [23, 30, 31], as well as to [32], in which negative sequence circulating current injection is used for the arm energy balancing. However, compared to the present study, these studies lack experimental verification. Moreover, many studies consider balanced AC grid conditions, neglecting the negative impact of AC faults on the MMC balancing, which is crucial especially in STATCOM applications [32, 33]. Furthermore, [31] presents a control method for leg energy balancing, which requires manipulation of the negative sequence of the grid current, and thus, this method cannot comply with the LVRT requirements as defined by recent grid codes [34].

The main contribution of the Chapter is the investigation, implementation and verification of a simple control method, solely based on PI controllers, for internal balancing of an MMC-STATCOM under unbalanced grid conditions, while at the same time Low-Voltage Ride-Through (LVRT) is provided according to the most

recent grid codes [34]. Unlike previous studies, this study focuses on the proof-of-concept of the control method using extensive experimental results of the MMC operation for different cases of AC contingencies, which are considered crucial in such studies, since simulation studies are based on average models, neglecting the non-linear effects of the modulation and the relative delays of the closed loop systems. For this purpose, a DS-MMC STATCOM laboratory set-up was developed. The laboratory configuration under investigation is presented in Figure 5.1. An AC controllable source, emulating the AC grid, was used to create the voltage sags. Only asymmetrical voltage sags at different voltage levels on phase-a and phase-b were investigated. Although the faults are indicated in Figure 5.1 as solid connections through switches to the ground, in the performed tests, the voltage sags were created by controlling the AC voltage output of the source.

In Section 5.2, the control system is theoretically presented with the focus laid on the internal controllers. In Section 5.3, the internal control scheme is experimentally validated. In Section 5.4, the internal energy balancing of the converter during LVRT is experimentally assessed under different case scenarios. The importance of the internal control scheme is highlighted compared to the uncontrolled case. Finally, Section 5.5 summarizes the main outcomes of the presented work.

5.2. Internal Control System

An overview of the control system of the MMC can be seen in Figure 5.2. The outer controllers of an MMC do not differ from those of a conventional two-level converter, and thus, they are not further described. This section focuses on the internal

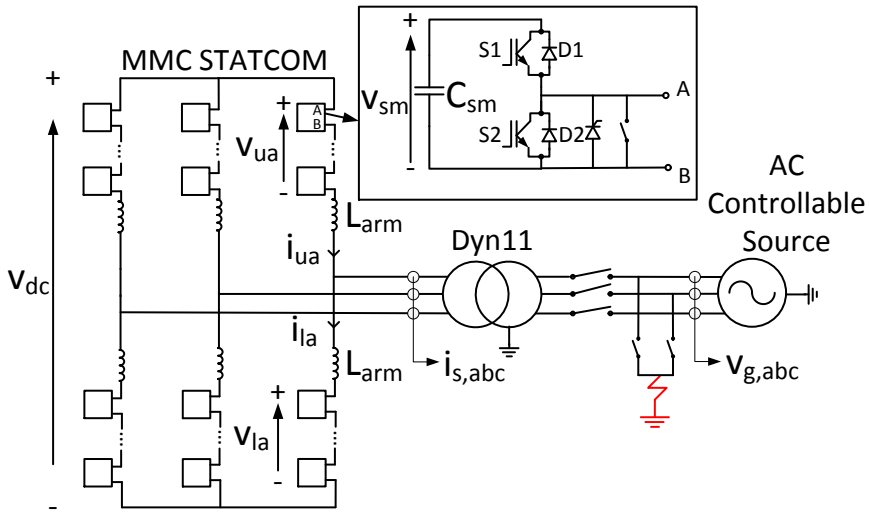

Figure 5.1: Modular Multilevel Converter (MMC)-based Static Synchronous Compensator (STATCOM) connection.

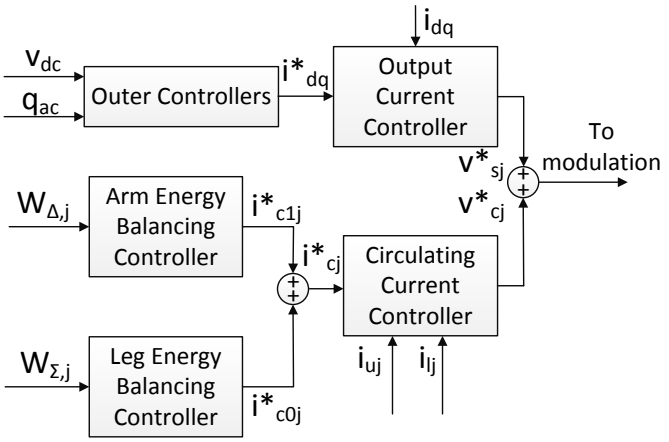

Figure 5.2: Overview of the MMC STATCOM control system.

control of the MMC, which is unique in the MMC topology.

The experimental setup parameters, which were also used for the simulations in this section, are shown in Table 5.1. It should be pointed out that the definition of the plant function is crucial for the control design procedure. Given the plant function and taking into account the system parameters and the associated delays, the tuning of the PI controllers can be performed for each system following the fundamental rules of cascaded linear controllers.

5.2.1. Leg Energy Balancing Controller

The leg energy balancing controller controls the total stored energy in the converter's legs. If this is shared equally among the legs, all of the capacitors are charged up to the same voltage level. Using the mathematical equations that describe the upper and lower arm power and neglecting the resulting oscillating terms, the average total energy in one leg is given by (5.1):

Table 5.1: Parameters of the MMC STATCOM setup.

Description	Symbol	Value
Max Tested Power (kVA)	S	1.25
Max Tested Phase RMS Voltage (V)	V_g	150
Rated DC Voltage (V)	V_{dc}	300
Submodule's Capacitance (mF)	C_{sm}	3.6
Arm Inductance (mH)	L_{arm}	20
Number of Submodules per arm	N	4
Transformer Turns Ratio	n	1:$\sqrt{3}$

$$\frac{\partial W_{\Sigma,j}}{\partial t} = i_{c0j} v_{dc} - \hat{v}_{sj} \hat{i}_{sj} cos(\phi_{i,j}) \tag{5.1}$$

where subscript j indicates the phase, i_{c0j} is the dc component of the circulating current in phase j, v_{dc} is the pole-to-pole voltage, $\hat{v}_{sj}$ is the peak voltage that drives the output current i_{sj} in phase j and $\phi_{i,j}$ is the angle of the current vector in phase j. Equation (5.1) reveals that the DC component of the circulating current is responsible for exchanging active power between the converter legs, since the second term of (5.1) is zero in an STATCOM application. Based on this finding, a PI controller is introduced to provide the reference for the desired energy sum [35]. The reference is usually set by (5.2):

$$W^*_{\Sigma,j} = 2N \frac{1}{2} C_{\text{sm}} V^2_{\text{sm}} \tag{5.2}$$

The closed loop system used for tuning the leg energy controller is shown in Figure 5.3. The Laplace transformation of (5.1) gives directly the plant function of the loop. The PI controller is then tuned to achieve a closed loop bandwidth that gives the desired 30-ms rise time, relatively slow in comparison with the inner circulating current shown in Figure 5.2. Despite the existence of an integrator in the calculation of W_Σ from (5.1), the leg energy controller uses an integral part to eliminate expected static errors in the average energy level [19].

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5.2.2. Decoupled Arm Energy Balancing Controller

The arm energy balancing controller ensures a balanced operation between the upper and lower arm of each leg by controlling the total energy stored in each of them. If the circulating current is assumed to be the superposition of a DC component and a fundamental frequency component, the energy difference between the arms can be expressed as:

$$\frac{\partial W_{\Delta,j}}{\partial t} = -\hat{v}_{sj} \hat{i}_{c1j} cos(\phi_{c,j}) \tag{5.3}$$

where $\hat{i}_{c1j}$ is the peak value of the first fundamental injected circulating current in phase j and $\phi_{c,j}$ is its phase angle of the circulating current in phase j. Based on (5.3) and as noted in [22], the fundamental component of the circulating current is responsible for exchanging active power between the converter's arms. The arm

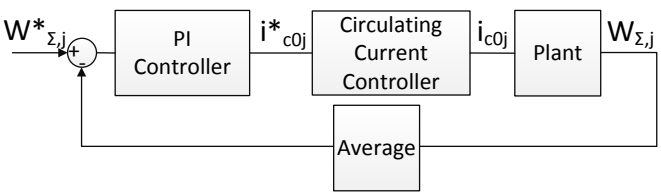


Figure 5.3: Leg energy balancing closed loop control system.

energy controller can be implemented using a PI controller with a similar bandwidth as the leg energy controller [21].

In this Chapter, a comprehensive and intuitive method is implemented to decouple the arm energy controller based on the idea introduced in [27]. Hereby, only an unbalance in phase-a is considered in Figure 5.4, but the result is valid for the other phases, as well, due to the high degree of symmetry. Due to the double-star topology of the MMC STATCOM with the absence of a physical DC-link, the sum of the vectors of the circulating currents of all phases naturally sums up to zero:

$$i_{c1a} + i_{c1b} + i_{c1c} = 0 \tag{5.4}$$

As a result, an injection of fundamental circulating current in one arm of the MMC phase leg would unavoidably couple with the other phases of the converter, if no further action is taken. To achieve a decoupled control, the main idea of this implementation is the injection of active current in the unbalanced phase and reactive currents in the balanced phases so that the average of the capacitor voltages is not shifted, and thus, the total average energy difference remains unaffected. In this example, since phase-a is unbalanced, an active current (in phase with the voltage of phase-a) should be applied as shown in Figure 5.4. The reactive currents of phase-b and phase-c could be combined to form a vector that is opposite the active vector of phase-a, as shown in Figure 5.4. The magnitude of the vectors to be applied can be determined based on the law of cosines and basic trigonometry. Therefore, the amplitude of the vectors of phase-b and phase-c are $\sqrt{3}$-times smaller than the vector of phase-a. In Figure 5.4, axis-qb- is denoted as the reactive axis of phase-b in the anti-clockwise direction. Similarly, axis-qc+ is the reactive axis of phase-c in the clockwise direction.

If a PI controller is used with a gain $K_{p,arm}$ and a small integral gain $K_{i,arm}$, while e_a, e_b and e_c are the errors fed to the controller, the final commanded current reference for all phases is given by the following Equation (5.3). If there is an unbalance between the energies of the upper and lower arm of a phase leg j then $e_j \neq 0$, while if

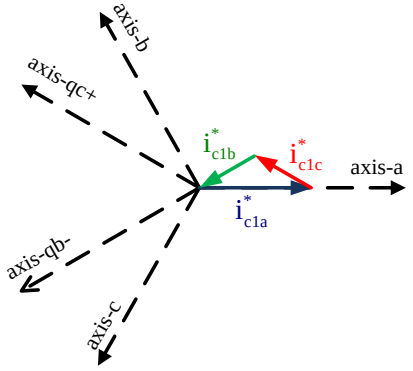


Figure 5.4: Arm energy balancing controller current vectors for decoupled operation.

balanced, $e_j = 0$. In this example, $e_a \neq 0$, while $e_b, e_c = 0$. It should be clear from (5.3) that a possible unbalance in, e.g., phase-a produces an error e_a and the need for a fundamental component of the circulating current in phase-a (first term of the first equation). At the same time, a fundamental component in phase-b and phase-c is also commanded by the error e_a, aligned with the respective phase-reactive axes in positive sequence as shown in Figure 5.4 (second term of the second and third expression) to create a vectorial triangle that will cancel out the unbalance.

$$
\begin{aligned}
i^*_{c1a} &= (K_{p,arm} + K_{i,arm}\int dt)\left(e_a cos(\omega_1 t) + \frac{1}{\sqrt{3}} e_b cos(\omega_1 t + \frac{\pi}{2}) \cdots \right. \\
&\left. \cdots + \frac{1}{\sqrt{3}} e_c cos(\omega_1 t - \frac{\pi}{2})\right) \\
i^*_{c1b} &= (K_{p,arm} + K_{i,arm}\int dt)\left(e_b cos(\omega_1 t - \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} e_a cos(\omega_1 t - \frac{7\pi}{6}) \cdots \right. \\
&\left. \cdots + \frac{1}{\sqrt{3}} e_c cos(\omega_1 t - \frac{\pi}{6})\right) \\
i^*_{c1c} &= (K_{p,arm} + K_{i,arm}\int dt)\left(e_c\ cos(\omega_1 t + \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} e_a cos(\omega_1 t + \frac{7\pi}{6}) \cdots \right. \\
&\left. \cdots + \frac{1}{\sqrt{3}} e_b cos(\omega_1 t + \frac{\pi}{6})\right)
\end{aligned}
\tag{5.5}
$$

Note: The reactive axes of phase-a are at $+\frac{\pi}{2}$ and $-\frac{\pi}{2}$; the reactive axes of phase-b are at $-\frac{7\pi}{6}$ and $-\frac{\pi}{6}$; the reactive axes of phase-c are at $+\frac{7\pi}{6}$ and $+\frac{\pi}{6}$.

For simplification reasons and for lower computational effort in the calculation of the references of the circulating current fundamental component, the authors assume that the positive sequence voltage is significantly larger in magnitude than the negative sequence voltage, which is the case in most AC faults, as the experiments shown in Section 5.4. In the rare case when the positive and the negative sequences have similar magnitudes [36], the simplification would result in an imperfect decoupling of the arm currents. However, this error would be dealt with by the action of the integral part of the arm energy balancing controller.

The closed loop system for tuning the arm energy balancing controller is shown in Figure 5.5. The plant function for this controller is derived by the Laplace transformation of (5.3), and the bandwidth is set appropriately in order to achieve a rise time of approximately 30 ms.

5.2.3. Circulating Current Controller

In an STATCOM application, the average circulating current is zero since there is no exchange of active power between the DC and the AC side. However, as noted in [22], the circulating current of an MMC presents naturally a second order harmonic component when the current of fundamental frequency is controlled. Apart from

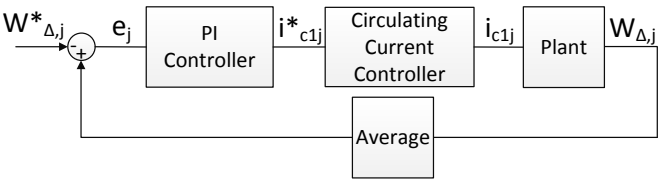


Figure 5.5: Arm energy balancing closed loop control system.

that, as noted previously, to ensure balanced operation between the legs of the MMC, the circulating current controller should be able to follow a DC, as well as a fundamental component reference.

In total, the circulating current controller needs to present high gain at 0 Hz, 50 Hz and 100 Hz. In order to achieve this, the control scheme shown in Figure 5.6 is employed, utilising resonant controllers connected in parallel and tuned at the respective frequencies. The analytical control design procedure for the circulating current controller is shown in [37].

The delay block is used to model the associated input delays, such as the Pulse Width Modulation (PWM) delay and the computational delay of the digital controller. The plant function of the circulating current controller is given by (5.6):

$$\frac{i_c}{v_c} = \frac{1}{L_{\text{arm}} s + R_{\text{arm}}} \tag{5.6}$$

The proportional gain is tuned based on the desirable bandwidth of the control system, which is imposed by the desirable rise time and is limited by the inherited delays of the control system, as shown in (5.7).

$$\frac{\ln(9)}{t_{r_{\max}}} < \omega_{bw} < \frac{\omega_s}{10} \tag{5.7}$$

where $t_{r_{\max}}$ is the maximum rise time according to the design requirements, bw is the bandwidth of the circulating current controller that is dominated by the proportional gain and ω_s is the switching angular frequency.

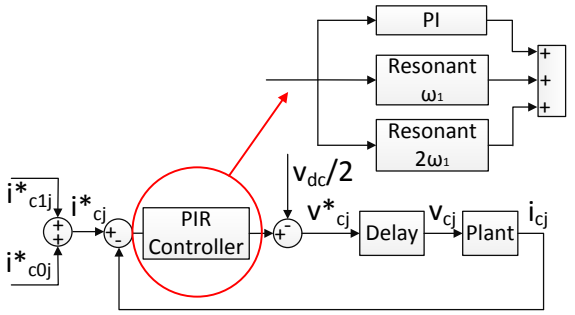


Figure 5.6: Circulating current controller.

5.3. Experimental Validation of Internal Control

Simulation results of MMC-STATCOM under different cases of grid unbalances at higher voltages have been previously presented in [37]. However, experimental verification is considered crucial to prove the validity of the proposed control scheme, considering the delays and non-linearities of the real system. This section presents experimental results that verify the validity of the previously-described control system. The current experimental work is performed in a small-scale laboratory setup, shown in Figure 2.3(a) with the specifications noted in Table 5.1. The converter is connected to an AC source through a Dyn 11 isolation transformer, and the dSPACE platform is used to implement the control scheme and record the results. The control parameters used for the experiments are presented in Table 5.2.

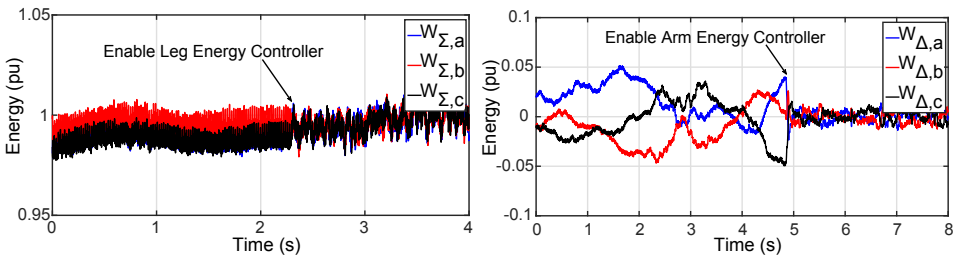
At first, the effect of the leg energy balancing controller is demonstrated in Figure 5.7(a). The parameters of the setup are similar for all phases, and therefore, only a small difference exists between the leg's sum energies. When the controller is activated, this difference is eliminated.

The controller's performance is shown in simulation and experimentally in Figure 5.8(a),(b), respectively, by applying a $+10\%$ energy step in phase-a, while phase-b and phase-c receive a -5% command. In this way, the leg energy controller causes the energy to flow out of Leg-b and Leg-c and into Leg-a. The controller is tuned for a rise time of approximately 30 ms.

The arm energy balancing controller effect is evaluated in Figure 5.7(b). Initially, the energy oscillates between the arms of each leg. After the controller activation,

Table 5.2: Control parameters of the experimental setup.

Controller	K_p	K_i	K_r
Arm Energy Controller	0.2	0.5	-
Leg Energy Controller	0.2	0.3	-
Circulating Current Controller	32.2	3.22 x 10^3	ω_1: 3.22 x 10^3 ω_2: 3.22 x 10^3
Output Current Controller	24.2	2.42 x 10^3	-



(a) (b)

Figure 5.7: Experimental effect of: (a)Leg energy controller; (b) Arm energy controller.

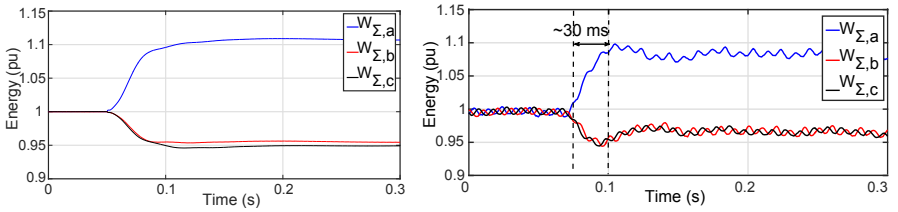


Figure 5.8: Leg energy controller step response (a) in simulation and (b) experimental performance.

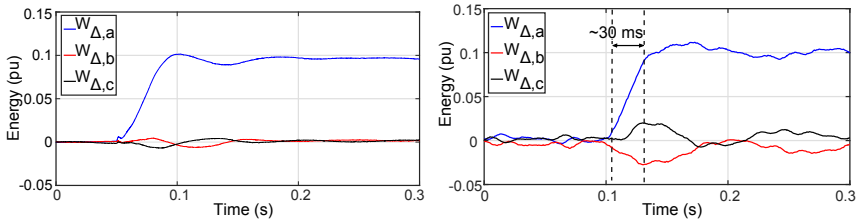


Figure 5.9: Arm energy controller step response (a) in simulation and (b) experimental performance.

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the arm energy difference remains at zero, and the stability of the converter is enhanced. In Figure 5.9(a), the step response of the arm energy balancing controller is simulated, while in Figure 5.9(b), it is demonstrated experimentally. The controller is tuned for a rise time of 30 ms, and a step change of 10% in the energy difference of the arms of phase-a is applied. The controller reacts as expected, and its decoupled performance is verified, as phase-b and phase-c are not affected by the change in the energy difference of phase-a.

5.4. Low-Voltage Ride-Through of the MMC STATCOM

Generally, under unbalanced conditions, the established instantaneous power theory [38] is applicable:

$$\begin{cases} p = P_0 + \hat{P}_1 cos(2\omega_1 t) + \hat{P}_2 sin(2\omega_1 t) \\ q = Q_0 + \hat{Q}_1 cos(2\omega_1 t) + \hat{Q}_2 sin(2\omega_1 t) \end{cases} \tag{5.8}$$

As can be observed, (5.8) contains the average terms P_0 and Q_0, as well as the oscillating terms $\hat{P}_1$, $\hat{P}_2$, $\hat{Q}_1$ and $\hat{Q}_2$. The oscillating terms are the result of the presence of the negative sequence voltage component.

Applying the dq-transformations and taking into consideration both the positive and the negative sequence components, the power terms can be written in matrix form, as shown in (5.9). From (5.9), it can be seen that there are six power terms that can be controlled and only four independent variables. Moreover, (5.9) shows that any change in the positive or negative sequence current component results in active and reactive power oscillations, as long as negative sequence voltage is

present, e.g., in asymmetrical AC faults.

$$\begin{bmatrix} P_0 \\ \hat{P}_1 \\ \hat{P}_2 \\ Q_0 \\ \hat{Q}_1 \\ \hat{Q}_2 \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix} \cdot \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix} \tag{5.9}$$

In case of faults on the AC-side, injection of positive sequence capacitive current is required to support the recovery of the Point of Common Coupling (PCC)voltage, while the injection of negative sequence inductive current supports the grid by reducing the negative sequence voltage at the PCC.

Recent grid codes suggest that when an AC fault arises, the converter should be able to avoid tripping while injecting capacitive positive sequence reactive current according to (5.10). This is usually referred to as Positive Sequence Injection Low-Voltage Ride-Through (PSI-LVRT):

$$i_q^+ = k^+(0.9 - V^+) \tag{5.10}$$

where V^+ is the positive sequence voltage vector given in pu at the PCC and k^+, which is the slope of the droop controller, usually takes values within the interval (0–10). It can be deduced that a 10% dead-band is considered in (5.10) [39].

As highlighted in [40], the injection of positive sequence current does not reduce the unbalance at the PCC, so recent grid codes require the injection of inductive negative sequence current proportional to the negative sequence voltage at the PCC, according to (5.11) [16]:

$$i_q^- = -k^-(V^- - 0.05) \tag{5.11}$$

where V^- is the negative sequence voltage vector given in pu at the PCC and k^- usually takes values within the interval (0–10). A dead-band of 5% is considered in this case. When both positive and negative sequence currents are injected, the injection strategy is commonly referred to as Mixed Sequence Injection Low-Voltage Ride-Through (MSI-LVRT).

In this section, experimental results evaluate the control structure of MMC under grid disturbances in the three test case scenarios listed below:

1. Experimental Scenario 1: 95% voltage sag in phase-a with PSI-LVRT.
2. Experimental Scenario 2: 95% voltage sag in phase-a with MSI-LVRT.
3. Experimental Scenario 3: 95% voltage sag in phase-a and 50% voltage sag in phase-b with PSI-LVRT.

The tested voltage sags were applied by defining the voltage level, the start time and the duration of the sag at the respective phase through the controllable AC source, as shown in Figure 5.1. In every case, experimental results evaluate the performance of the MMC STATCOM with and without the insertion of the described energy controllers. It should be noted that the control system is implemented using the dSPACE environment. The sampling frequency used in the control model of MATLAB/Simulink, which is compiled in dSPACE is 20 kHz. Due to the large number of result points obtained, downsampling was necessary for the depiction of the results in the ControlDesk of dSPACE. As a result, the data are presented in the figures of this manuscript with a sampling rate of 1 kHz. Regarding the effective frequency of a submodule, this was defined by the sorting algorithm used for the capacitor voltage balancing. This value was monitored at all times of the control operation, and it varied between 800 Hz and 1 kHz.

5.4.1. Experimental Scenario 1

In the first case scenario, an asymmetrical voltage sag occurs at the AC-side of the MMC STATCOM for 300 ms. phase-a voltage is reduced to $\mathbf{5\%}$ of its value, while phase-b and phase-c remain unaffected, as shown in Figure 5.10.

In this first scenario, only positive sequence current injection is considered, and according to (5.10) and the measured V^+, for $k^+ = 2.5$, approximately 0.6 pu capacitive reactive current is injected as shown in Figure 5.11(a). It should be noted that based on these waveforms, the current does not surpass its rated values. The peak value of the currents observed at the end of the transient are caused due to the inevitable delays in the decomposition of the voltage sequences by the phase locked loop. It is also worth noting that the injected currents of all three phases, during the transient, are symmetrical due to the PSI followed in this experimental scenario. The distortion of the currents is at the sixth harmonic and its multiples and could be associated, on the one hand, with the effect of dead-time and inverter non-linearities and, on the other hand, with a slight difference between the energies of the arms of the converter system, as shown in Figure 5.12(b). The distortion in the current before the injection could be also attributed to the same reasons.

As is depicted in (5.8) and (5.9), the presence of negative sequence voltage re-

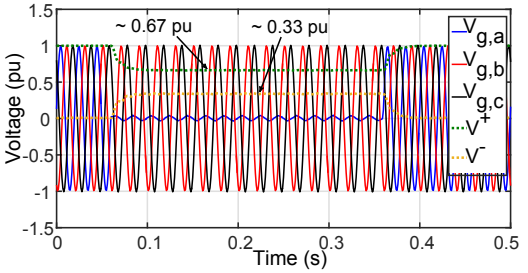
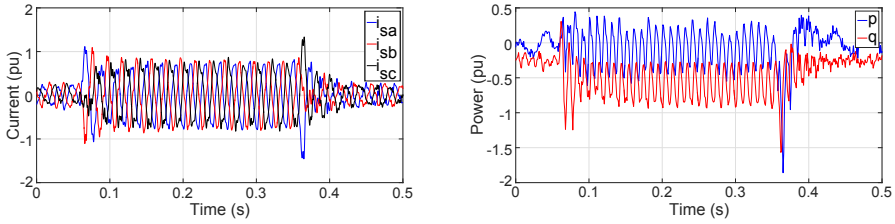
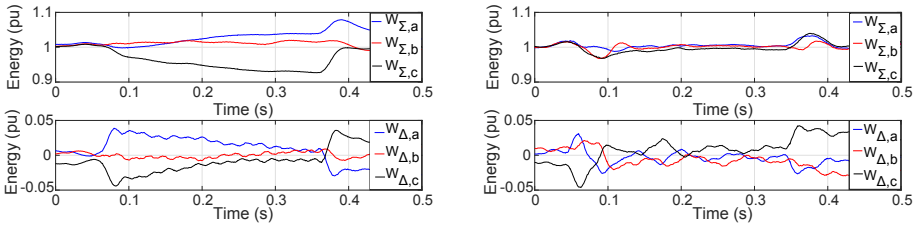


Figure 5.10: AC voltage waveforms for Experimental Scenario 1.



(a) (b)

Figure 5.11: (a) Current waveforms and (b) instantaneous p and q waveforms for Scenario 1.



(a) (b)

Figure 5.12: (a) W_Σ and W_Δ for Scenario 1 without energy controllers and (b) with energy controllers.

sults in active and reactive power oscillations. These oscillations during the voltage sag can be seen in Figure 5.11(b), where the instantaneous active and reactive powers are plotted. During the sag, the average reactive power is negative, which in this case indicates capacitive operation of the converter. Furthermore, the active and reactive power exhibit peak values when the converter returns to normal operation, mainly due to the aforementioned Phase-Locked Loop (PLL) delay in the decomposition of the voltage sequences. These peaks, however, occur for a short period of time (~10 ms) and therefore do not cause a problem in the operation of the MMC.

The internal balance of the MMC is assessed by the sum of the upper and lower arm total energies (W_Σ), as well as their difference (W_Δ), as these reflect directly on the capacitors' voltages. Firstly, in Figure 5.12a, W_Σ and W_Δ are shown for every phase, when the energy balancing controllers are not activated.

An unbalance between the converter legs can be observed in Figure 5.12(a). More particularly, phase-c delivers energy to phase-a and phase-b. In this way, the capacitors of phase-c get discharged while the ones of phase-a and phase-b get charged, which may result in converter tripping, if the fault persists. The difference of the energies between the upper and lower arm present in this case acceptable performance.

Figure 5.12(b) depicts W_Σ and W_Δ when the energy controllers are activated. The leg energy balancing controller manages to eliminate the energy differences between the converter legs and keep them equal at 1 pu. The arm energy controller exhibits an improved performance in comparison to the previous case, as it acts

quickly after the initial transient, keeping the energy levels of the upper and lower arms of each phase equal.

5.4.2. Experimental Scenario 2

In the second case scenario, the fault is identical to the one applied in the previous case, with the phase-a voltage reducing to 5% of its initial value. The resulting AC-voltage waveforms are therefore as depicted in Figure 5.10. In this case however, the MMC STATCOM will be tested for MSI-LVRT.

The positive sequence current droop controller is set again to $k^{+} = 2.5$, while the one for the negative sequence current is chosen to be $k^{-} = 1$. As a result, the required capacitive positive sequence current is again found to be approximately 0.6 pu, while the inductive negative sequence current required, according to (5.11), is 0.28 pu. The injected current waveforms are shown in Figure 5.13(a). Note that in this case, the currents are increased due to the negative sequence injection, but remain inside their rated limits. It is also evident that during the sag, the MSI strategy results in unbalanced current injection. Figure 5.13(b) shows the instantaneous active and reactive powers. Due to the increased current injection, the power oscillations increased. This result can also be explained by (5.9).

Moreover, similarly to the previous scenario, the internal balance of the converter and its ability to ride through the AC-fault without tripping is assessed hereby. Firstly, the waveforms of W_{Σ} and W_{Δ} when the energy controllers are deactivated are shown in Figure 5.14(a). In this figure, it can be seen that the leg energy of phase-

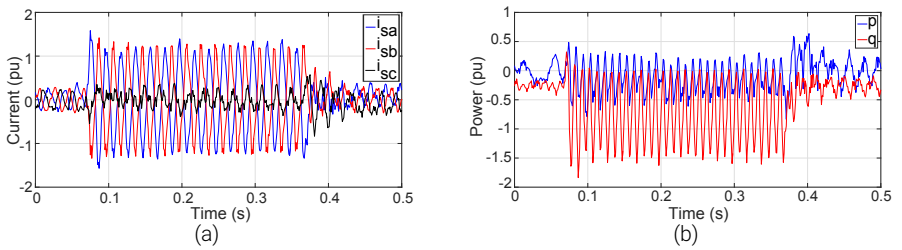


Figure 5.13: (a) Current waveforms and (b) instantaneous p and q waveforms for Scenario 2.

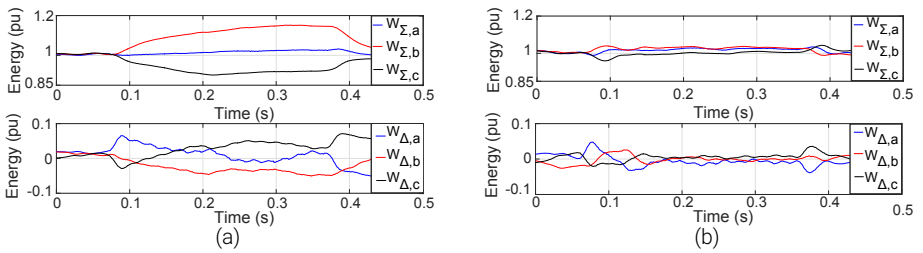


Figure 5.14: (a) W_{Σ} and W_{Δ} for Scenario 2 without energy controllers and (b) with energy controllers.

b increases unacceptably, and by the end of the voltage sag, it reaches 1.15 pu. Furthermore, an inspection of the energy difference between the arms shows that an unbalance exists between the upper and lower arm.

On the other hand, Figure 5.14(b) depicts the waveforms of W_Σ and W_Δ when the energy controllers are activated. A simple inspection of the waveforms reveals that the energy controllers manage to keep all three MMC legs, as well as their arms balanced after an initial transient. This operation apparently ensures the safe LVRT of the converter under AC faults.

5.4.3. Experimental Scenario 3

In the final tested scenario, a more severe asymmetrical voltage sag occurs at the AC-side of the MMC STATCOM for 300 ms. phase-a voltage is reduced again to 5% of its value, and phase-b experiences a voltage sag of 50%, while phase-c remains unaffected, as shown in Figure 5.15. The applied voltage sag causes the positive sequence voltage vector to reduce to 0.5 pu as shown in Figure 5.15. This scenario considers again a PSI-LVRT and according to (5.10), the required capacitive positive sequence current for $k^+ = 2.5$ is 1 pu. The resulting current waveforms are shown in Figure 5.16(a).

Once again, due to the emergence of the negative sequence voltage vector, the instantaneous active and reactive powers will present severe oscillations that due to the high current injection are larger in comparison to the first tested scenario (see Figure 5.11(b)). Figure 5.16(b) depicts the aforementioned power waveforms. It can be noted that the average injected reactive power is 1 pu. In this figure, the active and reactive power waveforms exhibit again severe peaks that exceed 2 pu. As explained before, these peaks are the result of a delayed sequence separation and should not cause a problem in the operation of the converter system, as they appear for a very short duration.

In Figure 5.17(a), the energy controllers are deactivated. During the voltage sag, severe unbalance between the energy levels of the converter legs is noticed. At the same time, the arm voltages seem to drift away in this case. In particular, phase-b upper arm energy is increased in comparison to the lower arm, resulting in an unacceptable operation of the MMC STATCOM.

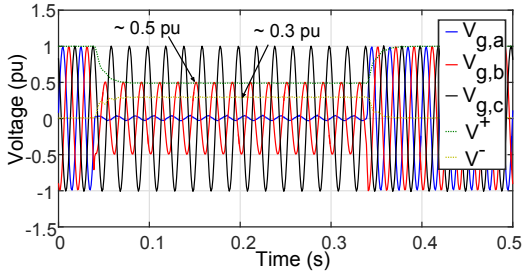


Figure 5.15: AC voltage waveforms for Experimental Scenario 3.

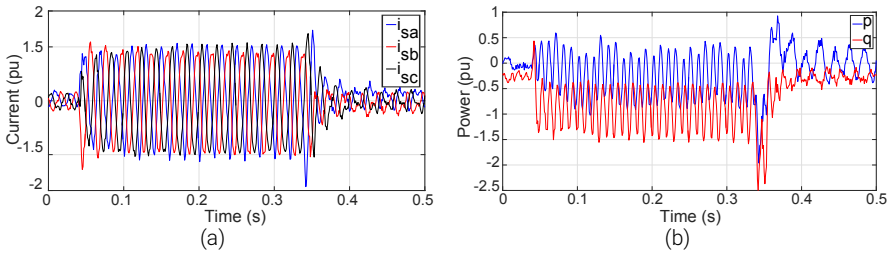


Figure 5.16: (a) Current waveforms and (b) instantaneous p and q waveforms for Scenario 3.

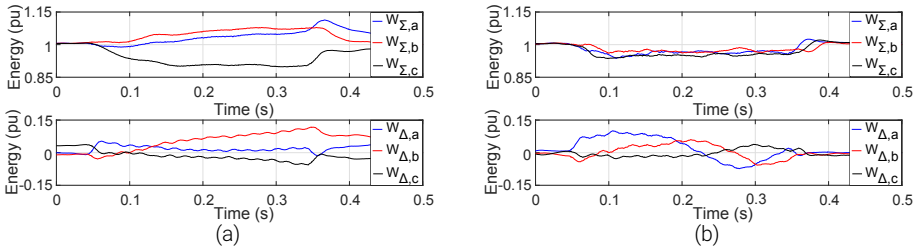


Figure 5.17: (a) W_Σ and W_Δ for Scenario 3 without energy controllers and (b) with energy controllers.

In Figure 5.17(b), the energy controllers are activated, and the improvement on the resulting energy waveforms is evident. The leg energy balancing controller acts quickly, bringing the total leg energies together and keeps each phase energy level at approximately 1 pu. The arm energy balancing controller brings the energy difference levels close to zero as expected, after an initial transient that causes unbalance between the arms, ensuring the safe LVRT of the MMC STATCOM.

5.5. Conclusions

This Chapter focused on the identified problem of internal balancing of a DS-MMC STATCOM under unbalanced grid conditions, while investigating the LVRT response of the converter. The most recent grid codes were used as the reference to determine the positive and negative output current injection values for different types of voltage sags. The chosen voltage sag scenarios were carried out experimentally, and the proposed leg and arm energy balancing controllers' performance was tested using a developed laboratory setup, taking into account all of the non-linearities of the modulation and the delays of the real system.

At first, the step response of the leg and arm energy balancing controllers was tested in normal operation. The developed controllers design simplified their implementation in the experimental setup and allowed the fast tuning of the closed-loop system. During the different tests of voltage sags, the arm and leg energies were monitored with and without the use of the energy controllers. The results showed the problem of energy balancing in case no energy controllers were used

and highlighted the improved performance of the MMC STATCOM when the energy controllers are activated. In all of the tested cases, the converter managed to ride through the fault successfully, while at the same time keeping its internal balance.

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6

High Order Harmonic Mitigation using the MMC

Apart from the presented Low-Voltage-Ride-Through capability, the Multilevel Modular Converter (MMC) offers ac grid support in various ways, independent of its connectivity to the dc grid. Due to the increase of power electronic-based loads, the maintenance of high power quality poses a challenge in modern power systems. To limit the Total Harmonic Distortion (THD) in the line voltage and currents at the Point of the Common Coupling (PCC), Active Power Filters (APF) are commonly employed. This paper investigates the use of the MMC for harmonics mitigation due to its high bandwidth compared to conventional converters. A selective harmonics detection method and a harmonics controller are implemented, while the output current controller of the MMC is tuned to selectively inject the necessary harmonic currents. Unlike previous studies, focus is laid on the experimental verification of the active filtering capability of the MMC. For this reason an MMC-based Double-Star (DS) STATCOM is developed and tested for two representative case studies, i.e. for grid currents and PCC voltage harmonics. The results verify the capability of the MMC to mitigate harmonics up to the 13^{th} *order, while maintaining a low effective switching frequency and thus, low switching losses.*

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6.1. Introduction

A major problem in modern power systems is the reduction of power quality due to the introduction of harmonic content by various power electronic-based loads. The current harmonics can cause voltage fluctuations and malfunction of electronic equipment. One of the biggest challenges of the grid operators is to keep the power quality standards high, by limiting the line voltage and currents' Total Harmonic Distortion (THD) at the Point of Common Coupling (PCC) [1].

The techniques for harmonic elimination can be divided into three main categories, i.e. passive, active and hybrid filtering [2]. The use of Passive Power Filters (PPF) is well-estab-lished, especially for low voltage systems. In this case, inductors and capacitors are tuned to mitigate specific harmonic content thereby, improving power quality. However, in medium/ high voltage systems, the size and cost of PFFs increases, while several unwanted side effects appear, such as ringing transient response and resonance [3, 4]. Moreover, PPFs have limitations such as difficulty in tuning, fixed filter frequency and resonance due to matching with line impedance [5]. As a result, active filtering topologies are investigated [4].

Active and hybrid filters are commonly used in industrial applications. An Active Power Filter (APF) is a power electronic converter designed to a fraction of the load power, which is used for harmonic filtering and is connected close to the non-linear load or at the PCC [6]. With the recent improvements in the ratings and the switching behavior of power semiconductor devices, APFs are increasingly used to overcome the PPF drawbacks [5]. APFs are able to detect the load current harmonics and generate a compensating current using an output current controller [6].

Voltage-Source Converters (VSCs) are commonly used for harmonic mitigation [7]. Moreover, conventional multilevel converter topologies such as Flying Capacitor Converter (FCC), three-level diode Neutral Point Clamped (NPC) converter and Cascaded H-Bridge converter (CHB) are used for power quality improvement in different applications. In the last decade, Modular Multilevel Converter (MMC) has been introduced for high voltage (HVDC), as well as for medium voltage (STATCOM) applications. Apart from the advantages over the conventional topologies due to its modularity and scalability, the inclusion of many submodules results in a low effective switching frequency of the submodule power semiconductor devices, while maintaining a high switching frequency of the converter, and therefore, in an increased effective control bandwidth without compromising the converter's efficiency. Using the available bandwidth in the MMC, it is possible to increase the accuracy of harmonic elimination in lower order harmonics, while at the same time being able to control higher order harmonics [8]. The aforementioned advantages make the MMC promising for APF applications [9].

Different control strategies can be used for the current and voltage harmonics compensation to improve the THD. These control strategies are based on detection of harmonics through measurement of either the load and converter currents or the grid voltage and current. Several open-loop control schemes using grid voltage feed-forward have been proposed to compensate the grid harmonic voltage [10, 11,

12, 13], but they are not sufficient to suppress line current harmonics due to dead time effect [14]. Feed-forward compensation for line current harmonics can also be implemented by first extracting the current harmonic components using high pass filters in the stationary reference frame. At medium voltage and low current, there is little margin for error and thus, feed-forward compensation schemes are not preferred, whereas feedback-based approaches are recommended [14].

When proportional-resonant (PR) controllers or PI-resonant controllers are used for harmonic compensation, two possible implementations arise. The first is to use a single frame for each n^{th} harmonic rotating at frequency $n\omega$. The second is to use nested frames. More specifically, two controllers in two frames rotating at $(n+1)\omega$ and $-(n+1)\omega$ can be implemented in the main synchronous frame [10]. Both implementations are equivalent in terms of computational burden [10] and thus, high bandwidth is necessary for the current control loops in order to have satisfactory results in the elimination of steady-state errors [14]. Additionally, predictive harmonic control has been proposed and validated in [15]. However, the controller design is demanding in terms of tuning and depends on the application. Moreover, a non-optimized design can increase the computational burden and the hardware utilization significantly.

An investigation of the performance of the MMC in the mitigation of harmonics can be found in [16, 17]. These studies consider a hybrid structure of the MMC with 'fundamental' cells, which are intended to compensate the fundamental input power factor and the 'harmonic' cells, whose number depends on the number of harmonics that need to be compensated. A PI controller and a static decoupler are used to determine the modulation of each cell, which is used to cancel a specific load current harmonic. However, in this case the MMC design becomes more complex without a significant benefit in efficiency, while redundant submodules switching at high frequencies are used, which could unnecessarily increase the cost and volume of the system. More studies have also investigated the use of MMC as APF [8, 18, 19]. However, these studies consider only average simulation models without experimental validation, which in this case is essential, since simulation studies neglect the non-linearities and delays introduced in the real system, as well as quantization errors due to the ADC interface and accuracy limitations of the sensors.

Recent grid codes require the mitigation of high order harmonics of current and voltage, which cannot be easily accomplished with conventional converters [20, 21]. This Chapter proves that even a 5-level MMC-based APF is able to mitigate such high harmonics without increasing its switching frequency and thus, its losses. Contrary to existing literature on MMC applications as APF, this is achieved through extensive experimental results, which are obtained using a developed MMC prototype in a laboratory set-up for two representative case studies, i.e. for current and voltage harmonics mitigation. More specifically, in this study the performance of the MMC STATCOM topology is evaluated in the mitigation of voltage and current harmonics at the PCC up to the 13^{th} order and the results on the THD and indi-

vidual harmonic components are compared to limits as specified by National Grid data [22]. To achieve this, a simple harmonics detection method is applied using Low-Pass Filters (LFP) in dq-frame. The voltage and current harmonics are controlled first using PI controllers, which generate the reference for the output current harmonic components and subsequently, PR controllers are used in parallel to the fundamental output current control loop of the MMC.

The Chapter is structured as follows: Section 6.2 introduces the control strategy used for the current and voltage harmonics detection and elimination and the tuning of the required filters and controllers is thoroughly explained. In Section 6.3 the laboratory set-up of the MMC STATCOM is presented. The case study and the obtained results for the current harmonics are presented in Section 6.4, while Section 6.5 presents experimental results for the voltage harmonics elimination. Section 6.6 summarizes the main conclusions drawn from the analysis.

6.2. Harmonic Mitigation Control Scheme

In this study an MMC-based STATCOM is used in Double-Star (DS) configuration with Half-bridge submodules, as shown in Figure 6.1. This configuration has been extensively studied [23, 24] and has been shown to be superior against the topology with delta-connected Full-Bridge (FB) submodules (FB-D), especially regarding negative sequence current injection [25].

The control overview of the MMC DS-STATCOM is presented in Figure 6.2. More specifically, the energy controllers and the circulating current controller follow the

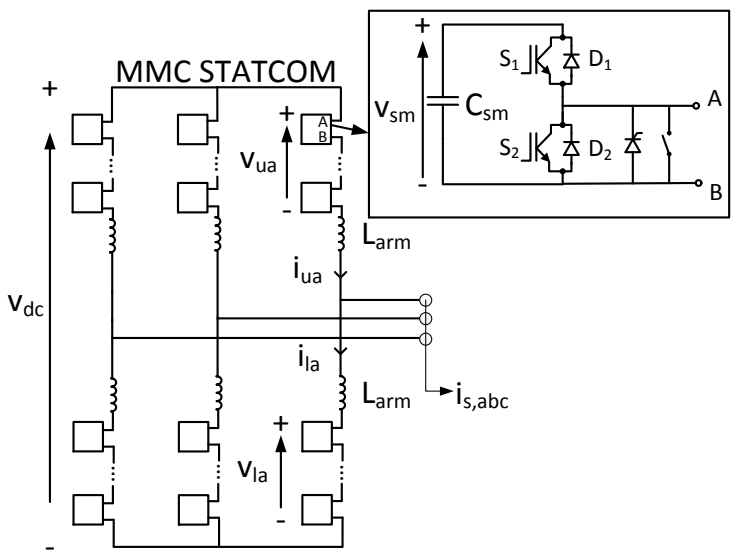

Figure 6.1: MMC DS-STATCOM schematic.

structure presented in [26] and are tuned accordingly to provide the circulating voltage reference $v^*_{c,j}$, where j denotes the phase. The v_{dc} and q_{ac} outer controllers are implemented as PI in the dq-frame and control the d- and q-components of the current i respectively. This control structure is common in VSC converters and is presented in Figure 12.7 of [27]. The reference of the i_{dq} is then transformed into $\alpha\beta$-reference frame, i.e. $i^*_{\alpha\beta}$. An additional control loop is introduced for the harmonics mitigation including two steps, namely (i) detection and (ii) harmonics control. This loop provides the reference for the harmonic components of the output current $i^*_{sh,\alpha\beta}$, which is added to the outer controllers reference $i^*_{\alpha\beta}$ and is subsequently fed to the output current controller. The generated output voltage reference v^*_{sj} and the v^*_{cj} are then used to determine the number of submodules to be inserted in each arm. In this study, the submodule gate signals are determined using Nearest Level Control (NLC) and a simple submodule capacitor balancing algorithm as presented in [28]. This Section focusses on the harmonics control loop and the output current controller.

6.2.1. Harmonics detection

The measured grid current or the PCC voltage is fed to the harmonic detection block, as shown in Figure 6.2. Regarding the detection methods, various techniques have been investigated in literature [29, 30, 31]. The methods are usually divided into two main categories: i) the selective detection methods that detect the magnitude of each harmonic individually and ii) the non-selective methods that simply split the current into fundamental and non-fundamental components [30].

In this study, a selective detection method is implemented in the dq-reference frame and the positive and negative-sequence components are both extracted for each harmonic with the appropriate rotation. The detection method as well as the reference frame transformation are usually associated with time delays arising from sampling frequency [32]. Because the filters are non-ideal and can introduce a phase shift, the reference signal might be different in shape or phase than the harmonic which needs to be attenuated [33]. Moreover, the trade-off between the filter's response and its attenuation is well-known [34]. These effects on the detection method are discussed in [7], where a comparison of different detection methods is conducted and the limitations of the active filtering procedure are highlighted. Additionally, in this case, the angular position is necessary and needs to be obtained from the PLL. This requires careful implementation especially in cases of unbalances. Therefore, these effects need to be taken into consideration in the real system and thus, transformation to both positive and negative-sequence reference frame is required to compensate for possible errors [35, 36].

Previous studies have shown that mapping the harmonic components to dc signals is more effective in detection and easier in implementation than the use of bandpass filters tuned for each harmonic in $\alpha\beta$- or abc-frame [37]. Therefore, a second-order low-pass filter (LPF) is used to extract the dc component that corre-

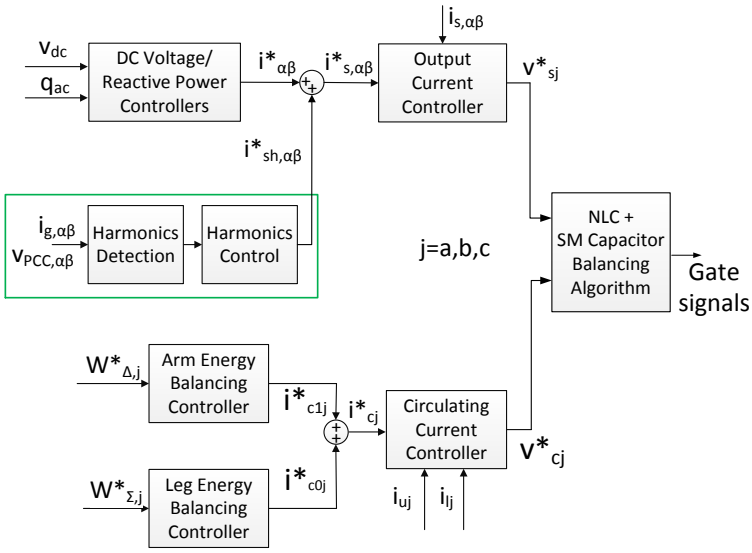

Figure 6.2: MMC control structure including harmonics.

sponds to the desired frequency component in the abc-reference frame. A Butterworth second-order LPF is implemented using Second-Order Generalized Integrator (SOGI) [38], and its transfer function is given by:

$$G(s) = \frac{k_{SOGI}\omega'^2}{s^2 + k_{SOGI}\omega' s + \omega'^2} \tag{6.1}$$

where k_{SOGI} is the gain of the LPF and ω' is the cutoff frequency in rad/s. In this case study, the parameters are selected as: k_{SOGI}=$\sqrt{2}$ and ω'=100 rad/s.

The grid current harmonics detection takes place as shown in Figure 6.3.

6.2.2. Harmonics control

The output of the LPF is compared to zero, which is the desired harmonic content. To compensate for static errors in the harmonics detection, the formulated error is then passed through a PI controller to create the harmonic reference for the output current controller. The aim of this study is to compensate harmonics up to the 13^{th} order, namely 5^{th}, 7^{th}, 11^{th} and 13^{th} which have the highest amplitude. As a result, the harmonic reference generation block includes eight PI controllers in parallel (positive and negative sequence for each harmonic order). Since every PI controller has infinite gain at 0 Hz, the desired frequencies of 250 Hz, 350 Hz, 550 Hz and 650 Hz are achieved by the rotation of the sensed current in the dq-frame.

It should be noted that the focus of these controllers is laid on the steady state performance and stability. As a result, a small integral part is used to reduce the steady-state error provided that the output current controller can follow the har-

monic currents reference fast and precisely. The current harmonics control structure is shown in Figure 6.3. The resulting harmonic current reference i_{sh}^* is added to the outer controller reference and fed to the output current controller as can be seen in Figure 6.4. Since the output current reference i_s^* includes more harmonics than the fundamental and the control is implemented in the $\alpha\beta$-frame using PR control, four resonant controllers are added in parallel, tuned at the aforementioned desired frequencies.

The harmonic resonant controllers need to be tuned faster than the fundamental one. Therefore, depending on the higher frequency component they need to follow, the resonant parts of the output current controller are chosen as:

$$K_{R_n} = nK_{R_1} \tag{6.2}$$

where K_{R_1} is the fundamental resonant gain, K_{R_n} is the resonant gain of the n^{th} harmonic and n is the order of the harmonic component.

The reference output voltage v_s^* is fed to the modulation, which inserts a time delay in the loop before creating the v_s. The output voltage drives an output current through an impedance with a primarily inductive part $L_{arm}/2$. Therefore, the plant function is given by:

$$\frac{i_s}{v_s} = \frac{2}{sL_{arm}} \tag{6.3}$$

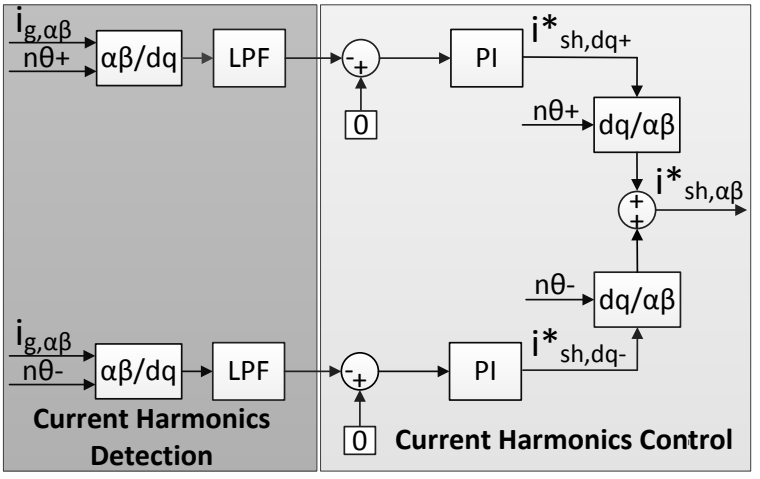

Figure 6.3: Detection and control structure for the mitigation of high order current harmonics. The grid currents are sensed and transformed with appropriate dq-transformations both in the positive and the negative sequence. The PI controller eliminates the resulting dc static error. The currents are transformed back to the $\alpha\beta$-frame since the output current controller (see Figure 6.4) uses parallel PR controllers as described in [39].

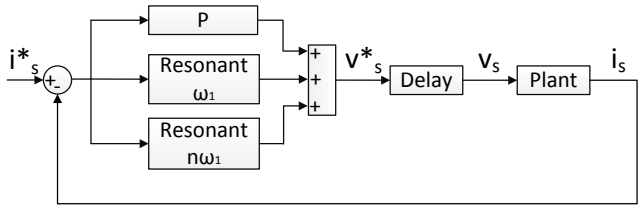

Figure 6.4: Output current controller including resonant controllers for n^{th} harmonic order.

The ability of the MMC-STATCOM output current control to follow higher order harmonics was experimentally tested. Figure 6.5 shows the measured value of the harmonic current compared to the reference. It should be noted that in all cases, the magnitude of the injected current shown is the maximum that could be controlled without saturating the voltage reference. From the results, it can be deduced that the developed controller follows with high accuracy the 5^{th} and 7^{th} harmonic order reference. The accuracy is slightly deteriorated in the 11^{th} and 13^{th} harmonic order due to the higher dynamic of the current reference that needs to be followed. However, the result can be considered adequately accurate.

6.2.3. Voltage harmonics control

To achieve voltage harmonic components mitigation, the same detection method is used to extract the dc component of the PCC voltage harmonics. The main difference lies on the voltage harmonics control. Firstly, the references for the voltage harmonic components $v^*_{PCC,n}$, as specified by grid codes and TSOs [22], are used. Secondly, a transformation of the voltage reference output of the PI controller to current is necessary before it is fed to the output current controller. For this purpose, the line impedance Z_{nh} value needs to be estimated for each n^{th} harmonic order and is used as shown in Figure 6.6.

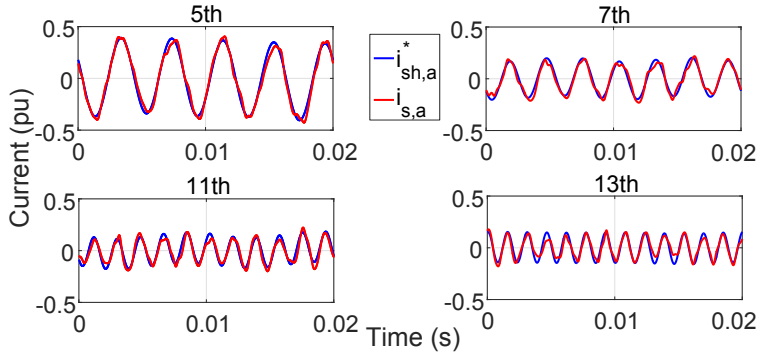

Figure 6.5: Performance of the current controller of the MMC DS-STATCOM in following sinusoidal reference currents up to the 13^{th} order.

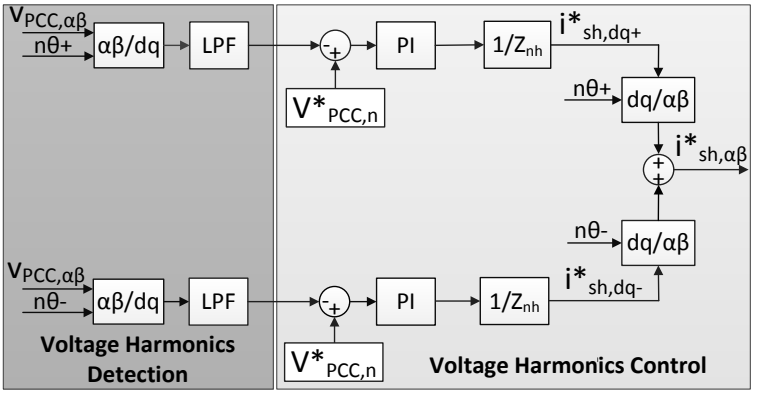

Figure 6.6: Voltage harmonics detection and control.

6.3. Experimental Set-Up

To test the active filtering capability of the MMC DS-STATCOM, a laboratory set-up was built. The MMC STATCOM prototype is shown in Figure 2.3(a), while Table 6.1 summarizes the main parameters of the lab-scaled system. The MMC is controlled via an FPGA that is part of the dSPACE simulator, which acts as the central controller and is connected to a PC equipped with ControlDesk interface. The control algorithm of the MMC was implemented in Matlab/Simulink and HDL code was automatically generated and loaded to the FPGA of the dSPACE interface. The communication of the dSPACE simulator to the submodules of the MMC takes place via optical transmission (i.e. optical fibers) to provide the necessary isolation and noise immunity. The submodules send the capacitor voltage measurement and a fault indication signal to the dSPACE, while dSPACE sends the necessary PWM signals to the submodule switches. The sampling frequency was 10 kHz and the gains for the different employed controllers are presented in Table 6.2. Details on the set-up connection for the investigated voltage and current harmonics mitigation case studies are given in Sections 6.4 and 6.5 respectively.

6.4. Experimental Results on Voltage Harmonics Mitigation

Apart from current harmonics, problems can be created by the presence of voltage harmonics, which is a common phenomenon in weak grids, e.g. in wind power plants. To mitigate this problem, STATCOMs are often utilized [40, 41, 42]. In this Section, the ability of the developed control system to attenuate harmonics at the PCC voltages is assessed experimentally.

The schematic of the used experimental set-up is shown in Figure 6.7. In this case, the controllable AC source is used to emulate the behavior of the wind power plant and is connected to the isolation transformer through a 2.2 mH line inductor

Table 6.1: Parameters of Experimental Setup.

Description	Symbol	Value
Max Tested Power (kVA)	S	1.25
Max Tested Phase RMS Voltage (V)	V_g	150
Pole-to-pole Voltage (V)	V_{dc}	400
Submodule's Capacitance (mF)	C_{sm}	3.6
Arm Inductance (mH)	L_{arm}	20
Number of Submodules per arm	N	4
Transformer Ratio	n	1:$\sqrt{3}$

Table 6.2: Controller Gains of Lab Setup in rad/s.

Controller	K_p	K_i	K_r
Arm Energy	0.2	0.5	-
Leg Energy	0.2	0.3	-
Circulating Current	20	800	ω_1: 8e3 ω_2: 8e3
Output Current	24	-	ω_1: 2.4e3; ω_5: 12e3; ω_7: 16.8e3; ω_{11}: 26.4e3; ω_{13}: 31.2e3
DC Voltage	0.15	1	-
Reactive Power	0.15	1	-
Harmonics	1	0.01	-

to emulate the behavior of a grid line.

The harmonics injected by the AC source are controlled and a desired waveform is generated. The control system is then responsible to sense the harmonic content of the voltage and with the appropriate current injection it should be able to mitigate them, respecting the limits of the grid operator for the PCC voltage. The maximum harmonic attenuation that the STATCOM can provide is usually limited by its current rating and the limited available DC link voltage, while it also depends on the line inductance.

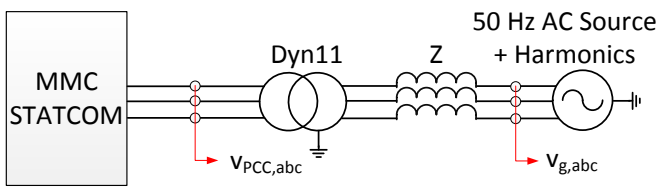

Figure 6.7: Schematic of experimental setup for voltage harmonic mitigation.

Table 6.3: Voltage Harmonics at the PCC

Harmonic order	Grid voltage	Specified limit
2^{nd}	-	0.8 %
5^{th}	3.3 %	2 %
7^{th}	2.1 %	0.59 %
11^{th}	1.7 %	0.64 %
13^{th}	-	1.5 %
17^{th}	0.7 %	0.1 %

In this scenario the values for the injected PCC voltage harmonics and their respective limits, as set in [22], are presented in Table 6.3. The specified limits are used as references $V^*_{PCC,n}$ in the closed-loop control scheme presented in Figure 6.6. Due to the aforementioned limitations of the converter, harmonics up to the 11^{th} order are controlled and attenuated. It should also be noted that in this case study the converter does not inject reactive current at the fundamental frequency.

A frequency sweep is conducted for the line impedance Z using an impedance analyzer and its value is measured for frequencies up to 1 kHz in order to take the effect of the parasitic elements into consideration. The respective impedance value at each frequency (Z_{nh}) is used for the control of the voltage harmonics as explained in Section 6.2. The measurements are presented in Figure 6.8.

Figure 6.9 shows the comparison between the voltage at the PCC before and after the activation of the control system for harmonic mitigation. Before, the voltage at the PCC is equal to the voltage generated by the non-ideal controllable AC source taking into account the transformer ratio, since no current is flowing in the system, and the THD is 4.9%. The activation of the harmonic compensation results in a significant reduction in the THD from 4.9% to 3%, as depicted in Figure 6.9, in the time domain.

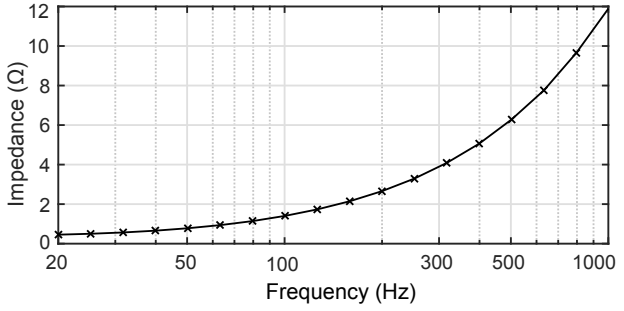

Figure 6.8: Line impedance Z measurements obtained by performing frequency sweep with an impedance analyzer.

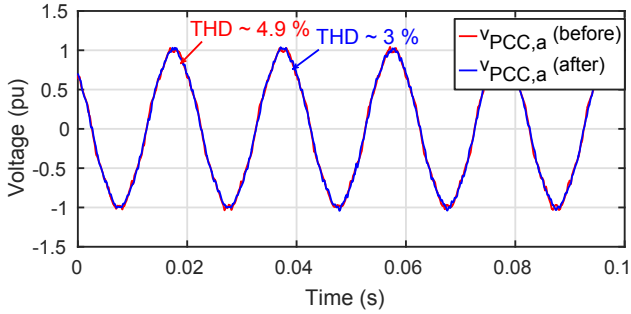

Figure 6.9: Voltage at the PCC of phase-a before (red) and after (blue) harmonic compensation - Time domain. The %THD is reduced by 1.9%.

Figure 6.10 shows the effectiveness of the voltage mitigation control system of the MMC STATCOM with a comparative graph in the frequency domain. Considering the defined references, it can be concluded that the selectivity of the detection and control method for each harmonic component is verified. Moreover, it can be seen that the harmonic components of all the frequencies of interest follow the specified values as set by the grid codes. Although closed-loop control is used, the obtained values for the harmonic components are slightly below the specified limits due to overcompensation resulting from the measurement of the line impedance Z. More specifically, the impedance values, which are used in the harmonics control (see Figure 6.6), were estimated using the impedance analyzer at low currents. When the system is operated at high currents, close to saturation, the inductor impedance value can be higher than the measured one resulting in harmonics overcompensation. It has to be noted that the average effective switching frequency of the submodules in this case was once again recorded to be approximately 0.9 kHz.

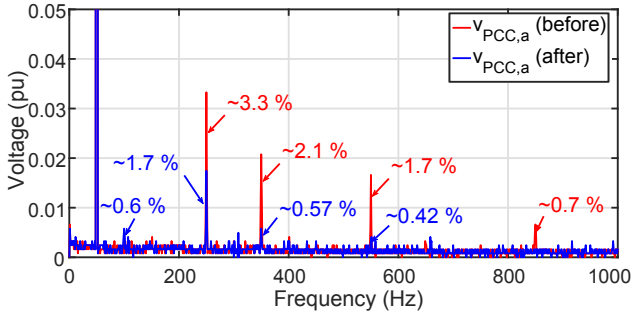

Figure 6.10: Voltage at the PCC of phase-a before (red) and after (blue) harmonic compensation - Frequency domain. The target harmonics are overcompensated.

6.5. Experimental Results on Current Harmonics Mitigation

In this Section, the ability of the MMC to act as an active filter and attenuate the current harmonics is evaluated experimentally. A diode rectifier load is connected to the PCC as shown in the schematic of Figure 6.11.

An ideal AC source is used to simulate the grid. This is connected to a Dy11n isolation transformer and a diode bridge rectifier is placed in parallel to the STATCOM.

On the DC side of the bridge rectifier, a resistor R of 200 Ω is connected. This load is highly non-linear and draws a harmonic current [43]. This current is being drawn from the ac grid resulting in polluted grid current waveforms which may have a severe impact on sensitive loads connected to the PCC. The grid currents are sensed and fed to the control system, as described in Section 6.2. The aim is the elimination of the current harmonics up to the 13^{th} order, using a relatively low effective switching frequency (≈1 kHz), which is mainly determined by a simple sorting algorithm that is employed to ensure the balanced operation of the submodules within one arm [28].

Figure 6.12 depicts the currents when STATCOM operates close to its nominal power, injecting 0.73 pu of inductive reactive current to the grid and the harmonic compensation is not activated. The total current flowing to the grid is highly distorted with approximately 26% THD, mainly due to the presence of the 5^{th}, 7^{th}, 11^{th} and 13^{th} order current harmonics.

Figure 6.13 depicts the current waveforms after the application of the harmonic compensation. It can be seen that the STATCOM currents are now distorted, while the THD of the grid currents is effectively reduced to 9%.

A comparative graph in Figure 6.14 shows the grid currents before and after the application of the harmonic compensation in the time domain, while Figure 6.15 depicts the result of the Fast Fourier Transformation (FFT) of the grid current waveforms. It can be seen that the injection strategy eliminates almost completely the

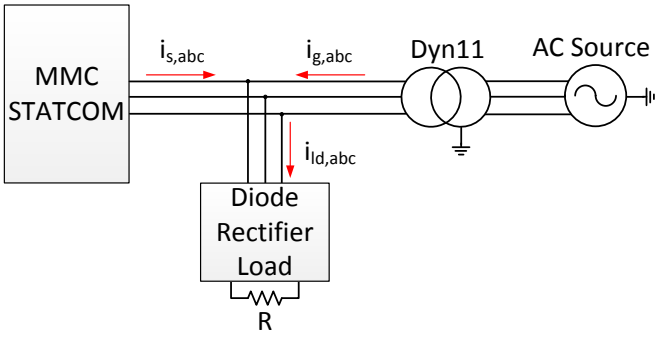

Figure 6.11: Schematic of experimental set-up for current harmonic mitigation.

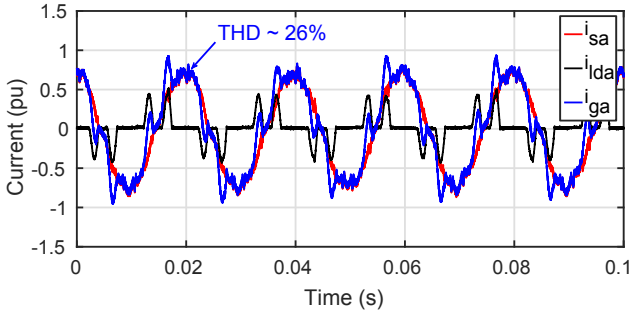

Figure 6.12: DS-STATCOM current (red), load current (black) and grid current (blue) at the PCC of phase-a without harmonic compensation. Grid current has a %THD of 26%.

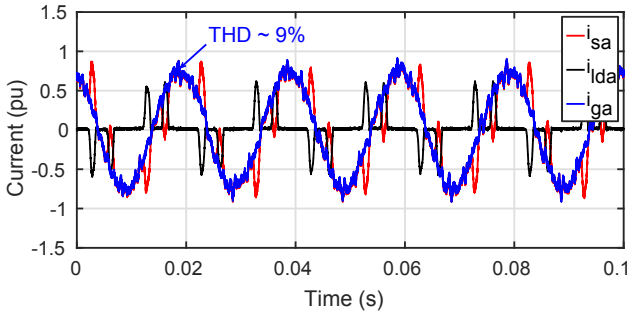

Figure 6.13: DS-STATCOM current (red), load current (black) and grid current (blue) at the PCC of phase-a with harmonic compensation. Grid current has now a %THD of 9%.

targeted harmonic components in the grid current, which now appear in the STATCOM output current.

To estimate the average switching frequency of one submodule when the harmonic compensation was activated, the PWM signal voltage pulses were mon-

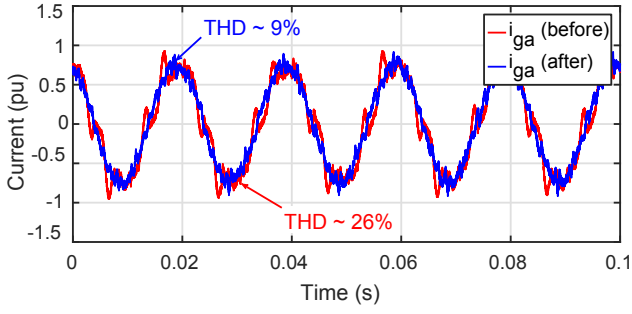

Figure 6.14: Grid current at the PCC of phase-a before (red) and after (blue) harmonic compensation - Time domain. The %THD is reduced by 15%.

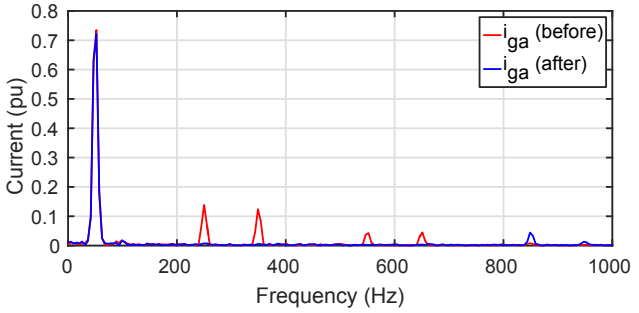

Figure 6.15: Grid current at the PCC of phase-a before (red) and after (blue) harmonic compensation - Frequency domain. The target harmonics are completely eliminated.

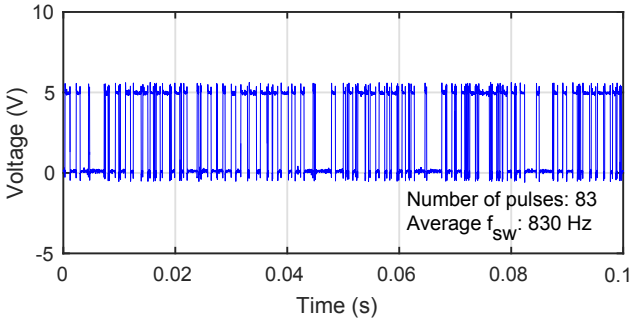

Figure 6.16: PWM signals of first submodule of phase-a when the harmonic compensation is enabled. The sorting algorithm ensures approximately equal switching frequency for all submodules.

itored for several cycles. Figure 6.16 shows only the recorded number of PWM pulses fed to the first submodule of phase-a in 100 ms. However, it can be considered that on average the switching frequency is similar for all submodules. It can be seen that the average effective switching frequency is approximately 0.83 kHz, which is well within the limit of 1 kHz. This result is particularly important since it proves that the MMC-STATCOM can efficiently mitigate high order of harmonics (up to 650 Hz) with the use of low switching frequency due to its increased bandwidth.

6.6. Conclusions

Recent grid codes require the compensation of high order current and voltage harmonics. For this reason, this study focussed on the use of the MMC as an active filter to mitigate those harmonics. A selective harmonics detection method and an output harmonic current controller were implemented and experimentally verified using a developed MMC prototype, which was operated as DS-STATCOM. Tuning was performed taking into account the non-linearities of the system and the delays introduced by the measurements and the control loop, which are usually neglected

when approaching this problem through average model simulations. Finally, two realistic representative case studies for current and voltage harmonics were defined and tested.

The MMC ability to selectively inject harmonic currents up to 13^{th} order was proven, while the main limitations were set by the set-up rating, the number of levels of the MMC and the available DC link voltage. In fact, it was seen that the increased bandwidth of the MMC allowed for the grid current harmonics control up to the 13^{th} order and for PCC voltage harmonics up to the 11^{th} order, while maintaining the average effective switching frequency below 1 kHz and thus, the MMC losses low. More specifically, harmonics mitigation resulted in a reduction of the current THD from 26% down to 9% and of the voltage THD from 4.9% to 3%. Therefore, the advantages of the MMC technology were hereby proven for active filtering purposes.

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7

Conclusions

In this Chapter the answers to the key questions, which were set in Chapter 1, are provided. The conclusions are based on the findings of the research studies conducted and presented in the previous Chapters. Finally, recommendations are made for extension of the current work and future research.

7.1. General Conclusion

Overall, this dissertation proposes a more holistic approach in the study of HVDC grids' protection. Unlike previous studies which deal with dc faults as independent phenomena, this work provides a theoretical background into the fault development stages backed by experimental verification and proposes a modular dc breaker design, which can be used to isolate dc faults in multiple HVDC lines, and a control strategy to ride through dc faults using the Full-bridge MMC. At the same time, this dissertation presents the possibilities of continued operation of the MMC for ac grid support, both for Low-Voltage-Ride-Through (LVRT) and high-order harmonics mitigation based on the most recent grid codes, even when a dc fault affects the whole or part of a dc grid. By implementing the proposed protection and control strategies, which make full use of the advantages and the control freedom of the MMC operation, the system designer can maximize the utilization of the grid assets even during contingencies. Hereby, the conclusions on each of the investigated topics are presented as answers to the key questions which were defined in Chapter 1.

7.2. Answers to key questions

The main characteristics of dc faults

In order to develop dc fault protection strategies for HVDC grids, we first need to understand the main parameters that influence the temporal development of dc faults. The term 'dc faults' usually refers to cable faults and thus, the performed study in Chapter 2 focussed on both pole-to-ground faults as well as pole-to-pole faults (short-circuit). Additionally to the fault type, the configuration of the grid plays an important role on the fault development (i.e. monopolar/bipolar, symmetric/asymmetric, metallic/ground return), as well as the impedance of the cables and the fault itself. Finally, since converter stations are connected to the ends of the dc lines, the switching operation of the converter is also important when referring to MMC stations, since the circuit changes depending on whether the MMC maintains switching operation or not during a fault.

Chapter 2 presented an analysis of the impact of the aforementioned parameters on the dc fault development and verified the theoretical fault development with detailed experimental results. The performed study showed that in case of pole-to-ground faults, the symmetric monopolar grid topology is able to ride through the fault, since the 'healthy' pole takes up the whole voltage of the dc link and controlled operation can resume. However, it has to be noted that in this case both pole cables need to be rated for the full dc link voltage. Apart from this case, it can be concluded that independent of the choice of the aforementioned parameters, the dc faults develop in three stages. During the first stage, high overcurrents develop on the dc cables, as the cables capacitance gets discharged through the fault. Although these overcurrents can reach values higher than 10 pu, their duration is very small and thus the dc cables are able to withstand the developed stresses. At the

same time, the dc voltage of the cables drops, oscillating according to the RLC cable parameters. Once the voltage at the dc output of the MMC drops below the nominal level, the second stage starts and the capacitors of the submodules discharge through the fault, while the fault currents circulate through the converter legs. The moment this happens depends on the fault propagation time to the dc output of the converter. Depending on the circulating current amplitude and the overcurrent protection threshold of the valves, switching operation can either continue or stop. On one hand, in case switching stops, the MMC behaves like a diode-bridge rectifier and the submodule capacitors stop discharging. At this moment, the third dc fault stage starts. On the other hand, in case switching operation continues, the submodule capacitors discharge and momentarily increase the dc link voltage. The moment at which the submodule capacitors voltage level reaches the level of the dc link voltage signifies the beginning of the third dc fault development stage. In this stage, the ac grid contributes to the fault and the steady-state reached depends on the fault impedance and the ac grid voltage. Overall, it has to be noted that the MMC cannot continue its control operation, even if switching does not stop, due to the imposed low dc link voltage level.

The requirements for dc breaker design optimization

As analysed in Chapter 2, the dc current does not have a natural zero-crossing during a fault, while the fault currents in the converters reach peaks higher than 3 pu within 5 ms. As a result, to isolate the faults, the breakers need to break high currents within 5 ms, dissipate the energy stored in the HVDC lines during a fault, as well as maintain high efficiency during normal operation. Moreover, the high cost of the breakers poses a challenge towards the realization of dc grids. Therefore, optimization in all the aforementioned breaker design requirements is necessary.

Although hybrid breakers bring advantages in most of the defined requirements, their cost is estimated at half of the converter station. The hybrid breakers consist of a Nominal Current Path (NCP) which is used during normal operation, while the Current Commutation Path (CCP) and the Energy Absorption Path (EAP) only conduct during faults. Therefore, it was observed that there exists the possibility of equipment sharing between breakers who are located close to each other. More specifically, Chapter 3 proposed a breaker circuit configuration called the Multi-line Breaker (MLB), which realizes the concept of equipment sharing for breakers located at the node of a dc grid, protecting multiple lines of the grid at the same time. This is realized by minimising the number of CCP and EAP paths needed and also the number of the involved switching elements within the breaker, while offering a bidirectional fault isolation capability.

The steps to ride through a dc fault without the use of dc breakers

Since the studies refer to multi-terminal HVDC grids, the use of ac breakers to de-energise the grid before the fault isolation is not advised. As a result, the use of

submodules with fault-blocking capability is necessary. The main objective during a dc fault is to controllably bring the fault current to zero to allow the fault isolation, while maintaining control towards the ac grid. Chapter 4 presents a step-by-step methodology to ride through a dc fault using a Full-bridge MMC. More specifically the steps that need to be followed are:

1. the outer control mode (v_{dc} or p_{ac}) needs to change to converter energy (W_{conv}) control. Although the control of the dc voltage is lost as it drops during the dc fault, the voltage of the submodules can be controlled independently. In fact, the control of the W_{conv} and the capacitor balancing algorithm which is used after the employed modulation technique, ensure that the submodule capacitors remain charged at their nominal voltage level independent of the dc grid state of operation and thus, the converter energy is maintained. By decoupling the dc grid voltage level from the submodule capacitor voltage levels, each arm can act as a virtual dc link even during a dc fault and thus, the MMC remains controllable. In this way, the MMC is able to operate as STATCOM and provide reactive power support to the ac grid.
2. the dc current controller described in Chapter 4 is necessary to drive the dc current to zero and decouple the ac from dc side operation.
3. arm and leg energy controllers are necessary to allow the STATCOM operation during the fault.
4. as soon as the fault is isolated, the dc voltage needs to be ramped up to its nominal level using the dc current controller with a rate of rise limiter to ensure the smooth re-energization of the dc lines and to avoid high inrush dc currents and dc voltage overshoot.

The ancillary services that the MMC can provide during dc faults

In case of dc faults in multi-terminal HVDC grids, two main protection concepts are identified, i.e. 1) use of Half-bridge MMC with dc breakers and 2) use of MMC with fault-blocking capability and mechanical disconnectors. In any case, once the MMC is isolated from the dc grid or as presented in Chapter 4, remains connected controlling the dc current to zero, the MMC should be able to provide ancillary services to the ac grid, as it is an expensive asset with high controllability. In this dissertation, Chapters 5 and 6 focussed on the additional role the MMC can play when disconnected from the dc grid. Two identified aspects in which the MMC can assist the grid operator with its high level of control are:

1. Low-Voltage-Ride-Through and
2. Harmonic filtering.

The MMC control requirements to support the ac grid during dc faults

Regarding the Low-Voltage-Ride-Through of the MMC, a problem considering internal balancing of the converter was identified under unbalanced grid conditions, while injecting the required positive and negative sequence output current, as specified by the most recent grid codes. To solve this problem, arm and leg energy balancing controllers are necessary. On this aspect, Chapter 5 presented the investigation, implementation and verification of a simple control method, solely based on PI controllers to deal with the problem. The analysis proved the effectiveness of the method and the advantages it offers considering implementation in real systems.

Moreover, recent grid codes require the compensation of high order current and voltage harmonics. For this reason, the MMC can be used as an active filter to mitigate those harmonics. To achieve this, a selective harmonics detection method and an output harmonic current controller are necessary. Chapter 6 presented the developed control structure and the verification of the concept for both voltage and current harmonics and it was concluded that the MMC, with its increased bandwidth, offers many advantages in active filtering compared to other converter topologies.

7.3. Recommendations for future research

2. On DC Fault Dynamics of MMC-based HVDC Connections

For future work, the developed set-up could be expanded to facilitate a multi-terminal dc network. It would be interesting to examine the use of more pi-sections or different configurations that resemble the cable structure more accurately, so that the dc fault propagation is accounted for. In this way, the effect of the experimentally used cable equivalent model on the fault development accuracy could be studied. Finally, the effect of the transformer topology on the fault development can be investigated both theoretically and experimentally.

3. Multi-Line Breaker for HVDC Applications

As future work, the development of a laboratory prototype of the MLB would be interesting to verify its operation. However, in this case, the tests would make sense if performed under high voltage and high current. Moreover, it would be interesting to perform similar studies using different proposed breakers as building blocks of the MLB to prove the effectiveness of the general concept.

4. DC Fault Ride-through using Full-bridge MMC

Potential future research can include the development of a Full-bridge MMC in the laboratory to experimentally verify the proposed control concepts. The main challenge as identified in Chapted 4 is the control response at the transition moments between STATCOM and inverter/rectifier operation, i.e. when the fault is detected and when it is cleared. At these moments, the control of the MMC stations should

be coordinated to maintain grid stability. As a result, a sensitivity analysis on the parameters influencing the control response of the different stations during grid restoration could be investigated.

5. Low-Voltage-Ride-Through of the MMC
As future work, it is proposed to study the effect of the negative sequence voltage in the calculation of the references of the circulating current fundamental component, in ac fault cases in which the positive and negative sequences have similar magnitudes.

6. High Order Harmonic Mitigation using the MMC
An interesting research path would be the internal current harmonic mitigation. The injection of output harmonic current affects the circulating current and thus, the efficiency of the converter. As a result, it is considered important to investigate techniques that suppress the resulting circulating current. Finally, future work could focus on the experimental verification of this control technique.

List of Publications

Thesis-related Publications

Journal Papers:

6. **E. Kontos**, T. Schultz, L. Mackay, L. Ramirez Elizondo, C. M. Franck, P. Bauer, “Multi-Line Breaker for HVDC Applications", in IEEE Transactions on Power Delivery, vol. PP, no. 99, pp. 1 – 1, 2017.

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4. G. Tsolaridis, **E. Kontos**, S. Chaudhari, R. Teodorescu, P. Bauer, “Internal Balance during Low-Voltage-Ride-Through of the Modular Multilevel Converter STATCOM," Energies, vol. 10, no. 7, 2017.

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2. **E. Kontos**, G. Tsolaridis, R. Teodorescu, P. Bauer, “On DC fault dynamics of MMC-based HVDC Connections" in IEEE Transactions on Power Delivery, Special Section on “Frontiers of DC technology", vol. PP, no. 99, pp. 1 – 1, 2017.

1. **E. Kontos**, R. Teixeira Pinto, S. Rodrigues, P. Bauer, “Impact of HVdc Transmission System Topology on Multi-terminal DC Network Faults", in IEEE Transactions on Power Delivery, vol. 30, no. 2, pp. 844 – 852, 2015.

Conference Papers:

10. **E. Kontos**, H. Papadakis, M. Poikilidis, P. Bauer, "MMC-Based Multi-Port DC Hub for Multiterminal HVDC Grids," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany.

9. **E. Kontos**, P. Bauer, "Reactor design for DC fault ride-through in MMC-based multi-terminal HVDC grids," 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand.

8. **E. Kontos**, P. Bauer, R. Teixeira Pinto, "Improving the DC fault response of H-bridge MMC-based HVDC Networks", Cigre Session 2016, Paris, France.

7. **E. Kontos**, P. Bauer, "Analytical model of MMC-based multi-terminal HVDC grid for normal and DC fault operation", 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China.

6. **E. Kontos**, R. Teixeira Pinto, P. Bauer, "Fast DC fault Recovery Technique for H-bridge MMC-based HVDC Networks", 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada.

5. **E. Kontos**, R. Teixeira Pinto, P. Bauer, "Providing dc fault ride-through capability to H-bridge MMC-based HVDC networks", 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Korea.

4. **E. Kontos**, R. Teixeira Pinto, P. Bauer, "Effect of Power Flow Control Methods on the DC Fault Response of Multi-terminal DC Networks", IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA.

3. **E. Kontos**, S. Rodrigues, R. Teixeira Pinto, P. Bauer, "Limiting Reactor Size Optimization for DC Fault Protection in Multi-terminal HVDC Networks", 2014 IEEE Energy Conversion Congress And Exposition (ECCE), Pittsburgh, PA, USA.

2. **E. Kontos**, R. Teixeira Pinto, P. Bauer, E. Wiggelinkhuizen, "Multi-terminal Network Options for the Interconnection of Offshore Wind Farms: A Case Study Between Britain and the Netherlands", 2014 IEEE International Power Electronics and Motion Control Conference And Exposition (PEMC), Antalya, Turkey.

1. **E. Kontos**, R. Teixeira Pinto, C. Restrepo Patiñho, P. Bauer, "Interconnection of Offshore Wind Farms with two Asynchronous Grids in a Multi-terminal Network", in IEEE Benelux Young Researchers Symposium (YRS 2014), Ghent, Belgium.

Patent:

1. L. Mackay and **E. Kontos**, "DC switch yard and method to operate such a DC switch yard", Patent: WO 2017/034408 A1, 2017.

Other Publications

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3. A. Shekhar, **E. Kontos**, L. Ramirez-Elizondo, A. Rodrigo-Mor, P. Bauer, “Grid capacity and efficiency enhancement by operating medium voltage AC cables as DC links with modular multilevel converters", International Journal of Electrical Power & Energy Systems, vol. 93, pp. 479–493, 2017.

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6. A. Shekhar, **E. Kontos**, A. R. Mor, L. Ramirez-Elizondo, P. Bauer, “Refurbishing existing mvac distribution cables to operate under dc conditions," 2016 IEEE International Power Electronics and Motion Control Conference (PEMC), Varna, Bulgaria.

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4. R. Teixeira Pinto, S. F. Rodrigues, **E. Kontos**, P. Bauer, B. Ferreira, “Optimal power flow in MTDC networks for large offshore wind power plants: Validation of the distributed voltage control strategy," IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, Japan.

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Biography

Epameinondas (Minos) Kontos was born on January 19, 1988, in Corfu, Greece. He received his Diploma in Electrical and Computer Engineering from the National Technical University of Athens (NTUA), Athens, Greece, in 2010, with major in Electric Power. In 2012 he did his internship on solar inverter design at SMA Solar Technology AG, Kassel, Germany. In 2013, he obtained the M.Sc. (cum laude) degree in Sustainable Energy Technology from the Delft University of Technology (TU Delft), Delft, The Netherlands. In September 2013, he started working as a Ph.D. researcher on the TKI "Synergies at Sea" project at the DC Systems, Energy Conversion and Storage (DCE&S) group of TU Delft. The project was carried out in collaboration with the Energy Research Centre of the Netherlands (ECN). During his Ph.D., he worked as a visiting researcher at the Energy Department of Aalborg University (AAU), Aalborg, Denmark, while he supervised seven master student theses and delivered guest lectures on Multilevel Modular Converters at TU Delft and AAU. His interests include design of multilevel modular converters for HVDC applications, protection system design for multiterminal HVDC grids and control of power electronics.