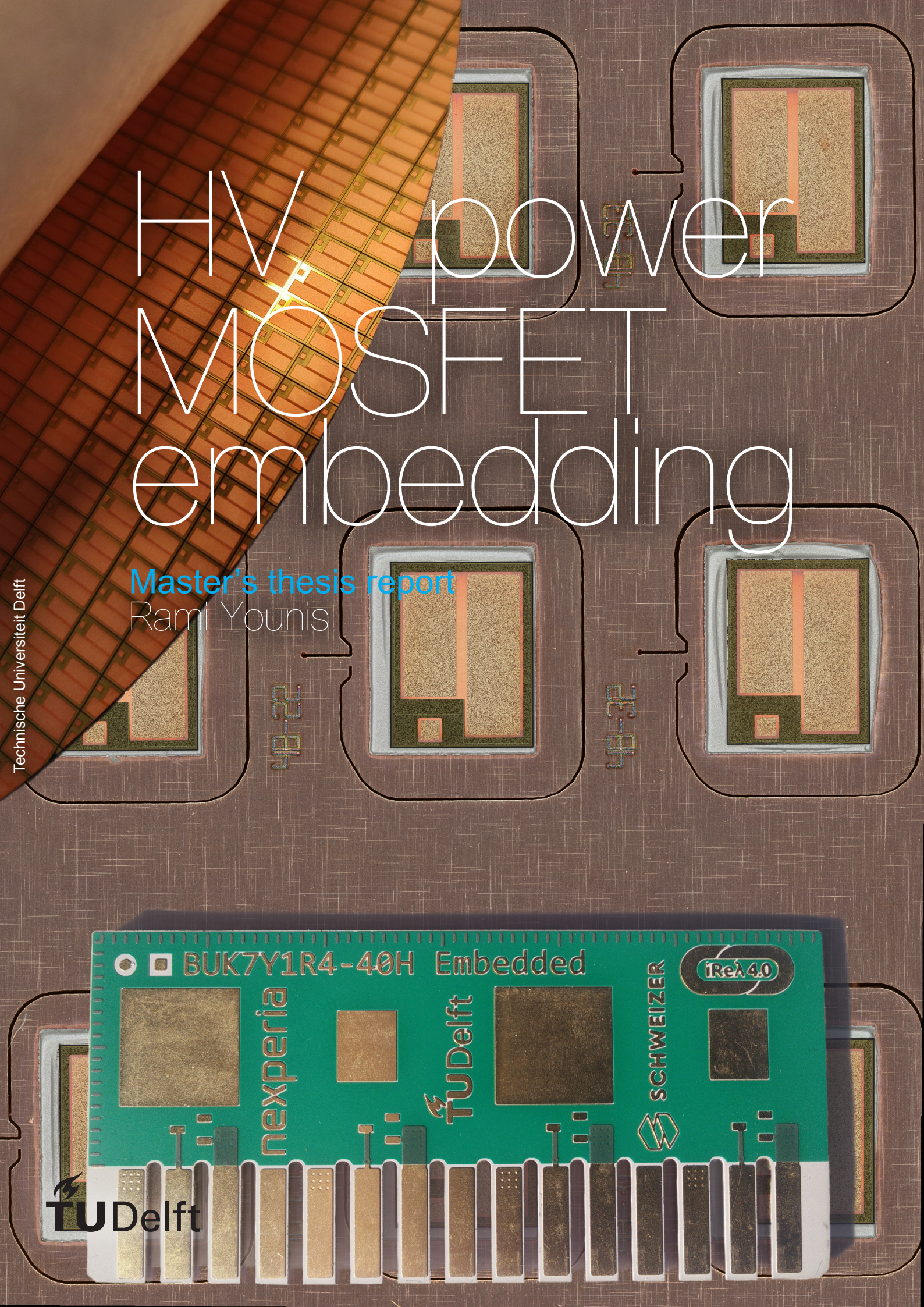
HV power MOSFET embedding

Master's thesis report

Rami Younis

Technische Universiteit Delft



HV power MOSFET embedding

Master's thesis report

by

Rami Younis

to obtain the degree of Master of Science

at the Delft University of Technology,

to be defended publicly on Wednesday December 7, 2022 at 13:00.

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This thesis is confidential and cannot be made public until December 7, 2023.

TU Delft

Abstract

Power electronics are an important technology used to convert electricity from a source like a battery or high voltage DC bus to more usable forms of electricity. This has to be done efficiently, reliably and without failures which is critical in applications like electric cars or datacenters. Power MOSFETs with upcoming SiC and GaN devices are an important building block used in these converters. Hence these power MOSFET devices have to be improved continuously to get a lower on resistance (R_{DSon}), a better thermal dissipation and lower parasitic losses. In this thesis we will take a look at the embedding of power MOSFETs inside a PCB to obtain these improvements. This new technology needs to be evaluated in terms of reliability, failure-modes and thermal/electrical performance. By designing, manufacturing and testing a PCB with embedded devices. During manufacturing silver sintering has been used for attaching the die to a copper coin. In the end the manufacturing has been done successfully. Testing showed an 18% lower R_{DSon} and a twice as low junction to ambient thermal impedance indicating a better performance compared to regular packaging.

Acknowledgements

I would like to thank my supervisor René Poelma for the opportunity to do this graduation project with him at Nexperia. At Nexperia I was able to collaborate with many colleagues who I would also like to thank, Anton Terpstra who helped a lot with the setup of the electrical measurements and everyone else who assisted me either online or offline. During the manufacturing process of the copper coins at CITC I got to know Sander Dorrestein, Martien Kengen, Henry Martin and Dave Reijs who have all assisted me during this process. Thanks to them the manufacturing went smooth and resulted in a working sample. For reviewing and manufacturing the PCB I would like to thank Jue Chen from Schweizer. And last but not least I would like to thank my colleagues at TU Delft, Dong Hu for his assistance with thermal measurements, Nikhil Gupta who has supported me during the whole project and of course the rest of the ECTM department.

Rami Younis
Delft, November 2022

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1

Project introduction

Currently a lot of industries are seeing increased use of electrification and power usage. From electric cars to the big data centers hosting cloud applications. To keep up with this a lot of power electronics devices are needed for efficient operation. With power MOSFETs, especially upcoming SiC and GaN devices, playing an important role. These devices have to be improved continuously to get lower on resistance (R_{DSon}), better thermal dissipation and lower parasitic losses.

Next to improving the bare devices themselves it is also needed to look at how they are packaged. With Moore's law on the decline there is the so called "more than Moore", meaning that instead of just improving transistors anything around it and smart architecture choices still improve performance. Here there are options to move away from using wirebonds, replace leaded solder with other alternatives, change the leadframes to attach the dies to and many more ways to increase integration.

So in this thesis we will take a look at improvements in the back end instead of the front end where just the device gets made. The focus will be on the embedding of power MOSFETs inside a PCB.

1.1. Problem description

Embedding technology offers new packaging opportunities for a bare-die portfolio of devices. The new technology needs to be evaluated in terms of reliability, failure-modes and thermal/electrical performance. Managing of reliable performance of bare-die semiconductors in customer embedding applications is needed. Embedding offers improved performance advantages in terms of low parasitics and thermal resistance due to a direct electrical and thermal path. Moreover, it frees up board space and allows for higher integration and power density.

1.2. Objectives

To investigate how embedding works and how it compares to a packaged device, in this case the BUK7Y1R4-40H see figure 1.1, a test vehicle with the same die embedded in it will be designed and manufactured. This will be a PCB with multiple embedded dies. Electrical and thermal measurements have to be done on this PCB to compare the performance. Besides that reliability tests have to be

done to investigate the life time of the devices when embedded. During the design, manufacturing and testing knowledge will be build up on design rules, failure modes, new manufacturing techniques and advantages or disadvantages of the technology.

BUK7Y1R4-40H

N-channel 40 V, 1.4 mΩ standard level MOSFET in LFPAK56

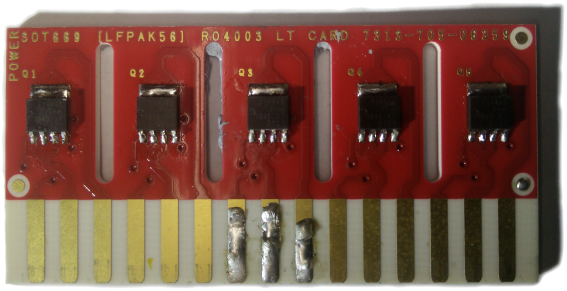
31 May 2018 **Product data sheet**

1. General description

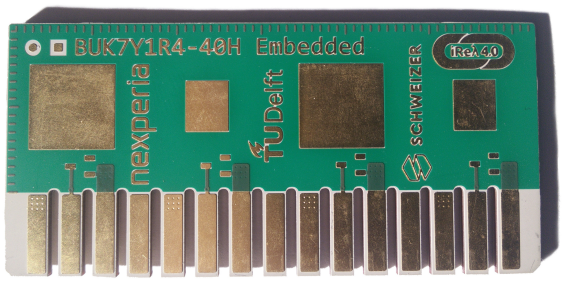
Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

Figure 1.1: The BUK7Y1R4-40H, a N-channel MOSFET, which will be used as comparison and the bare die of the same device will be used for embedding.

As a preview figure 1.2 shows a PCB with the mentioned packaged components and the PCB which is designed for this thesis with the embedded components. Its design and testing will be discussed in depth in this thesis.



(a) 5 LFPAK56 packaged devices on a PCB.



(b) 4 embedded devices inside a PCB.

Figure 1.2: A preview of the packaged and embedded evaluation boards, the embedded evaluation board has been designed and manufactured as part of this thesis and will be discussed in depth.

1.3. Approach

To be able to investigate embedded dies the design of a PCB/physical demonstrator based on a reliability evaluation board which is compatible to have dies embedded in them needs to be made. The test vehicle will be compared to a similar evaluation board which uses regular packaged LFPAK56 devices as shown in figure 1.2. Figure 1.3 shows an overview of the manufacturing and design steps needed to make the PCB.

To achieve the objectives the following steps need to be taken:

1. Obtain a wafer with dies that are suitable for embedding
2. Design a leadframe (Cu coin) to attach this die to
3. Design a PCB to embed the bare die with leadframe into by using finite element simulations
4. Attach the die to the leadframe using sintering

5. Manufacture the PCB and embed the die in it
6. Do electrical measurements like on resistance and analyze/compare the data
7. Do thermal measurements and analyze/compare the data
8. Do reliability measurements and analyze/compare the data

The expectation is that the embedded devices show a better electrical, thermal and reliability performance due to the shorter electrical path, shorter thermal path and different material choice compared to packaged devices. If this is actually the case will be investigated in the rest of this thesis.

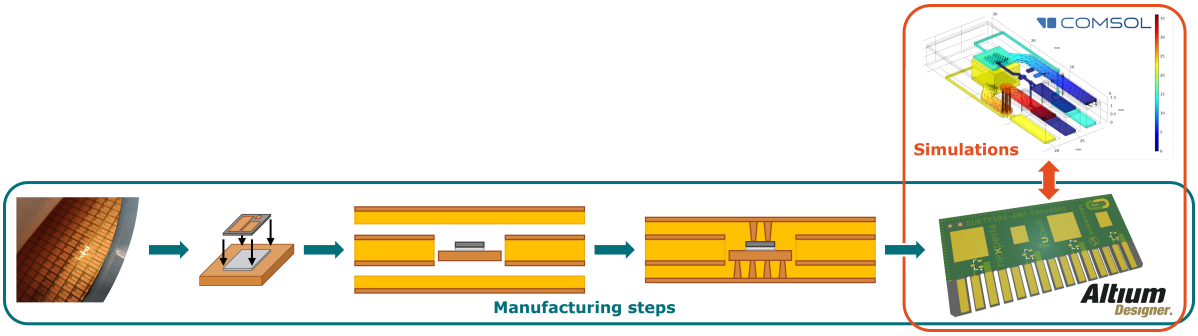


Figure 1.3: Manufacturing and design approach. Starting with a wafer, the bare dies are attached to a copper coin, then embedded in the inner PCB layers, next the other layers and vias are connected to get the final PCB. The design of this PCB has been done using finite element analysis to optimize the design.

1.4. Thesis outline

The thesis outline is as follows:

Ch 2, Literature To start chapter 2 will give an overview of power electronics packaging, PCB embedding and silver sintering.

Ch 3, Design & simulation Next chapter 3 will describe the design process and choices made. Going from the schematics of the PCB to the complete layout. This includes finite element analysis to verify the design and to predict the performance including the junction to heatsink thermal impedance.

Ch 4, Manufacturing Here the steps to manufacture the used die, the copper coin and the PCB are discussed. A focus on the die attachment by pressureless silver sintering is made since this is a critical step to get right.

Ch 5, Measurements & characterization Measurements have been done during the manufacturing phase, after manufacturing to characterize the electrical performance and to characterize the thermal performance. This includes among others: on resistance measurements, junction to heatsink thermal impedance measurements and junction to ambient thermal impedance measurements. Future reliability tests are planned as well.

Ch 6, Conclusion & summary To conclude a summary is given and the most important results and conclusions are discussed. With some recommendations at the end.

2

Literature

To get a better understanding of embedding it is important to first know how we got to this point. Figure 2.1 shows 3 ways of packaging a power MOSFET, discrete, in a module or embedded in a PCB. What is the current state of the art of packaging? This question will be answered in the next section 2.1 which will discuss current power electronic packaging. Section 2.2 will give an introduction on PCB design and how it relates to packaging. Finally section 2.3 will explain a die attachment technique called sintering.

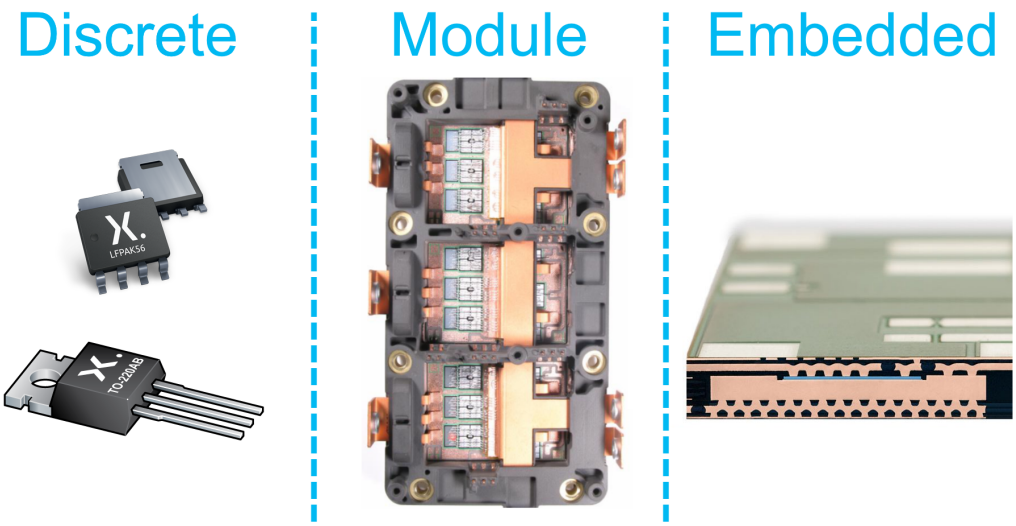


Figure 2.1: Different ways of ”packaging” a die, using a discrete package, using a module or embedding the die in a PCB.[20][1][26]

2.1. Power electronic Packaging

A lot is done to improve the MOSFETs at the front end with innovations in trench design[21], making dies thinner [2], by moving to wide bandgap materials like Silicon Carbide (SiC) or Gallium Nitride

(GaN)[16][18] which can work at higher temperatures and voltages. Another approach which can be taken to improve power electronics is to look at the packaging. Traditionally a die will be placed on a leadframe and wirebonds connect the die to the leads of the device, then it is all encapsulated in an epoxy or silicone gel. Because of the coefficient of expansion (CTE) mismatch between silicone gel and aluminium wirebonds the risk of heel crack exists[32]. For a great introduction and overview of power electronic packaging you can refer to [17].

With advanced packaging techniques there are multiple challenges for both Si and SiC power devices. Challenges include extra manufacturing steps, fast switching speeds and high heat dissipation, especially for SiC[12]. Some examples of packaging that is currently used or being researched are: Clipbonds which are similar to wirebonds but instead of a wire a flat piece of copper, a so called copper clip, is soldered to the top of the device, this increases both the electrical and thermal performance compared to wirebonds due to the big copper area. A Transfer-molded Power Module which uses a copper clip instead of wirebonds was developed and has a more than 10 times longer lifetime in power cycling test of ΔT_j=100°C [30]. A thin IGBT with copper clip with larger heat exchange area leads to 200% improvement in the IGBT power handling capability as compared with the conventional wirebonded IGBTs[7]. There are even ways to use double sided cooling enabling a reduction of up to 23% in junction to case thermal resistance[33].

(a) A bare die attach to a PCB using wirebonds.

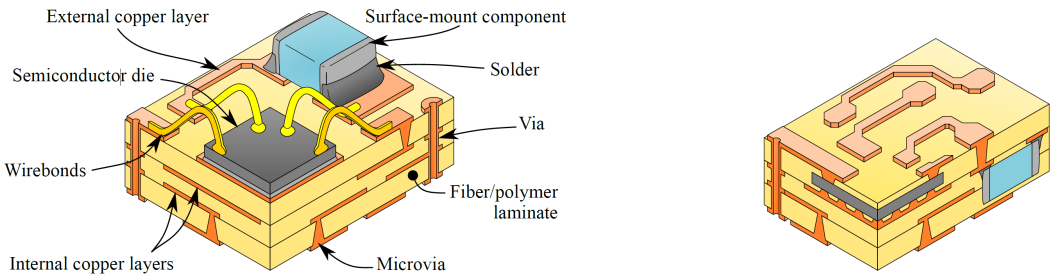
(b) A bare die attach to a PCB using a Cu clip.

Figure 2.2: Example of manufactured die with wirebonds and cu clip for performance comparison[7].

A next step in the future of packaging techniques is the embedding of dies in a PCB or other substrate[1]. This will be explored further in the next section.

2.2. PCB embedding

Usually a PCB is used as interface to connected components to each other by soldering them on the top or bottom of the PCB. A new idea is to also use the inside of the PCB to embed the components in it[1][6][10]. Figure 2.3 shows an example of what embedding is.



(a) A PCB with regular components.

(b) A PCB with embedded components.

Figure 2.3: An example of embedding a die and passive component inside a PCB[6].

When using PCB embedding for SiC an alternative is needed to FR4 which is a fiberglass material PCBs are usually made of. This is because temperatures over 175°C can easily be reached [11]. Either different existing materials or completely new materials can be used[9]. The way of connecting the die inside the PCB to the outside also needs consideration. Finite element analysis has been done on using vias[8][28]. A power module with embedded dies using vias to connect has been fabricated and tested[22]. A proposed way to increase copper density compared to vias is using blind blocks, which are complete areas above the die made of copper[13]. For a completely different approach a die was embedded and connected using a compressed metal foam[23].

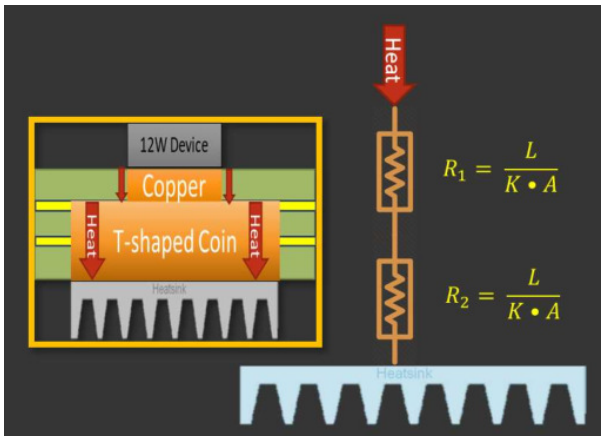


Figure 2.4: A T shaped Cu coin is used to attach to a die and at the same time have an thermal connection to the backside[31].

The embedded dies are usually connected to a piece of copper, referred to as direct bond copper, leadframe or copper coin. This can be done by attaching the die to a flat piece of copper[19]. This is also used for a Si and GaN die that are soldered on top[25]. A copper leadframe with a small cavity that fits the die was used in a three-phase inverter module, it was evaluated to have a thermal resistance of 0.50 °C/W ≤ $R_{th\ jmax-cooler}$ ≤ 0.61 °C/W. This equates to a 30%–44% reduction in R_{th} compared to a traditional LV module of comparable rating[16]. And a T shaped copper coin was used to both attach the die to and to replace vias on the bottom to connect to the outside since the bottom of the T shape is exposed on the bottom of the PCB, showing improved thermal performance[31].

2.3. Silver sintering

A lot of industries are moving towards a more sustainable future. This means one of the main die attach materials that is usually used, leaded solder, should be replaced. Besides the environmental reason, leaded solder has a low melting point, this means it is not suitable for high temperature applications. This can be replaced by using silver based materials. These cannot be soldered since silver doesn't have the same properties as leaded solder but instead sintering can be used[27]. A better electrical and thermal performance are also expected from silver. Figure 2.5 shows the sintering process from starting with small particles to a dense silver mass.

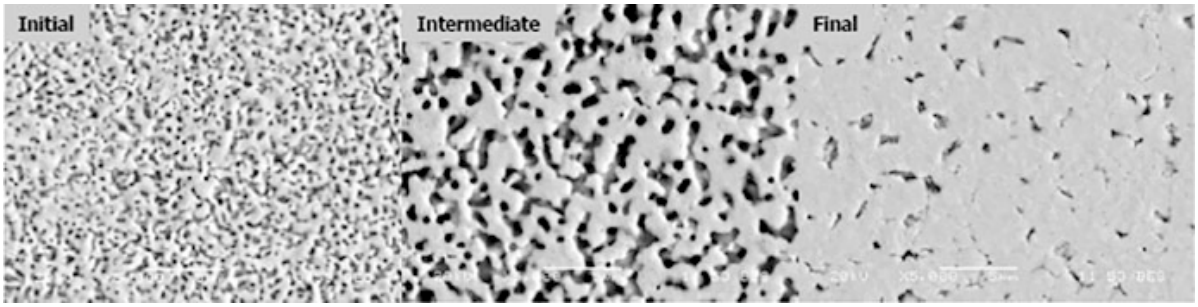


Figure 2.5: Different stages of the silver sintering process[27].

Silver sintering is already being used in research projects. A 10kW inverter module was made using IGBTs silver sintered to a copper leadframe[22]. A so called SKiN technology consist of sintering a chip to a substrate, on top of that a flexible PCB is sintered as well to make connections to the gate of the device. On the bottom of the substrate a heatsink is sintered. In all cases a layer of 30-100um silver is used as sinter material. This technique resulted in higher reliability and a 35% lower thermal resistance[29]. The mentioned copper leadframe with a cavity is filled with a thin layer of silver sinter material as die attach material as well[16].

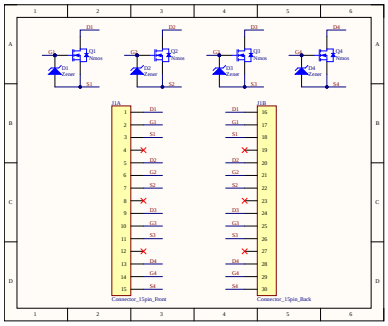
3

Design & simulation

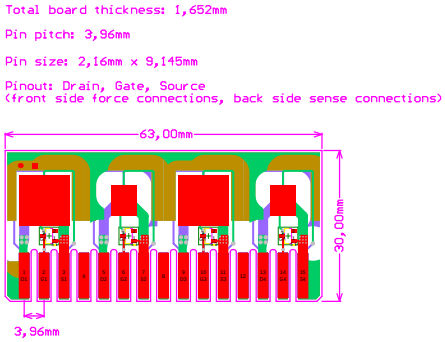
A Nexperia testboard with embedded copper coins has been designed for testing. For this first both the copper coin and the testboard PCB have to be designed. The design is based on thermal and electrical simulation results. During the design it was kept in mind that a comparison to the LFPAK56 packaged device has to be made. The MOSFET design handbooks [3] and [4] have been referred to during the design for aspects like thermal area and via choice.

The tools used to make the designs are Altium Designed for the PCB and copper coin frame. And COMSOL for the finite element simulations. How these 2 CAD tools interface will be further explained in section 3.4.

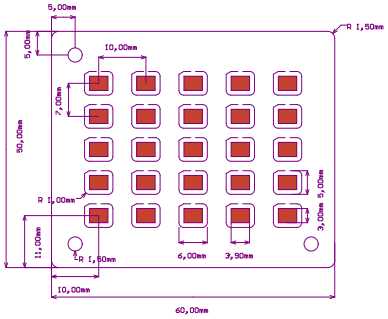
The PCB has 2 sets of requirements, on the one hand it has functional requirements and on the other hand it has manufacturing requirements. The following sections will discuss these requirements, specifications, simulations and materials and the resulting design choices that are relevant for each of these parts. Starting with the schematics in section 3.1, then the PCB layout 3.2, the copper coin 3.3 and finally how the simulation was used in section 3.4.



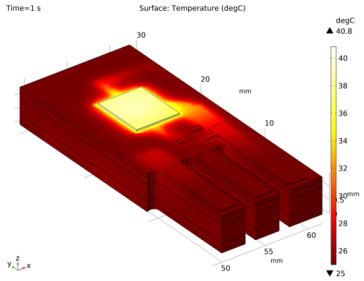
(a) Schematics



(b) PCB dimensions and copper layers



(c) Cu coin frame design



(d) Temperature simulation small area

Figure 3.1: An overview of manufacturing from schematics to simulation, these will all be discussed in the coming sections.

3.1. PCB schematics

There will only be one component in the PCB, the embedded MOSFET. As you can see in figure 3.2 there is are a front and back connector, 4 N type MOSFETs and 4 zener diodes. While there are enough pins to connect 5 devices the choice to use only 4 was made to have a distance of at least 3 mm between the device tracks to comply to the HV requirements.

The zener diode is connected to the gate, it protects the gate in the event a high voltage pulse appears on it. Since this is not expected to happen during the controlled tests it wasn't placed on the PCB in the end.

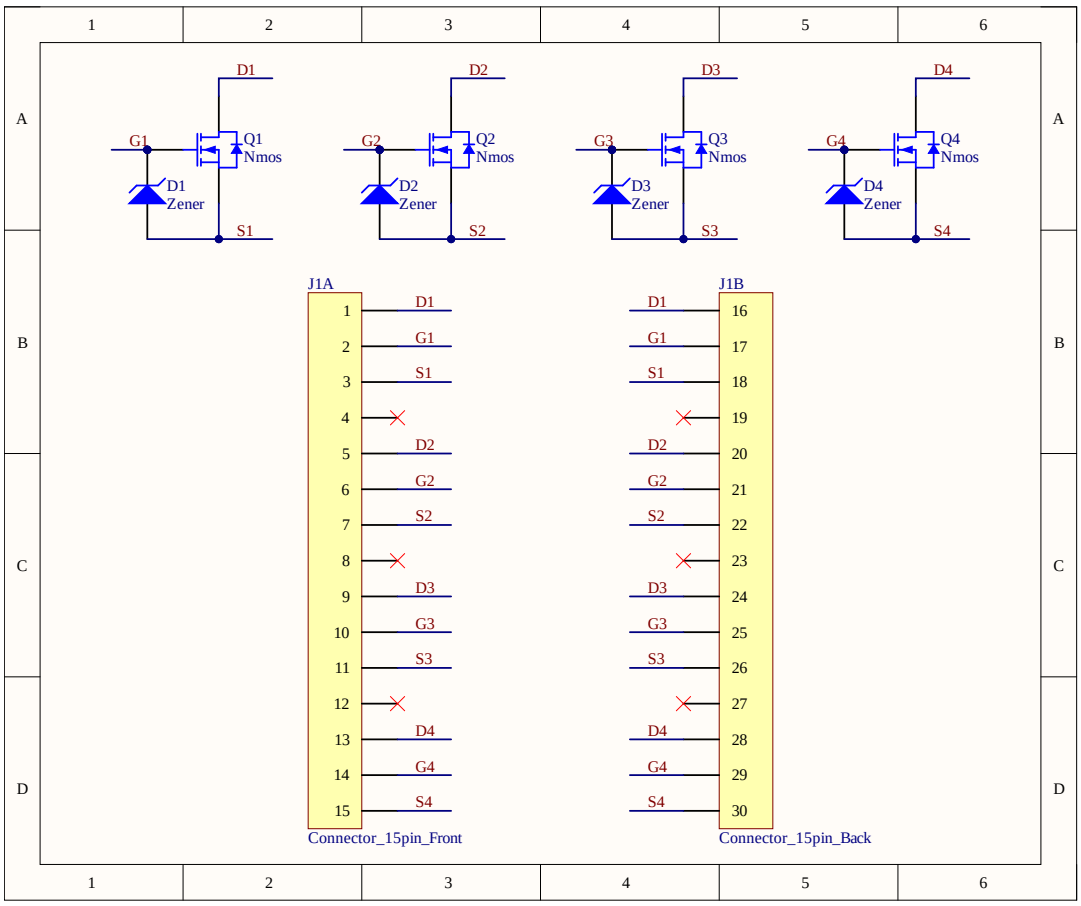


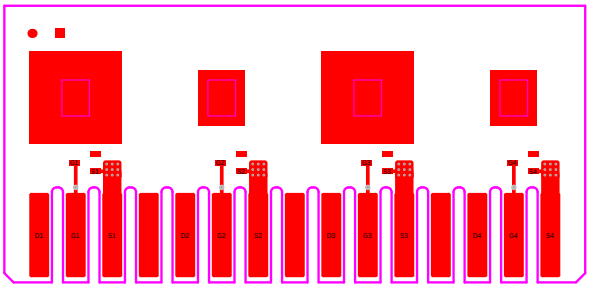
Figure 3.2: Schematics showing 4 N-channel MOSFETs and the connections to the 15 pin edge connector.

The MOSFET needs to be connected so a 4 wire/kelvin connection is possible, for this reason the force connections are made to the front side connector and the sense connections to the backside. Multiple ways to do the pinout were possible, this will be further explained in the layout part see section 3.2.1.

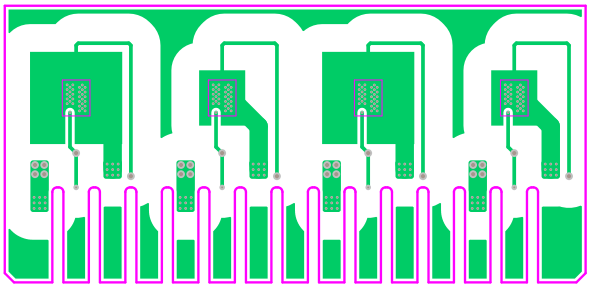
3.2. PCB layout

2 different layouts for the embedded MOSFET have been put on the PCB. The difference is the size of the copper area above and below the device. In once case a 10x10mm square is used, in the other case the minimum size of 5x6mm is used. In the simulation section 3.4 the effect of this area difference is discussed and the measurements in section 5.2.2 of the results show something similar.

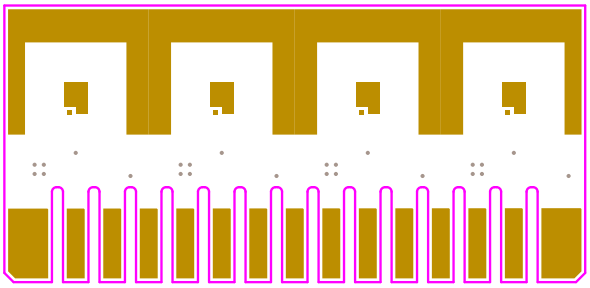
Below all 6 layers are shown in figure 3.3a to 3.3f, for all of them the outline of the PCB and the embedded die are shown in pink. The next sections will explain all the design choices that went into making these.



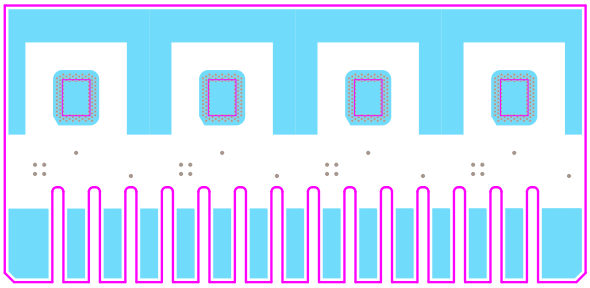
(a) Layer 1, consisting of the exposed heatsink pads, force connections, a place for a zener diode and fiducials.



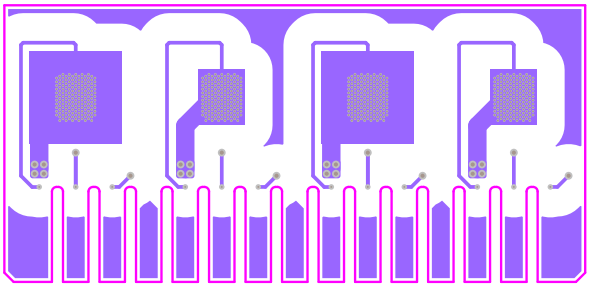
(b) Layer 2, the layer right above the embedded die with vias to the source and gate of the die, dead copper and a source sense wire



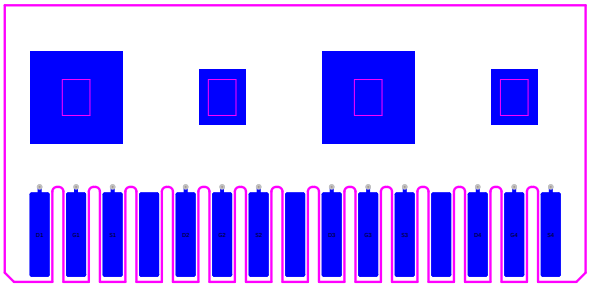
(c) Layer 3, the die is embedded here and there is dead copper



(d) Layer 4, the coin can be seen here with vias to the bottom for the drain and there is dead copper



(e) Layer 5, the layer below the die with vias to the cu coins for the drain, a drain sense wire and dead copper



(f) Layer 6, consisting of the exposed heatsink pads and the sense connections

Figure 3.3: All 6 PCB layers from top to bottom seen from above.

3.2.1. Size and shape

Since this is an embedded component no footprint to use for the layout exists yet. So a custom footprint that had to be made to fit it on the PCB.

The PCB should fit in the used measurement equipment which uses an edge connector. This determines the connector type on the PCB side, which is a 2 sides 15pin connector with a pitch of 3.96mm, a total width of 63mm and each pad has a width x height of 2.16mm x 9.145mm. The thickness of the PCB should be between 1.55 and 1.59 mm to fit, as seen in section 3.2.5 the thickness is 1.59 mm which does fit.

To electrically connect to the embedded devices the pinout is decided. In total 6 connections have to be made, a force connection and a sense connection for the drain, gate and source. To be compatible with the measurement equipment and as a logical choice the front connections are all force connections and the back sense connections with the same connection on the front and back, so drain force and drain sense on top of each other. This is to reduce any crosstalk between pins. Only the order of the pins still has to be decided. To keep the routing simple the gate is connected to the middle pin, source on the right and drain on the left. In figure 3.3b it is most clear why the source is on the right because of the gate location on the die.

3.2.2. Copper trace and vias sizing

The trace width and weight(term used for thickness in PCB manufacturing) is generally determined by the maximum constant current trough the trace and the maximum temperature it is allowed to reach taking into account the environments temperature. The thickness of the layers can be found in the stackup see figure 3.5. The toplayer at 64 µm is the thinnest layer that has current carrying traces on it. The force wire that carries the drain/source current is designed to be 2mm wide, so it has a cross-sectional area of $0.128 \cdot 10^{-3}$ mm^2. Using the IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design [14] the maximum allowed current can be calculated to be over 8A. A trace can support a higher current for short pulses, like when tests at very high currents need to be done[5].

To keep the PCB manufactureable there should be some ”dead copper” on layer 2-4 since otherwise there is a risk of delamination because of air bubbles. In figure 3.3 the dead copper can be seen on the 4 middle layers. This copper has no electrical purpose so it isn't connected to anything.

Like the traces the vias should also be able to handle the used currents and have a size that is manufacturable. Vias can be classified as through, blind and buried.

- Through vias go from to top layer to the bottom layer
- Blind vias start at the top/bottom and end on a middle layer
- Burried vias start at a middle layer and end on another middle layer

They can be manufactured using regular drilling with a drill bit or using a laser for small vias. Small laser drilled vias are also called microVia or µVia. 6 copper layers have been used where layer 1 and 6 are the top and bottom layer respectively. The types of used vias can be seen in table 3.1. The radius of the laser drilled µVias cannot be larger than the plated copper thickness of the layer above it to be completely filled. Since in this case the layers are around 0.1mm a diameter of max 0.2mm can be used.

Table 3.1: Via types and sizes

	Diameter hole [mm]	Via type	Manfacturing type	Layer pair
Vias to outer layers	0.2	Blind	Laser drill	1-2 and 5-6
Vias to die/coin	0.2	Buried	Laser drill	2-3 and 4-5
Vias trough PCB	0.45	Buried	Regular drill	2-5

3.2.3. HV clearance & creepage

Since compatibility with HV SiC devices of up to 1.5kV is needed the spacing requirements of the traces needs to be taken into account. First it is important to understand how the spacing is defined, there is clearance and creepage. Clearance is the shortest direct distance going trough air. Creepage on the other hand is the distance over the surface that 2 conductors share. This is made clear in figure 3.4.

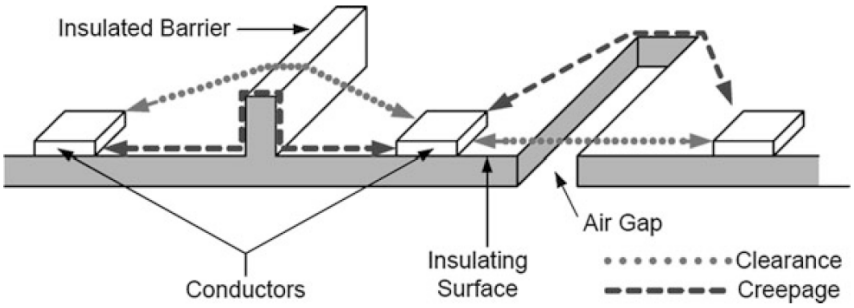


Figure 3.4: Clearance and creepage definitions[17].

There are a multitude of reasons for needing a larger distance between traces at high voltages. The most obvious problem is electrical breakdown and arcing. Other less directly noticable issues are electrochemical migration and Conductive Anodic Filament (CAF) growth, in both cases traces of copper, silver or other conductive materials form thin wires in between the traces which reduces the distance and will eventually result in breakdown.

The first parameter to look at is the breakdown voltage of air at 3000V/mm. For 1.5kV this would mean having a spacing under 0.5mm results in arcing. But because of other breakdown mechanisms more space is needed. One way to measure this is by using the Comparative Tracking Index (CTI). The CTI is measured by observing when breakdown occurs at a distance of 4mm after 50 drops of 0.1% ammonium chloride solution on the material. The inner layers of the used PCB material has a CTI of 340V and the outer layer 600V.

There are many standards all with different design rules and requirements:

- IEC-61950-1
- IEC-60664
- IPC-2221
- IPC-9592B
- UL-60950

They all have different tables or formulas to calculate the minimum required spacing depending on CTI value, pollution factor, medical use, material or even height above sea level. Most commonly when there is no regulatory reason (like medical or military use) the IPC-2221 standard is used for PCB design. In this case at 1.5kV that would give a distance of 2.75mm. With this information in mind a distance of 3mm has been chosen which is on the safe side since enough space was available.

3.2.4. Placement accuracy

Fiducials are features on a PCB that are used for camera based inspection and manufacturing. They are easy to detect shapes of a known size on a known location. In this case a small square and circle have been added to the top left corner for this. During manufacturing of multiple PCBs in a panel these can be used as reference for milling the PCB out of the panel.

Placement of the embedded device was done manually in this case, using the edge of the copper coin as reference. But for automatic placement fiducials on the inner layers could be needed as well.

3.2.5. Stackup and materials

The stackup consists of 6 copper layers, of which 2 are not used electrically, with a total thickness of 1.592mm. See figure 3.5. The outer layers are used to connect to the pins and to radiate heat away using the copper area above the embedded dies. One layer lower from both sides is used for traces to connect the outer layer to the die in the middle, some extra dead copper is added all sufficient distance away from the traces just to keep it manufacture-able. And finally the 2 inner layers only consist of dead copper and a cutout for the embedded device.

The materials used are copper, and 2 different kind of FR4 like dielectric materials as replacement of regular FR4. The top and bottom dielectric layer are of a high thermal conductivity type which helps with the thermal path to the heatsink. In table 3.2 the CTI, glas transitiong temperature Tg and thermal conductivity λ are given. Because of the high voltage and high temperature there is compatibility with SiC devices.

Table 3.2: Material parameters of inner and outer PCB layers.

	CTI	Tg	λ
Inner layers	340V	300°C	0.5W/(m·K)
Outer layers	600V	300°C	10W/(m·K)

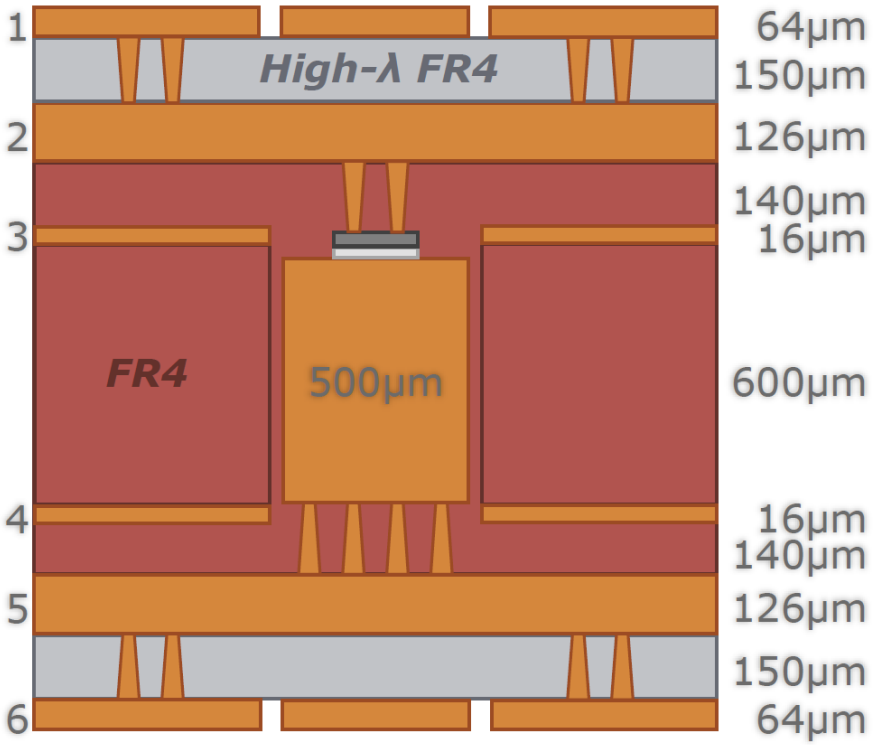


Figure 3.5: Stackup showing the 6 copper layers and dielectric FR4 like materials with thicknesses, with a total thickness of 1592µm.

3.3. Copper coin

To embed the MOSFET it is attached to a piece of copper, here called a copper coin. A frame with multiple coins is designed. The copper coin is used as a leadframe to attach the die to using silver

sintering. It's size and shape needed to be determined to make it suitable for embedding. A size of 5x6mm and thickness of 500um have been used. 5x6mm is the same size as the LFPAK56, this way a reasonably fair comparison in performance can be made. Since the die is 3x3.9mm and centered this gives at least 1mm around it on each side. The thickness is chosen so that the total thickness with the die on top fits in the inner PCB layer. The coin has rounded corners to make it easier to manufacture with one corner in a different shape to indicate the gate location of the die. This makes sure the coin can only be placed in the PCB in one way.

In figure 3.6 you can see how the copper coins are designed to be manufactured. A frame of 5x5 coins is made where the coin is connected at one point. Since this is a research project it has to be easy to manually handle which is the reason for the relatively large space between and around the coins.

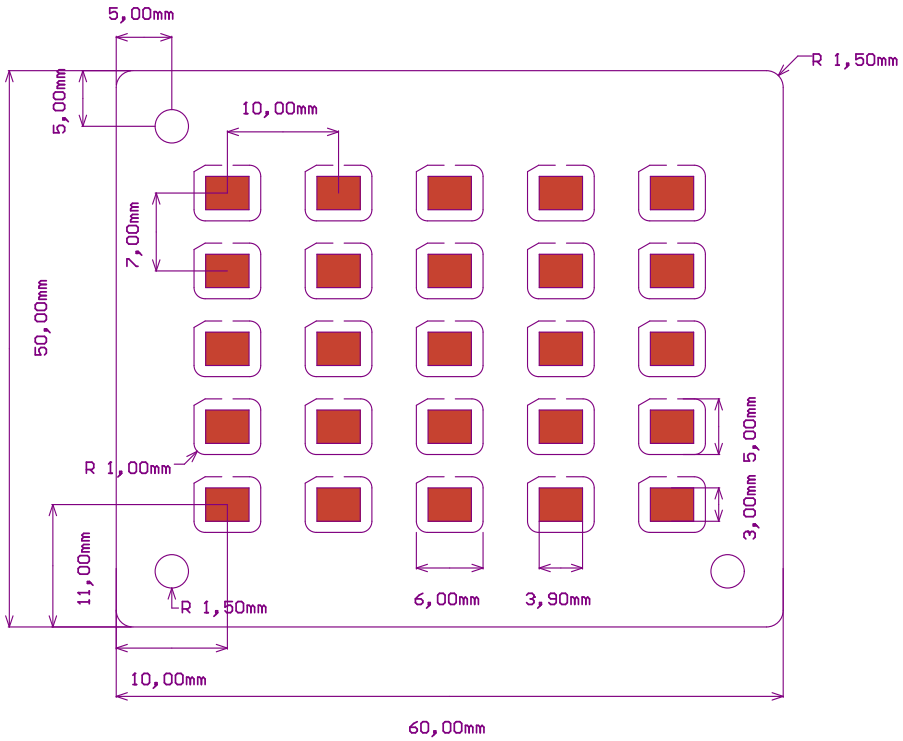


Figure 3.6: The designed copper coin frame schematic to be used for manufacturing, showing 25 copper coins of 5x6mm with a silver spot of 3x3.9mm.

The die will be sintered to the coin, but it cannot be directly sintered to copper. So a silver spot is made on each coin. The silver spot is applied to the coin using photolitography and immersion silver coating. The steps to do this are as follows:

1. Photoresist is added with openings where the silver spot goes.
2. The Cu surface is micro etched to clean it and prepare it to for Ag coating.
3. Immersion silver coating, this exchanges Cu and Ag atoms.
4. The photoresist is removed.

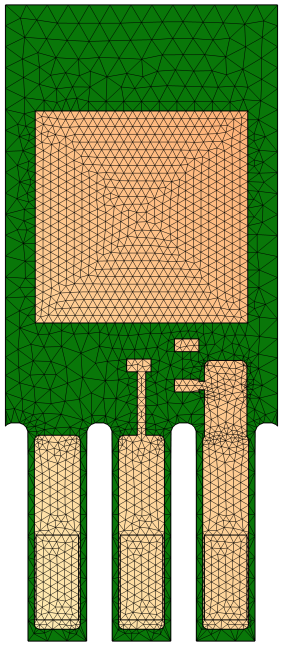
3.4. Finite element analysis

As mentioned at the start of the chapter simulations have been used to verify and optimize the design. This is done to get an indication in advance if and how embedding has an effect on performance without

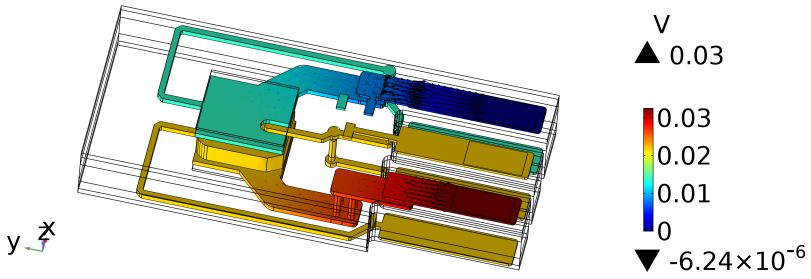
going through the whole manufacturing process. Design parameters like PCB stackup, materials, trace widths and copper area size can all be changed easily.

The finite element analysis(FEA) is done using COMSOL. This means a model is split into a finite amount of small elements and numerical physics calculations can be done on those. In this case a 3D model of the PCB including the embedded Cu coin and die is used. Electrical and thermal calculations have been done.

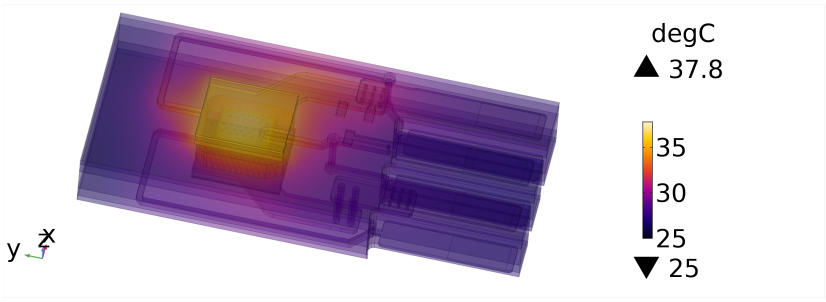
To get a working simulations first the model has to be prepared. First the model has to be made or imported, materials have to be defined, next boundary conditions have to be defined and finally the model has to be split into small elements called a mesh. This will be discussed in the setup section bellow. Next the resulting data will be shown in plots and 3D heatmaps in the results section that follows. The current density, voltage distribution, heat distribution and calculated thermal impedance will be discussed.



(a) Mesh top view.



(b) Voltage/current simulation small area example.



(c) Temperature simulation small area heatsink example.

Figure 3.7: A mesh view of the simulation with electrical and thermal results which will be explained after the setup below.

3.4.1. Setup

The very first step is defining the geometry, the “ECAD file import” function was used. This imports all 3D geometry information into the working environment from in this case an ODB++ file. This file was exported using Altium, which is the PCB CAD software used to design the PCB. This way all layer and trace information is available in the simulation after minimal cleanup of the imported file. Since the PCB contains 4 embedded devices it was cut to only 1/4 of the PCB to only simulate a single device. Since the middle 2 copper layers are very thin and to optimize the model they have not been included.

Materials are defined using either build in material from COMSOL or using datasheet parameters. Below the used materials are described and in table 3.3 the used parameters are shown.

Copper All traces and vias are made of copper, since the model was imported it was easy to select them all without further modifications.

Inner PCB layers An FR4 alternative with high Tg was used, the datasheet parameters have been filled in.

Outer PCB layers An FR4 alternative with high Tg and high thermal conductivity was used, the datasheet parameters have been filled in.

Silicon The complete chip is defined to be pure silicon, no doping or trenches have been used to keep the simulation simple, instead the conductance was experimentally calculated to get an 1mΩ resistance.

Sinter material The hybrid silver sinter material was defined by changing the build in silver material using datasheet parameters.

Below the parameters that have been used for that materials in the simulation are listed:

- Electical conductivity, σ, (S/m), the electical conductivity is used for the electrical simulations, it will influence the voltage distribution and current density.
- Heat capacity, C_p, (J/(kg·K)), the heat capacity is used during the thermal simulations
- Relative permittivity, ε, the relative permittivity is used during the electical simulations.
- Density, ρ, (kg/m^3), the density is used for thermal simulations
- Thermal conductivity, k, (W/(m·K)), the thermal conductivity is used for thermal simulations

Table 3.3: Material properties used during the simulations.

Material	σ(S/m)	C_p (J/(kg·K))	ε(-)	ρ(kg/m^3)	k (W/(m·K))
Copper	5.998e7	385	1	8960	400
Inner layers	-	860	4.4	2000	0.5
Outer layers	-	800	4.4	3000	6
Silicon	1e4	700	11.7	2330	85
Silver sinter material	1e6	235	1	9336	130

After defining the materials the physics simulations have to be setup. Starting with the electrical simulation. First the materials that are involved have to be selected, then the boundary conditions have to be defined. Starting with current conservation which applies to everything. Then electric insulation which applies to the outside surfaces of the model, this means no current can enter or leave through those surfaces. The initial voltage of everything is set to 0V. Finally the source is permanently set to 0V and the drain has a current of 10A entering it. This fully defines the electrical part of the simulation.

For the thermal simulation again first all materials have to be selected. The initial value for everything is set to 25°C. All outside boundaries are automatically defined as insulation, this will be overwritten by the next definitions. Starting with heat flux, here all outside boundaries are defined to be in air so there is heat transfer due to convection. Since only a 1/4 slice of the PCB is simulated a symmetry option is added to the sides of this slice so it is as if the rest of the PCB is actually there while using less computational resources. To simulate having a cooling plate attached to one side of the PCB the temperature of the top or bottom is set to 25°C. And finally a heat source of 10W is defined, a volume of 2.6625mm x 3.5625 x 5µm at the top of the die is used for this. This is were the active area of the MOSFET is. It was already experimentally confirmed to give accurate simulation results by the die manufacturer so this volume was used.

The last step needed before the simulation can be run is to define a mesh, which means separating the model into small elements. The minimum element size shouldn't be smaller than the smallest feature size, which in this case will be the via sizes. The size of the elements will determine the resolution of the results so a big element size is also not desired. But smaller elements also increase the computation time, so an optimization between resolution and computation time has to be made. After changing the minimum element size, maximum element size and related parameters the mesh is generated as shown in figure 3.8

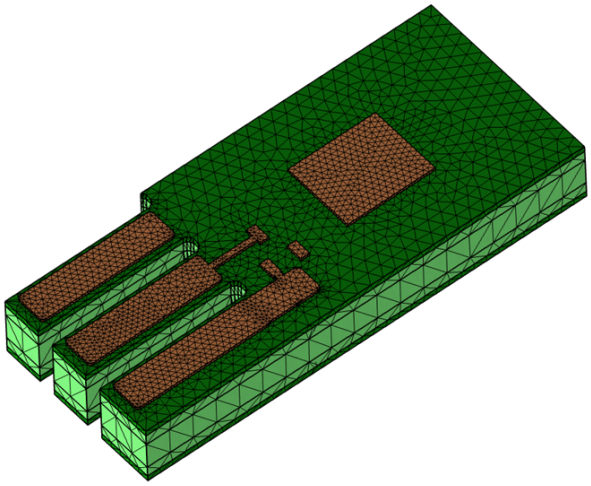


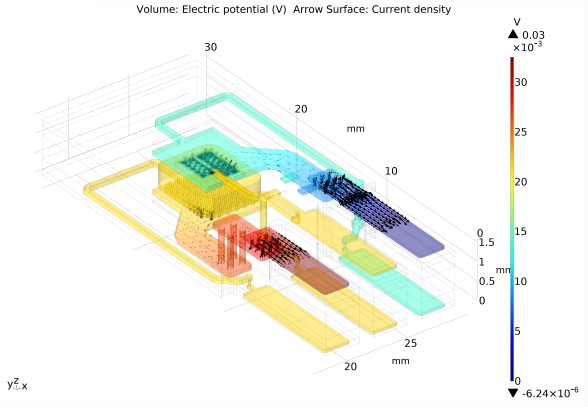
Figure 3.8: The section of the PCB to be simulated is divided into small elements called a mesh as seen here.

3.4.2. Results

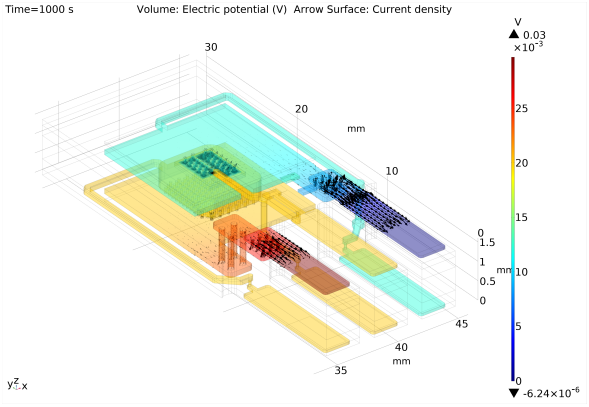
Now that the simulations have run, the results can be analyzed. A time independent study was done for the electrical simulations and a time dependent study for the thermal simulations. Time dependence was used for the thermal simulations to be able to generate a thermal impedance graph of the device heating up over time.

Figure 3.9 show a colored voltage distribution and arrows for the current distribution. First focusing on the voltage distribution it is clear that there is a small voltage drop from the drain and source force pins to the area in the center as expected. But the main voltage drop is over the die itself, this shows that the sense wires that run around the top and bottom areas to the drain and source sense pins on the bottom do actually measure the die. This is required for a kelvin connection and a desired result.

The current distribution shows that no current runs through the sense wires. The biggest current density is at the vias on top of the die and the vias connecting the pins to the rest of the trace on the PCB. Clearly the amount of vias on the back of the copper coin is more than needed to support the current density, but they are also used to transfer heat from the Cu coin to the next layer.



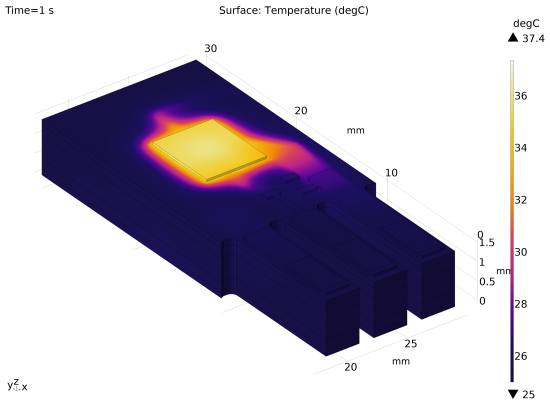
(a) Voltage/current small area



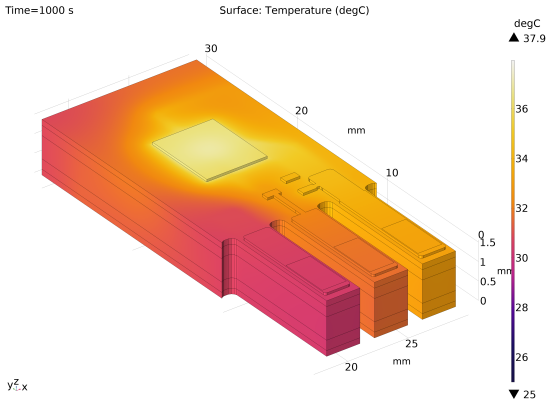
(b) Voltage/current big area

Figure 3.9: Voltage and current distribution simulation results showing a uniform voltage for the kelvin connection.

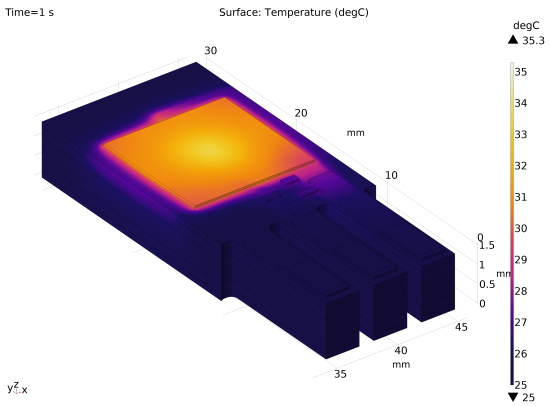
The thermal simulations ran from 10^{-5}s till 10^{3}s with 4 data points per decade. The simulations have been done for both the big and small area heatsinks with either the front or back heatsink connected to a cooling plate by setting it to 25°C. Figure 3.10 shows a top view of the big and small areas with backside cooling at different time steps. Here it already becomes clear that the heat mainly spreads to the copper on top and via the traces. The overall temperature for the bigger area is lower than the small area indicating better heat transfer to both the cooling plate and outside environment.



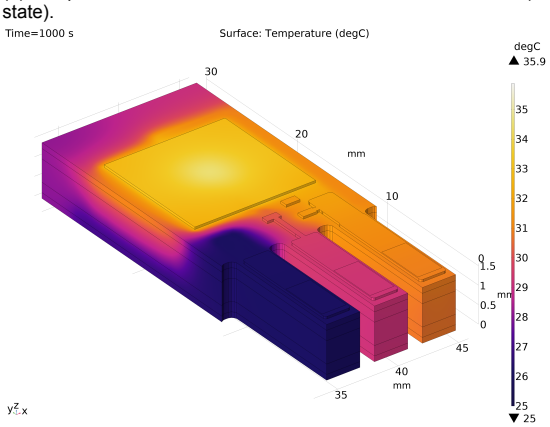
(a) Temperature simulation results for the small area at 1s.



(b) Temperature simulation results for the small area at 1000s(steady state).



(c) Temperature simulation results for the big area at 1s.



(d) Temperature simulation results for the big area at 1000s(steady state).

Figure 3.10: Thermal simulation results showing the temperature increase is greatest for the small area.

To quantise how well the heat is removed from the device junction to heatsink/solderpoint thermal impedance curves have been plotted. The thermal impedance here is defined as the temperature difference between the die and the area that is attached to the cooling block of 25°C divided by the input power. Resulting in the 4 curves in figure 3.11.

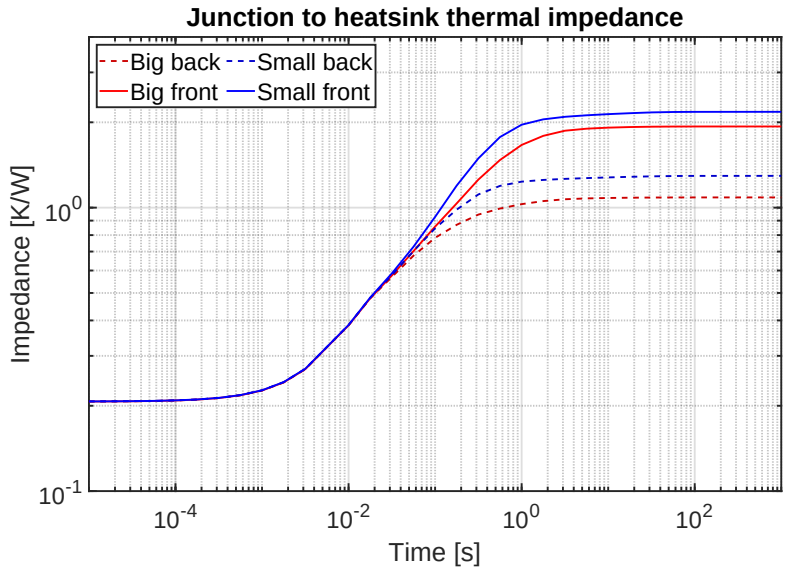


Figure 3.11: Simulated thermal impedance curves.

A lower thermal impedance indicates better heat transfer, so here we can conclude that from best to worst performance we have the big area cooled from the back, the small area cooled from the back the nig area cooled from the front and the small area cooled from the front. It also becomes clear that only for longer duration of over $3 \cdot 10^{-2}$ different in cooling area or side makes a difference. Measurements similar to the simulations have been done by attaching a cooling block, resulting in a similar conclusion, see section 5.2.2

4

Manufacturing

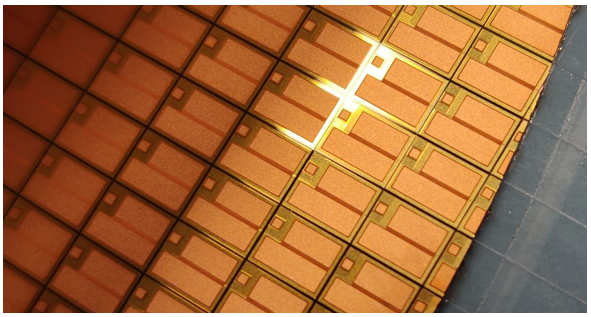
A working sample with embedded MOSFETs has been manufactured. To get to this working sample all parts have to be made, from the die and copper coin to the PCB. Extra focus is put on the sintering step since this was the most challenging and a manually done step.

Below is a list with an overview of manufacturing steps and thus what will be discussed in this chapter:

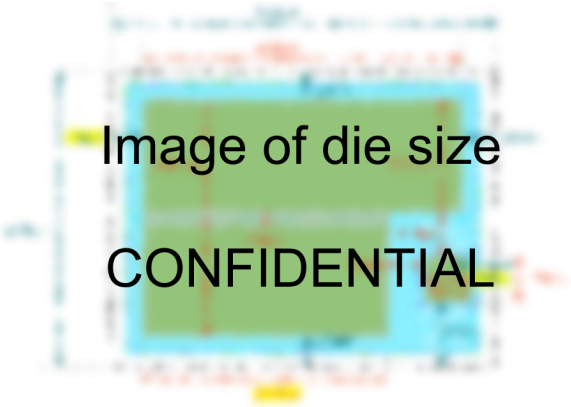
- A wafer with MOSFET dies with Cu top metalization
- Manufacturing of Cu coins
- Sintering of the dies to the Cu coins
  - Applying sinter paste using kapton tape mask
  - Placing the dies using a pick and place tool
  - Sintering in an oven using the correct temperature profile
- PCB manufacturing and embedding
  - Placing/embedding the Cu coin with die in a hole in the middle PCB layer
  - Laminating the top and bottom layers
  - Finalizing by adding vias, traces, soldermask, etc

4.1. MOSFET die with copper top metalization

The embedded MOSFET is prepared by taking a wafer with regular Si MOSFETs and adding a top metalization layer. Figure 4.1a shows the manufactured die and figure 4.1b shows the size schematically.



(a) Wafer with MOSFET dies with a copper top metalization.



(b) Die size specifications.

Figure 4.1: Die picture and specifications.

Table 4.1: Die specifications.

BUK7Y1R4-40H	
Type	Si N-channel Trench MOSFET
Die size	3.9 mm x 3.0 mm x 70 µm
Metal top-side	Pure Cu, tCu = 10 µm
Passivation protection	Polyimide, tPI = 5 µm
Metal back-side	TiNiAg, tTiNiAg = 0.6 µm

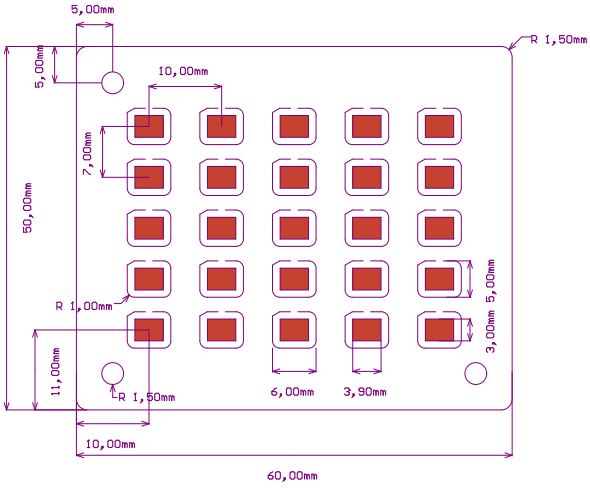
As specified in table 4.1 a Si N-channel MOSFET is used. To manufacture this regular MOSFETs standard processing steps are done. Starting from a Si wafer and then layer by layer patterning and doping the features like trenches, gate, source, etc. For embedding an extra step is needed to get a copper top metal layer. As explained in previous chapter this is done so vias can attach to this layer. The top metalization is a 1P1M (1 poly layer and 1 metal layer) of copper and polyimide. The backside is TiNiAg which didn't need any modification since this can easily be silver sintered. Below the steps to add the top copper layer are listed:

1. A seed layer of 300nm is sputtered on the whole wafer.
2. A photoresist layer is added to pattern the copper above the gate and source area.
3. copper gets galvanicly plated on top of the exposed parts of the seed layer by running a current trough the seed layer and suspending the wafer in a solution with copper ions.
4. Once a 10 µm thick copper layer is plated on top of the seed layer the resist will be removed.
5. As a last step the seed layer will be etched away.

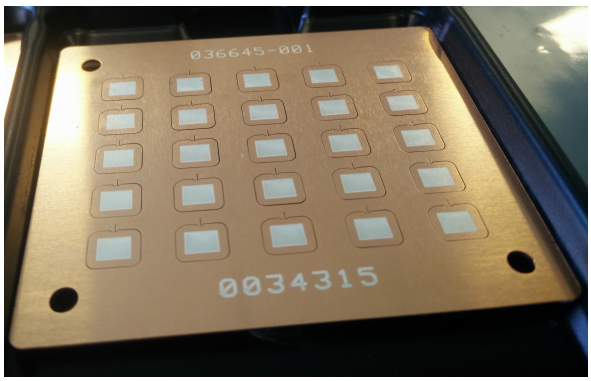
4.2. Copper coin frame with silver spot

The copper coin frame manufacturing steps will be explained in this section. The die will be bonded to the copper coin and then placed into the PCB.

The copper coins are 5x6mm and .5mm thickness with a silver coated spot the size of the die in the middle. The silver spot is used for better adhesion to the silver sinter paste. These coins are delivered in a frame with 25 per frame, at a distance of 10x7mm away from each other as discussed in the design chapter, and see in figure 4.2.



(a) Design drawing to manufacture the cu coin frame.



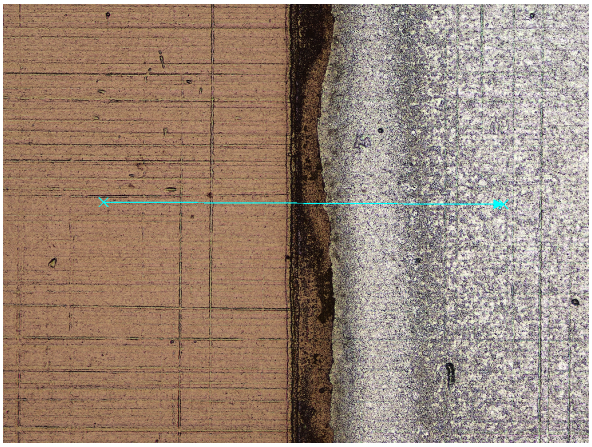
(b) Manufactured cu coin frame.

Figure 4.2: Cu coin frame with 25 copper coins and silver spots.

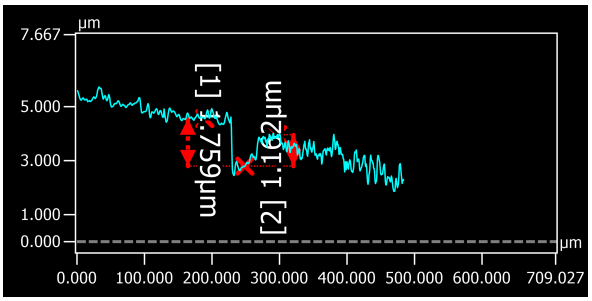
The manufacturing ideally starts with a copper sheet of the correct thickness. Optionally a first step is etching or plating copper on a sheet that is too thick or thin respectively. Next the silver spot is made, this is done in 4 steps:

1. Photoresist is added with openings where the silver spot goes.
2. The Cu surface is micro etched to clean it and prepare it to for Ag coating.
3. Immersion silver coating, this exchanges Cu and Ag atoms.
4. The photoresist is removed.

Once this is done the Cu coins are lasercut in the correct shape. After the manufacturing the frame consists of only copper and silver.



(a) Mousebite microscope picture.



(b) Height measurement of the mousebite.

Figure 4.3: Mousebite measurement showing a small trench between the copper and silver.

During the making of the silver spot a small undesirable trench is etched around it as a side effect. This phenomena is called mouse bite and becomes issue when applying sinter paste. This impact be discussed in the next section.

4.3. Sintering of the die to the copper coin

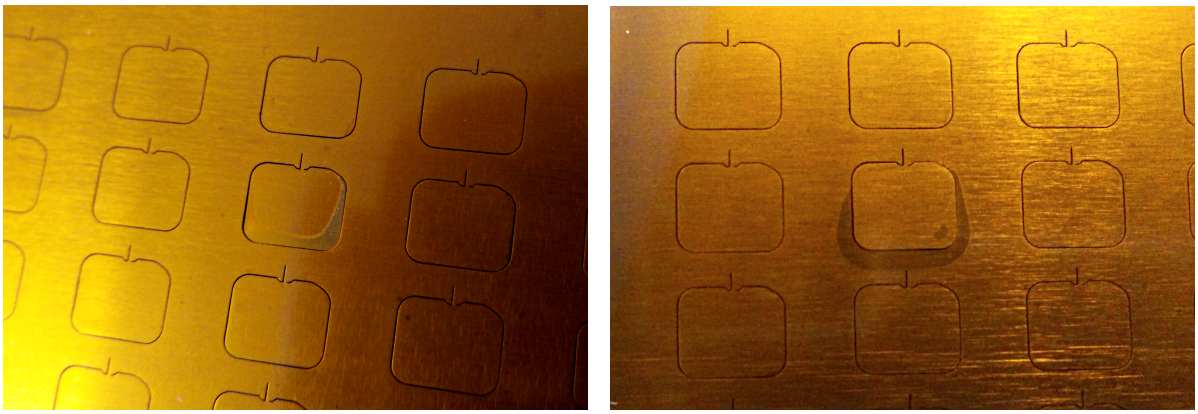
The die with copper top metalization and the copper coins with silver spot have to be attached to each other in a leadfree way. During the sintering trials multiple ways of applying the sinter paste and placing the dies have been tried. First the final list of manufacturing steps will be elaborated on. Next the challenges that have been found using other methods will be explained to make clear why they haven't been used.

4.3.1. Manufacturing steps

The process all the way from applying kapton tape until sintering the die in an oven will be discussed here.

Preparation before placement

Since the copper coins all only have 1 connected point to the rest of the frame they can tilt in multiple directions. This issue is also known as die paddle tilt. So kapton tape was used at the back of the frame to keep the coins flat and so it can stick to the vacuum suction of the table on the Finetech. From the air bubbles that form when applying the tape you can see in which direction the coin is bend. They need to be gently pushed in the correct direction to remove all bubbles so all coins are as flat as possible relative to the frame. This is shown in figure 4.4 below.



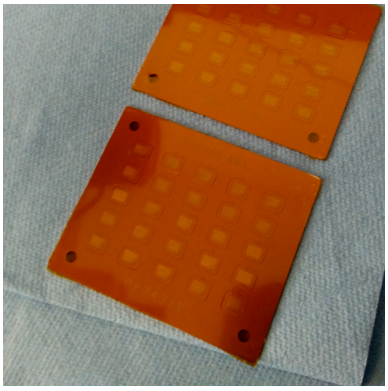
(a) Air bubble under the coin indicates it is bend up.

(b) Air bubble around the coin indicates it is bend down.

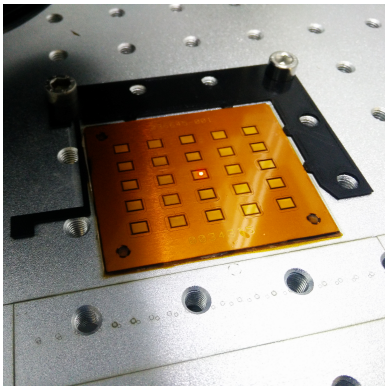
Figure 4.4: After applying kapton tape on the backside air bubbles will show how the coin is bend(this bending is also known as die paddle tilt).

The next step is applying sinterpaste, to do this first a mask of kapton tape is made on the front side. An overview of the steps needed is shown in figure 4.5.

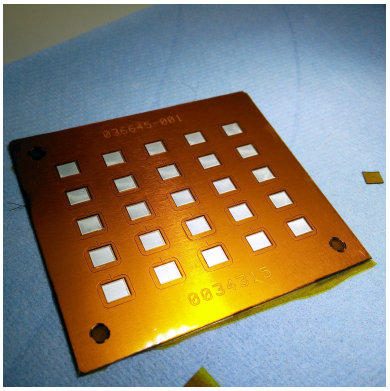
(a) High temperature kapton tape and tools



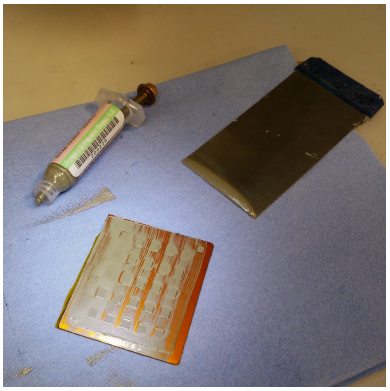
(b) Both sides of the frame have a layer of tape applied to them



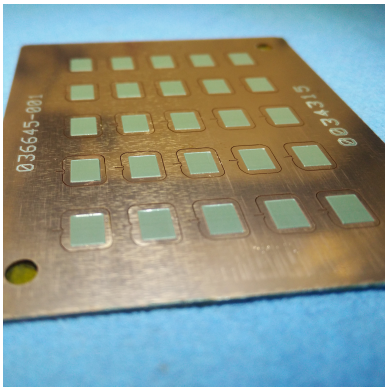
(c) Openings are cut using a laser and 3D printed mall



(d) Tape rectangles are removed to expose the silver spot



(e) Sinter paste is applied using a squeegee



(f) Tape is removed to end up with paste over all silver spots only

Figure 4.5: Steps and tools needed to apply sinter paste.

To make a mask for stencil printing kapton tape is put on the front side. 2 layers of tape with a thickness of 30µm each are used for a total of 60µm. One layer of tape and a metal stencil was tried as well with worse results, this will be discussed later in this chapter in the challenges section 4.3.2.

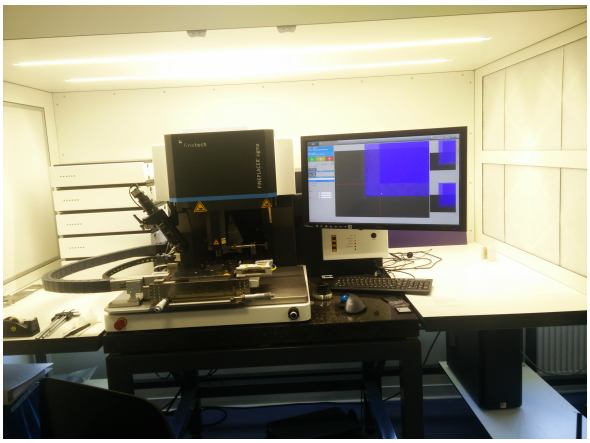
Openings are cut in the tape using a Huaray fiber laser. To align the frame with the laser a 3D printed mall has been designed, shown in subfigure 4.5c. The openings were cut larger than the silver spots, 3.4x4.4 mm instead of 3x3.9mm, since the aligning was done manually and not accurate enough to exactly line up.

To make the opening the tape rectangles that have been cut need to be removed using tweezers. This is done under a microscope, it is important to not accidentally scratch the copper coin with the tweezers.

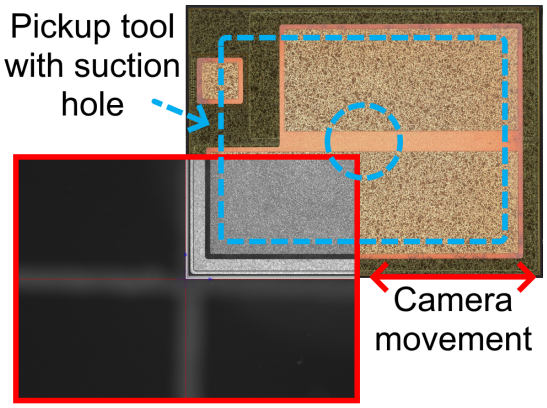
Next sinter paste is applied using a squeegee. The squeegee has to be held as horizontal as possible and apply a only small a mount of pressure to make sure paste goes in all openings.

Finally the tape is removed to reveal the frame with paste only in the middle of each copper coin. The frame is now ready to have dies placed on it.

Placement of dies



(a) Finetech sigma placer, this was used to accurately place the dies on the Cu coins.



(b) Pickup tool camera FOV and movement.

Figure 4.6: Finetech sigma placer tool and camera view.

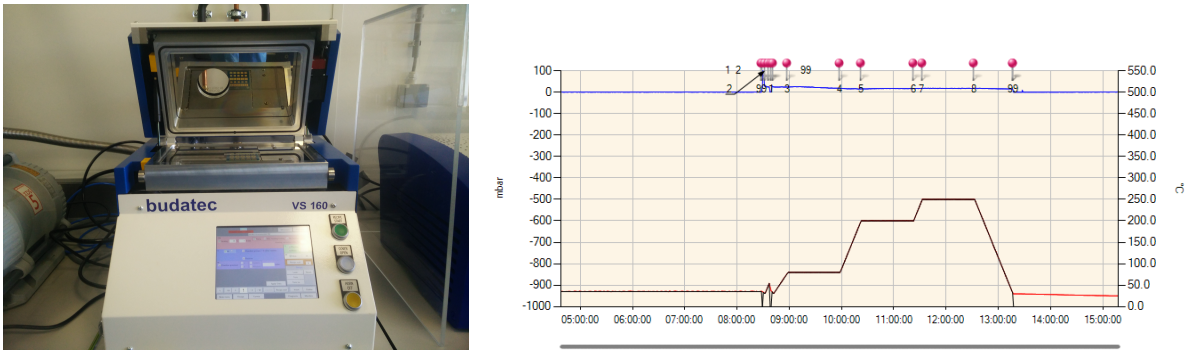
The next step is using the Finetech sigma placer, see figure 4.6a, which is a pick and place tool with 0.5µm placement accuracy by using cameras and optics to align the die to the copper coin. It has a movable table to position the Cu coin frames and an arm to pick up the dies. Placement can be done with a set force or distance from the surface by doing a touchdown first to calibrate the 0 height.

First the setup of the machine had to be done. The arm to place the die had to be aligned with the camera manually. In this case the camera is looking at the bottom left of the pickup tool(instead of exactly the center), this is done so it is easier to see the rotation of the die once picked up since the camera can only move sideways, see figure 4.6b. The next setup step is to show masks on the screen, this is so there is a colored overlay to see how to align the die. Once aligned the dies are placed on a gelpack which is located next to the arm so they can be picked up. The prepared Cu coin frame with sinter paste is placed on the table, this table can be moved manually by pressing a foot pedal for big movements, or using 2 rotating knobs for fine movements. On the screen both the pickup tool with picked up die and the frame can be seen at the same time, using the overlay you align them by moving the table.

The challenge here now is to place the dies at the correct height. To do this the touchdown option is used. Since the frame and Cu coin are now flat because of the tape a touchdown next to the paste is possible, this is the 0 height. Then the die gets placed on the paste at a set height of 55µm, this way the die is pushed into the paste for 5µm. Getting this height correct so the die sticks to the paste and no paste overflows was done by testing multiple heights from 50-65µm.

Sintering using oven with N_2 flush

Now that the dies are placed a Budatec oven, figure 4.7a, is used for sintering, it follows a heating profile and can be flushed with nitrogen gas to keep oxygen out. A modified sinter profile with a peak temperature of 250°C was used. The modification was adding a 1h preheat at 70°C, see figure 4.7b for the profile.



(a) Budatec vs 160, sinter oven, can setup thermal profile. (b) Budatek sinter profile used during manufacturing.

Figure 4.7: Sinter oven with temperature curve.

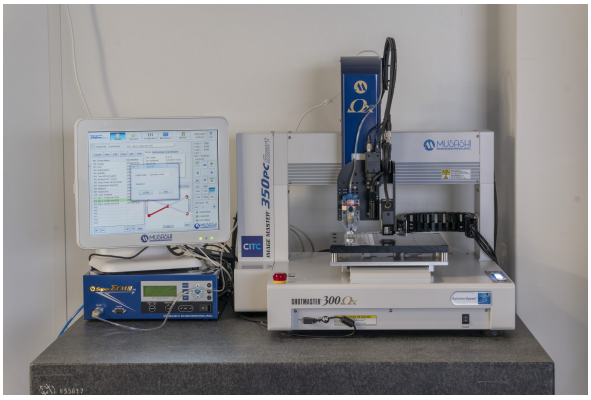
A hybrid pressure-less sinter paste was used as sinter material, which means it is a combination of silver particles and a glue with solvent.

4.3.2. Challenges & alternate methods

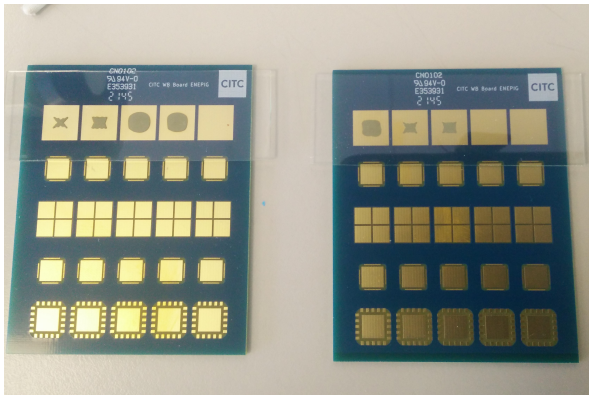
The main challenge is getting repeatability in placing dies correctly. There are 2 main parameters to get right, the thickness of the sinter paste and the flatness of the Cu coin or frame. With a too thick paste layer there is a big chance of overflow, which will short circuit the die. But with a too thin layer the paste dries out fast and risks having under fill/voids under the die or the die not sticking at all. If the Cu coin or frame are not flat the touchdown will not be at the same height as the paste, this again causes voiding, overflow or the die not sticking at all. This also includes the mousebite issue. How all these undesired phenomena are removed or reduced will be explained below.

Paste layer spreading and BLT

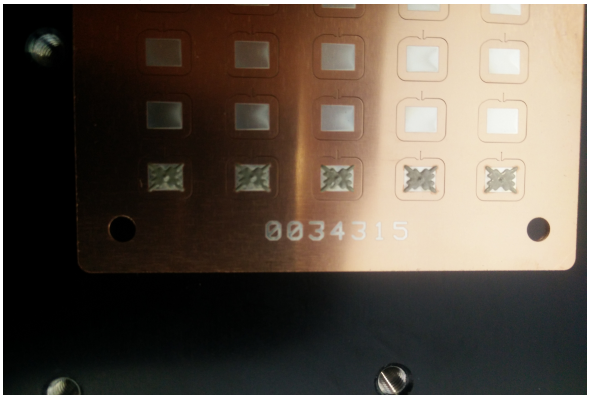
To get a reliable sinter paste layer thickness there are multiple techniques that can be applied. The first method that comes to mind is dispensing the paste on the copper coins and pressing the dies down on them to spread the paste.



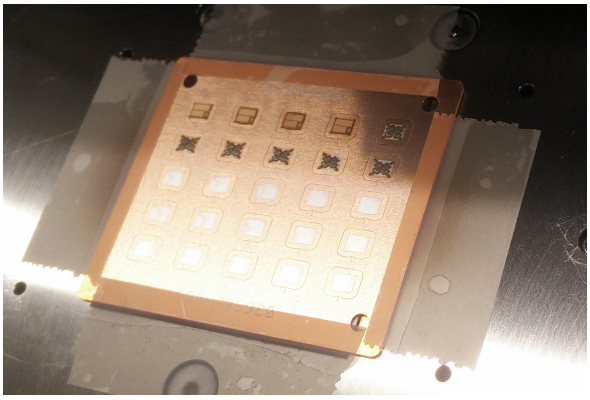
(a) Musashi image master 350pc smart, paste dispenser



(b) Dispense test using a glass plate



(c) Frame with paste before die placement.



(d) Frame with 4 dies placed, frame taped to keep it flat

Figure 4.8: Dispenser and setup.

A Musashi paste dispenser was used. It uses a laser and camera to scan the surface height for 3D alignment and air pressure for the paste dispensing. The parameters to be determined are the pressure, needle size, dispense gap and dispense pattern. These parameters were experimentally determined. In the end the following parameters were used:

- pressure: 32kPa
- needle size: purple needle of 21 ga
- dispense gap: 0.15mm

The used pattern with these parameters was cross shaped and can be seen in figure 4.8c. The goal was to get the pattern get as close to a rectangle as possible when a die is placed on top. Figure 4.8b shows a glass plate on top of different patterns to determine the best one.

In the end dispensing cannot give an accurate enough small amount of paste, even at low dispense pressure, it either gave overfill or under fill, rarely a good reproducible thickness.

The next option is using a stencil to apply the paste. Since here no 3D scan is made before applying the paste the flatness of the Cu coins and frame becomes important. So stencil printing using a metal stencil didn't work because the frames aren't flat enough. The silver spot mousebite makes a shape in the paste around the edge of the silver spot which aligned with the stencil opening further decreasing the reliability of stencil printing.

As solution a kapton tape mask was used as described in the sections above. This gives an accurate amount of paste and gets rid of the flatness issue since the tape sticks to the frame.

Frame flatness

The issue of the frame not being flat and the individual Cu coins not being flat in the frame was solved by applying tape to the backside as explained in the manufacturing steps. This solved the touchdown height not being the same as the 0 height when placing the die. Removing any overflow or voiding from this issue.

The problem of the mousebite around the silver spot could be removed by making the silver spot bigger than the placed die. Or the silver spot can be removed completely if the used sinter material can attach to copper, which is the case for the silver sinter material used here but wasn't verified. Another improvement to the frame would be to attach the Cu coins with 2 or more attachment points to reduce the degrees of freedom it has.

4.4. PCB manufacturing and embedding

The finished Cu coin frames with sintered dies on them are send to a PCB manufacturer to be embedded. There the Cu coins are singulated from the frame and embedded in the PCB.

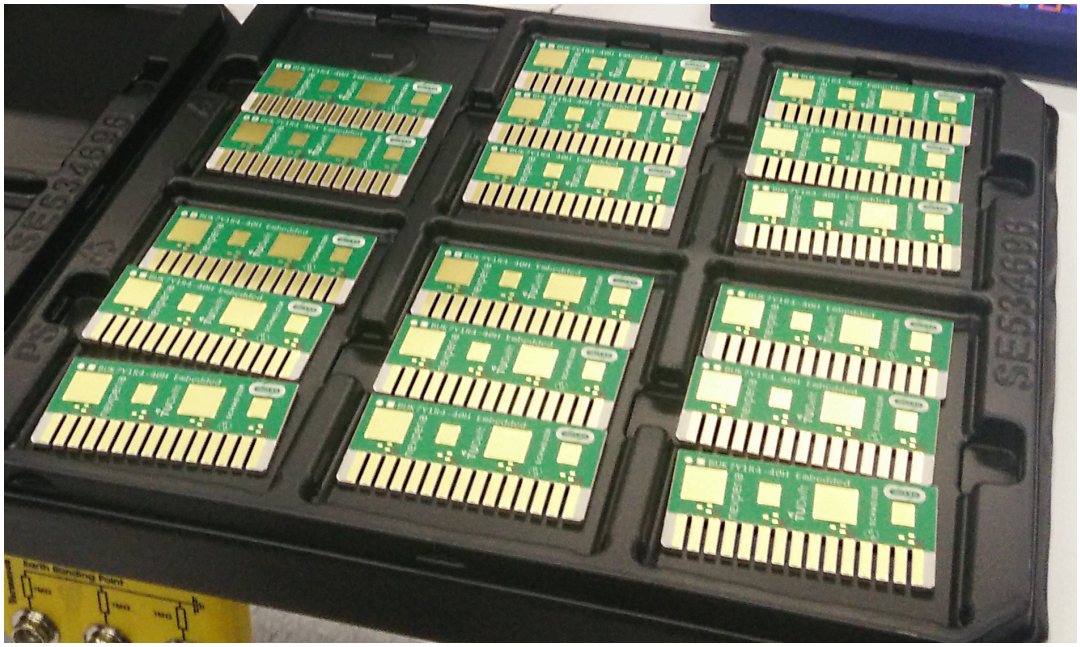


Figure 4.9: First batch of manufactured PCBs.

As described in the design chapter the PCB consists of 6 copper layers. Which can easily be manufactured using standard procedures. The only addition to the process is the embedding. To do this a cutout is made in the middle FR4 layer after patterning the traces on the copper to place the Cu coin. Then the layers above and below are laminated and regular PCB manufacturing steps remain. Here it is important to make sure no air remains around the embedded Cu coin by adding enough resin. Figure 4.10 shows an schematic illustration of the embedding process.

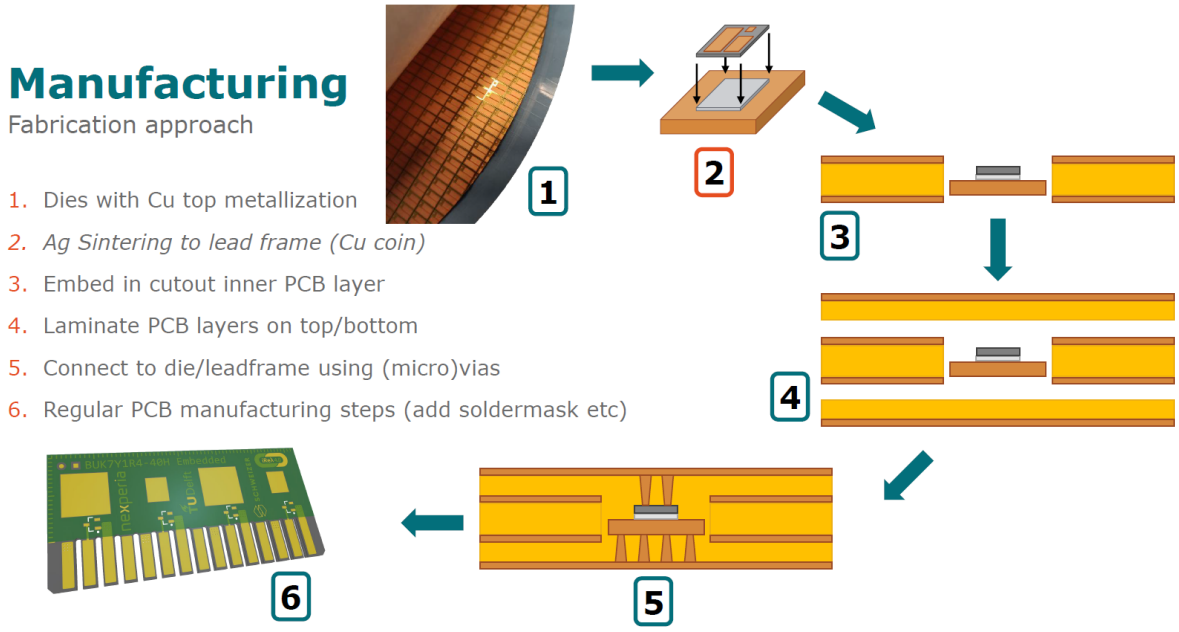


Figure 4.10: An overview of manufacturing steps from bare die to PCB.

In this case laser drilling of micro vias has to be done to attach the Cu coin and the gate and source on top of the die to the traces above it. After laminating the final layers regular vias are drilled, copper is plated on the top and bottom layer, soldermask is applied and the Electroless nickel immersion gold(ENIG) surface finish is applied to protect the copper from oxidation.

Some PCBs without embedded die have been manufactured as well for testing purposes.

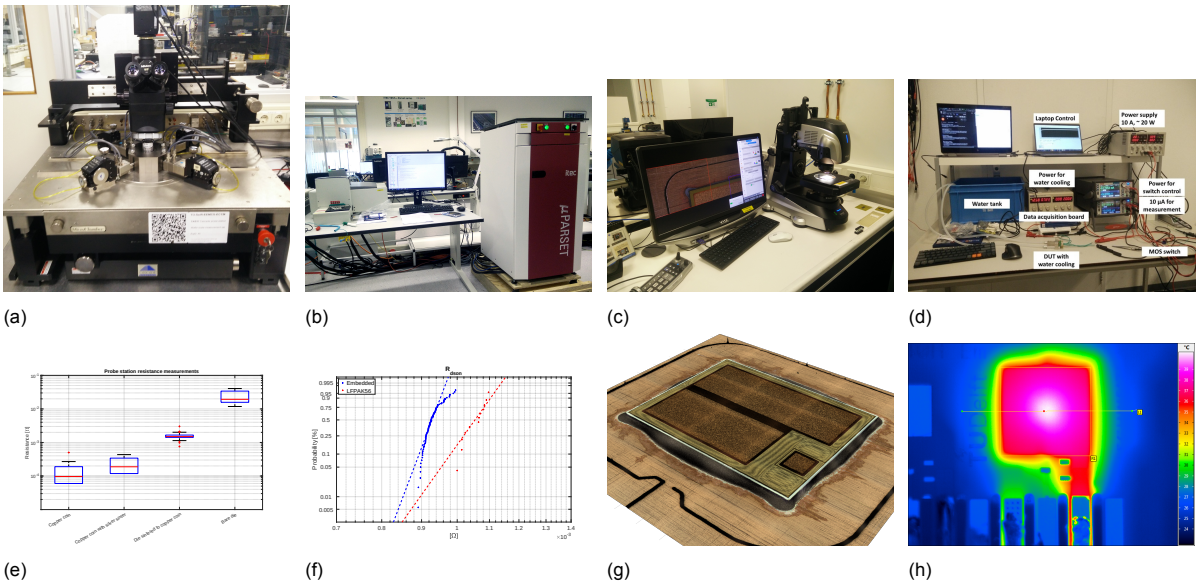
4.5. Conclusion

To summarize the manufacturing steps, we start with a wafer of bare dies and they end up embedded inside a PCB. So first the wafer gets a top layer of copper. Then a Cu coin frame is prepared to attach the die to. The die is attached to it using sintering by stencil printing with a kapton tape mask of 60µm thick, placing the dies with an accurate pick and place machine and putting them in a sinter oven. These Cu coins with dies are then embedded in the middle layer of the PCB and the rest of the PCB is build around it. From a manufacturing point of view some challenges have been solved to make all these steps possible. With these out of the way the process can be suitable for automatic stencil printing and pick & place machines for high volume manufacturing.

5

Measurements & characterization

The next step after manufacturing is to measure the embedded devices. Both the electrical and thermal characteristics have been investigated. Some measurements have also been done during the manufacturing. To quantise the embedded MOSFETs performance compared to the packaged version multiple electrical measurements have been done. During the manufacturing x-ray, height and placement accuracy measurements have been done before and after sintering. Functionality test have been done. And finally reliability tests are planned to be done. Figure 5.1 gives and preview of some measurement equipment and results which will be discussed in the sections to come.



(a) (b) (c) (d)

(e) (f) (g) (h)

Figure 5.1: A preview of measurement setups and results, to be discussed in the rest of this chapter.

5.1. Process measurements

During the manufacturing process multiple measurements have been done to verify if steps have been done correctly. Bond line thickness, gate placement accuracy, x-rays of the copper coins and probe

station resistance measurements have been done. They will be explained bellow.

5.1.1. Bond line thickness sinter paste

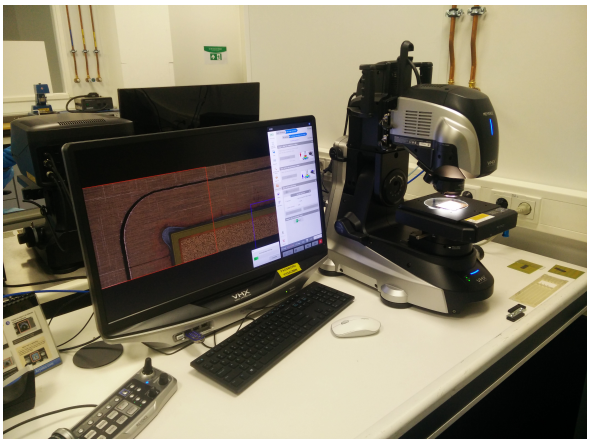
The bond line thickness(BLT) is an important parameter when attaching the die to the Cu coin. It specifies the thickness of the material between the die and the Cu coin. To get a certain thickness after sintering the shrinkage of the material during sintering has to be taken into account.

3 different methods of applying sinter paste have been used:

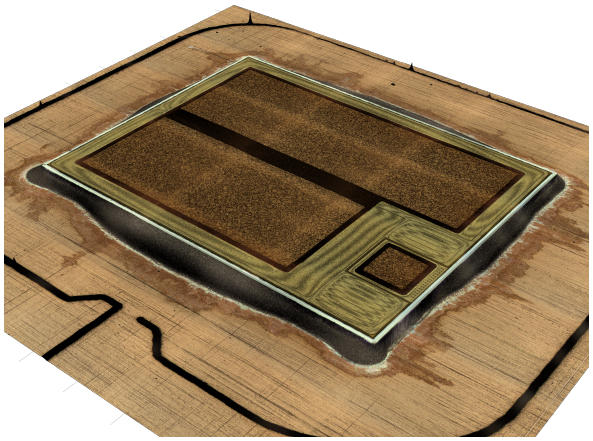
- Dispensing using a needle, with the goal of getting a 50µm BLT.
- Stencil printing with the goal of getting a 50µm BLT.
- Stencil printing with the goal of getting a 25µm BLT.

For each of these methods the BLT has been measured. Measurements were done before and after sintering to calculate the shrinkage for the dispensing method as well.

The measurement is done using a Keyence confocal laser scanning microscope. These types of microscopes use a laser to focus only on a small part of the sample at a time on different focal heights, this results in a 3D height map of the sample. The used setup can be seen in figure 5.2a. Here a 20x lens was used.



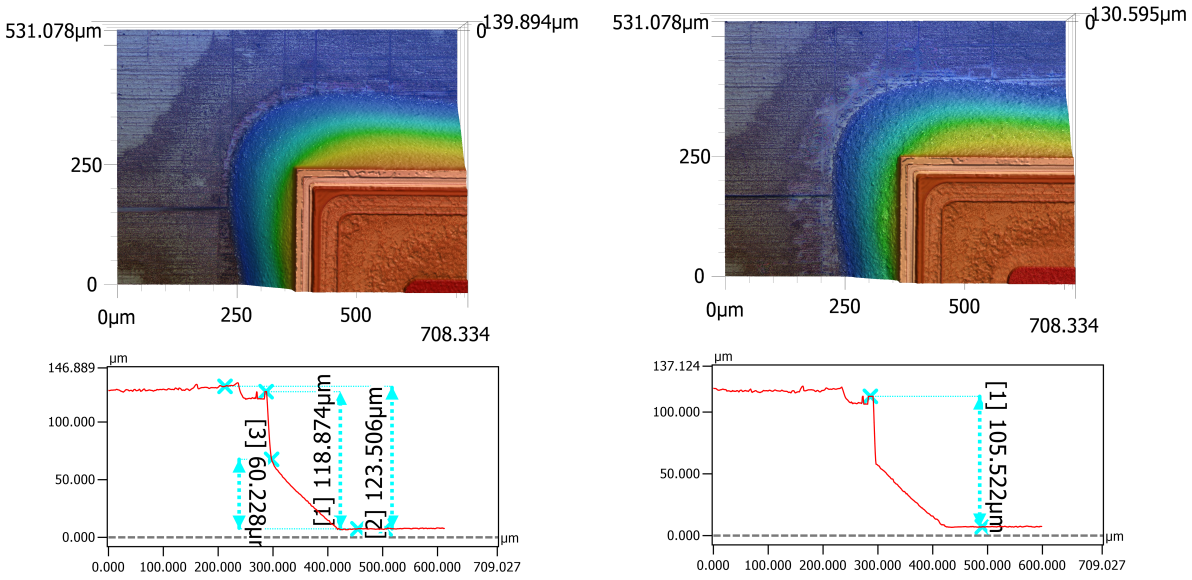
(a) Keyence confocal microscope used to measure BLT.



(b) Example 3D view with real colors of the measured die with sinter paste.

Figure 5.2: Measurement setup for BLT using a confocal microscope.

Starting with dispensed sinter material on the Cu coin and a 50 µm BLT goal measurements have been done. To get to this goal the die is placed at 60 µm above the coin, this is measured by a touchdown of the pickup tool on the frame next to the Cu coin. Figure 5.3 shows before and after sintering measurement examples for one of the dies.



(a) Before sintering

(b) After sintering.

Figure 5.3: Before and after sintering BLT measurements for dispensing.

From the measurements it became clear that there is a large variation in height before and after placement. The targeted heights and measured height of 50µm did not match either. Even tho there was a big variation in height the shrinkage standard deviation was low and the shrinkage was calculated to be 16% on average. The placement height problem seemed to be that the cu coins individually also had a height and tilt variation. And it turned out that the frame with Cu coin isn't completely flat. So this is measured next.

3 Cu coins in a row on a single frame without any sinter paste or other modification have been measured. As seen in figure 5.4 the Cu coins are not at the same height as the frame and each one has a different rotation and height. This is the main reason for the BLT to not be the same for the previous results. Since the touchdown height next to the frame isn't the same as the height of the Cu coin. As discussed in the manufacturing chapter putting tape on the backside solved this.

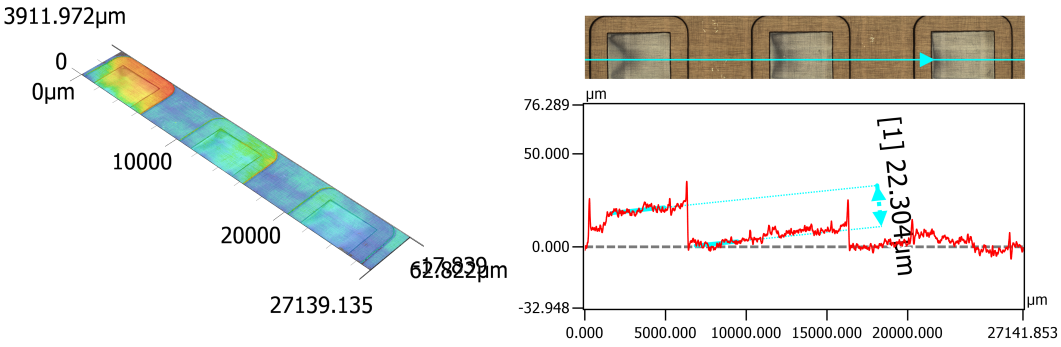


Figure 5.4: Frame flatness measurement showing variation in height.

The coin flatness has been fixed but dispensing still proved to be difficult to get the same thickness consistently. So as discussed in the manufacturing chapter stencil printing using 60µm of kapton tape as stencil was used.

The shrinkage was always around 16% and had a low standard deviation as expected even with the random placement height, so the next measurements are done only before sintering. In figure 5.5 the measurements on the 50um goal with kapton tape stencil can be seen. They show the coins are flat and the thickness is similar for the different dies. On average a height of 120 µm which means a BLT of 50 µm before sintering, which will become lower because of the shrinkage after sintering.

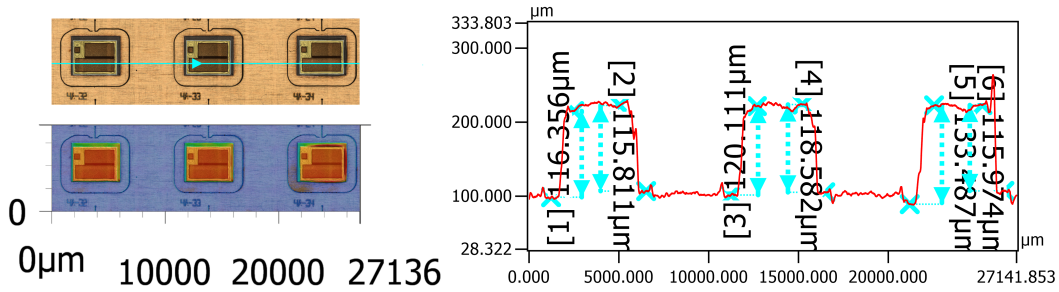


Figure 5.5: Stencil printed before sintering with a 50 µm goal.

Even tho the result shows dies with a preferred BLT, some of the devices still had the issue of paste overflow. When the die is placed some paste can be pushed up around the edges which causes this. This short circuits the device and is obviously not desired. To overcome this issue a test batch was made with a thinner BLT, so there is less material that potentially overflows.

Figure 5.6 show one of the same measurements but for a 30 µm goal. Also showing a good BLT with little variation between different dies. But with the issue of paste drying too fast, causing dies not to stay attached to the paste.

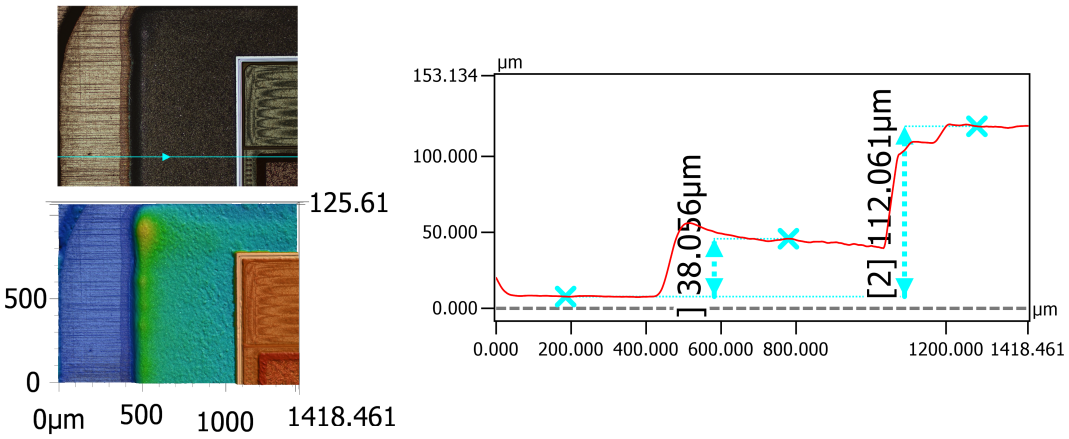


Figure 5.6: Stencil printed before sintering with a 30 µm goal.

Table 5.1: Dispense BLT before, after and shrinkage. Using a 60µm stencil before sintering. And using a 30µm stencil before sintering.

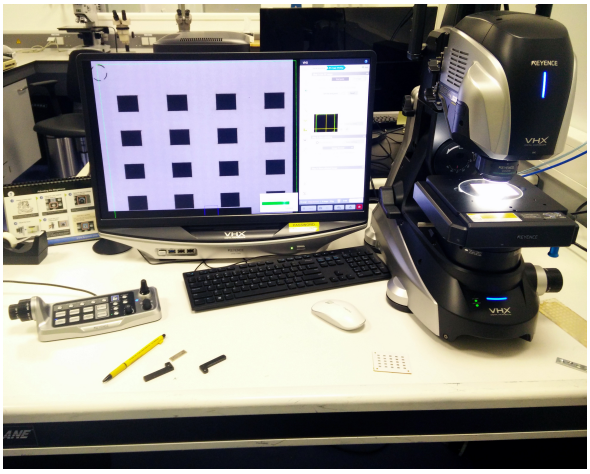
Dispense			**Stencil 60µm**	**Stencil 30µm**
Before [µm]	After [µm]	Shrinkage [%]	Before [µm]	Before [µm]
105	68	21	49	35
49	35	12	50	36
66	41	10	58	39
30	20	18	60	41
85	60	16	60	41
70	49	15	61	42
72	50	15	61	43
62	40	17	63	44
70	45	18	68	47
Standard deviation				
21	14	3.3	6.0	3.8

To conclude table 5.1 shows an overview of the BLT measurements. Measurements for dispensing before and after sintering are used to calculate the shrinkage. And measurements for a 60µm and 30µm stencil have been done. For all the standard deviation is calculated showing a high deviation for dispensing, a very low deviation for the shrinkage and low deviation for both stencils. So in the end a 60µm kapton tape stencil mask gave the most reliable results after removing the coin height variations using kapton tape on the backside. This issue can be fixed in a future Cu coin frame design by attaching the coin from multiple points.

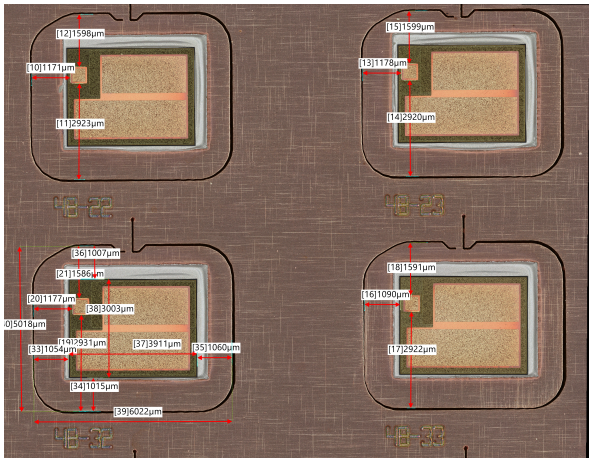
5.1.2. Gate placement accuracy

During the manufacturing multiple measurements had to be done to make sure the Cu coins actually meet the specifications required for embedding. The placement accuracy is especially important since the vias need to connect to the right spot on the dies.

A Keyence confocal microscope has been used to do the measurements. The distance from the gate to the left side of the Cu coin is used as X axis measurement and the distance from the gate to the bottom as Y axis measurement. In figure 5.7 the equipment and measurement are shown. Besides the distance from gate to cu coin some extra measurements are done to confirm the measurements are correct since the cu coin and die size are known.



(a) Keyence VHX confocal microscope used to measure gate placement accuracy.



(b) Measurements of dies on Cu coin after sintering.

Figure 5.7: Gate accuracy measurements using a confocal microscope.

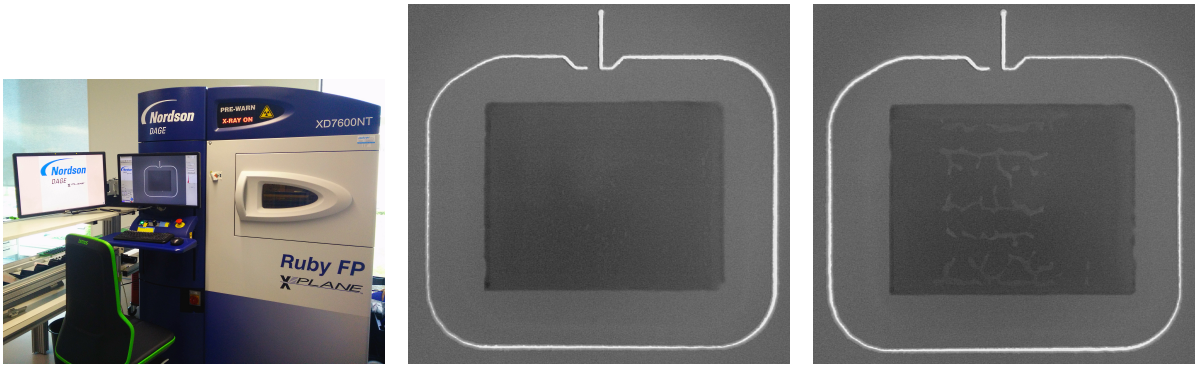
In table 5.2 the gate location measurement on the X and Y axis are shown with their error from the ideal placement. measurements have been done on 21 samples spread over multiple frames. The gate is 500 µm wide and the via that connects to it is 200 µm wide, so there at most is 150 µm of play in the placement on either side. So with an error of over 150 µm the via will not fully be in the gate area anymore. The table clearly shows the placement error is small enough to be used in this case with all vias landing on the gate..

Table 5.2: Gate location measurement results, all in µm.

Location	Goal	Min	Mean	Max	Min error	Mean error	Max error
X measurement	1180	1168	1177	1187	-12	-3	7
Y measurement	2915	2909	2922	2937	-6	7	22

5.1.3. X-ray Cu coins

After sintering X-ray pictures have been made to check for voiding under the dies. These pictures are used for traceability, if a device fails a reliability test it is possible to check if that specific die had voids underneath it or not. The X-rays have been done using the Nordson dage XD7600NT with a 135kV 1.9W beam. Figure 5.8 shows the used equipment and an example of a die without voiding and one with voiding. Figure 5.8b shows the desired result after sintering, here the whole die is attached to the copper coin using the sinter paste. Unlike figure 5.8c where there are bubbles under the die, these can become failure points for the die to detach during prolonged operation.



(a) Xray equipment. (b) Sintered die without voiding. (c) Sintered die with voiding.

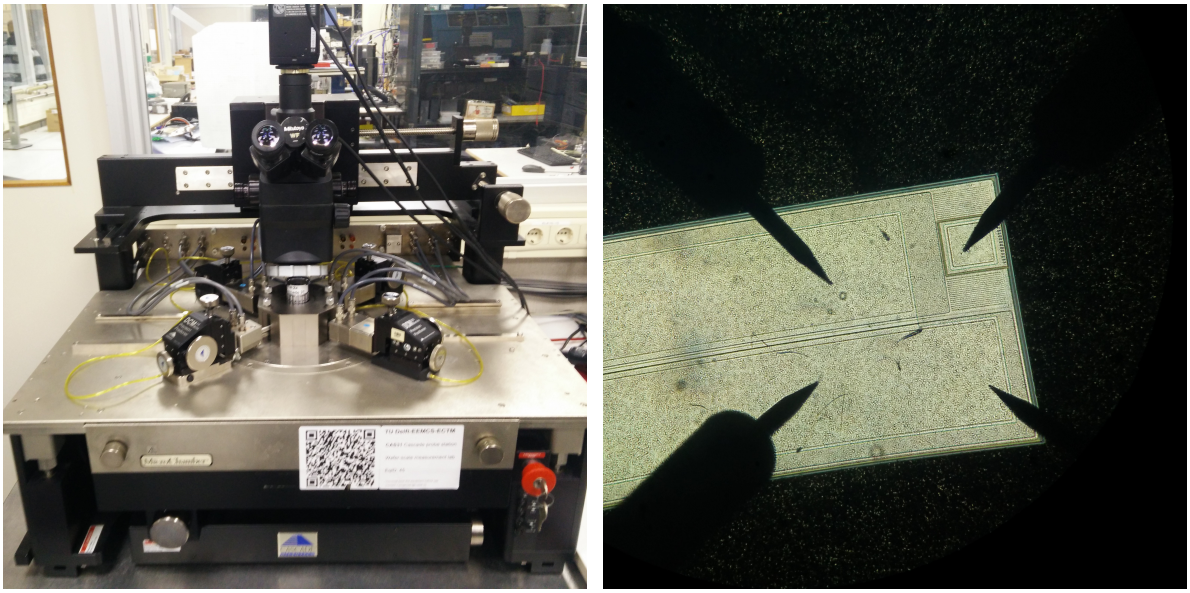
Figure 5.8: X-ray equipment and measurement images.

5.1.4. Cascade probe station Cu coin resistance

Some preliminary tests are done on the bare dies before they are embedded, the cascade needle probe station with HP 4156C analyzer was used at the ECTM lab. Only low power measurements are possible. The resistance of the bare dies and Cu coins with and without dies and paste on them have been measured.

To do this a 4 point measurement was done. The connection is done as follows: The die is placed on the chuck on top of a vacuum suction hole, 1 needle and the chuck (the plate on which the die lies) are used as electrical connection for the drain. The gate is connected with 1 needle to turn on/off the device. 2 needles are used to connect to the source, 1 to force a current and 1 to sense the voltage, so a current of 0A was forced on the sensing needle. The chuck is connected to force a current and the needle, which is placed on the chuck next to the die, to sense the voltage.

Measuring the resistance was done by generating Id vs Vds curves with varying Vgs, so a known current is forced through the device and the voltage drop is measured. Using Ohms law the resistance can then be calculated.



(a) Cascade needle probe station at ECTM TUDelft.

(b) An example image of probes above a power MOSFET for testing in a different configuration.

Figure 5.9: Cascade needles probe station and microscope image.

This resulted in the following measurements, see figure 5.10. Only measurements where the Vgs was high enough, so a fully on device with a Vgs over 10V, were used here and multiple measurements have been averaged.

First the resistance of Cu coins with and without silver sinter material are measured, they show the lowest resistance, with sinter shows a slightly higher resistance. To verify the resistance of the copper coin is calculated using equation 5.1:

$$R = \rho \frac{l}{A} = 280n\Omega \tag{5.1}$$

Where:

- R is the resistance in Ω
- ρ is the conductivity of copper: $16.8 \cdot 10^{-9}$ Ωm
- l is the length of the copper coin: 0.5 mm
- A is the area of the copper coin: 5 mm x 6 mm

This is lower than the measured value, since the measurement was done via the chuck so it does include the chuck contact resistance as well.

Next are dies sintered to the Cu coins, they show a resistance distribution between 1mΩ and 2mΩ. This is close to the datasheet value of the device.

The last box shows bare dies, they have a much higher measured resistance. This is because of 2 reasons. The backside couldn't be touched with 2 needles for measurement, so a needle was placed next to the device. So the measurement there is the die plus contact resistance to the chuck. And because needles are used there is a spreading resistance in the very thin copper layer on top, this wont be an issue once embedded since it will be connected using multiple vias.

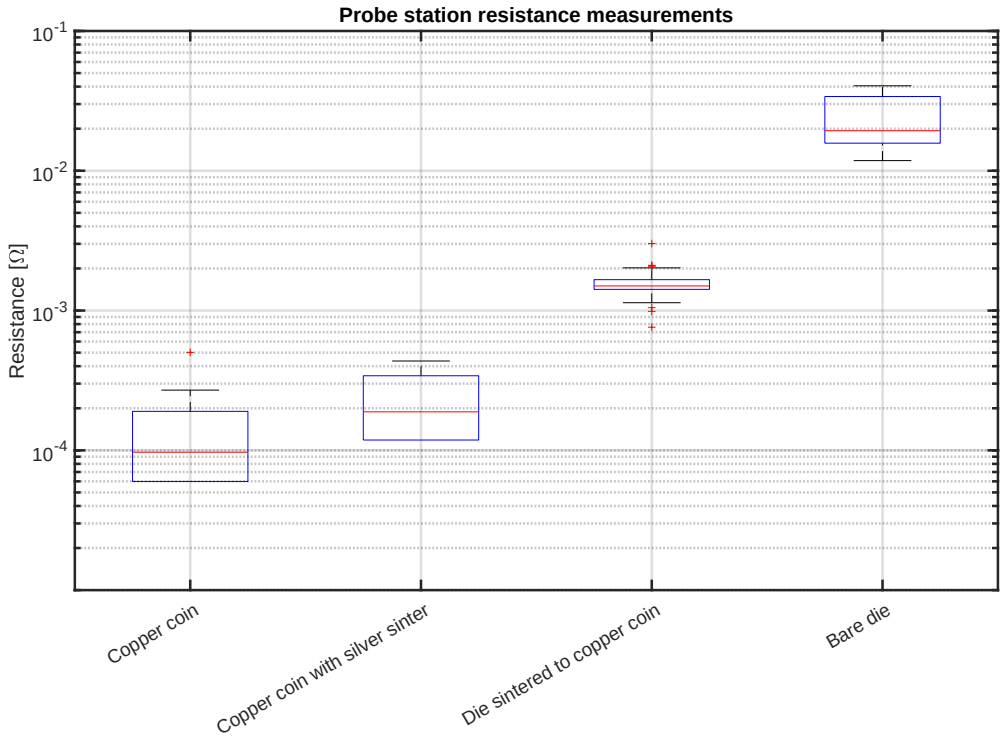


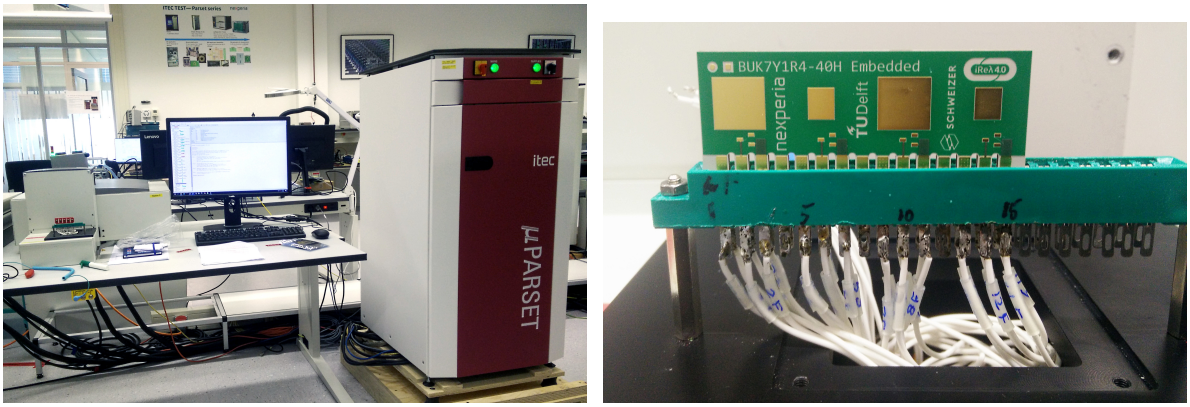
Figure 5.10: Resistance for 4 measurement types, only a copper coin, a copper coins with silver sinter material on it, a copper coin with a die silver sintered to it and separate dies.

5.2. Performance characteristics

The performance of the manufactured PCB was characterized for both electrical and thermal parameters. First electrical measurements including on resistance are discussed, next junction to heatsink thermal impedance, then IR camera profile measurements and finally junction to ambient thermal impedance.

5.2.1. Parset Electrical parameters

The PCBs have been designed to be tested using an automatic test system, the Power Micro Parset. The puParset has multiple channels to measure, it can supply power to a device and it is fully programmable. This is used to individually control the force and sense pins on the PCB which are connected to the embedded device. Since there are 4 devices on 1 PCB there are a total of 12 pins to measure. The puParset that was used has 12 channels so all devices can be measured, even tho it is possible all at the same time a sequential measurement was done so the measurements don't influence each other. A custom socket to connect the pins on the PCB in the right order was soldered.



(a) Power µParset station used for electrical measurements with a red PCB in the custom test socket.

(b) PCB with 4 embedded devices in custom test socket connected to the puParset

Figure 5.11: Parset setup with custom socket.

The following parameters have been measured:

- V_f, Forward voltage of the body diode
- V_{gth}, Threshold voltage
- $I_{DSleakage}$, Drain source leakage at 10V Vds and at 40V Vds applied
- I_{GS}, Gate source leakage in forward and reverse
- ΔV_{gth}, Threshold voltage difference at 1µA and 1mA applied
- $V_{DSbreakdown}$, Breakdown voltage
- R_{DSon}, On resistance

The same measurements have been done on the embedded devices and on 12 LFPAK56 packaged devices as reference. The LFPAK56 uses the same die and is the commercially available version. In figure 5.12, 5.13 and 5.14 the results are shown. In total 98 embedded devices and 12 packaged devices have been measured. 21 of the 119 total embedded devices are not functional at 0 hours so those have not been included in this data. This gives a yield loss of only 20% which can be vastly improved when not in the experimental and manual sample production stage anymore. These packaged devices and the embedded devices are from different batches of wafers and the measurements have been done at different days, so some differences can be expected.

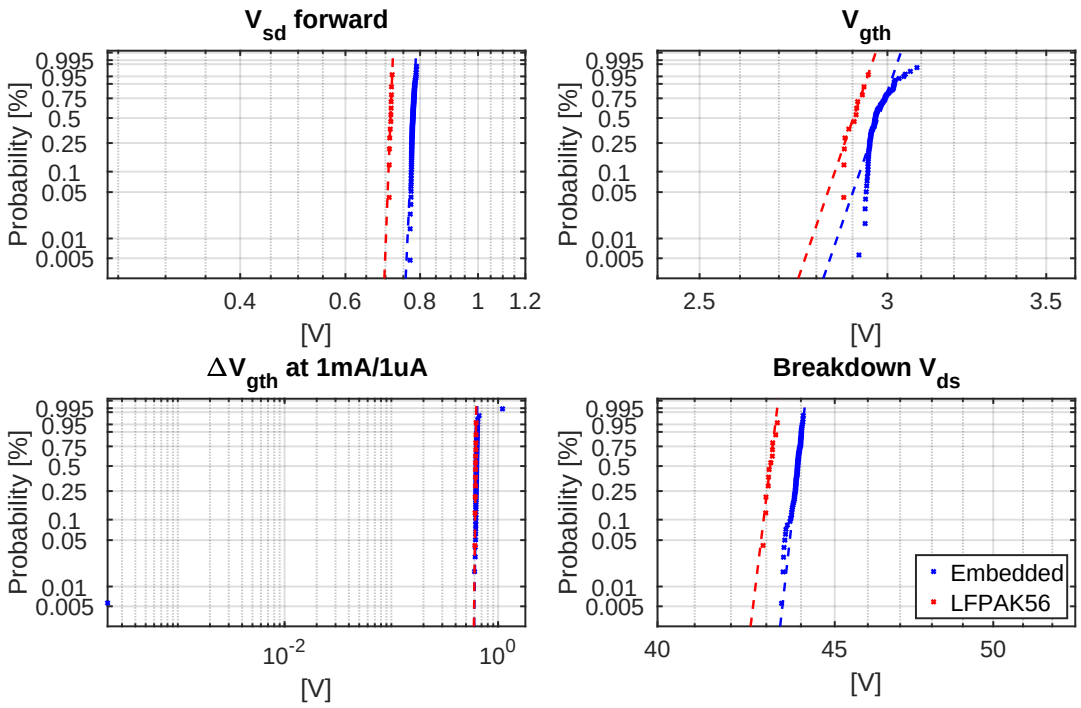


Figure 5.12: Parset voltage measurements showing only a small difference between packaged and embedded devices.

Since the source and the body of the NMOS are shorted in the device a body diode exist between the source and the drain terminal. The forward voltage is measured by applying a pulse of 25A to the drain with the source and gate connected to ground. The forward voltage of the body diode is 0.6V higher for the embedded devices. This is a value related only to the device itself[24], so the difference can be explained by the measurements not taking place at the same time and being from a different batch as mentioned. A temperature difference could have this effect too.

The threshold voltage is measured my applying 1mA to the Source and measuring the gate to source voltage. It also 0.15V higher for the embedded devices which is likely again because of the batch difference.

The difference in gate source voltage at 1mA and 1uA is measured in the same way as the gate source voltage but at 2 different currents. It shows the same difference for for the packaged and embedded devices.

The breakdown voltage is measured by applying a voltage to the drain that rises until it is found using a current limit of 250 µA. Here it is 1V higher for the embedded device and has a similar distribution. This could be because the breakdown voltage is influence by the gate to source and gate to drain capacitance which is different for a packaged and embedded device. But the difference can still be explained by being a different batch as well since its not significant.

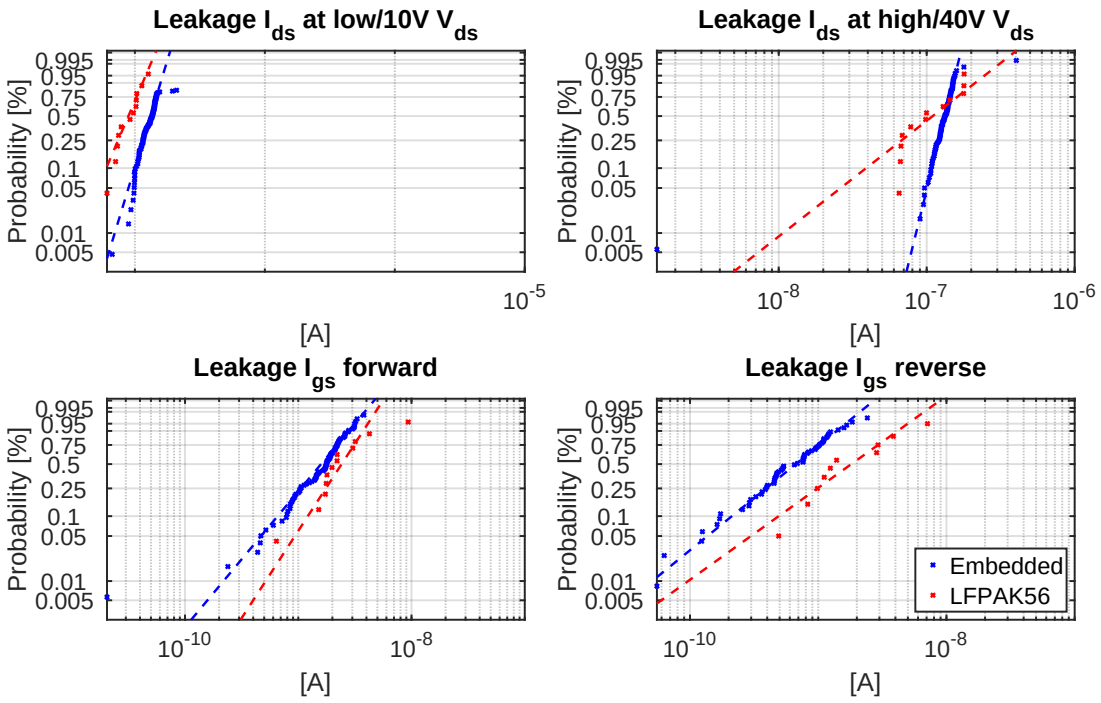


Figure 5.13: Parset leakage current measurements showing only a small difference between packaged and embedded devices.

The drain to source leakage current is measured by measuring the drain current with 10V or 40V applied to the drain and 0V to the source with the gate floating. Similarly the gate to source leakage current is measured by shorting the drain and source, applying 0V to the gate and either a negative voltage of -20V to the source to measure the forward direction or a positive voltage of 20V to measure the reverse direction. For both types of leakage current measurements it was unknown if the new materials would negatively influence them. But from the results can be seen that both the drain to source and drain to gate leakage are similar to the packaged device and within the datasheet specifications.

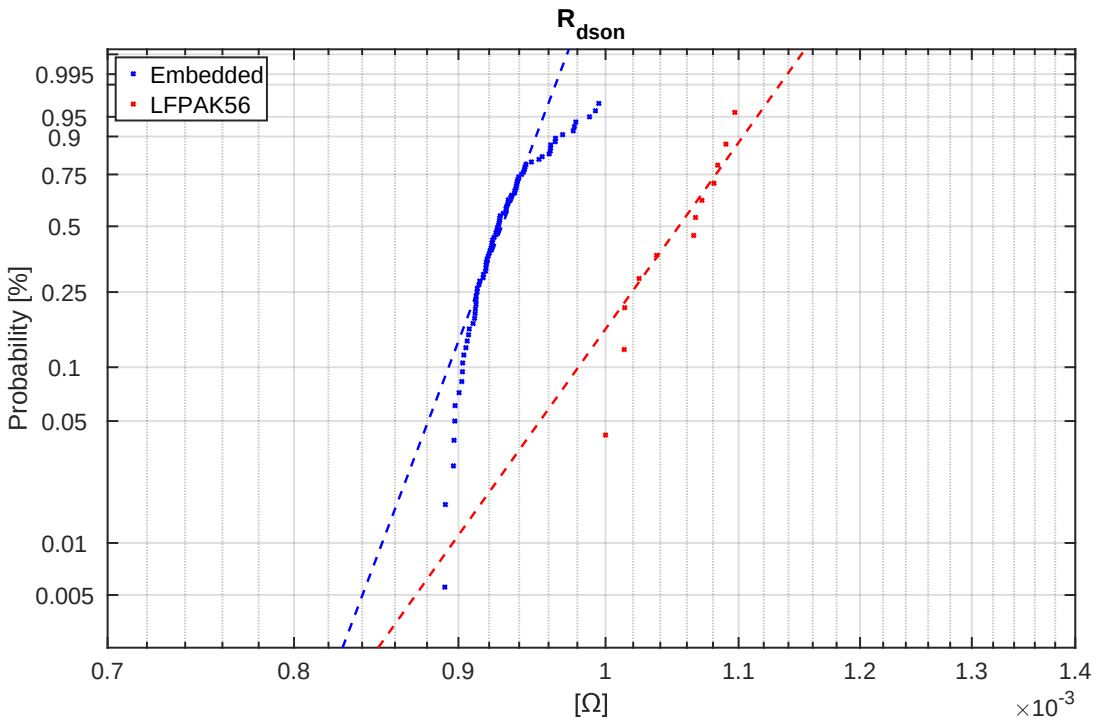


Figure 5.14: Parset Rdson measurements showing a significantly lower resistance for the embedded devices compared to the packaged devices.

To measure the on resistance first 10V is applied to the gate to fully turn on the device, next a current of 25A is applied to the drain while the source is connected to ground. After the device settles after 2ms the voltage drop from drain to source is measured. With the known current of 25A the resistance is automatically calculated. Here the on resistance is lower than the packaged devices, which is the main expected result. Since the electrical path is shorter and has more copper compared to the packaged device. The weibull plot doesn't show a straight line so the distribution isn't a normal distribution. Investigating this resulted in figure 5.15, showing a difference in big and small area. The samples with the highest on resistance, above 0.956mΩ, are all devices with a big area. This could indicate an issue during PCB manufacturing of the bigger areas, for example vias detaching. Looking at the lowest resistances, under 0.916mΩ, only devices with a small area are seen.

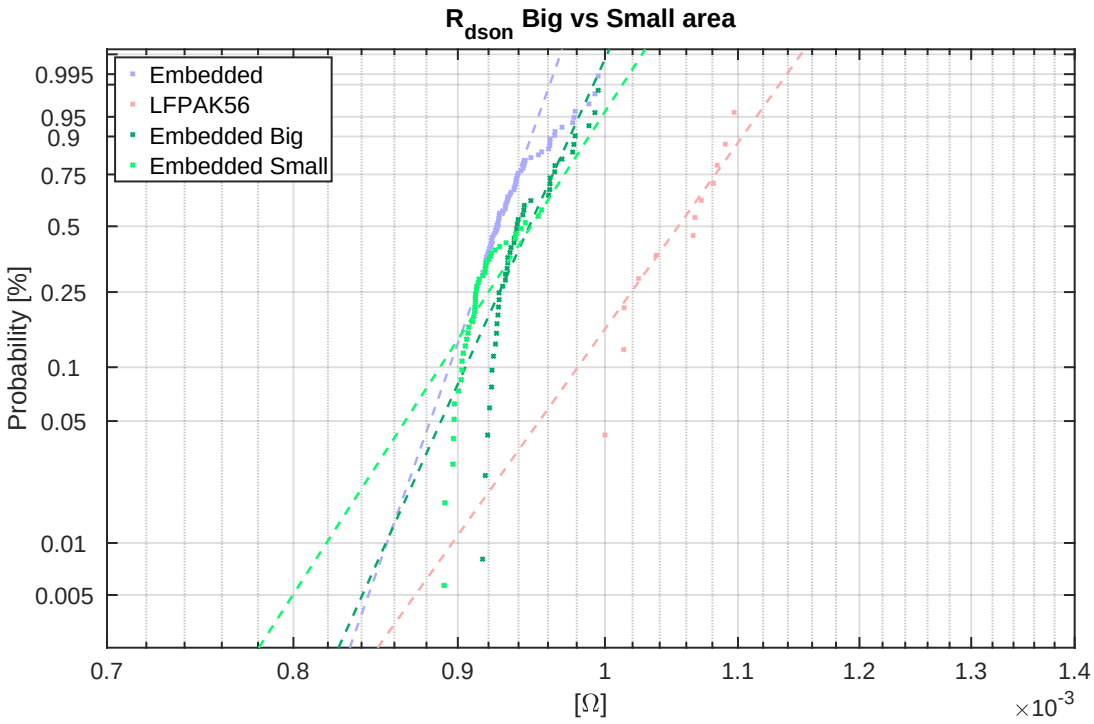


Figure 5.15: Parset Rdson measurements showing the difference in resistance for a big vs small area above/below the device.

5.2.2. Thermal impedance junction to heatsink

To measure the thermal resistance of the devices first a calibration had to be done. Using the Keithly 2450 SourceMeter and the TPS thermal chamber. A current was applied trough the body diode of the device and the voltage drop was measured. This resulted in a table with different voltage drops at known temperatures and currents. Since there is a (close to) linear relation between voltage and temperature the temperature coefficient can be calculated. See table 5.3.

Table 5.3: Calibration of forward voltage for different temperatures.

Current >	10uA	100uA	1mA	10mA	100mA	1A
Temperature v	1E-05	0.0001	0.001	0.01	0.1	1
23°C	0.38102	0.44426	0.5054	0.56529	0.62413	0.675
55°C	0.30063	0.36826	0.43514	0.50131	0.566	0.63
85°C	0.21964	0.29304	0.36475	0.43621	0.5067	0.577
100°C	0.18062	0.25568	0.33041	0.40475	0.478	0.552
125°C	0.114982	0.193535	0.27227	0.35132	0.42979	0.508
Temp. Coeff.:	**-0.002581**	**-0.002430**	**-0.002256**	**-0.0020661**	**-0.0018786**	**-0.001555**

Figure 5.16: Calibration measurement setup, a Keithly 2450 SourceMeter is used to measure the Vf with the device in the TPS thermal chamber at a know stable temperature.

Once the calibration is complete it is possible to measure the Vf and calculate the junction temperature using the following formula:

$$T_{junction} = \frac{V_{junction} - V_{known}}{tc} + T_{known} \tag{5.2}$$

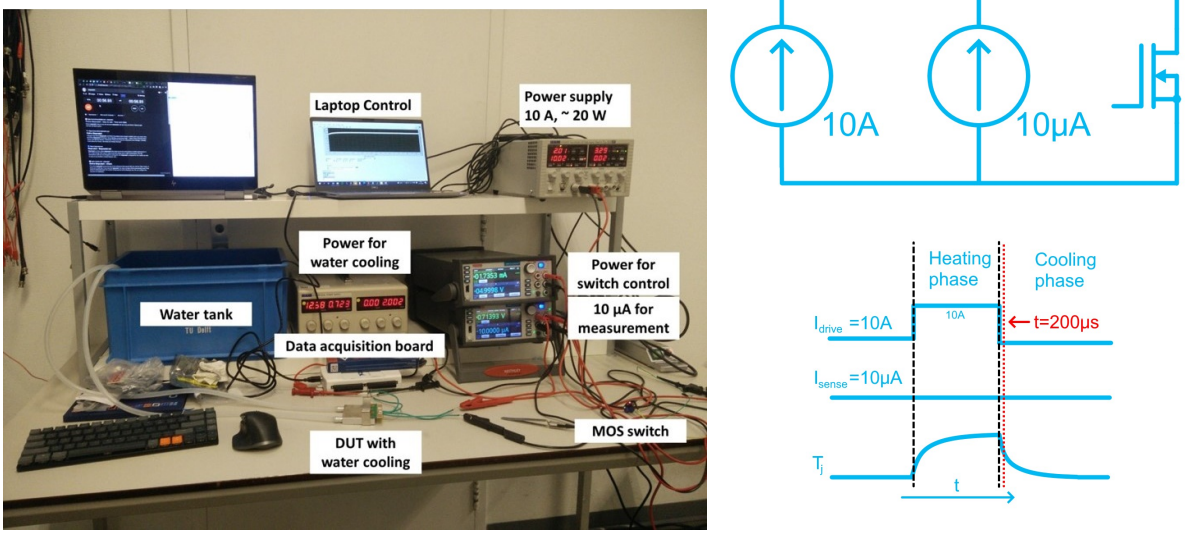
Where:

- $T_{junction}$ is the junction temperature in °C
- T_{known} is a known temperature at a known voltage in °C, taken from table 5.3
- $V_{junction}$ is the measured forward voltage in V
- V_{known} is a known forward voltage at a known temperature in V, taken from table 5.3
- tc is the temperature coefficient at the measured current, taken from table 5.3

There a known voltage and temperature are chose from the table at the measured current. As an example the temperature for a voltage of 0.35V using a measuring current of 10µA is calculated here using the known voltage at 55°C:

$$T_{junction} = \frac{V_{junction} - V_{known}}{tc} + T_{known} = \frac{0.35 - 0.30063}{-2.6 \cdot 10^{-3}} + 55 = 36°C \tag{5.3}$$

To calculate the thermal impedance the temperature difference between the junction and heatsink should be known after applying a known amount of power. This is achieved by the transient thermal measurement setup in figure 5.17. The device under test(DUT) is attached to a water cooled heat sink using thermal paste. The Keithly sourcemeter is used to apply a 10µA current for measuring the junction voltage and a separate powersupply is used to apply a high current to heat up the device. Controlled via a laptop with Labview the measurement starts 200µs after the heat pulse is turned off.



(a) Thermal impedance measurement setup.

(b) Thermal impedance measurement schematic.

Figure 5.17: Thermal impedance measurement setup and schematic.

Measurements have been done for the big and small heatsink, both on the front and the backside of the PCB. This way it is possible to determine which side is the best to use if you want to attach only a single heatsink. The measurements have been done according to the JESD51-14 standard. Which means the thermal impedance was measured during the cooling down phase after applying a heat pulse. The power pulse of 2 minutes for the big heatsink was 10A and the power pulse for the small heatsink 3A, which corresponds to 7W and 2W respectively. With this setup the junction temperature $T_{junction}$, heatsink temperature $T_{heatsink}$ and the power P are known, this can be used to calculate the thermal impedance Z_{th} using equation 5.4.

$$Z_{th} = \frac{T_{junction} - T_{heatsink}}{P} \tag{5.4}$$

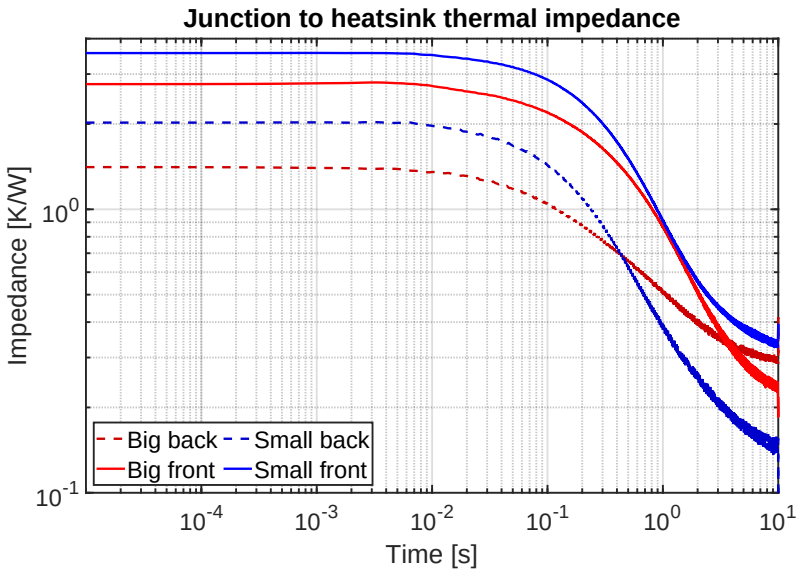
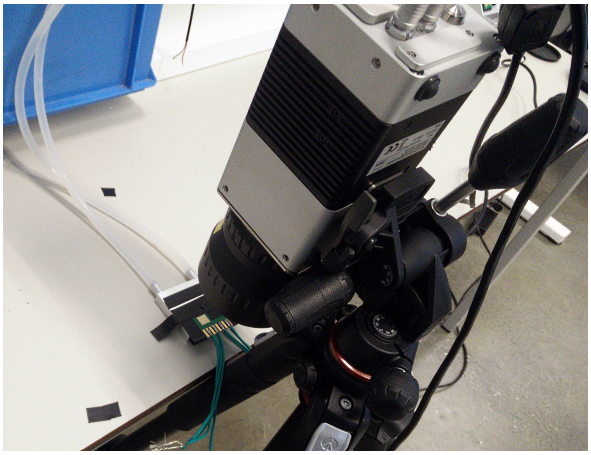


Figure 5.18: Thermal impedance curves, measured during cooldown.

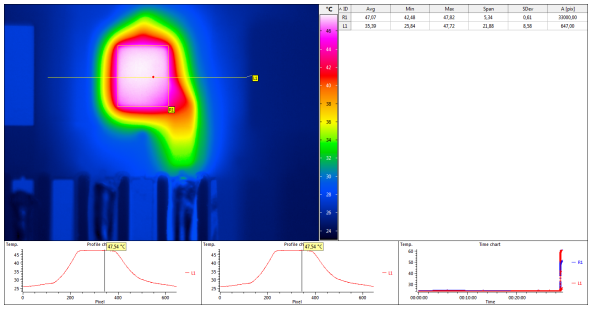
As seen in figure 5.18 focusing on the left side which is right when the power pulse is turned off. From best to worst thermal impedance are the big heatsink on the back, the small heatsink on the back, the big heatsink on the front and the small heatsink on the front.

5.2.3. IR setup thermal profiles

The same water cooled setup as above is used again, but now instead of measuring during cooldown, a thermal camera is used to measure the temperature from the top during heating up. Thermal paste was used as thermal interface material between the PCB and the water cooled block. The IR thermal camera is used to measure the temperature trough a piece of electrical tape. This is done since the gold surface finish will reflect IR light and not give any usefull information, see the setup in figure 5.19.



(a) IR thermal camera and pcb on heatsink, electrical tape is used since the gold surface finish will reflect in the IR spectrum



(b) Interface of the thermal camera showing a small heatsink being heated up at 10A, profile and time graphs are available as well

Figure 5.19: The used setup for doing thermal measurements using an IR camera.

Using this setup it was again investigated what the influence of cooling either the front or backside and either the big or small area heatsink on the PCB is. To do the measurements a current is applied to

heat up the device. For each configuration a measurement was done at 5A, 10A and 15A. A profile temperature graph trough the middle of the heatsink area on the PCB was made, see line L1 in figure 5.21a. Each measurement took 20s. A profile graph was made in the first 10% of heating up(dotted bright line), at halfway to steady state(dashed line) and at steady state(solid dark line) as explained in figure 5.20.

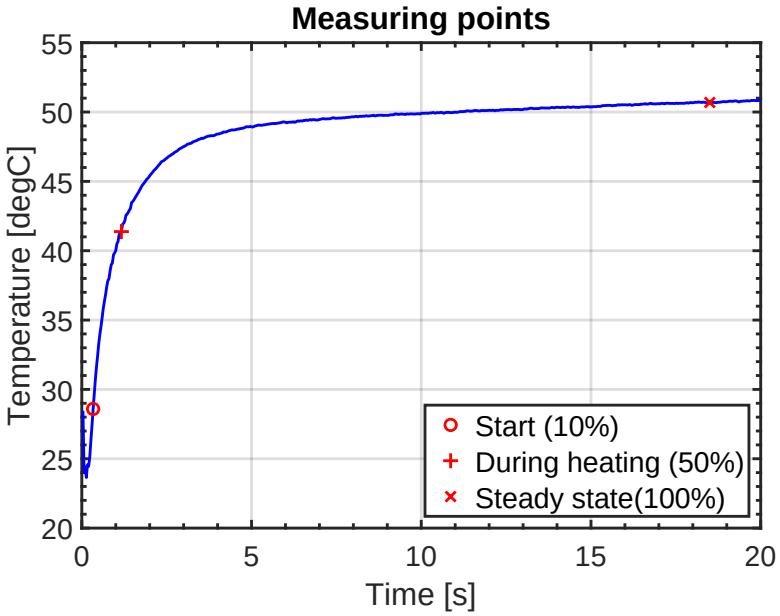
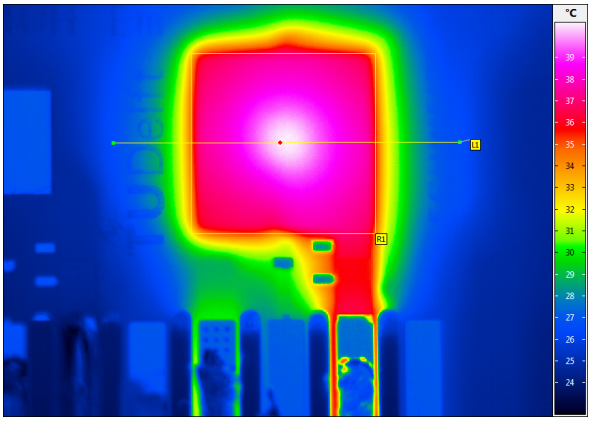
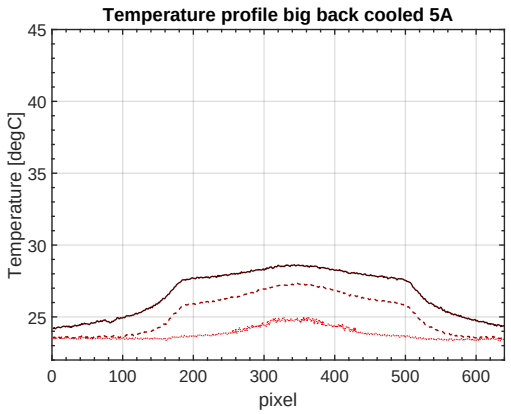


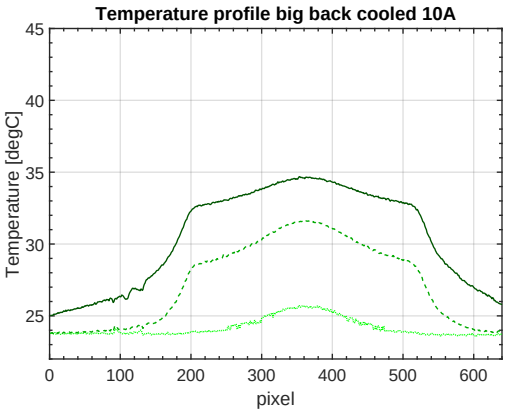
Figure 5.20: Measuring points for temperature profile graphs at the first 10% of heating up, at halfway to steady state and at steady state.



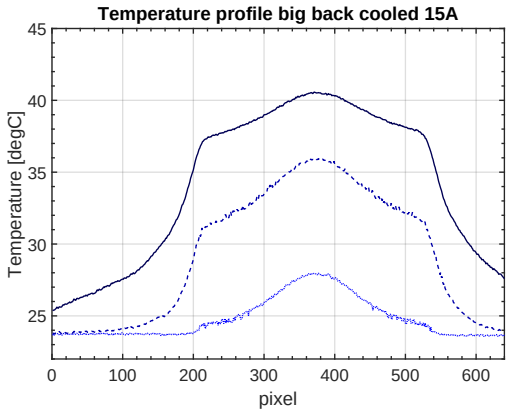
(a) Thermal image of big heatsink cooled from back at 15A stead state, measurements to make the profile graphs are done using line L1



(b) Temperature profiles at 5A



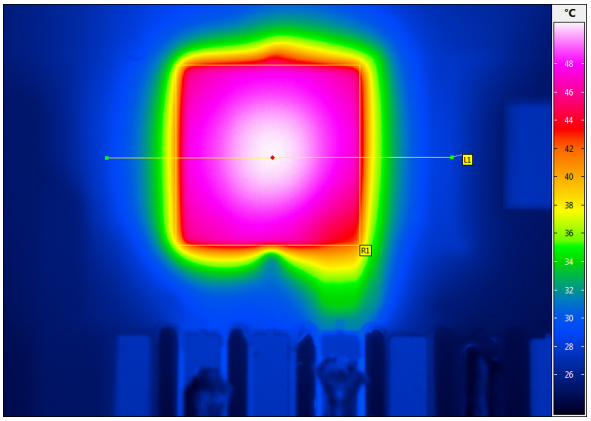
(c) Temperature profiles at 10A



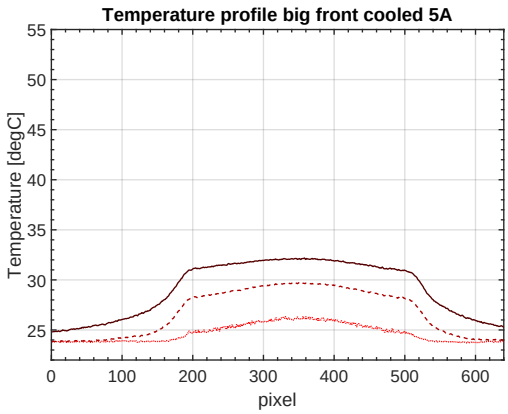
(d) Temperature profiles at 15A

Figure 5.21: Temperature profiles trough the center for the **big** heatsink cooled from the **back** at different currents, the dotted bright line is at the first 10% of heating up, the dashed line at halfway and the solid dark line at stead state.

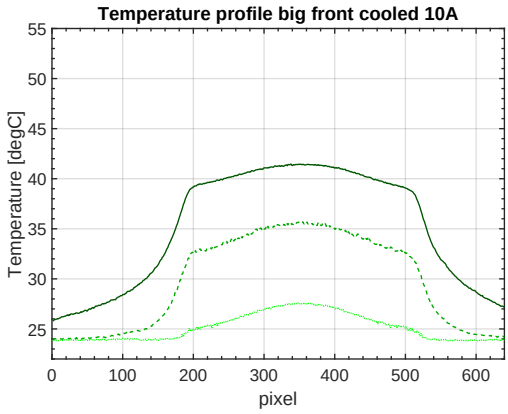
These profiles can be seen in figure 5.21b, 5.21c and 5.21d for the big heatsink cooled from the back. From the figure it is clear that especially at higher currents the center where the device is embedded has a hot spot. The heat spreads very well trough the heatsink area and via the copper trace but quickly drops off to the sides where there is no copper.



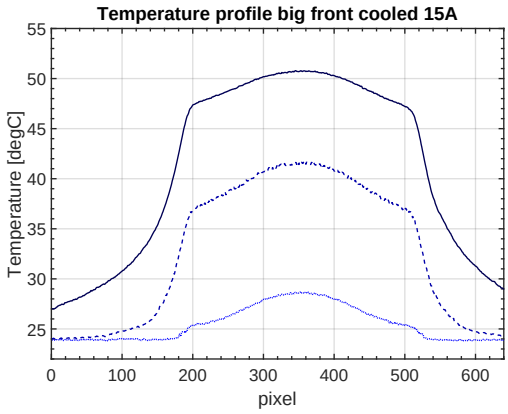
(a) Thermal image of big heatsink cooled from front at 15A stead state, measurements to make the profile graphs are done using line L1



(b) Temperature profiles at 5A



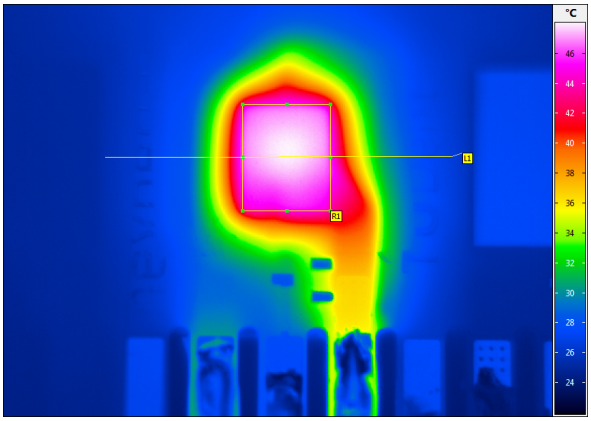
(c) Temperature profiles at 10A



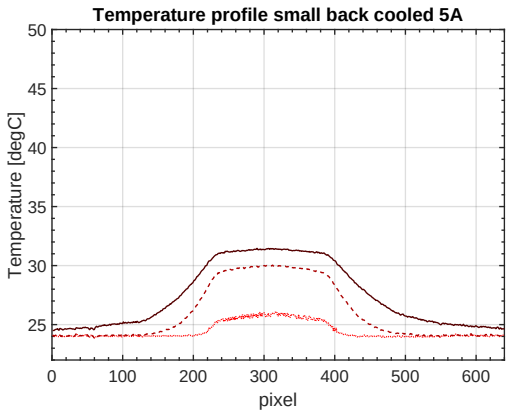
(d) Temperature profiles at 15A

Figure 5.22: Temperature profiles trough the center for the **big** heatsink cooled from the **front** at different currents, the dotted bright line is at the first 10% of heating up, the dashed line at halfway and the solid dark line at stead state.

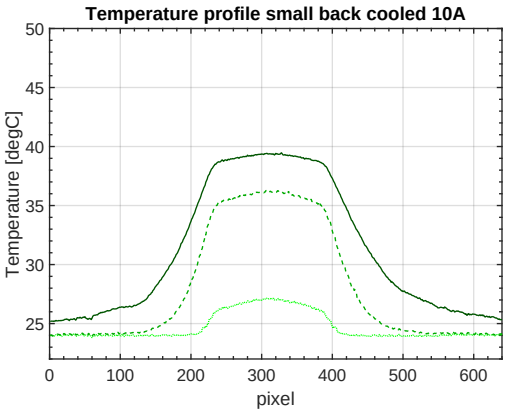
Next the PCB is flipped and the same measurement is repeated with the front side attached to the water cooled block. Besides flipping the PCB and reapplying thermal paste for a better thermal connection, no other parameters are changed. The results can be seen in figure 5.22. For all currents the measured temperature is higher. Taking the peak temperature at 15A for both the front and back side cooled configuration, we get 51°C and 41°C, this is a 24% difference. So clearly it is more efficient to cool via the backside.



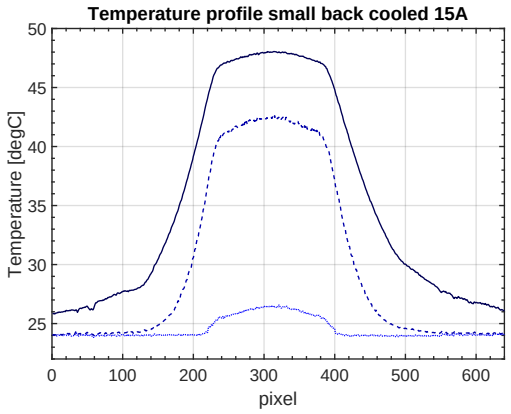
(a) Thermal image of small heatsink cooled from back at 15A stead state, measurements to make the profile graphs are done using line L1



(b) Temperature profiles at 5A



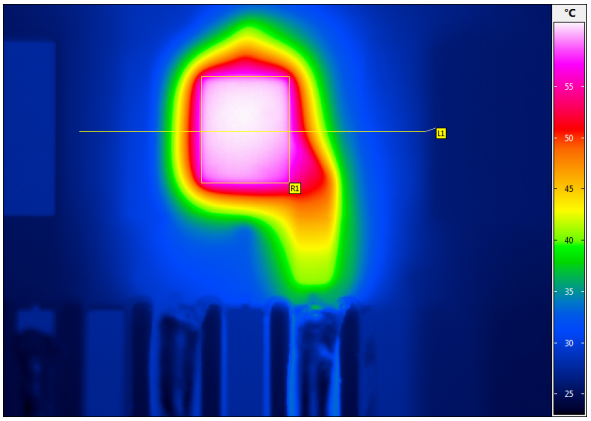
(c) Temperature profiles at 10A



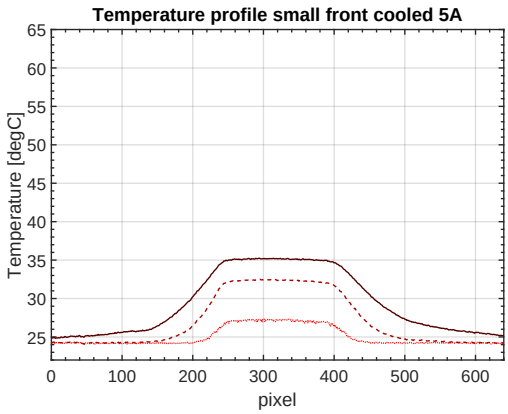
(d) Temperature profiles at 15A

Figure 5.23: Temperature profiles trough the center for the **small** heatsink cooled from the **back** at different currents, the dotted bright line is at the first 10% of heating up, the dashed line at halfway and the solid dark line at stead state.

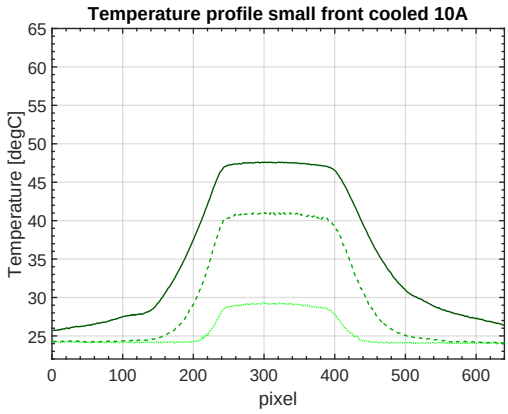
Now the same measurement is done for the small area with backside cooling. See figure 5.23. As expected since there is a smaller area heat is less effectively removed resulting in higher temperatures.



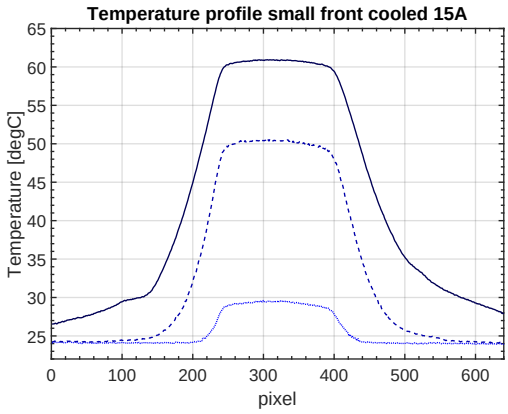
(a) Thermal image of small heatsink cooled from front at 15A stead state, measurements to make the profile graphs are done using line L1



(b) Temperature profiles at 5A



(c) Temperature profiles at 10A



(d) Temperature profiles at 15A

Figure 5.24: Temperature profiles trough the center for the **small** heatsink cooled from the **front** at different currents, the dotted bright line is at the first 10% of heating up, the dashed line at halfway and the solid dark line at stead state.

Finally the same measurement is done with the small area while the front side is cooled. In figure 5.24 below the resulting temperature profiles can be seen again. In the same way as the front and back side cooling of the big heatsink, here again there is a difference. The front side cooling reaches a peak temperature of 61°C and the back side cooling reaches 48°C, this is a 27% difference, comparable to the big area.

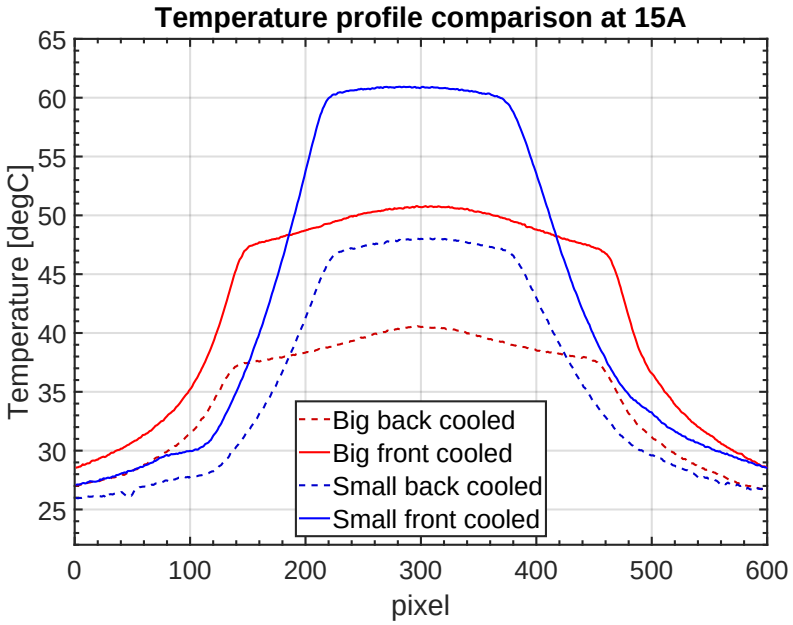
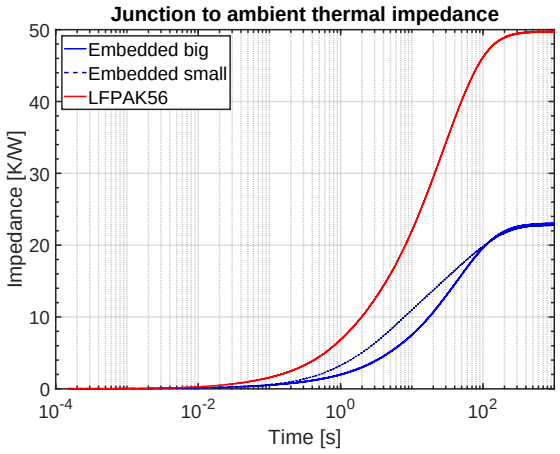


Figure 5.25: Comparison of profiles at 15A for all configurations, note that the distance to the IR camera wasn't exactly the same for each measurement, resulting in slightly wider or smaller profiles measured in pixels.

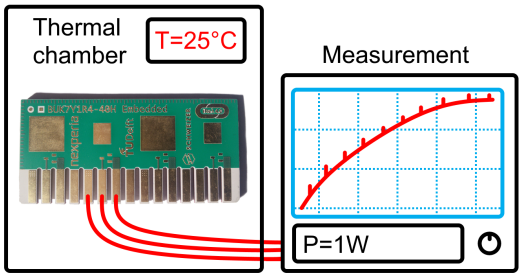
To conclude all generated heat gets conducted to the outside of the PCB via the copper heatsink areas with very little heat conducted to the sides. This means devices could be spaced close together while still effectively being cooled. As expected the bigger area has a lower overall temperature which means heat gets transferred to the attached water cooled plate better. And the back side of the PCB has better heat transfer from die to outside compared to the front. This is summarized in figure 5.25 by showing the profile at 15A for the 4 different configurations.

5.2.4. Thermal impedance junction to ambient

Thermal impedance was measured during heating up in a separate setup. Here a thermal chamber was used to keep the device at a known temperature and pulsed powersupply to heat up and measure the device at the same time. The main goal of this measurement was to compare the packaged devices to the embedded device. This wasn't practical with previous setup since the packaged device doesn't have an area that is easily attached to the water cooled block.



(a) Thermal impedance for big and small embedded device compared to LFPAK56 packaged device.



(b) Schematic setup of the measurement, using a thermal chamber to keep the reference temperature known and a measurement every 150µs during heating up.

Figure 5.26: Thermal to ambient impedance measurement results and setup.

The measurement was done for 1000s with 150µs time steps. Here the measured thermal impedance is the junction to ambient impedance, which isn't the same as the junction to heatsink impedance as measured in previous experiments. The big and small embedded device end up at the same steady state point because they are both heated up at low power (approximately 1W) and end up at the same temperature. See figure 5.26b for a schematic setup. From the data in figure 5.26a it is clear that the embedded device has a significantly better thermal impedance.

5.3. Reliability evaluation

Besides functionality it is important to know if the device is reliable. To do this multiple standards are used in the industry. Mainly the automotive industry has rigid requirements, so those standards should be met or exceeded. Table 5.4 shows a list of tests that are planned to be done after the completion of this thesis.

Table 5.4: Reliability test list.

Test	Test conditions	Samples	Notes
Temperature Cycling (TC)	JEDEC JESD22-A104, T=-65°C to 150°C, 1000 cycles	5	Optional 2000 cylces
Intermittent Operational Life (IOL)	MIL-STD-750-1 Method 1037, T=25°C, ΔTj≥100°C, ton=toff=2 min, t=1000 hrs	5	Optional t=2000h
High Humidity High Temperature Reverse Bias (H3TRB)	JEDEC JESD22-A101, T=85°C, 85% RH, reverse biased at 80% of rated breakdown voltage, t=1000 hrs	5	Optional t=2000h
High Humidity High Temperature Reverse Bias (H3TRB)	JEDEC JESD22-A101, T=85°C, 85% RH, reverse biased at 80% of rated breakdown voltage, t=1000 hrs	2	Dummy PCB without embedded devices, rated voltage for SiC will be used

Temperature Cycling (TC) according to the JEDEC JESD22-A104 standard. The device will go in an oven and cycle from T=-65°C to 150°C for 2000 cycles. This will make the materials that are used expand and contract. Since they have different coefficients of thermal expansion (cte), they will do this at different rates which can result in parts breaking.

Intermittent Operational Life (IOL), according to the MIL-STD-750-1 Method 1037. Instead of an oven the device is turned on and of repeatedly to heat it up. It will be done at T=25°C, heat up ΔTj≥100°C using a time of ton=toff=2 min for t=1000 hrs in total. Depending on the amount of failures the test can be extended to 2000h. Similar to TC here the device heats up and cools down with materials that have different cte, but now the heat source is the device itself which give a different temperature profile.

High Humidity High Temperature Reverse Bias (H3TRB), according to the JEDEC JESD22-A101 standard. With parameters T=85°C, 85% relative humidity, reverse biased at 80% of the rated breakdown voltage, t=1000 hrs. This means the devices will go in a temperature and humidity controlled chamber with a voltage applied that is close to the breakdown voltage. Over time the temperature and absorbed humidity in the materials can cause the breakdown voltage to lower which makes the device fail. Depending on the amount of failures the test can be extended to 2000h. This is an important test for industrial applications like the automotive sector [15].

Since the manufactured devices don't have a SiC device embedded a high voltage test cannot be done, but to test the PCB materials and trace spacing a dummy without embedded die can be used. The same H3TRB test can be done but at 80% of the rated breakdown voltage of a SiC device, which could be 1200V for a 1500V SiC device. Positive test results would then give confidence in embedding a SiC device using the same PCB.

5.4. Conclusion

During the sintering of dies to the copper coins the BLT has been measured at 60µm, the placement accuracy was measured, x-rays have been made and electrical measurements were done on a probe station showing a resistance of close to 1mΩ for the sintered die. This meant that the Cu coins are ready to be used for embedding. After the embedding the PCB was tested. The electrical measurements showed an increased performance by having a 18% lower on resistance at 0.93mΩ compared to packaged devices at 1.1mΩ. With the lowest resistance for the small area. From the thermal measurements it is clear that embedding will help dissipate heat and a big area on the back side of the PCB is the optimal cooling location with a junction to heatsink thermal resistance of 1.409K/W. A significant consideration to be made is in the choice between between a small area for a lower resistance or a big area for better thermal performance. The next steps are reliability measurements to make sure embedding also can keep working for longer times.

6

Conclusion & summary

6.1. Project summary

Embedding of power MOSFETs is an interesting new technology. To study it a BUK7Y1R4-40H MOSFET is embedded in an evaluation board which is designed for this thesis. The designed evaluation board with embedded MOSFETs is shown in figure 6.1. The process from designing to testing is summarized below chapter by chapter.

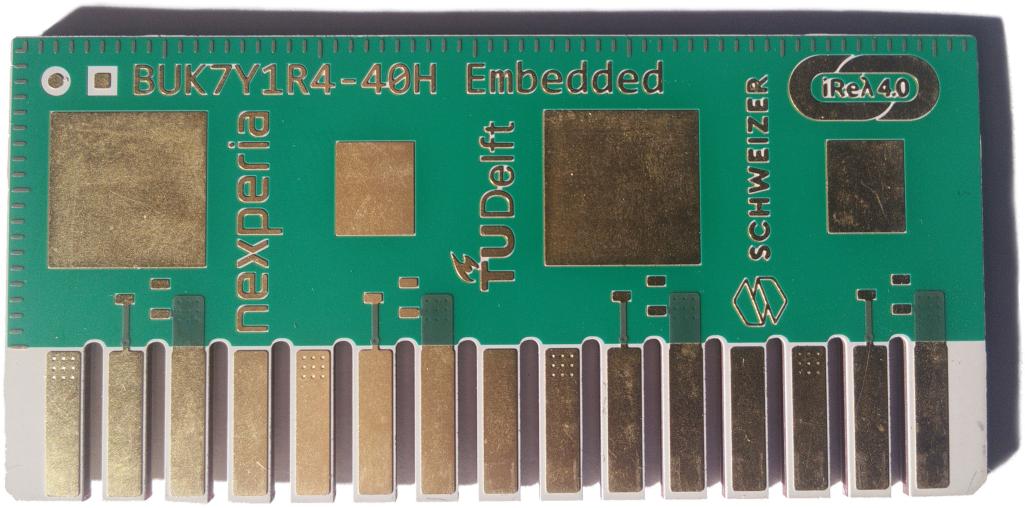
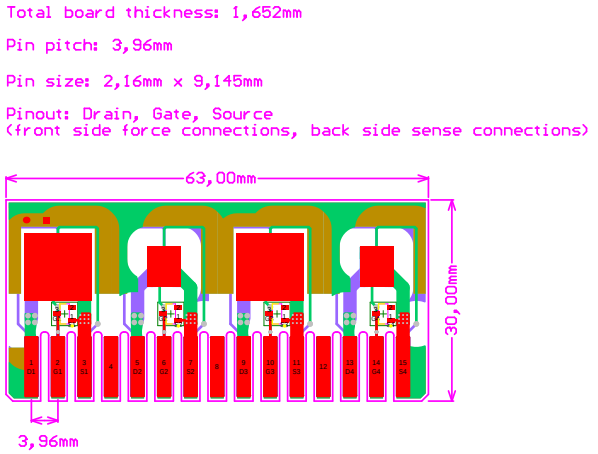


Figure 6.1: The embedded evaluation board which is the result of the design and manufacturing steps in this thesis.

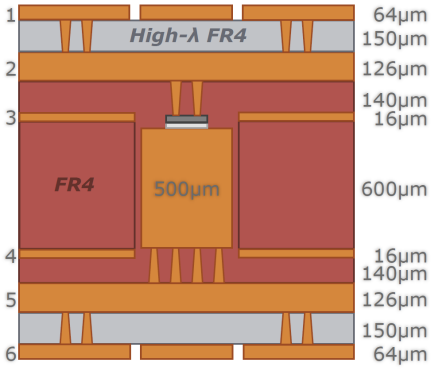
Chapter 2, Literature To start chapter 2 will gave an overview of power electronics packaging, PCB embedding and silver sintering. In packaging usually wirebonds and leaded solder are used, these need to be improved, especially for SiC devices. So a new way of packaging, namely embedding in PCBs, has potential to do this. Before embedding a bare die is attached to a copper leadframe. The attaching can be done using silver sintering to replace leaded solder since this has improved performance and is more environmentally friendly.

Chapter 3, Design & simulation The next chapter described the design process and choices made. Going from the schematics of the PCB to the complete layout. This includes finite element analysis to verify the design and to predict the performance including the junction to heatsink thermal impedance. Starting with the schematics, 4 devices and the connector are drawn. Taking into account a kelving connection has to be made so there are 2 pins used for the source, drain and gate each. The design of the PCB is next. Figure 6.2 shows all the traces on 6 layers from the top and the stackup of these layers next to it. Some design choices that had to be made are:

- The size and shape of the PCB, this was done by using the reference evaluation board so the same test equipment can be used.
- Trace and via sizes, these where chosen to be able to handle the used currents and to move heat away from the die. A 10x10mm and an 5x6mm area are used above the embedded dies as heatsink to investigate how it effects the thermal behaviour.
- Clearance and creepage distances, to make sure no arcing occurs at high voltage a minimum distance of 3mm is used between traces of different potential.
- The stackup and material choice, the PCB consists of 6 layers, this was needed to get an electrically isolated area above and below the embedded die. The materials used have a high Tg to survive high temperatures.



(a) PCB size and copper layers shown from the top.



(b) Stackup showing the 6 copper layers and FR4 materials with thickness.

Figure 6.2: PCB design and stackup.

To embed the MOSFET it is attached to a copper coin. A frame with multiple Cu coins is designed. Each Cu coin is 5mm x 6mm x 0.5mm, this is the same size as the LFPAK56 to keep the comparison relatively fair.

During the designing of the PCB use was made of finite element analysis. Electrical and thermal simulations have been done. The electrical simulation showed a voltage distribution that was usable for kelvin measurents and the thermal simulations showed that backside cooling with a bigger area works best.

Chapter 4, Manufacturing Here the steps to manufacture the used die, the copper coin and the PCB are discussed. A focus on the die attachment by pressureless silver sintering is made since this is a critical step to get right.

To summarize the manufacturing steps, we start with a wafer of bare dies and they end up embedded inside a PCB. So first the wafer gets a top layer of copper. Then a Cu coin frame is prepared to attach the die to. The die is attached to it using sintering by stencil printing with a kapton tape mask, placing the dies with an accurate pick and place machine and putting them in a sinter oven. These Cu coins with dies are then embedded in the middle layer of the PCB and the rest of the PCB is build around it.

Below is a list with an overview of manufacturing steps that have been done:

- A wafer with MOSFET dies with Cu top metalization
- Manufacturing of Cu coins
- Sintering of the dies to the Cu coins
  - Applying sinter paste using kapton tape mask
  - Placing the dies using a pick and place tool
  - Sintering in an oven using the correct temperature profile
- PCB manufacturing and embedding
  - Placing/embedding the Cu coin with die in a hole in the middle PCB layer
  - Laminating the top and bottom layers
  - Finalizing by adding vias, traces, soldermask, etc

Chapter 5, Measurements & characterization The next step after manufacturing is to measure the embedded devices. Both the electrical and thermal characteristics have been investigated. Some measurements have also been done during the manufacturing. To quantise the embedded MOSFETs performance compared to the packaged version multiple electrical measurements have been done. During the manufacturing x-ray, height and placement accuracy measurements have been done before and after sintering. Functionality test have been done. And finally reliability tests are planned to be done.

A list of measurements is given here:

- Bond line thickness(BLT), the thickness of the sinter material was measured to verify the amount of paste used was correct.
- Placement accuracy was measured to make sure the gate goes to the right location so when embedded the via will touch it.
- X-rays have been made to investigate voiding under the die.
- Cu coin resistance was measured after sintering to confirm the die still works after the sinter process.
- Electrical performance showed similar leakage and better on resistance measurements compared to the packaged devices. Imporant to highlight is figure 6.3, it shows the on resistance weibull plots for the embedded devices in blue and the packaged devices in red. Showing a lower on resistance for the embedded devices. Here it is also visible that there is less variation between embedded devices since the slope is higher.

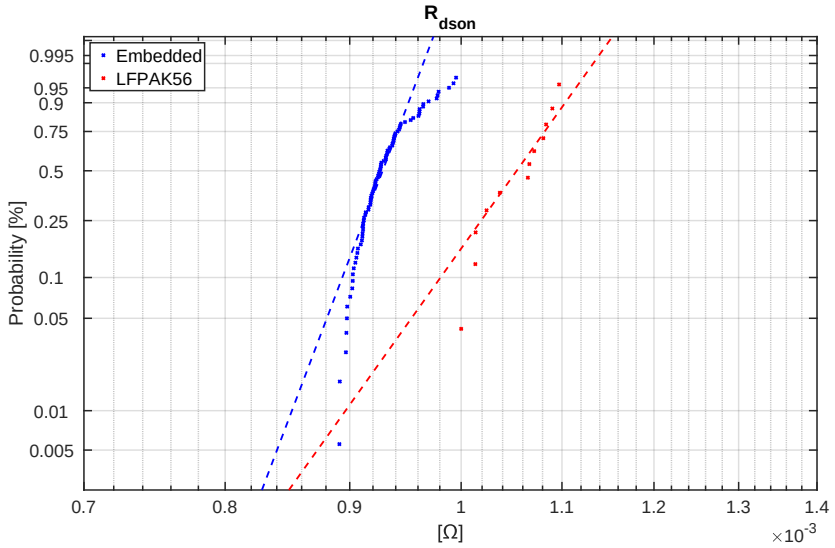
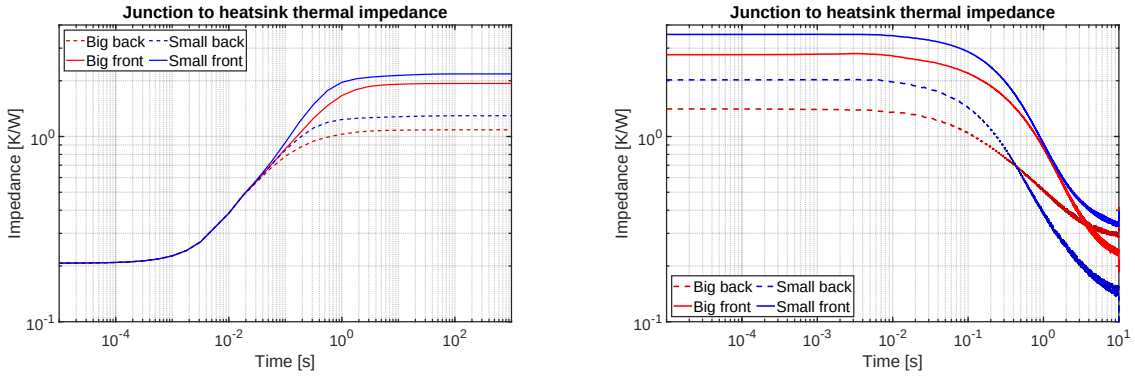


Figure 6.3: Parset Rdson measurements showing a significantly lower resistance for the embedded devices compared to the packaged devices.

- Thermal junction to heatsink measurements were done by first calibrating in an oven. The measurement was done by applying a heat pulse while the PCB is connected to a water cooled block. During the cool down period after the pulse the measurement is done. Simulations have been done with similar boundary conditions but for heating up. The results are in figure 6.4.



(a) Thermal impedance curves, simulated during heat up.

(b) Thermal impedance curves, measured during cool down.

Figure 6.4: Simulation and measurement of junction to heatsink thermal impedance with the Y-axis at the same scale.

Using the same scale for the Y-axis it becomes clear that the simulation and measurement are similar in multiple aspects. At the end of heating up during simulation and the start of cooling down the order of the lines is the same, this shows that the big area on the back is the best location to actively cool and the small area on the front the worst. At the start of heating up the thermal impedance is 0.2 K/W, during cool down all measurements also approach this value.

- Thermal IR camera profile, the same setup was used with a thermal camera to see the temperature distribution on the PCB as showing in figure 6.5.

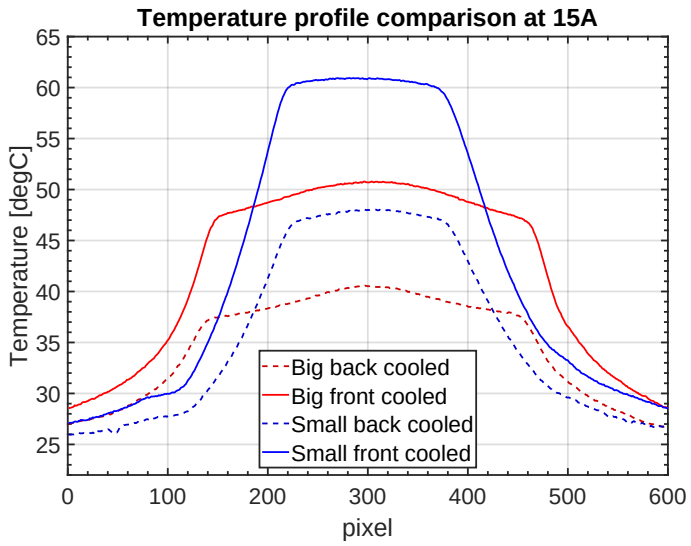


Figure 6.5: Comparison of profiles at 15A for all configurations, note that the distance to the IR camera wasn't exactly the same for each measurement, resulting in slightly wider or smaller profiles measured in pixels.

- Thermal junction to ambient measurements are done in a thermal chamber at a known temperature, the difference between internal and thermal chamber temperature was used for the measurement. The result can be seen in figure 6.6

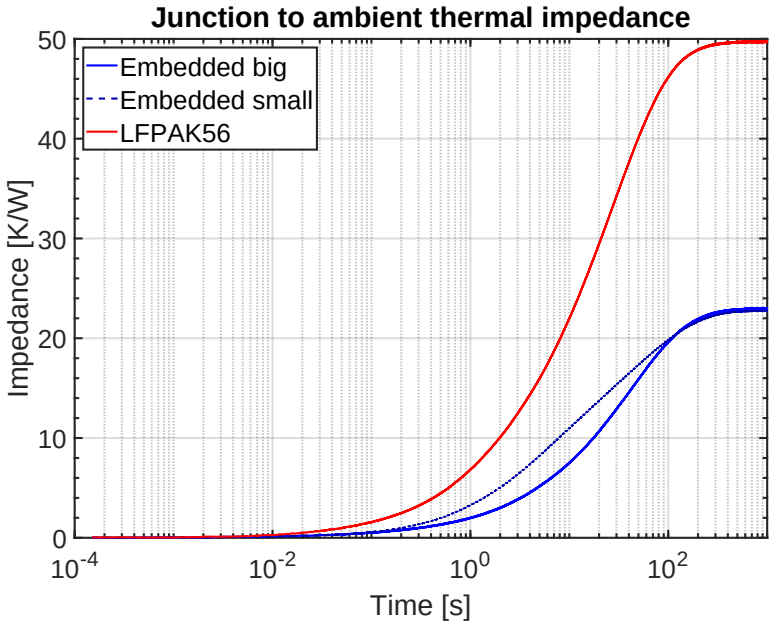


Figure 6.6: Thermal impedance for big and small embedded device compared to LFPAK56 packaged device.

- Reliability tests are planned to be done to investigate the lifetime of the embedded devices.

6.2. Conclusions

- The main objective to successfully design an evaluation board with embedded devices that can be compared to the packaged LFPAK56 is reached. A total of 98 embedded devices have been produced. Using 4 connections a kelvin connection can be made to the embedded device for

accurate electrical measurements and by having high thermal conductive layers and a big copper area above and below the device a good thermal connection can be made to a heatsink.

- The electrical performance of the embedded devices show a performance that is similar or better than the packaged devices. Most notably they have a lower R_{DSon}. With an average R_{DSon} of 0.93mΩ, compared to a R_{DSon} of 1.1mΩ, for the embedded and packaged devices respectively. This is an 18% lower resistance. The devices with a small area had an average lower R_{DSon}.
- Junction to heatsink thermal simulations and measurements have been done as seen in figure 6.4. Both showing that cooling from the backside on the big heatsink area gives the thermal resistance to an external cooling block at 1.409K/W. Next would be the backside of the small heatsink at 2.022K/W, the frontside of the big heatsink at 2.764 and last the frontside of the small heatsink at 3.558K/W. The option to cool from both sides at the same time is there as well and would improve the cooling performance even more.
- Thermal profiles in figure 6.5 shows heat escape well via the copper areas above or below the die with a sharp drop of around them. So dies can be spaced close together than packaged devices while still effectively removing heat in an actual application.
- Comparing junction to heatsink thermal impedance wasn't easy since a heatsink couldn't be directly connected to the LFPAK56. Showing that embedding already gives an advantage by making it more practical to attach a heatsink. But to still be able to compare junction to ambient thermal impedance was measured as well. Showing a more than twice as good impedance for the embedded devices, see figure 6.6.
- Sintering is a viable alternative to soldering but getting reliable BLT needs improvement, some comments on this are made in the recommendations.
- The placement of the dies was accurate enough so the gate via and other vias successfully connected to the die to make electrical contact.

6.3. Recommendations

- Now that a Si device has been embedded and proved to have good performance, the obvious next step is to embed a SiC device. Especially since material choice and creepage/clearance distances have been decided based on SiC devices from the start.
- An issue during manufacturing was the flatness of the Cu coins and frame. This could be improved by using more connections to attach the Cu coin to the frame. Resulting in a repeatable BLT.
- Another improvement would be to do silver sintering directly on copper instead of a silver spot. Since the silver spot gave the mousebite issue. It would also make it possible to use a regular metal stencil, potentially improving throughput and repeatability in getting the same BLT.
- The difference in on resistance between the big and small area can be investigate by doing a cross section and analyzing the differences like via attachment or warping.
- Reliability tests are still planned to be done, since the positive electrical performance it is also important to know if the performance lasts over time.
- A high voltage test using a dummy PCB with nothing embedded could be put trough H3TRB tests as well to see if the materials fail at high voltage and humidity.
- An improvement to the PCB could be to add cutouts between the devices, that way 4 devices can be measured at the same time without thermally influencing each other at all.
- Finally a demonstrator using embedding technology to make a functioning inverter using SiC would give a good view on practical design choices that have to be made using embedding.

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