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DOI

[10.23919/VLSITechnologyandCir65189.2025.11074934](https://doi.org/10.23919/VLSITechnologyandCir65189.2025.11074934)

Publication date

2025

Document Version

Final published version

Published in

Proceedings of the 2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)

Citation (APA)

Guo, A., Peng, W., Yang, Y., Hu, X., Muratore, D., & Du, S. (2025). A Fully Integrated Sc Converter Hybridizing Dickson and Continuously-Scalable-Conversion-Ratio Topologies with a Wide Bipolar Vcr Range for Energy Harvesting. In *Proceedings of the 2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (pp. 1-3). IEEE.
<https://doi.org/10.23919/VLSITechnologyandCir65189.2025.11074934>

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A Fully Integrated SC Converter Hybridizing Dickson and Continuously-Scalable-Conversion-Ratio Topologies with a Wide Bipolar VCR range for Energy Harvesting

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Abstract

This paper proposes a fully integrated hybrid Dickson and continuously-scalable-conversion-ratio (CSCR) converter for bipolar-input thermoelectric energy harvesting (TEH). This is the first reported fully integrated converter achieving dual-polarity operation with an extended voltage conversion ratio (VCR) range, thanks to the 4-rail CSCR topology and the reconfigurable hybrid Dickson-CSCR architecture. The TEH interface system is fabricated in a 180-nm BCD process, achieving above 75% efficiency for VCR ranging from -6.48 to -2.55 and from 2.55 to 6.67 with a 1.2 V regulated output.

Introduction

Thermoelectric energy harvesting (TEH) has been a promising solution to power edge devices for the Internet of Things (IoT). A thermoelectric generator (TEG) generates DC voltage (V_{TEG}) that can vary in a wide range in both polarities (from -1V to +1V) depending on the ambient temperature and the Seebeck coefficient α (Fig. 1) [1]. Therefore, a boost converter that can operate efficiently in a wide range of both positive and negative voltage conversion ratios (VCR) is needed [2-3]. For miniaturization, fully-CMOS-integrated switched-capacitor (SC) converters, such as reconfigurable-SC (R-SC) and continuously scalable conversion-ratio (CSCR) converters [4-6], were proposed for wide-range EH. An R-SC converter reconfigures the topology into discrete VCRs while suffering from efficiency degradation between adjacent VCRs [7]. By contrast, a CSCR converter achieves a smoother PCE to VCR with a multiphase soft-charging technique but suffers from high charge-sharing loss (P_{CSL}) when operating under a large VCR [8-10]. A reconfigurable CSCR (RCSC) converter was proposed to improve the VCR by adjusting the number of intermediate phases [11], but it still suffers from large voltage swings on the top plate (TP) of the core capacitors (C_C) and necessitates complex control logic and detection circuitry. In addition, reported SC converters can only work for positive input polarity, limiting their TEH applications.

Proposed System

This paper proposes a hybrid Dickson-CSCR power converter with a Dickson R-SC converter and a 4-rail CSCR core to harvest energy from a wide range dual-polarity input (Fig. 2). The inherent switch pairs in each SC cell connected to the TEG (nodes V_P and V_N) can be directly utilized to convert energy from both polarities. To extend VCR, an additional adjustable voltage rail (V_X), an intermediate voltage between V_{IN} and V_{OUT} generated by a Dickson R-SC converter is introduced to decrease the voltage swing on TPs of C_C from $V_{OUT}-V_{IN}$ to $V_{OUT}-V_X$, while the voltage swing on the bottom plates (BP) remains at $V_{IN}-V_{SS}$. In this case, the P_{CSL} can be maintained low with fewer auxiliary soft-charging phases, significantly reducing design complexity and the time required for a full cycle of the soft-charging process (Fig. 3 top). Hybridizing the Dickson R-SC converter, with $VCR_{R-SC} = 3$ or 5, and a 4-rail CSCR converter, with $M=N=4$, the proposed architecture achieves a wide VCR range with simple CSCR implementations. The adjustable VCR_{R-SC} contributes to smaller P_{CSL} by maintaining the small soft-charging steps and proper voltage rails relationship ($V_{IN} < V_X < V_{OUT}$) in the CSCR part (Fig. 3 bottom). This principle could be extended to wider VCRs with more VCR_{R-SC} options.

Implementations

Fig. 4 presents the power stage schematic of the proposed interface. The R-SC region contains four Dickson cells (C_{1-4}). The 4-rail CSCR converter has 4 internal nodes (T_{1-4}) connected to the TPs of C_C and 4 nodes (B_{1-4}) connected to the

BPs. Implemented with the outphasing technique, 17 CSCR cells are implemented to achieve 8 intermediate virtual soft-charging voltage rails at TP and BP, respectively. The 4 cornerstone nodes are connected to external voltage rails: V_P , V_N , V_X , and V_{OUT} . Polarity control is achieved by controlling the clock phases of the polarity switch pairs inherent in the Dickson cells and the CSCR cells. In this case, no additional switches are needed at the input power path for dual-polarity inputs.

The system architecture is given in Fig. 5. The output voltage, V_{OUT} , is regulated at 1.2V via a pulse-skipping technique. To achieve a fast response to the temperature change, this TEH system samples V_{TEG} at around 1kHz to track its polarity and choose a suitable VCR_{R-SC} , by generating a V_{TEG} polarity signal (SEL_{PO}) and a VCR_{R-SC} selection signal (SEL_M). The R-SC works around the corner frequency to achieve a high conversion efficiency, while the operational frequency of the 4-rail CSCR is adapted to track the maximum power point (MPP) of TEG at $V_{IN}=V_{TEG}/2$. The phase to drive the polarity switches is selected by a pair of transmission gates with a dead time implemented when the polarity transitions. The level shifters for mode switches ensure that the level-shifted driving clock is reset to V_{SS} when disabled.

Measurements

The proposed converter, fabricated in a 180-nm BCD process, has an active chip area of 3.57mm², with 4nF MIM capacitors for the R-SC, and 8nF MOS capacitors for the 4-rail CSCR. Fig. 6 illustrates the reconfiguration of the Dickson R-SC converter adaptive to a varying V_{IN} . When V_{IN} is lower than 250mV, the R-SC is configured to 1:5 ($VCR_{R-SC}=5$) to reduce the voltage swing on the TPs and reduce the charge-sharing loss caused by insufficient soft-charging. When V_{IN} increases, the R-SC switches to 1:3 to balance the voltage swing on the TPs and BPs of the C_C in the CSCR block. The zoomed-in waveforms of V_{IN} , V_X , V_{OUT} , and the voltage swing on TP (V_{TP}) at different VCR_{R-SC} are presented at the bottom, showing the voltage swing on TPs of the 4-rail CSCR converter.

The polarity transition of the input (V_P-V_N) is detected rapidly (Fig. 7), as shown by the signal SEL_{PO} , and the lower voltage between V_P and V_N is selected as the global V_{SS} . The regulation of V_{OUT} at 1.2V when $V_{TEG}=700mV$. The voltage ripple at V_{OUT} is 8.37mV and 16.8mV when the load is 120μW and 720μW, respectively.

Fig. 8 and Fig. 9 show that the proposed system achieves smooth and approximately symmetric PCE and P_{OUT} curves at both positive and negative V_{IN} under the MPP condition. Thanks to the proposed dual-polarity 4-rail CSCR converter, a wide effective VCR range with PCE higher than 75% is achieved from -6.48 to -2.55 and from 2.55 to 6.67. A peak PCE of 84% is achieved at $V_{IN}=350mV$ ($VCR=3.45$) when R-SC is configured to 1:3, and the PCE valley caused by the two configurations of the R-SC is reduced to less than 4.19%. The minimum V_{IN} is $\pm 130mV$ ($VCR=9.23$) and V_{OUT} is regulated at 1.2V. With the TEG internal resistance $R_{TEG}=130\Omega$, the peak output power of 1.31mW is achieved. This work is compared to prior SC interfaces for EH in Table 1. The proposed interface expands the range of $PCE>75\%$ to the widest VCR range with the least soft-charging phases compared to the conventional 3-rail CSCR works. With a smaller R_{TEG} (34Ω), a peak output power of 10.8mW is achieved, which is sufficient for most EH applications. Moreover, the proposed TEH interface is the only SC-based interface to achieve dual-polarity inputs. The chip micrograph is presented in Fig. 10.

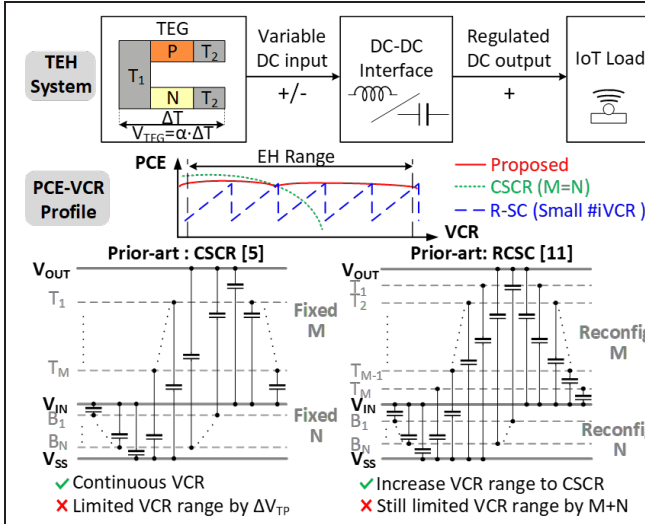


Fig. 1. Thermoelectric energy harvesting (TEH) system, the PCE-VCR profile for EH applications of the proposed topology and the prior-art works, and the limitation of prior-art switched-capacitor power converters.

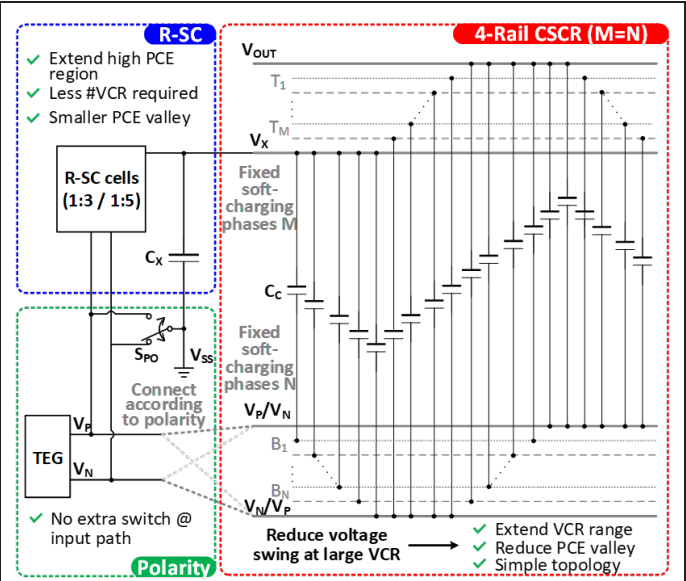


Fig. 2. The proposed reconfigurable hybrid Dickson-CSCR power converter for TEH system with dual-polarity operation.

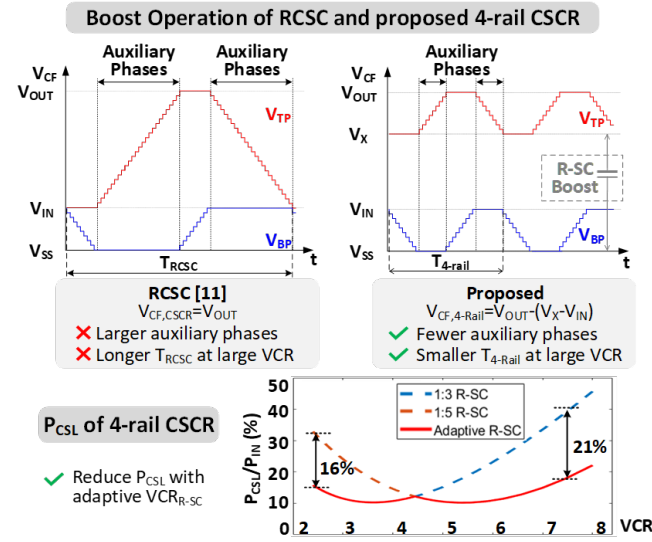


Fig. 3. Schematic of the proposed 4-rail CSCR converter with dual-polarity input, connection of the flying capacitors and switch control for dual-polarity operation in the R-SC.

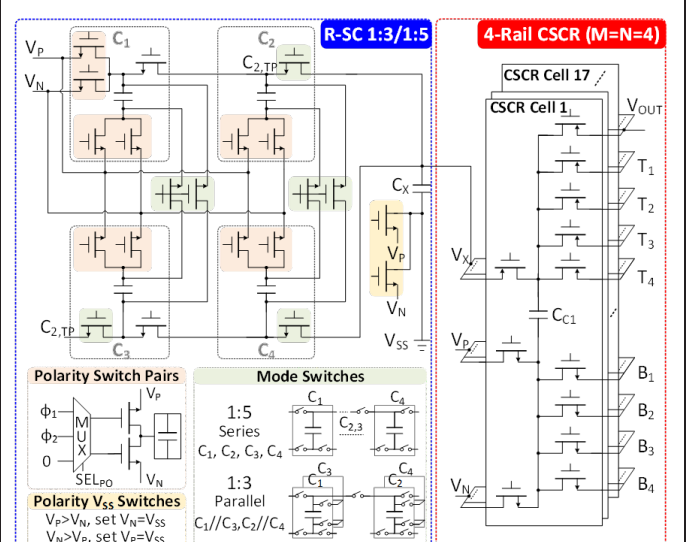


Fig. 4. Schematic of the proposed 4-rail CSCR converter with dual-polarity input, connection of the R-SC cells, and switch control for dual-polarity and reconfiguration operation.

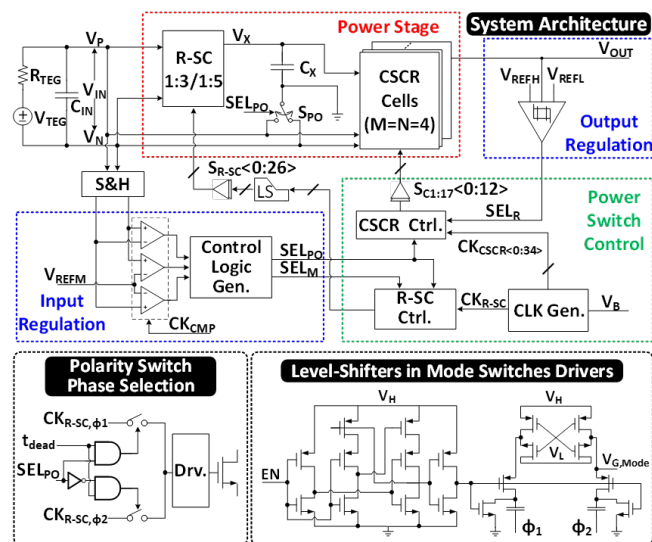


Fig. 5. The system overview of the proposed TEH system, and the circuit implementation of the phase selection for polarity switch pairs and the level-shifters for mode switches.

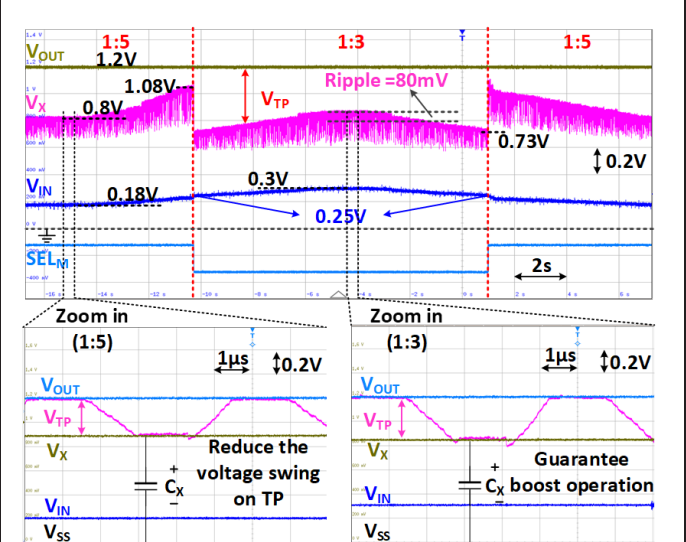


Fig. 6. The measurement results of the 4-rail CSCR converter with the R-SC configuration between 1:3 and 1:5.

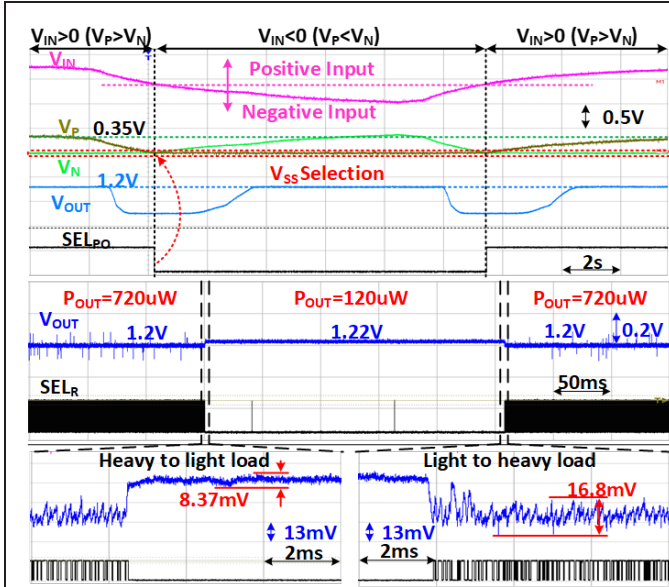


Fig. 7. Measurement results of the interface response for the polarity transitions, and the regulated output at 1.2V with different loads.

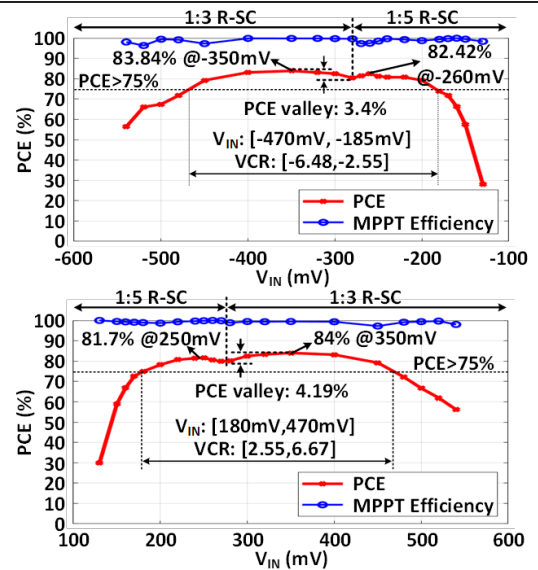


Fig. 8. Measured PCE at MPP and the MPPT efficiency versus the dual-polarity V_{IN} and respective VCR with V_{IN} .

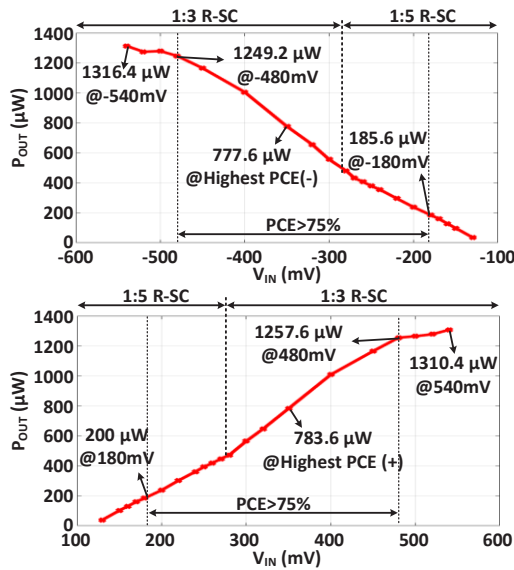


Fig. 9. Measured P_{OUT} versus dual-polarity V_{IN} with 1.2V regulated V_{OUT} .

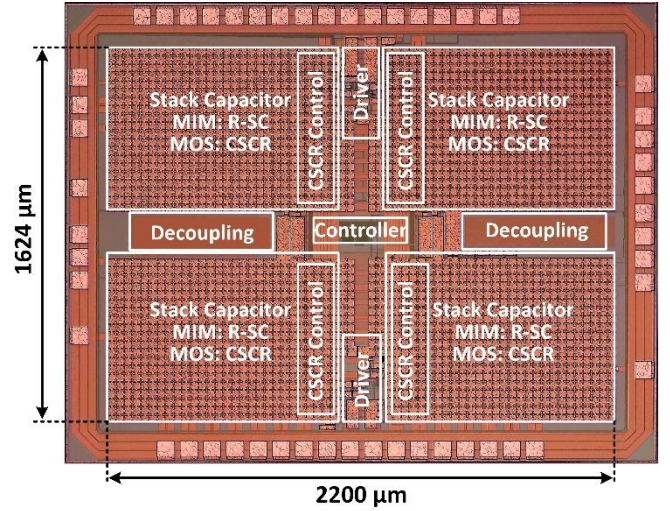


Fig. 10. Chip micrograph.

TABLE I. Comparison with state-of-the-art SC EH interfaces

Reference	Liu, JSSC'16 [4]	Gi, TCAS-I'20 [5]	Kim, JSSC'21 [6]	Wang, ISSCC'23 [11]	This Work
Technology (nm)	180	180	180	65	180
Active Chip Area (mm ²)	4	5.84	7.25	4.76	3.57
EH Source	PV+TEG	PV	TEG	PV	TEG
R_{REG} (Ω)	N/R	-	1260	-	130
On-chip Capacitance (nF)	2	19.8	10.2	19.8	CSCR: 8 R-SC: 4
SC Topology	R-SC	CSCR (M=39, N=11)	CSCR & SC (M=11, N=4)	RCSC (M=N=16)	4-rail CSCR (M=4, N=4)
f_{sw} Range (kHz)	27-1050	900-2700	CSCR: 15.3-67.1 SC: 625-10000	200-2000	CSCR: 200-294 R-SC: 7600
V_{OUT} (V)	3.3	3.2	0.75	0.5-2	1.2
V_{IN} @ MPP (V)	0.45-3	0.64-1.4	0.1-0.5	0.4-2.5	$\pm(0.13-0.54)$
Max P_{OUT} (μW)	48	2100	20800**	39700	1310 (@ $R_{REG}=130\Omega$) 10800 (@ $R_{REG}=34\Omega$)
Peak PCE @ V_{IN}	89% @ 2.5V	88.9% @ 1.4V	85.4% @ 0.4V	90% @ 1.78V	84% @ +0.35V 83.84% @ -0.35V
Dual-Polarity Input	No	No	No	No	Yes
VCR Range (PCE>75%)	1.1-4	2.28-5*	1.5-3.75*	0.33-2	$\pm(2.55-6.67)$ $\pm(2.55-6.48)$

* Estimated from the paper ** This work includes a discharging path with a 1.3V battery

References

- [1] Q. Wan, et al., JSSC, vol. 54, no. 6, pp. 1720-1732, 2019.
- [2] P. Cao, et al., ISSCC, 2019, pp. 420-422.
- [3] Q. Kuai, et al., JSSC, vol. 57, no. 6, pp. 1899-1912, 2022.
- [4] X. Liu, et al., JSSC, vol. 51, no. 5, pp. 1302-1312, 2016.
- [5] H. Gi, et al., TCAS-I, vol. 67, no. 10, pp. 3601-3612, 2020.
- [6] H. Kim, et al., JSSC, vol. 56, no. 9, pp. 2724-2735, 2021.
- [7] Y. Jiang, et al., JSSC, vol. 54, no. 11, pp. 3118-3134, 2019.
- [8] N. Butzen, et al., ISSCC, 2017, pp. 178-179.
- [9] N. Butzen, et al., JSSC, vol. 54, no. 4, pp. 1039-1047, 2019.
- [10] Lipski M., ICECS, 2020, pp. 1-4.
- [11] Y. Wang, et al., ISSCC, 2023, pp. 1-3.