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A Hybrid Magnetic Current Sensor With a Dual Differential DC Servo Loop

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***Abstract*— This article presents a hybrid magnetic current sensor for contactless current measurement. Pick-up coils and Hall plates are employed to sense the high and low-frequency fields, respectively, generated by a current-carrying conductor. Due to the differentiating characteristic of the pick-up coils, a flat frequency response can then be obtained by summing the outputs of the coil and the Hall paths and passing the result through a 1st-order low-pass filter (LPF). For maximum resolution, the LPF corner frequency (2 kHz) is set such that the noise contribution of each path is equal. To suppress the coil-path offset without the use of large ac coupling capacitors, an area-efficient dual dc servo loop (D3SL) is used. This effectively suppresses the coil-path offset, resulting in a total offset of 73 μT, which is mainly dominated by the Hall path. Fabricated in a standard 0.18-μm CMOS process, the current sensor occupies 3.9 mm^2 and draws 7.1 mA from a 1.8 V supply. It achieves 43 mA resolution in a 5 MHz bandwidth, which is 1.5× better than the state-of-the-art hybrid sensors. It also achieves the lowest energy efficiency FoM (3.5×) among CMOS magnetic current sensors.**

***Index Terms*— Contactless sensing, dc servo loop (DSL), high resolution, hybrid current sensors, magnetic current sensing, temperature compensation.**

I. Introduction

MAGNETIC current sensors are widely employed in high-voltage industrial applications such as electric drivers, photovoltaic inverters, chargers, and power supplies. In such applications, their inherent galvanic isolation outweighs their lower accuracy and resolution compared to shunt-based sensors [1], [2], [3], [4].

Magnetic current sensors can be made using fluxgates [5], [6], [7], magnetoimpedance [8] and tunneling magnetoresistance (TMR) [9] sensors. Their limited linearity means that closed-loop current sensing schemes are required to achieve high dynamic range (DR) [5]. However, the need to drive a field-canceling coil makes it difficult to achieve wide bandwidth. Furthermore, magnetoimpedance and TMR sensors are not CMOS-compatible, leading to two-die solutions and increased production cost.

Alternatively, magnetic current sensors can be made using CMOS-compatible Hall plates and pick-up coils, which have a much wider linear input range [10], [11], [12], [13], [14], [15]. However, although they can achieve wide bandwidths, pick-up coils cannot sense dc signals, while the resolution of Hall plates decreases with the square-root of bandwidth due to its thermal noise. By combining Hall plates and pick-up coils, hybrid current sensors with wide bandwidth and high resolution can be realized [16], [17], [18], [19], [20].

One of the main challenges in the design of hybrid current sensors is achieving a flat response over the frequency range. A current sensor with a flat frequency response ensures compatibility with frequency-dependent systems, enabling accurate current monitoring and control over a wide frequency range. As shown in Fig. 1, a 1st-order low-pass filter (LPF) can be used to smoothly combine the differentiating characteristic of coils and the all-pass characteristic of Hall plates. The corner frequency of the LPF defines the crossover frequency f_X, which also defines the sensor's noise bandwidth. For maximum resolution, f_X should be chosen such that the Hall and coil paths contribute the same amount of noise. In practice, a high-pass filter (HPF) is required to block the offset of the coil path, which may often be significantly larger than the mV-level output of the Hall plates. However, the HPF creates a parasitic pole at f_{Par} in the coil path, which, in turn, causes a dip around f_X in the combined response of the two signal paths. To minimize this dip, f_{Par} must be set much lower than f_X, which is quite challenging since f_X is typically in the order of a few kHz.

In [17], the crossover frequency f_X (=2 kHz) was optimized for maximum resolution, while coil-path offset was blocked by the combination of ac-coupling and a dc-servo loop. However, a large off-chip capacitor (10 μF) was used to stabilize the dc servo loop (DSL). Furthermore, this design sensed the coil voltage, which, due to its differentiating characteristic, limited its high-frequency DR. The sensor achieved a resolution of 480 mA$_{rms}$ in a 3 MHz BW and consumed 38.5 mW.

In [20], a hybrid current sensor achieves greater DR by reading out the coil current instead of the coil voltage. To eliminate the need for external components, its coil path employed a two-stage LPF. Coil-path offset was then blocked by a large on-chip capacitor (1.2 nF) placed between the two stages. However, the resulting parasitic pole caused a 3% dip in the sensor's frequency response around f_x (=10 kHz). Compared

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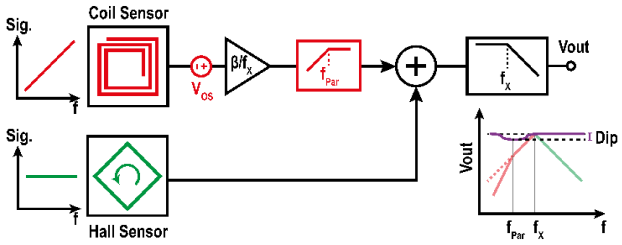

Fig. 1. Effect of parasitic pole on the gain flatness.

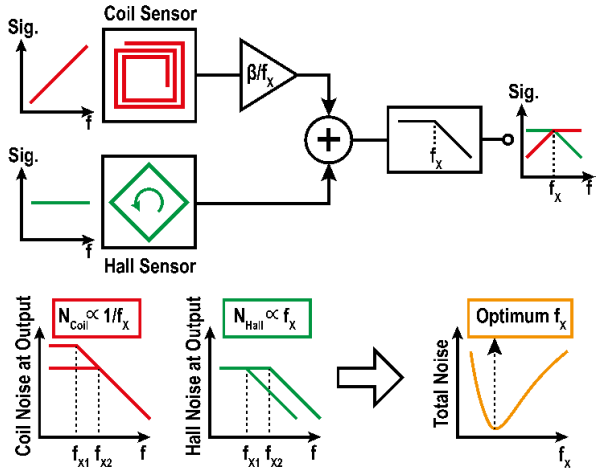

Fig. 2. System block diagram and optimum crossover frequency.

to [17], this sensor achieves 7× better resolution (69 mA_{rms}) and 3× less power dissipation (14 mW).

In this article, an extended version of [21], the design of a hybrid magnetic current sensor with an optimized crossover frequency is presented. As in [16] and [20], a two-stage coil path is used. However, to simultaneously suppress coil-path offset and achieve good gain flatness, the large blocking capacitor in [16] and [20] is replaced by an area-efficient dual-differential dc servo loop (D3SL). The gain drift with temperature of the Hall plates is partially compensated by a near-PTAT bias current. Their remaining gain drift is compensated for by designing the amplifiers in the Hall path to have a temperature-dependent gain. A similar approach is used to compensate for the gain drift of the coil path.

The rest of this article is organized as follows. The proposed system, including the crossover frequency optimization for noise, the design of the D3SL, and the temperature compensation in both the coil path and Hall path, are presented in Section II. Section III shows and discusses the measurement results. Finally, conclusions are drawn in Section IV.

II. Proposed Hybrid Magnetic Current Sensor

A. System Architecture

A system block diagram of the proposed hybrid current sensor is shown in Fig. 2. A LPF with a corner frequency f_X is used to flatten the coil's differentiating characteristic and to limit the noise bandwidth of the Hall path. To achieve a flat response, the output of the coil path at f_X must be equal to that of the Hall path. As a result, the gain of the coil path can be expressed as β/f_X, where β is a constant. Taking into account the equivalent noise bandwidth of a 1st-order filter, the total output noise power of the Hall path is proportional to f_X and can be expressed as

$$N_{\text{Hall}} = 2kTR_{\text{H}} \times \pi f_{\text{X}} \tag{1}$$

where R_H is the output resistance of the Hall plate. In contrast, the output noise power of the coil path is inversely proportional to f_X and can be expressed as

$$N_{\text{Coil}} = 2kTR_{\text{C}} \times \beta^2 \times \frac{\pi}{f_{\text{X}}} \tag{2}$$

where R_C is the resistance of the coil.

The sensor's total noise power is the sum of the contributions of the coil path and the Hall path. As shown in Fig. 2, if the crossover frequency is set too low, the noise of the coil path will be dominant, while if it is set too high, the noise of the Hall path will become dominant. At the optimum crossover frequency, the noise contribution of both paths is equal, resulting in the minimum total output noise. This optimized crossover frequency can be calculated as

$$f_{\text{X,Opt}} = \sqrt{\frac{R_{\text{C}}}{R_{\text{H}}}} \times \beta. \tag{3}$$

In this design, $f_{X,Opt}$ is 2 kHz. Simulations show that even large (20%) variations in f_X only increase the total noise slightly (<4%). Therefore, no trimming is required.

A simplified single-ended schematic of the proposed hybrid current sensor is shown in Fig. 3, while the actual implementation is fully differential. As in [16] and [20], the coil path employs a two-stage LPF based on a pole-zero cancellation scheme for reading out the coil current. The first stage sets a pole $f_{p1} = 140$ kHz $(1/2\pi R_1 C_1)$ to limit the first-stage output swing at high frequencies, while the second stage cancels the pole f_{p1} with a zero f_{z2} $(1/2\pi R_3 C_3)$ and introduces a new pole $f_X = 2$ kHz $(1/2\pi R_4 C_3)$. The pole f_X sets the crossover frequency and is chosen for maximum resolution. To ensure the robustness of the pole-zero cancellation scheme, the same type of components are used to realize f_{p1} and f_{z2}.

In the Hall path, the up-modulated outputs of the spinning Hall plates are first amplified by two capacitively coupled amplifiers (CCAs). The amplified Hall signal is then demodulated back to dc and injected into the 2nd stage of the coil path via an LPF with a pole at f_{z2}. The combination of this LPF

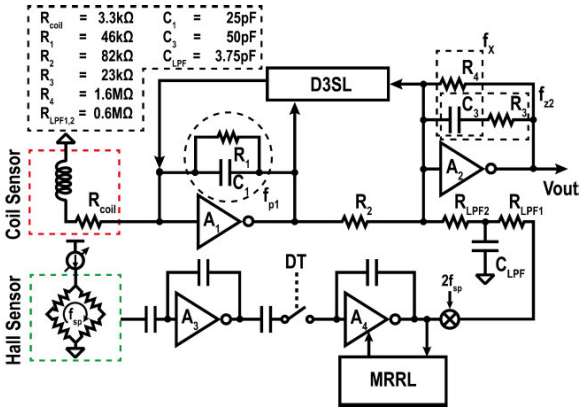

Fig. 3. Simplified single-ended schematic of the hybrid sensor.

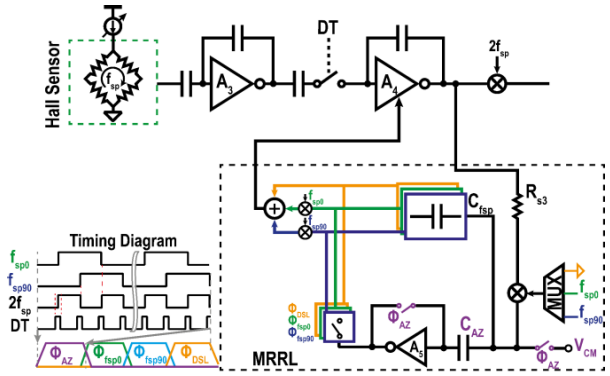

Fig. 4. Multiplexed RRL.

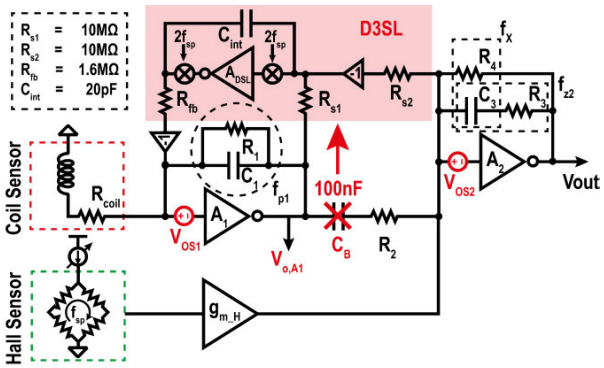

Fig. 5. Dual differential dc servo loop.

and the transfer function of the coil-path's 2nd stage results in a 1st-order LPF with a pole at f_X.

As in [20], a multiplexed ripple-reduction-loop (MRRL) is used to suppress spinning-induced ripple (Fig. 4), which is caused by the offset of the Hall plates [22]. The ripple can be decomposed into four orthogonal components: two square waves in quadrature at f_{sp}, a square wave at $2f_{sp}$ that results in a residual offset in the final output, and a dc component that is blocked by the first CCA. The MRRL operates in four phases to consecutively suppress the quadrature component at f_{sp}, the offset of A_4, and the offset of A_5. In the first two phases, the MRRL is configured as a ripple-reduction loop (RRL), which senses the ripple via a sensing resistor R_{s3} (=10 MΩ) and a chopper demodulator. The resulting dc signal C_{fsp} (=5 pF) to generate a correction signal, which is then up-modulated and fed back to the amplifier A_4 via an auxiliary input stage. In the second phase, the choppers are disabled, and the MRRL functions as a DSL to attenuate the offset of A_4. In the last phase, the offset of A_5 is autozeroed to reduce the residual ripple it causes.

B. Dual Differential DC Servo Loop

To achieve accurate sensing of dc signals using the Hall path, it is essential to eliminate the offset contribution of the coil path. Without an offset cancellation technique, the offsets of A_1 and A_2 would be amplified, resulting in an output-referred offset in the coil path (Fig. 5)

$$V_{OS,Out} = -\left(1+\frac{R_1}{R_{Coil}}\right)\left(\frac{R_4}{R_2}\right)V_{OS1} + \left(1+\frac{R_4}{R_2}\right)V_{OS2} \quad (4)$$

where V_{OS1} and V_{OS2} are input-referred offsets of A_1 and A_2, respectively. In [16] and [20], a blocking capacitor is used between the coil-path stages to attenuate the coil-path offset. Due to its high impedance at dc, the blocking capacitor rejects V_{OS1} and ensures that V_{OS2} appears at the output with a gain of 1. However, the blocking capacitor C_B and the series resistor R_2 create a parasitic pole f_{Par} (=230 Hz), which causes a dip in the sensor's transfer function. In [20], C_B (1.2 nF) occupies more than 10% of the chip area, and R_2 (500 kΩ) contributes 25% of the noise in the coil path. Therefore, it is not possible to further increase the size of these components to decrease f_{Par}. Instead, a higher than optimal crossover frequency (10 kHz rather than 2 kHz) was chosen in [20] to achieve less than 3% dip around f_X. To achieve the optimum crossover frequency (2 kHz), reduce the noise contribution of R_2 to less than 5%, and achieve a gain flatness of ±1%, a 100× larger blocking capacitor would be required, which is not practical.

Therefore, the blocking capacitor is replaced by a D3SL in this work (see Fig. 5). It senses the dc voltage across R_2 and drives it to zero by regulating the output of A_1. Like a blocking capacitor, this ensures that the dc current flowing through R_2 is zero, by driving the output-referred offset of A_1 to V_{OS2}.

In the proposed scheme, the voltage across R_2 is sensed via two sensing resistors $R_{s1,2}$ (=10 MΩ), and then integrated on a capacitor C_{int} (=20 pF) built around the amplifier A_{DSL}. The resulting voltage is fed back to the input of A_1 via a feedback resistor R_{fb} (=1.6 MΩ) to close the feedback loop and regulate the output of A_1. By applying feedback theory, f_{Par} caused by the D3SL can be calculated as

$$f_{Par} = \frac{1}{2\pi \times R_{s1,2} \times C_{int} \times \frac{R_{fb}}{R_1}} \quad (5)$$

in this design $R_{s1,2}$ = 10 MΩ, R_{fb} = 1.6 MΩ, R_1 = 46 kΩ, and C_{int} = 20 pF, which leads to a D3SL corner frequency f_{Par} = 15 Hz.

As shown in Fig. 6, to reduce the offset of A_1 to less than 1 μV, a two-stage amplifier A_{DSL} with a high dc gain of 120 dB is employed. The first stage of A_{DSL} is a current reuse telescopic stage designed to maximize noise efficiency, while the second stage is a conventional common source stage with a rail-to-rail output driver. To achieve a 60° phase margin, a Miller compensation capacitor with a nulling resistor is used. To mitigate the offset of A_{DSL}, the first-stage PMOS and NMOS input pairs are chopped. Otherwise, the offset of A_{DSL} would appear at the output of A_1 and then be amplified to the final output. The choppers modulate A_{DSL} offset and the resulting ripple is then attenuated by the D3SL low-pass characteristic. Since $R_{s1,2}$ are much larger than R_2, and R_{fb} is much larger than R_{coil}, the noise contribution of the D3SL is negligible. From simulations, it only increases the output integrated noise by 5%.

C. Temperature Compensation

As Hall-plate sensitivity is strongly temperature-dependent, a temperature compensation scheme is required. Otherwise, the Hall plates would exhibit a significant gain drift over

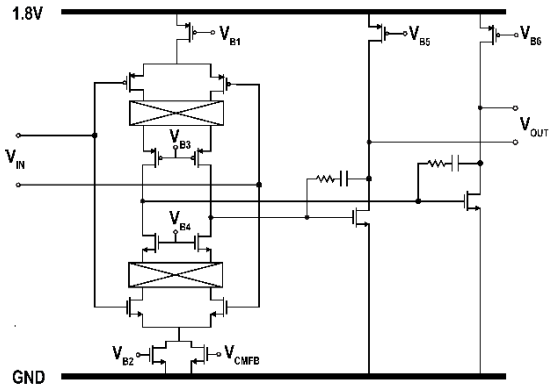

Fig. 6. Schematic of A_{DSL}.

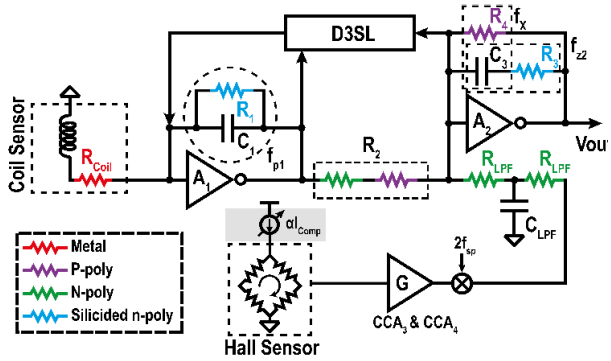

Fig. 7. Temperature compensation scheme.

temperature (>20% from −70 °C to 170 °C [23]). The sensitivity of the Hall path can be expressed as [see Fig. 7]

$$S_{\text{Hall-Path}} \propto I_{\text{Bias}} \times S_{\text{Hall}} \times \left(\frac{R_4}{2R_{\text{LPF}}}\right) \tag{6}$$

where I_{Bias} is the Hall-plate bias current and S_{Hall} is the current-related sensitivity of the Hall plate. It is worth noting that the gain of the CCAs (A_3 and A_4) used in the Hall path is temperature-independent. This is because the gain is determined by the ratio of capacitors.

In [16] and [20], a PTAT bias current with a large positive TC_{PTAT} is employed to partially compensate for the large negative TC (about −0.4%/K) of Hall plates. As the Hall plates are realized in an n-well layer with a large positive TC ($\text{TC}_{\text{Nwell}} = 0.37\%/\text{K}$), the supply voltage of the Hall plate has a very large TC of $\text{TC}_{\text{PTAT}} + \text{TC}_{\text{Nwell}}$ (∼0.77%/K). This limits the maximum bias current at room temperature for a given supply voltage.

In this work, to simultaneously compensate for the Hall-plates gain drift and increase the maximum bias current, two different types of resistors are used as R_4 and R_{LPF} (Fig. 7). R_{LPF} and R_4 are non-silicided n-poly (−0.15%/K) and non-silicided p-poly (−0.02%/K) resistors, respectively. Thus, the dc gain of the output stage has a positive TC of 0.13%/K.

The remaining Hall-plate sensitivity drift is compensated by using a tunable sub-PTAT bias current. As shown in Fig. 8, the sub-PTAT bias current is generated by forcing a PTAT voltage ΔV_{GS} across two parallel resistors: a fixed non-silicided n-poly R_{C1} (5.7 kΩ) and a tunable silicided n-poly R_{C2} (7.5–17.2 kΩ).

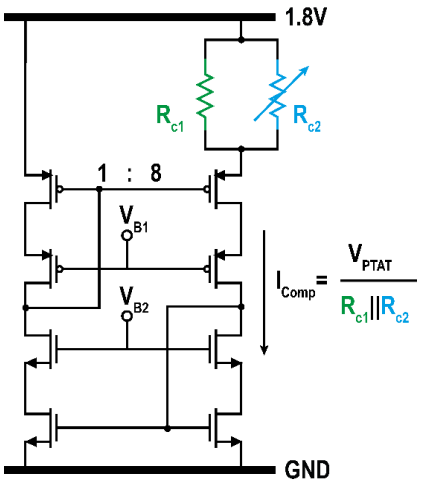

Fig. 8. Tunable sub-PTAT bias generator.

This tunability provides ±9% tuning range with a resolution of 0.3%.

As the coil path reads out the coil current and the coil is made of metal with a large TC of 0.34%/K, a temperature compensation scheme is required to minimize the gain drift over the temperature in the coil path. The coil-path output is proportional to the ratio of resistors

$$V\text{out}_{\text{Coil}} \propto \begin{cases} \dfrac{R_1}{R_{\text{Coil}} \times R_2}, & f_{\text{X}} < f < f_{\text{p1,z2}} \\ \dfrac{R_3}{R_{\text{coil}} \times R_2}, & f > f_{\text{p1,z2}}. \end{cases} \tag{7}$$

In [16] and [20], the TC of the coil resistance R_{Coil} is compensated by using silicided n-poly (TC = 0.29%/K) and non-silicided p-poly resistors (TC = −0.02%/K) as $R_{1,3}$ and R_2, respectively. However, the residual TC causes a 2.7% gain drift over the temperature range. In this work, this residual TC is canceled by combining two types of resistors as R_2: 75% non-silicided p-poly (TC = −0.02%/K) and 25% n-poly (TC = −0.15%/K) resistors. This combination achieves the desired TC to cancel the residual TC.

III. Measurement Results

The integrated hybrid current sensor [see Fig. 9] was implemented in a standard 0.18-μm CMOS process and occupied 3.9 mm^2. Similar to [16] and [20], it is mounted on a low-resistance (250 $\mu\Omega$) S-shaped current rail (Fig. 9, bottom). The current flows through the current rail, generating a perpendicular magnetic field over the rail slots. The resulting magnetic field is then sensed via two coils and Hall plates positioned above the slots. The S-shaped geometry provides differential sensing and higher sensitivity (∼2×) compared to a straight current rail. A non-conductive glue is used to isolate the chip from the current rail. The die thickness is 200 μm. This results in a current-to-magnetic coupling of about 283 μT/A. The sensor draws about 7.1 mA from a 1.8-V supply at room temperature. About 60% of this current (4.4 mA) is used to bias the Hall plates. Each Hall plate consists of four Hall devices connected in parallel to reduce the initial offset. The current-related sensitivity of each Hall

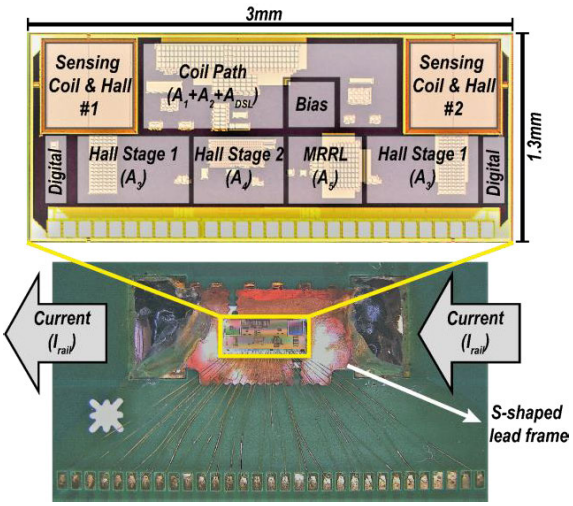

Fig. 9. Sensor die on a copper lead-frame (bottom) Die micrograph (top).

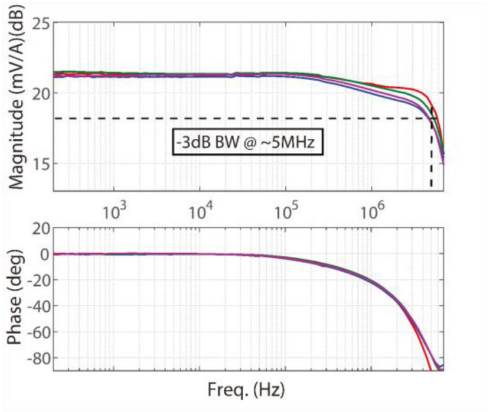

Fig. 10. Sensitivity versus frequency.

device is 45 V/A · T. Based on the geometry of the current rail, the coils consist of 43 minimum-width turns of top metal with an outer width of 500 μm. The coil can be modeled as a series inductance (1043 nH) with a resistance (3.3 kΩ), in parallel with a parasitic capacitor (3.95 pF). Simulations show that the coil current flowing into the virtual ground of A_1 has a differentiating characteristic up to ~100 MHz.

In this design, a spinning frequency (f_{sp}) of 25 kHz is selected to achieve a good tradeoff between the offset and the filtered residual ripple. Fig. 10 shows the magnitude and phase of the sensor's overall frequency response with a 1-A input dc through the current rail. Four samples have been measured. To achieve a flat frequency response, the Hall-plates biasing current is trimmed via an 8-bit current DAC. The −3 dB BW of the sensor is approximately 5 MHz. At frequencies above 200 kHz, the gain decreases slightly due to eddy current induced in the current rail [24]. This was confirmed by FEM simulations in ANSYS. These show that eddy-current effects cause the flux through the coils to roll off at frequencies above 150 kHz, which agrees well with the measured data. Since each of the prototypes was assembled by hand, we attribute the observed spread in the roll-off to variations in the vertical distance between the coils and the lead-frame and in the alignment of the coil centers with the slits. The sensor's frequency response around f_X is shown in

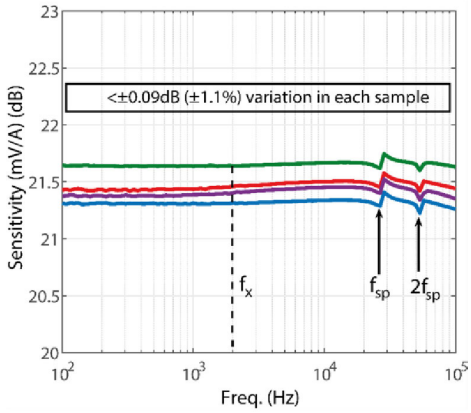

Fig. 11. Zoomed in sensitivity versus frequency around f_X.

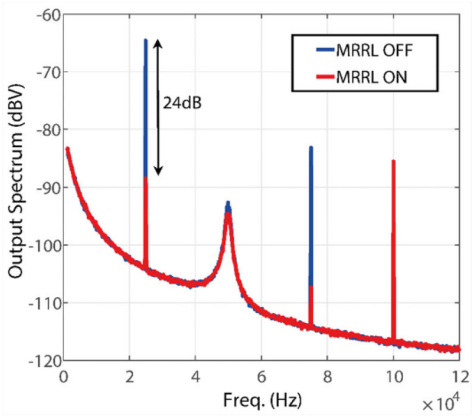

Fig. 12. Output spectrum w/ MRRL ON/OFF.

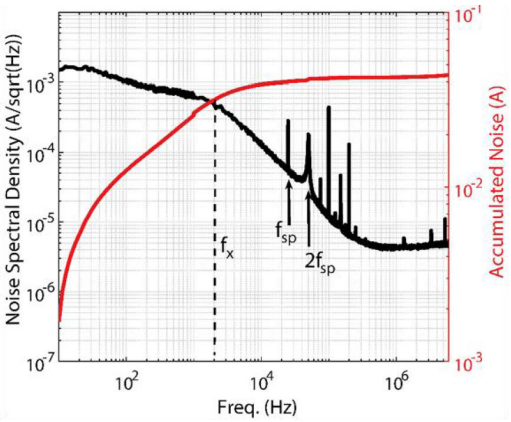

Fig. 13. Noise spectral density and accumulated noise referred to current rail.

Fig. 11. The parasitic pole caused by the D3SL causes less than 1% dip in the transfer function. The MRRL notches at f_{sp} and $2f_{sp}$ limit the gain variation to around ±1.1%.

The output spectrum at zero input current is shown in Fig. 12. Enabling the MRRL reduces the spinning tones at f_{sp} and $3f_{sp}$ by more than 24 dB. Measurements on five samples show that the achieved reduction spreads from 22 to 26 dB.

The noise spectral density and the accumulated noise are shown in Fig. 13. The noise spectral density has a 1st-order low-pass characteristic with a corner frequency of f_X (~2 kHz). At this frequency, the noise contribution of the coil path and the Hall path are equal. The integrated input-referred

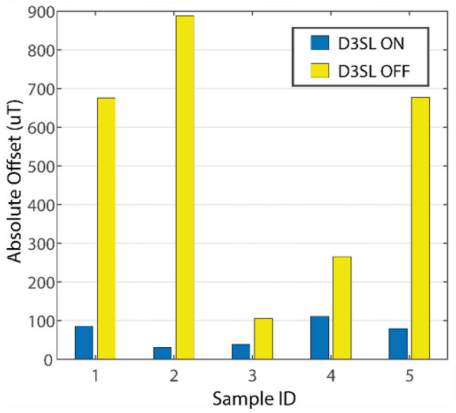

Fig. 14. Sensor absolute offset (Hall) referred to current rail w/ D3SL ON/OFF.

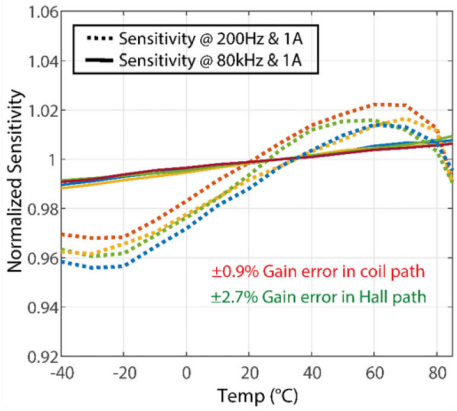

Fig. 15. Sensitivity versus temperature.

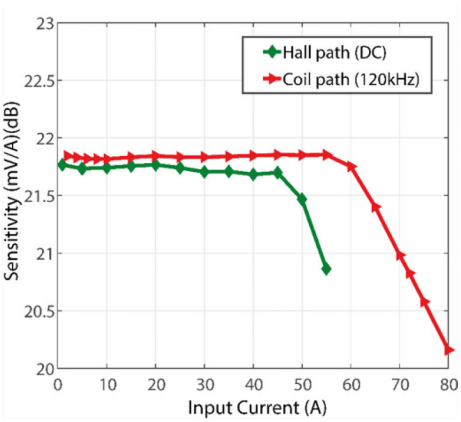

Fig. 16. Sensitivity versus input range for dc and extrapolated ac (rms) currents.

noise is 43 mA_{rms} in a 5 MHz BW. The total input-referred ripple is 5 mA_{rms}, which is more than 8× smaller than the integrated noise. In addition, the residual ripple at f_{sp} only causes a 0.3 mA step in the accumulated noise plot, which proves that the MRRL suppression is sufficient.

To verify the effectiveness of the proposed D3SL, the sensor offset (Hall + coil) of five samples has been measured (Fig. 14). By enabling the D3SL, the offset is reduced from 600 μT (1σ) to 73 μT (1σ). Of this, about 60 μT (1σ) is due to the output-referred offset of A_2, and could be reduced by e.g., trimming.

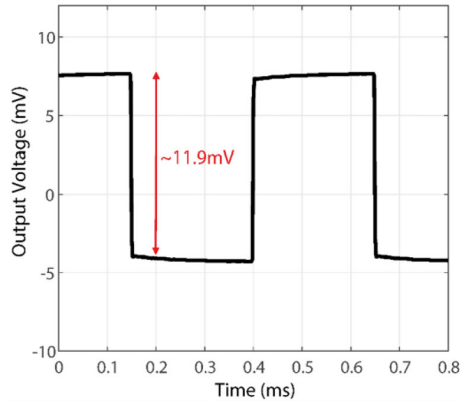

Fig. 17. Transient response for a 1 A_{p-p} square wave @ $f_X = 2$ kHz (1024× averaging).

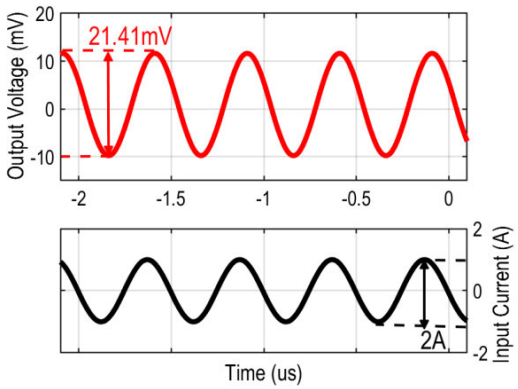

Fig. 18. Transient response for a $2A_{p-p}$ sine wave @1 MHz (1024× averaging).

The gain drift of the sensor is characterized in an oven from −40 °C to 85 °C. A 1-A input current is generated outside the oven and applied at 200 Hz and 80 kHz to measure the gain drift of the Hall and coil paths, respectively. The normalized sensitivities are shown in Fig. 15. After fixing the TC trim setting, four samples have been characterized. With a fixed TC trim setting, the coil path and Hall path gain drifts are below ±0.9% and ±2.7%, respectively.

To evaluate the linearity of the Hall path, a dc current is applied to the current rail. As shown in Fig. 16, the −1 dB compression point of the input current is 55 A, limited by the self-heating of the current rail. Due to the complexity of supplying large (tens of amps) current at high frequencies, the input range of the coil-path is determined by injecting a test current into the coil path (bypassing the coil sensors). This results in an equivalent input range of 72 A_p (51 A_{rms}). The sensor's response to a 1 A_{p-p} square wave and a 2 A_{p-p} sine wave are illustrated in Figs. 17 and 18, respectively. The slight lack of amplitude flatness in the square-wave response is due to the residual gain mismatch between the Hall and coil paths.

Table I summarizes the performance of the proposed hybrid sensor in comparison to other state-of-the-art magnetic current sensors. Compared to prior hybrid sensors, the resolution (1.5×), DR (+9.5 dB), and gain error (1.6×) have significantly improved. Furthermore, it achieves the highest

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Source	**This work**	JSSC'23 [20]	JSSC'17 [17]	JSSC'19 [14]	JSSC'22 [5]	APEC'19 [19]
Sensor Type	**Coil + Hall**	Coil + Hall	Coil + Hall	Hall	IFG	Coil + Hall
Technology (μm)	**0.18**	0.18	0.18	0.35	0.25	0.18
Supply (V)	**1.8**	1.8	5	3.3	1.8/5	1.8
Area (mm^2)	**3.9**	4.6	8.75	N/A	4+3.6	2.74
Resolution (mA_{rms})	**43**	69	480	480	11[c]	710
Input Range (A)	**DC: ±55[a] AC: ±51[a]**	±46[a]	±18[a]	±300	±53[c]	±60
Dynamic Range (dB)	**61.5**	54	17	56	74	39
BW (MHz)	**5**	5	3	1.7	0.125	15.3
Power Consumption (mW)	**12.8**	14	38.5	13.2	100[d]+13	63.5
Gain Flatness	**±1.1%**	±1.5%	N/A	N/A	N/A	±3.7%
Residual Ripple @f_{sp} (μT)	**1.5**	6	8	N/A	N/A	N/A
Residual Offset (μT)	**73**	57	40	262	N/A	N/A
FoM[b][fW/Hz]	**0.45**	1.6	2281	5	8.5	145

[a]Extrapolated [b]FoM = Power/(BW x (Range/Resolution)^2) [c]Conversion rate = 45μT/A [d]Full-range power

energy-efficiency FoM (3×) among other magnetic current sensors.

IV. CONCLUSION

This article presents a hybrid magnetic current sensor consisting of coil sensors and Hall plates for high and low frequencies, respectively. A two-stage LPF reads out the coil current, while two CCAs are used to amplify the upmodulated Hall voltage. By optimizing the crossover frequency f_X (2 kHz) for noise, coil and Hall paths are combined. A D3SL reduces the coil-path offset from 600 to 73 μT. The D3SL acts similar to a blocking capacitor between the coil-path stages in an area-efficient manner. With this approach, the D3SL causes a parasitic pole at 15 Hz which is more than 100× smaller than f_X and so has a negligible effect (±1% dip) on the gain flatness. To achieve the same flatness and parasitic pole, a 100 nF blocking capacitor would have been required, occupying ∼100× more chip area. The gain drift over the temperature in both paths is reduced by using different types of resistors. In addition, in the Hall path, a sub-PTAT bias generator is employed to cancel the residual TC of the Hall path. This results in a gain error of ±0.9% and ±2.7% (from −40 °C to 85 °C) in the coil and Hall paths, respectively. Overall, the presented sensor is the most energy-efficient magnetic sensor reported so far, achieving a FoM of 0.45 fW/Hz.

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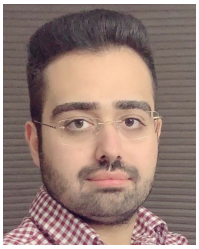

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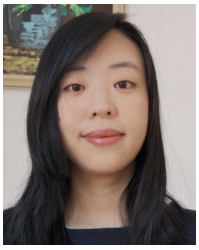

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