Design Study on the Switched and Linear Operation of Broadband CMOS Class-E Power Amplifiers

A thesis submitted to the

Faculty of Electrical Engineering, Mathematics and Computer Sciences

in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering

at

Delft University of Technology

by

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August 2010

Abstract

This research work aims to gain understanding of the power amplifier (PA) operating as a linear PA under low power drive conditions and as a switch-mode PA in high power drive conditions both with the same Class-E load. Two approaches were taken here. Firstly, an analytical approach was developed to investigate the switching operation of conventional Class-E amplifier. The model used in the analytical approach takes into account the non-ideal switch resistance, finite dc-feed inductance, finite loaded quality factor, and arbitrary switch duty-cycle. This approach presents an accurate closed-form expression for modeling Class-E power amplifier. Using this approach, the frequency response of conventional Class-E power amplifier was studied in detail and the impact of the loaded quality factor and finite dc-feed inductance on the broadband performance was analyzed. It shows that the Class-E PA with conventional load network cannot provide stable output power, efficiency, and reliable operating voltage conditions across a broad frequency band ($\Delta B > 40\%$). In addition, study of the load impedances of the amplifier indicates that the Class-E PA is sensitive to the load phase angle at fundamental frequency.

In the second approach, a purely linear voltage-control current source was constructed numerically as a way to represent the transistor. Based upon that model, the influence of non-ideal drive signal on the switching operation was studied. It shows that the power amplifier with finite dc-feed inductance is tolerant to a non-ideal drive signal. For the rise and fall times of 25%T, only 5% drop in drain efficiency was found for the optimum finite dc-feed inductance. The performance of that model in linear operation was also investigated. The results agree with the classical theory for linear power amplifiers.

The linearity (intermodulation distortion and 1dB compression point) was analyzed by using a realistic transistor model (an extended drain NMOS). It shows that the Class-B biased PA with finite dc-feed inductance can provide not only similar IMD3 feature as the optimum Class-AB biased PA with RF choke does, but also high efficiency simultaneously. Based upon this device, a systematic design process was applied to implement a broadband high efficiency Class-E PA. The PCB for this broadband high efficiency Class-E PA was fabricated. Good agreement was found between the simulation and measurement. The measurements indicated that the PA achieves a drain efficiency > 67% and a PAE > 52% with a Pout > 30dBm from 560-1050MHz, where the output power variation is within 1.0dB and efficiency variation is within 13%. The highest efficiency is observed at 700MHz from a 5.0V supply with peak drain efficiency of 77% and peak PAE of 65% at 31dBm output power and 17dB power gain. When using dynamic supply modulation, the PA achieves a PAE of 40% and a drain efficiency of 60% at 10dB power back-off across the frequency band 500MHz to 1100MHz.

Acknowledgements

I would like to take the opportunity to acknowledge to all the people who helped me in my works and life.

My sincere gratitude is directed to my daily supervisor Ir. Mustafa Acar at NXP Semiconductors Research. He actively instructed me through the entire project, shared the valuable knowledge with me, offered useful support at every stage of the project, and answered all my questions with great patience. I would like to thank my other two supervisors at NXP Semiconductors Research: Dr.-Ing. Mark P. van der Heijden and P.D. Eng. Melina Apostolidou for the fruitful discussions in daily work and the feedback during the monthly meetings. Also thanks Dr.-Ing. Agnese Bargagli for kind help in Cadence simulation.

I am deeply grateful to my supervisor Dr.-Ing. Leo C.N. de Vreede at Delft University of Technology for providing me such a good opportunity to do this interesting research project at NXP, for visiting my progress presentations in Eindhoven, and for reviewing my thesis report. I also thank all the M.Sc. Thesis Committee members for reviewing this report.

My thanks are extended to all engineers at NXP Nijmegen, especially Michel de Langen and Tennyson Nguty, for bonding the dies and assembling the boards. I would also like to express my appreciation for the support I received from Jan Vromans in doing the measurements with the Labview setup.

I would like to acknowledge my friends and teachers at Delft University of Technology of the Netherlands who were kindly helping me during my course work and teaching me with the best of their knowledge.

I owe my loving thanks to my parents, my sisters and friends in China. They supported me very much during my study abroad. Without their encouragement and understanding it would have been impossible for me to finish this work.

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Eindhoven, The Netherlands

August 15th, 2010

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Chapter 1

Introduction

1.1 Motivation

In wireless communication systems, power amplifiers (PAs) are considered as key blocks which have a great influence on the power level, efficiency, linearity and cost of the transmitter system. High-efficiency and high-linearity power amplifiers are always of great interest for designers. Unfortunately, efficiency and linearity usually conflict with each other [1][2]. For example, conventional linear PAs such as Class-A, Class-AB, and Class-B PAs have good linearity but low efficiency no matter in terms of peak efficiency or average efficiency at power back-off. On the contrary, the switch-mode PAs like Class-D and Class-E have high efficiency, but they are usually nonlinear in nature. To overcome the conflict, various transmitter architectures with improved average efficiency and intermodulation distortion (IMD) have been proposed. At present, three architectures have already shown attractive results, namely, supply voltage modulation-based methods like envelope tracking (ET), envelope elimination and restoration (EER) and polar modulation, load modulation-based concepts like Doherty, and linear amplification using nonlinear components (LINC)-based concepts like outphasing. For the outphasing concept in [3], mixed-mode operation of Class-B PA was proposed to enhance the average efficiency in power back-off operation. Fig. 1.1 shows the efficiency as a function of normalized output voltage for a pure Class-B amplifier, outphasing amplifier, and a mixed-mode outphasing amplifier. For intermediate and high output power, saturated Class-B mode is used, while for the very low output power normal Class-B operation is employed to improve the efficiency. When the Class-B amplifier delivers the saturated output power, it can be regarded as a switch. Hence, the operation mode of this amplifier alternates between switch-mode and linear-mode in this system.
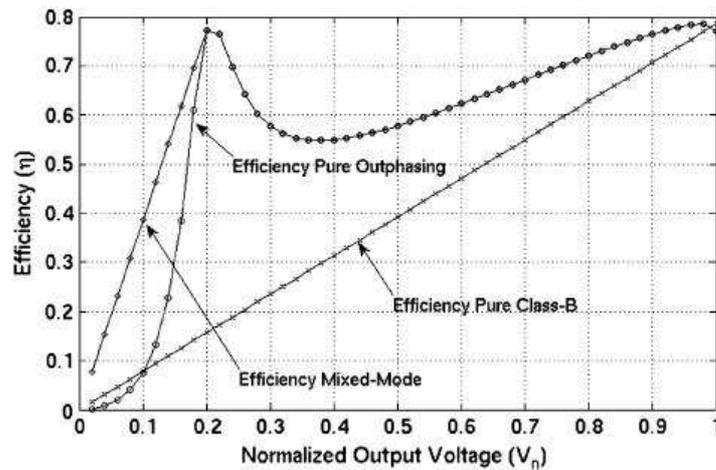
FIGURE 1.1: Mixed-mode outphasing amplifier

In addition, the coexistence of various wireless communication standards requires that the user terminal can cover the multi-mode multi-frequency operations. For the systems using amplitude-modulation signals, for instance, wideband code division multiple access (WCDMA), the amplitudes of signals are modulated to carry more information. Linear power amplifiers are needed for these systems. In contrast, the global system for mobile communications (GSM) and general packet radio service (GPRS) systems apply constant amplitude signals [4]. Saturated power amplifiers are employed in these systems to increase the efficiency. Therefore, multi-mode multi-frequency power amplifiers operating as a linear amplifier for amplitude-modulation signals and at the same time as a saturated or switch-mode amplifier for constant amplitude signals are highly desired.

These applications motivate us to investigate the hybrid-mode power amplifier which operates as linear-mode or switch-mode PA for different purposes in order to understand the trade-off between the linearity and efficiency.

1.2 Thesis Research Goal

To analyze the performance of switch-mode power amplifier, simple switch models were usually used as a starting point to simplify the transistor model [5]. These simple models are helpful, but do not represent the real RF operating conditions due to many assumptions made at the very beginning. Therefore, many of the design trade-offs assumed based upon the simple models are not correct in practice. Furthermore, the simple switch models cannot be used to analyze the linear operation of the power amplifier because of the discontinuity of switch resistance in the models.

Therefore, the main objectives in this thesis are

1. to analyze the properties of Class-E power amplifier operating in switch-mode or linear-mode,

2. to design broadband high efficiency CMOS power amplifier.

The end product of this thesis will be a hardware that can demonstrate the high efficiency feature over a broad frequency band.

1.3   State of the Art Review

To the best of the author's knowledge, there is little published work on hybrid-mode power amplifier. In [4], a multi-mode Class-AB/F power amplifier was implemented to operate for both IS-95A CDMA and PCS 1900 GSM signals. The circuit topology is based upon that of the Class-F amplifier. The mode of operation is set by the base bias. An intermediate fundamental load is selected to achieve both the Class-AB and Class-F operations. However, the topology of Class-F amplifier is quite complex to implement. In [6], a dual-mode (CDMA/AMPS) power amplifier was implemented by using SiGe/Si HBT process. Some simulation and measurement results were given with very simple design approach. It seems that no work has been published on a comprehensive analysis of hybrid-mode power amplifier based on Class-E topology. It is worth investigating how the load impedances and gate bias voltage affect the linearity and efficiency.

In this thesis, broadband Class-E power amplifier is also a very important subject. Recent works have demonstrated a high efficiency (more than 70%) Class-E power amplifier in broad frequency range (more than 20%).

Many researchers have applied the reactance compensation technique to design the broadband Class-E amplifier. In [7], a drain efficiency of 74% at 8W operating power and power flatness of 0.7dB were achieved across bandwidth of 135 to 175 MHz with a supply voltage of 7.2V by using the conventional output load network. A low loaded quality factor was used to realize the broadband application. In fact, the load impedance used in this paper is one special case of many solutions, which corresponds to maximum output power ($q = 1.412$) [5]. In [8], a double reactance compensation load network was designed to provide a wider bandwidth. The simulation results show that an octave-band (100-200MHz) power amplifier, with 1dB output power flatness and drain efficiency of about 70% can be achieved. Jager applied this technique to design multi-band and multi-mode handset power amplifiers for DCS1800, PCS1900, CDMA2000, and WCDMA [9]. By using InGaP/GaAs HBT technology, a Class-E power amplifier with gain of 22.5dB, output power more than 30dBm and high power added efficiency (PAE> 50%) was obtained from 1.6GHz to more than 2GHz.

In [10], Everard proposed a new topology placing an inductor in parallel with the shunt capacitor to present the constant load angle over a broad bandwidth. A 35% bandwidth with 60% drain efficiency over the band 130MHz to 180MHz was achieved.

In [11], Lie compared and discussed the effects of high breakdown and high-f_T SiGe transistors on the Class-E power amplifier. It shows that the output power of the high-f_T PA at higher frequencies is 1-1.5dB larger than that of high-breakdown PA. The frequency responses of PAE and gain of the high-f_T PA from 500MHz to 1200MHz are much flatter than that of high-breakdown PA. However, the peak PAE of high-breakdown PA is 4% higher than that of high-f_T PA.

In [12], a third-order Butterworth bandpass filter was applied to design broadband Class-E power amplifier from 600MHz to 1000MHz. The optimum load was obtained by using the load/source-pull simulation. By using GaN HEMT transistor, more than 33W output power with drain efficiency of 66% or better was obtained over all the band.

In [13], a cascode Class-E power amplifier has been introduced to allow a higher supply voltage without enhancing the device stress. To obtain a broad frequency range of operation, a relatively low quality factor has been used both in the driver and PA output network. The measured results show that a PAE of more than 60% over the 1.4-2GHz was achieved.

In [14], Qin employed a broadband Class-E power amplifier by using a low cost PHEMT device. A 5% improvement in PAE was found for open circuit termination of 2nd, 3rd and 4th harmonics, as compared to using 50 ohm load. With the conventional Class-E output load network, a bandwidth of 34.8% was achieved from 1.52GHz to 2.16GHz with more than 50% PAE. The peak PAE of 72.1% was obtained at 1.95 GHz. The variation of PAE in the band is about 20%.

In [15], a compact broadband Class-E power amplifier was implemented by using GaN HEMT transistor for base stations. It shows that the 2nd harmonic input tuning can improve drain efficiency by 8%. Good broadband performance is observed from 2.0GHz to 2.5GHz with drain efficiency of more than 74% and PAE > 71%.

Table 1.1 summarizes the state-of-the-art in terms of flatness of output power, drain efficiency, power added efficiency and output power in radio frequencies band. The topologies of output load network used in these papers are shown in Fig. 1.2.

1.4   Thesis Organization

This thesis is divided into two major parts: theory and implementations.

TABLE 1.1: Summary of published broadband Class-E PAs

Ref./Year	BW (GHz)	ΔB (%)	ΔP_{out} (dB)	Pout (dBm)	η (%)	PAE (%)	PAE_{PK} (%)	Technology	Topology
[8] 2001	0.1-0.2	66.7	< 1.0	> 40	> 70	N.A.	N.A.	LDMOS	Fig.1.2(b)
[11] 2006	0.5-1.2	82.3	< 3.0	> 17.2	N.A.	> 50	70	SiGe	Fig.1.2(a)
[12] 2009	0.6-1.0	50	< 1.7	> 45.2	> 66	> 61.9	80.6	GaN	Fig.1.2(d)
[13] 2005	1.4-2.0	35.3	< 1.0	> 22	N.A.	> 60	67	CMOS	Fig.1.2(a)
[14] 2004	1.52-2.16	34.8	< 2.0	> 20	N.A.	> 50	72.1	PHEMT	Fig.1.2(a)
[9] 2003	1.6-2.0	22.2	< 1.0	> 30	N.A.	> 50	55	InGaP/GaAs	Fig.1.2(c)
[15] 2009	2.0-2.5	22.2	< 2.5	> 38	> 74	> 71	74	GaN	Fig.1.2(a)
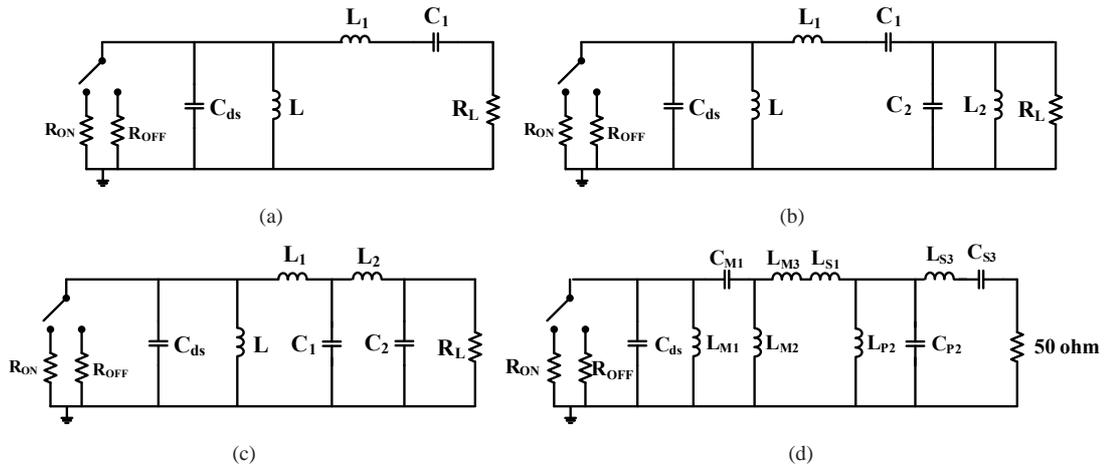
FIGURE 1.2: Topologies of output load network for broadband Class-E power amplifiers

- Chapter 2 aims to give a general overview of power amplifiers. It will introduce some important definitions that characterize a power amplifier. Then, a brief description of classification of RF power amplifiers is given.

- Chapter 3 presents the comprehensive analytical derivation of general Class-E model. This analytical model takes into account the non-ideal switch resistance, finite dc-feed inductance, finite loaded quality factor, and arbitrary duty-cycle. The model combines all possible operation modes of Class-E power amplifier together: optimum and sub-optimum operation. From the analytical solution, the required load impedance will be found. The influence of the load impedance on the efficiency, power-output capability and drain voltage and current waveforms will be discussed. In addition, the broadband characteristics of conventional Class-E output load network are investigated with the loaded quality factor, dc-feed inductance and duty-cycle as parameters.

- Chapter 4 builds up a purely linear transistor model to link the input drive signal and transistor behavior. The effects of a non-ideal drive signal (i.e. square wave with 10% rise and fall times, sinusoidal wave) on the switch-mode operation are investigated with the

dc-feed inductance as a parameter. Using this linear model, the effects of gate DC bias voltage on the 1dB compression point and efficiency of linear operation are analyzed.

- Chapter 5 analyzes the switching and linear operation of a real transistor (extended drain NMOS). The effects of finite dc-feed inductance and gate bias voltage on the linearity are discussed. In addition, a systematic design approach for broadband Class-E power amplifier will be presented, and the post-layout simulation for the proposed broadband Class-E power amplifier will be shown here.

- Chapter 6 presents the measurement setup and measurement results of proposed broadband Class-E power amplifier. The effects of dynamic supply modulation on the power added efficiency are verified.

- Chapter 7 concludes the thesis by giving some suggestions on the future work.

Chapter 2

Background

This chapter presents the main fundamental concepts of RF power amplifiers. First, some key parameters of an RF power amplifier are defined, as they will frequently be used in the following chapters. Then, an overview of different power amplifier classes of operation is described.

2.1 Parameters of Power Amplifiers

Power amplifiers are key elements to build a wireless communication system. They are used to amplify the signal being transmitted so that it can be received and decoded. The main performance parameters for a power amplifier are the output power that it can deliver, power gain, efficiency, and linearity [2][16][17][18][19].

2.1.1 Output Power

Consider the basic circuit of Fig.2.1, the output power is defined as the power delivered by the power amplifier and flowing into the load R_L.
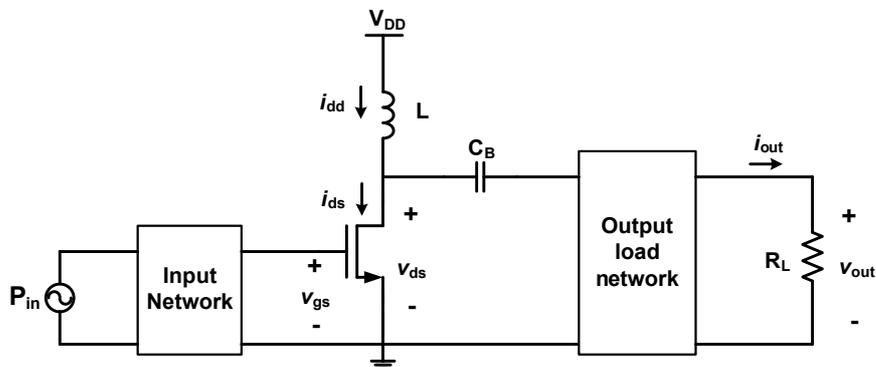
FIGURE 2.1: Block diagram of power amplifier

The instantaneous output power is defined as

$$p_{out}(t) = v_{out}(t) \cdot i_{out}(t). \tag{2.1}$$

The total or average output power P_{out} is defined as

$$P_{out,tot} = \frac{1}{T} \int_{-T/2}^{T/2} p_{out}(\tau) \, d\tau. \tag{2.2}$$

In most cases, only the power at the fundamental frequency is desired and the harmonics power is suppressed to very low level. Thus, it is more meaningful to define a fundamental average output power, P_{out,f_0}. Assuming the fundamental output voltage is a sine wave with operation frequency f_0 and amplitude of V_0, the fundamental average output power is defined as

$$P_{out,f_0} = \frac{V_0^2}{2R_L}. \tag{2.3}$$

The amplitude V_0 can be obtained from the Fourier Series expansion of $v_{out}(t)$. In the following text, the general term output power, denoted as P_{out}, will be used to indicate the average output power at the fundamental frequency.

2.1.2 Power Gain

To drive the power amplifier, a certain amount of RF input power at operation frequency f_0 is needed. The power gain at operating frequency is defined as

$$G_P = 10log_{10}(\frac{P_{out}}{P_{in}}). \tag{2.4}$$

2.1.3 Efficiency

A power amplifier is used to convert DC power from power source into RF power. Efficiency is a measure of how much of the DC power source is usefully applied to the amplifier's output load. The DC power consumption P_{DC} is defined as

$$P_{DC} = V_{DD} \cdot I_{DD}. \tag{2.5}$$

where I_{DD} is the dc component of Fourier Series expansion of $i_{dd}(t)$. The drain or collector efficiency η is defined as

$$\eta = \frac{P_{out}}{P_{DC}}. \tag{2.6}$$

To account for the power gain of the power amplifier, the Power Added Efficiency (PAE) is a more practical measure and it is defined as

$$
\begin{aligned}
PAE &= \frac{P_{out} - P_{in}}{P_{DC}} \\
&= \eta(1 - \frac{1}{G_P})
\end{aligned}
\tag{2.7}
$$

If the power gain is sufficiently high, the PAE defined in Eq.2.7 becomes equal to the drain efficiency.

2.1.4 Power-Output Capability

The power-output capability c_p is useful for comparing different types of amplifiers, and is defined as the output power produced when the device has a peak drain or collector voltage of 1 volt and a peak drain or collector current of 1 ampere. Assuming the maximum drain voltage in Fig.2.1 is V_{DSM} and the maximum drain current is I_{DSM}, the power-output capability is given by

$$c_p = \frac{P_{out}}{V_{DSM}I_{DSM}}. \tag{2.8}$$

2.1.5 Linearity

In the communication systems (W-CDMA, WiMAX, W-LAN), the transmitted signals have varying envelopes. In order to amplify these signals, the power amplifiers must have sufficient amplitude linearity. The third-order intercept point (IP3), adjacent channel power ratio (ACPR), 1dB compression point, and harmonics suppression are various means of quantifying linearity of power amplifiers.

The 1dB compression point (P1dB) of a power amplifier indicates the output power level that causes the gain to drop by 1dB from its small signal value. The 1dB compression point of the amplifier with a third-order nonlinearity is illustrated in Fig.2.2. The third-order intercept point (IP3) is the point where the third-order term as extrapolated from small-signal conditions crosses the extrapolated power of the fundamental. ACPR is defined as the ratio of power in a bandwidth
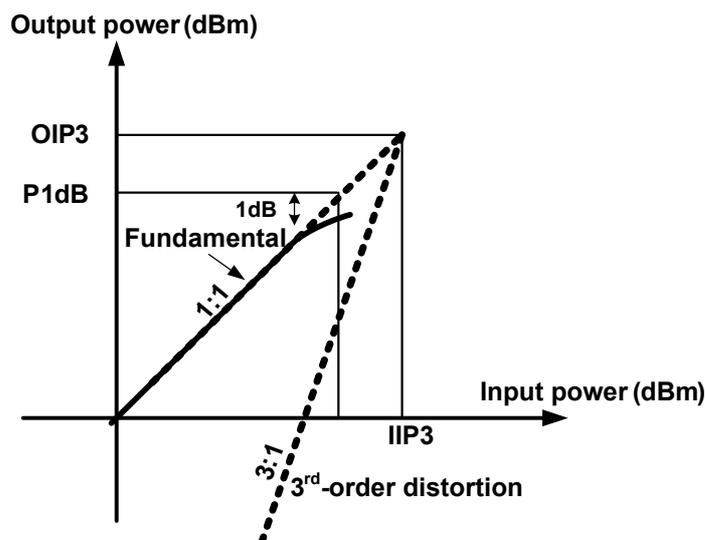
FIGURE 2.2: 3rd-order intercept point and 1dB compression point definitions.

away from the main signal (the distortion product) to the power in a bandwidth within the main signal.

2.2 Power Amplifier Classification

For the power amplifier shown in Fig.2.1, the MOS transistor can be operated [20]

- as a dependent-current source;

- as a switch.

When a MOSFET is operated as a dependent-current source, the transistor must be operated in the active region or the saturation region. The drain-to-source voltage V_{ds} must be larger than the overdrive voltage $V_{gs} - V_{TH}$, where V_{TH} is the transistor threshold voltage determined by the characteristics of the active device. The drain current I_{ds} and the drain-to-source voltage V_{ds} are determined by the gate-to-source voltage V_{gs} and the transistor biasing point. The magnitudes of I_{ds} and V_{ds} are nearly proportional to the magnitude of V_{gs}. The transistor produces an amplified replica of the input voltage or current waveform, and provides an accurate reproduction of both the envelope and the phase of the input signal. Therefore, this type of operation is suitable for linear power amplifier which is required to amplify amplitude modulated signals.

When a MOSFET is operated as a switch, the transistor is operated in the triode region or linear region when the transistor is conducted and in the cutoff region when the transistor is shut down. To maintain the MOSFET in the triode region or linear region, the drain-to-source voltage V_{ds} is less than the overdrive voltage $V_{gs} - V_{TH}$. When the transistor is operated as a switch, the
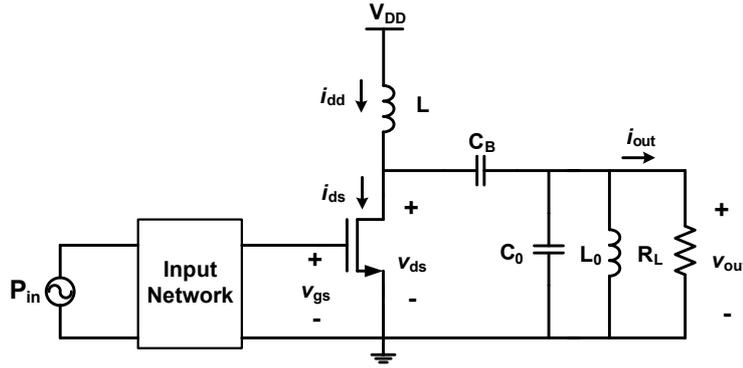
FIGURE 2.3: Linear power amplifier schematic.

magnitude of I_{ds} and V_{ds} are independent of the magnitude of V_{gs}. The transistor output is represented as a non-ideal single-pole single throw switch: the ON-resistance may be non-zero, the OFF-resistance may be non-infinite, and the turn-on and turn-off switching times may be non-zero. As the switch is cyclically operated at the desired operation frequency, DC energy from the power supply is converted to RF energy at the switching frequency and harmonics.

2.2.1   Linear Power Amplifier

For linear power amplifier, the MOSFET is operated as a dependent-current source. The classification of this type operation is based on the conduction angle of the drain current. Fig.2.3 shows the classical linear power amplifier topology. The optimum resistive load R_L is in parallel with the harmonic trap (C_0 and L_0) which is used to remove the unwanted harmonic components. The dc-feed inductor is usually an RF choke, and capacitor C_B is used for ac coupling. The DC gate bias voltage V_{gs} determines the conduction angle of the drain current. If the maximum linear input range is V_{GSM}, the gate bias voltage $V_{gs} = (V_{GSM} + V_{TH})/2$ corresponds to Class-A mode where the conduction angle of drain current is $360°$. For Class-A mode, the gate-source voltage is always larger than the transistor threshold voltage so that the drain current is always greater than zero. When the transistor is biased at $V_{gs} = V_{TH}$ corresponding to Class-B mode, the drain current conducts only in half of one period, and is zero for the rest of time. Thus the conduction angle of drain current is $180°$ for Class-B mode. When the transistor is biased between $(V_{GSM} + V_{TH})/2$ and V_{TH}, the conduction angle is between $180°$ and $360°$. This corresponds to Class-AB mode. For Class-C mode, the transistor is biased below V_{TH}. The conduction angle is less than $180°$. Fig.2.4 shows the V_{gs} and I_{ds} waveforms of Class-A, B, AB, and C. The linear power amplifiers have been comprehensively illustrated in many literatures. Here the important conclusions will be described.

From Class-A mode to Class-B mode, the conduction angle of drain current is reduced. The overlap of drain current and drain voltage is also reduced. This results in the increase in efficiency. For Class-A with optimum load, maximum efficiency of 50% can be achieved, while
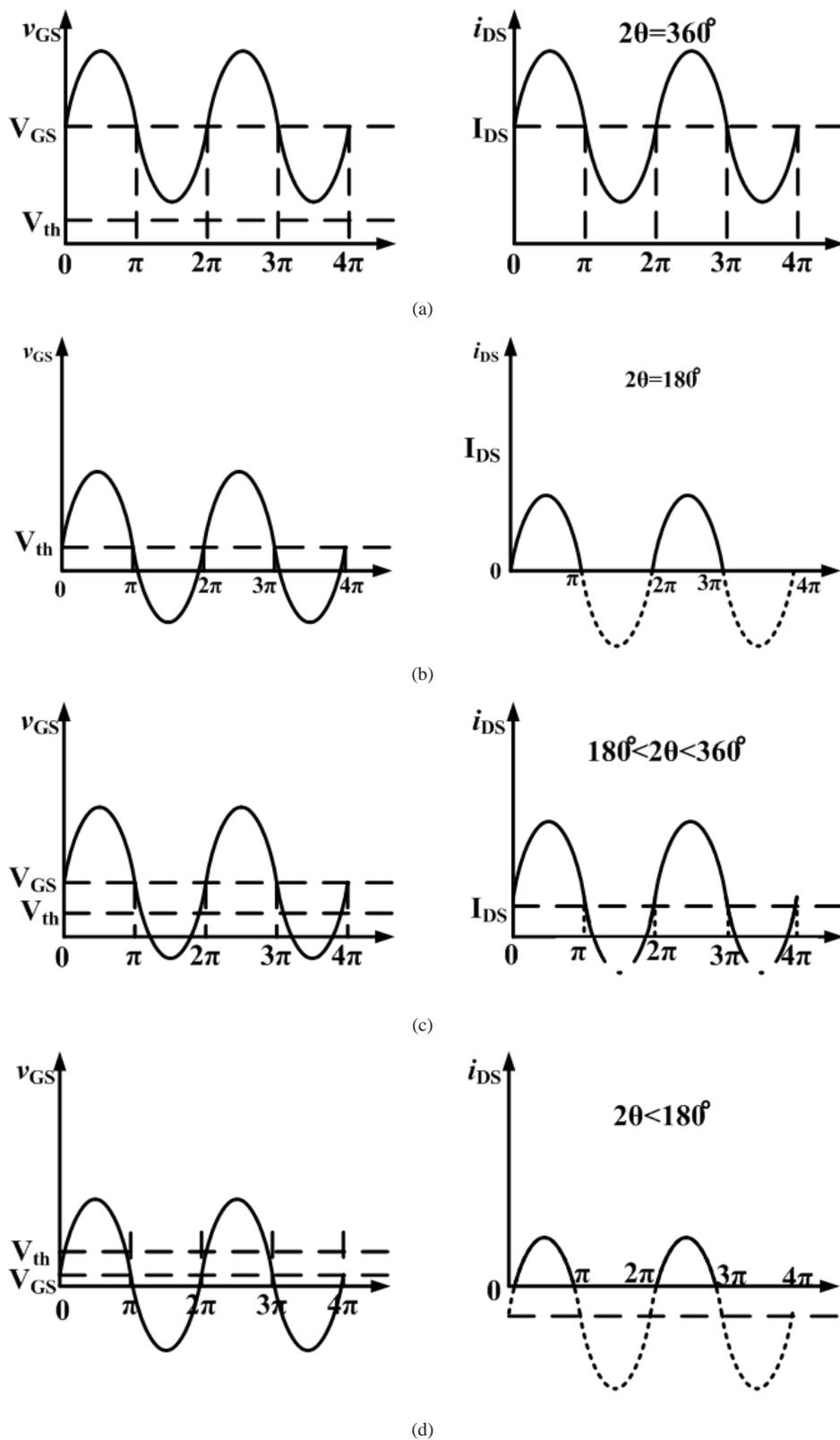
FIGURE 2.4: Waveforms of the gate-to-source voltage V_{gs}, and drain current I_{ds} of (a) Class A, (b) Class B, (c) Class AB, (d) Class C.
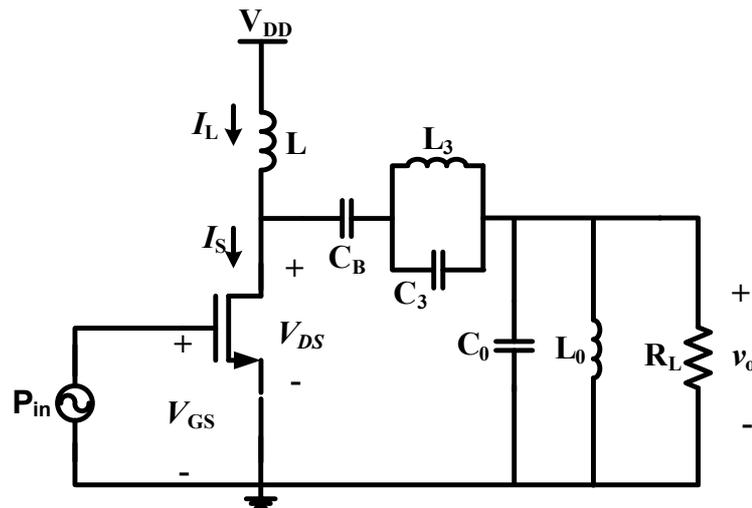
FIGURE 2.5: Class-F power amplifier

maximum efficiency of 78.5% can be achieved for Class-B. The maximum output power for Class-A and Class-B is the same, but if the conduction angle is continuously reduced, the output power will decrease. In addition, as the conduction angle decreases, the harmonic content of the output signal increases. Class-AB represents a compromise between efficiency and linearity.

Class-F is a special type of power amplifier. Class-F power amplifier has a load network which resonates at one or more harmonic frequencies in addition to the fundamental frequency[19]. The addition of harmonics to the fundamental shapes the drain voltage to become an approximate square wave rather than sine wave with a consequent improvement in both efficiency and output power. Fig. 2.5 shows the configuration of a Class-F amplifier with a third harmonic resonator. The transistor is biased at Class-B mode, thus the output current is a half sine wave. The resonator L_3 and C_3 resonates at $3f_0$, where f_0 is the fundamental frequency. Therefore the third harmonic component is presented at the drain terminal which in turn leads to a rectangular voltage waveform across the drain-to-source. The product of the rectangular drain voltage and half sine wave drain current is the power losses of the transistor. Since the power losses are minimum due to the shapes of the drain current and drain voltage, the efficiency is relatively high. The theoretical efficiency of a Class-F with third-harmonic resonator is 88.4%. The major advantage of Class-F PAs is given by the low peak voltage and rms current, that is very beneficial from the device stress point of view. However, although Class-F PAs feature a 100% efficiency in the ideal case, Class-F power amplifier requires the complex output networks to provide open and short circuits at the harmonic frequencies. Consequently, it is generally used in fixed-frequency applications at UHF and microwave frequencies.
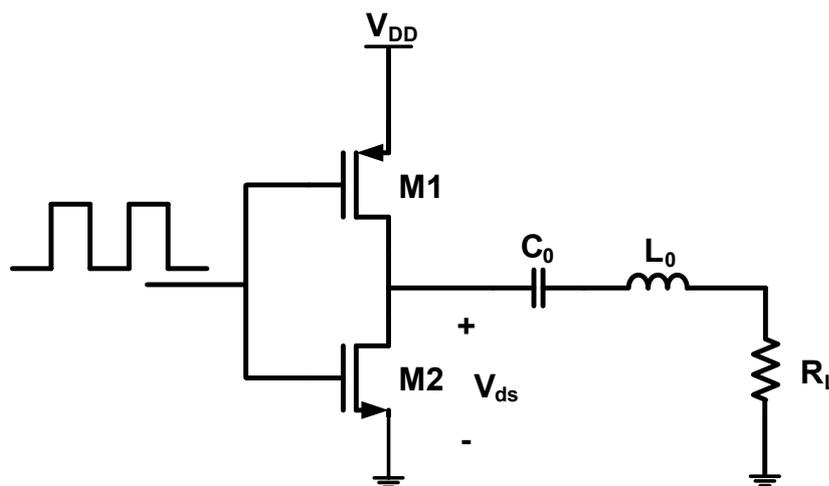
FIGURE 2.6: Class-D power amplifier

2.2.2   Switching Power Amplifier

Switch-mode operation (Classes D, E, and F) of power amplifiers achieves high efficiency by utilizing the power transistors as switches rather than linear amplifiers.

Class-D is an attractive power amplifier in low frequency. The schematic of a Class-D amplifier is shown in Fig.2.6. When M1 is turned on, M2 is turned off and vice versa. The output voltage across M2 alternates between the supply and ground that forms a square wave with a 50% duty cycle. The output load network L_0 and C_0 is tuned to the fundamental frequency to select the wanted component. The theoretical efficient of Class-D is 100% because there is no voltage across the switch when conducting and no current through them when off. No power dissipates on the switches and hence all the power is supplied to the load. However, charging and discharging of each drain capacitances once per RF cycle causes a Class-D power amplifier to become less efficient as frequency increases. Consequently, the use of Class-D is generally limited to low frequencies.

Class E power amplifier is a high-efficient amplifier used for RF applications. The basic circuit of a Class E amplifier is shown in Fig.2.7. The main idea of the Class E RF power amplifier is that the transistor turns on as a switch at zero voltage, resulting in zero switching loss and high efficiency. In fact, the parasitic capacitance of the switch can become part of C_1. In other words, the parasitic drain-source capacitance can become part of the amplifier circuit, which is a huge advantage, especially in CMOS. The combination of the dc-feed inductor L and the L-C-R series-resonant circuit acts as a current source whose current is $I_L - I_R$. When the switch is closed, the current $I_L - I_R$ flows through the switch. When the switch is opened, the current $I_L - I_R$ flows through the capacitor C_1, producing the voltage across the shunt capacitor C_1 and the switch. Therefore, the shunt capacitor C_1 shapes the voltage across the switch. For the
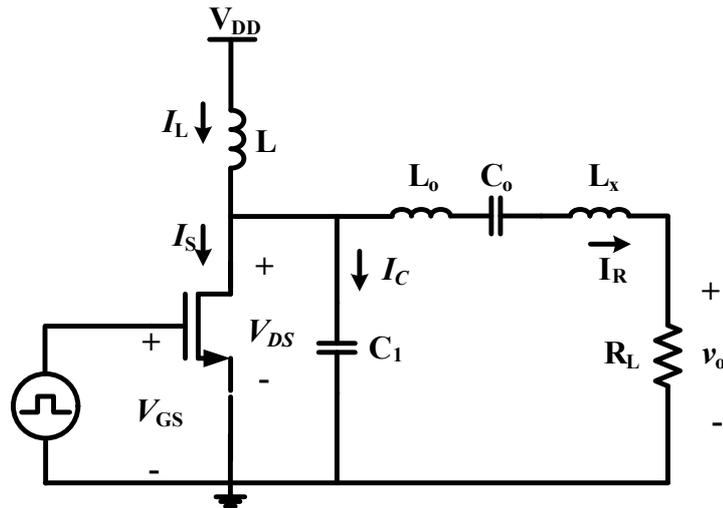
FIGURE 2.7: Class-E power amplifier

nominal or optimum operation, the zero voltage switching and zero slop switching conditions must be satisfied simultaneously:

$$V_{ds}(T) \ = \ 0 \tag{2.9}$$

$$\left.\frac{dV_{ds}(t)}{dt}\right|_{t=T} \ = \ 0 \tag{2.10}$$

Class-E power amplifier has two main advantages: a) soft switching which reduces the losses, and b) simple circuit topology compared to other switch-mode PA classes. However, Class-E power amplifier also has disadvantages: the drain voltage has a high peak value due to charging the large output capacitance. But the sub-optimum mode can be applied to reduce the peak drain voltage at the cost of drop in efficiency. To maintain high efficiency, using a high voltage breakdown device is a good option to design the Class-E power amplifier.

In summary, the gate bias voltage, input drive signal, and the output load network determines the class of operation of the power amplifier. For a given power amplifier, it can operate in any of the classical operating modes. For a small RF input signal, the amplifier works in Class-A, AB, B or C depending on the gate bias voltage. The efficiency can be improved by biasing the device near the threshold voltage but at the expense of higher harmonics. An alternative way to increase efficiency is to increase the input RF power so that the transistor works as a switch. But this leads to a non-linear amplifier in nature.

Chapter 3

Switch-Mode Class-E Power Amplifier Analytical Modeling

Since Sokal [21] published the literature on high-efficiency Class-E switch-mode tuned power amplifier, many analytical studies of this circuit have appeared. Early analyses assumed an ideal switch, an RF-choke in dc-feed network, an infinite loaded quality factor, and 50% switch duty-cycle. The effects of switch resistance [22][23][24][25], finite dc-feed inductance [22][26][27], finite loaded quality factor [22][26][28], and arbitrary switch duty-cycle [23][24][28] on the output power and efficiency were investigated later. However, none of the abovementioned techniques include all aspects of the Class-E circuits in one analysis. Recently a new analytical modeling method for Class-E PAs was presented by M. Acar [5][29][30][31] and D.A.C. Cortés[32]. This method is based upon design equations, that make it possible to design a Class-E PA by only specifying the supply voltage, frequency, process and output power of the PA. In the analysis, the switch resistance, finite dc-feed inductance, finite loaded quality factor, and arbitrary switch duty-cycle can be all taken into account. In this chapter, a general model covering optimum Class-E mode [33] and sub-optimum modes (variable voltage [29] and variable slope [30]) will be developed based on this new method. This general model combines all the Acar's and Cortés' work and also expands by the bandwidth characteristic of conventional Class-E topology. Furthermore, it will show the required load impedances at fundamental and harmonic frequencies. Based upon this model, the effects of the variations of load impedances on the performance of switch-mode Class-E power amplifier will be given.

3.1 Analytical Derivation of Class-E Power Amplifier Model

In this section, the detailed mathematical derivation of the Class-E power amplifier with infinite and finite loaded quality factors is presented.

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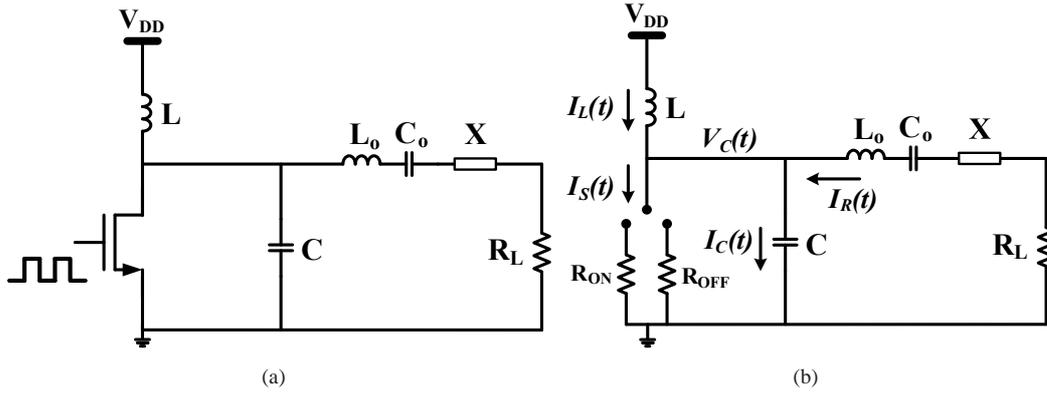
FIGURE 3.1: Class-E amplifier. (a)Basic circuit. (b)Equivalent circuit.

3.1.1   Circuit Description and Assumptions

The general Class-E PA is given in Fig. 3.1. It consists of an active device operated as a switch at the switching frequency f_0, a series R-L-C circuit, a dc-feed inductor L, and a shunt capacitor C, which may be partly or wholly made up of the parasitic shunt capacitance of the device. The combination of L_0 and C_0 forms a harmonic filter that is tuned to the switching frequency of the amplifier. The value of the load resistance R_L will mainly determine the output power level. The shunt capacitor C, dc-feed inductor L and excess reactance X will mainly determine the operation mode of Class-E amplifier.

The analytical derivation of the equations considers the following assumptions[5]:

1. The real power dissipation in the circuit only occurs on switch resistances (R_{ON} and R_{OFF}) and load resistance R_L.

2. The loaded quality factor Q_0 of the series resonant circuit (L_0 and C_0) is high enough in order for the output current I_R to be sinusoidal at the switching frequency.

3. In Fig. 3.2 the switching action of the active device is instantaneous. The switch is closed in the time interval $0 \leq t < d \cdot \pi/\omega$, whose resistance is R_{ON}. In the time interval $d \cdot \pi/\omega \leq t < 2\pi/\omega$ the switch is opened whose resistance is R_{OFF}. Note that the value of d determines the switch duty-cycle. For instance, $d = 1$ corresponds to conventional 50% switch duty-cycle.

Analyses of the sub-optimum operation, Variable-Slope (Class-E_{VS}) and Variable-Voltage (Class-E_{VV}) Class-E amplifiers, are presented in [29] and [30]. In these literatures, it has been shown that the variable-slope Class-E operation of finite dc-feed inductance allows using significantly larger switch size while the variable-voltage Class-E operation can obtain lower peak drain voltage feature. To analyze sub-optimum operation and conventional operation simultaneously, the Class-E conditions become
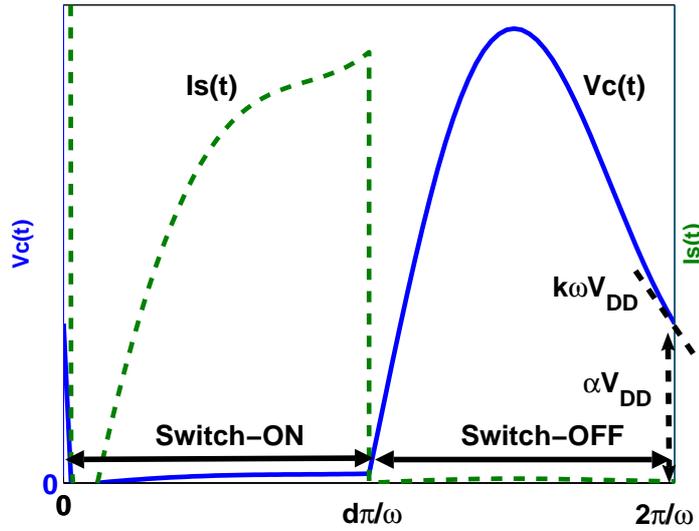
FIGURE 3.2: General drain voltage and current waveforms

$$V_C(\frac{2\pi}{\omega}) = \alpha V_{DD} \tag{3.1}$$

$$\frac{dV_C(t)}{dt}\bigg|_{t=2\pi/\omega} = \omega V_{DD} k \tag{3.2}$$

where αV_{DD} is the voltage of $V_C(t)$ at the moment the switch is closed; $\omega V_{DD} k$ is the slope of $V_C(t)$ at the moment the switch is closed. For conventional Class-E operation, $\alpha = 0$ and $k = 0$. For Variable-Voltage operation (Class-E$_{VV}$), $\alpha \neq 0$ and $k = 0$. For Variable-Slope operation (Class-E$_{VS}$), $k \neq 0$ and $\alpha = 0$. For $\alpha \neq 0$ or $k \neq 0$, it is also known as the sub-optimum operation [33]. α and k are real values that can be selected freely and therefore give degrees of freedom in the design Class-E PA.

The mathematical approach and the equations used to obtain the results given in this thesis are presented in following two sections. In Section 3.1.2 the equations of Class-E amplifier with infinite loaded quality factor will be derived [1]. For the case of finite loaded quality factor, the equations will be given in Section 3.1.3.

3.1.2 Derivation of Class-E Amplifier Equations with Infinite Loaded Quality Factor

Since the loaded quality factor of the output series resonant circuit (L_0 and C_0) is assumed to be infinite, the output current I_R is sinusoidal.

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[1]Section 3.1.2 refers to the work in [5][32].

$$I_R(t) = I_R \sin(\omega t + \phi) \tag{3.3}$$

In the time interval $0 \leq t < d \cdot \pi/\omega$, the switch is closed. Applying the Kirchhoff's current law (KCL) at the switch, we can get

$$I_{Son}(t) = I_{Lon}(t) + I_R(t) - I_{Con}(t), \tag{3.4}$$

where

$$I_{Son}(t) = \frac{V_{Con}(t)}{R_{ON}} \tag{3.5}$$

$$I_{Lon}(t) = \frac{1}{L} \int_0^t (V_{DD} - V_{Con}(\tau)) \, d\tau \tag{3.6}$$

$$I_{Con}(t) = C\frac{dV_{Con}(t)}{dt}. \tag{3.7}$$

Substituting Eqs.3.3, 3.5 - 3.7 into Eq.3.4 and taking derivative we get

$$\frac{d^2V_{Con}(t)}{dt^2} + \frac{1}{R_{ON}C}\frac{dV_{Con}(t)}{dt} - \frac{V_{DD} - V_{Con}(t)}{LC} - \frac{\omega I_R}{C}\cos(\omega t + \phi) = 0. \tag{3.8}$$

In the time interval $d \cdot \pi/\omega \leq t < 2\pi/\omega$, the switch is opened. The current $I_L(t)$ flowing through the dc-feeding inductor L can be written as

$$I_{Loff}(t) = \frac{1}{L} \int_{d\pi/\omega}^t (V_{DD} - V_{Coff}(\tau)) \, d\tau. \tag{3.9}$$

The current $I_S(t)$ flowing through the switch is

$$I_{Soff}(t) = \frac{V_{Coff}(t)}{R_{OFF}}. \tag{3.10}$$

The current $I_C(t)$ flowing through the capacitor C is

$$I_{Coff}(t) = C\frac{dV_{Coff}(t)}{dt}. \tag{3.11}$$

Substituting Eqs.3.3, 3.9 - 3.11 into Eq.3.4 and taking derivative we can get the differential equation when the switch is opened

$$\frac{d^2 V_{Coff}(t)}{dt^2} + \frac{1}{R_{OFF}C}\frac{dV_{Coff}(t)}{dt} - \frac{V_{DD} - V_{Coff}(t)}{LC} - \frac{\omega I_R}{C}\cos(\omega t + \phi) = 0. \tag{3.12}$$

The two differential equations 3.8 and 3.12 describe the Class-E amplifier in terms of independent component values. To relate these components, new parameters are defined:

$$m_{on} = \omega R_{ON} C \tag{3.13}$$

$$m_{off} = \omega R_{OFF} C \tag{3.14}$$

$$q = \frac{1}{\omega \sqrt{LC}} \tag{3.15}$$

$$p = \frac{\omega L I_R}{V_{DD}}. \tag{3.16}$$

With the parameters defined in 3.13 to 3.16 the differential equations 3.8 and 3.12 can be rewritten as:

$$\frac{d^2 V_{Con}(t)}{dt^2} + \frac{\omega}{m_{on}}\frac{dV_{Con}(t)}{dt} - q^2\omega^2(V_{DD} - V_{Con}(t)) - pq^2\omega^2 V_{DD}\cos(\omega t + \phi) = 0 \tag{3.17}$$

$$\frac{d^2 V_{Coff}(t)}{dt^2} + \frac{\omega}{m_{off}}\frac{dV_{Coff}(t)}{dt} - q^2\omega^2(V_{DD} - V_{Coff}(t)) - pq^2\omega^2 V_{DD}\cos(\omega t + \phi) = 0. \tag{3.18}$$

The equations of 3.17 and 3.18 are linear, nonhomogeneous, second-order differential equations. The their general solutions are given by:

$$\begin{aligned}
V_{Con}(t) &= Con1\, e^{1/2\frac{\left(-1+\sqrt{1-4q^2 m_{on}^2}\right)\omega t}{m_{on}}} + Con2\, e^{-1/2\frac{\left(1+\sqrt{1-4q^2 m_{on}^2}\right)\omega t}{m_{on}}} + V_{DD} + \\
&\quad \frac{V_{DD}pq^2 m_{on}\left(m_{on}\left(q^2-1\right)\cos\left(\omega t + \phi\right) + \sin\left(\omega t + \phi\right)\right)}{1 + \left(q^4 - 2q^2 + 1\right)m_{on}^2}
\end{aligned} \tag{3.19}$$

$$
\begin{aligned}
V_{Coff}(t) \;=\;& Coff1\, e^{1/2 \frac{\left(-1+\sqrt{1-4\,q^2 moff^2}\right)\omega t}{moff}} + Coff2\, e^{-1/2 \frac{\left(1+\sqrt{1-4\,q^2 moff^2}\right)\omega t}{moff}} + V_{DD} + \\
& \frac{V_{DD}p\,q^2 m_{off}\,\left(moff\,\left(q^2-1\right)\cos\left(\omega t+\phi\right)+\sin\left(\omega t+\phi\right)\right)}{1+\left(q^4-2\,q^2+1\right)moff^2}
\end{aligned}
\tag{3.20}
$$

As can be seen in 3.19 and 3.20 for each solution there are two unknown constants $Con1$, $Con2$ or $Coff1$, $Coff2$. These constants can be solved by using boundary conditions. When these constants are solved, the Class-E model will be described without the explicit component values. The properties of the Class-E amplifier (i.e. drain efficiency, output power, waveforms, ects) will be obtained without specifying any component value. This is one of advantages of this analytical modeling.

The coefficients $Con1$ and $Con2$ in Eq.3.19 can be solved from the continuity of the capacitor charge and inductor flux at $t = 0$,

$$
C \cdot V_{Con}(t)\big|_{t=0} = C \cdot V_{Coff}(t)\big|_{t=2\pi/\omega}
\tag{3.21}
$$

$$
L \cdot I_{Lon}(t)\big|_{t=0} = L \cdot I_{Loff}(t)\big|_{t=2\pi/\omega}
\tag{3.22}
$$

Substituting the Class-E condition 3.1 into capacitor C charge continuity equation 3.21 yields

$$
V_{Con}(t)\big|_{t=0} = \alpha V_{DD}
\tag{3.23}
$$

The inductor L flux continuity equation 3.22 can be simplified by substituting the equations 3.3 - 3.7, 3.10 - 3.11, and Class-E conditions 3.1 - 3.2 into the equation. It yields

$$
\frac{dV_{Con}(t)}{dt}\bigg|_{t=0} = \omega V_{DD}k + \frac{\alpha V_{DD}\omega}{m_{off}} - \frac{\alpha V_{DD}\omega}{m_{on}}
\tag{3.24}
$$

By solving the above two equations, given by 3.23 and 3.24, the coefficients $Con1$ and $Con2$ can be found in terms of q, d, α, k, m_{on}, m_{off}, V_{DD}, ω, p, and ϕ. Therefore, the expression of switch voltage $V_{Con}(t)$ in 3.19 can be also described by these parameters.

Similarly, the coefficients $Coff1$ and $Coff2$ in Eq.3.20 can be solved from the Class-E conditions at $t = 2\pi/\omega$,

$$
V_{Coff}(\frac{2\pi}{\omega}) = \alpha V_{DD}
\tag{3.25}
$$

$$\frac{dV_{Coff}(t)}{dt}\bigg|_{t=2\pi/\omega} = \omega V_{DD}k. \tag{3.26}$$

Hence, the coefficients $Coff1$ and $Coff2$ can be found in terms of q, d, α, k, m_{on}, m_{off}, ω, V_{DD}, p, and ϕ. The expression of switch voltage $V_{Coff}(t)$ in Eq.3.20 can be also described by these parameters.

So far, the switch voltages, $V_{Con}(t)$ and $V_{Coff}(t)$, have been determined in terms of q, d, α, k, m_{on}, m_{off}, ω, V_{DD}, p, and ϕ. The supply voltage V_{DD}, the operating angular frequency ω , the technology-frequency related parameters m_{on} and m_{off} are assumed to be known a priori. The duty-cycle d, the variable-voltage parameter α, the variable-slope parameter k, and the normalized resonant frequency q have the physical meanings and could be set for the specific behavior. The initial phase ϕ and the parameter p are intermediate variables, and will be expressed as a function of the other parameters by using the continuity of the capacitor charge and inductor flux at $t = d\pi/\omega$,

$$C \cdot V_{Con}(t)|_{t=d\pi/\omega} = C \cdot V_{Coff}(t)|_{t=d\pi/\omega} \tag{3.27}$$

$$L \cdot I_{Lon}(t)|_{t=d\pi/\omega} = L \cdot I_{Loff}(t)|_{t=d\pi/\omega}. \tag{3.28}$$

All calculations of above equations are done by MAPLE. The detailed codes is presented in Appendix.

To this point, the obtained analytical solutions for switch voltages are only related to the parameters of q, d, α, k, m_{on}, m_{off}, ω, and V_{DD}. Infinite solutions are existing due to the freedom in the values of dc-feed inductor, the switch duty-cycle, the variable-voltage and variable-slope. For every real value of these parameters there is a solution for switch voltage.

The analytical solution and the circuit component values of Class-E model are related by the design set K [5]. The elements of design set K are defined as:

$$K_L = \frac{\omega L}{R_L} \tag{3.29}$$

$$K_C = \omega C R_L \tag{3.30}$$

$$K_P = \frac{P_{OUT}R_L}{V_{DD}^2} \tag{3.31}$$

$$K_X = \frac{X}{R_L} \tag{3.32}$$

The expression of K_L can be derived by using the principle of power conservation,

$$P_{OUT} + P_{switch} = P_{DC}, \tag{3.33}$$

where P_{OUT} is the output power delivered to the load R_L; P_{switch} is the power loss in the switch; P_{DC} is the power from the DC-supply.

The output power P_{OUT} is equivalent to

$$P_{OUT} = \frac{I_R^2 R_L}{2}. \tag{3.34}$$

The power loss in the switch P_{switch} is equivalent to

$$P_{switch} = \frac{\omega}{2\pi} \left(\int_0^{d\pi/\omega} \frac{V_{Con}^2(t)}{R_{ON}} dt + \int_{d\pi/\omega}^{2\pi/\omega} \frac{V_{Coff}^2(t)}{R_{OFF}} dt \right). \tag{3.35}$$

The DC-supply power P_{DC} is equivalent to

$$
\begin{aligned}
P_{DC} &= V_{DD} I_0 \tag{3.36} \\
&= V_{DD} \frac{\omega}{2\pi} \left(\int_0^{d\pi/\omega} \frac{V_{Con}(t)}{R_{ON}} dt + \int_{d\pi/\omega}^{2\pi/\omega} \frac{V_{Coff}(t)}{R_{OFF}} dt \right). \tag{3.37}
\end{aligned}
$$

From the Eqs.3.34 - 3.37 the K_L can be expressed as

$$
\begin{aligned}
K_L &= \frac{\omega L}{R_L} \\
&= \frac{p^2 V_{DD}^2}{2\omega L P_{OUT}} \\
&= \frac{p^2 V_{DD}^2}{2\omega L (P_{DC} - P_{switch})} \\
&= \frac{p^2 V_{DD}^2 q^2 \pi}{\omega \left(\int_0^{d\pi/\omega} \frac{V_{Con}(t)V_{DD} - V_{Con}^2(t)}{m_{on}} dt + \int_{d\pi/\omega}^{2\pi/\omega} \frac{V_{Coff}(t)V_{DD} - V_{Coff}^2(t)}{m_{off}} dt \right)}. \tag{3.38}
\end{aligned}
$$

The K_C and K_P can be expressed as function of K_L. This is,

$$K_C = \omega C R_L = \frac{1}{q^2 K_L} \tag{3.39}$$

$$K_P = \frac{P_{OUT} R_L}{V_{DD}^2} = \frac{p^2}{2 K_L^2} \tag{3.40}$$

The K_X can be found by using the two fundamental quadrature Fourier components of $V_C(t)$

$$
V_R = \frac{1}{\pi}\left(\int_0^{d\pi/\omega} V_{Con}(t)\sin(\omega t + \phi)\,dt + \int_{d\pi/\omega}^{2\pi/\omega} V_{Coff}(t)\sin(\omega t + \phi)\,dt \right) \tag{3.41}
$$

$$
V_X = \frac{1}{\pi}\left(\int_0^{d\pi/\omega} V_{Con}(t)\cos(\omega t + \phi)\,dt + \int_{d\pi/\omega}^{2\pi/\omega} V_{Coff}(t)\cos(\omega t + \phi)\,dt \right) \tag{3.42}
$$

$$
K_X = \frac{V_X}{V_R}. \tag{3.43}
$$

The drain efficiency η can be expressed as

$$
\begin{aligned}
\eta &= 1 - \frac{P_{switch}}{P_{DC}} \\
&= 1 - \frac{\int_0^{d\pi/\omega} \frac{V_{Con}^2(t)}{m_{on}}\,dt + \int_{d\pi/\omega}^{2\pi/\omega} \frac{V_{Coff}^2(t)}{m_{off}}\,dt}{\int_0^{d\pi/\omega} \frac{V_{Con}(t)V_{DD}}{m_{on}}\,dt + \int_{d\pi/\omega}^{2\pi/\omega} \frac{V_{Coff}(t)V_{DD}}{m_{off}}\,dt}
\end{aligned} \tag{3.44}
$$

Since p and ϕ both are functions of $q, d, \alpha, k, m_{on}, m_{off}, \omega$, and V_{DD}, K_L, K_C, K_P, K_X and η are functions of $q, d, \alpha, k, m_{on}, m_{off}, \omega$, and V_{DD}.

3.1.3 Derivation of Class-E Amplifier Equations with Finite Loaded Quality Factor

In Section 3.1.2, the loaded quality factor Q_0 of output series resonant circuit L_0 and C_0 in Fig. 3.1 is assumed to be infinite. Only fundamental current is flowing through the load resistor. In this section, the analytical solution in the previous section is extended to cover the effect of the finite loaded quality factor as well. An extended model has been developed to allow more accurate prediction of effects of the finite loaded quality factor. The purpose of this section is to derive the analytical solutions of the Class-E amplifier at any Q_0. The circuit for this derivation is shown in Fig. 3.3. The excess reactance X in Fig. 3.1 has already been absorbed into L_1 or C_1. If the K_X solved by the Eq.3.38 is larger than zero, the X shows inductive reactance. It will be absorbed into the inductor L_1. For this case ($K_X \geq 0$), the loaded quality factor is defined as

$$
Q_L = \frac{\omega L_1}{R_L} = \frac{\omega(L_0 + L_X)}{R_L} = Q_0 + K_X \tag{3.45}
$$
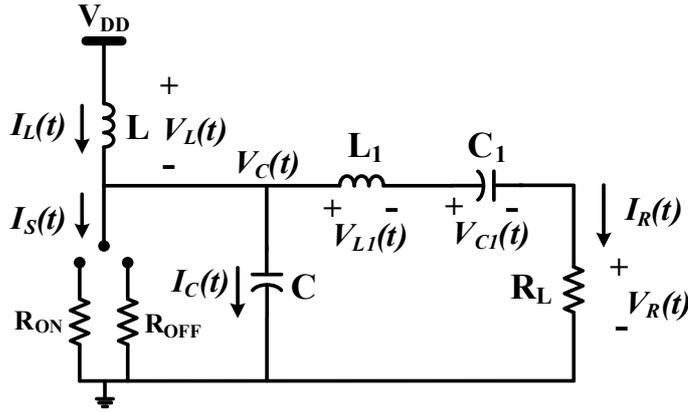
FIGURE 3.3: Class-E amplifier with finite loaded quality factor

$$Q_C = \frac{1}{\omega C_1 R_L} = \frac{1}{\omega C_0 R_L} = Q_0 \tag{3.46}$$

where Q_0 is a finite loaded quality factor of L_0 or C_0. If the K_X is smaller than zero, the X shows capacitive reactance. It will be absorbed into the capacitor C_1. For this case ($K_X < 0$), the loaded quality factor is

$$Q_L = \frac{\omega L_1}{R_L} = \frac{\omega L_0}{R_L} = Q_0 \tag{3.47}$$

$$Q_C = \frac{1}{\omega C_1 R_L} = \frac{1}{\omega (C_0 + C_X) R_L} = Q_0 - K_X \tag{3.48}$$

Applying the Kirchhoff's voltage law (KVL) at the switch, we can get

$$V_{DD} = V_L(t) + V_C(t) = V_L(t) + (V_{L1}(t) + V_{C1}(t) + V_R(t)). \tag{3.49}$$

Applying the KCL at the switch, we can get

$$I_L(t) = I_S(t) + I_C(t) + I_R(t). \tag{3.50}$$

In the following derivation, the currents and voltages will all be expressed in terms of $V_{C1}(t)$ in order to solve the Eqs.3.49 and 3.50.

The current $I_R(t)$ flowing through the capacitor C_1 is equal to

$$I_R(t) = \frac{dQ_{C1}(t)}{dt} = C_1 \frac{dV_{C1}(t)}{dt}. \tag{3.51}$$

The voltage $V_{L1}(t)$ across the output inductor L_1 is equal to

$$V_{L1}(t) = L_1 \frac{dI_R(t)}{dt} = L_1 C_1 \frac{d^2 V_{C1}(t)}{dt^2}. \tag{3.52}$$

The voltage $V_R(t)$ across the output resistor R_L is equal to

$$V_R(t) = I_R(t) R_L = C_1 R_L \frac{dV_{C1}(t)}{dt}. \tag{3.53}$$

Therefore the switch voltage $V_C(t)$ can be expressed as the summation of $V_{L1}(t)$, V_{C1} and $V_R(t)$,

$$
\begin{aligned}
V_C(t) &= V_{L1}(t) + V_{C1}(t) + V_R(t) \\
&= L_1 C_1 \frac{d^2 V_{C1}(t)}{dt^2} + V_{C1}(t) + C_1 R_L \frac{dV_{C1}(t)}{dt}.
\end{aligned} \tag{3.54}
$$

The current $I_C(t)$ passing through the capacitor C can be found by taking derivative of $V_C(t)$ in Eq.3.54,

$$
\begin{aligned}
I_C(t) &= C \frac{dV_C(t)}{dt} \\
&= C L_1 C_1 \frac{d^3 V_{C1}(t)}{dt^3} + C \frac{dV_{C1}(t)}{dt} + C C_1 R_L \frac{d^2 V_{C1}(t)}{dt^2}.
\end{aligned} \tag{3.55}
$$

The current $I_S(t)$ flowing through the switch resistance[2] R_S

$$
\begin{aligned}
I_S(t) &= \frac{V_C(t)}{R_S} \\
&= \frac{1}{R_S} (L_1 C_1 \frac{d^2 V_{C1}(t)}{dt^2} + V_{C1}(t) + C_1 R_L \frac{dV_{C1}(t)}{dt}).
\end{aligned} \tag{3.56}
$$

Summation of $I_R(t)$, $I_C(t)$ and $I_S(t)$ will result in

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[2]We use R_S to replace the R_{ON} or R_{OFF} in derivation at the beginning. For different time interval, the R_S will be replaced by corresponding switch resistance.

$$
\begin{aligned}
I_L(t) &= I_R(t) + I_C(t) + I_S(t) \\
&= CL_1C_1\frac{d^3V_{C1}(t)}{dt^3} + (\frac{L_1C_1 + CC_1R_LR_S}{R_S})\frac{d^2V_{C1}(t)}{dt^2} \\
&\quad + (C + C_1 + \frac{C_1R_L}{R_S})\frac{dV_{C1}(t)}{dt} + \frac{V_{C1}(t)}{R_S}.
\end{aligned}
\tag{3.57}
$$

Therefore the voltage $V_L(t)$ across dc-feed inductor L can be expressed as,

$$
\begin{aligned}
V_L(t) &= L\frac{dI_L(t)}{dt} \\
&= LCL_1C_1\frac{d^4V_{C1}(t)}{dt^4} + (\frac{LL_1C_1 + LCC_1R_LR_S}{R_S})\frac{d^3V_{C1}(t)}{dt^3} \\
&\quad + (LC + LC_1 + \frac{LC_1R_L}{R_S})\frac{d^2V_{C1}(t)}{dt^2} + \frac{L}{R_S}\frac{dV_{C1}(t)}{dt}.
\end{aligned}
\tag{3.58}
$$

Substituting Eqs.3.52-3.54 and Eq.3.58 into Eq.3.49, we can get a linear, nonhomogeneous, forth-order differential equation. That is,

$$
\begin{aligned}
&LCL_1C_1\frac{d^4V_{C1}(t)}{dt^4} + (\frac{LL_1C_1 + LCC_1R_LR_S}{R_S})\frac{d^3V_{C1}(t)}{dt^3} + \\
&(\frac{RC_1L}{R_S} + LC + LC_1 + L_1C_1)\frac{d^2V_{C1}(t)}{dt^2} + \\
&(RC_1 + \frac{L}{R_S})\frac{dV_{C1}(t)}{dt} + V_{C1}(t) - V_{DD} = 0
\end{aligned}
\tag{3.59}
$$

Eq.3.59 only contains one node voltage variable $V_{C1}(t)$. Once the solution of $V_{C1}(t)$ is obtained, all other voltages and currents will be known. To solve the equation, the parameters defined in Eqs.3.13 - 3.15, Eqs.3.29 - 3.32, and Eqs.3.45 - 3.46 will be used again. For the readers' convenience, we re-write the definitions.

$$q \quad = \quad \frac{1}{\omega \sqrt{LC}} \tag{3.60}$$

$$m_{on} \quad = \quad \omega R_{ON} C \tag{3.61}$$

$$m_{off} \quad = \quad \omega R_{OFF} C \tag{3.62}$$

$$K_L \quad = \quad \frac{\omega L}{R_L} \tag{3.63}$$

$$K_C \quad = \quad \omega C R_L \tag{3.64}$$

$$K_P \quad = \quad \frac{P_{OUT} R_L}{V_{DD}^2} \tag{3.65}$$

$$K_X \quad = \quad \frac{X}{R_L} \tag{3.66}$$

$$Q_L \quad = \quad \frac{\omega L_1}{R_L} \tag{3.67}$$

$$Q_C \quad = \quad \frac{1}{\omega C_1 R_L} \tag{3.68}$$

The following two equations will also be used in the derivation:

$$\frac{R_{ON}}{R_L} \quad = \quad \frac{m_{on}}{K_C} \tag{3.69}$$

$$\frac{R_{OFF}}{R_L} \quad = \quad \frac{m_{off}}{K_C} \tag{3.70}$$

In the time interval $0 \le t < d \cdot \pi/\omega$, the switch is closed. The switch resistance R_S in Eq.3.59 corresponds to R_{ON}. Substituting the above equations into Eq.3.59 and re-arranging the equation results in,

$$
\begin{aligned}
&(\frac{Q_L}{Q_C} \frac{1}{q^2 \omega^4}) \frac{d^4 V_{C1_{on}}(t)}{dt^4} + (\frac{Q_L}{Q_C} \frac{1}{q^2 \omega^3 m_{on}} + \frac{1}{Q_C q^2 \omega^3}) \frac{d^3 V_{C1_{on}}(t)}{dt^3} + \\
&(\frac{1}{Q_C q^2 \omega^2 m_{on}} + \frac{1}{q^2 \omega^2} + \frac{1}{Q_C q^2 \omega^2 K_C} + \frac{Q_L}{Q_C \omega^2}) \frac{d^2 V_{C1_{on}}(t)}{dt^2} + \\
&(\frac{1}{Q_C \omega} + \frac{1}{q^2 \omega m_{on}}) \frac{d V_{C1_{on}}(t)}{dt} + V_{C1_{on}}(t) - V_{DD} = 0
\end{aligned}
\tag{3.71}
$$

Similarly, in the time interval $d \cdot \pi/\omega \le t < 2\pi/\omega$ the switch resistance R_S corresponds to R_{OFF}. Eq.3.59 can be re-written as,

$$\left(\frac{Q_L}{Q_C}\frac{1}{q^2\omega^4}\right)\frac{d^4 V_{C1_{off}}(t)}{dt^4} + \left(\frac{Q_L}{Q_C}\frac{1}{q^2\omega^3 m_{off}} + \frac{1}{Q_C q^2\omega^3}\right)\frac{d^3 V_{C1_{off}}(t)}{dt^3} +$$

$$\left(\frac{1}{Q_C q^2\omega^2 m_{off}} + \frac{1}{q^2\omega^2} + \frac{1}{Q_C q^2\omega^2 K_C} + \frac{Q_L}{Q_C\omega^2}\right)\frac{d^2 V_{C1_{off}}(t)}{dt^2} +$$

$$\left(\frac{1}{Q_C\omega} + \frac{1}{q^2\omega m_{off}}\right)\frac{d V_{C1_{off}}(t)}{dt} + V_{C1_{off}}(t) - V_{DD} = 0 \tag{3.72}$$

Here we use $V_{C1_{on}}(t)$ and $V_{C1_{off}}(t)$ to denote the different time intervals. To make the derivation clear and simple, we will define new symbols to replace the coefficients of above two differential equations. They are

$$sa_1 = \frac{Q_L}{Q_C}\frac{1}{q^2\omega^4} \tag{3.73}$$

$$sb_1 = \frac{Q_L}{Q_C}\frac{1}{q^2\omega^3 m_{on}} + \frac{1}{Q_C q^2\omega^3} \tag{3.74}$$

$$sc_1 = \frac{1}{Q_C q^2\omega^2 m_{on}} + \frac{1}{q^2\omega^2} + \frac{1}{Q_C q^2\omega^2 K_C} + \frac{Q_L}{Q_C\omega^2} \tag{3.75}$$

$$sd_1 = \frac{1}{Q_C\omega} + \frac{1}{q^2\omega m_{on}} \tag{3.76}$$

$$se_1 = 1 \tag{3.77}$$

$$sf_1 = -V_{DD} \tag{3.78}$$

$$sa_2 = \frac{Q_L}{Q_C}\frac{1}{q^2\omega^4} \tag{3.79}$$

$$sb_2 = \frac{Q_L}{Q_C}\frac{1}{q^2\omega^3 m_{off}} + \frac{1}{Q_C q^2\omega^3} \tag{3.80}$$

$$sc_2 = \frac{1}{Q_C q^2\omega^2 m_{off}} + \frac{1}{q^2\omega^2} + \frac{1}{Q_C q^2\omega^2 K_C} + \frac{Q_L}{Q_C\omega^2} \tag{3.81}$$

$$sd_2 = \frac{1}{Q_C\omega} + \frac{1}{q^2\omega m_{off}} \tag{3.82}$$

$$se_2 = 1 \tag{3.83}$$

$$sf_2 = -V_{DD} \tag{3.84}$$

then the Eqs.3.71 and 3.72 become

$$sa_1\frac{d^4V_{C1_{on}}(t)}{dt^4} + sb_1\frac{d^3V_{C1_{on}}(t)}{dt^3} + sc_1\frac{d^2V_{C1_{on}}(t)}{dt^2} +$$
$$sd_1\frac{dV_{C1_{on}}(t)}{dt} + se_1V_{C1_{on}}(t) + sf_1 = 0 \qquad (3.85)$$

$$sa_2\frac{d^4V_{C1_{off}}(t)}{dt^4} + sb_2\frac{d^3V_{C1_{off}}(t)}{dt^3} + sc_2\frac{d^2V_{C1_{off}}(t)}{dt^2} +$$
$$sd_2\frac{dV_{C1_{off}}(t)}{dt} + se_2V_{C1_{off}}(t) + sf2 = 0 \qquad (3.86)$$

The general solutions of Eqs.3.85 and 3.86 are

$$V_{C1_{on}}(t) = a_1e^{Ca_1t} + b_1e^{Cb_1t} + c_1e^{Cc_1t} + d_1e^{Cd_1t} - sf_1/se_1 \qquad (3.87)$$

$$V_{C1_{off}}(t) = a_2e^{Ca_2t} + b_2e^{Cb_2t} + c_2e^{Cc_2t} + d_2e^{Cd_2t} - sf_2/se_2 \qquad (3.88)$$

where the Ca_1, Cb_1, Cc_1, Cd_1 are the roots of $sa_1x^4 + sb_1x^3 + sc_1x^2 + sd_1x + se_1 = 0$ while the Ca_2, Cb_2, Cc_2, Cd_2 are the roots of $sa_2x^4 + sb_2x^3 + sc_2x^2 + sd_2x + se_2 = 0$. To find out the expressions of eight unknowns coefficients (i.e. a_1, b_1, c_1, d_1, a_2, b_2, c_2, d_2), the continuity of capacitor charge and inductor flux will be applied to capacitors C, C_1 and inductor L, L_1.

$$CV_C(t)|_{t=0} = CV_C(t)|_{t=2\pi/\omega} \qquad (3.89)$$

$$CV_C(t)|_{t=d\pi/\omega^-} = CV_C(t)|_{t=d\pi/\omega^+} \qquad (3.90)$$

$$C_1V_{C1}(t)|_{t=0} = C_1V_{C1}(t)|_{t=2\pi/\omega} \qquad (3.91)$$

$$C_1V_{C1}(t)|_{t=d\pi/\omega^-} = C_1V_{C1}(t)|_{t=d\pi/\omega^+} \qquad (3.92)$$

$$LV_L(t)|_{t=0} = LV_L(t)|_{t=2\pi/\omega} \qquad (3.93)$$

$$LV_L(t)|_{t=d\pi/\omega^-} = LV_L(t)|_{t=d\pi/\omega^+} \qquad (3.94)$$

$$L_1V_{L1}(t)|_{t=0} = L_1V_{L1}(t)|_{t=2\pi/\omega} \qquad (3.95)$$

$$L_1V_{L1}(t)|_{t=d\pi/\omega^-} = L_1V_{L1}(t)|_{t=d\pi/\omega^+} \qquad (3.96)$$

By solving the above eight boundary conditions, the coefficients in Eqs.3.87 and 3.88 can be expressed in terms of parameters defined in Eqs.3.60-3.68. Therefore the capacitor voltage $V_{C1}(t)$ is obtained and given in the terms of q, d, α, k, m_{on}, m_{off}, V_{DD}, ω, Q_0. The rest of voltages and currents are also determined.

The analytical expressions for the voltages and currents in Fig. 3.3 are very complex but can be computed numerically. The purpose of the derivations in Sections 3.1.2 and 3.1.3 is to present
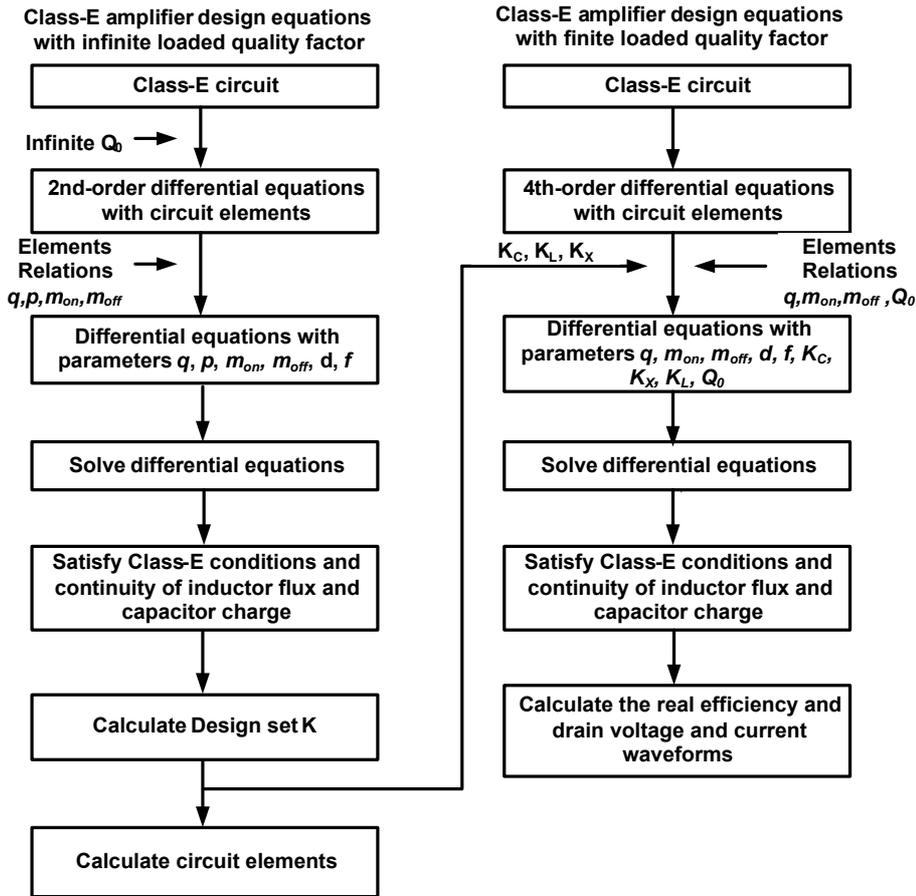
FIGURE 3.4: Analytical design flowchart of Class-E power amplifier at a single frequency.

the approach we used to model the Class-E amplifier. All those equations can be calculated by MAPLE.

Fig.3.4 summarizes the analytical approach of systematical design of Class-E power amplifier. The starting point is to express the ideal Class-E circuit (infinite loaded quality factor) as time-domain 2nd-order differential equations in terms of circuit elements, then the higher level differential equations will be generated based upon the elements relations. After solving the 2nd-order differential equations by applying the boundary conditions and Class-E circuit conditions, the design set K can be obtained. If the actual loaded quality factor is given, the more realistic solutions of the Class-E amplifier can be found by solving 4th-order differential equations for the given quality factor and obtained design set K.

For the obtained design set K, the relations between the circuit elements and design set K can be expressed in Fig.3.5. Each circuit element is placed in the corners of a triangle and the related design set element is shown in the inner part of the triangle [5]. In the triangles for K_C, K_L, K_X two elements are shared by the other triangles, whereas in K_P only one element R_L is shared. Therefore, either V_{DD} or P_{OUT} must be known in order to be able to make a uniquely defined Class-E PA design. Fig.3.6 shows two procedures to calculate the circuit elements. For a given
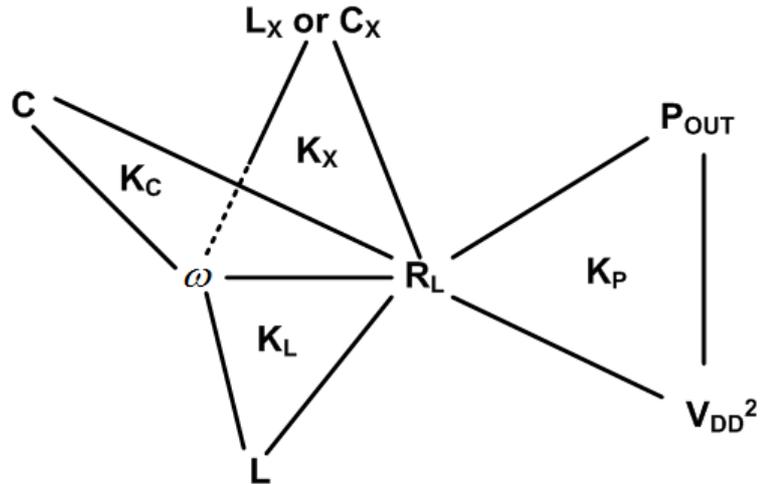
FIGURE 3.5: Relations between the elements of the design set K
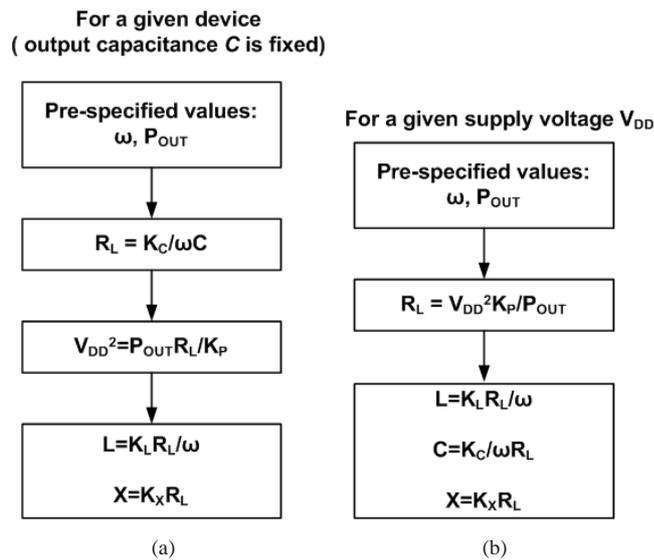
FIGURE 3.6: Class-E amplifier components design:(a) for a given device, (b) for a given supply voltage

device, the device output capacitance C is fixed so that the load resistance R_L can be found from K_C, then the supply voltage will be known via K_P. The dc-feed inductor L and excess reactance X can be obtained from K_L and K_X. It is similar to the case of given supply voltage.

3.2 Analysis and Discussion of Class-E Power Amplifier Model

In Sections 3.1.2 and 3.1.3, the analytical approach is applied to model the Class-E power amplifiers. In this section, the validity of the analytical approach will be presented by an example. After that, the effects of variations of drain load impedances on the performance of Class-E power amplifiers will be discussed comprehensively.

TABLE 3.1: Input parameters for analytical model

$\omega = 1$	$m_{on} = 0.01$	$m_{off} = 1000$
$q = 1.412$	$d = 1$	$V_{DD} = 1$
$\alpha = 0$	$k = 0$	$Q_0 = 2$

TABLE 3.2: Results of analytical model and ADS based upon the parameters in Table3.1

$K_L = 0.725$	$K_C = 0.692$	$K_P = 1.27$	$K_X = 0.0186$
$\eta\|_{Q_0=\infty} = 95.43\%$	$\eta\|_{ADS(Q_0=\infty)} = 95.40\%$	$\eta\|_{Q_0=2} = 91.94\%$	$\eta\|_{ADS(Q_0=2)} = 91.80\%$

(a) Drain voltage Vds(t)

(b) Drain current Is(t)
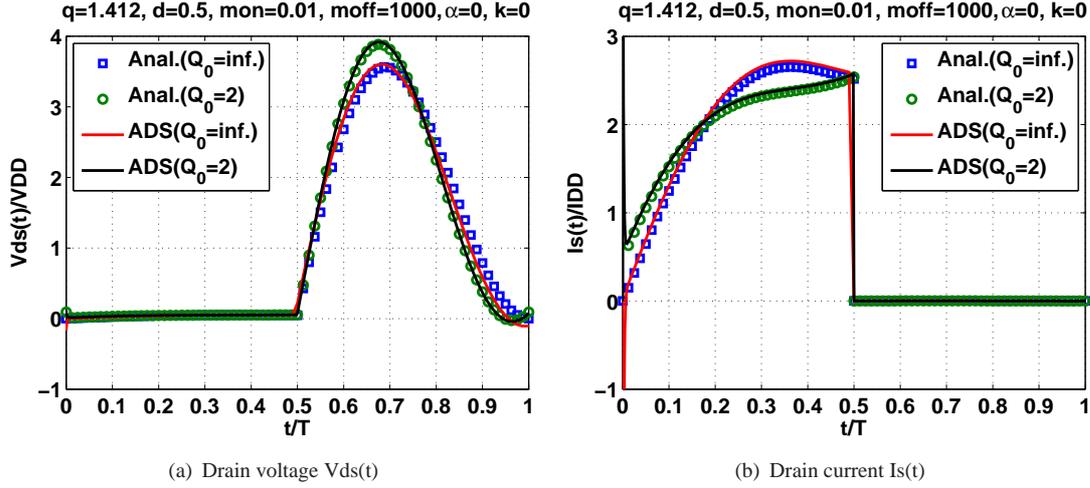
FIGURE 3.7: Class-E amplifier waveforms for analytical approach and ADS simulation

3.2.1 Accuracy Comparison between Analytical Approach and ADS Solution

In this section, an example is presented to compare the accuracy of the analytical approach with commercial circuit simulator (ADS). For analytical design equations, we assume that the amplifier operates at maximum output power mode[3] ($q = 1.412$) with zero switching voltage ($\alpha = 0$) and zero switching slope ($k = 0$). To simplify the computation, we choose $V_{DD} = 1$, 50% duty-cycle ($d = 1$), $\omega = 1$, and device technology parameters $m_{on} = 0.01$ and $m_{off} = 1000$. By substituting these input parameters summarized in Table 3.1 into the design equations shown in Section 3.1.2, we can get the ideal drain efficiency, design set K, and ideal drain current and voltage waveforms. Substituting the obtained design set K and finite quality factor $Q_0 = 2$ into the design equations shown in Section 3.1.3, the real drain efficiency and drain voltage and current waveforms can be obtained. Table3.2 shows the design set K, and drain efficiency calculated by analytical approach for $Q_0 = 2$ and $Q_0 = \infty$. The drain current and voltage waveforms are shown in Fig.3.7.

To verify the correctness of the analytical solutions, a Class-E circuit shown in Fig. 3.8 is built up in the ADS. Assuming the operating frequency f_0 is 1GHz, the supply voltage V_{DD} is 1V, and

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[3]In [5], the author has proved that the maximum output power is obtained when $q = 1.412$ for given R and V_{DD}.
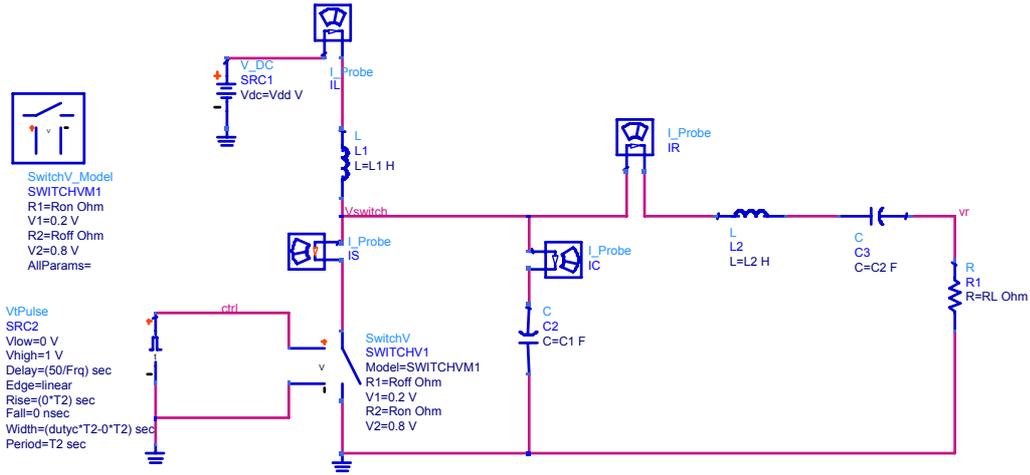
FIGURE 3.8: Class-E model in ADS

TABLE 3.3: Component Values at 1GHz

$Q_0 = 2$	$Q_0 = 100$
$L = \frac{K_L R_L}{\omega} = 0.1154nH$	
$C = \frac{K_C}{\omega R_L} = 110.14pF$	
$R_{ON} = \frac{m_{on}}{\omega C} = 0.0145Ohm$	
$R_{OFF} = \frac{m_{off}}{\omega C} = 1.445kOhm$	
$C_1 = \frac{1}{\omega R_L Q_0} = 79.577pF$	$C_1 = \frac{1}{\omega R_L Q_0} = 1.59pF$
$L_1 = \frac{(Q_0+K_X)R_L}{\omega} = 0.3213nH$	$L_1 = \frac{(Q_0+K_X)R_L}{\omega} = 15.9nH$

the load resistor R_L is 1Ω, the component values can be calculated based upon the given design set K and Eqs.3.29-3.32 and Eqs.3.45-3.46 (since $K_X > 0$). Table3.3 shows the component values for $Q_0 = 2$ and $Q_0 = 100$. We can regard $Q_0 = 100$ as infinite loaded quality factor. To make a fair comparison the rise and fall times of the drive signal in the ADS model is set to zero. By substituting the component values into the ADS model, we get the drain efficiency of 91.8% for $Q_0 = 2$ and 95.4% for $Q_0 = \infty$. All the results are summarized in Table. 3.2. One can observe that the results of analytical solution and ADS solution are almost the same. The drain voltage and current waveforms obtained from ADS simulation are also shown in Fig. 3.7. One can find that a very good agreement in the waveforms are observed between ADS and the analytical model. The results presented above indicate the analytical design solutions give reasonable accuracy. In addition, it is apparent that for a low Q_0 value the efficiency decreases and peak drain voltage increases. This example also tells us that the quality factor Q_0 affects the performance of Class-E amplifier.

3.2.2 Effects of Drain Load Impedances on Class-E Amplifier

Since the sufficiently good accuracy, the general Class-E model derived in Sections 3.1.2 and 3.1.3 can be used to evaluate the performance of the Class-E power amplifier in a specified

(a) K_P

(b) K_P

(c) K_L

(d) K_X
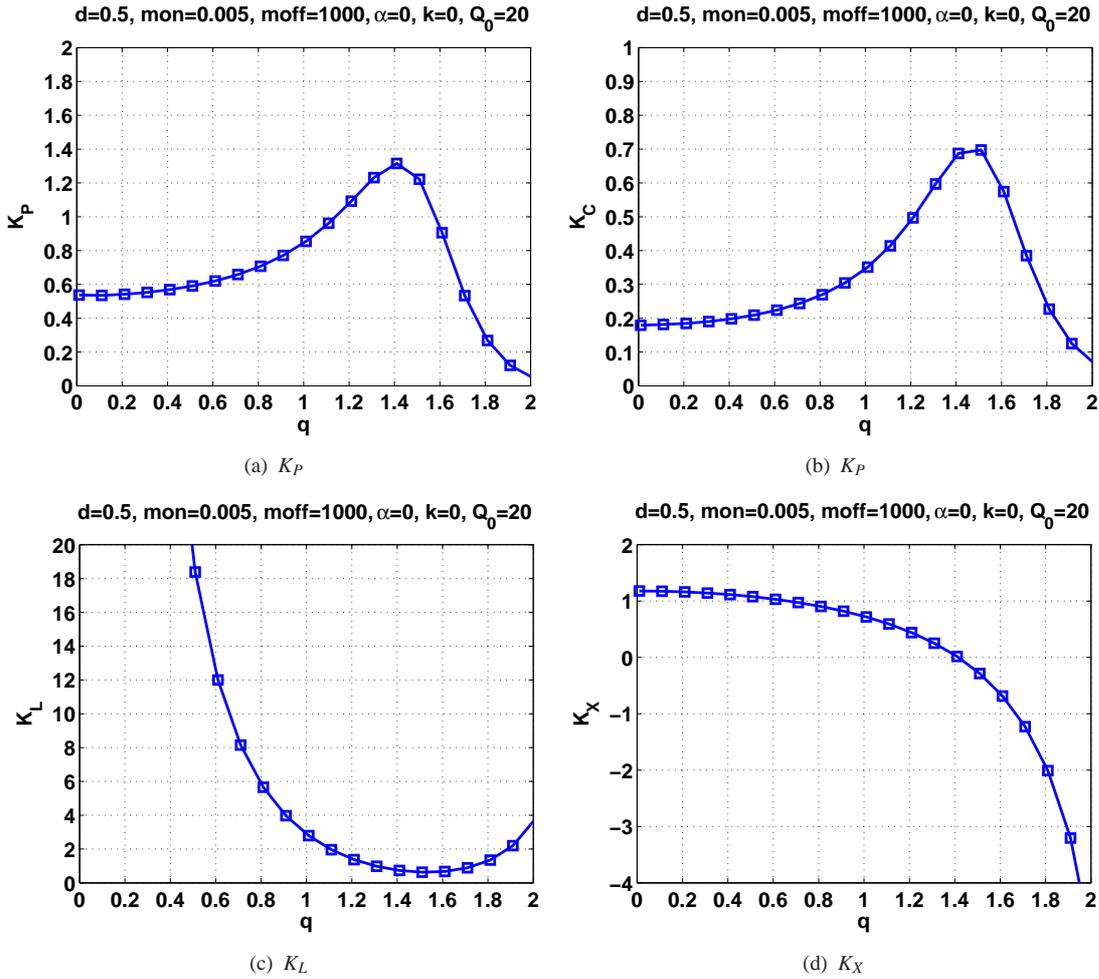
FIGURE 3.9: Elements of the design set K_P, K_C, K_L, K_X as a function of q

situation. In the following discussion, normalization to $V_{DD} = 1$, $R_L = 1$, design angular frequency $\omega_0 = 1$, and technology parameters $m_{on} = 0.005$ and $m_{off} = 1000$ have been used for convenience.

In [34] and [35], a technique, which is based upon a finite number of harmonics, for analysis of Class-E power amplifiers is developed. The analysis shows the number of harmonics will determine the maximum achievable efficiency. The fundamental and harmonic impedances for "optimum" Class-E PAs with infinite dc-feed inductance are also given in [34]. However the Class-E PAs with infinite dc-feed inductance might not be an "optimum" PA. Fig.3.9 and 3.10 illustrate the drain efficiency, power-output capability and design set K as a function of q (varying the dc-feed inductance from infinite to finite values). It is observed that the power-output capability has a peak value when $q = 1.412$. The same conclusion can be also obtained from the design set K_P which achieves a maximum value when $q = 1.412$. The efficiency remains constant for different dc-feed inductances. Therefore, for a given V_{DD} and R_L, the optimum Class-E operation is obtained when $q = 1.412$.

(a) Drain efficiency

(b) Power-output capability
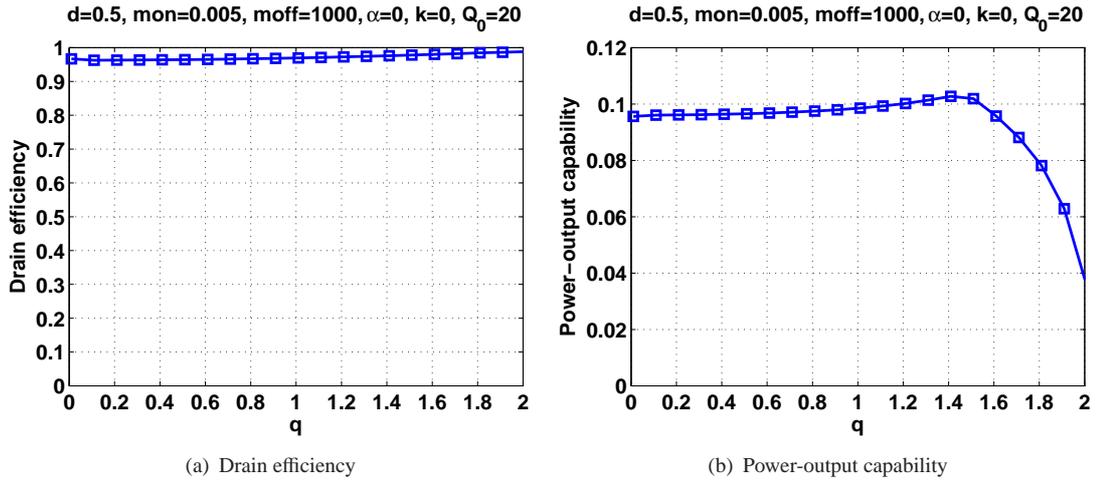
FIGURE 3.10: Drain efficiency and power-output capability as a function of q
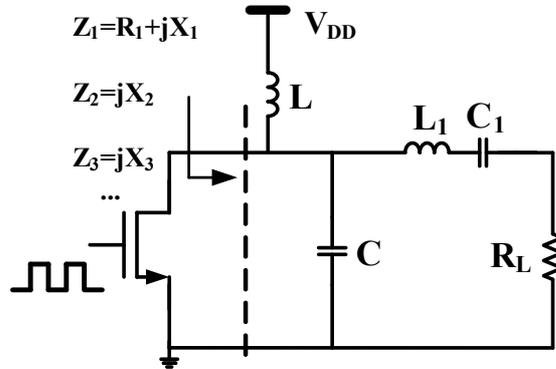
FIGURE 3.11: Drain load impedances of Class-E PAs

To enable the design of Class-E amplifiers a closer examination of the output load network is required. The drain load impedances Z_k shown in Fig.3.11 consists of shunt capacitance, dc-feed inductance and output load network . The admittance of load network as a function of frequency is given as:

$$Y_k(\omega)|_{\omega=k\omega_0} = j\omega C + \frac{1}{j\omega L} + \frac{1}{R_L + j\omega L_1 + 1/j\omega C_1}. \tag{3.97}$$

where k is a real number. When k is an integer, Y_k describes the admittance at fundamental and harmonic frequencies.

Substituting Eqs. 3.63, 3.64, 3.66-3.68 into Eq.3.97 and normalizing to R_L we can get:

$$Y_k(\omega)R_L|_{\omega=k\omega_0} = \frac{(\frac{\omega}{\omega_0})^2 \frac{1}{Q_C^2}}{(1-(\frac{\omega}{\omega_0})^2 \frac{Q_L}{Q_C})^2 + (\frac{\omega}{\omega_0} \frac{1}{Q_C})^2} + j \frac{(\frac{\omega}{\omega_0})^2 \frac{1}{q^2} - 1}{K_L(\frac{\omega}{\omega_0})^2}$$

$$+ j \frac{\frac{\omega}{\omega_0} \frac{1}{Q_C}(1-(\frac{\omega}{\omega_0})^2 \frac{Q_L}{Q_C})}{(1-(\frac{\omega}{\omega_0})^2 \frac{Q_L}{Q_C})^2 + (\frac{\omega}{\omega_0} \frac{1}{Q_C})^2} \tag{3.98}$$
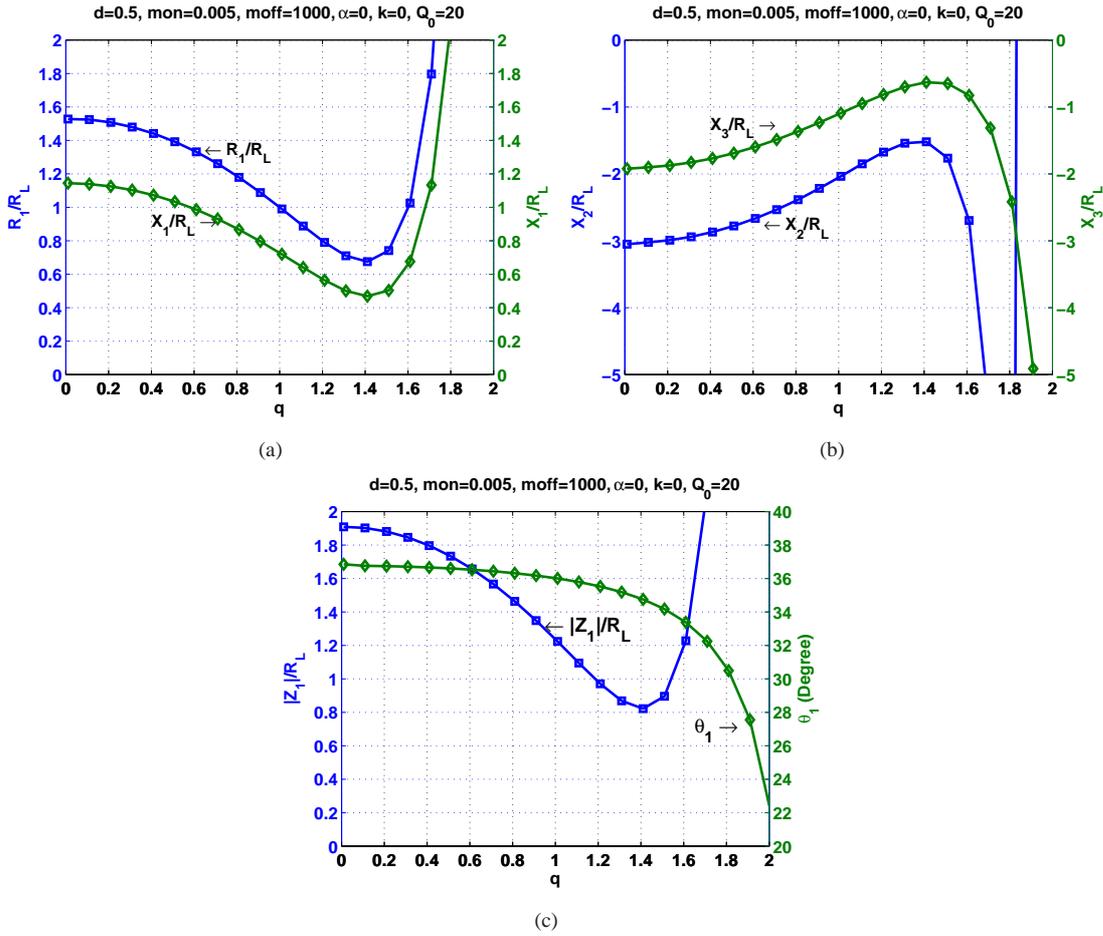
FIGURE 3.12: Equivalent drain load impedance as a function of q: (a)fundamental impedance in terms of resistance and reactance, (b)second and third harmonics impedance in terms of reactance, (c)fundamental impedance in terms of magnitude and phase

then taking inverse of the admittance we can get the normalized impedance,

$$\frac{Z_k(\omega)}{R_L} = \frac{1}{Y_k(\omega)R_L}. \tag{3.99}$$

The required drain load impedances Z_k at fundamental, second and third harmonic frequencies are shown in Fig.3.12. The magnitude $|Z_1|$ of drain load impedance at fundamental frequency reaches its minimum value when $q = 1.412$ which results in the maximum output power. For readers' convenience the drain load impedances for maximum output power operation and for infinite dc-feed inductance are summarized in Table 3.4.

In Table3.4, the required drain load impedances Z_k at fundamental and harmonic frequencies are given. The effects of variations of drain load impedances at fundamental, second and third harmonic frequencies on drain efficiency, K_P, and peak drain-source voltage and peak drain current are given in Figs.3.13-3.24. When investigating the effects of load phase angle θ_k (/magnitude

TABLE 3.4: Harmonic impedances for maximum output power and infinite dc-feed inductance

k	$Z_k = R_k + jX_k$ for $R_L = 1$ $q = 1.412$	$Z_k = |Z_k|exp(j\theta_k)$ for $R_L = 1$ $q = 1.412$	$Z_k = R_k + jX_k$ for $R_L = 1$ $q = 0$	$Z_k = |Z_k|exp(j\theta_k)$ for $R_L = 1$ $q = 0$
1	$0.6831 + j0.4653$	$0.8265\angle34.26$	$1.5287 + j1.1254$	$1.8983\angle36.36$
2	$-j1.4571$	$1.4571\angle-90$	$-j2.7538$	$2.7538\angle-90$
3	$-j0.6253$	$0.6253\angle-90$	$-j1.8338$	$1.8338\angle-90$
4	$-j0.4170$	$0.4170\angle-90$	$-j1.3749$	$1.3749\angle-90$
5	$-j0.3173$	$0.3173\angle-90$	$-j1.0998$	$1.0998\angle-90$
6	$-j0.2576$	$0.2576\angle-90$	$-j0.9164$	$0.9164\angle-90$
7	$-j0.2174$	$0.2174\angle-90$	$-j0.7855$	$0.7855\angle-90$
8	$-j0.1884$	$0.1884\angle-90$	$-j0.6873$	$0.6873\angle-90$
9	$-j0.1663$	$0.1663\angle-90$	$-j0.6109$	$0.6109\angle-90$
10	$-j0.1490$	$0.1490\angle-90$	$-j0.5498$	$0.5498\angle-90$
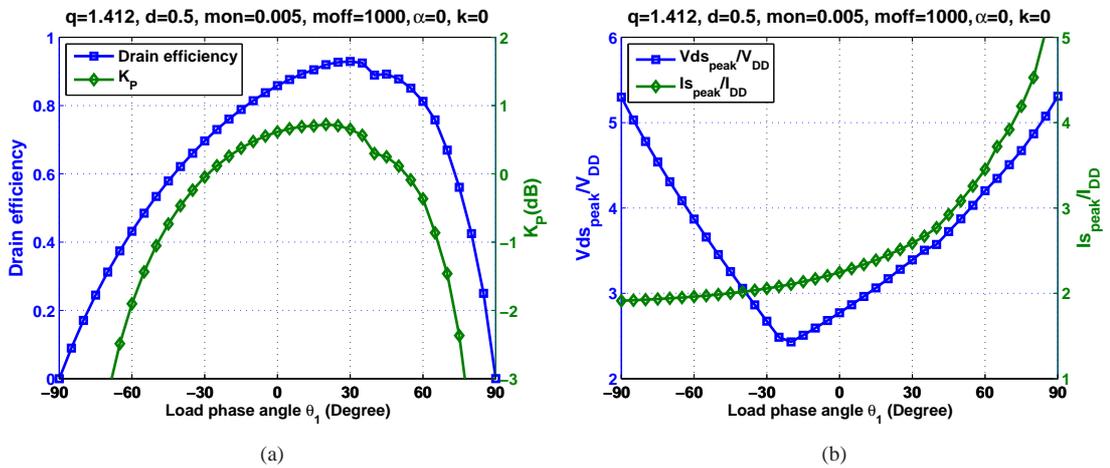
FIGURE 3.13: Effects of load phase angle θ_1 on: (a) drain efficiency and K_P, (b) maximum drain-source voltage and current
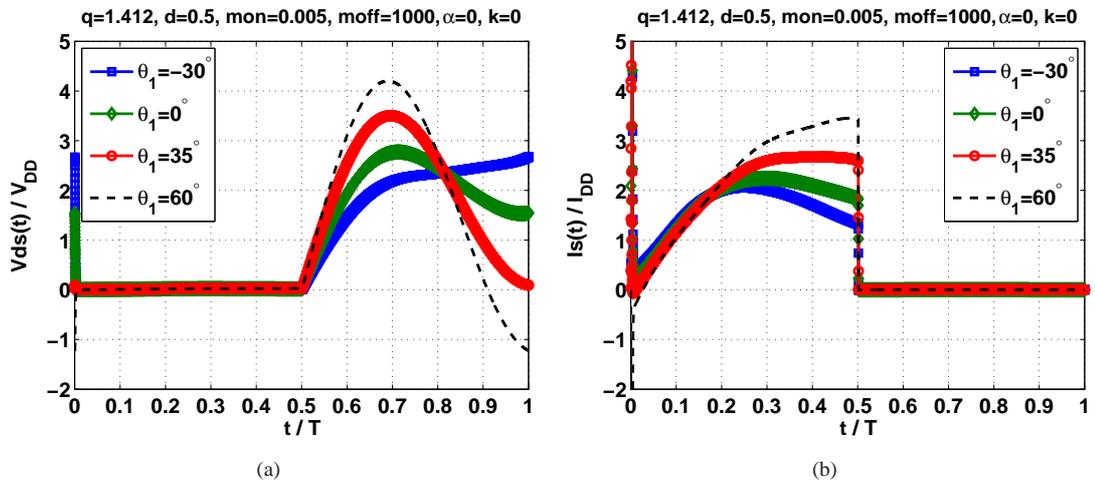
FIGURE 3.14: Waveforms as a function of load phase angle θ_1: (a) drain-source voltage, (b) switch current
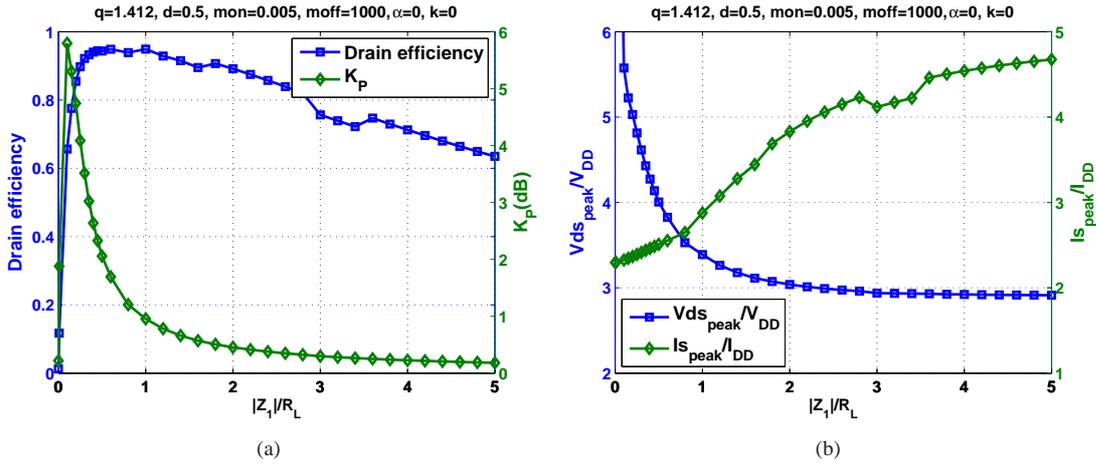
FIGURE 3.15: Effects of magnitude $|Z_1|$ on: (a) drain efficiency and K_P, (b) maximum drain-source voltage and current
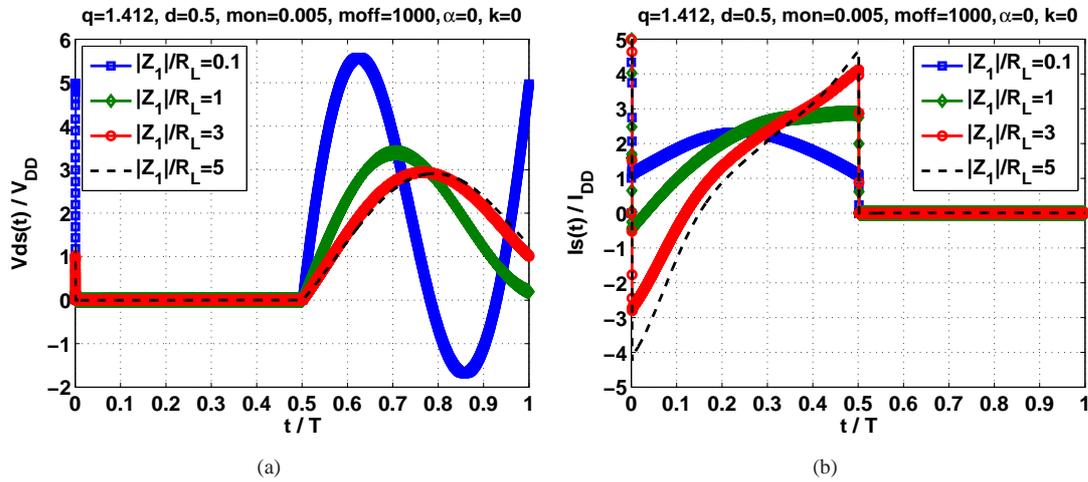
FIGURE 3.16: Waveforms as a function of $|Z_1|$: (a) drain-source voltage, (b) switch current

$|Z_k|$ of drain load impedance) at certain harmonics, the magnitudes $|Z_k|$ of drain load impedance (/load phase angles θ_k) at this frequency and other frequencies are fixed at their required values.

The effects of load phase angle θ_1 of drain load impedance Z_1 at fundamental frequency f_0 on the performance of maximum output power operation are shown in Fig. 3.13, and the effects on drain-source voltage and current waveforms are shown in Fig. 3.14. The drain efficiency remains constant for load phase angles between about $10°$ and $40°$. The K_P keeps constant for load phase angles between about $0°$ and $35°$. The load phase angles θ_1 for constant efficiency and for constant output power are only overlapped in a narrow range ($10°$ ~ $35°$). Out of this range the efficiency and output power decrease very fast. The effect of variation can also be seen in the waveforms. For capacitive loading ($\theta_1 < 0°$) or larger inductive loading ($\theta_1 > 60°$), the drain-source voltage becomes large at the turn-on moment, resulting in low efficiency. We can also find out that the device should have negative current conducting capability when the

load phase angle θ_1 is larger than $60°$. For a large load phase angle θ_1, the peak drain voltage is beyond $4V_{DD}$ which might lead to drain-source breakdown.

Fig. 3.15 shows the effects of magnitude $|Z_1|$ variation of drain load impedance Z_1 at fundamental frequency f_0. It is apparent that comparing with the variation of θ_1 the amplifier is tolerant of variations of $|Z_1|$, and maintains high efficiency for values between 0.25 and 2. As expected, K_P increases with decreasing $|Z_1|$ except for relatively small values of $|Z_1|$. Peak output power occurs at 0.1, but the corresponding efficiency is low and peak drain voltage is large. Therefore, $|Z_1|$ should be larger than $0.1R_L$. From Eqs.3.61 and 3.64, one can obtain that:

$$\frac{m_{on}}{K_C} = \frac{\omega R_{ON}C}{\omega R_L C} = \frac{R_{ON}}{R_L}. \tag{3.100}$$

For $q = 1.412$, d=0.5, $m_{on} = 0.005$, $m_{off} = 1000$, $\alpha = 0$, and $k = 0$, one can find $K_C = 0.6871$. Therefore,

$$|Z_1| > 13.7R_{ON}. \tag{3.101}$$

The above equation indicates that the magnitude $|Z_1|$ should be at least 14 times larger than the ON-resistance. As the magnitude $|Z_1|$ becomes very small, the ON-resistance of the switch draws more and more current than the load current causing low efficiency. For small values of $|Z_1|$, they give high conduction losses and low efficiencies. As the magnitude $|Z_1|$ becomes very large, output power tends to become constant. The peak drain-source voltage Vds_{peak} decreases as the magnitude $|Z_1|$ increases, while peak switch current Is_{peak} increases as $|Z_1|$ increases. The effect of magnitude $|Z_1|$ variation can also been found in the waveforms shown in Fig. 3.16. For $|Z_1| = 0.1$, the drain-source voltage at the turn-on moment is very large resulting in the large switch loss. For large values of $|Z_1|$, the waveforms are almost similar which indicates that the amplifier is quite tolerant of large magnitude $|Z_1|$.

The effects caused by changes in load phase angle θ_2 of drain load impedance Z_2 at second harmonic frequency $2f_0$ are shown in Fig. 3.17. It is obvious that the efficiency decreases as load phase angle θ_2 varies from the pure capacitive loading ($\theta_2 = -90°$) to the resistive and capacitive loading ($-90° < \theta_2 < 0°$) resulting in the power loss at resistive load of second harmonic impedance. The K_P keeps constant for capacitive loading ($-90° \leq \theta_2 \leq 0°$) and increases for inductive loading because of second harmonic tuning. The drain-source voltage and drain current waveforms are shown in Fig.3.18. For inductive loading $\theta_2 > 0°$ at $2f_0$, the peak drain-source voltages are larger than $4V_{DD}$ although the drain-source voltages at turn-on moment are small.
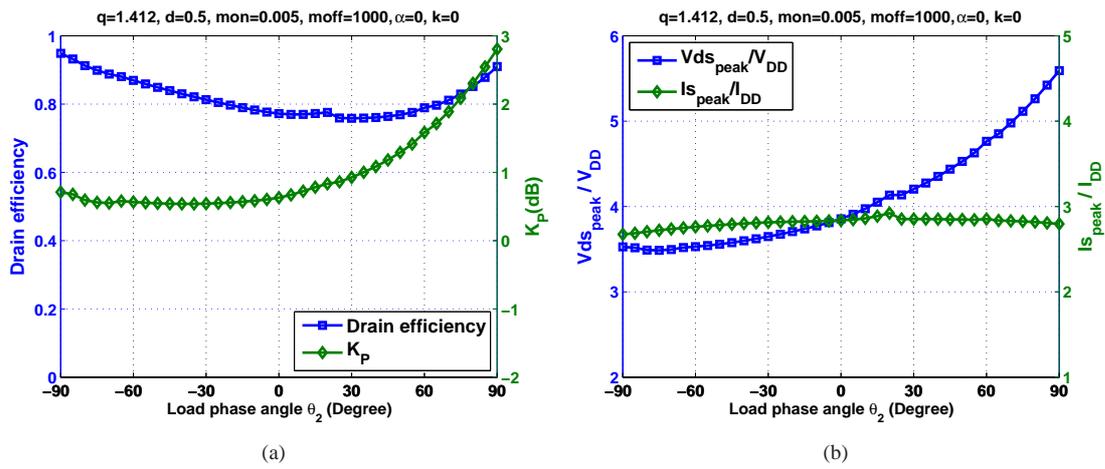
FIGURE 3.17: Effects of load phase angle θ_2 of second harmonic impedance: (a) drain efficiency and K_P, (b) maximum drain-source voltage and current
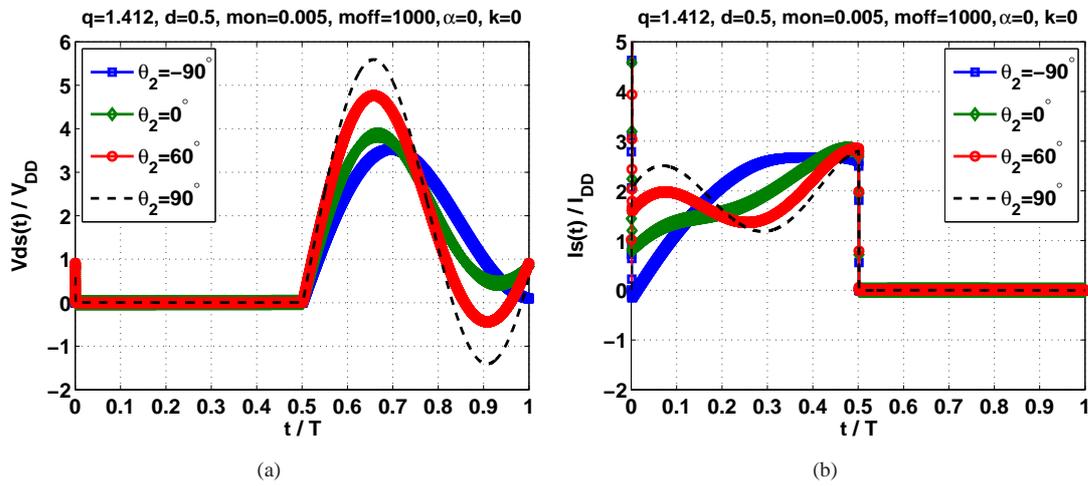
FIGURE 3.18: Waveforms as a function of θ_2: (a) drain-source voltage, (b) switch current
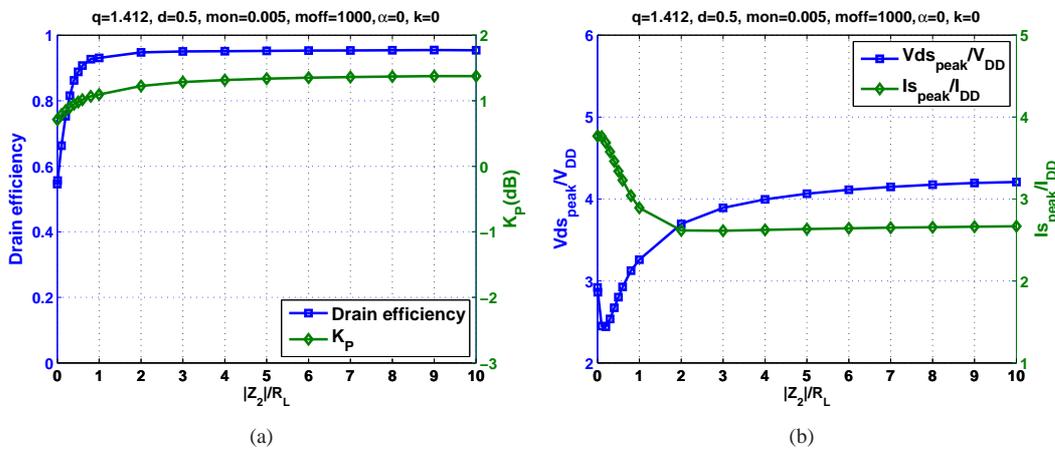
FIGURE 3.19: Effects of magnitude $|Z_2|$ of second harmonic impedance: (a) drain efficiency and K_P, (b) maximum drain-source voltage and current
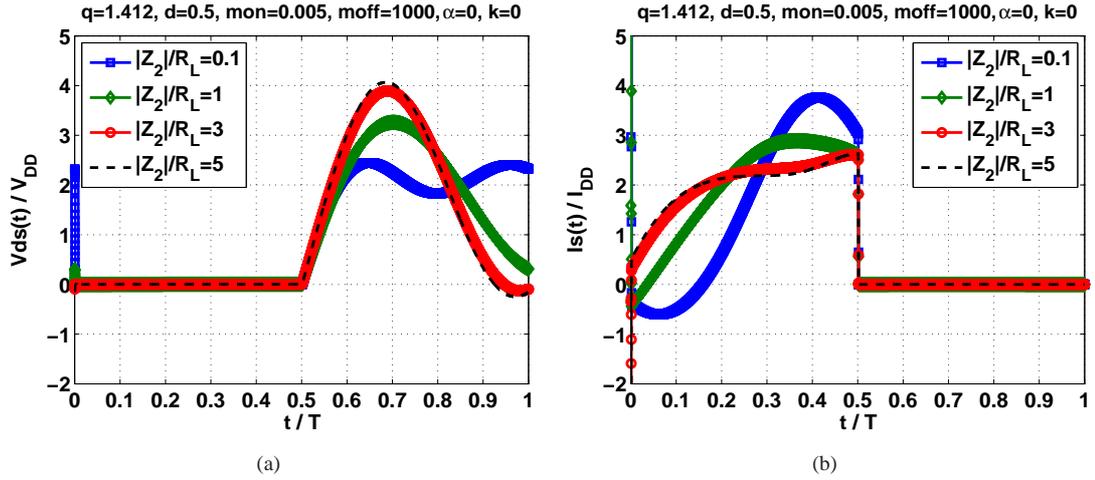
FIGURE 3.20: Waveforms as a function of $|Z_2|$: (a) drain-source voltage, (b) switch current
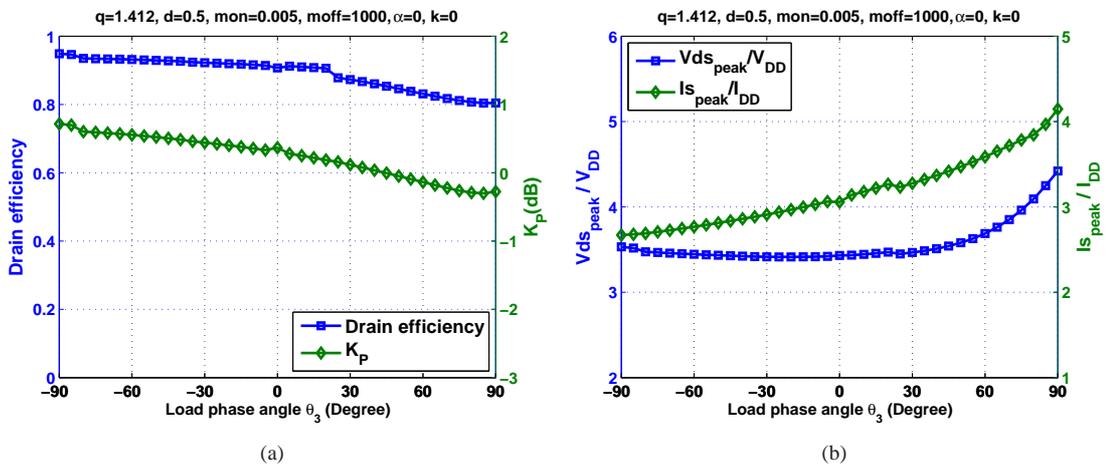
FIGURE 3.21: Effects of load phase angle θ_3 of third harmonic impedance: (a) drain efficiency and K_P, (b) maximum drain-source voltage and current

Fig. 3.19 illustrates the effects of magnitude $|Z_2|$ variation of drain load impedance Z_2 at second harmonic frequency $2f_0$. It is apparent that the amplifier is very tolerant of variations of $|Z_2|$ except for very small values, and maintains high efficiency and constant K_P. The peak drain-source voltage for large values of $|Z_2|$ is about $4.2V_{DD}$ which is not beyond $4V_{DD}$ too much.

The effects of load phase angle θ_3 of drain load impedance Z_3 at third harmonic frequency $3f_0$ are shown in Fig. 3.21. One can observe that the efficiency remains almost constant for capacitive loading ($-90° \leq \theta_3 \leq 0°$), and decreases by 10% for inductive loading. The change of K_P for all the variations of θ_3 is less than 1dB. The peak drain-source voltage Vds_{peak} keeps constant and is less than $4V_{DD}$ for a very wide range of θ_3.

In Figs. 3.23 and 3.24, the effects of magnitude $|Z_3|$ variations are shown. It is obvious that the amplifier is almost independent on $|Z_3|$ except for very small values.

(a)

(b)
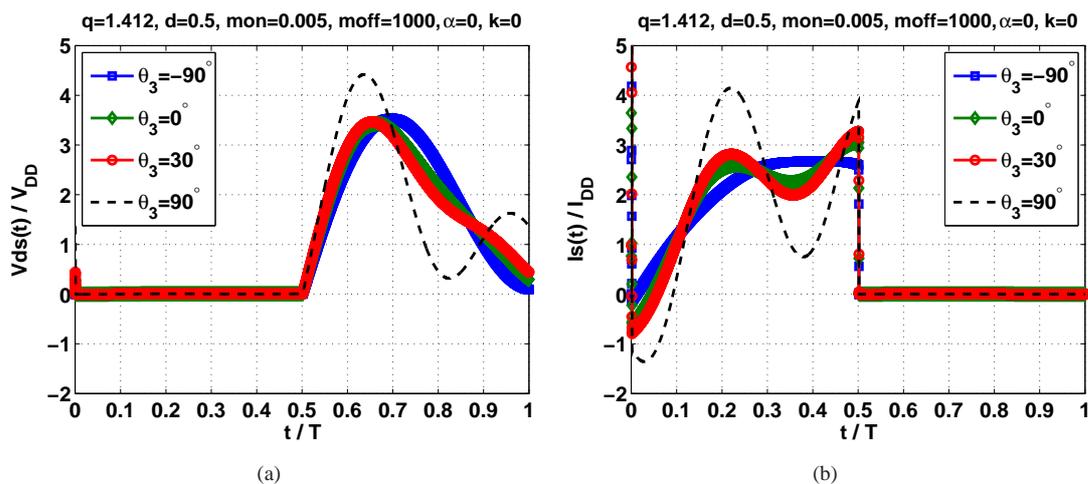
FIGURE 3.22: Waveforms as a function of θ_3: (a) drain-source voltage, (b) switch current

(a)

(b)
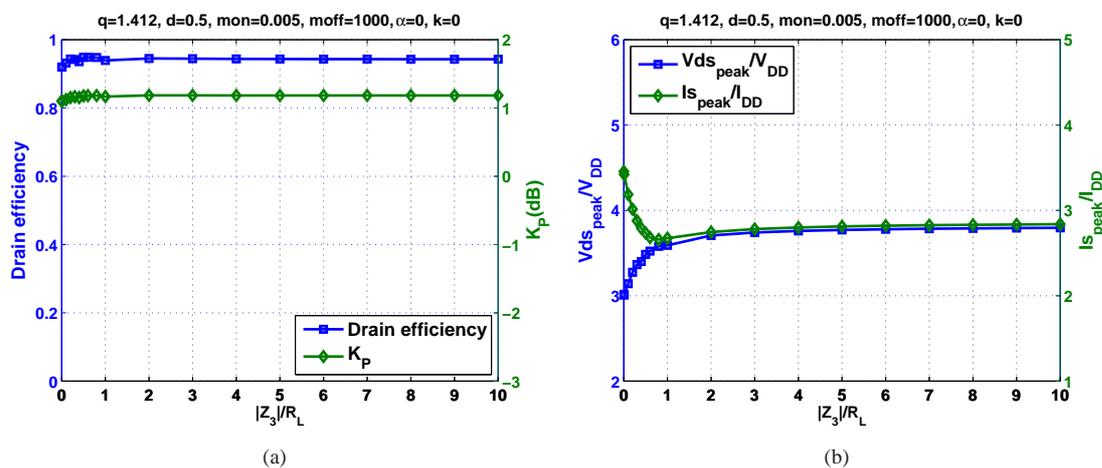
FIGURE 3.23: Effects of magnitude $|Z_3|$ of third harmonic impedance: (a) drain efficiency and K_P, (b) maximum drain-source voltage and current

(a)

(b)
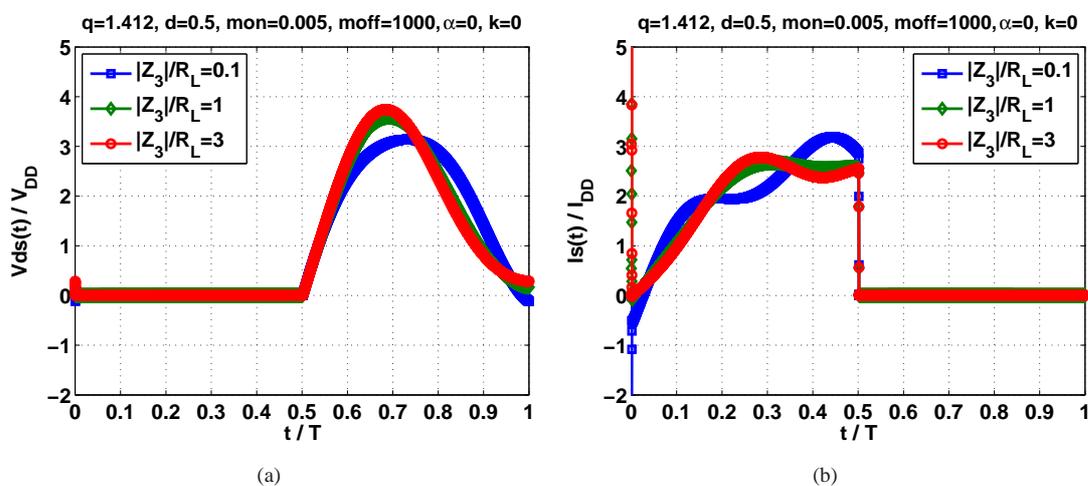
FIGURE 3.24: Waveforms as a function of $|Z_3|$: (a) drain-source voltage, (b) switch current

Several remarks are needed here to understand the significance of these graphs.

1. For a high-efficient Class-E power amplifier, the load phase angle θ_1 is the most important design parameter because the efficiency, K_P and peak drain-source voltage all are very sensitive to it. The optimum range of load phase angle θ_1 for high efficiency, high output power and low peak drain-source voltage operation is between $10°$ and $40°$.

2. Decreasing magnitude $|Z_1|$ can improve the output power, but magnitude $|Z_1|$ should be at least 14 times larger than the ON-resistance R_{ON}.

3. To obtain high efficiency, the ideal impedances at harmonic frequencies should be open conditions.

4. It is apparent that a tune-up procedure must not be based on either drain efficiency or output power. A moderate efficiency and output power with reliable drain voltage would be a better tuning indicator.

The methods developed in this section may be applied to any other problem that can be simplified to variations in load phase angle and magnitude. A straightforward example is prediction of performance with frequency variations which will be presented in the next section. This manifests itself as a set of values of $\theta_k(\omega)$ and $|Z_k(\omega)|$ corresponding to the value of frequency.

3.2.3 Broadband Characteristics of Conventional Class-E Output Load Network

The usable bandwidth is an important aspect of power amplifier performance. In [36] Raab briefly analyzed the frequency variations of classical Class-E load network with infinite dc-feed inductance. The drain efficiency and output power are given for different loaded quality factor Q_0. Kumar designed a broadband Class-E PA with the classical load network by using reactance-compensation technique [7]. Actually the load network he used corresponds to the finite dc-feed inductance for $q = 1.412$.

It seems that no work has been published on the comprehensive analysis of conventional Class-E load network across a broad bandwidth. In this section, the effects of loaded quality factor Q_0, finite dc-feed inductance q and duty-cycle d on drain efficiency, output power, peak drain-source voltage and peak drain current will be studied.

The analytical design equations derived in Sections 3.1.2 and 3.1.3 aim at the conventional output load network of Class-E PAs shown in Fig.3.1. For a fixed-tuned output load network designed at frequency f_0, which means the design set K is fixed, the frequency variations can be modeled by scaling the frequency parameter ω in Section 3.1.3. By this method, the power amplifier performance as a function of frequency can be investigated.
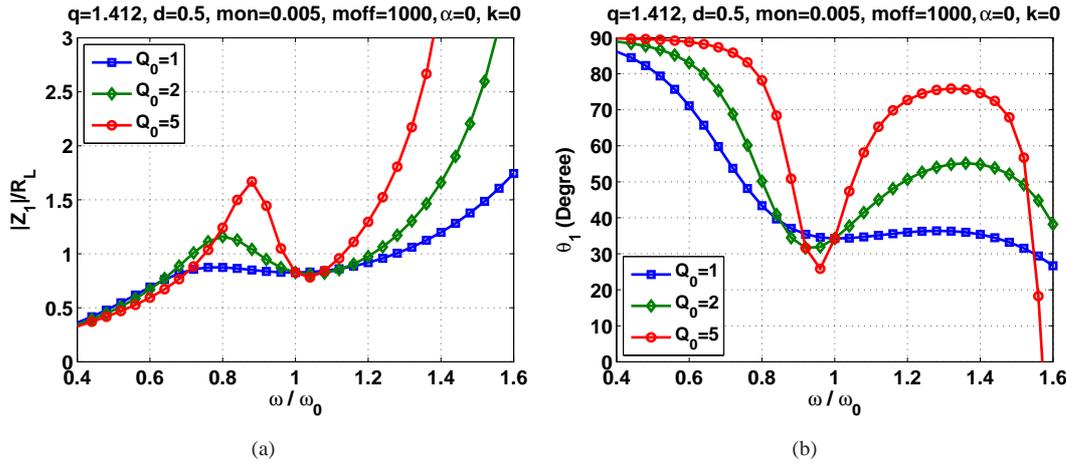
FIGURE 3.25: Fundamental impedance as a function of frequency for different Q_0
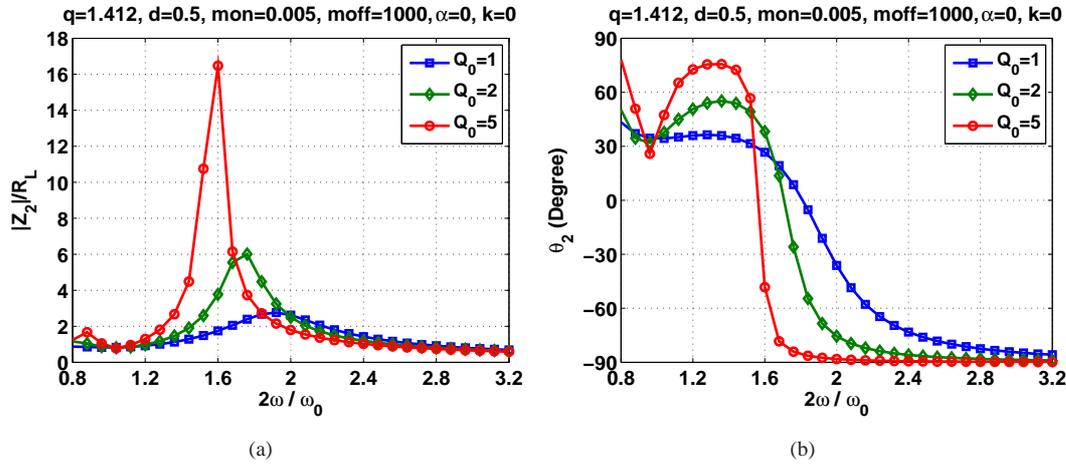
FIGURE 3.26: Second harmonic impedance as a function of frequency for different Q_0

First the effects of loaded quality factor Q_0 is investigated. Figs. 3.25 and 3.26 show the magnitudes and load phase angles of drain load impedance at fundamental and second harmonic frequencies for different loaded quality factor Q_0. The output load network is set for maximum output power ($q = 1.412$). We can predict the broadband performance based upon the results obtained in the Section 3.2.2. The magnitude $|Z_1|$ and load phase angle θ_1 is more tolerant of frequency variations for low Q_0 values than for high Q_0 values. For example, the magnitude $|Z_1|$ and load phase angle θ_1 for $Q_0 = 1$ is almost flat from $\omega = 0.8\omega_0$ to $\omega = 1.2\omega_0$. This means it is possible to provide very flat drain efficiency and output power in this band. But the load phase angle θ_2 for $Q_0 = 1$ deviates from the required value of $-90°$ and increases sharply as the frequency decreases which will result in the drain efficiency drop at low frequency. For $Q_0 = 5$, the load phase angle θ_2 is near $-90°$ from $\omega = 0.85\omega_0$ satisfying the required load phase angle at second harmonic frequency. This will show high efficiency in band. However since the change rate of the load phase angle θ_1 is fast for $Q_0 = 5$, the output power for $Q_0 = 5$ will decrease sharply between $\omega = 0.8\omega_0$ and $\omega = 1.2\omega_0$.

(a) Drain efficiency

(b) K_P

(c) Peak drain voltage

(d) Peak drain current
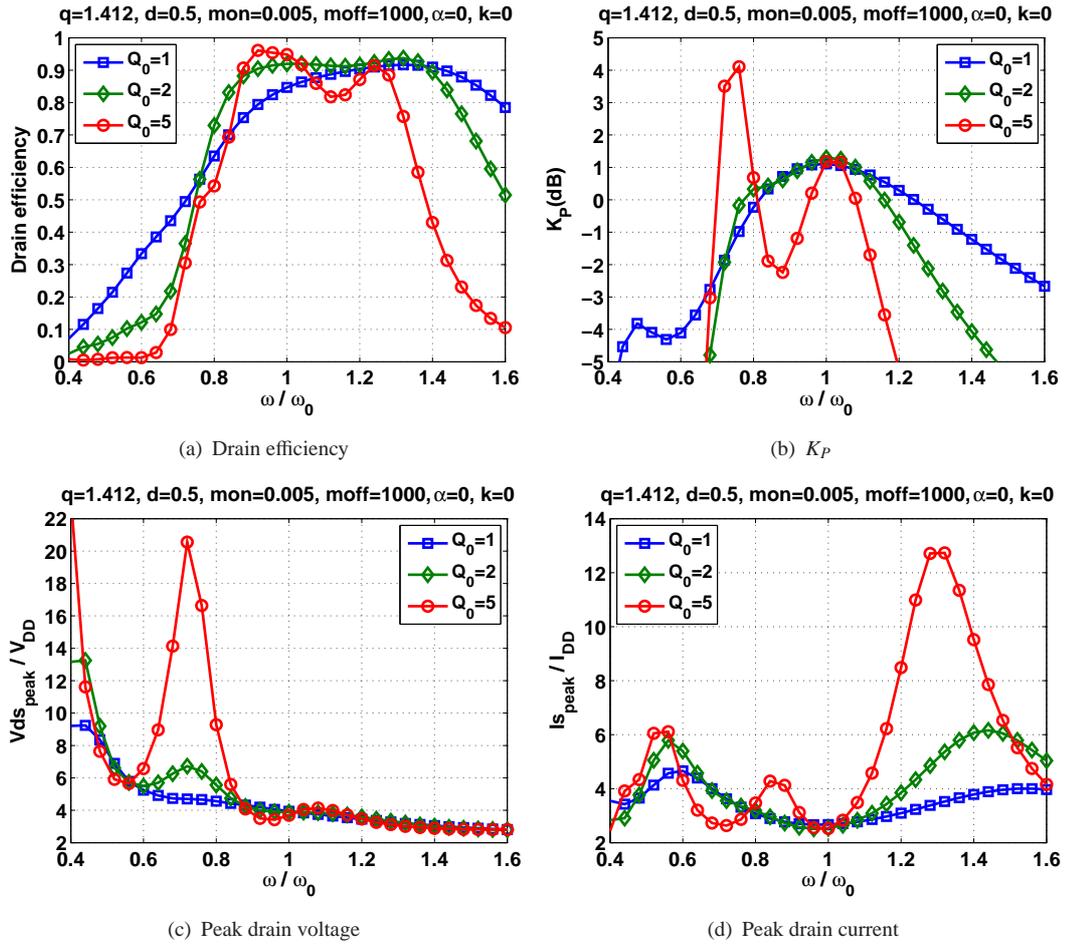
FIGURE 3.27: Effects of finite load quality factor on the wideband operation

Fig. 3.27 presents the variation of efficiency, K_P, peak drain-source voltage, and peak drain current as a function of frequency with Q_0 as a parameter, and Table 3.5 summarizes the bandwidth for different criteria. The overlapping frequency range in Table 3.5-3.7 is the frequency range in which the drain efficiency is larger than 80%, and output power flatness is less than 1dB, and peak drain voltage is less than $4V_{DD}$. It is apparent that the bandwidth in terms of drain efficiency and output power is wider for low Q_0 values than for high Q_0 values. The large loaded quality factor Q_0 can improve the peak drain efficiency, but reduce the usable bandwidth due to the dramatical variation of load phase angle in the band. The effect of large loaded quality factor is visible at $\omega = 1.1\omega_0$ and $\omega = 0.85\omega_0$ where the efficiency is decreasing faster due to load angle θ_1 beyond 60° for $Q_0 = 5$. These results agree very well with what we predicted based upon Figs.3.25 and 3.26. One must notice that the peak drain-source voltage might be larger than $4V_{DD}$ even the drain efficiency is larger than 80% at some frequencies. The peak drain-source voltage decreases as the frequency increases. In summary, the bandwidth over which a given efficiency can be obtained is roughly inversely proportional to Q_0 for moderate and large values of Q_0 [36].

TABLE 3.5: Effects of loaded quality factor Q_0 on the bandwidth

	Frequency range for drain efficiency$\geq 80\%$	Frequency range for $\Delta K_P \leq \pm 0.5dB$	Frequency range for $Vds_{peak} \leq 4V_{DD}$	Overlapping frequency range
$Q_0 = 1$	$0.92\omega_0 \leq \omega \leq 1.58\omega_0$	$0.82\omega_0 \leq \omega \leq 1.24\omega_0$	$\omega \geq 0.96\omega_0$	$0.96\omega_0 \leq \omega \leq 1.24\omega_0$
	52.8%	40.8%		25.5%
$Q_0 = 2$	$0.82\omega_0 \leq \omega \leq 1.46\omega_0$	$0.78\omega_0 \leq \omega \leq 1.16\omega_0$	$\omega \geq 0.92\omega_0$	$0.92\omega_0 \leq \omega \leq 1.16\omega_0$
	56.1%	39.2%		23.1%
$Q_0 = 5$	$0.86\omega_0 \leq \omega \leq 1.30\omega_0$	$0.96\omega_0 \leq \omega \leq 1.08\omega_0$	$\omega \geq 0.88\omega_0$	$0.96\omega_0 \leq \omega \leq 1.08\omega_0$
	40.7%	11.8%		11.8%

FIGURE 3.28: Fundamental impedance as a function of frequency for different Q_0

The effects of finite dc-feed inductance on the drain load impedance at fundamental frequency are shown in Fig. 3.28. As q increases, the center frequency moves to higher frequency. The variations of load phase angle θ_1 and magnitude $|Z_1|$ of finite dc-feed inductance ($q = 1.61$) is smaller than that of infinite dc-feed inductance ($q = 0.01$) so that the finite dc-feed inductance can improve the bandwidth in terms of drain efficiency and output power. Fig. 3.29 shows the broadband features of Class-E power amplifier for different dc-feed inductance when $Q_0 = 2$. Table 3.6 summarizes the bandwidth for different q. One can observe that the bandwidth with an efficiency of 80% or better is 42.9% for $q = 0.01$ while it is 56.1% for $q = 1.41$. The bandwidth for a 80% drain efficiency is improved by 30.7% via finite dc-feed inductance. The bandwidth of 1dB output power flatness is 29.2% for $q = 0.01$ while it is 39.2% for $q = 1.41$. Meanwhile, the K_P for $q = 1.41$ is 3dB larger than that for infinite dc-feed inductance.

When the output load network is fixed, the duty-cycle is the only one parameter that the designer can tune with besides the supply voltage. The effects of duty-cycle variation can now be examined. Fig. 3.30 shows how drain efficiency , K_P, peak drain-source voltage and peak drain current vary with duty-cycle in a broad frequency band, and Table 3.7 summarizes the bandwidth performance of the amplifier. One can observe that the frequency range for high efficiency shifts to the low frequency band as the duty-cycle increases. The bandwidth for high

(a) Drain efficiency

(b) K_P

(c) Peak drain voltage

(d) Peak drain current
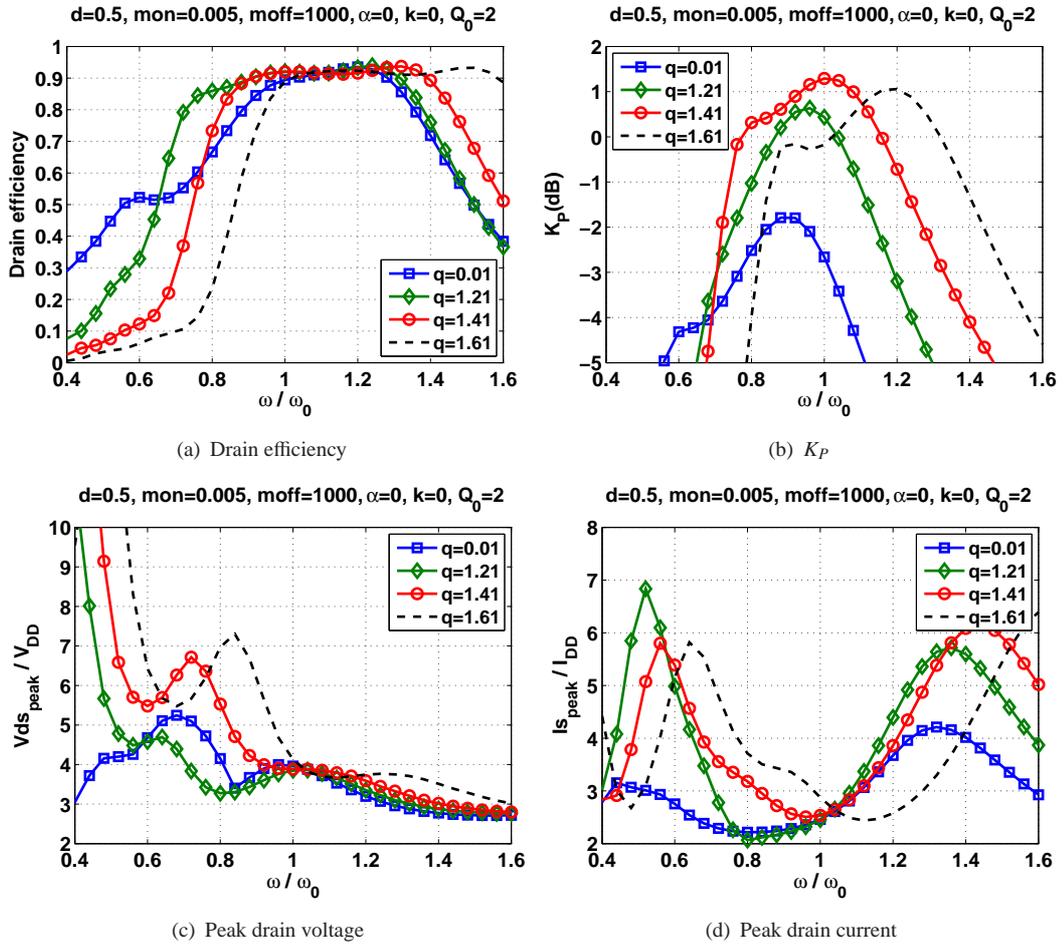
FIGURE 3.29: Effects of finite dc-feed inductance on the wideband operation

TABLE 3.6: Effects of dc-feed inductance on the bandwidth

	Frequency range for drain efficiency$\geq 80\%$	Frequency range for $\Delta K_P \leq \pm 0.5dB$	Frequency range for Vds$_{peak} \leq 4$V$_{DD}$	Overlapping frequency range
q=0.01	$0.88\omega_0 \leq \omega \leq 1.36\omega_0$ 42.9%	$0.76\omega_0 \leq \omega \leq 1.02\omega_0$ 29.2%	$\omega \geq 0.80\omega_0$	$0.88\omega_0 \leq \omega \leq 1.02\omega_0$ 14.7%
q=1.21	$0.72\omega_0 \leq \omega \leq 1.38\omega_0$ 62.9%	$0.84\omega_0 \leq \omega \leq 1.06\omega_0$ 23.2%	$\omega \geq 0.70\omega_0$	$0.84\omega_0 \leq \omega \leq 1.06\omega_0$ 23.2%
q=1.41	$0.82\omega_0 \leq \omega \leq 1.46\omega_0$ 56.1%	$0.78\omega_0 \leq \omega \leq 1.16\omega_0$ 39.2%	$\omega \geq 0.92\omega_0$	$0.92\omega_0 \leq \omega \leq 1.16\omega_0$ 23.1%
q=1.61	$0.94\omega_0 \leq \omega \leq 1.66\omega_0$ 55.4%	$1.04\omega_0 \leq \omega \leq 1.32\omega_0$ 23.7%	$\omega \geq 1.02\omega_0$	$1.04\omega_0 \leq \omega \leq 1.32\omega_0$ 23.7%

(a) Drain efficiency

(b) K_P

(c) Peak drain voltage

(d) Peak drain current
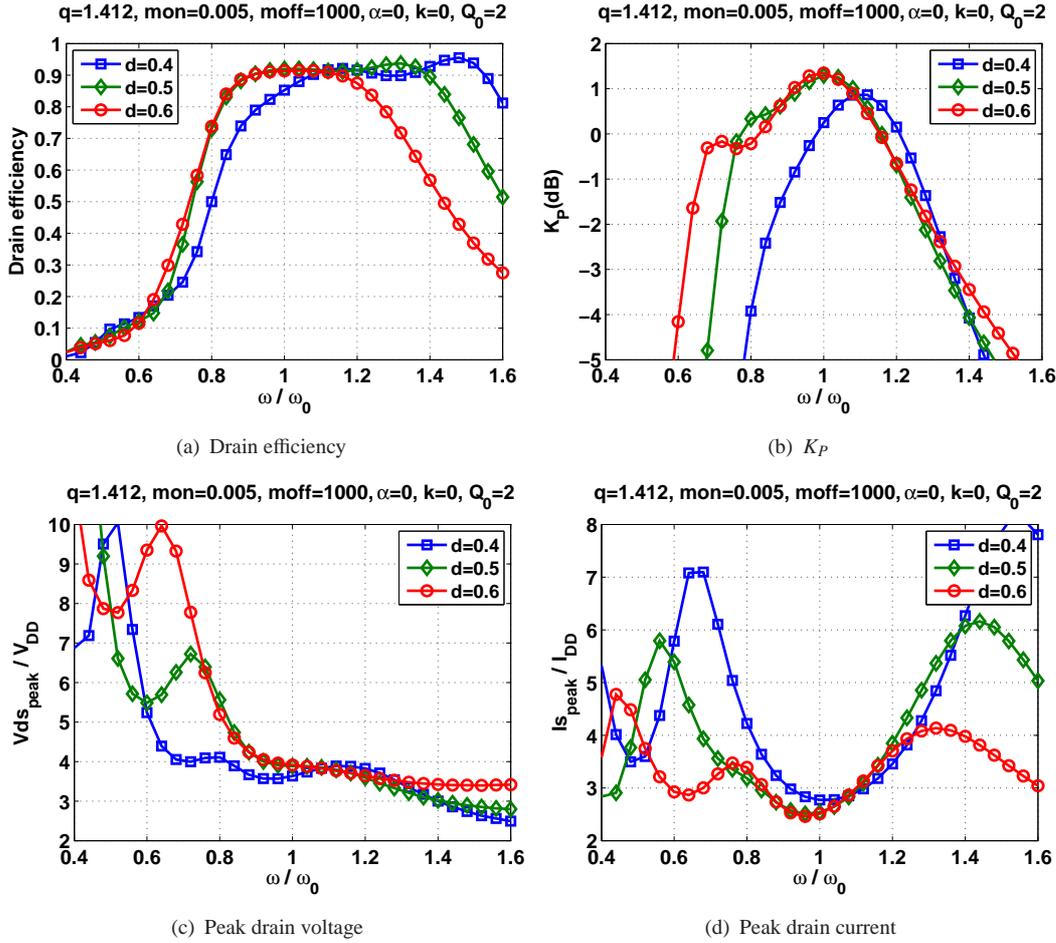
FIGURE 3.30: Effects of duty-cycle on the wideband operation

TABLE 3.7: Effects of duty-cycle on the bandwidth

	Frequency range for drain efficiency $\geq$ 80%	Frequency range for $\Delta K_P \leq \pm 0.5 dB$	Frequency range for $Vds_{peak} \leq 4V_{DD}$	Overlapping frequency range
d=40%	$0.94\omega_0 \leq \omega \leq 1.60\omega_0$ 52.0%	$0.96\omega_0 \leq \omega \leq 1.22\omega_0$ 23.9%	$\omega \geq 0.76\omega_0$	$0.96\omega_0 \leq \omega \leq 1.22\omega_0$ 23.9%
d=50%	$0.82\omega_0 \leq \omega \leq 1.46\omega_0$ 56.1%	$0.78\omega_0 \leq \omega \leq 1.16\omega_0$ 39.2%	$\omega \geq 0.92\omega_0$	$0.92\omega_0 \leq \omega \leq 1.16\omega_0$ 23.1%
d=60%	$0.82\omega_0 \leq \omega \leq 1.26\omega_0$ 42.3%	$0.86\omega_0 \leq \omega \leq 1.14\omega_0$ 28.0%	$\omega \geq 0.92\omega_0$	$0.92\omega_0 \leq \omega \leq 1.14\omega_0$ 21.4%

efficiency decreases as the duty-cycle increases from 50% to 60%. The usable frequency range for $Vds_{peak} \leq 4V_{DD}$ is extended to $\omega/\omega_0 = 0.76$ when small duty-cycle ($d = 40\%$) is applied, although the efficiency is less than 80% in the low frequency band. The device reliability is one of most important factors designers have to take into account.

For broadband systems, we need the power amplifiers can have the characteristics of high-efficiency, flat output power, low peak drain-source voltage (which is less than drain-source

breakdown voltage BV_{ds}) across broad frequency band. From the above results, one can conclude that the conventional Class-E output load network is not a good option which can provide the bandwidth of 40% or more. A broadband methodology must be deployed in order to keep good performance over a broad range of frequencies. In Section 5.2, the output load network for broadband application will be addressed.

3.3 Conclusion

This chapter presents an analytical solution in the time domain for the Class-E power amplifiers taking into account the finite dc-feed inductance, non-ideal switch resistance, duty-cycle and finite loaded quality factor. The analysis in this chapter has provided means of determining the performance of a Class-E tuned power amplifier with arbitrary circuit parameters. The accuracy of the developed analytical model shows very good agreement with commercial circuit simulators such as Agilent ADS. A systematic study of the performance of Class-E amplifier upon the drain load impedance has been performed. The simulation shows that the performance of Class-E PA is very sensitive to the load phase angle θ_1. For the maximum output power operation ($q = 1.412$), the optimum range of θ_1 is between $10°$ and $40°$. Meanwhile, the magnitude $|Z_1|$ should be at least 14 times larger than the device's ON-resistance. In addition, the performance of conventional Class-E power amplifier in a broad frequency band is given with the loaded quality factor, finite dc-feed inductance, and duty-cycle as parameters. The study shows that the low loaded quality factor Q_0 can improve the bandwidth, but the efficiency in-band is lower than that of the PA with high loaded quality factor. The study also indicates that the bandwidth of Class-E PA with finite dc-feed inductance ($q = 1.412$) is 8% wider than that of the PA with RF choke. It has been demonstrated that the power amplifier with conventional Class-E output load network is difficult to provide the characteristics of high efficiency, flat output power and low peak drain-source voltage over a very wide frequency band ($\Delta B > 40\%$). So new output matching topologies for wideband class-E operation need to be investigated.

Chapter 4

Effects of Drive Signal and Linear Operation of Class-E Power Amplifier

In chapter 3, an analytical approach is used to model the Class-E power amplifier. In the model, the transistor is operated as a switch which only has two states: ON or OFF. However, the rise and fall times of drive signal to the Class-E amplifier, in practice, are usually not very sharp at high frequency; consequently, the switch resistance varies to ON-resistance or OFF-resistance gradually but not suddenly. Thus it is necessary to build up a model that can include the imperfections in the drive signal with the behavior of the transistor. Once having this model, the effects of the drive signal on the Class-E amplifier will be obtained. In addition, the performance of the Class-E amplifier operating in linear mode can also be investigated by using this model.

Generally a NMOS transistor can be regarded as a voltage-controlled current source shown in Fig.4.1 The drain current can be expressed as [37]:
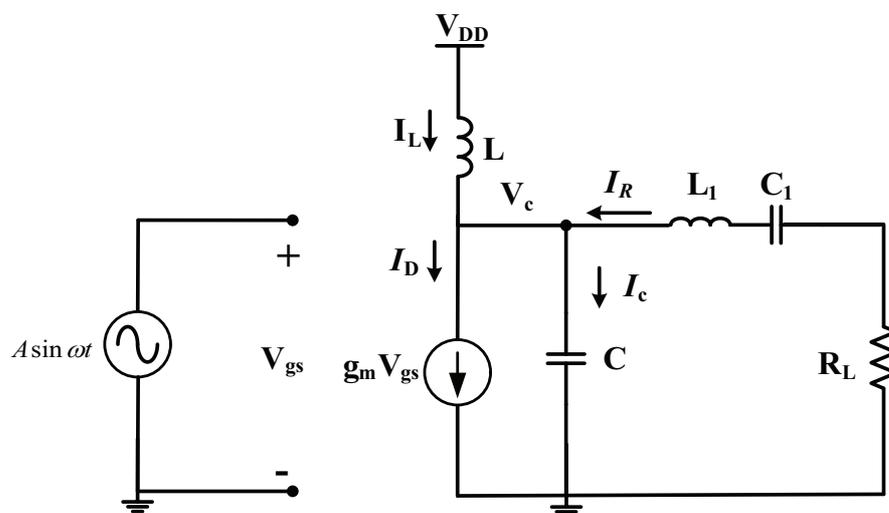
FIGURE 4.1: Simplified small-signal model of Class-E power amplifier

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in triode region or linear region ($V_{DS} \leq V_{GS} - V_{TH}$)

$$I_D = \frac{W}{L}\frac{\mu_n C_{ox}}{2}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \tag{4.1}$$

in saturation region ($V_{DS} > V_{GS} - V_{TH}$)

$$I_D = \frac{W}{L}\frac{\mu_n C_{ox}}{2}[2(V_{GS} - V_{TH})V_{DS}(sat) - V_{DS}^2(sat)] \tag{4.2}$$

where

$$V_{DS}(sat) = V_{GS} - V_{TH}.$$

Similar to the derivation in chapter 3, an equation only containing one unknown variable $V_C(t)$ can be found by applying Kirchhoffs current law at the circuit. However, an explicit analytical solution for $V_C(t)$ appears difficult because of terms such as $V_{GS}(t) = A\sin(\omega t)$ in the equation. Then, a more programmable approach based on the numerical computations in Cadence simulator is used to solve the circuit. In this chapter, a numerical model used for analyzing the Class-E amplifier will first be described. The effects of drive signal on the performance of Class-E amplifier will be discussed in Section 4.2. In Section 4.3, the linear operation of Class-E amplifier will be given.

4.1 Numerical Modeling of CMOS Transistor

A CMOS transistor model mainly concerns transistor's I/V relationships as a function of drive signal and device capacitance.

For the measured I-V curves, the dependent-current source I_D can be modeled via polynomial function for different V_{gs}:

$$I_{Dn}|_{V_{gs}=V_{gsn}} = c_0 + c_1 V_{ds} + c_2 V_{ds}^2 + c_3 V_{ds}^3 + \cdots . \tag{4.3}$$

The coefficients c_n can be obtained by curve fitting. The accuracy of the fitted curves is dependent on the order of polynomial function. Higher order polynomial function fitting always gives better results. Fig.4.2 shows an example using the 6th-order polynomial functions to fit the measured I-V curves. Good agreement is shown between the measured results and fitted curves.

Besides using polynomial functions to fit the measured results, one could create desired I-V curves to model the wanted dependent-current source by defining current function:
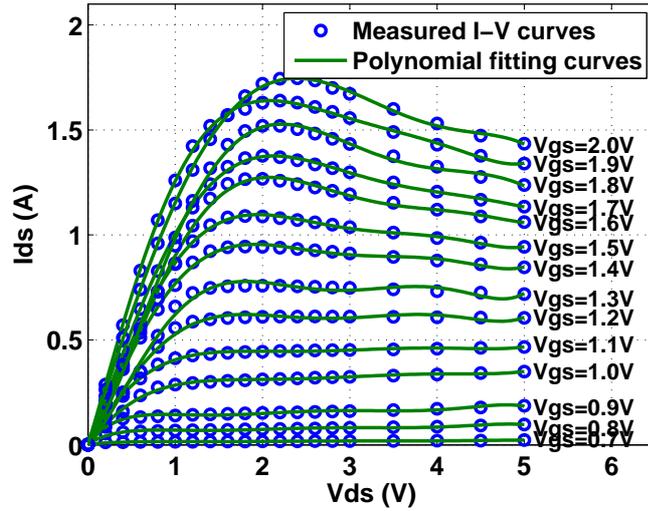
FIGURE 4.2: 6th-order polynomial functions fitting measured I-V curves
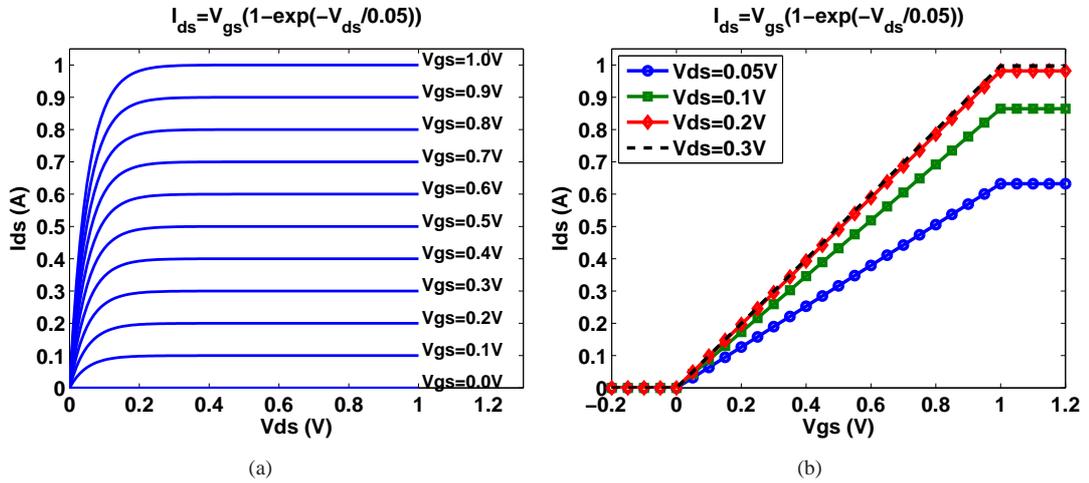
FIGURE 4.3: I-V curves created by Eq. 4.4 for $g_m = 1$, $V_{TH} = 0V$, $I_{max} = 1A$, $V_k = 0.05V$ and $\lambda = 0$

$$I_D = g_m(V_{gs} - V_{TH})I_{max}(1 - \exp(-\frac{V_{ds}}{V_k}))(1 + \lambda V_{ds}) \qquad (4.4)$$

Here the g_m, V_{TH}, I_{max}, V_k and λ are user defined parameters. One can determine when the transistor is turned on beyond V_{TH}, how sensitive the transistor is to V_{gs} by g_m, the maximum drain current that the transistor can conduct by I_{max}, the channel-length modulation by λ, and the linear resistor by V_k. Fig.4.3 shows created I-V curves for $g_m = 1$, $V_{TH} = 0V$, $I_{max} = 1A$, $V_k = 0.05V$ and $\lambda = 0$.

The I-V relationships described by Eq.4.3 or 4.4 provide a reasonable model for understanding the "dc" behavior of CMOS circuits. Moreover, the device capacitances must also be taken into account to predict the "ac" behavior of the device. In [38], an approach to extract the
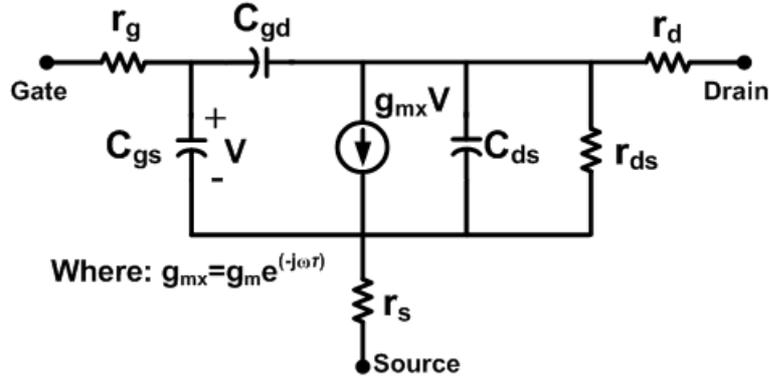
FIGURE 4.4: NMOS small-signal equivalent model

TABLE 4.1: Extracted small-signal model parameters of extended drain NMOS transistor in CMOS 65nm technology with W=3840 μm, L=0.28 μm, V_{gs}=0V, V_{ds}=1V at 1GHz

$r_g = 0.018\Omega$	$r_s = 0.023\Omega$	$r_d = 0.041\Omega$
$C_{gs} = 8.41pF$	$C_{gd} = 2.757pF$	$C_{ds} = 3.244pF$
$r_{ds} = 42.265k\Omega$	$g_m = 2.559mS$	$\tau = -2.49 \times 10^{-10}$

freq (500.0MHz to 1.500GHz)

Red markers : Measured results

Blue lines   : Modeled S-parameters

(a) S11 and S12

freq (500.0MHz to 1.500GHz)

Red markers : Measured results

Blue lines   : Modeled S-parameters

(b) S22 and S21
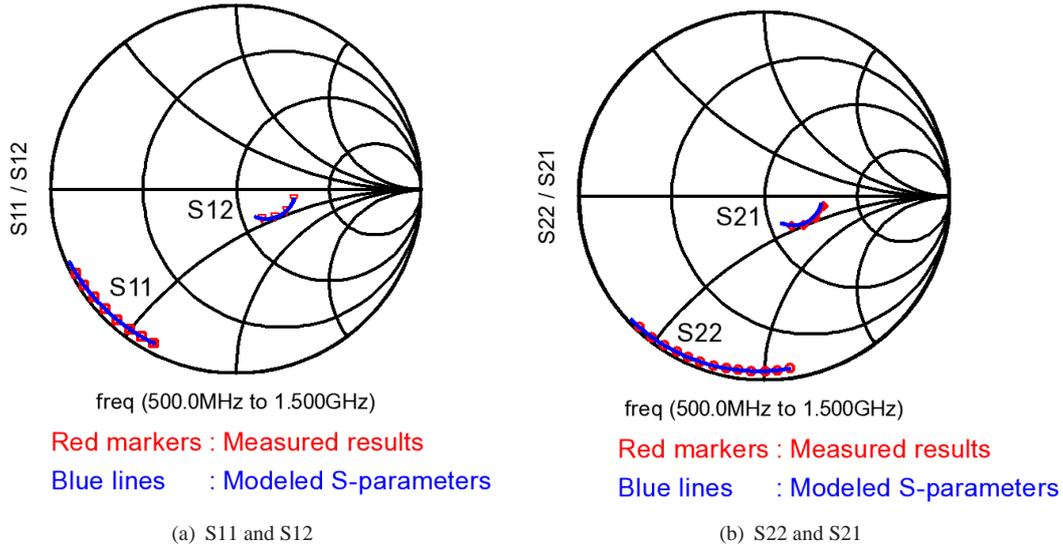
FIGURE 4.5: S-parameters measured by Cadence and modeled S-parameters using extracted model parameters

small-signal model parameters of silicon MOSFETs is described. One can obtain the small-signal model parameters only by S-parameter measurements. Fig.4.4 shows the schematic of the equivalent model used to characterize the small-signal behavior of NMOS transistor. An example is given to extract the small-signal model parameters of extended drain NMOS transistor in CMOS 65nm technology [39]. Table 4.1 shows the extracted parameters. In Fig.4.5, the S-parameters obtained by Cadence and modeled S-parameters using the extracted model parameters are given in Table 4.1 from 0.5 to 1.5 GHz. This demonstrates good accuracy for the technique developed in [38].
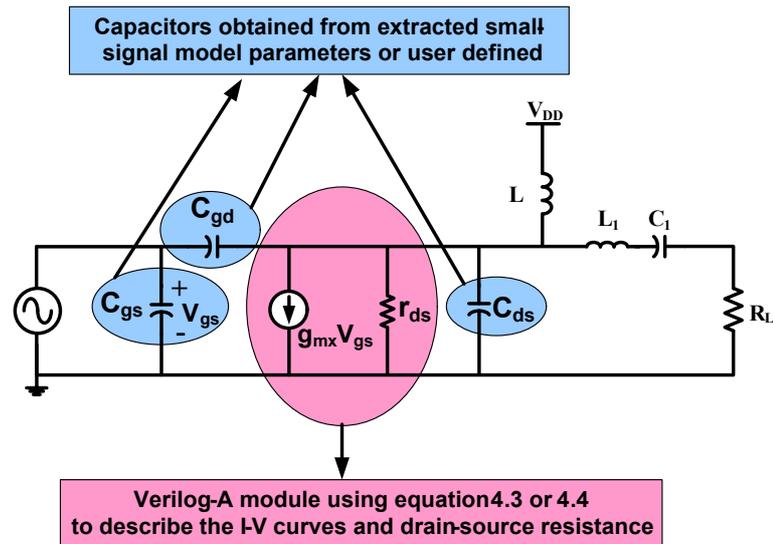
FIGURE 4.6: Numerical model of Class-E power amplifier
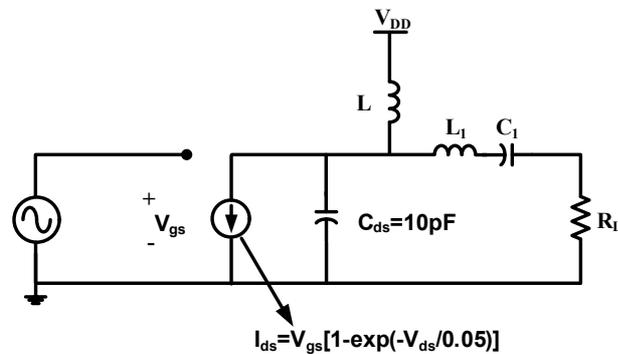
FIGURE 4.7: Simulation model

Fig.4.6 presents the methodology one can use to model a CMOS transistor. A Verilog-A module based upon Eq.4.3 or 4.4 is used to describe the "dc" behavior of the device, and capacitors extracted by [38] or defined by user are used to describe the "ac" behavior of the device.

In the following sections, the I-V curves shown in Fig.4.3 are used to model the DC behavior of the device. For this current source, the ON-resistance R_{ON} at knee voltage V_k=0.05V for V_{gs}=1V is $R_{ON} = V_k/I_D = 0.079\Omega$. In Chapter 3, all the results are obtained for m_{on}=0.005. For comparison purpose, the same m_{on} is used here. Consequently the corresponding total output capacitance at 1GHz is $C = m_{on}/(\omega R_{ON}) = 10pF$. To simplify the model, the C_{gs} and C_{gd} are neglected. Therefore the required drain-source capacitance is 10pF. Fig.4.7 shows the model will be used for investigating the effects of drive signal and linear operation.
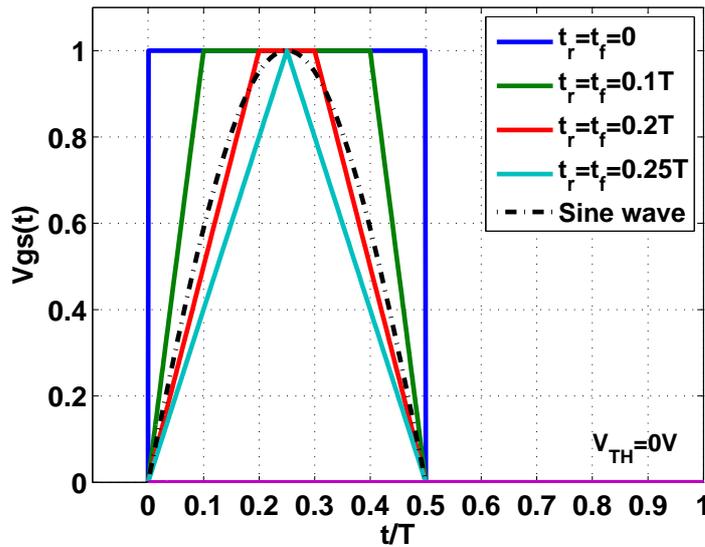
FIGURE 4.8: Test waveforms of drive signal to gate terminal

4.2 Effects of Drive Signal on Class-E Power Amplifier

In this section the effects of drive signal on the performance of Class-E power amplifiers are presented. Fig.4.8 shows five different drive signal waveforms in this experiment: ideal square wave, square wave with rise and fall times[1] of 0.1T, square wave with rise and fall times of 0.2T, triangular wave (t_r=t_f=0.25T), and sinusoidal wave. The duty cycles[2] of these drive signals are all 50%. The effects of these drive signals on the drain efficiency, power-output capability, and K_P are shown in Fig.4.9, and the effects of drive signals on drain-source voltage and drain current waveforms are shown in Fig.4.10 as a function of q.

One can observe that the increase in the rise and fall times leads to the decrease of drain efficiency. However, the drain efficiency is more tolerant of variations of rise and fall times for finite dc-feed inductance than for infinite dc-feed inductance. For example, a 11% drop in drain efficiency can be seen for q = 0.01 (infinite dc-feed inductance) when the rise and fall times increase to 0.25T while only 5% decrease in drain efficiency is found for q = 1.81. The peak power-output capability shifts to a smaller dc-feed inductance (q = 1.61) when the drive signal is a non-ideal square wave. However, the maximum value of K_P is still at q = 1.41 for different rise and fall times. The peak drain-source voltage decreases as the rise and fall times increase. For q = 0.01, the peak drain-source voltage reduces to 3.3V$_{DD}$ but the drain efficiency also reduces. Like drain efficiency, the output power is also more tolerant to the variations of rise and fall times for finite dc-feed inductance than for infinite dc-feed inductance.

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[1]The rise time t_r refers to the time required for the drive signal to change from threshold voltage to the maximum gate voltage. In reverse, fall time t_f is the time required for the drive signal to decrease from the maximum gate voltage to threshold voltage.

[2]The duty cycle is defined as the proportion of time during which the gate-source voltage is larger than the threshold voltage V$_{TH}$.

(a) Drain efficiency

(b) Power-output capability

(c) Peak drain-source voltage

(d) Peak drain current

(e) K_P
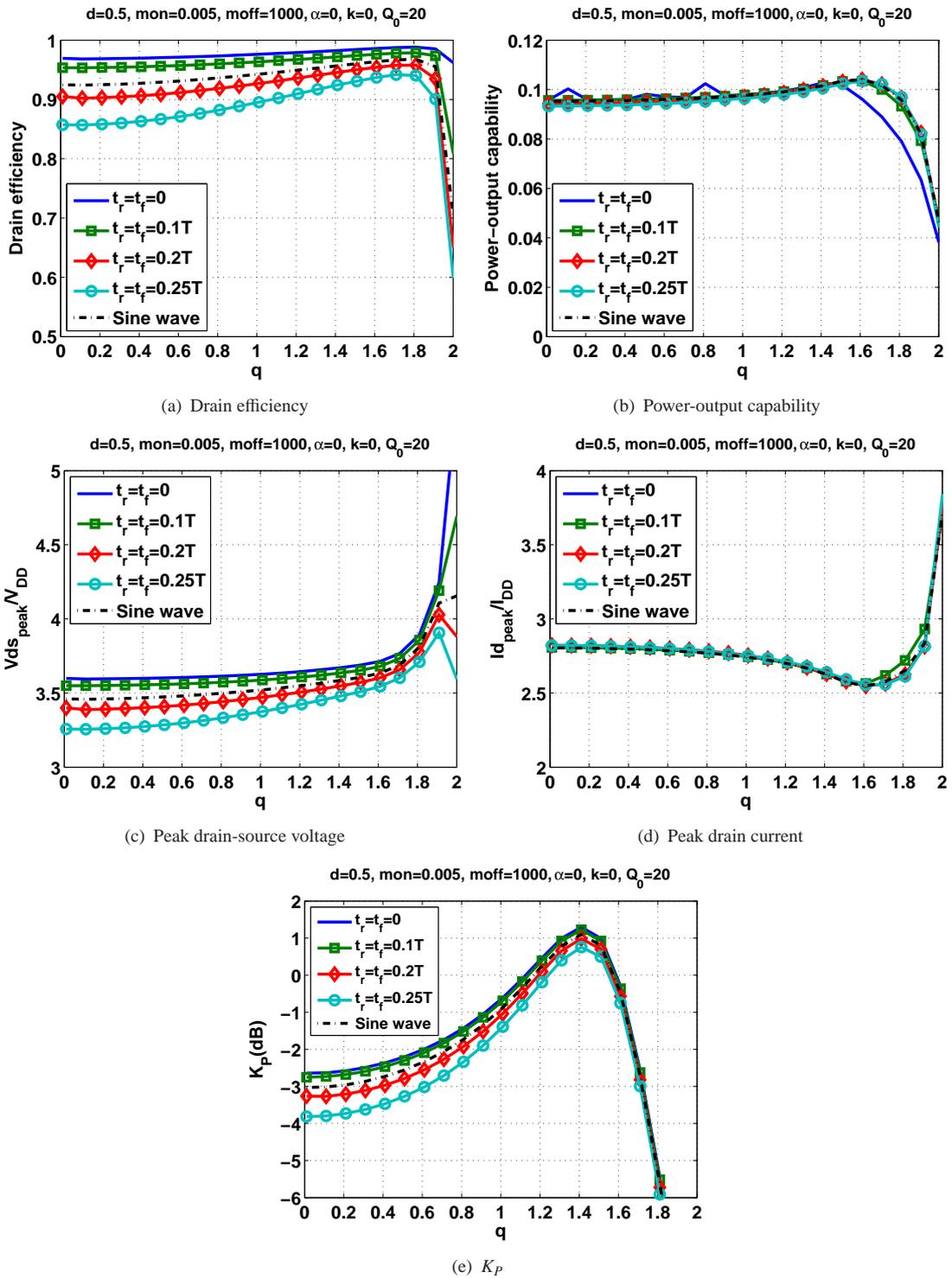
FIGURE 4.9: Effects of drive signal on the performance of Class-E power amplifier
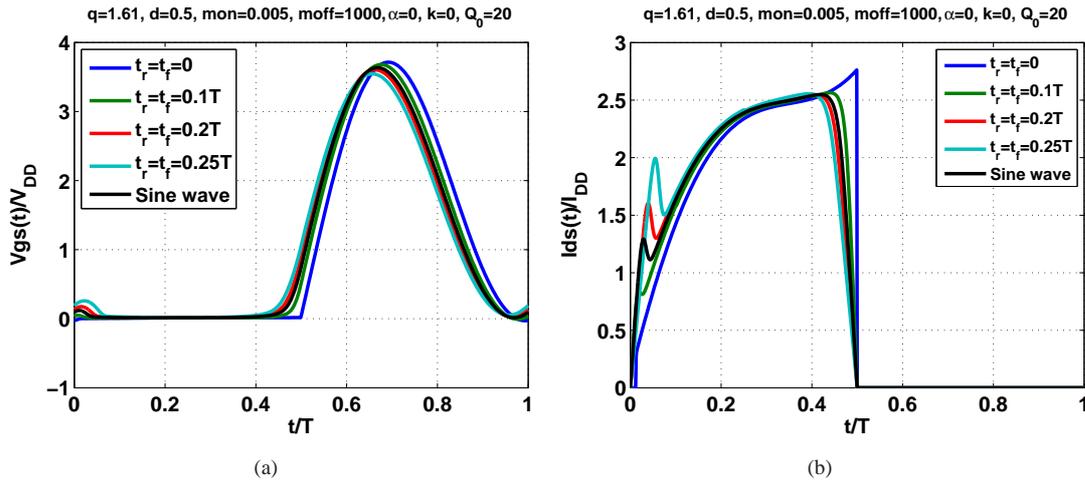
FIGURE 4.10: Drain-source voltage and drain current waveforms as a function of rise and fall time

4.3   Linear Operation of Class-E Power Amplifier

In the above sections, the analyses are focused on switch-mode operation of Class-E power amplifier. The drive signals applied to the Class-E amplifier usually swing to the maximum allowed gate-source voltage sharply to avoid power loss at the transistor. However, the process of the amplitude changes in the drive signal is worth investigating. In this case, the drive signal is a sinusoidal wave based on a DC gate bias voltage, and the amplitude of the drive signal reaches the maximum gate-source voltage gradually and not suddenly. The Class-E power amplifier operates here in linear mode. In this section, the effects of gate bias on linear operation of Class-E amplifier is presented.

For the linear operation, a sinusoidal wave is applied to the gate of the amplifier. The input signal is based upon a certain DC gate bias voltage. The amplitude increases from a very small value to a large value. For the created I-V curves shown in Fig.4.3, the linear input range is from 0 to 1V. Thus the DC gate bias voltage for Class-A operation is 0.5V, and 0V for Class-B operation. For Class-AB operation, the gate bias voltage can be chosen between 0V and 0.5V. Fig.4.11 shows the output power and drain efficiency as a function of input power for $q = 1.41$. One can see that the saturation power and corresponding efficiency for Class-A and Class-B biasing are almost the same, but the efficiency for a same output power (less than saturation power) is quite low for Class-A biasing compared with Class-B biasing. For example, when the amplifier delivers 16dBm output power, the drain efficiency for Class-A is only 10%, but 60% for Class-B biasing. One can get the same conclusion from the drain current and voltage waveforms shown in Fig.4.12. For a same input amplitude, the drain current for Class-B biasing only conducts at the first half of one cycle, but the transistor always conducts current for Class-A biasing. Therefore, the overlap between drain voltage and drain current is smaller for Class-B biasing
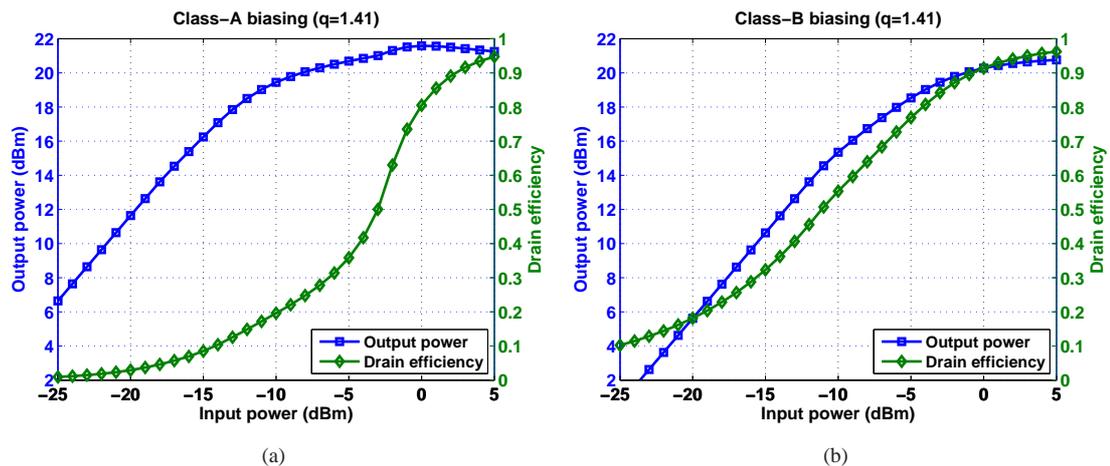
FIGURE 4.11: Output power and drain efficiency as a function of input power for linear operation

than for Class-A biasing, which improves the drain efficiency. Since the created transistor only conducts current when the input signal is larger than 0V, the efficiency for Class-B biasing is still relatively high at 10dB power back-off. However, for the same output power, the input power of Class-B biasing must be 6dB larger than that of Class-A biasing.

Fig.4.13 presents the effects of dc-feed inductance on the performance of Class-E amplifier, which is driven into 1dB compression point for different bias conditions. For comparison purpose, the results of switch-mode operation are shown on the same graphs. One can observe that the drain efficiency and power-output capability have peak values when $q = 0$. The output 1dB compression point and drain efficiency decrease as q increases. At 1dB compression point, the drain efficiency can be improved by shifting biasing voltage to threshold voltage or Class-B mode. The difference of output 1dB compression point between Class-A and Class-B biasing is about 1dB. These results agree with the classical linear amplifier theory. The effects of gate biasing on drain-source voltage and drain current waveforms are shown in Fig.4.14. The figure corresponds to $q = 1.41$ at 1dB compression point. It is apparent that the overlap between current through the transistor and voltage across the transistor is smallest when the amplifier is biased at Class-B mode. One can also observe that the peak drain voltage is more than $3V_{DD}$ at 1dB compression point. It is different from the classical power amplifier theory which claims that the output swing is $2V_{DD}$ for optimum load condition. This is due to that the Class-E load shapes the drain voltage waveform.

4.4 Conclusion

A linear transistor model was created in this chapter by using numerical method in order to analyze the effects of drive signal on the Class-E amplifier and linear operation of Class-E amplifier. In this model, the drain current I_{ds} is a linear function of gate-source voltage V_{gs}. The
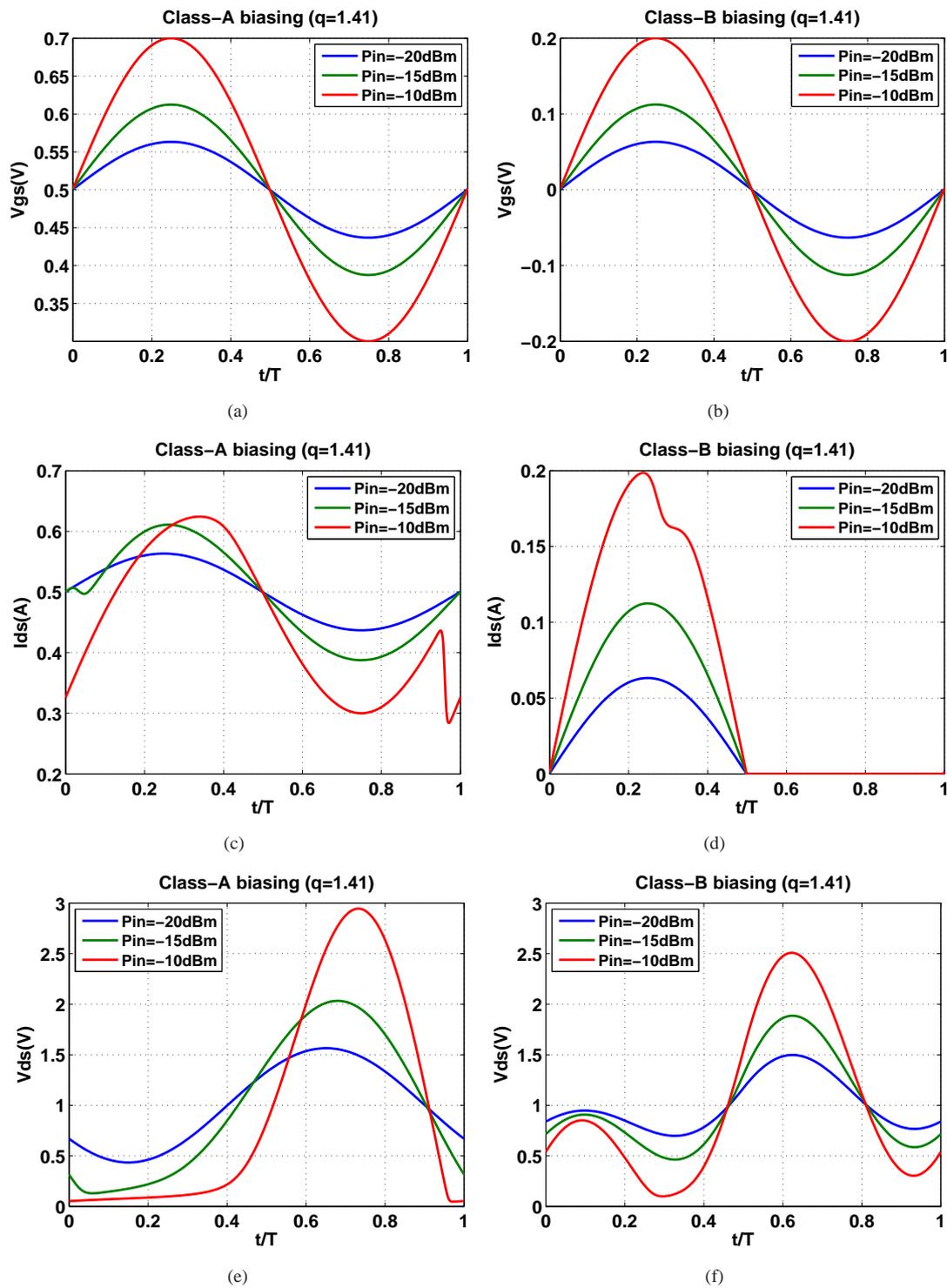
FIGURE 4.12: Voltage and current waveforms of Class-A and B biasing at $q = 1.41$
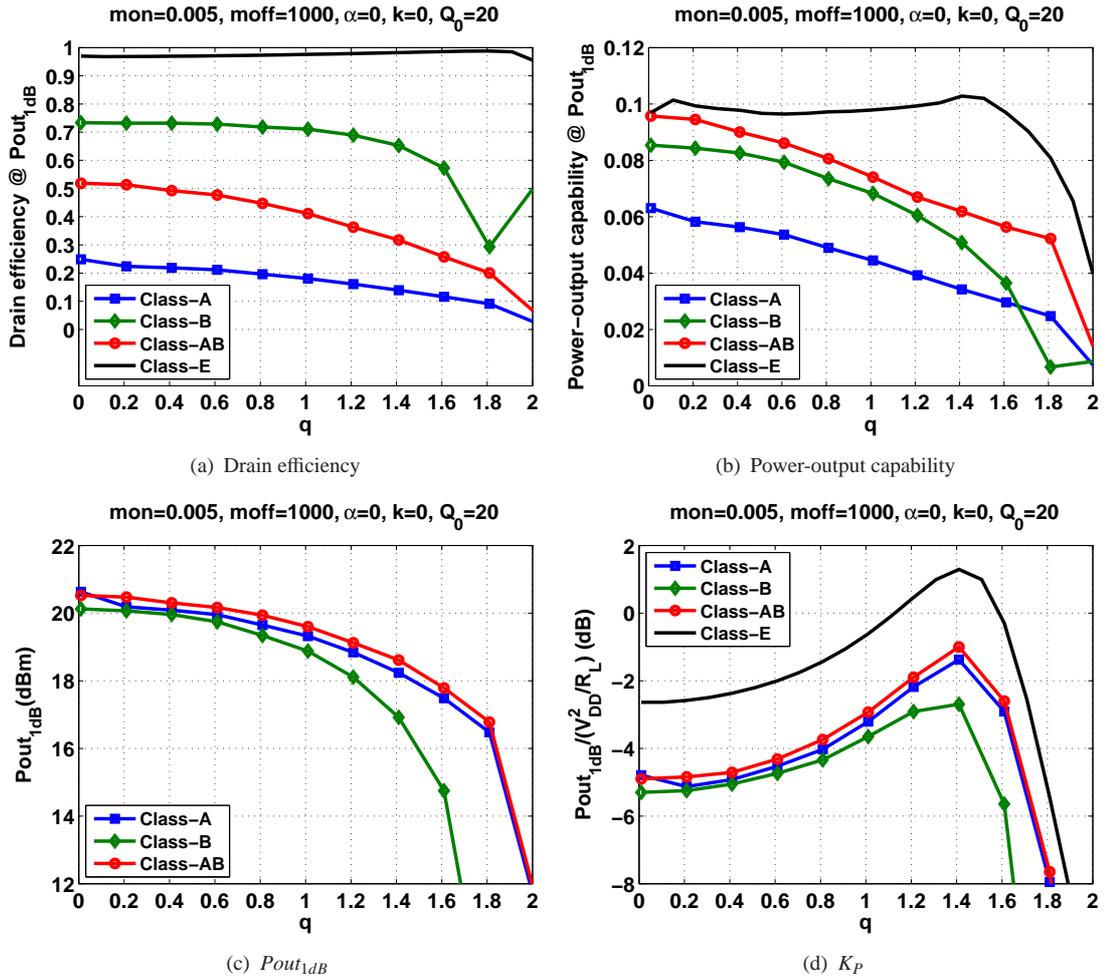
FIGURE 4.13: Effects of dc-feed inductance for Class-E power amplifier at 1dB compression point with different gate bias voltages

transconductance g_m and device capacitance C_{ds} are constants which are independent of gate-source V_{gs} and drain-source voltage V_{ds}. Based upon this transistor model, the effects of rise and fall times of drive signal were discussed. It has been demonstrated that the Class-E power amplifier with finite dc-feed inductance is more tolerant of the variations of drive signal. For the rise and fall times of 25%T, only 5% drop in drain efficiency was found for the PA with finite dc-feed inductance ($q = 1.81$) while 11% drop for the PA with the RF choke. For the Class-E power amplifier operating in linear mode, the DC gate bias voltage is a key design parameter which determines the efficiency, output 1dB compression point and power gain. The efficiency for Class-B biasing is higher, but the output 1dB compression point and power gain of Class-B biasing are smaller than that of Class-A biasing. The trade-off exists between these parameters. Designers should choose a suitable gate bias voltage to satisfy a given specification. The shortcoming of this model is that it is a purely linear model. The non-linearity of transconductance g_m and device capacitances C_{gs}, C_{ds}, C_{gd} are not taken into account. Therefore the linearity of the amplifier and intermodulation performance cannot be estimated directly by this model. In
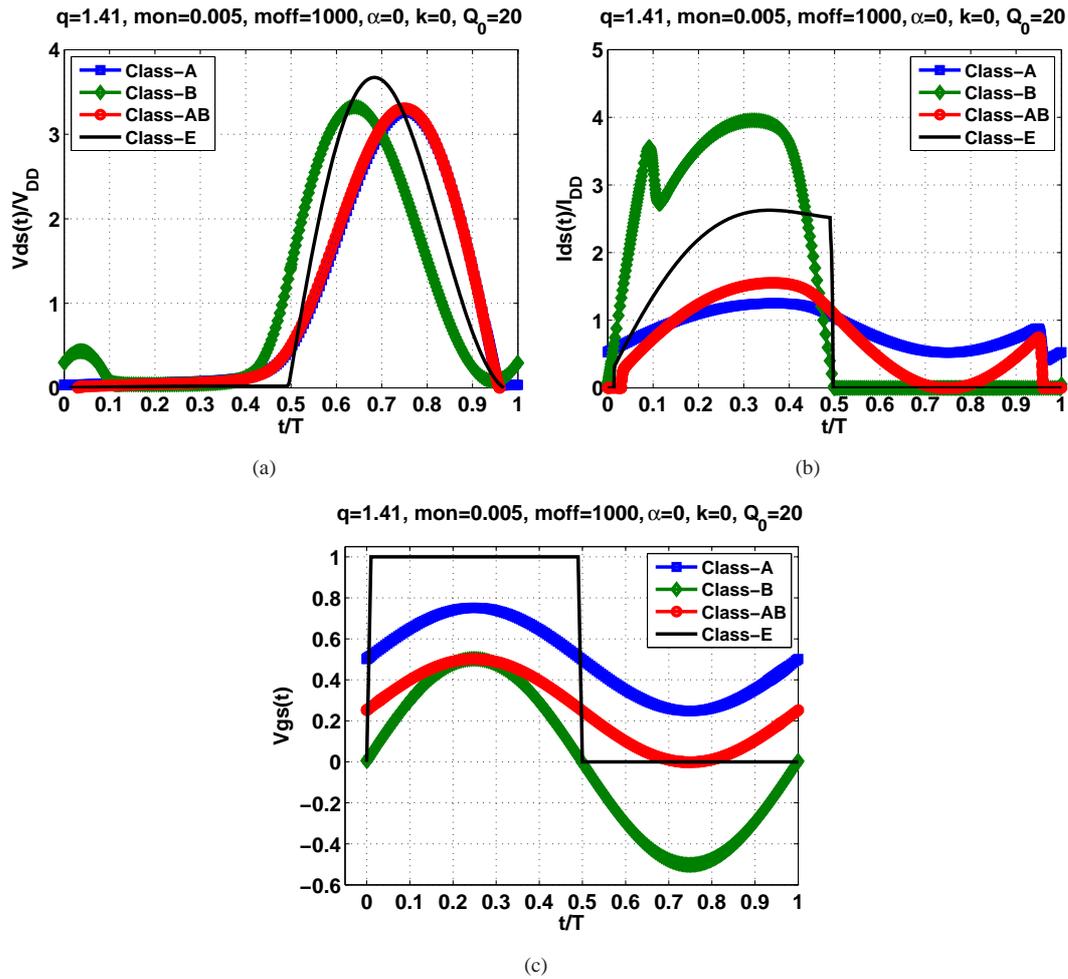
FIGURE 4.14: Waveforms at 1dB compression point for $q = 1.41$

the chapter 5, a real transistor model will be given, and the linearity for a given technology will be analyzed.

Chapter 5

Broadband Class-E Power Amplifier Design Based Upon ED-NMOS Device

In this chapter a broadband Class-E power amplifier was designed in order to verify the results obtained in the previous chapters. The broadband Class-E power amplifier was build with extended-drain NMOS (ED-NMOS) transistors in 65nm CMOS technology [39], which have higher breakdown voltage than the standard transistors. First the switching and linear operation of this device is studied in Section 5.1.1. In Section 5.2 a systematic design approach is applied to design a broadband Class-E power amplifier from 0.65GHz to 1.05GHz. The post-layout simulation results are presented in Section 5.3.

5.1 Analysis of Switching and Linear Operation of ED-NMOS

5.1.1 DC I-V Characteristics and Non-Linear Capacitances of ED-NMOS

In [31] Acar has demonstrated that the drain efficiency is limited by transistor technology. Moreover, the design set K is as a function of transistor technology parameters m_{on} and m_{off}. Therefore it is necessary to know the transistor technology parameters in advanced. The transistor technology parameters consist of the ON-resistance, OFF-resistance, and the total output capacitance seen into drain node. The ON-resistance and OFF-resistance can be obtained by measuring the DC I-V characteristics. The output capacitance can be acquired by measuring the S-parameters for different gate-source and drain-source voltages. Unfortunately the PCB for S-parameters measurements was not ready when I started to design the power amplifier. Hence the output capacitance is obtained by simulating the device in Cadence, then extracting the small-signal model.

FIGURE 5.1: Schematics of active device

FIGURE 5.2: Layout of active device

The active device used in this design is an ED-NMOS transistor with a drive inverter in 65nm CMOS technology. It was designed by M. Acar. Fig. 5.1 shows the schematics of active device, and the layout is shown in Fig. 5.2.

To measure DC I-V characteristics, a test setup was built up shown in Fig. 5.3. The die was mounted on a test PCB. The die and PCB was connected via bondwires which are not shown in the figure. The cable resistance of supply cable is 0.1Ω. During the test, the gate biasing VBN and VBP for the NMOS and PMOS of inverter are connected together. When the VBN, VBP and the supply voltage $VDD1$ of inverter are fixed, the gate bias voltage for the ED-NMOS is also fixed. Therefore the gate bias voltage of ED-NMOS is determined by inverter. Hence the DC I-V characteristics of the ED-NMOS can be obtained by setting different supply voltage

FIGURE 5.3: DC I-V measurement setup

VDD2 for V_{ds} of the ED-NMOS and different VDD1, VBN and VBP for V_{gs} of the ED-NMOS. Fig. 5.4 shows the measured results for VBN=VBP=0V. Since VBN=VBP=0V, the NMOS of inverter is always opened and the PMOS of inverter is always closed, the output node of inverter or the gate voltage of ED-NMOS is always equal to supply voltage VDD1. In Fig. 5.3, two parasitic source resistors R_{S1} and R_{S2} are added to the sources of inverter and ED-NMOS to take into account parasitic resistance of metal lines of layout. In Fig. 5.4, the simulation results obtained by using Cadence transistor model of ED-NMOS are also shown. The cable losses are taken into account in the simulation. To better model the chip, av-extraction was done in Cadence to extract the parasitic capacitances and resistances. The extraction shows that there is 0.02Ω parasitic resistance at the source node. However, the simulated DC I-V curves shown in Fig. 5.4(a) is larger than the measured results. This may be due to the error between the transistor library model and the real fabricated transistor. One can tune the source resistance R_{S2} to make the simulation results close to the measured ones. Finally when R_{S2}=0.14Ω, the simulation results are close to measured results which is shown in Fig. 5.4(b). Besides the transistor model in Cadence, the DC I-V curves can also be modeled by polynomial functions that were presented in Section 4.1. Fig. 4.2 shows the modeled I-V curves by 6th-order polynomial functions.

The av-extraction in Cadence can extract the parasitic capacitances resulting from the metal lines of layout. Fig. 5.5 shows the parasitic capacitances (red) extracted by Cadence. In principle, S-parameter measurements were supposed to be done to extract the actual device capacitances. But since there is no pad on the die for probe measurement, we did not measure the actual S-parameters. The device capacitances are estimated by Cadence simulation using the same method mentioned in [38]. Since the efficiency is mainly related with final stage, only the

FIGURE 5.4: Measured DC I-V curves for VBN=VBP=0V

FIGURE 5.5: Schematics of active device with parasitic capacitance (red) extracted by Cadence

capacitances of ED-NMOS are extracted. Fig. 5.6 shows the non-linear capacitances C_{ds}, C_{gd}, and C_{gs} as a function of drain-source voltage V_{ds} for different gate bias voltage V_{gs}. From the figure, one can observe that the non-linear capacitances C_{ds} and C_{gd} for different V_{gs} are almost overlaid on each other. The capacitances C_{ds} and C_{gd} can be expressed as:

$$C(v_{ds}) = \frac{C_{j0}}{(1 + v_{ds}/V_{bi})^n} \tag{5.1}$$

where C_{j0} is the capacitance at zero voltage, V_{bi} is built-in potential, and n is the grading co-efficient of the pn-junction [40]. For C_{ds}, $C_{j0} = 3.8pF$, $V_{bi} = 0.2V$, and $n = 0.2$. For C_{gd}, $C_{j0} = 5.5pF$, $V_{bi} = 0.2V$, and $n = 0.2$. For the nonlinear gate-source capacitance C_{gs}, 15th-order polynomial functions are used to fit the curves. Fig. 5.7 summarizes the transistor model that will be used.

(a)

(b)

(c)
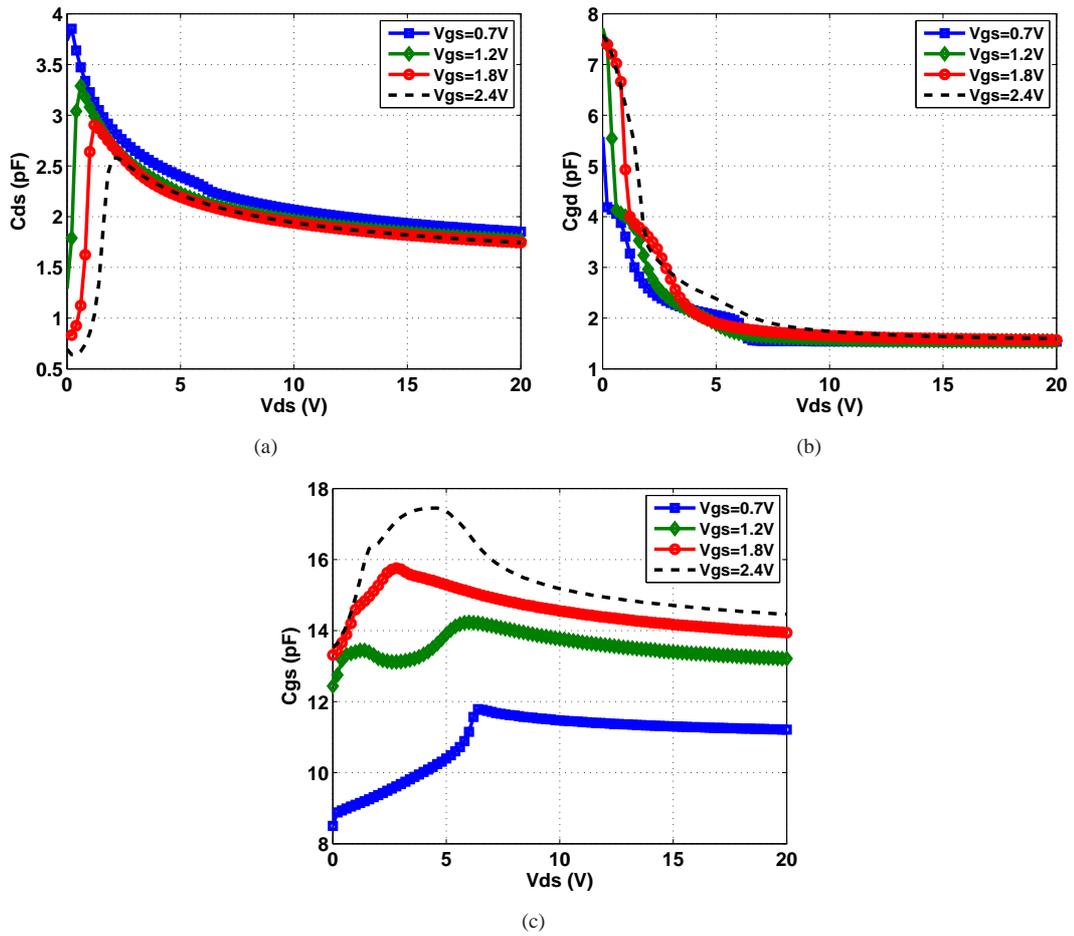
FIGURE 5.6: ED-NMOS device capacitances obtained by Cadence simulation for different gate bias voltage V_{gs}: (a)C_{ds}, (b)C_{gd}, (c)C_{gs}.
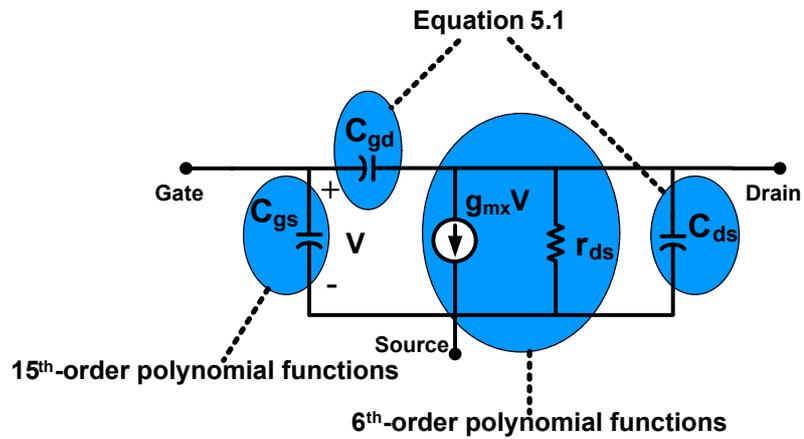
FIGURE 5.7: Synthesized transistor model
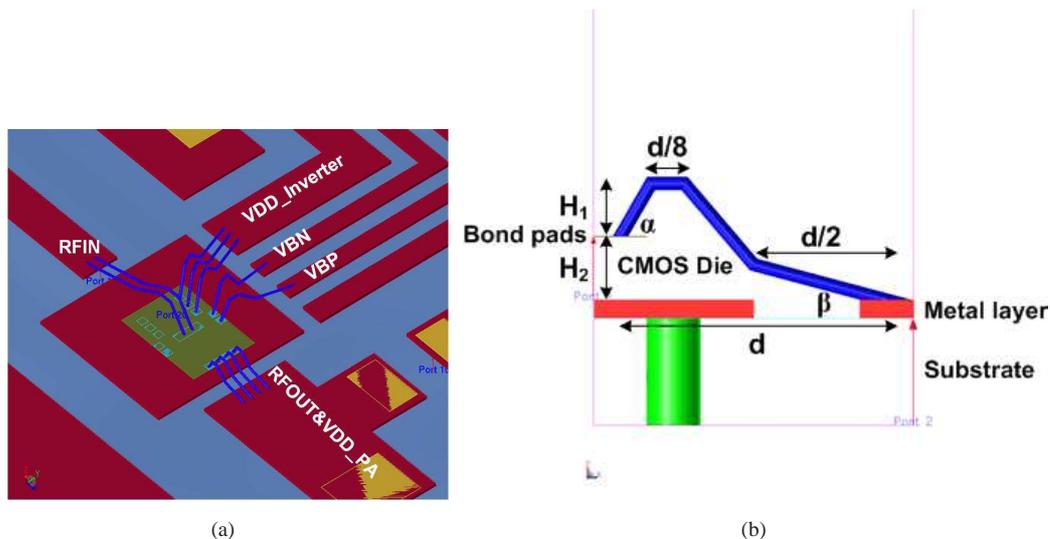
FIGURE 5.8: Bondwires illustrations
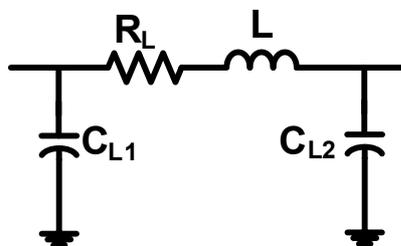
FIGURE 5.9: Bondwires equivalent circuit

5.1.2   Bondwires Simulation

Besides modeling of the device itself, the bondwires linking the die and PCB should be taken into account. Fig.5.8 shows the distributions of bondwires for this die: four bondwires connecting the drain terminal of ED-NMOS to PCB, two bondwires for the RFIN and PCB, three bondwires for power supply of inverter, one bondwire for each of gate bias of NMOS and PMOS of inverter, and six short bondwires for source to ground. A 3D model shown in Fig. 5.8(b) was built in ADS-EMDS to simulate the inductance and parasitic resistance and capacitance of the bondwires. In the model, the projection length d, the height H_1 and H_2, and angles α and β have to be defined. Since the rough dimension of the PCB is given, the approximate projection length d could be obtained. However, from the experience, the height H_1 and angles α and β are difficult to control in practice. Thus only estimated values are given for these parameters. For all the bondwires, we assumed $\alpha = 60°$, $\beta = 15°$, and $H_1 \approx 0.2d$. The projection length d is shown in Table5.1. The equivalent circuit of bondwires is shown in Fig.5.9 which consists of bondwire inductance L, parasitic series resistance R_L, and parasitic capacitances C_{L1} and C_{L2} to ground (e.g., bondwire capacitance and bond pads). By S-parameter simulation, the component values can be obtained. Table5.1 shows the component values for different bondwires at 1GHz. In the following sections, the simulation model takes into account the effects of the bondwires.

TABLE 5.1: Bondwire equivalent inductance and parasitic resistance and capacitance at 1GHz

	d (mm)	H_1 (mm)	N	L (nH)	R_L (Ω)	C_{L1} (fP)	C_{L2} (fP)
Drain-PCB (L_{B1})	0.5	0.1	4	0.24	0.05	16.9	25.7
Source-PCB (L_{B2})	0.4	0.08	6	0.07	0.02	8.8	50.0
RFIN-PCB (L_{B3})	1.4	0.3	2	0.93	0.21	22.0	38.4
VBN/VBP-PCB (L_{B4})	0.9	0.2	1	0.80	0.19	15.0	28.1
VDD1-PCB (L_{B5})	1.0	0.2	3	0.56	0.10	23.4	34.0

5.1.3   Switch-Mode Operation of ED-NMOS

For this transistor, the measured ON-resistance for V_{gs} = 2.2V is equal to 0.76Ω. The simulated average output capacitance ($C_{ds} + C_{gd}$) is 4.14pF. Thus the technology parameter $m_{on} = \omega CR_{ON}$ at 1GHz is equal to 0.02. The breakdown drain-source voltage BV_{ds} of ED-NMOS transistor is about 15V. To relieve the device stress, a lower breakdown drain-source voltage BV_{ds} = 12V is used in the simulation. Since the peak drain voltage is usually three to four times of supply voltage, a supply voltage of 4V was chosen at the beginning. Therefore, the switch-mode performance of this synthesized ED-NMOS transistor as a function of q can be investigated. Fig. 5.10 shows the simulation results for Q_0 = 5 at 1.0GHz. From the figures, one can observe that the maximum drain efficiency of 93% is obtained at $q \approx 1.7$, but the maximum output power of about 30dBm is obtained at infinite dc-feed inductance. The peak drain voltage for V_{DD} = 4V is beyond BV_{ds} = 12V. To protect the device, the peak drain voltage must be reduced. One can derease the supply voltage to lower the peak drain voltage, but the output power will be decreased at the same time. In this case, variable-voltage operation is a good choice. For the same supply voltage, the peak drain voltage can be decreased by increasing parameter α. For example, the peak drain voltage decreases from 3.7V_{DD} to 3V_{DD} when the α increases from 0 to 1. The degradation of drain efficiency is only 2%.

For comparison purpose, the results obtained by ED-NMOS Cadence library model are also shown on the same graph. The results are very close to that of the synthesized transistor model.

5.1.4   Linear Operation of ED-NMOS

In the previous section, the switch-mode characteristics of ED-NMOS have been investigated. The linearity of ED-NMOS will be discussed in this section. Because of the convergence problem of the synthesized transistor model, the Cadence library model was used here to investigate the power amplifier. The transistor is biased at V_{gs} = 1.55V, V_{gs} = 1.2V, and V_{gs} = 0.7V, corresponding to Class-A, Class-AB, and Class-B modes respectively. A single-tone sinusoidal signal was fed into the gate of the transistor. Fig. 5.11 shows the large signal performance over power sweep at 1GHz for four different loads (q = 0.01, q = 1.21, q = 1.41 and q = 1.61).
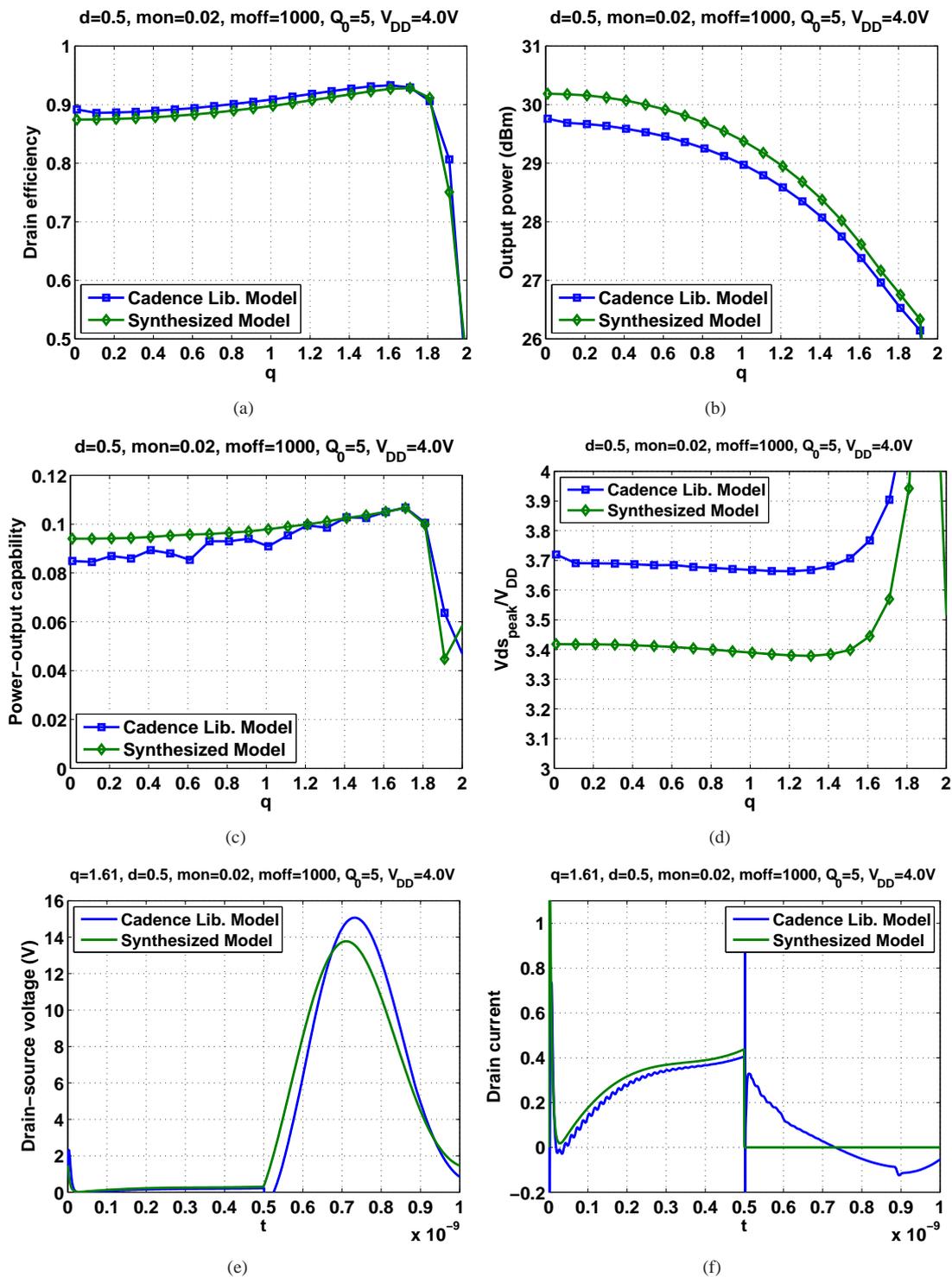
FIGURE 5.10: Switch-mode performance of ED-NMOS using synthesized model
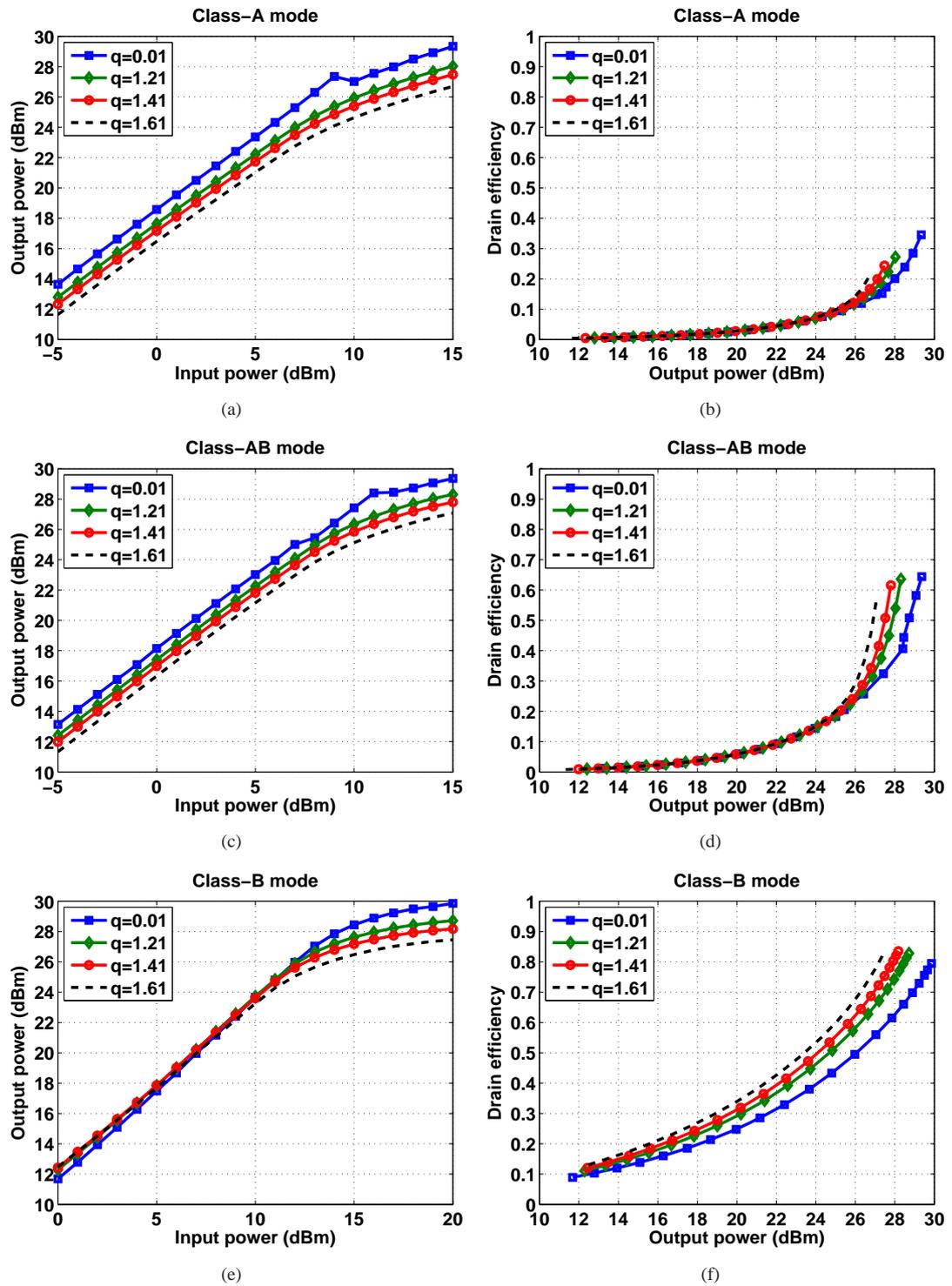
FIGURE 5.11: Large signal performance over power sweep at 1GHz for different gate bias and q

It is apparent that the output power of $q = 0.01$ is about 0.5-1dB larger than that of $q \geq 1.21$ for the same input signal. For Class-A and Class-AB modes, the dc-feed inductance has little effect on the drain efficiency when output power is below the saturation power. The efficiency is dependent of the dc-feed inductance only when the power amplifier delivers the power that is near the saturation power. This is due to that the transistor is always turned on or conducting current for a small input signal when biasing at Class-A or Class-AB mode. The efficiency is higher for large q than for small q. One can also find that the efficiency is very sensitive to gate bias voltage. For the same output power, (i.e. 26dBm), the efficiency for Class-B mode is 35% larger than that of Class-AB, and 55% larger than that of Class-A, which is expected from the classical power amplifier theory.

Fig. 5.12 shows the drain efficiency, output 1dB compression point, power-output capability and power gain as a function of q when the amplifier is driven into 1dB compression point. It can be observed that the maximum output 1dB compression point is obtained at $q = 0.01$ or RF choke. The output 1dB compression point decreases as q increases. The output 1dB compression point of Class-B is about 2dB larger than that of Class-A. For the Class-E load condition, the Class-B bias always shows better drain efficiency and power-output capability. One can also observe that the power gain of Class-B is about 6dB small than that of Class-A or Class-AB for $q = 0.01$. The power gain of Class-B is very tolerant of q, but that of Class-A or Class-AB decreases as q increases.

The intermodulation distortion characteristic is an important parameter to evaluate the linearity of an amplifier. When applying a two-tone signal with equal amplitude to the amplifier, the intermodulation products can be found in the output spectrum. Fig. 5.13 shows the third-order intermodulation distortion (IMD3) as a function of total two-tone output power. For the power amplifier, we hope the device can deliver high output power with good linearity. In Fig.5.13, one can find that for $P_{out} = 25dBm$ the smallest IMD3 of -35dBc can be obtained when the device is biased at $V_{gs} = 1.2V$ with RF choke. As the gate bias voltage V_{gs} moves from the Class-A mode to Class-B mode, the IMD3 for the amplifier with the RF choke degrades gradually. When the device is biased at Class-B mode, the amplifier shows better IMD3 for finite dc-feed inductance than for RF choke. For example, IMD3 is equal to -30dBc for $P_{out} = 25dBm$ when the amplifier is biased at 0.7V for $q = 1.21$, which is about 5dB worse than that of best value obtained at $V_{gs} = 1.2V$, but the efficiency is 20% higher than that of amplifier biased at 0.7V with RF choke. From the figure, the output third-order intercept point (OIP3) can be calculated. When $q = 0.01$, the OIP3 for Class-A is about 38dBm, while 39.5dBm for Class-AB. It is about 10 dB more than output 1dB compression point of Class-A and Class-AB. That agrees very well with the classical theory of OIP3 and P1dB, which is OIP3=P1dB+9.6dB. For the Class-B, the OIP3 is about 37dBm when $q = 1.21$, which is only 5dB larger than P1dB.
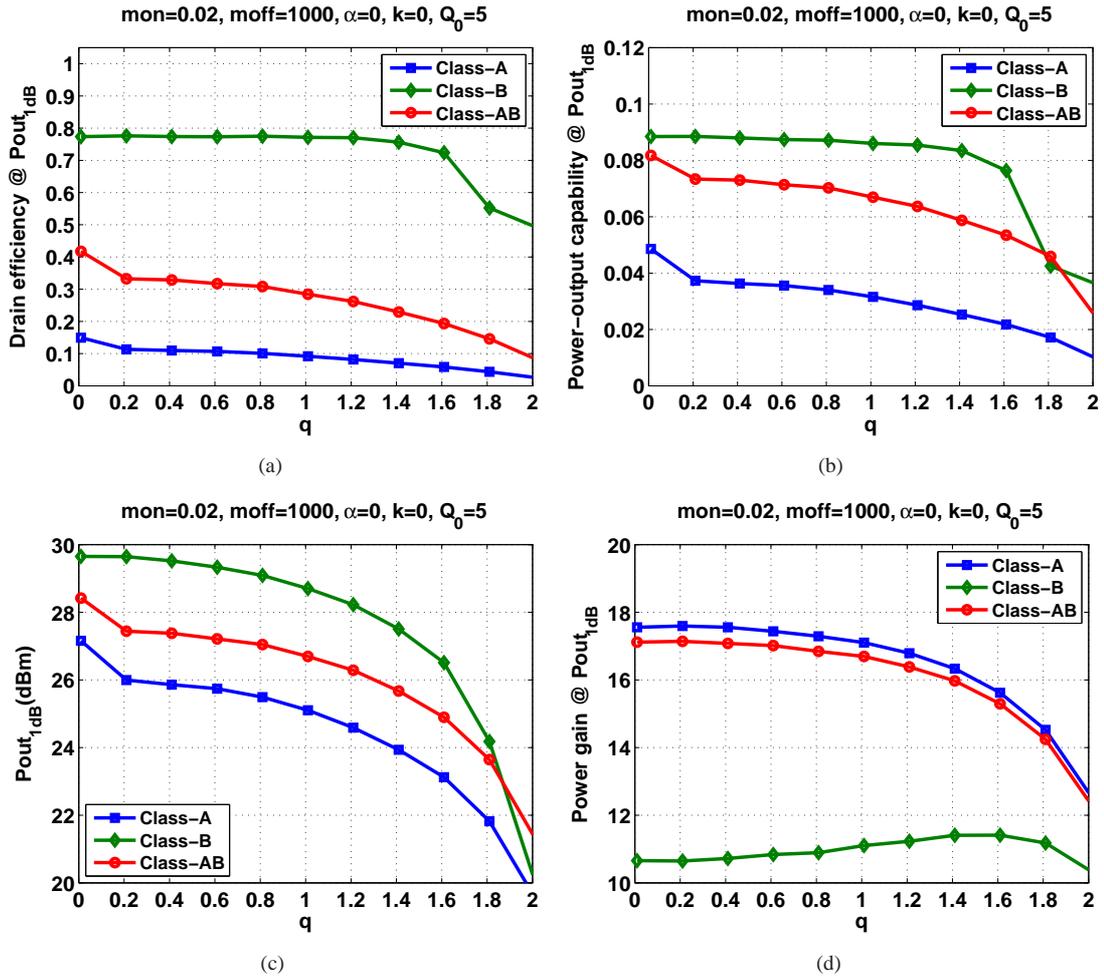
FIGURE 5.12: Simulated drain efficiency, power-output capability, 1dB compression point and power gain versus q for Class-A,AB,and B biases.

From above figures, one can conclude that to maintain high efficiency and high linearity at high output power for this device (ED-NMOS), the amplifier should be biased at Class-B mode with finite dc-feed inductance.

5.2   Broadband Class-E Power Amplifier Design

In this section, the systematic design approach for broadband Class-E power amplifier will be described. The design approach is mainly divided into two parts: optimum load design at a single frequency and broadband output load network design. The specification for the final broadband Class-E power amplifier is shown in Table 5.2.
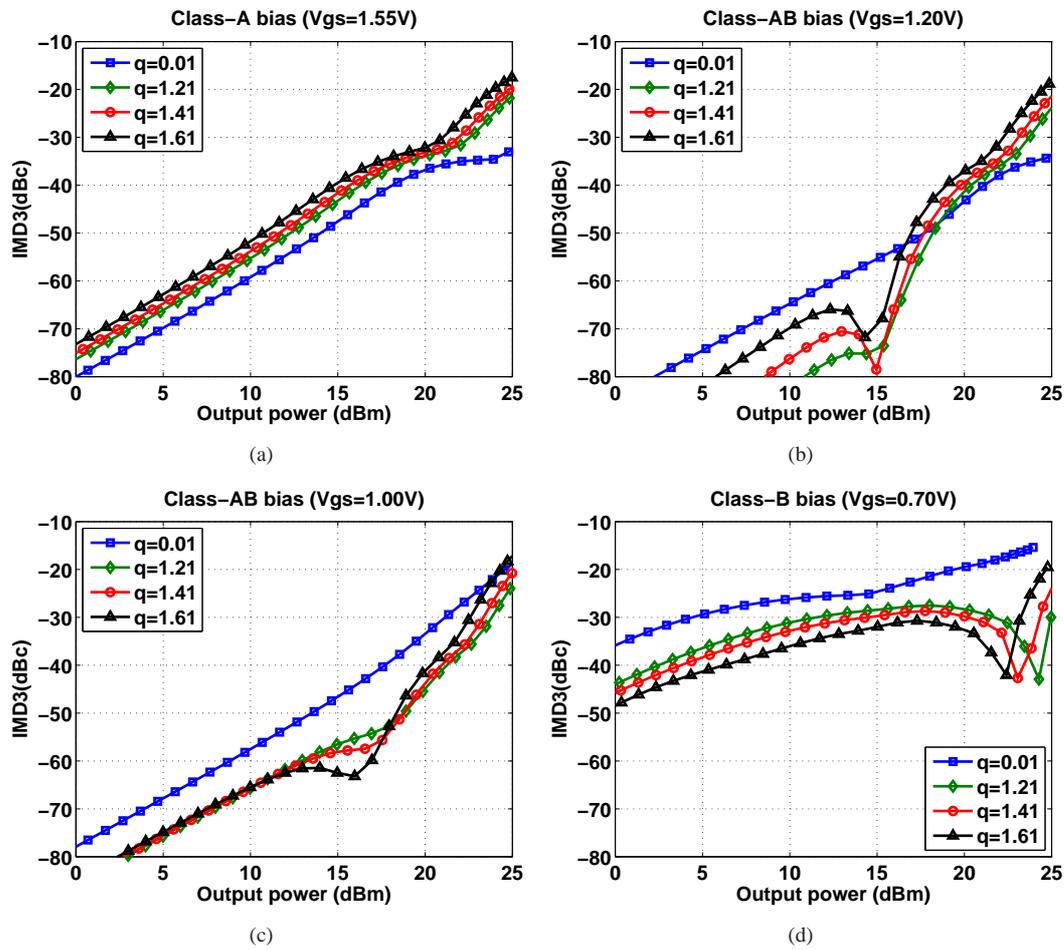
FIGURE 5.13: 3rd-order intermodulation distortion as a function of output power for different q at $f_0 = 1GHz$ with $\Delta f = 100kHz$.

TABLE 5.2: Specifications for broadband Class-E power amplifier

Specification	Target value
Operation frequency	650MHz-1050MHz
Output Power	$\geq 30dBm$
Output power flatness	$\leq 3dB$
Drain efficiency	$\geq 70\%$
Power added efficiency	$\geq 60\%$
Power gain	$\geq 20dB$

5.2.1 Optimum Load Design

First, an optimum load will be found at a single frequency. The power amplifier with this optimum load can satisfy the required specifications given in Table 5.2. The detailed steps are described as follows.

- Step 1: Calculate the technology parameter $m_{on} = \omega C R_{ON}$ and $m_{off} = \omega C R_{OFF}$.

In Section 5.1.3, we have known that the average total output capacitance C is 4.14pF and ON-resistance R_{ON} is 0.75Ω. Since the technology parameter m_{on} determines the maximum value of theoretical drain efficiency, it is wise to predict the worst theoretical drain efficiency this device can obtain. Because the m_{on} is proportional to frequency, the maximum m_{on} is obtained at the maximum operating frequency. For this design, the maximum operating frequency is about 1GHz. Thus the maximum m_{on} is equal to 0.02. The minimum m_{off} is equal to 300 corresponding to $R_{OFF} = 10k\Omega$.

- Step 2: Calculate the duty-cycle d of the drive signal.

The device used in this design includes an inverter which is used to drive the final stage. The simulated output signal waveform of the inverter at 1GHz is shown in Fig. 5.14. For the nominal operation, the gate bias voltages for both NMOS and PMOS are 1.2V, and the supply voltage is 2.4V. Since the threshold voltage of ED-NMOS is about 0.7V, the device can be regarded in an active state when $V_{gs} > 0.7V$. Thus the duty-cycle is defined as the ratio of time interval of $V_{gs} > 0.7V$ to one period. From the figure, one can observe that the duty-cycle d is 56%, the rise time t_r (from 0.7V to 2.1V) is 18%, and the fall time t_f (from 2.1V to 0.7V) is 20%.

- Step 3: Calculate the design set K in Maple based upon the input parameters m_{on}, m_{off}, d, ω, V_{DD}, q, α, and k by analytical approach.

The input parameters m_{on}, m_{off}, and d are determined by the device itself and the external drive signal. Generally, $\omega = 1$ and $V_{DD} = 1$. The parameter q, α, and k are user defined. The efficiency, output power, and drain voltage and current waveforms are dependent on these parameters. User can tune these parameters to meet a specific requirement. Usually, α and k are set to zero at the beginning so that the amplifier will operate at optimum Class-E condition (zero-voltage switching and zero-slope switching). Then one can sweep q to obtain the design set K.

Inverter output signal at 1GHz (V_{DD}=2.4V, VBN=VBP=1.2V)
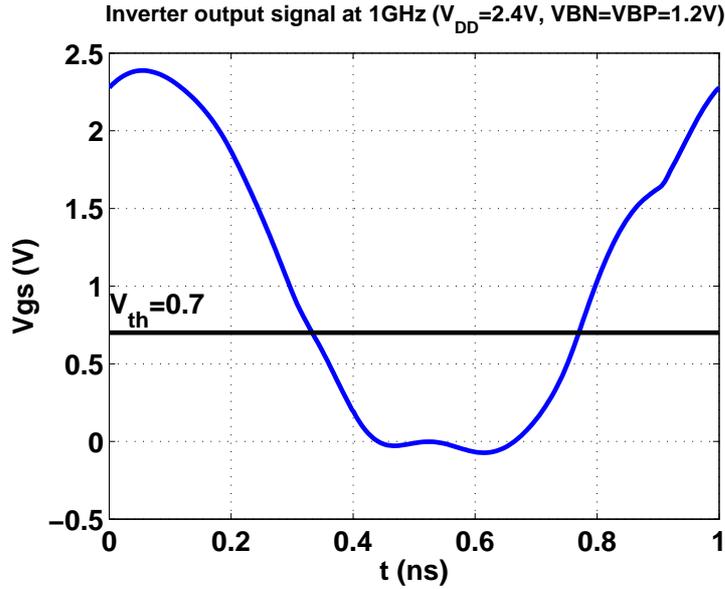
FIGURE 5.14: Simulated inverter output signal at 1GHz

- Step 4: Calculate the supply voltage V_{DD}, load resistance R_L and passive components L, L_1, C_1 based upon the design set K, loaded quality factor Q_0, and desired output power P_{OUT}.

Since the total output capacitance C and design set K_c have been obtained in step 1 and 3, the load resistance can be found from Eq.3.64

$$R_L = \frac{K_C}{\omega C}. \tag{5.2}$$

The supply voltage can be obtained by

$$V_{DD} = \sqrt{\frac{K_C}{K_L} \frac{P_{OUT}}{\omega C}}. \tag{5.3}$$

The passive component values L, L_1, and C_1 are found in a way similar to the example shown in Section 3.2.1. The desired output power for this design is 1W or 30dBm. In Section 4.2, the effects of non-ideal drive signal on the output power and efficiency have already been discussed. For the drive signal of this device, the rise and fall times are about 20%. In Fig.4.9(e), one can observe that the ouput power for 20% rise and fall times is about 1dB smaller than for ideal square wave signal. Accounting this effect, the output power in Eq.5.3 shoule be at least 1dB larger than the designed output power. For this design, $P_{OUT} = 31dBm$. Fig.5.15 shows the calculated supply voltage V_{DD} and load resistance R_L as a function of q. One can observe that for finite dc-feed inductance the required load resistance is larger than that for RF choke. This relieves the difficulty in the load resistance design.
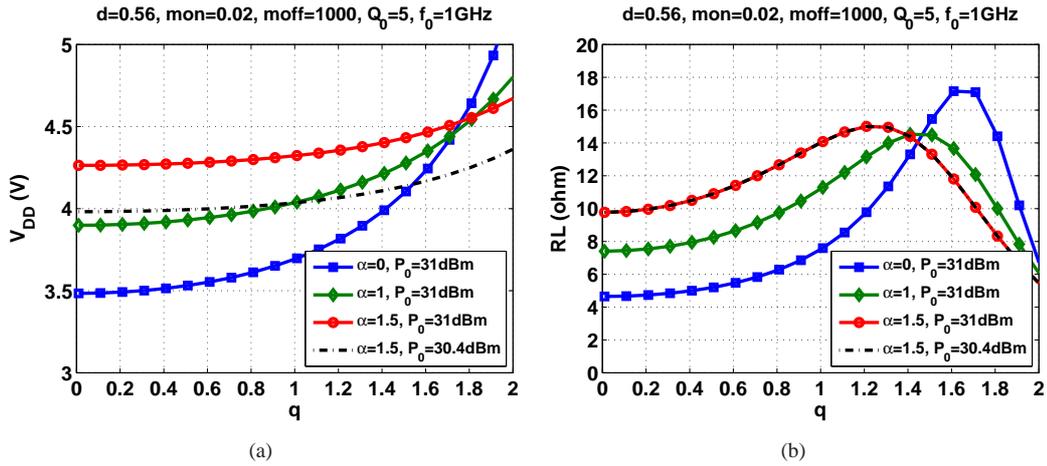
FIGURE 5.15: Calculated supply voltage and load resistance for P_{out}=31dBm

- Step 5: Substitute the calculated supply voltage, load resistance, passive component values into the Class-E circuit in Cadence and simulate the circuit to evaluate the performance of the amplifier for different load impedances.

Fig. 5.16 shows the drain efficiency, output power, power-output capability, and maximum drain voltage and current as a function of q. It is apparent that the output power for $\alpha = 0$ is very near 30dBm that agrees very well with what we predicted in step 4. The peak drain-source voltage for $\alpha = 0$ is about $4V_{DD}$ which is also equal to theory value (i.e., $4V_{DD}$ for $d = 56\%$).

- Step 6: Make decision based upon the simulation results.

To assure a reasonable device life time, the device stress should be considered firstly. If the peak drain current is larger than the allowed maximum drain current, it means that the device cannot deliver the desired current. One has to reduce the desired output power to decrease the peak current. If the peak drain-source voltage is larger than the breakdown voltage, one can decrease it by modifying the amplifier operation mode from the optimum operation to sub-optimum operation. For example, one can increase the switch voltage at the moment the switch is closed by increasing the parameter α. The absolute value of peak drain-source voltage for $\alpha = 0$ shown in Fig. 5.16(e) is larger than breakdown voltage $BV_{ds} = 12V$. Thus we can increase α to decrease the peak drain-source voltage. On the same figure, the performance of the amplifier for $\alpha = 1$ and $\alpha = 1.5$ is shown. The drain-source voltage and drain current waveforms are shown in Fig. 5.17. The increase of switching voltage at the moment the switch is closed is very apparent in the figure. One can find that the peak drain-source voltage has decreased to $2.7V_{DD}$, but the absolute value is still larger than 12V. In this case, one has to adjust the desired output power level to decrease the supply voltage. Here, we decreased the output power from 30dBm to 29.4dBm, thus the output power in Eq.5.3 will be reduced to
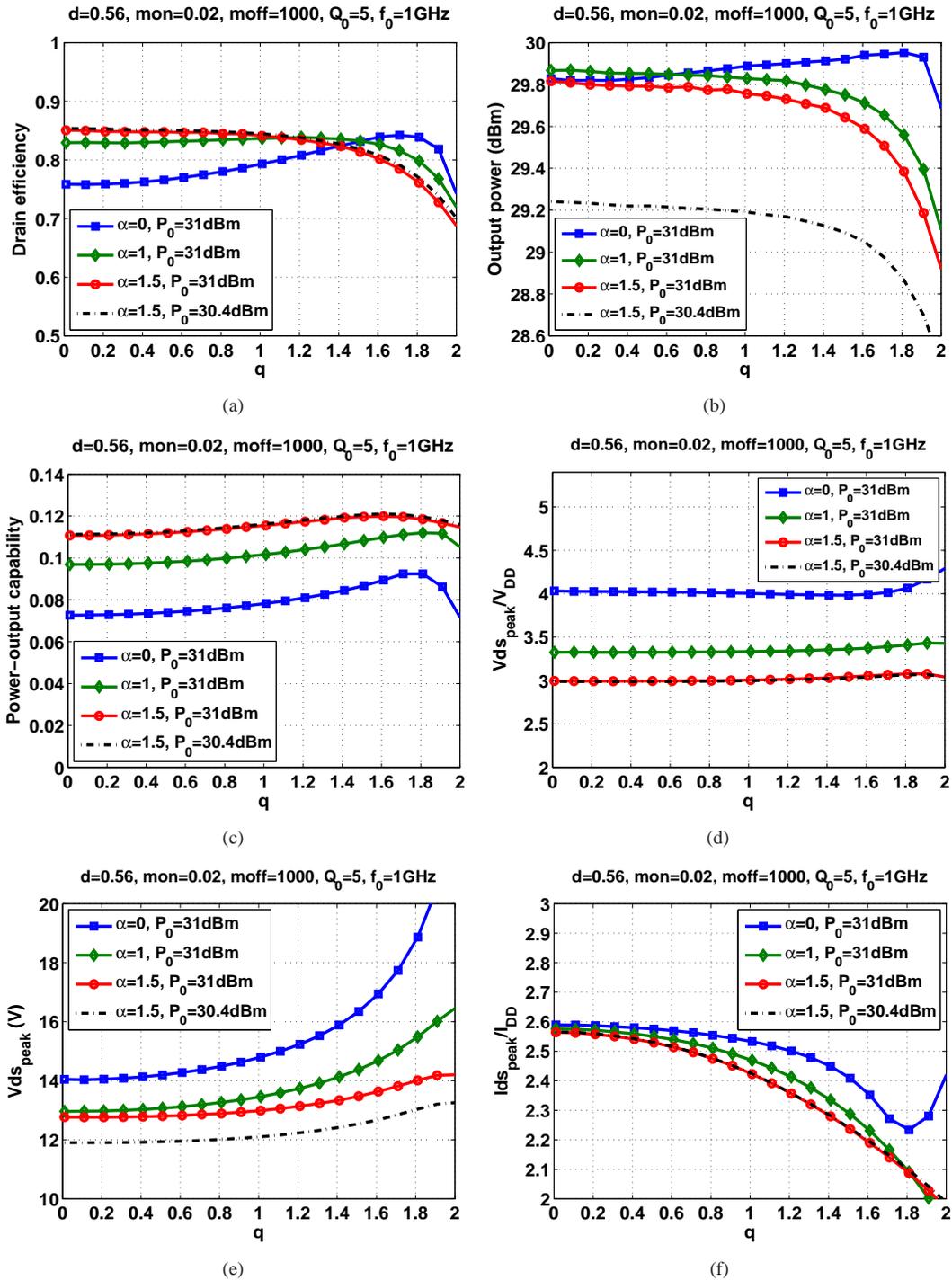
FIGURE 5.16: Simulated results as a function of q for different α
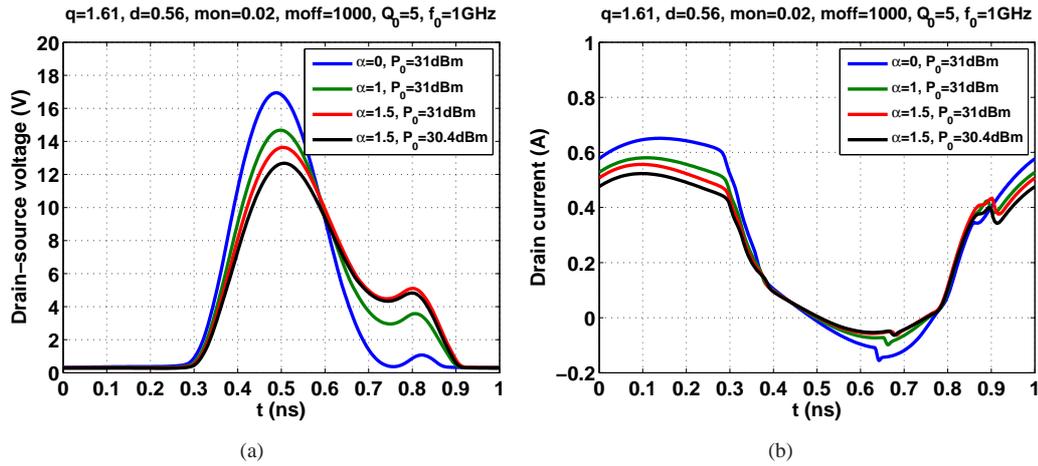
FIGURE 5.17: Drain-source voltage and drain current waveforms for different α

30.4dBm. The simulation results are also shown in Fig. 5.16. One can find that by decreasing the required output power the absolute value of drain-source voltage is below the breakdown voltage for $q < 1$.

- Step 7: Select the optimum q and calculate the corresponding load impedance.

Once the efficiency, output power, and peak drain-source voltage are all satisfied, the optimum load is obtained. The tunning procedure mentioned in step 6 will be ceased. For $\alpha = 1.5$ and $P_{OUT} = 30.4dBm$, the peak drain efficiency of 85% is obtained at $q = 0.01$ or infinite dc-feed inductance. The peak output power of 29.2dBm is also obtained at $q = 0.01$. Therefore the optimum load is obtained at $q = 0.01$ for this device and this specifications. The optimum load impedances at fundamental and higher harmonic frequencies can be calculated. Fig.5.18 shows the load phase angle θ_1 and load magnitude $|Z_1|$ as a function of q for different α at the fundamental frequency. It consists of the device output capacitance and output load network. The optimum load impedance for RF choke at fundamental, second, and third harmonic frequencies are

$$
\begin{aligned}
Z_{1opt} &= 15.3\angle 20.8 \\
Z_{2opt} &= 24.1\angle -88.3 \\
Z_{3opt} &= 13.8\angle -89.7
\end{aligned}
$$

Fig.5.19 summarizes the aforementioned design steps for Class-E power amplifier at a single frequency.
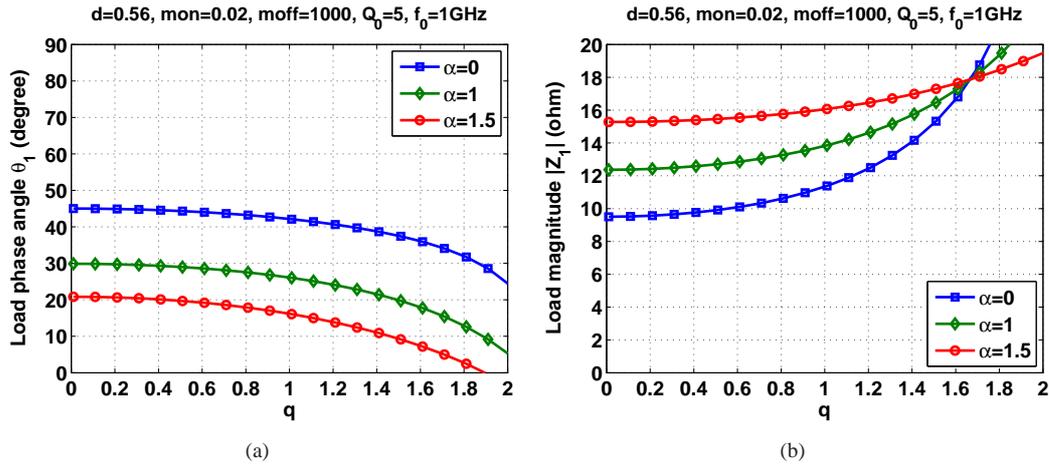
FIGURE 5.18: Load impedance as a function of q for different α

It is necessary to investigate the effects of load impedance variations on the performance of the power amplifier. Section 3.2.2 has shown that the amplifier is very sensitive to the load phase angle θ_1 at fundamental frequency, and relatively tolerant to the load magnitude $|Z_1|$ and other higher harmonic impedances. Thus only the effects of the variation of load phase angle θ_1 on the efficiency, output power and device stress are shown in Fig.5.20. One can observe that to maintain the desired drain efficiency(>80%), output power(>29dBm), and peak drain-source voltage(<12V) the usable load phase angle range is between $0°$ to $20°$. It also means that the load phase angle θ_1 of broadband output load network should be in this range over the operation frequency range.

5.2.2 Broadband Output Load Network

The optimum equivalent drain load impedances seen from the drain node have been given in the previous section. The optimum load impedances Z_{L1opt} not including the device capacitance and bondwires for the operating frequencies are shown in Fig. 5.21. The ideal output performance is shown in Fig. 5.22 where the drain efficiency exceeds 85%, and the output power 29.3dBm. The peak drain-source voltage is almost constant around 12V, and the peak drain current around 0.65A over all the frequencies. The falling of PAE is due to the increase in the power dissipation of the inverter as the frequency increases. In order to achieve a wide bandwidth Class-E sub-optimum mode operation, a load network providing the correct load impedance over the bandwidth of operation is required. The proposed load network configuration using lumped elements is shown in Fig. 5.23. It consists of a series DC blocking capacitor $C_{blocking}$, followed by a network like second-order low-pass filter. The dc-feed inductor L is also a part of the output load network.
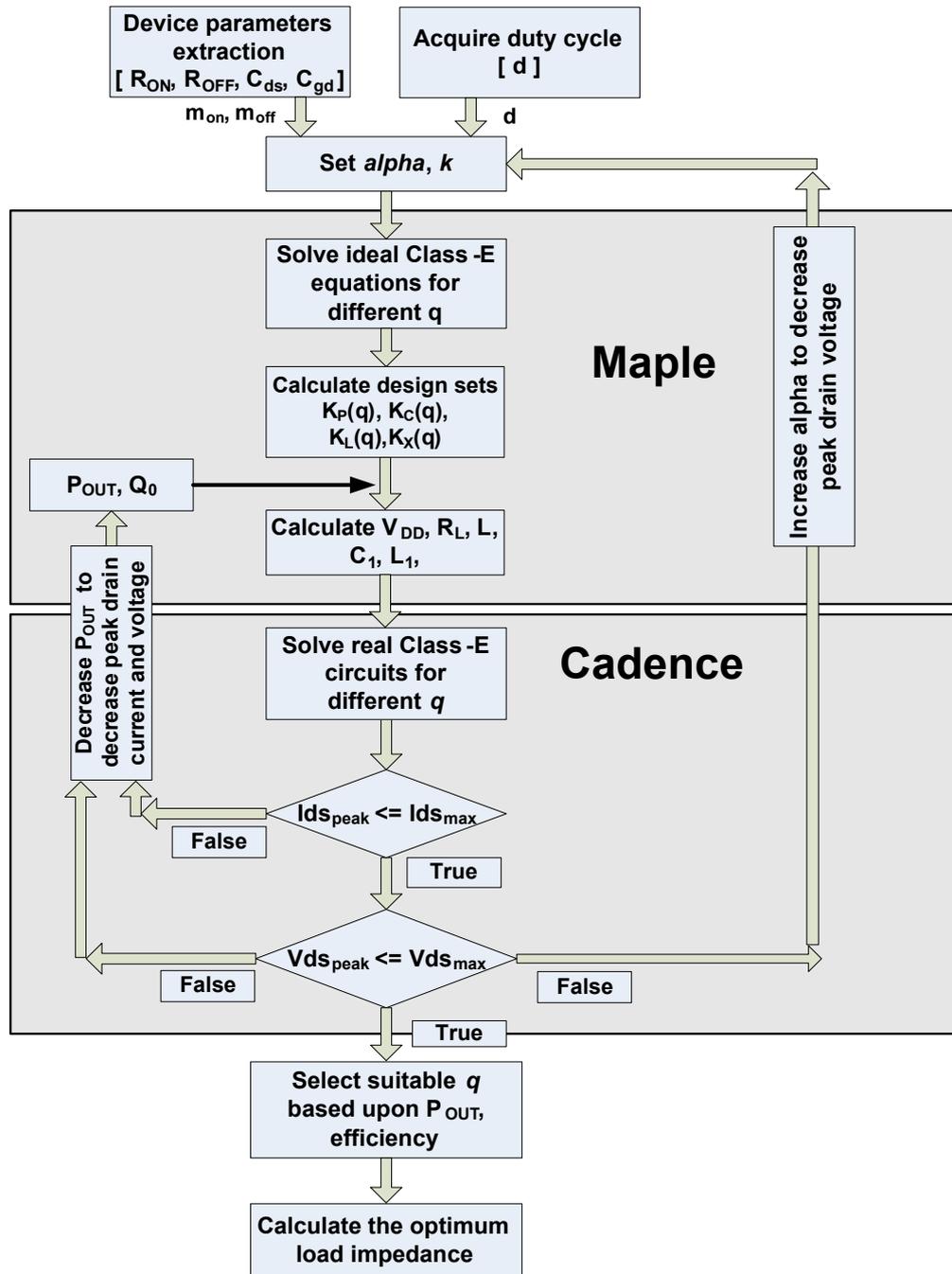
FIGURE 5.19: Class-E power amplifier design flowchart
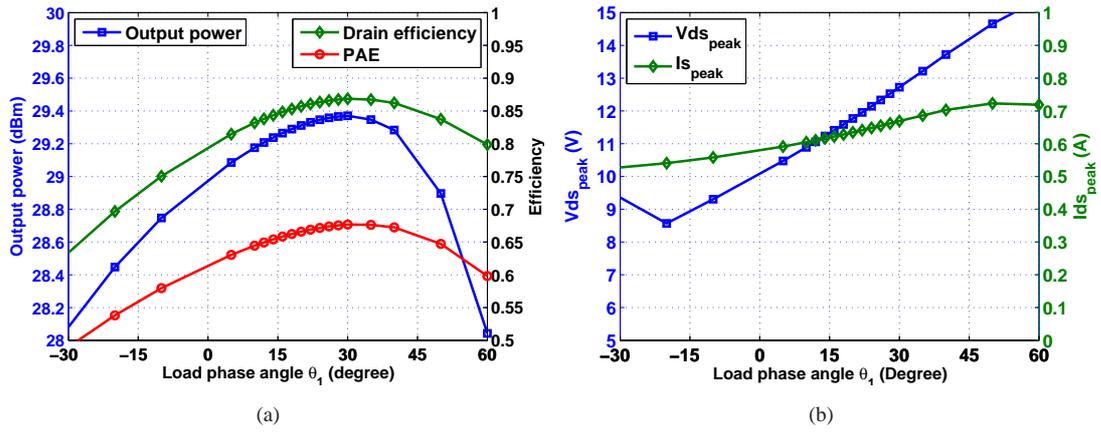
FIGURE 5.20: Effects of load phase angle θ_1 on the performance of power amplifier
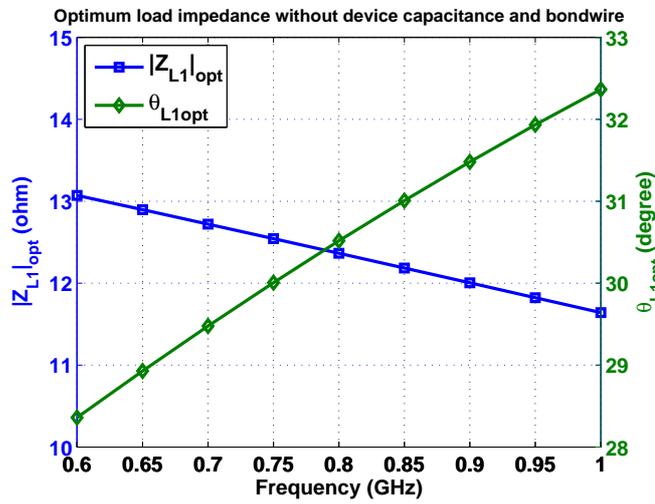
FIGURE 5.21: Optimum fundamental load impedances Z_{L1opt} over frequency
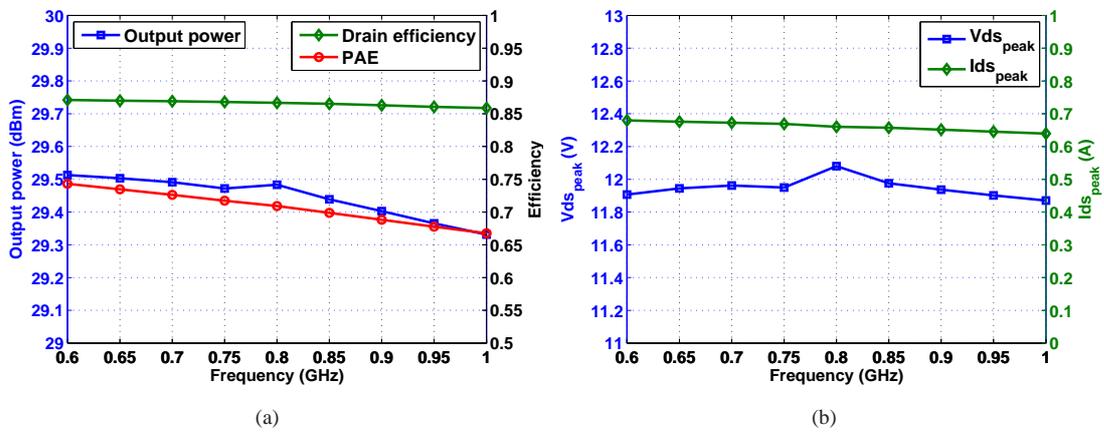
FIGURE 5.22: Ideal output power, drain efficiency and PAE for the ideal optimum load impedances
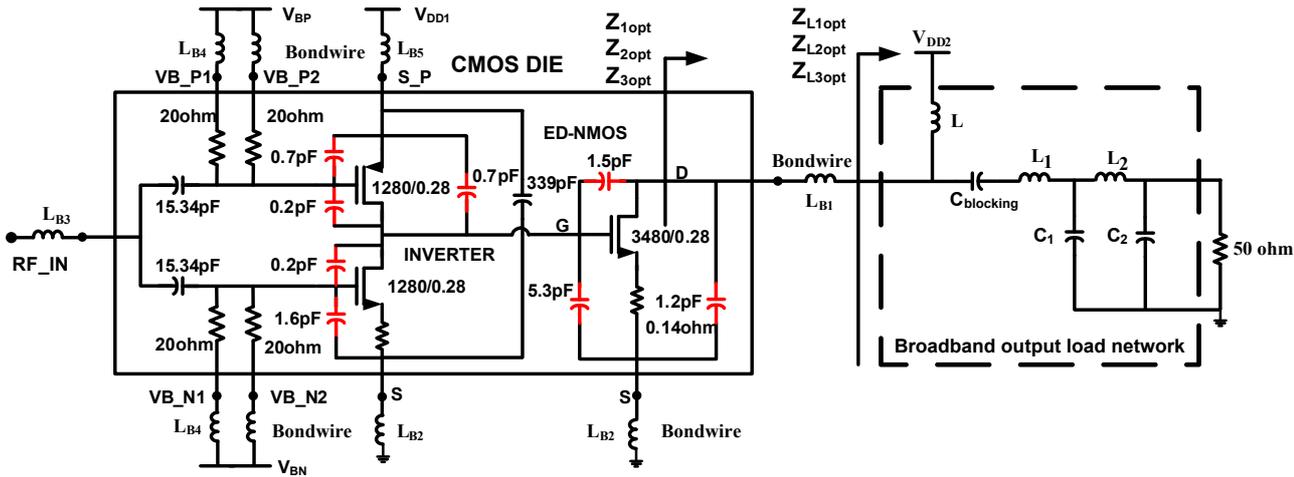
FIGURE 5.23: Broadband output load network for the PA

TABLE 5.3: Ideal lumped element values for output load network

L	L_1	C_1	L_2	C_2
12nH	4.5nH	7.8pF	7.5nH	3.3pF

The output load network was synthesized by ADS optimizer. The optimization goals were set to the optimum load impedances at the operation frequencies. For this design it is the drain load phase angle $\theta_1 < 20°$, $\theta_2 < -60°$, and load magnitude $|Z_1| \approx 15$. However, these goals cannot be satisfied at all operation frequencies. Table 5.3 presents element values of the ideal lumped elements. The synthesized load impedances over the operation frequencies are shown in Fig.5.24. The synthesized load magnitude $|Z_1|$ is around 20Ω that is larger than the optimum value of 15Ω. This will lead to lower output power. The ripple of $|Z_1|$ is relatively small. The synthesized θ_1 is below 20° from 0.7GHz to 1.1GHz, but θ_2 of second harmonic load phase angle at 1.4GHz is larger than 0° which will lead to low drain efficiency. θ_2 is smaller than -60° above 1.6GHz so that the usable frequency range is from 0.8GHz to 1.1GHz.

The simulated amplifier performance for the synthesized output load network are shown in Fig5.25. One can observe that the output power is larger than 27dBm from 0.8GHz to 1.2GHz with 1dB flatness. The drain efficiency is above 80%, and PAE is about 60% from 0.8GHz to 1.2GHz. The peak drain efficiency is about 90%. The power gain is about 12dB with 1dB ripple. The peak drain-source voltage is below 12V except around 0.8GHz. It is 12.3V around 0.8GHz. We think that is acceptable. The drain-source voltage waveforms are shown in Fig.5.26 as a function of frequency. It is apparent that the operation mode is different at different frequencies dut to the different load impedances.
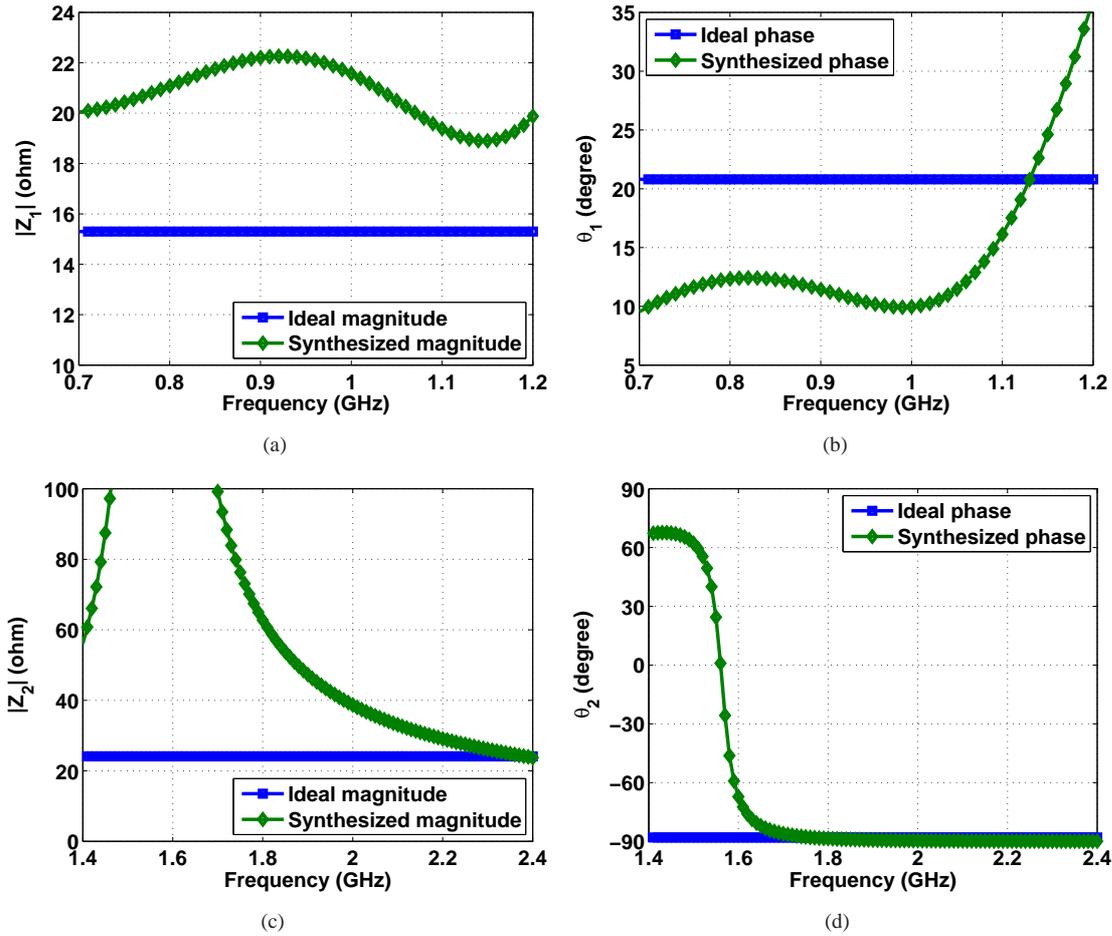
FIGURE 5.24: Synthesized drain load impedances as a function of frequency with ideal lumped elements

5.3   Layout and Post-Layout Simulations

The layout was designed to implement the broadband Class-E power amplifier. Murata's high Q inductors and capacitors were selected for the output load network. Since the effects of microstrip lines and parasitic resistances, capacitances and inductances of Murata's components, the final passive component values are different from the ideal lumped elements given in Table 5.3. But the main design goal is still to realize the required load magnitudes and phase angles in the operation frequency band. The Murata component values are shown in Table 5.4. The final layout is shown in Fig. 5.27. In the figure, the resistor R_{stab} and capacitor C_{stab} at the input make the power amplifier unconditionally stable both at low and high frequencies. The final layout was simulated by Momentum, and imported into schematics to do post-layout simulations with Murata components. The synthesized drain load impedances are shown in Fig. 5.28. One can see that the load phase angle θ_1 is much flatter for $C_1 = 6.2pF$ than for $C_1 = 6.8pF$. But this component of $C_1 = 6.2pF$ is out of stock, and can only be delivered after two months. We could not wait for so long time. Therefore in the final design, the component of $C_1 = 6.8pF$
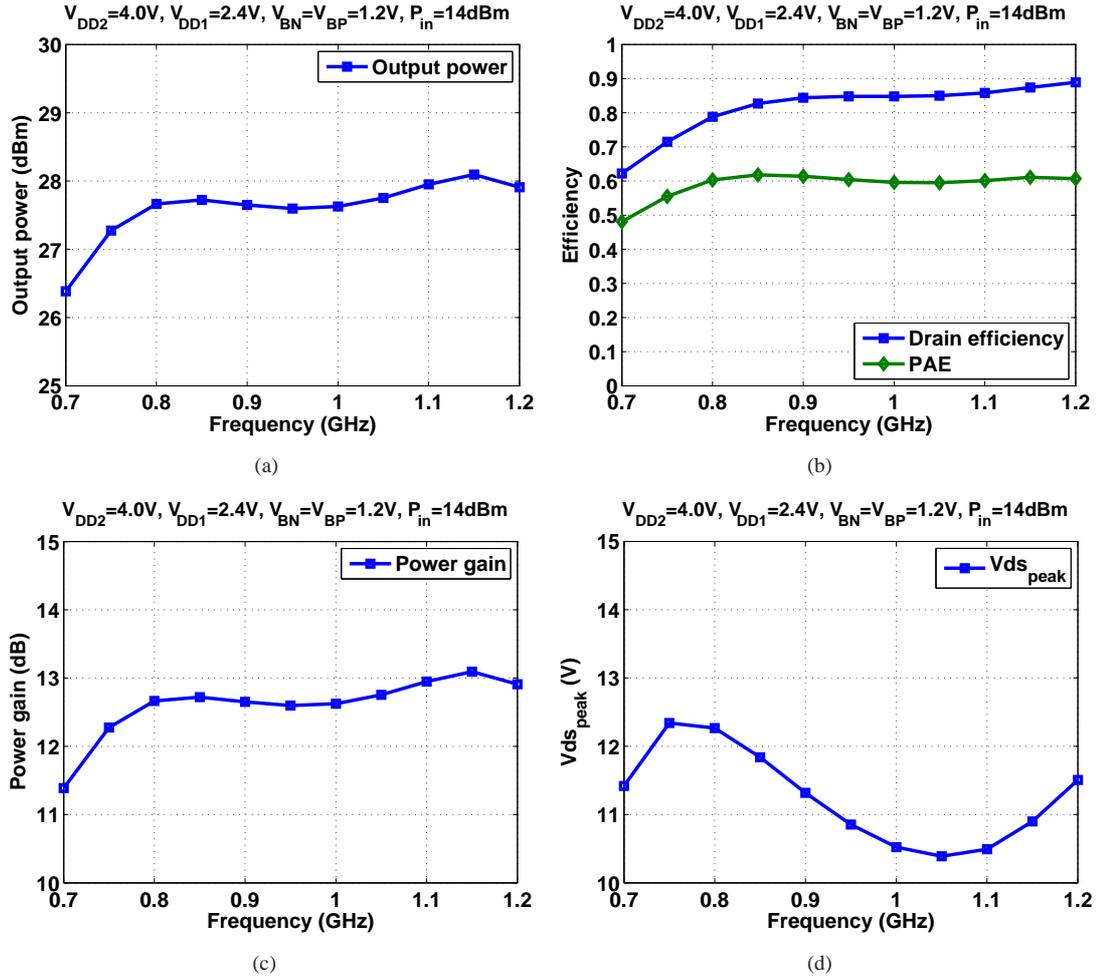
FIGURE 5.25: Power amplifier performance for the synthesized ideal lumped elements

TABLE 5.4: Murata lumped element values for output load network

L	L_1	C_1	L_2	C_2
12nH	3.3nH	6.8pF	7.5nH	2.2pF

was used. One can also find that the load phase angle θ_2 at 1.2GHz (the second harmonics of 0.6GHz) is larger than 0°. This will lead to lower drain efficiency.

The post-layout simulation results of switch-mode operation from 0.6GHz to 1.2GHz are presented in Fig.5.29. The power level of the input RF signal is 14dBm so that the power amplifier operates at switch-mode. The supply voltage for the final stage (ED-NMOS) is 4V, and 2.4V for inverter. The gate bias voltage for NMOS and PMOS of the inverter is 1.2V.

One can observe that the output power is larger than 27dBm from 0.65GHz to 1.05GHz, but smaller than what we expected. This is because the synthesized load magnitude $|Z_1|$ is larger than the optimum value of 15.3Ω. The flatness of the output power is less than 1dB from 0.65GHz to 1.05GHz. The drain efficiency is larger than 75% from 0.65GHz to 1.05GHz, and the power-added efficiency is above 50% in this range. The drain efficiency is smaller than the
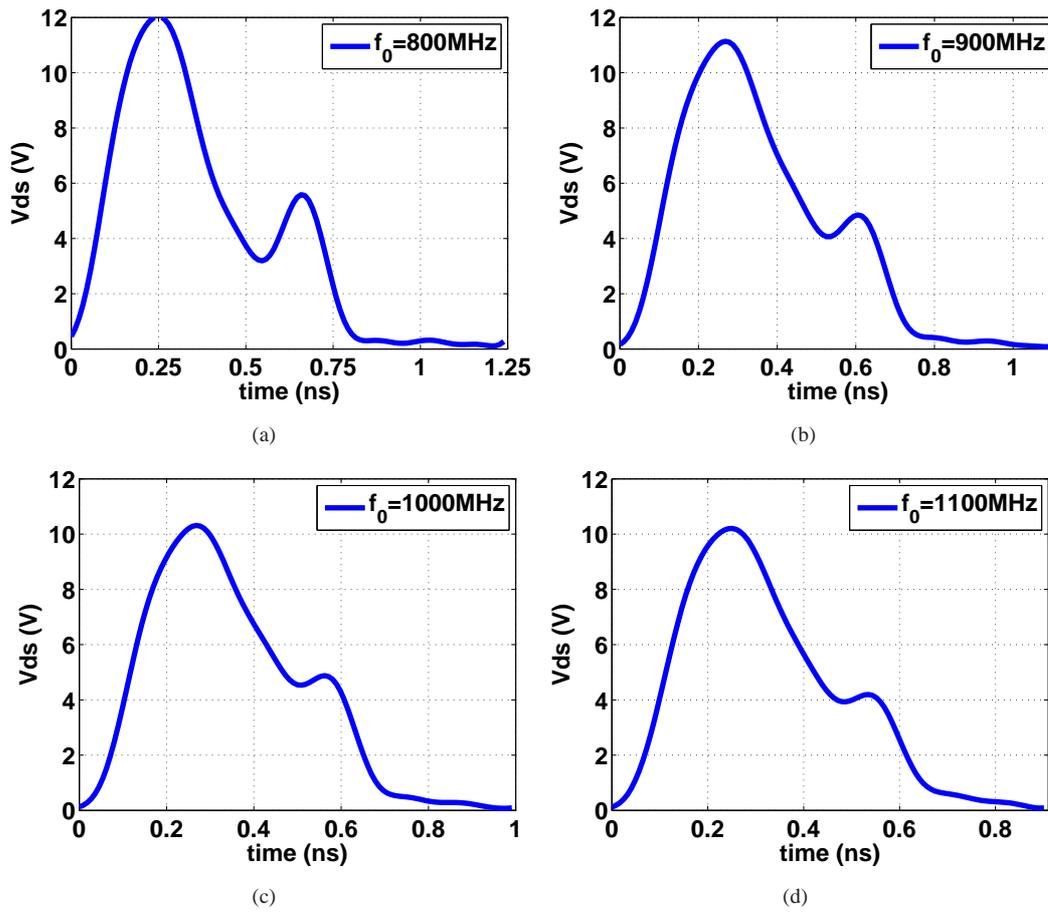
FIGURE 5.26: Drain-source voltage waveforms at different frequencies for the synthesized ideal lumped elements
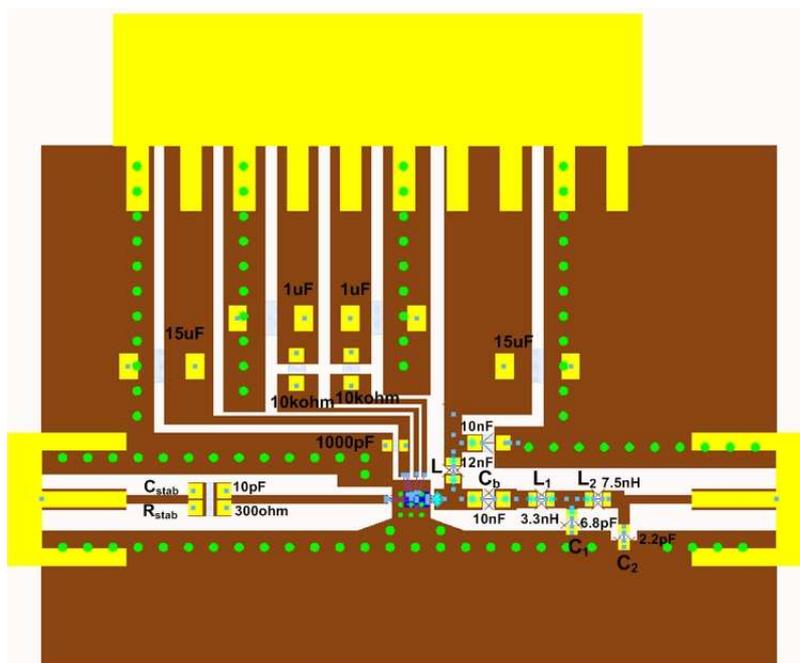
FIGURE 5.27: Final PCB layout
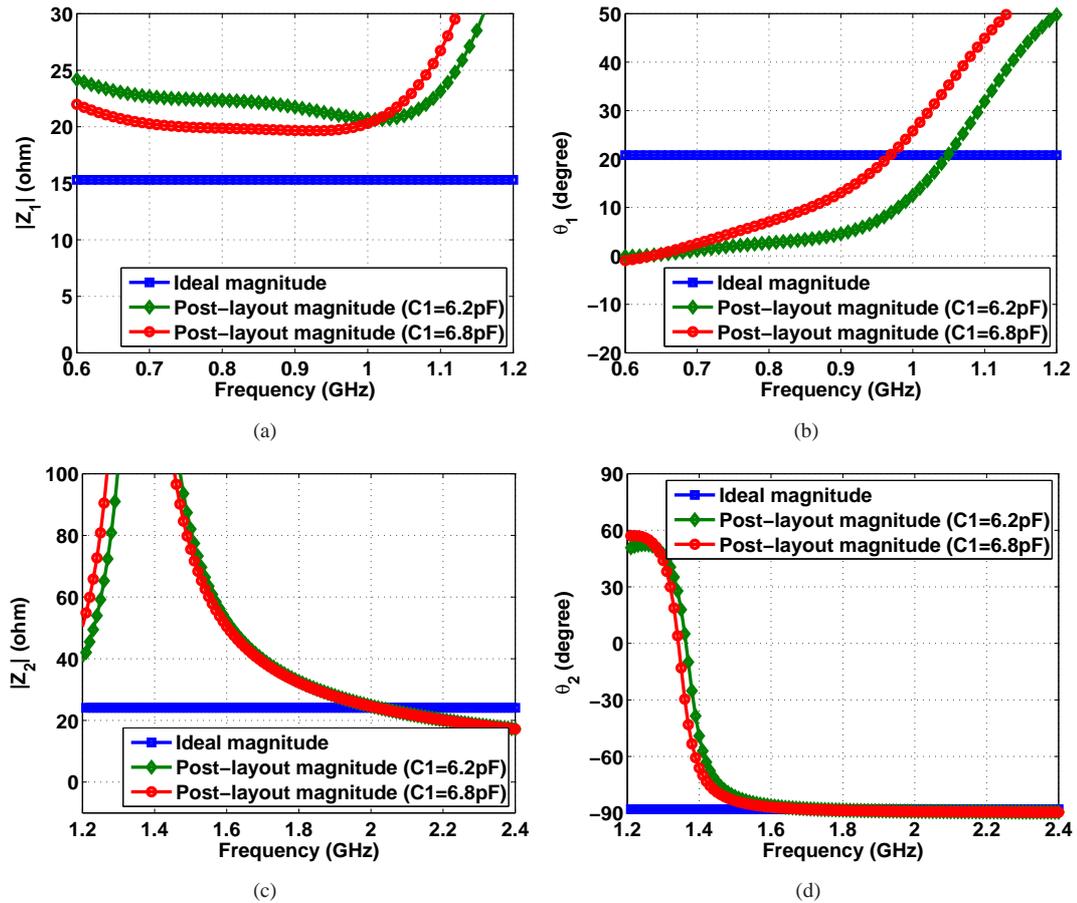
FIGURE 5.28: Drain load impedances for final layout with Murata components

result obtained by ideal lumped elements. This is due to the loss at the parasitic resistances of passive components and metal loss of microstrip lines. The output power and drain efficiency are quite flat from 0.65GHz to 1.05GHz because of the flat load magnitude $|Z_1|$ and small ripple in load phase angle θ_1 over this range. The power gain is more than 13dB from 0.65GHz to 1.05GHz without input matching. The peak drain-source voltages at 0.65GHz and 1.05GHz are about 12.5V. We think the device can undertake this high drain voltage. Fig.5.29(e) shows that the amplifier is unconditionally stable from 0 to 5GHz.

We are very interested in how the duty-cycle influences the performance of the broadband Class-E power amplifier. In this design, the duty cycle is adjusted by setting the different gate bias voltages of NMOS and PMOS of inverter. Fig 5.30 shows the waveforms of the drive signals to the final stage (ED-NMOS) tuning by V_{BN} and V_{BP} at 1GHz. The duty cycle decreases from 72.3% to 49.1% when the gate bias voltages V_{BN} and V_{BP} increases from 1.0V to 1.3V.

The effects of variations of duty-cycle on the output power, drain efficiency, PAE, power gain, peak drain-source voltage and stability are shown in Fig.5.31. It is apparent that by increasing the duty cycle (decreasing V_{BN} and V_{BP}) the output power can be improved, but the peak drain-source voltage will be increased simultaneously. The power gain is also increased by increasing
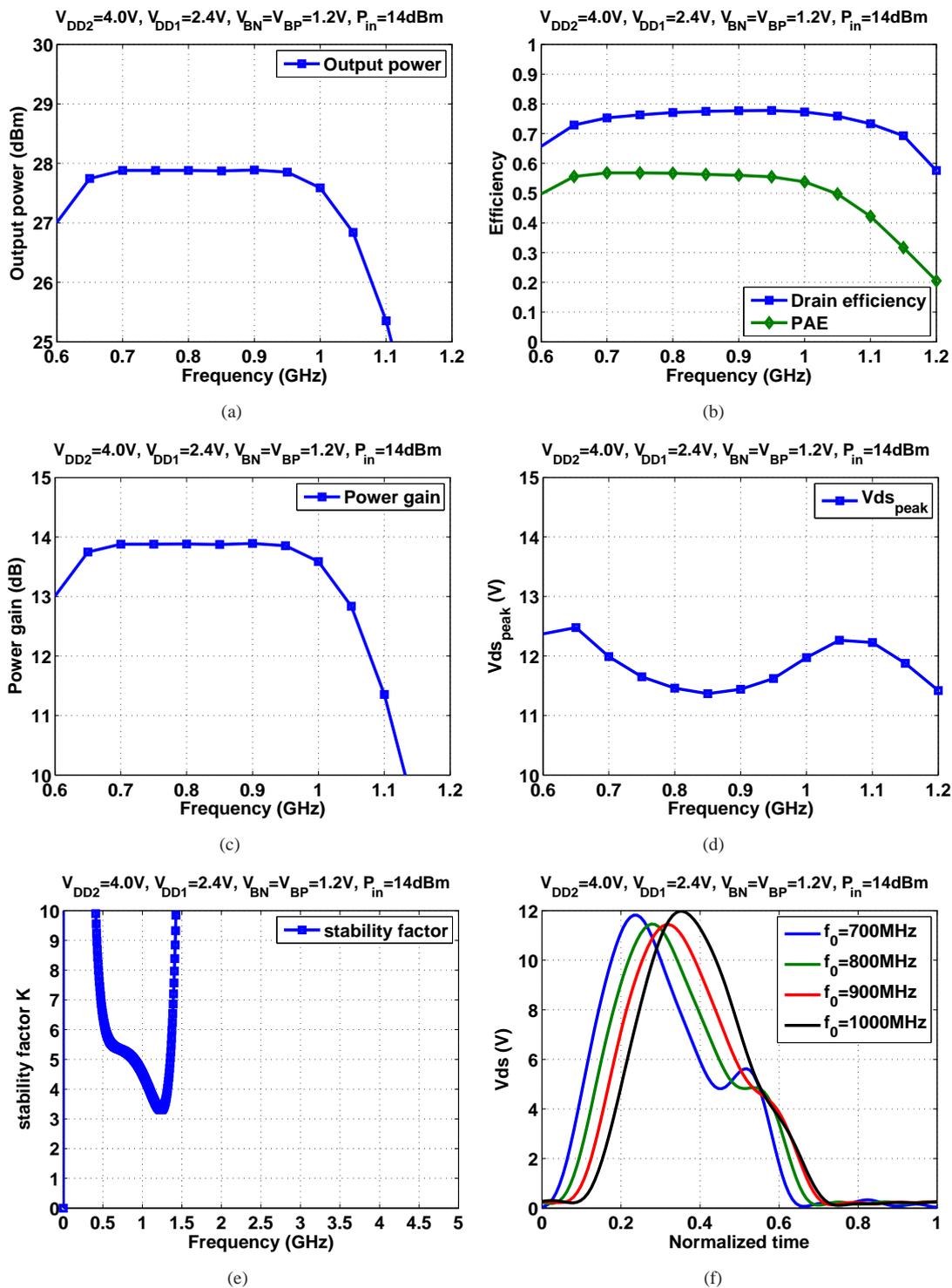
FIGURE 5.29: Post-layout simulation results of switch-mode operation over broad frequency range.
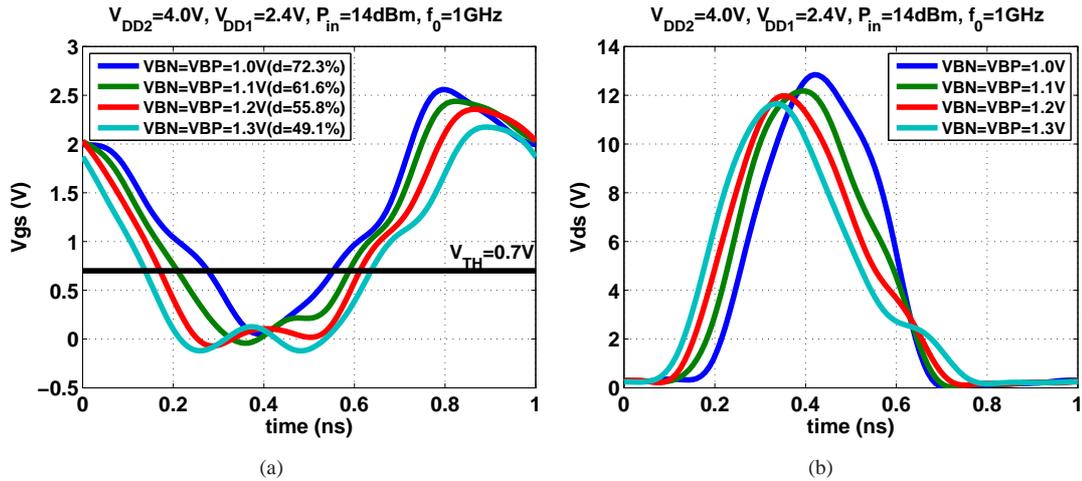
FIGURE 5.30: Drive signal waveforms tuning by gate bias voltages of NMOS and PMOS of inverter.

the duty-cycle. This agrees very well with the theory shown in [5]. The peak drain efficiency is improved by increasing the duty-cycle because of higher output power. However the fluctuation in drain efficiency for $V_{BN} = V_{BP} = 1.0V$ is larger than that for $V_{BN} = V_{BP} = 1.2V$. This is because the amplifier is designed for duty cycle $d = 56\%$ or $V_{BN} = V_{BP} = 1.2V$. The required load impedances for $d = 72.3\%$ or $V_{BN} = V_{BP} = 1.0V$ are different from that for $d = 56\%$ or $V_{BN} = V_{BP} = 1.2V$. The figure also shows that the amplifier is stable for all different duty-cycles.

Since the gate bias voltage affects the linear operation, it is necessary to investigate the DC gate bias voltage of ED-NMOS as a function of $V_{BN} = V_{BP}$. Fig.5.32 shows the relation between the these two voltages. For ED-NMOS, the threshold voltage is about 0.7V, and the maximum linear input voltage is 2.4V. Thus the gate bias voltage for Class-A mode is 1.55V, and 0.7V for Class-B mode.

Fig.5.33-5.36 show the simulation results for linear-mode at 0.7GHz, 0.8GHz, 0.9GHz and 1.0GHz. In these figures, one can find that the small-signal power gain is only valid when gate bias voltage is larger than the threshold voltage. The small-signal power gain is about 25dB for $V_{BN} = V_{BP} = 1.0V$, and 29dB for $V_{BN} = V_{VP} = 1.1V$. For the same output power, the third-order intermodulation distortion (IMD3) for $V_{BN} = V_{BP} = 1.0V$ is better than other bias voltages, but the drain efficiency is quite low for this bias voltage. Fig.5.37 shows the characteristics at 1dB compression point. It shows that for Class-A or B mode the small-signal power gain is much larger than that of Class-C mode, but the drain efficiency at 1dB compression point is quite low for Class-A or B mode compared with Class-C mode.
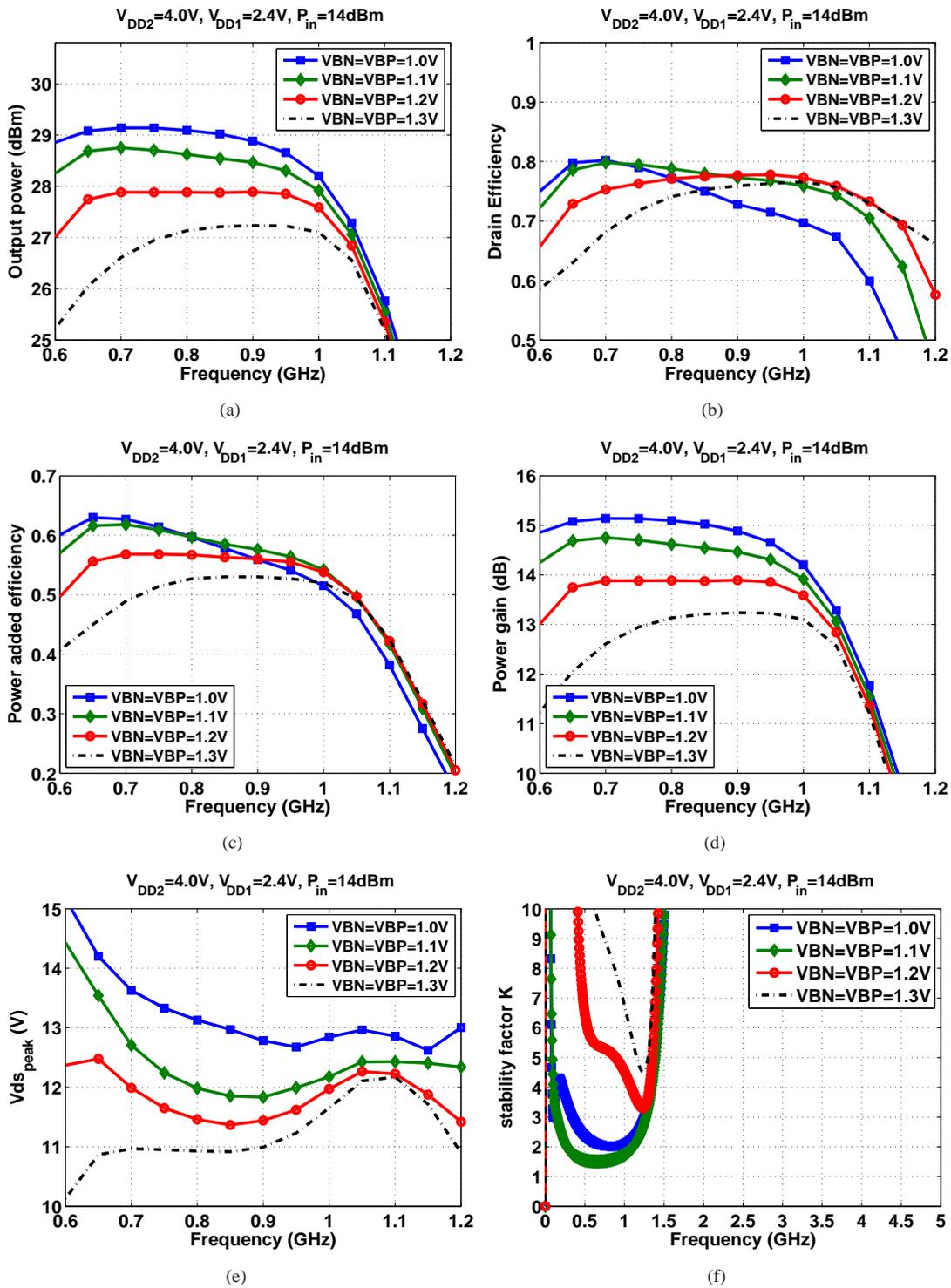
FIGURE 5.31: Effects of variations of duty-cycle on the performance of switch-mode
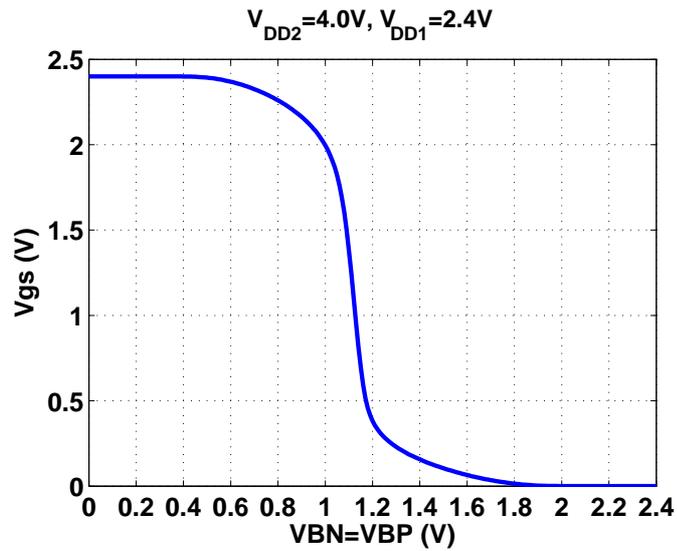
FIGURE 5.32: DC static gate-source bias voltage as a function of V_{BN} and V_{BP}.
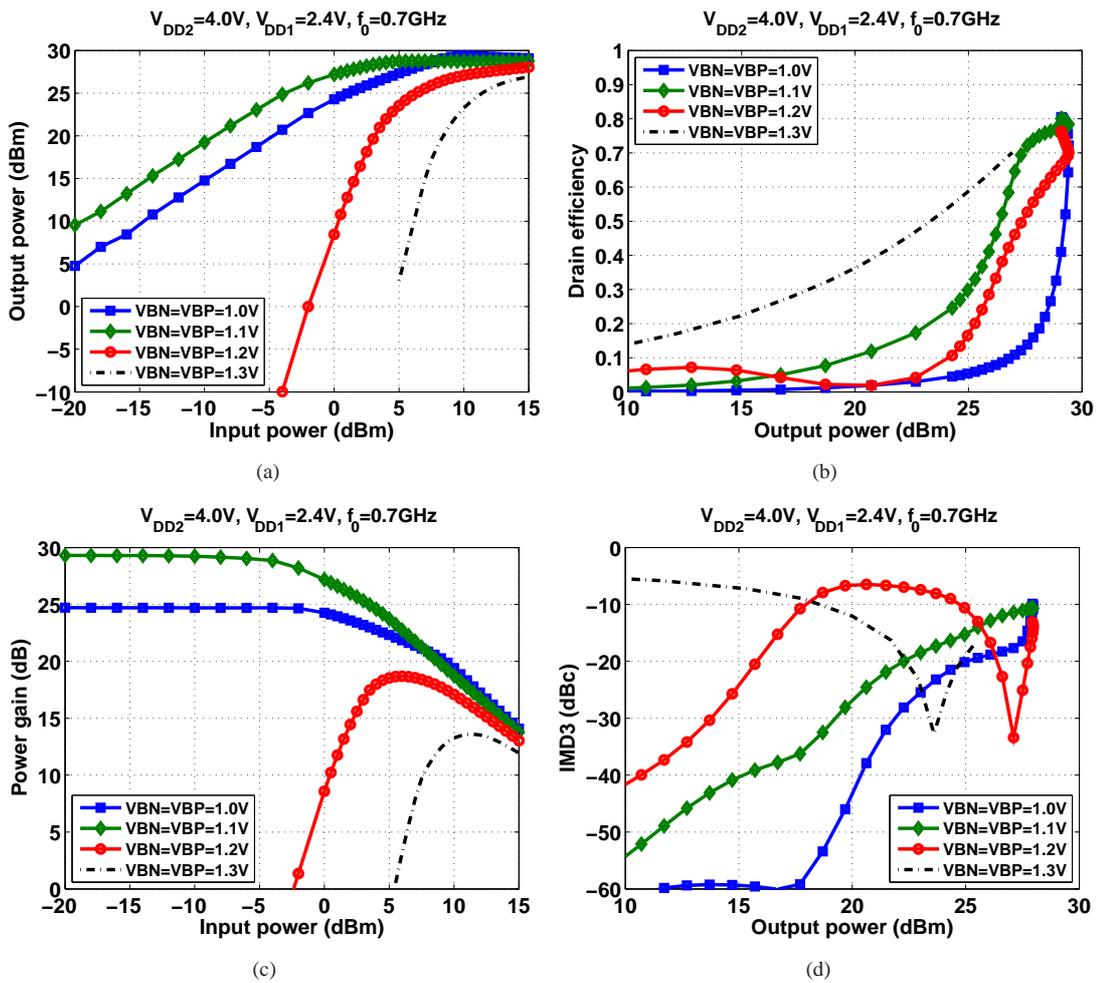
FIGURE 5.33: Post-layout simulation results of linear-mode operation at 0.7GHz.
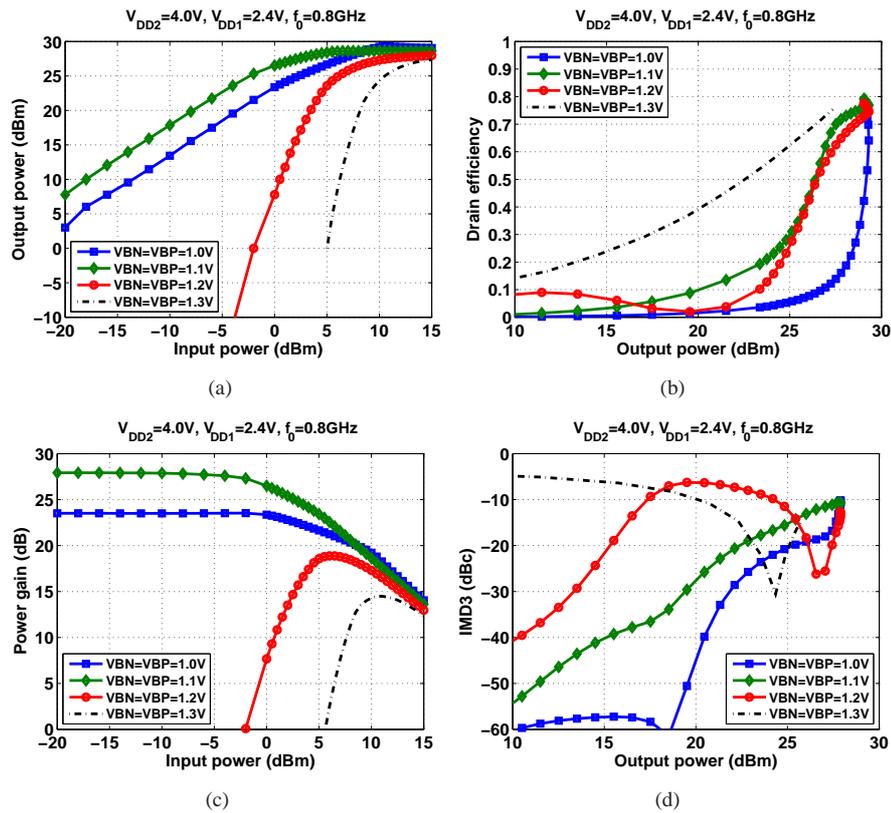
FIGURE 5.34: Post-layout simulation results of linear-mode operation at 0.8GHz.
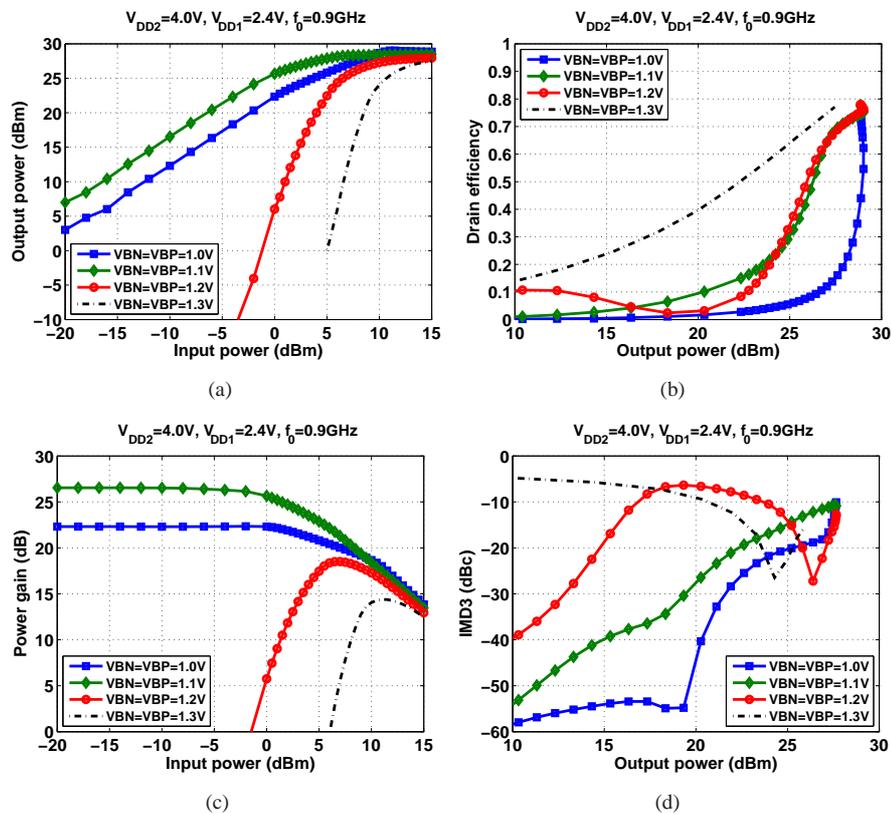
FIGURE 5.35: Post-layout simulation results of linear-mode operation at 0.9GHz.
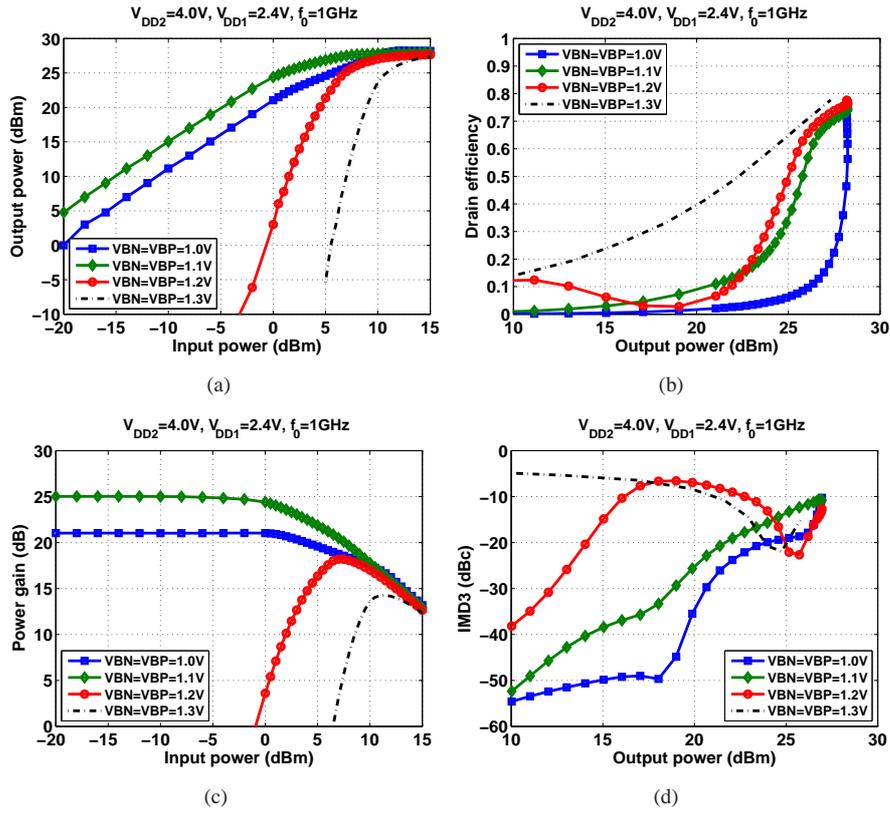
FIGURE 5.36: Post-layout simulation results of linear-mode operation at 1.0GHz.
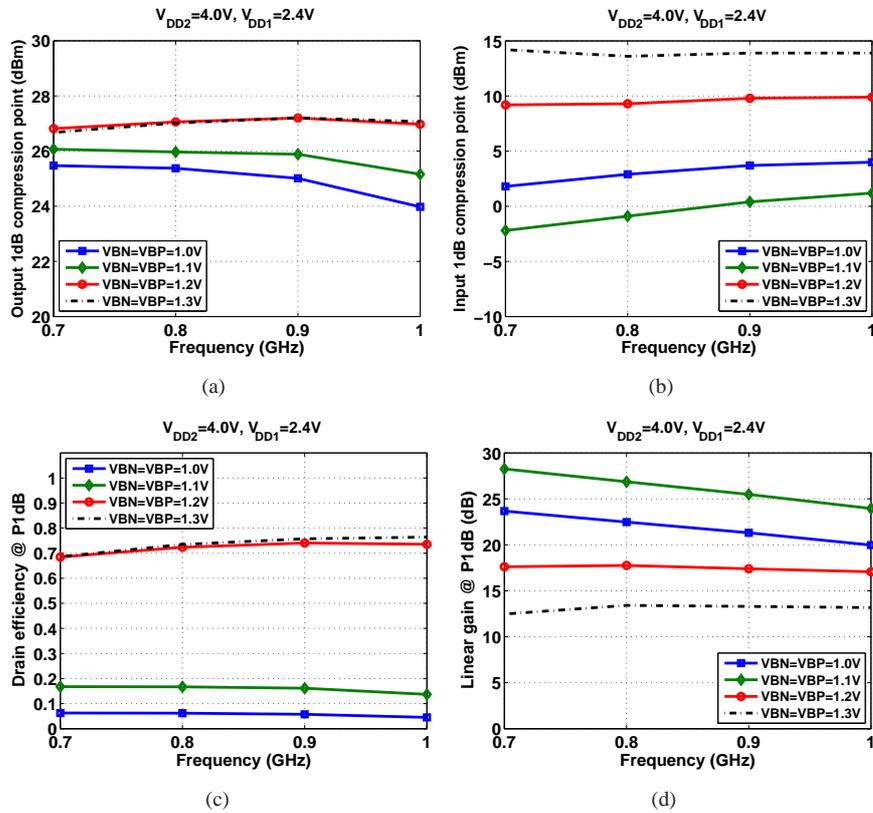
FIGURE 5.37: Post-layout simulation results of linear-mode operation at 1dB compression point

5.4   Conclusion

In this chapter, the effects of load network and gate bias voltage on the linearity of ED-NMOS were investigated. It shows that the best IMD3 is obtained when the power amplifier is biased at Class-AB mode with RF choke. For the Class-B biasing condition, the finite dc-feed inductance can improve the IMD3 performance. In addition, a systematic design approach for broadband Class-E power amplifier was described, and a broadband Class-E power amplifier based upon an existing CMOS die was implemented from 0.65-1.05GHz. The post-layout simulation results for switch-mode show that the drain efficiency exceeds 75%, output power is larger than 27dBm from a 4.0V supply, and peak drain-source voltage is less than 12.5V. The output power flatness is less than 1dB.

Chapter 6

Measurements

To verify the performance of the proposed broadband output load network, a broadband Class-E power amplifier was implemented. Fig.6.1 shows a photo of the fabricated PCB of the proposed design. The PCB size is 35×25mm^2. The measurement results will be given in this chapter.

6.1 Test Setup

The block diagram of the test setup is shown in Fig.6.2. The one-tone or two-tone signals are generated by Rohde & Schwarz SMIQ with AMIQ to drive the amplifier. The output of the broadband power amplifier is fed to the spectrum analyzer Rohde & Schwarz FSQ. To protect the spectrum analyzer, two 6-dB attenuators were inserted between the amplifier output and FSQ. All the equipments are controlled by the automatic test program in Labview.
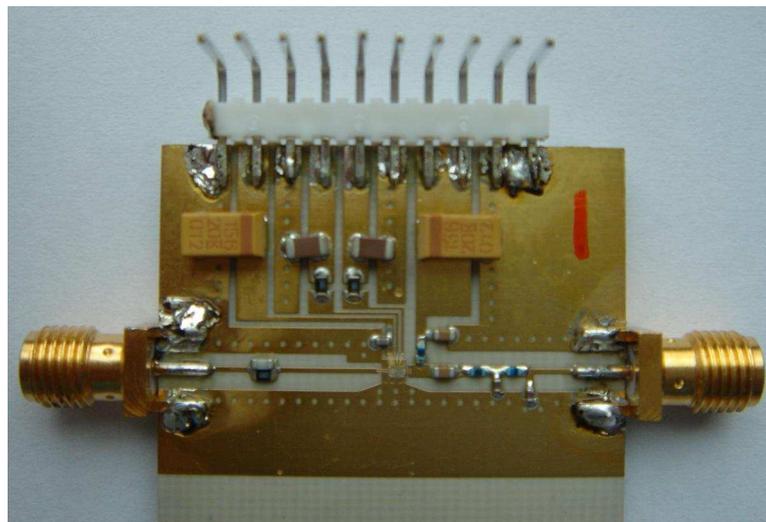
FIGURE 6.1: Photograph of implemented broadband Class-E power amplifier
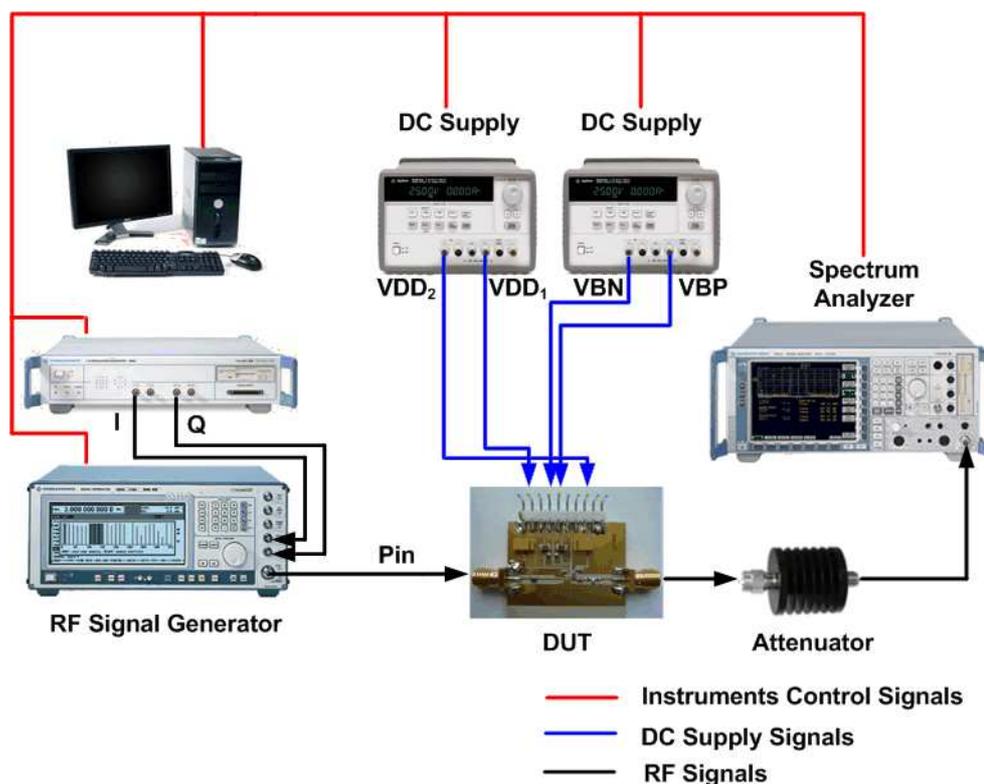
FIGURE 6.2: Block diagram of the measurement setup for broadband Class-E power amplifier

6.2 Measurement Results

6.2.1 Comparison of Simulated and Measured Results

Fig.6.3 shows the comparison between the simulated and measured output power, power gain, drain efficiency, and power added efficiency (PAE) values against frequency from 500 to 1200MHz. The device is biased at $V_{DD1} = 2.4V$, $V_{DD2} = 5.0V$, and $V_{BN} = V_{BP} = 1.1V$ at RF input power of 14dBm.

Close agreement is achieved between the simulated and measured output power and power gain between 0.6GHz and 1.0GHz. At high frequencies (i.e. 1.1GHz and 1.2GHz), the measured output power is 2dB larger than the simulated results. Fig.6.3(a) shows that the measured bandwidth for $\Delta P_{out} < 1dB$ is wider than the simulation result. But at f_0=1.0GHz, the maximum difference of 8% is found in drain efficiency. The difference between measurement and simulation might be due to the transistor models. The model of ED-NMOS is a first-round model which means the device was only measured and modelled once. The model was not developed after that. The DC I-V measurement shown in Fig.5.4 also implies that the ED-NMOS model in Cadence Library is different from the fabricated one. Besides the transistor model, the inaccurately modelled bondwires might also contribute to the difference, especially at high frequencies.
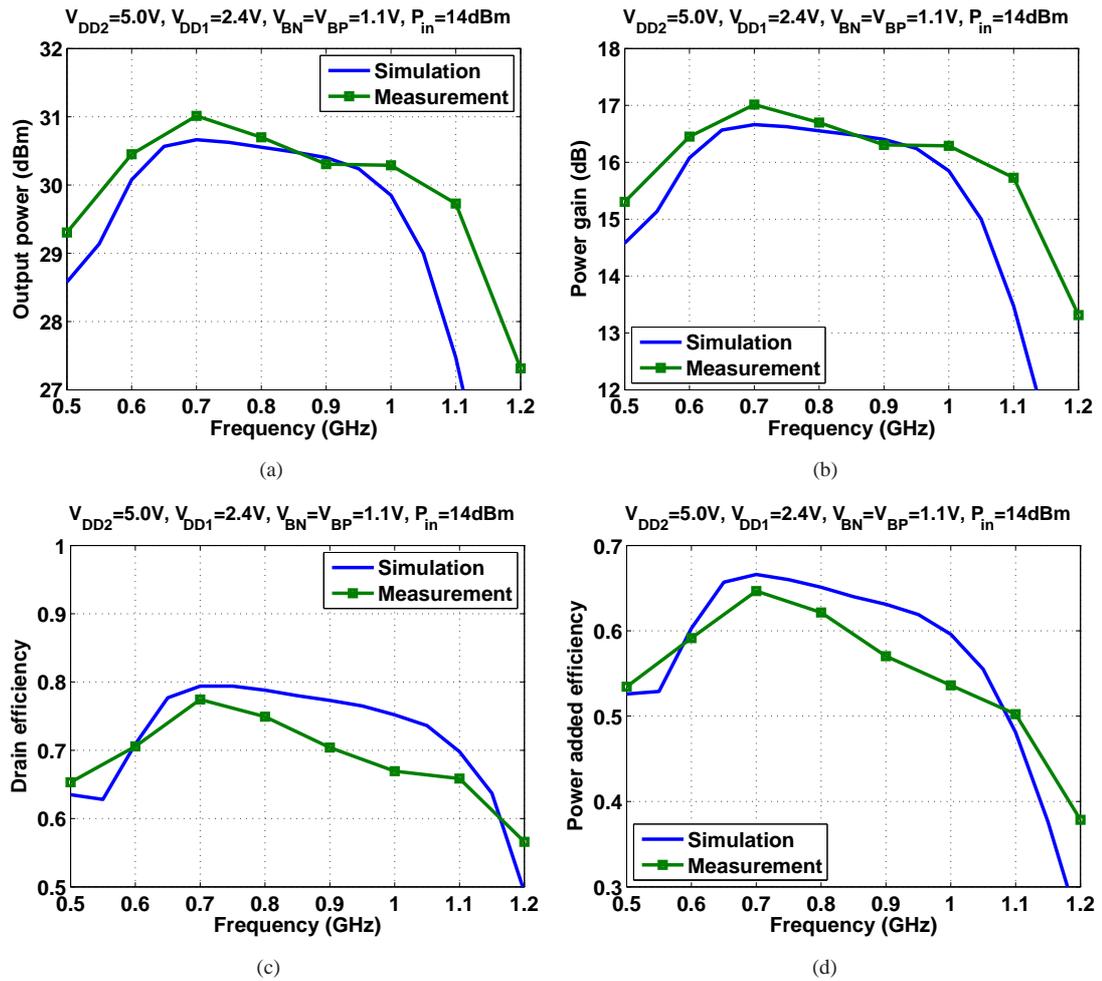
FIGURE 6.3: Comparison of simulated and measured performance of the proposed broadband Class-E PA as a function of frequency: (a) output power, (b) power gain, (c) drain efficiency, (d) power added efficiency.

We only know the rough length of the bondwires, and do not know the height of the bondwires. This might lead to that difference.

Measured output power indicates the flat characteristic associated with broadband design from 560MHz to 1050MHz, at a value of 30.5±0.5dBm. A power gain of between 16-17dB has been observed over the frequency band 560MHz to 1050MHz. The drain efficiency and PAE remain above 67% and 52% across the same bandwidth. The peak drain efficiency of 77% and peak PAE of 65% are measured at 700MHz with 31dBm output power. The fluctuations in drain efficiency and PAE over a bandwidth of 490MHz are less than 13%. Therefore the measured bandwidth[1] for this CMOS Class-E power amplifier is about 60.9% with $P_{out} \geq 30dBm$, $\eta \geq 67\%$, and $PAE \geq 52\%$. Since the equipment for the waveform measurement is not available for us at this moment, the drain voltage waveforms cannot be shown here.

---

[1]Bandwidth: the frequency range for which the variation in the output power is less than 1.0dB.

TABLE 6.1: Comparison broadband Class-E PAs

Specifications	Y. Qin 2005[42]	D.Y.C. Lie 2006[11]	J. Jang 2007[41]	A.A. Tanany 2009[12]	**This Work** 2010
Frequency [GHz]	0.54-0.89	0.5-1.2	0.8-0.94	0.6-1.0	0.56-1.05
Bandwidth [%]	48.9	82.3	16.1	50	60.9
P_{out} [dBm]	> 20	> 17.2	> 31	> 45.2	> 30
ΔP_{out} [dB]	< 2.5	< 3.0	< 0.5	< 1.7	< 1.0
Power Gain [dB]	> 8.0	> 7.2	> 30	> 10	> 16
Drain Efficiency [%]	N.A.	N.A.	N.A.	> 66	> 67
PAE [%]	> 50	> 50	> 55	> 62	> 52
PAE$_{peak}$ [%]	66.5	70	62	80.6	65
Technology	PHMET	SiGe	CMOS	GaN	CMOS
Topology	Single-stage	Single-stage	Two-stage	Single-stage	Two-stage

TABLE 6.2: Comparison CMOS Class-E PAs

Specifications	C. Yoo 2001[43]	K.Mertens 2002[44]	J. Ramos 2005[45]	J. Jang 2007[41]	**This Work** 2010
Frequency [MHz]	900	700	855	875	700
V_{DD} [V]	1.8	2.2	2.3	3.3	5.0
P_{out} [dBm]	29.5	30.0	30.0	31.7	31.0
Power Gain [dB]	N.A.	18	20	30.3	17
Drain Efficiency [%]	46	N.A.	67	N.A.	77
PAE [%]	41	62	66	62	65
Technology	0.25μm CMOS	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS	65nm CMOS
Topology	Two-stage single-ended PA	Two-stage differential PA	Two-stage differential PA	Two-stage differential PA	Two-stage single-ended PA

Table 6.1 summarizes the published broadband Class-E power amplifiers around 1.0GHz. Compared with PHMET and SiGe technologies, this CMOS power amplifier can deliver higher output power because the breakdown voltage of the extended-drain NMOS is much higher. High supply voltage of 5.0V is applied to the final stage. Compared with the CMOS power amplifier in [41], the bandwidth of this work is much wider than that one. The peak PAE is less than the GaN power amplifier in [12]. However, the output power, drain efficiency and PAE of this work is relatively flat across a very broad frequency range.

In Table 6.2, the performance of the proposed Class-E power amplifier is compared with that of other power amplifiers in CMOS technology at a single frequency. Since the purpose of this design is to implement a broadband Class-E PA, we designed a load network which has a relatively flat impedance over a broad frequency band although the magnitude of load impedance is large. In [39], Acar has already shown that 4W output power can be obtained with 70% PAE at 2.0GHz by using ED-NMOS device. Therefore, there is no doubt that when using the ED-NMOS device to design a Class-E power amplifier higher output power could be achieved at a single frequency by using lower load impedance.
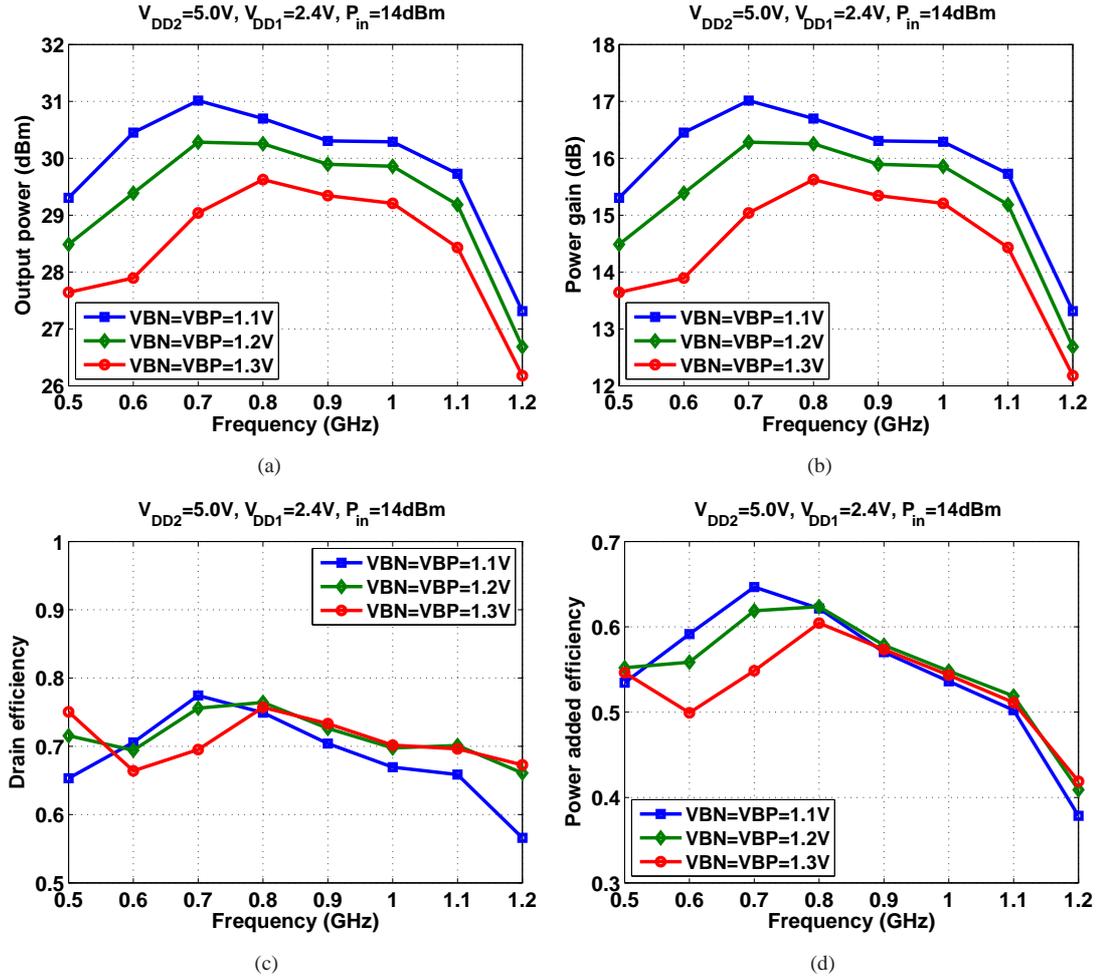
FIGURE 6.4: Broadband measurement of dynamic inverter gate bias of Class-E PA: (a) output power, (b) power gain, (c) drain efficiency, (d) power added efficiency.

6.2.2 Dynamic Inverter Gate Bias

In chapter 5, the effects of variations of inverter gate bias voltage has been studied in simulation. Fig.6.4 shows the measured results of variations of $V_{BN} = V_{BP}$ from 1.1V to 1.3V. From Fig.5.32, one can observe that the gate bias voltage of ED-NMOS increases as the gate bias voltages (V_{BN} and V_{BP}) of inverter decrease. Thus the device can deliver more output power to the load as the gate bias of inverter decreases. One can adjust the output power level by tuning the gate bias voltages of inverter. The fluctuation of efficiency between 500 to 1100MHz for these three bias voltages are relatively small.

Fig.6.5 shows the output power, drain efficiency, and PAE as a function of input power at 900MHz for different gate bias voltages of inverter. It is apparent that the small-signal power gain only exists when the power amplifier is biased at Class-A or Class-AB mode. When the power amplifier is driven into switch-mode, the drain efficiency and PAE are less sensitive to the gate bias voltages.
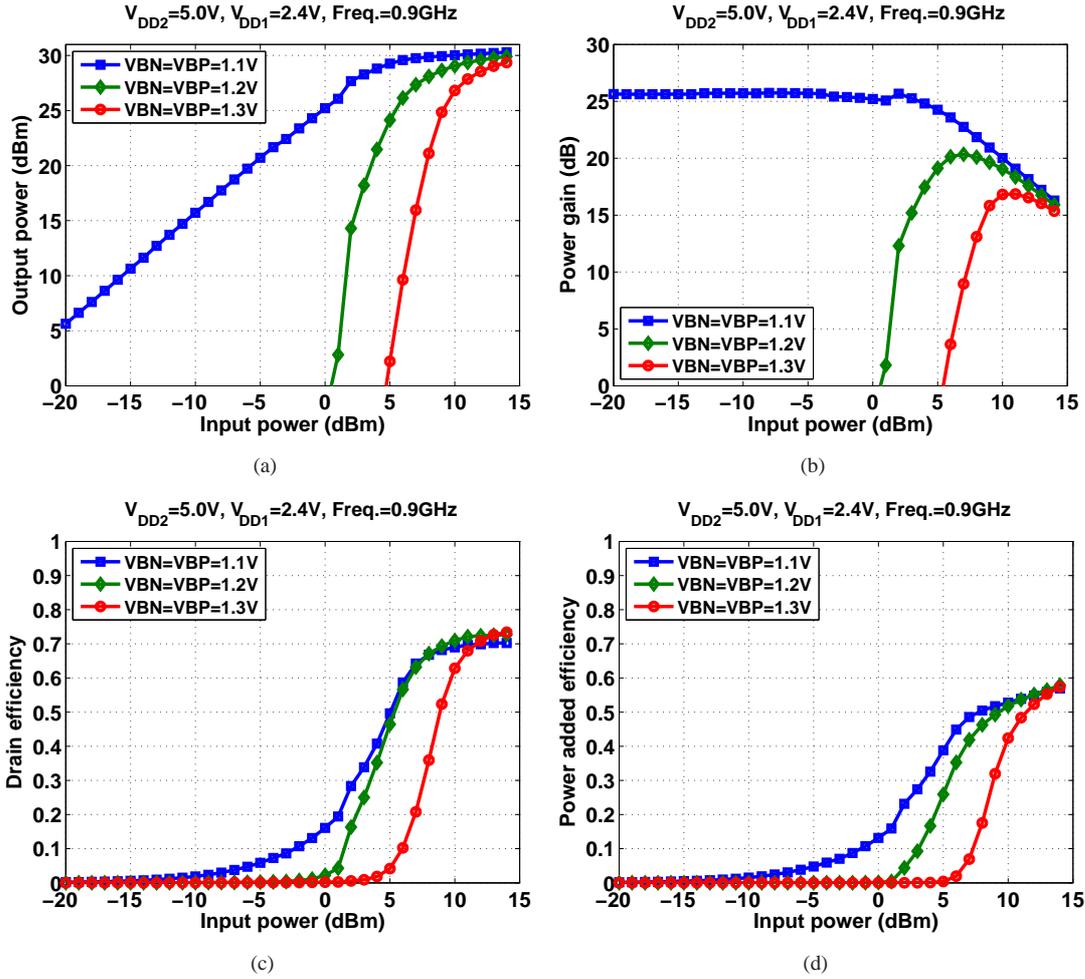
FIGURE 6.5: Measured RF input power sweep at 0.9GHz with inverter gate bias as a parameter: (a) output power, (b) power gain, (c) drain efficiency, (d) power added efficiency.

6.2.3 Dynamic Supply Voltage for ED-NMOS and Inverter

For an envelope tracking amplifier, the average efficiency is improved by dynamically modulating the supply voltage of power amplifier. Fig.6.6 shows the output power, drain efficiency, and power added efficiency as a function of supply voltage (V_{DD2}) of ED-NMOS across 500MHz to 1200MHz. The supply voltage of inverter is fixed at 2.4V, and the RF input power is also fixed at 14dBm. One can observe that when the supply voltage decreases from 5.0V to 1.0V, a 12dB output power drop is associated with that variation. The drain efficiency is quite tolerant to the changes of V_{DD2}. However, the power added efficiency decreases linearly as the supply voltage V_{DD2} decreases.

To improve PAE at power back-off, supply modulation is applied to both of ED-NMOS and inverter. Fig.6.7 plots the output power at 0.9GHz as a function of supply voltage V_{DD2} of ED-NMOS with supply voltage V_{DD1} of inverter as a parameter. V_{DD2} changes from 1.0V to 5.0V. Meanwhile, V_{DD1} changes from 1.6V to 2.4V. A power variation of 16dB is found in
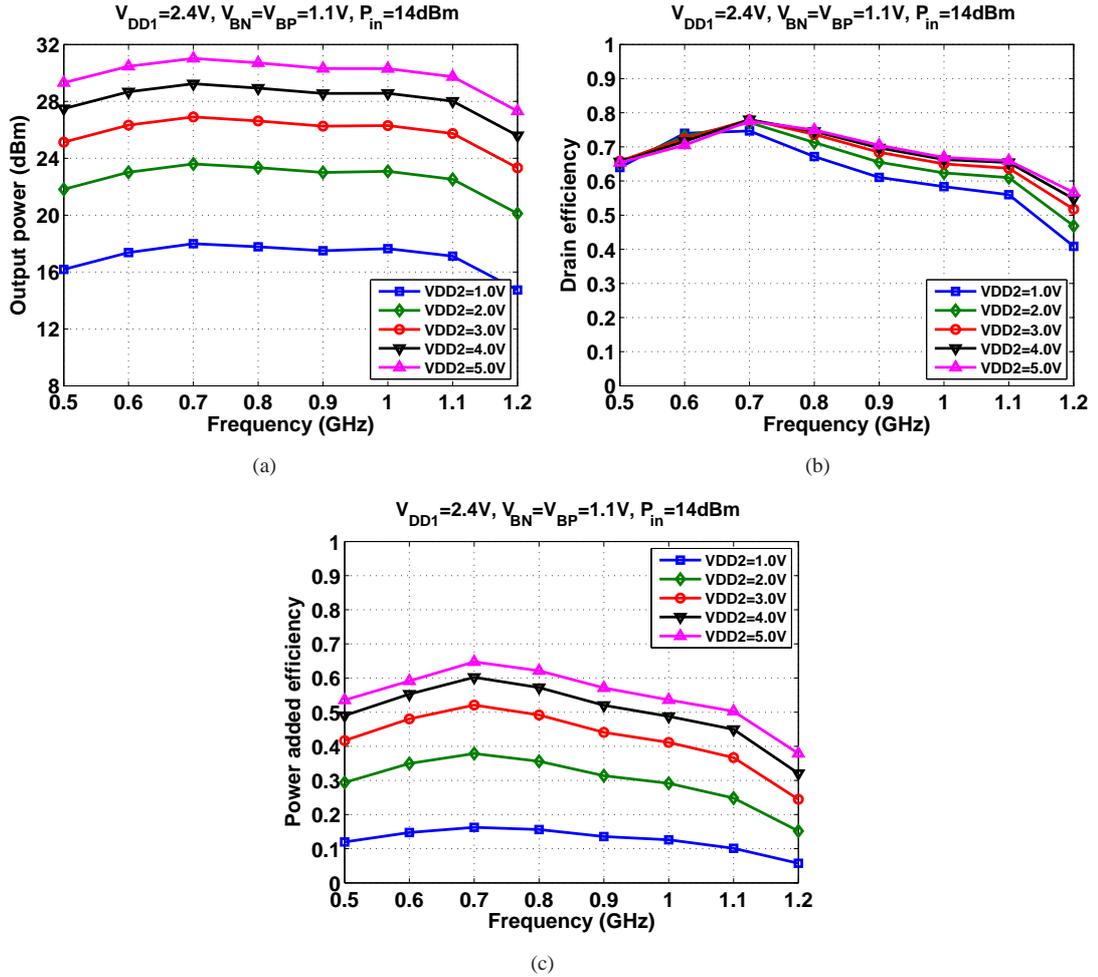
FIGURE 6.6: Broadband measurement of dynamic supply voltage for ED-NMOS: (a) output power, (b) drain efficiency, (c) power added efficiency.

that figure. The corresponding drain efficiency and PAE against the output power are shown in Fig.6.8. From Fig.6.8(b), one can observe that the PAE can be improved by decreasing V_{DD1} for low output power. For example, the PAE is increased by 27% at output power of 18dBm when decreasing V_{DD1} from 2.4V to 1.6V. Fig.6.9 plots the drain efficiency and PAE for the optimum supply voltages of ED-NMOS and inverter for different output power. It shows that the PA exhibits a 45% PAE and a 68% drain efficiency at 10dB power back-off from 30.2dBm at 0.9GHz. Fig.6.10 shows the drain efficiency and PAE against the output power for optimum supply voltages at other frequencies. It shows the PAE exceeds 40% at 10dB power back-off across 500MHz to 1100MHz.

6.2.4 Third-Order Intermodulation Distortion

The linearity of the proposed power amplifier is tested by feeding two-tone signals into the power amplifier and measuring the third-order intermodulation distortion (IMD3). Fig.6.11 shows the
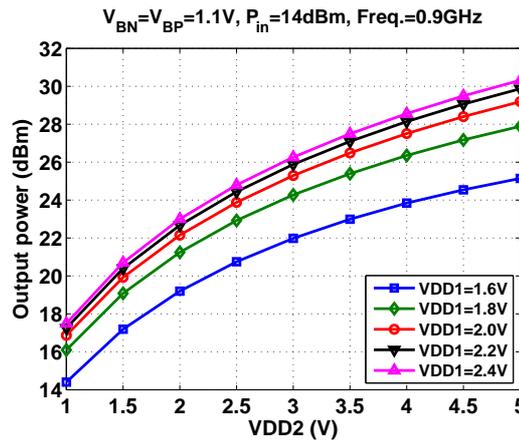
FIGURE 6.7: Measured output power as a function of V_{DD2} at 900MHz with V_{DD1} as a parameter.
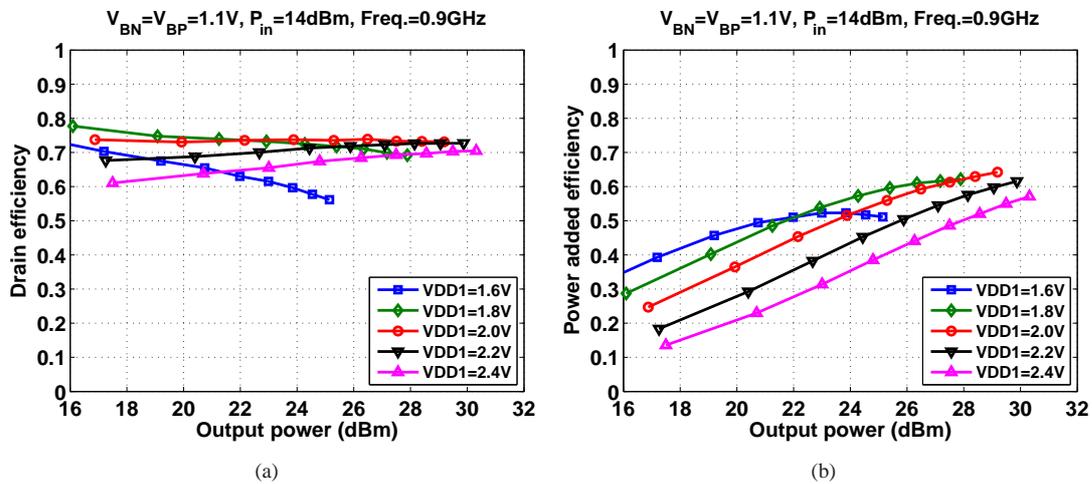
FIGURE 6.8: Efficiency against output power for the supply modulation shown in Fig.6.7: (a) drain efficiency vs.Pout, (b) PAE vs. Pout.
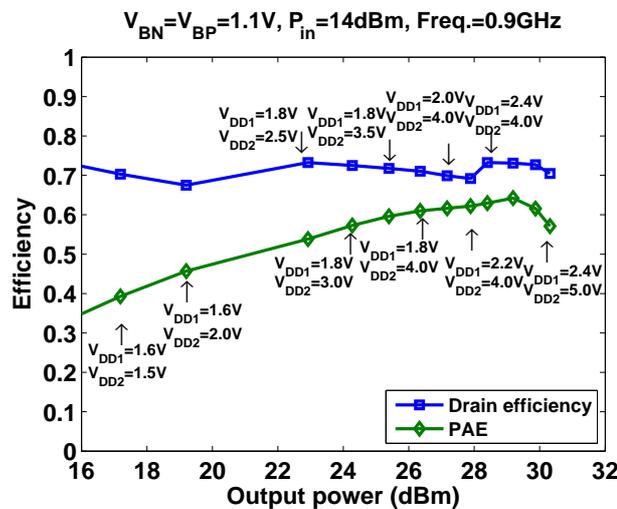
FIGURE 6.9: Measured drain efficiency and PAE with optimum supplies of ED-NMOS and Inverter.
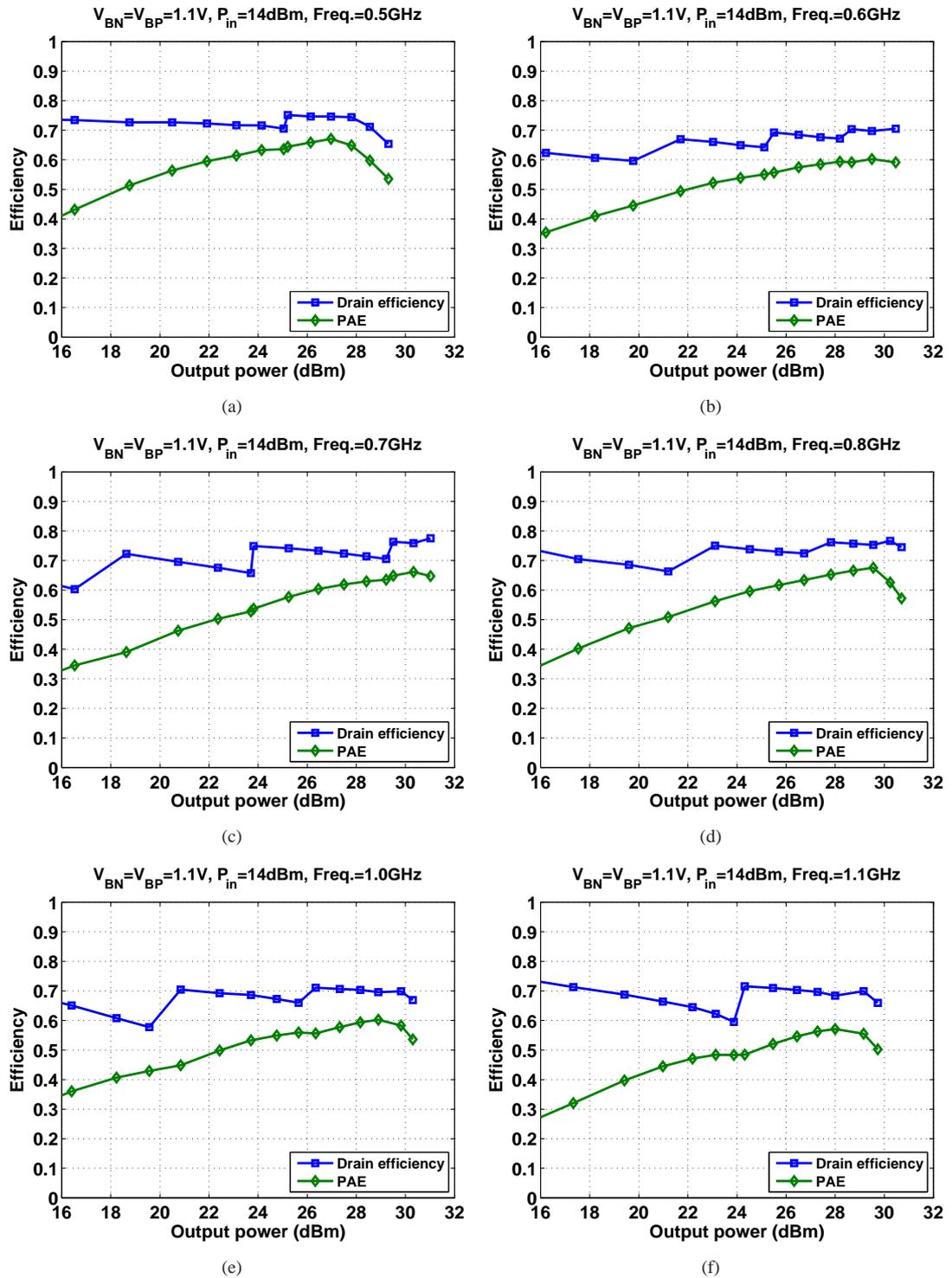
FIGURE 6.10: Measured drain efficiency and PAE versus output power for the optimum supply voltages of ED-NMOS and Inverter at: (a) 0.5GHz, (b) 0.6GHz, (c) 0.7GHz, (d) 0.8GHz, (e) 1.0GHz, and (f) 1.1GHz.
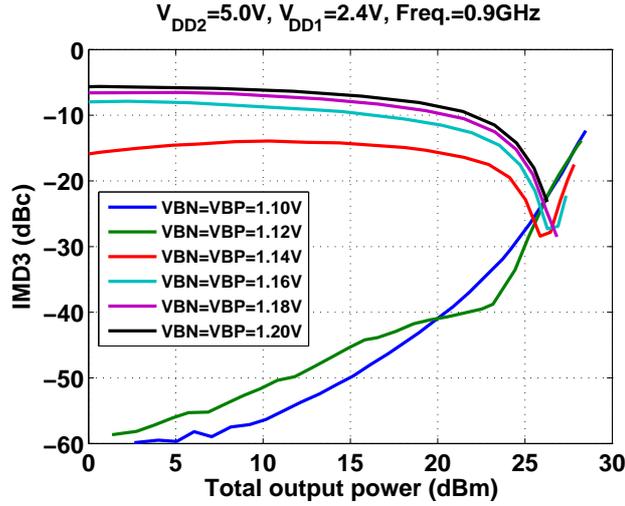
FIGURE 6.11: Measured IMD3 with VBN=VBP as a parameter at 0.9GHz

measured IMD3 at 0.9GHz as a function of total two-tone signal output power with gate bias of the inverter as a parameter. When the gate bias voltages (V_{BN} and V_{BP}) of inverter increases from 1.1V to 1.2V, the gate bias voltage of ED-NMOS decreases to or under the threshold voltage, which has been shown in Fig.5.32. Thus, the device becomes a strong non-linear amplifier so that the IMD3 performance gets worse. The optimum IMD3 of -30dBc for $P_{out} = 25dBm$ is obtained at $V_{BN} = V_{BP}$=1.12V. The IMD3, drain efficiency, and PAE versus total output power for Class-AB mode are shown in Fig.6.12 across 500MHz to 1200MHz. One can observe that the efficiency is less than 20% for IMD<-30dBc. To improve the linearity and efficiency, an advanced transmitter architecture, such as ET, LINC, or Doherty, should be implemented.

6.3   Conclusion

In this chapter, the measurement of the proposed broadband CMOS Class-E power amplifier was done. The measured results are close to the simulation. The measurement showed that the amplifier, with a 5.0V supply for ED-NMOS, 2.4V supply for inverter, 1.1V gate bias for inverter, and 14dBm RF input power, was capable of delivering more than 30dBm output power with $\eta \geq 67\%$ and $PAE \geq 52\%$ over the band 560MHz to 1050MHz. The flatness of output power is less than 1.0dB, and the fluctuations in drain efficiency and PAE are less than 13% over the same band. The measurement also indicated that the output power, power gain and PAE can be improved by increasing the gate bias voltage of ED-NMOS through decreasing the gate bias of inverter. To understand the performance at power back-off, the supply voltages of ED-NMOS and inverter were modulated. The measurement showed more than 40% PAE and 60% drain efficiency can be achieved at 10dB power back-off over the band 500MHz to 1100MHz. IMD3 measurement showed that the drain efficiency is less than 25% for $P_{out} = 25dBm$ with $IMD3 < -25dBc$ across the same frequency band.
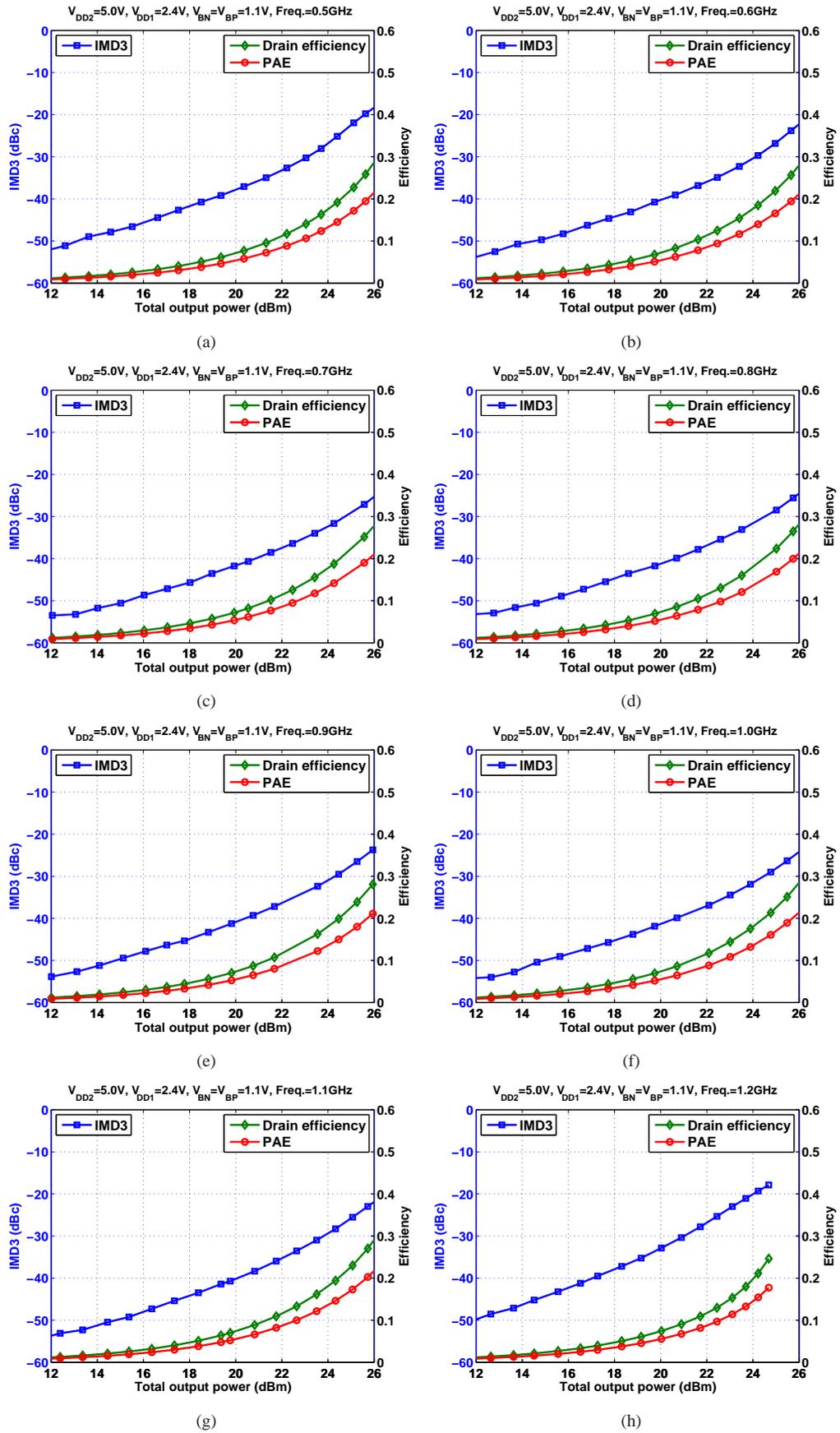
FIGURE 6.12: Measured IMD3, drain efficiency and PAE versus output power at: (a) 0.5GHz, (b) 0.6GHz, (c) 0.7GHz, (d) 0.8GHz, (e) 0.9GHz, (f) 1.0GHz, (g) 1.1GHz, and (h) 1.2GHz.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This project focused on analyzing the performance of an RF power amplifier with a Class-E like load for linear and switching operation. Meanwhile, the broadband characteristics of Class-E power amplifier is another subject. To understand the fundamental principles of the Class-E power amplifier, an analytical approach based upon mathematical derivations was applied to the conventional Class-E circuit. The non-ideal switch resistance, finite dc-feed inductance, finite loaded quality factor, and arbitrary switch duty-cycle were all taken into account to give a closed-form solution for the Class-E power amplifier. The mathematical derivations also take into account the different operation modes, such as variable voltage and variable slope. From the analytical solution, the required load impedances at fundamental and harmonic frequencies were obtained. The influence of the load impedance variation was studied. It shows that the load phase angle at fundamental frequency is the most important parameter to design. The amplifier is sensitive to that parameter. In addition, the broadband characteristics of the conventional Class-E power amplifier were discussed. Since the load phase angles of fundamental frequencies increase very fast as frequency varies, the conventional Class-E output load network cannot operate over a very broad frequency range ($\Delta B > 40\%$). Other topologies have to be used for the broadband applications.

To understand the impact of a non-ideal drive signal on the switched operation, numerical methods to represent the transistor were implemented. The simulation shows that the amplifier with finite dc-feed inductance is quite tolerant to the non-ideal drive signal. For 20% rise and fall times, the drain efficiecny is only degraded by 5% for $q = 1.81$, while for the RF choke this degradation is more than 10%. The developed transistor model was also used to analyze the linear operation of the amplifier. It showed that the gate bias voltage determines the power gain and drain efficiency when the amplifier is driven into 1dB compression point.

To analyze the linearity of the Class-E power amplifier when operating in the linear mode, a realistic compact CMOS transistor model (extended-drain NMOS) was used. The results indicated that for the Class-AB operation mode, the power amplifier with the RF choke has the best linearity or highest third-order intermodulation distortion suppression. As the gate bias voltage moves to Class-B operation, the power amplifier with finite dc-feed inductance can provide a similar IMD3 performance as the RF choke does. In addition, a broadband Class-E power amplifier based upon this CMOS device was designed and implemented to verify the developed systematic design approach. The measurements indicated a good broadband output power performance in the 560-1050MHz band, for which the output power is larger than 30dBm and output power variation is less than 1dB. The drain efficiency is between 67% and 77% and PAE is between 52% and 65% over the same band. When using the dynamic voltage supply for the ED-NMOS and inverter, the PA achieves a PAE of 40% and a drain efficiency of 60% at 10dB power back-off over the band 500MHz to 1100MHz. The IMD3 measurement shows the PA cannot provide an acceptable efficiency when requiring an IMD3 less than -30dBc. Clearly here a trade-off exists between the linearity and efficiency. To improve at this point, We could apply the envelope tracking, LINC or Doherty transmitter to achieve high efficiency and good linearity simultaneously.

7.2 Recommendations for Future Work

- In chapter 5 and 6, one can observe that the power added efficiency for this device is not very good compared with the achieved drain efficiency. This is due to the large power consumption of inverter. To improve at this point, a low-power inverter should be developed.

- To perform the digital pre-distortion, the memory effects and AM-AM and AM-PM conversion in this non-linear device should be studied. The impact of the finite dc-feed inductance on the memory effects and AM-PM conversion should be discussed.

- In [46], M. v. Schie had designed the broadband power combining network for the outphasing amplifier based upon Class-E power amplifier. In that work, the power combining network has broadband characteristics. If the output load network for each branch Class-E power amplifier is also broadband, the frequency response of the whole outphasing amplifier will be more reasonable.

Appendix A

Maple Code for Analytical Analysis

In this appendix the Maple code is shown for analytical analysis of conventional Class-E power amplifier introduced in chapter 3.

```
restart:
Digits:=10:
with(plots):
with(DiscreteTransforms):
Counter:=0:
NP:=41:
Vdd:='Vdd':
q:='q':
omega:='omega':
d:='d':
p:='p':
phi:='phi':
mon:='mon':
Con1:='Con1':
Con2:='Con2':
Coff1:='Coff1':
Coff2:='Coff2':

for j from 1 by 1 to NP do
tvcon(j):=0:
tvcoff(j):=0:
tison(j):=0:
tisoff(j):=0:
ticon(j):=0:
```

```
ticoff(j):=0:
tiron(j):=0:
tiroff(j):=0:
tilon(j):=0:
tiloff(j):=0:
ton(j):=0:
toff(j):=0:
od:


### Analytical solution for ideal Class-E power amplifier (infinite loaded quality
    factor)


### 2nd-order differential equations for ideal Class-E power amplifier in time-domain.
### Vcon(t) and Vcoff(t) are switch voltage at ON and OFF time intervals.
#eqn[1]:=diff(x(t),t$2)+(omega/mon)*diff(x(t),t)-(Vdd-x(t))*q^2*omega^2-p*Vdd*q^2*
    omega^2*cos(omega*t+phi):
#dsolve(eqn[1],x(t)):


aon:=(1/2)*(-1+sqrt(1-4*q^2*mon^2))/mon:
bon:=-(1/2)*(1+sqrt(1-4*q^2*mon^2))/mon:
Vcon(t):=Con1*exp(aon*omega*t)+Con2*exp(bon*omega*t)+Vdd+Vdd*(p*q^2*mon^2*(q-1)*(q+1)*
    cos(omega*t+phi)+p*sin(omega*t+phi)*mon*q^2)/(1+(q^4-2*q^2+1)*mon^2):


#eqn[2]:=diff(y(t),t$2)+(omega/moff)*diff(y(t),t)-(Vdd-y(t))*q^2*omega^2-p*Vdd*q^2*
    omega^2*cos(omega*t+phi):
#dsolve(eqn[2],y(t)):


aoff:=(1/2)*(-1+sqrt(1-4*q^2*moff^2))/moff:
boff:=-(1/2)*(1+sqrt(1-4*q^2*moff^2))/moff:
Vcoff(t):=Coff1*exp(aoff*omega*t)+Coff2*exp(boff*omega*t)+Vdd+Vdd*(p*q^2*moff^2*(q-1)
    *(q+1)*cos(omega*t+phi)+p*sin(omega*t+phi)*moff*q^2)/(1+(q^4-2*q^2+1)*moff^2):


### using inductor current and capacitor voltage continuities at turn-on moment, we
    can find the Con1,Con2 in terms of p,q,phi,d,omega,mon,moff,alpha,k.


eqn1:=subs(t=0,Vcon(t))-alpha*Vdd:
eqn2:=subs(t=0,(1/(p*Vdd*q^2*omega))*diff(Vcon(t),t)+alpha*Vdd/(p*Vdd*q^2*mon)-sin(
    omega*t+phi))-subs(t=2*Pi/omega,(omega*Vdd*k/(p*Vdd*q^2*omega))+alpha*Vdd/(p*Vdd*q
    ^2*moff)-sin(omega*t+phi)):


sm1:=solve({eqn1,eqn2},{Con1,Con2}):
assign(sm1):
```

```
### using Class-E contidions at turn-off moment, we can find the Coff1,Coff2 in terms
    of p,q,phi,d,omega,mon,moff,alpha,k.
eqn3:=subs(t=2*Pi/omega,Vcoff(t))-alpha*Vdd:
eqn4:=subs(t=2*Pi/omega,diff(Vcoff(t),t))-omega*Vdd*k:


sm2:=solve({eqn3,eqn4},{Coff1,Coff2}):
assign(sm2):


### using inductor current and capacitor voltage continuities at turn-off moment, we
    can find the p,phi in terms of q,d,omega,mon, moff,alpha,k.
eqn5:=subs(t=d*Pi/omega,Vcon(t))-subs(t=d*Pi/omega,Vcoff(t)):
ILond:=subs(t=d*Pi/omega,diff(Vcon(t),t)/(p*Vdd*q^2*omega)+Vcon(t)/(p*Vdd*q^2*mon)-sin
    (omega*t+phi)):
ILoffd:=subs(t=d*Pi/omega,diff(Vcoff(t),t)/(p*Vdd*q^2*omega)+Vcoff(t)/(p*Vdd*q^2*moff)
    -sin(omega*t+phi)):
eqn6:=ILond-ILoffd:


### express p and phi in terms of q,d,omega,mon, moff,alpha,k.
g1:=collect(expand(eqn5),{p,sin(phi),cos(phi)}):
g2:=coeff(g1,p,1):
a1:=coeff(g2,sin(phi)):
b1:=coeff(g2,cos(phi)):
c1:=coeff(g1,p,0):



g3:=collect(expand(eqn6*p),{p,sin(phi),cos(phi)}):
g4:=coeff(g3,p,1):
a2:=coeff(g4,sin(phi)):
b2:=coeff(g4,cos(phi)):
c2:=coeff(g3,p,0):


f[1]:=x*(ta1*sin(y)+tb1*cos(y))+tc1:
f[2]:=x*(ta2*sin(y)+tb2*cos(y))+tc2:


sm3:=solve({f[1],f[2]},{x,y}):
assign(sm3):



### set the values for input parameters Vdd, omega, d, q, mon, moff, alpha, k, loaded
    quality factor.
Counter:=Counter+1:
Vdd:=1:
omega:=1:
```

```
d:=1:

q:=1.412:

mon:=0.01:

moff:=1000:

alpha:=0:

k:=0:

LoadedQ:=2:


### calculate the values of p and phi.

ta1:=Re(evalf(a1)):

tb1:=Re(evalf(b1)):

tc1:=Re(evalf(c1)):


ta2:=Re(evalf(a2)):

tb2:=Re(evalf(b2)):

tc2:=Re(evalf(c2)):

tp:=allvalues(x):

tphi:=allvalues(y):


if Re(tp[1])>0 then

p:=Re(tp[1]):

phi:=Re(tphi[1]):

elif Re(tp[2])>0 then

p:=Re(tp[2]):

phi:=Re(tphi[2]):

end if:


TCon1:=eval(Con1):

TCon2:=eval(Con2):

TCoff1:=eval(Coff1):

TCoff2:=eval(Coff2):


### numerically express the switch voltage Vcon(t) and Vcoff(t).

TVcon(t):=TCon1*exp(aon*omega*t)+TCon2*exp(bon*omega*t)+Vdd+Vdd*(p*q^2*mon^2*(q-1)*(q
    +1)*cos(omega*t+phi)+p*sin(omega*t+phi)*mon*q^2)/(1+(q^4-2*q^2+1)*mon^2):

TVcoff(t):=TCoff1*exp(aoff*omega*t)+TCoff2*exp(boff*omega*t)+Vdd+Vdd*(p*q^2*moff^2*(q
    -1)*(q+1)*cos(omega*t+phi)+p*sin(omega*t+phi)*moff*q^2)/(1+(q^4-2*q^2+1)*moff^2):


### calculate the ideal drain efficiency and design set K.

pswitch:=int(TVcon(t)^2/mon,t=0..d*Pi/omega)+int(TVcoff(t)^2/moff,t=d*Pi/omega..2*Pi/
    omega):

pdc:=Vdd*(int(TVcon(t)/mon,t=0..d*Pi/omega)+int(TVcoff(t)/moff,t=d*Pi/omega..2*Pi/
    omega)):
```

```
Idc:=Re((omega/(2*Pi)*(int(TVcon(t)/mon,t=0..d*Pi/omega)+int(TVcoff(t)/moff,t=d*Pi/
    omega..2*Pi/omega)))):
Tpswitch:=Re(evalf(pswitch)):
Tpdc:=Re(evalf(pdc)):
ieff:=1-Tpswitch/Tpdc;


inton1:=int(TVcon(t),t=0..d*Pi/omega):
inton2:=int(TVcon(t)^2,t=0..d*Pi/omega):
intoff1:=int(TVcoff(t),t=d*Pi/omega..2*Pi/omega):
intoff2:=int(TVcoff(t)^2,t=d*Pi/omega..2*Pi/omega):


kl:=Re((p*Vdd*q)^2*Pi/(omega*((inton1*Vdd/mon-inton2/mon)+(intoff1*Vdd/moff-intoff2/
    moff)))));
kc:=1/(q^2*kl);
kp:=p^2/(2*kl^2);


vr:=int(TVcon(t)*sin(omega*t+phi),t=0..d*Pi/omega)+int(TVcoff(t)*sin(omega*t+phi),t=d*
    Pi/omega..2*Pi/omega):
vx:=int(TVcon(t)*cos(omega*t+phi),t=0..d*Pi/omega)+int(TVcoff(t)*cos(omega*t+phi),t=d*
    Pi/omega..2*Pi/omega):
kx:=Re(vx/vr);


mr:=evalf(kc/mon); # mr:=R/Ron:


if evalf(kx)>=0 then
QL:=evalf(LoadedQ+kx):
QC:=evalf(LoadedQ):
elif evalf(kx)<0 then
QL:=evalf(LoadedQ):
QC:=evalf(LoadedQ-kx):
end if:


T:=2*Pi/omega:
td:=d*T/2:



### Solve the 4th-order differential equations for Class-E power amplifier with finite
    loaded quality factor.


#constants in the differential equations


Ca1:='Ca1':
Cb1:='Cb1':
```

```
Cc1:='Cc1':
Cd1:='Cd1':


Ca2:='Ca2':
Cb2:='Cb2':
Cc2:='Cc2':
Cd2:='Cd2':


ca1:='ca1':
cb1:='cb1':
cc1:='cc1':
cd1:='cd1':


ca2:='ca2':
cb2:='cb2':
cc2:='cc2':
cd2:='cd2':


sa1:='sa1':
sb1:='sb1':
sc1:='sc1':
sd1:='sd1':
se1:='se1':
sf1:='sf1':
sa2:='sa2':
sb2:='sb2':
sc2:='sc2':
sd2:='sd2':
se2:='se2':
sf2:='sf2':


sa1:=(QL/QC)*(1/(omega^4*q^2)):
sb1:=(QL/QC)*(1/omega^3)*(1/(q^2*mon))+1/(QC*omega^3*q^2):
sc1:=1/(QC*omega^2*q^2*mon)+1/(omega^2*q^2)+1/(omega^2*q^2*QC*mr*mon)+(QL/QC)*(1/omega
    ^2):
sd1:=1/(QC*omega)+1/(omega*q^2*mon):
se1:=1:
sf1:=-Vdd:


sa2:=(QL/QC)*(1/(omega^4*q^2)):
sb2:=(QL/QC)*(1/omega^3)*(1/(q^2*moff))+1/(QC*omega^3*q^2):
sc2:=1/(QC*omega^2*q^2*moff)+1/(omega^2*q^2)+1/(omega^2*q^2*QC*mr*mon)+(QL/QC)*(1/
    omega^2):
```

```
sd2:=1/(QC*omega)+1/(omega*q^2*moff):
se2:=1:
sf2:=-Vdd:


S11:=fsolve(sa1*_Z^4+sb1*_Z^3+sc1*_Z^2+sd1*_Z+se1, _Z, complex):
ca1:=S11[1]:
cb1:=S11[2]:
cc1:=S11[3]:
cd1:=S11[4]:


S22:=fsolve(sa2*_Z^4+sb2*_Z^3+sc2*_Z^2+sd2*_Z+se2, _Z, complex):
ca2:=S22[1]:
cb2:=S22[2]:
cc2:=S22[3]:
cd2:=S22[4]:


# Capacitor C1 voltage:
RVc[1](t):=Ca1*exp(ca1*t)+Cb1*exp(cb1*t)+Cc1*exp(cc1*t)+Cd1*exp(cd1*t)-1/se1*sf1:
RVc[2](t):=Ca2*exp(ca2*t)+Cb2*exp(cb2*t)+Cc2*exp(cc2*t)+Cd2*exp(cd2*t)-1/se2*sf2:


# Inductor L1 voltage:
RVL1[1](t):=(QL/QC)*(1/omega^2)*diff(RVc[1](t),t$2):
RVL1[2](t):=(QL/QC)*(1/omega^2)*diff(RVc[2](t),t$2):


# switch voltage:
RVs[1](t):=(QL/QC)*(1/omega^2)*diff(RVc[1](t),t$2)+1/(QC*omega)*diff(RVc[1](t),t)+RVc
    [1](t):
RVs[2](t):=(QL/QC)*(1/omega^2)*diff(RVc[2](t),t$2)+1/(QC*omega)*diff(RVc[2](t),t)+RVc
    [2](t):


# Load resistor voltage:
RVr[1](t):=(1/(QC*omega))*diff(RVc[1](t),t):
RVr[2](t):=(1/(QC*omega))*diff(RVc[2](t),t):


# Lnductor L voltage:
RVl[1](t):=(1/(QC*omega))*diff(RVc[1](t),t)+(mr*mon/omega)*diff(RVs[1](t),t)+mr*RVs
    [1](t):
RVl[2](t):=(1/(QC*omega))*diff(RVc[2](t),t)+(mr*mon/omega)*diff(RVs[2](t),t)+(mon/moff
    )*mr*RVs[2](t):


### using inductor current and capacitor voltage continuities at turn-on moment and t=
    td, we can find the values of Ca1,Cb1,Cc1,Cd1,Ca2,Cb2,Cc2,Cd2.
# Capacitor charge continuity
```

```
eq1:=(subs(t=td,RVc[1](t))-subs(t=td,RVc[2](t))):
eq2:=(subs(t=0,RVc[1](t))-subs(t=T,RVc[2](t))):
eq3:=(subs(t=td,RVs[1](t))-subs(t=td,RVs[2](t))):
eq4:=(subs(t=0,RVs[1](t))-subs(t=T,RVs[2](t))):


# Inductor flux continuity
eq5:=(subs(t=td,RVr[1](t))-subs(t=td,RVr[2](t))):
eq6:=(subs(t=0,RVr[1](t))-subs(t=T,RVr[2](t))):
eq7:=(subs(t=td,RVl[1](t))-subs(t=td,RVl[2](t))):
eq8:=(subs(t=0,RVl[1](t))-subs(t=T,RVl[2](t))):



sm4:=fsolve({eq1,eq2,eq3,eq4,eq5,eq6,eq7,eq8},{Ca1,Cb1,Cc1,Cd1,Ca2,Cb2,Cc2,Cd2}):
assign(sm4):

### express the current and voltage in numbers.
RVc[1](t):=Ca1*exp(ca1*t)+Cb1*exp(cb1*t)+Cc1*exp(cc1*t)+Cd1*exp(cd1*t)-1/se1*sf1:
RVc[2](t):=Ca2*exp(ca2*t)+Cb2*exp(cb2*t)+Cc2*exp(cc2*t)+Cd2*exp(cd2*t)-1/se2*sf2:


RVs[1](t):=(QL/QC)*(1/omega^2)*diff(RVc[1](t),t$2)+1/(QC*omega)*diff(RVc[1](t),t)+RVc
    [1](t):
RVs[2](t):=(QL/QC)*(1/omega^2)*diff(RVc[2](t),t$2)+1/(QC*omega)*diff(RVc[2](t),t)+RVc
    [2](t):


RVL1[1](t):=(QL/QC)*(1/omega^2)*diff(RVc[1](t),t$2):
RVL1[2](t):=(QL/QC)*(1/omega^2)*diff(RVc[2](t),t$2):


RVr[1](t):=(1/(QC*omega))*diff(RVc[1](t),t):
RVr[2](t):=(1/(QC*omega))*diff(RVc[2](t),t):
 Idc:=Re(int((1/(QC*mr*mon))*diff(RVc[1](t),t)+diff(RVs[1](t),t)+omega*RVs[1](t)/mon,t
    =0..td)+int((1/(QC*mr*mon))*diff(RVc[2](t),t)+diff(RVs[2](t),t)+omega*RVs[2](t)/
    moff,t=td..T))/T;


Nir[1](t):=Re(1/(mr*QC*mon)*diff(RVc[1](t),t))/Idc:
Nir[2](t):=Re(1/(mr*QC*mon)*diff(RVc[2](t),t))/Idc:
Nic[1](t):=Re(1*diff(RVs[1](t),t))/Idc:
Nic[2](t):=Re(1*diff(RVs[2](t),t))/Idc:
Nis[1](t):=Re(1*omega/mon*RVs[1](t))/Idc:
Nis[2](t):=Re(1*omega/moff*RVs[2](t))/Idc:


### calculate the DC power, switch power, and output power.
Pdc:=Vdd*Idc;
```

```
Ps:=Re(evalf(int(omega*RVs[1](t)^2/mon,t=0..td)+int(omega*RVs[2](t)^2/moff,t=td..T)))/
    T;
PL:=Re(evalf(1/(mr*QC^2*mon*omega)*(int(diff(RVc[1](t),t)^2,t=0..td)+int(diff(RVc[2](t
    ),t)^2,t=td..T))))/T;



Vr0:=(1/(2*Pi))*(int(RVr[1](t),t=0..td)+int(RVr[2](t),t=td..T)):


va1:=(2/T)*(int(RVr[1](t)*cos(omega*t),t=0..td)+int(RVr[2](t)*cos(omega*t),t=td..T)):
vb1:=(2/T)*(int(RVr[1](t)*sin(omega*t),t=0..td)+int(RVr[2](t)*sin(omega*t),t=td..T)):
Vr1(t):=va1*cos(omega*t)+vb1*sin(omega*t):
va2:=(2/T)*(int(RVr[1](t)*cos(2*omega*t),t=0..td)+int(RVr[2](t)*cos(2*omega*t),t=td..T
    )):
vb2:=(2/T)*(int(RVr[1](t)*sin(2*omega*t),t=0..td)+int(RVr[2](t)*sin(2*omega*t),t=td..T
    )):
Vr2(t):=va2*cos(2*omega*t)+vb2*sin(2*omega*t):
va3:=(2/T)*(int(RVr[1](t)*cos(3*omega*t),t=0..td)+int(RVr[2](t)*cos(3*omega*t),t=td..T
    )):
vb3:=(2/T)*(int(RVr[1](t)*sin(3*omega*t),t=0..td)+int(RVr[2](t)*sin(3*omega*t),t=td..T
    )):
Vr3(t):=va3*cos(3*omega*t)+vb3*sin(3*omega*t):
Pr1:=Re(evalf((omega/(mr*mon))*int(Vr1(t)^2,t=0..T)))/T:
Pr2:=Re(evalf((omega/(mr*mon))*int(Vr2(t)^2,t=0..T)))/T:
Pr3:=Re(evalf((omega/(mr*mon))*int(Vr3(t)^2,t=0..T)))/T:

### calculate the real drain efficiency.
eff:=Pr1/Pdc;



pvs1:=plot(Re(RVs[1](t)/Vdd),t=0..td,title="Switch Voltage",labels=['t','Vs(t)/VDD'],
    thickness=3):
pvs2:=plot(Re(RVs[2](t)/Vdd),t=td..T,title="Switch Voltage",labels=['t','Vs(t)/VDD'],
    thickness=3):


pis1:=plot(Re(Nis[1](t)),t=0..td,title="Switch current",labels=['t','Is(t)/IDC'],view
    =[0..T,-10..10],thickness=3):
pis2:=plot(Re(Nis[2](t)),t=td..T,title="Switch current",labels=['t','Is(t)/IDC'],view
    =[0..T,-10..10],thickness=3):


pir1:=plot(Re(Nir[1](t)),t=0..td,title="Resistor current",view=[0..T,-3..3],labels=['t
    ','Ir(t)/IDC'],thickness=3):
```

```
pir2:=plot(Re(Nir[2](t)),t=td..T,title="Resistor current",view=[0..T,-3..3],labels=['t
    ','Ir(t)/IDC'],thickness=3):


pic1:=plot(Re(Nic[1](t)),t=0..td,title="Capacitor current",view=[0..T,-10..10],labels
    =['t','Ic(t)/IDC'],thickness=3):
pic2:=plot(Re(Nic[2](t)),t=td..T,title="Capacitor current",view=[0..T,-10..10],labels
    =['t','Ic(t)/IDC'],thickness=3):


VSPLOT:=display(pvs1,pvs2):
ISPLOT:=display(pis1,pis2):
IRPLOT:=display(pir1,pir2):
ICPLOT:=display(pic1,pic2):



### plot the current and voltage waveforms
VSPLOT;
ISPLOT;
IRPLOT;
ICPLOT;
```

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