A 10-bit 25Msps Pipeline ADC for Companding Baseband Processing in Wireless Application

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Abstract

This is a 10-bit 25Msps pipeline analog-to-digital converter design.

Direct conversion radio frequency (RF) receiver shows the greatest potential to meet commercial trends especially for Wireless LAN application. Except for RF frond-end, analog baseband interface is important to filter and digitize signal coming from down-converter. To be adaptive to large dynamic range requirement, conventional baseband circuit is realized by a combination of channel selection filter, automatic-gain-control (AGC) and Nyquist rate ADC. However there are several disadvantages on AGC loop: 1) subjected to presence of large interferences, allowable AGC gain is limited and AGC is generally distributed through the overall baseband chain to amplify signal and attenuate interference. 2) AGC gain settings are fixed after setting behavior even though input signal strength might vary, this requires large headroom of dynamic range (DR) especially for high Peak-to-Average Power Ratio (PAPR). 3) Large DR implies a longer setting time of AGC loop which is not allowable.

An alternate, less expensive way to improve DR of baseband without AGC is companding system, in which gain control works all the time adaptively during data processing. The input gain element compresses the high dynamic range input signal, which is then processed by the low dynamic range signal processor (filter and ADC) followed by expansion cell as output gain element. The compressing filter has been realized[1]. This thesis focuses on expanding ADC design for companding analog baseband interface. The pipelined ADC, based on switched capacitor (SC) technique, has most successfully covered resolution and sampling rate requirements of 802.11 standard. In this thesis, a 10-bit 25Msps pipline ADC with digital expander as back-end processor is designed in IBM 130nm CMOS technology at 1.2V power supply. The specifications of ADC is derived from WLAN 802.11 standard. Then overall optimization of pipeline ADC in the format of stage scaling down is analyzed while special attention is paid to various error sources degrading ADC linearity. At the circuit level, high performance topologies of essential blocks have been developed such as two stage switched OTA with

gain boosting and bootstrapping switch for highly linear sampling. Emphasis is given on dynamic comparator. A mismatch insensitive topology is proposed due to digital correction.

Finally the pipelined ADC core consumes 28mW with 60.3dB SNDR, 78dB SFDR and 76dB IMD3 is obtained. Combined with expander, extra 12dB DR is achieved with equal dynamic performance because companding takes place. Compared to conventional baseband interface, power dissipation is reduced by a factor of 3.3.

Acknowledgments

Researching a thesis is a unique exploration. One tries to look into the depth of the unknown and find answers to a question that does not necessarily have an answer. In some cases your conclusion fits the question, in some cases not. It would be much more difficult to continue research by myself excluding other ones' self-giving help. There are many teachers and friends who have helped this piece of work take form.

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1 Introduction

1.1 Background

A wireless local area network (WLAN) system, shown in its most general form in Fig. 1.1, consists of a network hardware backbone, along with a series of detached components [2]. These detached components may include computer desktops, computer laptops, personal digital assistants (PDAs), cell phones, gaming systems, security cameras, printers and appliances as clients. Using radio-frequency (RF) technology, the WLAN system allows clients to access local area network (LAN) resources while physically being detached from this network. At the same time, the clients are capable of communicating with one another (typically indirectly and through access points rather than peer-to-peer networks) while physically being detached from one another.

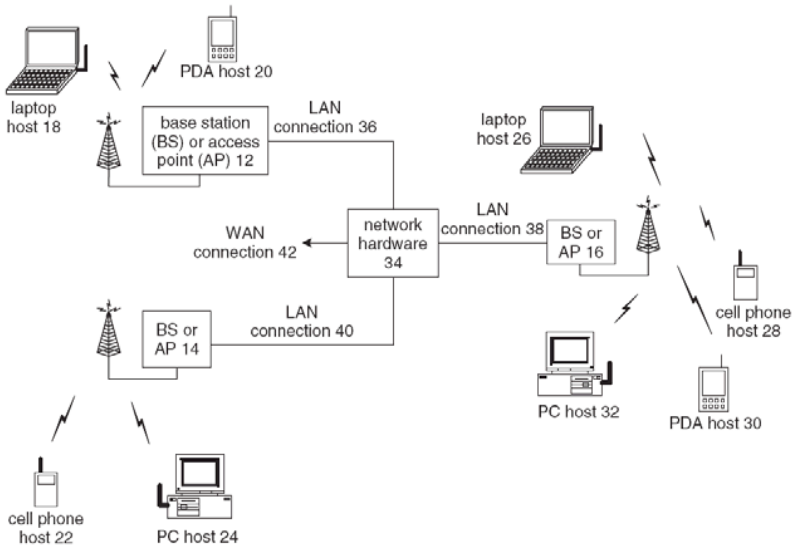


Figure 1.1: Example of WLAN network displaying various associated nodes and backbone network [2]

1.2 Wireless standard

To obtain ADC specification (analyzed in Chapter3), WLAN standard should be investigated at first. There are various WLAN standards, such as HyperLAN and the Institute of Electrical and Electronics Engineers (IEEE) 802.11. But now, in the United States, Europe, the Far East, as well as elsewhere in world, 802.11 has become the standard choice for WLAN and will therefore be emphasized in my research. The 802.11 is a specific standard that defines the medium access control (MAC) and physical (PHY) layers of a LAN.

1.2.1 802.11

The original 802.11 standard is a MAC standard plus a low data rate PHY which supports only 1 and 2Mbps data rate. This first version of the standard operates at the 2.4GHz industrial, scientific, and medical (ISM) band and allows the vendors to choose between a direct sequence spread spectrum (DSSS) and a frequency hopping spread spectrum (FHSS) implementations.

1.2.2 802.11b

802.11b is a PHY extension to the original 802.11 standard. It operates at the 2.4GHz band and allows for higher data rate of 5.5 and 11Mbps. It uses a technique known as complementary code keying (CCK) [7].

As shown in Fig. 1.2a, there are 11 designated channels [3][8] in the 802.11b/g band in the United States and additional 3 (not shown) belongs to other regions in the frequency range from 2.4 to 2.5GHz. However, as shown in Fig. 1.2b, there are only three non-overlapping channels that can transmit data. The channels are 5MHz apart with bandwidth 20MHz. In the United States channels 1, 6 and 11 are typically used to minimize overlap and therefore reduce interfere between operating devices.

The maximum allowed transmit power in the United States for the 802.11b/g is 30dBm or 1W. This is quite a high transmit power, and most 802.11b/g solutions today operate at significantly lower transmit power (in the range of 15 to 22dBm).

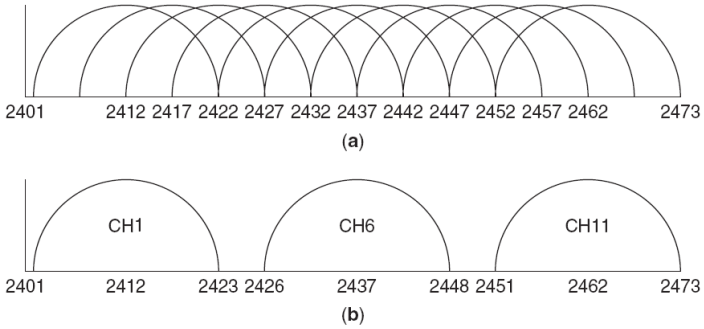


Figure 1.2: IEEE 802.11b channel allocations. Note that the overlap channels (a) as well as the three distinct (non-overlapping) channels (b) [3]

Table 1.1: 802.11b/g channel allocation in different regions

channel	Center frequency [Mhz]	Frequency range [MHz]	FCC USA	IC Canada	ETSI EU	Spain	France	MKK Japan
1	2412	2400∼2422	✓	✓	✓	-	-	-
2	2417	2407∼2427	✓	✓	✓	-	-	-
3	2422	2412∼2432	✓	✓	✓	-	-	-
4	2427	2417∼2437	✓	✓	✓	-	-	-
5	2432	2422∼2442	✓	✓	✓	-	-	-
6	2437	2427∼2447	✓	✓	✓	-	-	-
7	2442	2432∼2452	✓	✓	✓	-	-	-
8	2447	2437∼2457	✓	✓	✓	-	-	-
9	2452	2442∼2462	✓	✓	✓	-	-	-
10	2457	2447∼2467	✓	✓	✓	✓	✓	-
11	2462	2452∼2472	✓	✓	✓	✓	✓	-
12	2467	2457∼2477	-	-	✓	-	✓	-
13	2472	2462∼2482	-	-	✓	-	✓	-
14	2477	2467∼2487	-	-	-	-	-	✓

802.11b/g channel allocation in different regions is shown in Table 1.1 and Table 1.2 shows its data rate, modulation type and required sensitivity.

Table 1.2: 802.11b/g data rate, modulation type and required sensitivity [3]

Data rate [Mbps]	Modulation	Sensitivity [dBm]
1	D-BPSK	-80
2	D-QPSK	-
5.5	CCK	-
11	CCK	-76

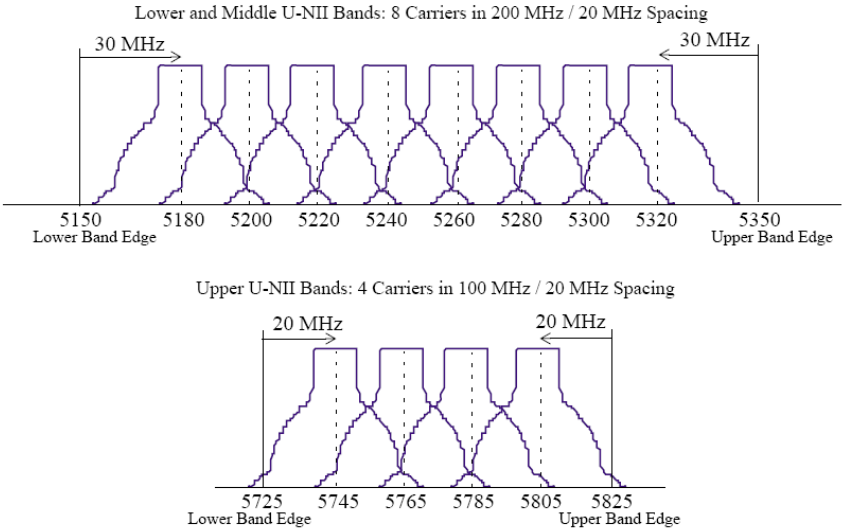


Figure 1.3: Lower, mid and upper U.S. 802.11a bands [4]

1.2.3 802.11a

802.11a is another PHY extension to the original 802.11 standard. It operates at 5GHz unlicensed national infrastructure for information (UNII) band and allows for data rates of 6-54Mbps. It uses a technique known as orthogonal frequency division multiplexing (OFDM).

To be different from 802.11b/g's channel allocation, 802.11a has more non-overlapping channels available to users. One of the advantages compared to 802.11g standard becomes apparent in Fig. 1.3: There are currently a total of 12 non-overlapping channels available in the United States with proposals at the FCC to open up even more spectrum in the 5GHz band as part of an expanded unlicensed National Information Infrastructure (UNII) spectrum [4]. The large number of channels available in the 802.11a

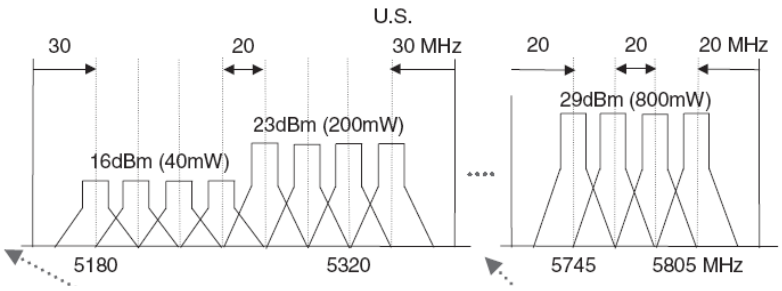


Figure 1.4: Different transmit power depend on different band of 802.11a [4]

Table 1.3: Channel allocation of 802.11a

channel	class	center frequency [MHz]	frequency range [MHz]	FCC USA
1∽35	-	5005∽5175	-	-
36	UNII Lower band	5180	5150∽5190	✓
40	UNII Lower band	5200	5190∽5210	✓
44	UNII Lower band	5220	5210∽5230	✓
48	UNII Lower band	5240	5230∽5250	✓
52	UNII Mid band	5260	5250∽5270	✓
56	UNII Mid band	5280	5270∽5290	✓
60	UNII Mid band	5300	5290∽5310	✓
64	UNII Mid band	5320	5310∽5350	✓
65∽148	-	5325∽5740	-	-
149	UNII Upper band	5745	5725∽5755	✓
153	UNII Upper band	5765	5755∽5775	✓
157	UNII Upper band	5785	5775∽5795	✓
161	UNII Upper band	5805	5795∽5825	✓

band allow for much higher overall network capacity and less inter-channel interfere. 802.11a channel allocation in different regions is shown in Table 1.3.

In the United States the maximum allowed transmit power for the 802.11a standard is dependent on the sub-band (Fig. 1.4). In the lower, mid, and higher 802.11a sub-bands, the maximum transmit power is limited to 16, 23, and 29dBm, respectively. The higher sub-band is primarily intended for long-range outdoor communications.

1.2.4 802.11g

802.11g was the second extension to the 802.11 standard. It operates at the 2.4GHz ISM band and allows for data rates ranging from 1 to 54Mbps [3][8]. The 1 and 2Mbps rates are obtained in the DSSS mode whereas 5.5 and 11Mbps rates come from CCK mode. Additionally, rates at 6 to 54Mbps are operated in OFDM mode. 802.11g standard borrows the OFDM technique and data rates from the 802.11a but operates at 2.4GHz ISM band. It can therefore operate at very high data rates while being backward compatible with 802.11b standard. So 802.11g has the same channel allocation as 802.11b and same data rate and performance as 802.11a.

The most important characteristic about different standards is data rate. In a real system, control of actual data rate selected by the link is done through the media access controller. The goal of MAC is to establish the fastest (but reliable) link. As such, it typically starts at the highest data rate and tries to establish a robust link. If it fails to do so, it will drop the rate to a lower one and retry. This process will continue until it establishes a link or determines that no link can be established[8].

Here the general way to calculate data rate of 802.11 a/g is given by the following modulation-related parameters: (a) modulation order (b) coding rate.

$$R_{data} = N_{sub} \times R_{symbol} \times N_{order} \times R_{code} \tag{1.1}$$

Where R_{data} is data rate, N_{sub} is number of sub-carriers, $R_{symbol}$is symbol transfer rate, $N_{order}$is modulation order and R_{code} is code rate based on modulation. The code rate determines the amount of redundancy and hence robustness built into the modulation. The closer the coding rate to unity, the less amount of redundancy built in, and the higher the data rate (the data are not "wasted" for the sake of redundancy). Now considering the 802.11a/g at Quadrature Amplitude Modulation (QAM)-64 modulation mode with code rate 0.75 and 48 sub-carriers for data transmission, the data rate is $48 \times 250ksps \times \log_2 64 \times 0.75 = 54Mbps$.

The IEEE 802.11a/g standards require any system that claims compatibility being able to maintain certain minimum sensitivity levels (ranging from -65 to -82dBm for

Table 1.4: 802.11a/g data rate, modulation type, coding rate and required sensitivity together with channel rejection [4]

Data rate [Mbps]	Modulation	Code rate	Sensitivity [dBm]	Adjacent channel rejection [dB]	Alternate Adjacent channel rejection
6	***BPSK***	***0.5***	***-82***	***16***	***32***
9	BPSK	0.75	-81	15	31
12	QPSK	0.5	-79	13	29
18	QPSK	0.75	-77	11	27
24	QAM-16	0.5	-74	8	24
36	QAM-16	0.75	-70	4	20
48	QAM-64	0.67	-66	0	16
54	***QAM-64***	***0.75***	***-65***	***-1***	***15***

the various data rates). The minimum required sensitivity level by the standard for the various data rates is listed in Table.1.4.

As the data rates increasing (through increasing modulation order or by using higher coding rate), the minimum sensitivity level suffers. This is related to the larger Signal-to-Noise-Ratio (SNR) required by the higher data rates. In other words, as the data rate increases, a higher received power level is required in order to be able to receive the signal (assuming noise levels stay constant). Actually ADC's specification would be defined based on the higher side limitation, QAM-64 and lower side limitation BPSK with 6Mbps data rate. It is useful to make a summary on Table 1.4. For 802.11g, this table only shows the OFDM-related rates. As mentioned earlier, 802.11g is backward compatible with 802.11b and is capable of operating at all the lower data rates (11, 5.5, 2, 1Mbps).

Finally the comparison between three WLAN standards is shown in Table 1.5. From data rates, sensitivity and adjacent channel rejection listed above, ADC specification could be defined in Chapter3.

Table 1.5: Comparison between 802.11b/a/g standard

	Band [GHz]	Available spectrum [MHz]	Non-overlapping channels	Modulation	Data rate [Mbps]
802.11a	5	300	12	OFDM	6∽54
802.11b	2.4	83.5	3	DSSS CCK	1∽11
802.11g	2.4	83.5	3	DSSS CCK OFDM	1∽54

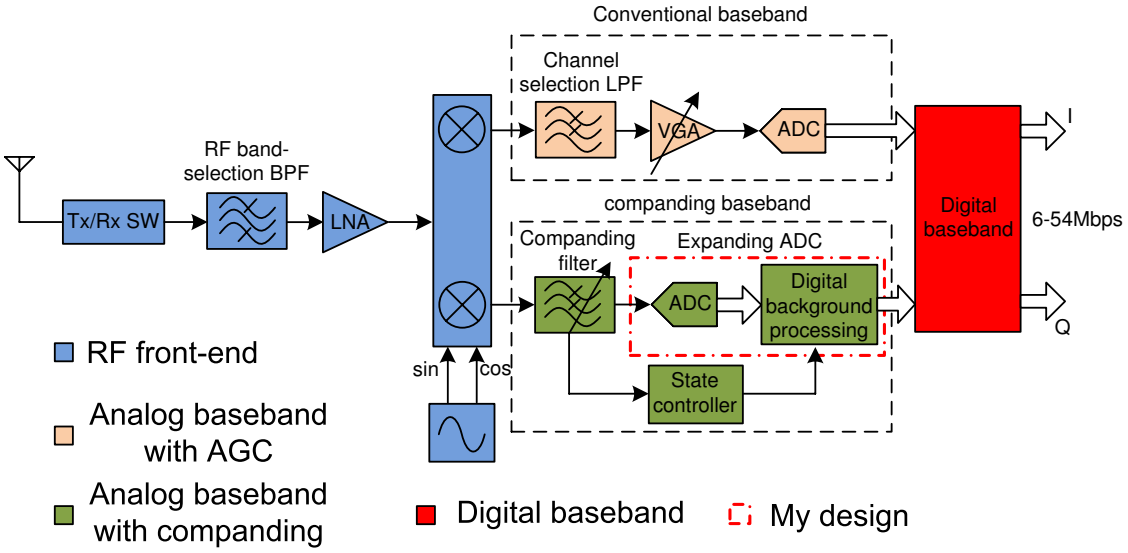


Figure 1.5: Direct conversion receiver block diagram with conventional AGC in I channel and companding baseband in Q channel

1.3 Motivation

Direct conversion (shown in Fig. 1.5) is an alternative wireless receiver architecture to the well-established superheterodyne, particularly for highly integrated, low-power terminals, such as WLAN applications. Its fundamental advantage is that the received signal is amplified and filtered at baseband rather than at some high intermediate frequency. This means lower current drain in the amplifiers and active filters while a simpler task of image-rejection [9]. Our receiver baseband interface is designed for 802.11a/g WLAN. To be adaptive to large dynamic range requirement, conventional baseband circuit is realized by a combination of channel selection filter, automatic-gain-control (AGC) and Nyquist rate ADC as shown I channel in Fig. 1.5. However there

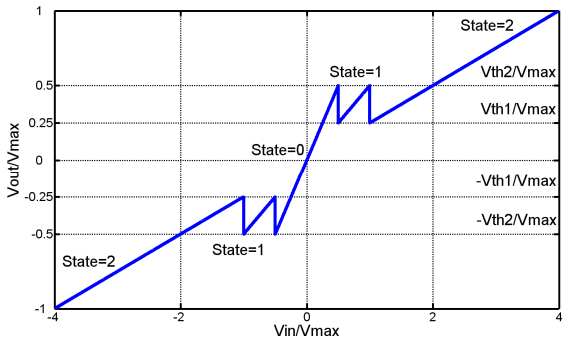
are several disadvantages on AGC loop: 1) subjected to presence of large interferes, allowable AGC gain is limited and AGC is generally distributed through the overall baseband chain to amplify signal and attenuate interfere. 2) AGC gain settings are fixed after setting behavior even though input signal strength might vary, this requires large headroom of DR especially for high Peak-to-Average Power Ratio (PAPR). 3) Large DR implies a longer setting time of AGC loop which is not allowable. For instance, in WLAN 802.11a/g using OFDM modulation the settling time for AGC loop is quite small ($< 6\mu s$).

To improve conventional baseband signal processing circuit, a new configuration of baseband interface: companding (combination of compressing and expanding) including an input gain element, a signal processor and output gain element in conception. The input gain element compresses the high dynamic range input signal, which is then processed by the low dynamic range signal processor (filter and ADC) followed by expansion cell as output gain element. In a practical way, companding baseband is composed of a SC compressing filter (has been realized [1]) and expanding ADC without AGC is carried out as shown in Fig. 1.5. Compressing filter's transfer function is shown in Fig. 1.6(a) and Fig. 1.6(b) with filtering corner frequency at 10MHz [1]. Eq1.2 gives mathematical description between input and output with adaptive varying statement.

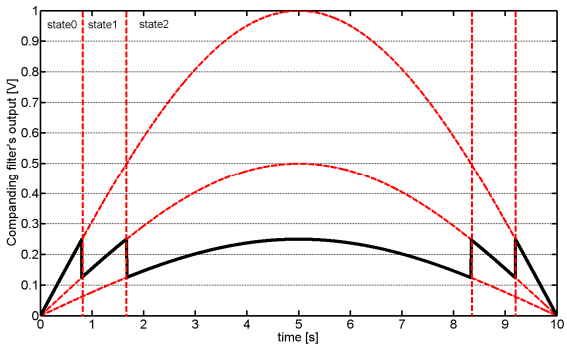
$$V_{out} = \begin{cases} V_{in}, & 0 \leq V_{in} \leq 0.25V_{ref} \\ 0.5 \times V_{in}, & 0.25 \leq V_{in} \leq 0.5V_{ref} \\ 0.25 \times V_{in}, & 0.5 \leq V_{in} \leq V_{ref} \end{cases} \tag{1.2a}$$

$$State = \begin{cases} 00, & 0 \leq V_{in} \leq 0.25V_{ref} \\ 01, & 0.25 \leq V_{in} \leq 0.5V_{ref} \\ 11, & 0.5 \leq V_{in} \leq V_{ref} \end{cases} \tag{1.2b}$$

Compressing filter not only works as channel selection filter which attenuates the adjacent and alternate adjacent channel rejection, but also works as AGC to limit signal level dependent on input level adaptively. At the same time together with output signal, there is a variable 'state' in two bits binary form restoring the statements due



(a)



(b)

Figure 1.6: Channel selection filter in baseband interface: a) Gain compressing dependant on different input strength b) companding gain control on sine-wave

to different conditions, such as 00, 01, 11 for low, mid, high input range respectively [1].

New baseband circuit implemented with companding would easily relax dynamic range for filter and ADC compared to the one without companding by 12dB which means reducing in power consumption by a factor of 4 at equal DR. Companding baseband only costs a digital background processing block as expander after ADC to recover compressed input to initial condition. After all, expander consumes less power and becomes easier to design [10].

Another aspect has to be mentioned is that output signal of compressing filter is a sampled signal due to switch capacitor technology enrolled in filter realization. This point would not introduce any puzzle if ADC begins with a high performance Sample-and-hold amplifier (SHA) which could acquire accurate value by sampling.

Finally overall performance including filter, ADC and background processor need to

be verified further. This work has shown that for 802.11a/g standard, a fine designed analog to digital converter with simple back-end digital circuit (expanding ADC) can cooperate with compressing filter well resulting 12dB improvement of dynamic range without losing any Signal-to-Noise-and-Distortion Ratio (SNDR) or Effective Number of Bits (ENOB).

1.4 Outline

This thesis is divided into 7 chapters. Chapter 1 introduces ADC design based on companding background for WLAN application. Chapter 2 describes ADC's fundamentals including sampling theory, spectrum alias effect and static/dynamic specifications. Chapter 3 analyzes the specification derivation from overall receiver budget link which optimizes the whole baseband signal processing performance. The first core part about pipeline ADC architecture is discussed in Chapter 4. 1.5bit residue stage algorithm improves ADC's speed and power consumption efficiently compared to multi-steps converter. Another aspect is to explain how various error sources affect ADC's static and dynamic performance. Chapter 5 circuit implementations for each block are introduced, for example, Operational transconductance amplifier (OTA), comparator, SHA, Multiplying digital-to-analog converter (MDAC), clock generator, back-end digital recover circuit and so on. In Chapter 6 simulation results are given to prove companding system with ADC provides sufficient SNDR through a large dynamic range. Chapter 6 concludes the entire design aspects.

2 ADC fundamental

Analog to digital converter (ADC) is a device that converts real world (analog) signals into digital codes. Conceptually, an ADC works as shown in Fig. 2.1. Analog signals have a continuous range of values on the real number line. An ADC takes a range of the real number line and divides it into smaller subranges. The size of each of the subranges is often referred to as the step size. These steps are usually uniform in size, but not always. A companding ADC for wireless application here is one example of an ADC having non-uniform step sizes. In this case the step sizes follow a adaptive scale.

To each subrange or step a code is assigned. Then, during the conversion process input samples are taken and mapped onto this real number line. The ADC then decides which subrange corresponds to the sample and sends the appropriate digital code to the output. Finally time/amplitude continuous input signal is quantized to time/amplitude discrete output signal.

To perform its task, an ADC always uses at least one comparator. A comparator is a device that compares two quantities and makes a decision based on which of the quantities is larger. The operation of a comparator is illustrated in Fig. 2.2. Generally, input to a comparator can be either analog or digital, but the output is always digital. In analog to digital conversion applications the input to comparator is analog, and the output is a binary digital quantity.

Most essential conceptions would be introduced in this chapter, i.e. resolution, anti-alias, INL/DNL, SNDR/ENOB and so on. All there parameters are used to describe and define ADC's performance which should be clarified at the beginning of design.

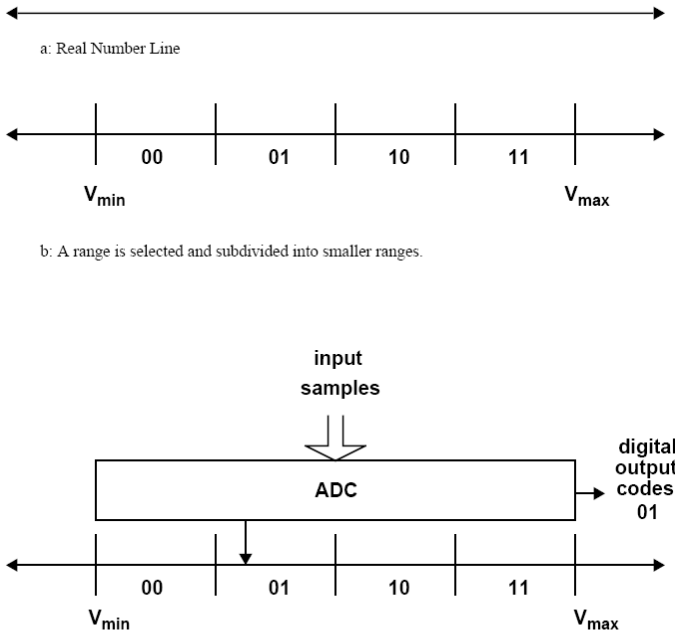


Figure 2.1: Description of an ADC

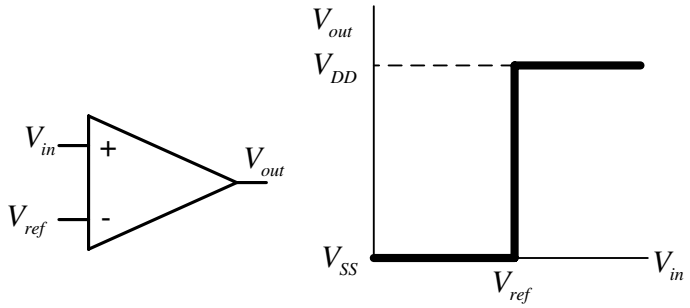


Figure 2.2: Comparator circuit and transfer function

2.1 General features

2.1.1 Resolution

Resolution is the number of output bits that an ADC uses to represent its analog input [5]. The resolution, together with the reference voltage determines the minimum detectable voltage (for an ADC). This is also known as the quantization step Δ or Lest

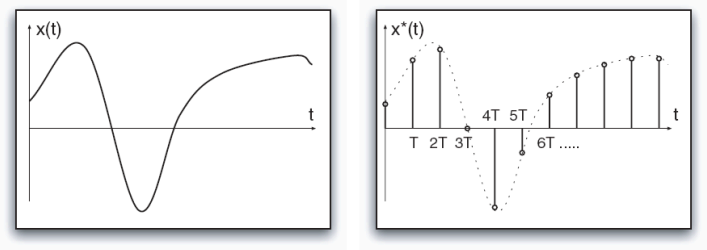


Figure 2.3: Continuous time signal (left) and its sampled data representation (right) [5]

Significant Bit (LSB) as shown in Eq2.1 considering an N bits ADC

$$\Delta = \frac{A_{FS}}{2^N} \tag{2.1}$$

2.1.2 Sampling theory and anti-alias

A sampler transforms a continuous-time signal into its sampled-data equivalently. Ideally, a sampler yields a sequence of delta functions whose amplitude equals the signal at the sampling times. For uniform sampling with period T the output of a sampler is given by Eq2.2

$$x^*(t) = x^*(nT) = \sum x(t)\,\delta(t - nT) \tag{2.2}$$

Fig. 2.3 shows the waveform of a continuous-time signal and the resulting sampled-data signal. The sampled data is made, as stated by eq2.2, by the superposition of weighted deltas. However, a practical circuit does not generate deltas but pulses with finite duration and amplitudes equal to the input at the sampling instances. Regardless of the pulse shape and duration, the pulses are intended to represent the input only at the exact sampling times, nT.

From Eq2.2, the Laplace transform result in

$$L[x^*(nT)] = \sum_{-\infty}^{+\infty} X(s - jnw_s) = \sum_{-\infty}^{+\infty} x(nT)\,e^{-nsT} \tag{2.3}$$

which provides two useful expressions for the Laplace transform of the sampled output. The right-hand equation will be used to discuss the relationships between the s-plane

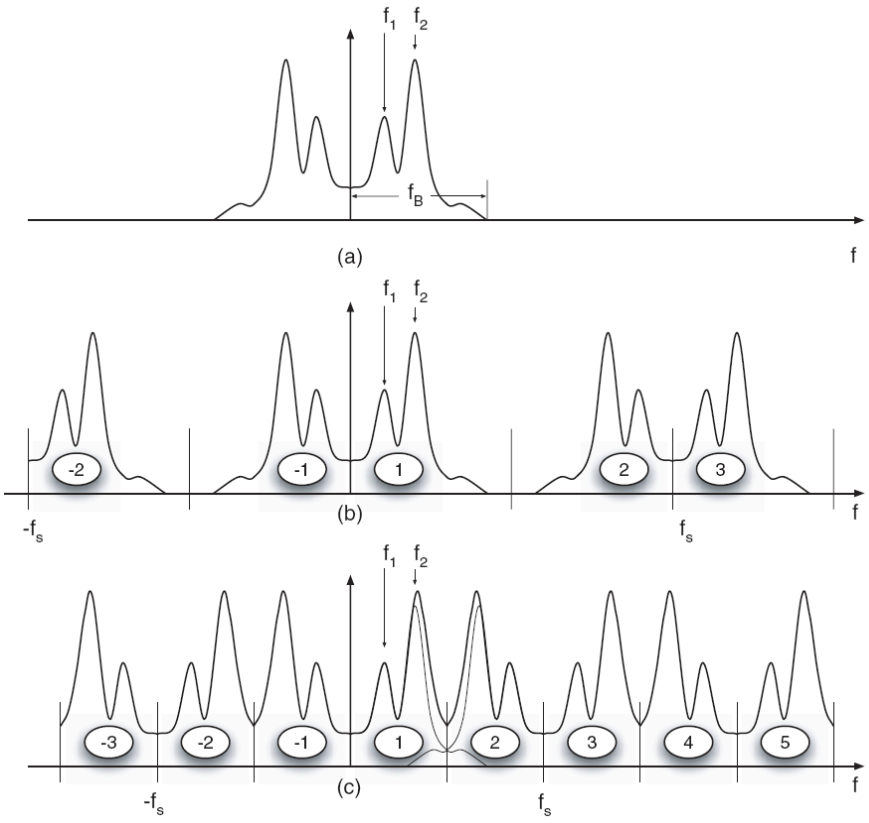


Figure 2.4: Bilateral spectrum of a continuous-time signal. b) Sampled spectrum by using $0.5f_s > f_b$ c) Sampled spectrum with $0.5f_s > f_b$ [5]

and the z-plane. The equation shows that the spectrum of $x^*(nT)$ is the superposition of infinite replicas of the input spectrum [11]. These replicas are centered at multiples of the sampling frequency being shifted along the f axis by $nf_s,\ n = 0,\ \pm f_s,\ \pm 2f_s...$ As a result, the spectrum is periodic with period f_s. Note that the transformation of the input spectrum from band-limited into an infinite replica reveals the non-linear nature of sampling.

Assume that the bilateral spectrum of the input signal is the one of Fig. 2.4 (a) showing two peaks at f_1 and f_2 and vanishing at frequencies higher than f_b . Fig. 2.4 (b) shows a possible sampled spectrum. Here, the sampling frequency is bigger than two times f_b . Consequently, replicas of the spectrum do not interfere with each other [5]. This situation is beneficial: the sampled spectrum within the original signal bandwidth exactly equals Fig. 2.4 (a), thus making it feasible to return back to the continuous-

time signal by filtering. Fig. 2.4(c) shows what happens when the sampling frequency is less than twice the input bandwidth. The replicas partially overlap and modify the spectrum. Furthermore, the peak at f_2 has been shifted and its amplitude increased. Therefore, the spectrum alteration makes it impossible to preserve the continuous-time features.

The above discussion reminds us what is stated by the sampling theory:
A band limited signal, x(t), whose Fourier spectrum, $X(jw)$, vanishes for angular frequencies $|w| > w_s/2$ is fully described by a uniform sampling x(nT), where $T = 2\pi/w_s$.

Half of the sampling frequency, $0.5f_s$, is often named Nyquist frequency. Frequency intervals, $(0.5f_s...f_s)$, $(f_s...1.5f_s)$ are named second and third Nyquist zones, and so forth. Since the spectrum in all Nyquist zones is the same, it is sufficient to focus only on the first nyquist zone $(0...0.5f_s)$. When bilateral spectra are considered the frequency range of interest becomes $(-0.5f_s...0.5f_s)$.

It was previously mentioned that if the sampling frequency is at least twice the bandwidth of the input then the replicas do not overlap. However, this condition must be verified not only for the signal, but also for noise and interferences. Noise has an unpredictable spectrum and can have components at any frequency. The same is true for interferences. Therefore, it is necessary to remove out of band interferences whose folding would corrupt the signal band. A filter placed in front of the sampler achieves this result. The frequency response of the filter must pass the signal band and reject the out-of-band interferences. This kind of filter, whose features are discussed shortly, is named anti-aliasing filter.

In order to preserve signal the anti-alias response must be flat from 0 to f_b . Beyond this, it must reject critical spur/interferes with the required anti-aliasing attenuation. Fig. 2.5(a) shows how the second nyquist zone $(0.5f_s...f_s)$ fold back into the first zone. Based on sampling theory only error band $(f_s - f_b...f_s)$ in second zone would be folded into the signal band $(0...f_b)$ meanwhile band $(0.5f_s...f_s - f_b)$ would not affect signal. Fig. 2.5(b) shows a typical mask of anti-aliasing filter. The transition band is $(f_b...f_s - f_b)$, within which the filter response must roll down such that the attenuation

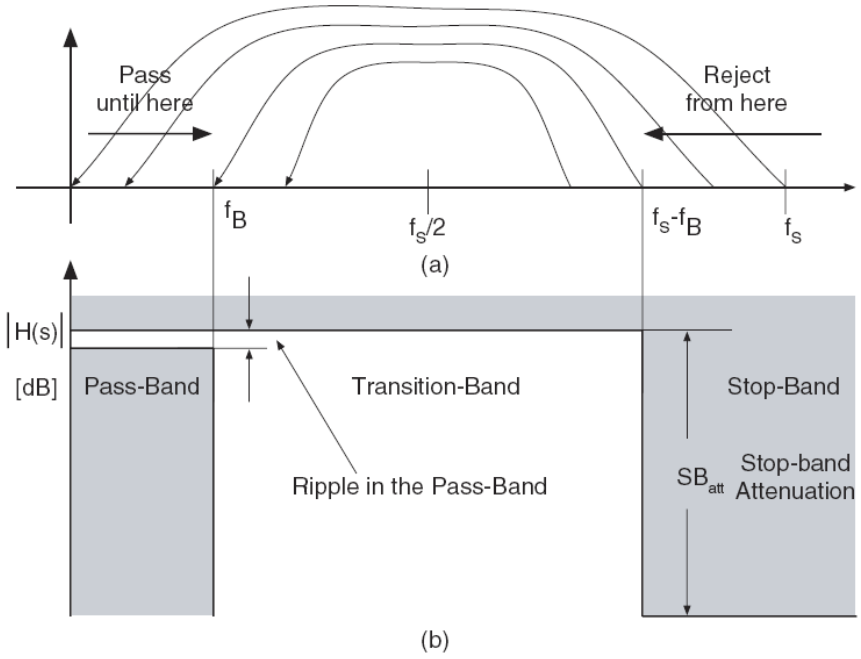


Figure 2.5: Alias effect (a), and anti-aliasing filter mask (b)

at the stop band limit becomes the required A_{SB}.

The width of the transition-band and the required attenuation in the stop-band determine the order of the anti-aliasing filter. It is known that a pole yields a 20dB per decade roll-off. So the filter's order can be illustrated as eq2.4

$$N_{order} = \frac{A_{SB}}{20 \lg \frac{f_s - f_b}{f_b}} \tag{2.4}$$

If $f_s = 3f_b$, an attenuation of 48dB requires an 8th order Butterworth filter, assuming that a flat response is necessary in the pass-band. However, if $f_s = 11f_b$ then an attenuation of 60dB only requires a 3rd order filter. Therefore, large transition regions greatly simply the anti-aliasing filter's design. However, high sampling frequency that widen the transition region require fast circuit for sampling and other analog or digital signal processing [11].

Here conception of oversampling can be included to describe such kind of charac-

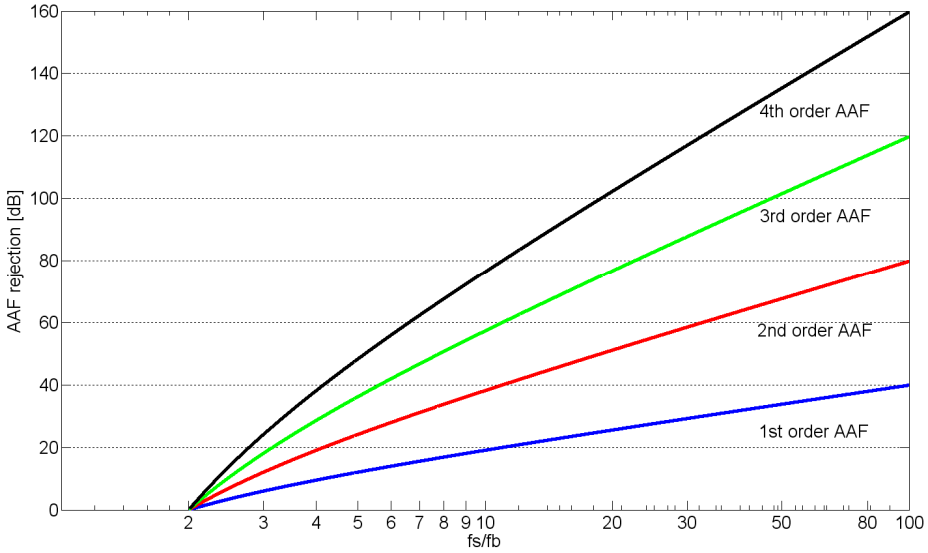


Figure 2.6: OSR relax AAF's order

teristics

$$OSR = \frac{0.5 f_s}{f_b} \tag{2.5}$$

It is clear that AAF's order would be relaxed by large oversampling rate, as shown in Fig. 2.6. Finally an Nyquist ADC should operates with sampling rate no less than double signal bandwidth. The maximum conversion rate equals $N \times f_s$ Mbps.

2.2 ADC with quantization noise

The input-output transfer characteristic depicts the static behavior of a data converter. For an ideal case the input-output characteristic is a staircase with uniform steps over the entire dynamic range [12].

2.2.1 ADC's Transfer function

Fig. 2.7 and 2.8 plot a unipolar/bipolar quantizer's transfer function. Quantization model can be modeled containing sampling, quantization and encoding in Fig. 2.9 and illustrated as follows:

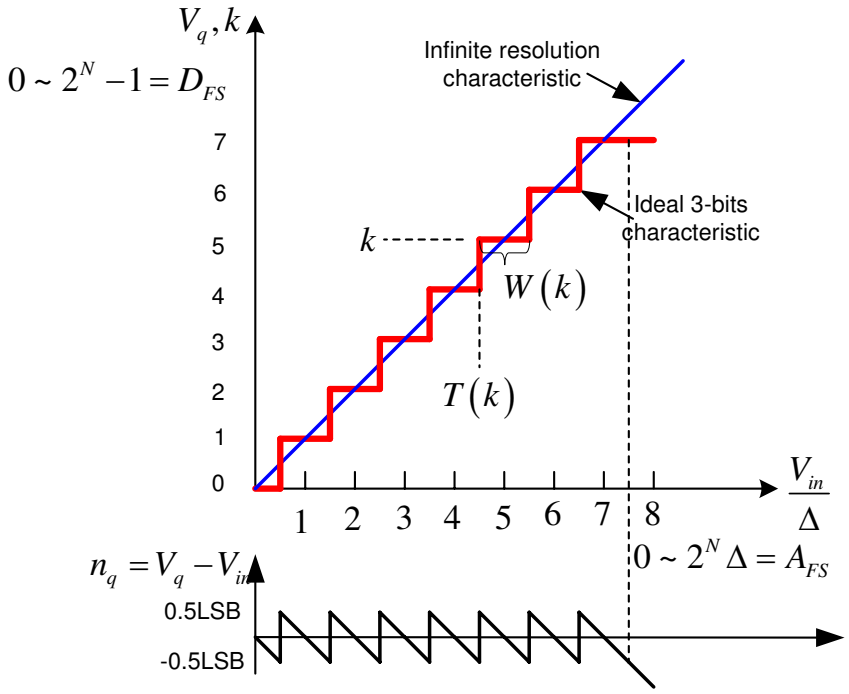


Figure 2.7: Unipolar quantizer transfer function

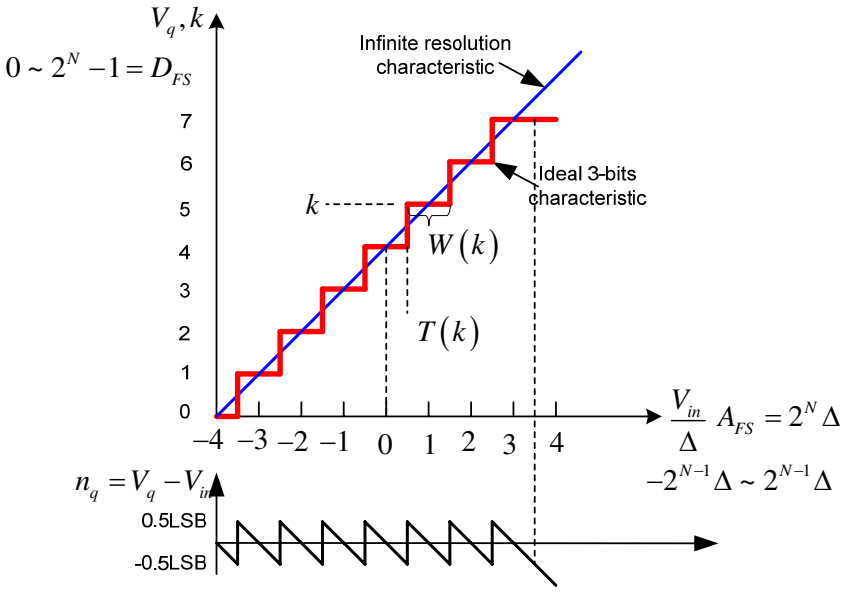


Figure 2.8: Bipolar quantizer transfer function

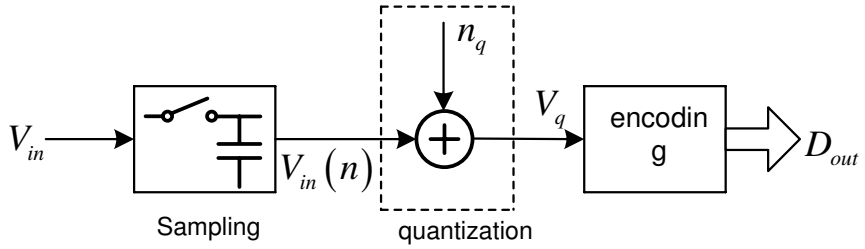


Figure 2.9: Conceptual mode of ADC

First ideal Sampling obtains sampled analog value at sampling instant. In second step quantization based on different residue value results from step one.

Unipolar:

$$\begin{aligned} V_q &= \left\lceil \frac{V_{in}}{\Delta} \right\rceil \quad \text{if residue} > 0.5 \\ V_q &= \left\lfloor \frac{V_{in}}{\Delta} \right\rfloor \quad \text{if residue} > 0.5 \end{aligned} \tag{2.6}$$

Bipolar:

$$\begin{aligned} V_q &= \left\lceil \frac{V_{in}}{\Delta} \right\rceil + 2^{N-1} \quad \text{if residue} > 0.5, \text{ or } 0 > \text{residue} > -0.5 \\ V_q &= \left\lfloor \frac{V_{in}}{\Delta} \right\rfloor + 2^{N-1} \quad \text{if } 0 < \text{residue} < 0.5, \text{ or residue} < -0.5 \end{aligned} \tag{2.7}$$

where $\lfloor\rfloor$ $\lceil\rceil$ means achieve the closest integral value at lower side and higher side. Finally encoding the quantized value to digital domain. Where quantization step is defined as minimum detectable/resolvable voltage, ideal step width as shown in Eq2.8

$$\Delta = \frac{A_{FS}}{2^N} \tag{2.8}$$

And transition (decision) level/point: $T(k)$ is position where output value k-1 turn to k. Midpoint is code center of k. Code width is defined as $W(k) = T(k+1) - T(k)$ note that the code width of the first and last code (000 and 111 on previous slide) is undefined. Finally it should be mentioned that quantization noise is included into ADC at second step by quantizer.

2.2.2 Quantization noise

The quantization error is an unavoidable fundamental limit of the quantization process: it becomes zero only when the number of bits goes to infinity, which is unfeasible in practice. Quantization noise can be modeled as

$$n_q = V_q - V_{in} \tag{2.9}$$

Where V_q is quantized voltage output which can be seen as output from an ideal DAC after ADC. Fig. 2.7, 2.8 and 2.9 depicts the quantization process: the quantization error n_q is added to the input to obtain the quantized output. The addition is a linear operation but the added term is a nonlinear function of the input while quantization noise ranges from $-\Delta/2$ to $\Delta/2$. If instead of the midpoint, one of two edges represents the quantization interval, then diagram would shift up or down by $\Delta/2$. The maximum variation of n_q is still Δ but it ranges from 0 to Δ or from 0 to $-\Delta$.

A large quantization error leads to a reduced capability to preserve the signal features. As is known to all the effect of noise is qualified by SNR defined by Eq2.10:

$$SNR = \frac{P_{sig}}{P_n} \tag{2.10}$$

Where P_{sig} and P_n are the power of the signal and power of noise in the band interest. In general way to investigate noise, power spectra density should be known. Considering quantization noise PDF, following conditions should be specified:
1) all the quantization levels are exercised with equal probability;
2) a large number of quantization levels are used;
3) the quantization steps are uniform;
4) the quantization error is not correlated with the input.

A large input signal fulfils the first requirement. The second condition holds if the quantizer uses a large number of bits, that is true in many cases except for sigma-delta modulator. Most quantizers comply with the third requirement. Only a few data converter use a non-linear response (like the logarithmic response used in telephony for coding audio signals). Even the last rule is normally verified. However, if the data

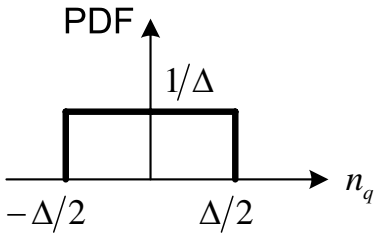


Figure 2.10: PDF of Quantization noise

converter input is a sine wave, as is normally used for testing, an improper choice of frequency can be problematic: when the ratio between the sampling frequency and the input sine wave frequency is a rational number the quantization noise becomes correlated with the input. Based on above conditions, probability distribution function (PSD) of quantization noise is shown in Fig 2.10.

Then mean value and average power can be calculated in Eq2.11 [11]

$$\overline{n_q} = \int_{-0.5\Delta}^{0.5\Delta} n_q \frac{1}{\Delta} dn_q = 0 \tag{2.11a}$$

$$\overline{n_q^2} = \int_{-0.5\Delta}^{0.5\Delta} n_q^2 \frac{1}{\Delta} dn_q = \frac{\Delta^2}{12} \tag{2.11b}$$

The use of Eq2.11 and average power of signal permit to figure out SNR. The power of a sine wave with maximum amplitude is

$$P_{in} = \left(\frac{V_{FS}}{2\sqrt{2}}\right)^2 = \left(\frac{2^N \Delta}{2\sqrt{2}}\right)^2 \tag{2.12}$$

Therefore, eq2.11 and 2.12 leads to [11]

$$SNQR = 6.02N + 1.72\ dB \tag{2.13}$$

Eq2.13 establish useful relationships between the maximum achievable SNR and the number of bits of a quantizer. Results show that every bit of resolution improves the SNR by 6.02 dB. Also, the power of the quantization noise diminishes by a factor 4 for every additional bit.

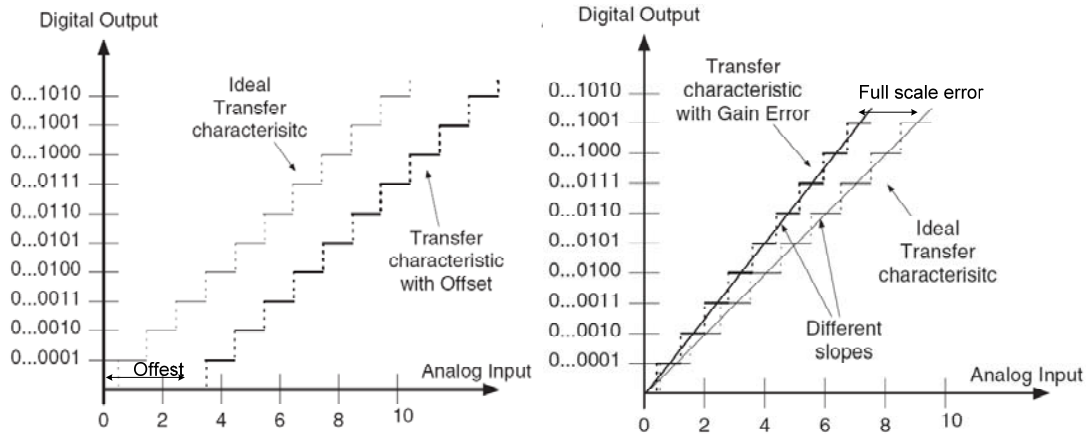


Figure 2.11: Offset and full scale error for analog to digital converter

2.3 Static specification

Deviation from the ideal transfer function produces static error which is described by static specifications such as offset, gain error, DNL (differential nonlinearity), INL (integration nonlinearity) defined below.

2.3.1 Offset, full scale error and gain error

The offset describes a shift for zero input which changes the transfer function so that all the quantization steps are shifted by offset shown in Fig. 2.11[13] left.

Gain error is the error on the slope of the straight line interpolating the transfer curve shown in Fig. 2.11 right. Normally ideal slope is one due to the fact that ideal input range equals output range with out any offset.

Conceptually simple, but lots of subtleties in how exactly these errors should be defined to analyze offset and gain error, for example, endpoint and midpoint specification[13].

1) Bottom endpoint or offset midpoint locates at 0.5before first transition point.

2) Top endpoint or gain midpoint locates at 0.5after last transition point.

Offset is the deviation of bottom endpoint from its ideal location which equals the deviation of first transition from its ideal location. Full scale error is the deviation of

top endpoint from its ideal location with offset removed which equals the deviation of last transition from its ideal location.

LSB or new step width after correcting for offset and full scale error is

$$W_{avg} = \frac{T\left(2^N - 1\right) - T\left(1\right)}{2^N - 2} \tag{2.14}$$

If N is large, then $W_{avg} \approx \Delta$. And new gain or slop of ADC is

$$Gain = \frac{2^N \Delta}{2^N W_{avg}} = \frac{\Delta}{W_{avg}} \tag{2.15}$$

Generally, it is non-trivial to build a converter with very good gain/offset spec. For instance, significant gain and/or offset errors in IF sampling can cause signal clipping and thereby degrade SNR and SFDR. In application requiring matched converters, such as interleaving, simultaneous sampling, and I/Q signal processing, the relative gain and offset matching between individual ADC is critical. Nevertheless, since gain and offset error affect all codes uniformly, these errors tends to be easy to correct using a digital pre- or post-processing operation or by trimming.

2.3.2 DNL: differential nonlinearity

In an ideal world, all ADC codes would have equal width which would be changed in practical way as shown in Fig. 2.12. DNL(k) is a vector that quantifies for each code k the deviation of this width from the "average" width (step size). DNL(k) is a measure of uniformity, it does not depend on gain and offset errors. Scaling and shifting a transfer characteristic does not alter its uniformity and hence DNL(k)[11].
Definition of average code width without offset and full scale error:

$$W_{avg} = \frac{T\left(2^N - 1\right) - T\left(1\right)}{2^N - 2} \approx \frac{V_{FS}}{2^N} = \Delta \tag{2.16}$$

So the DNL(k) equals

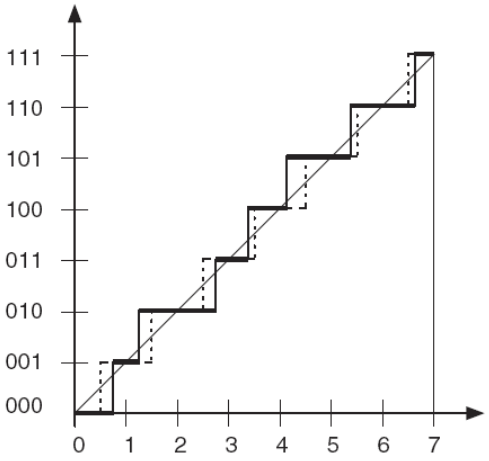


Figure 2.12: Transfer function of ADC with DNL

$$DNL\,(k) = \frac{W\,(k) - W_{avg}}{W_{avg}} = \frac{W\,(k)}{W_{avg}} - 1[LSB] \tag{2.17}$$

DNL has some special characteristics as follows:

1)Positive/negative DNL implies wide/narrow code, respectively,

2)DNL = -1 LSB implies missing code,

3)Impossible to have DNL < -1 LSB for an ADC. But possible to have DNL > +1 LSB,

4)If DNL>1LSB, then there is possibility of non-monotonic,

5)Can show that sum over all DNL(k) is equal to zero.

2.3.3 INL: Integrated nonlinearity

INL shown in Fig. 2.13 sometimes called relative accuracy, is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset[14].

INL for bin k is defined as Eq2.18

$$INL\,(k) = \frac{T\,(k) - T_{uniform}\,(k)}{W_{avg}},\ 1 \le k \le 2^N - 1 \tag{2.18}$$

Due to definition of $T_{uniform}\,(k)$, we can find that $INL\,(1) = INL\left(2^N - 1\right) = 0$

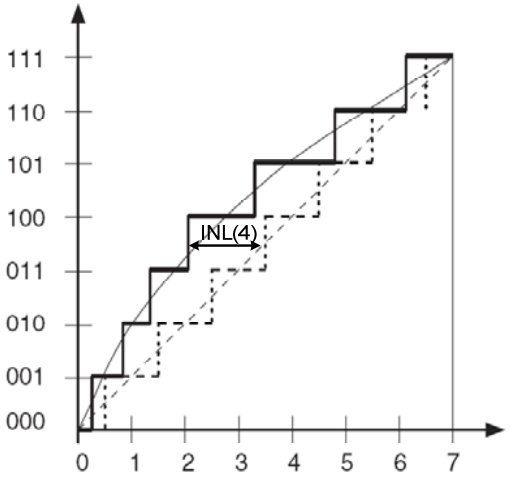


Figure 2.13: Transfer function of ADC with INL

and INL(0) is not defined. There is a direct connection (Eq2.19) between INL and DNL. The INL for output k can be obtained by integrating the DNL until code k-1

$$INL\,(k) = \sum_{i=1}^{k-1} DNL\,(i) \tag{2.19}$$

Means that once we compute DNL, we can easily find INL using a cumulative sum operation on DNL vector.

2.3.4 Example

Here is an example of DNL shown in Fig. 2.14. The first transition level at 2V and the last transition level at 7.5V. Total effective number of steps equals 6 excluding first and last step. So new average step width is $W_{avg} = (7.5 - 2)/6 = 0.9167V$. Assume ideal first transition at 0.5, last transition at 6.5. Offset can be calculated as $offset = (2 - 0.5)/\Delta = 1.5LSB$. Full scale error is $FS\ error = (7.5 - 6.5)/\Delta = 1LSB$. New gain is W_{avg}/Δ =0.9167.

Finally DNL is $+0.64/-1LSB$, INL is $+0.37/-0.64LSB$ and missing code exists. Whole calculation process is shown in Table2.1.

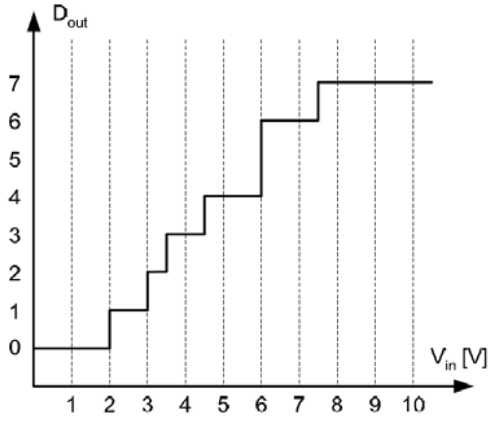


Figure 2.14: Transfer function of example to show DNL

Table 2.1: Calculation of DNL and INL

Code [k]	W [V]	DNL [LSB]	INL [LSB]
0	undefined	-	-
1	1	0.0909	0
2	0.5	-0.4546	0.0909
3	1	0.0909	-0.3637
4	1.5	0.6363	-0.2728
5	0	-1	0.3634
6	1.5	0.6363	-0.6365
7	undefined	-	0

2.4 Dynamic specification

2.4.1 SNDR and ENOB

Total error power includes all bins except DC, signal, ant 2nd through 7th harmonic. Both quantization noise and electronic noise affects SNR which can be defined as

Eq2.20[11]

$$\begin{aligned} SNR &= \frac{P_{sig}}{P_{n,avg}} = \frac{V_{sig}^2\,(rms)}{\overline{v_n^2}} \\ &= \frac{V_{sig}^2\,(rms)}{\overline{v_{nq}^2} + \overline{v_{n,cir}^2} + \overline{v_{n,a}^2} + \overline{v_{n,har}^2}} \\ &= \frac{V_{sig}^2\,(rms)}{\overline{v_{nq}^2} + \overline{v_{n,cir}^2} + \overline{v_{n,a}^2} + \sum_{i=2}^{7} V_i^2\,(rms)} \end{aligned} \tag{2.20}$$

Where $\overline{v_{nq}^2}$, $\overline{v_{n,cir}^2}$, $\overline{v_{n,j}^2}$, $\overline{v_{n,har}^2}$ are quantization noise, circuit noise especially for thermal noise, aperture error and harmonic components power respectively. If we define all the error source together and model them quantization noise, effective number of bits, called ENOB, can be defined as Eq2.21

$$ENOB = \frac{SNDR - 1.72dB}{6.02dB} \tag{2.21}$$

To get ideal ENOB only for zero circuit noise, perfect clock and transfer function with zero INL and zero DNL. It should be mentioned that low circuit thermal noise is costly: cutting thermal noise by $2\times$ can cost $4\times$ in power dissipation.

2.4.2 DR: dynamic range

In general way, dynamic range of ADC is related to SNR. This parameter is used to define input signal power range where output signal power not decreased as input power increasing as shown in Fig. 2.15. Due to the fact that ideal ADC's transfer function can be modeled as one[14], therefore, in principle maximum input signal power equals peak output power for a linear system as illustrated in Eq2.22.

$$DR \approx \frac{P_{sig,\max}}{P_n} \tag{2.22}$$

2.4.3 SFDR,THD,IMD3

Considering linearity, it is normally assumed that harmonic terms higher than the seventh have negligible effects. If f_{in} is the frequency of the input signal and f_s is the

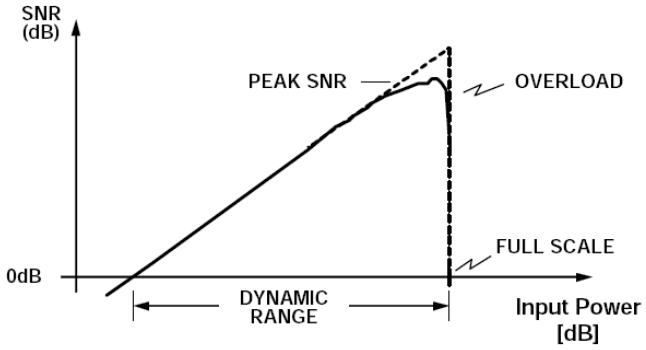


Figure 2.15: Dynamic range of ADC as a linear system

sampling frequency, then the n-th harmonic component is at $|Nf_s \pm nf_{in}|$, where N is a suitable number that folds the harmonic term into the first Nyquist zone.

SFDR is the ratio of signal amplitude to the amplitude of the highest spurious spectral component in the first Nyquist zone as shown in Eq2.23.

$$SFDR = \frac{P_{sig}}{P_{spur,\max}} \tag{2.23}$$

The SFDR is important for communication systems. Often it is necessary to perform analog-to-digital conversion on a small signal representing a channel that the antenna receives together with other big channels. It may happen that a high spur/interfere generated by a big channel falls very close to the small channel thus masking the associated information. Fig. 2.16 illustrates the problem. The input signal has two channels, a big one 0dB at around 6.72MHz, and a smaller one (-90dB) at around 3.8MHz. Sampling frequency is 16.4MHz. The bigger spur/interfere generates a big third order harmonic at 20.16MHz which gets folded back to 3.76MHz, just 40kHz from small channel. Even if the SFDR is 85dB the spur/interfere almost completely masks the -90dB signal.

The SFDR provides information similar to the THD but focus on the worst tone. THD is total harmonic distortion including no more than 7th harmonic which is defined

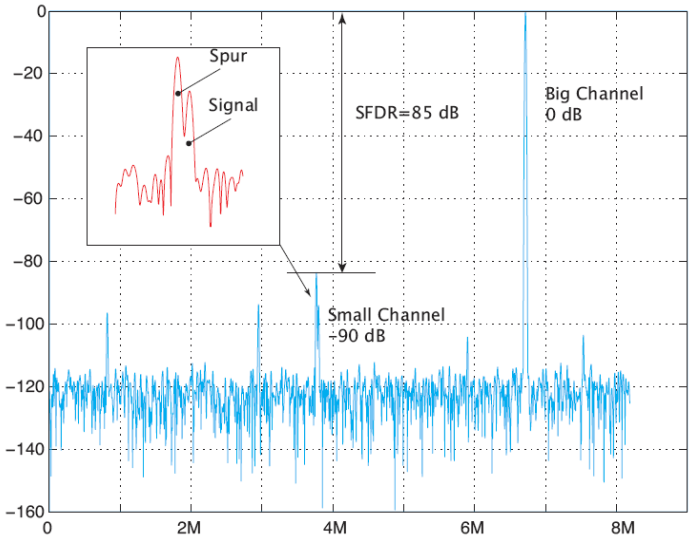


Figure 2.16: Spectrum of a small channel corrupted by a spur/interfere from bigger channel harmonic [5]

as:

$$THD = \frac{\sum_{i=2}^{7} V_i^2\,(rms)}{V_{sig}^2\,(rms)} \tag{2.24}$$

Non-linearity not only causes distortion of a pure tone; but also, when the input is made of multiple sine waves the interaction between them produces inter-modulation distortion (IMD) terms. IMD is important in multi-channel communication system. The third order products are generally difficult to filter out which should be attenuated sufficiently.

Two tone test shown in Fig. 2.17 is made by two closely spaced tones f_1 and f_2 . The third order harmonic occur at $(2f_1 - f_2)$ and $(2f_2 - f_1)$. These two frequencies are closed to input frequency. Other inter-modulation terms are set far away from input and can be filtered out in digital domain. Finally IMD3 is defined as

$$IMD3 = \frac{V_{sig}^2\,(rms)}{V_{IM3}^2} \tag{2.25}$$

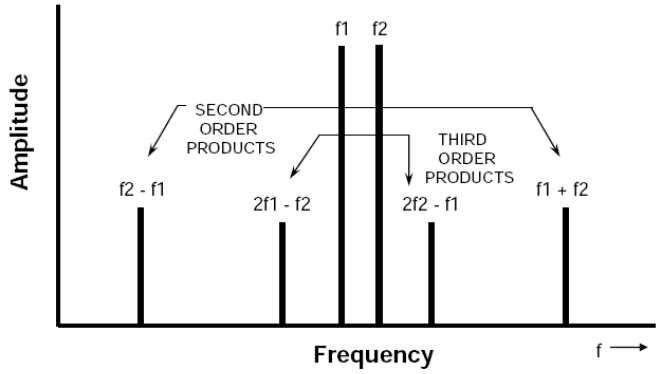


Figure 2.17: Inter-modulation distortion spectrum at two tone input sine wave

2.4.4 FOM: Figure of Merit

Figure of merit is a parameter used to measure the power effectiveness of an ADC[15]. It assumes that the total power is consumed mainly because of the bandwidth of the converted signal (BW) and the equivalent number of bits (ENOB). Publications or data-sheets use different definitions of the FOM. The basis of all these definitions is

$$FOM = \frac{P\,(pW)}{2^{ENOB} \times f_s} \quad [pJ/step] \tag{2.26}$$

Obviously smaller FOM means higher performance. Today's ADC record is obtained with FOM 4.4fJ/step by Twente University and Philips research published in ISSCC 2008.

4 Pipeline ADC architecture

4.1 Introduction

In a pipeline analog-to-digital converter, quantization is distributed along a pipelined signal chain resulting in an effective architecture for high-resolution high-speed ADCs. By pipelining the signal, a high throughput can be achieved costing a latency time that is linearly dependent on the number of stages. A general block diagram of a pipeline ADC is shown in Fig. 4.1[22]. It consists of 9 low resolution stages, digital correction logics including delay elements synchronizing the stages output codes. Each stage has a resolution of 1+1bits, of which first one represents the effective stage resolution and next one becomes redundancy for comparator offset compensation algorithm except for last stage. The block diagram of pipeline stage with its transfer function is also shown in Fig. 4.1. Each stage comprises a low resolution sub ADC in flash style and an arithmetic unit called multiplying digital to analog converter (MDAC) that performs as a combination of sample and hold operation, DAC, subtraction and amplification.

In this chapter, the pipeline ADC architecture is analyzed and the principle of digital correction is also presented. The error sources of a switched capacitor (SC) pipeline stage and their effects on the ADC performance are given from system level view.

4.2 Pipeline ADC algorithm

All analog to digital converter can be modeled as a ideal quantizer which includes exclusive non-ideality: quantization noise. Assuming ideal DAC, pipeline ADC's stage can be modeled as Fig. 4.2. Here sub ADC includes its own quantization noise. There are two output signal: 1) quantization output 2) residue output due to subtraction operation in Eq4.1

$$V_{out} = V_{in} + n_q \tag{4.1a}$$

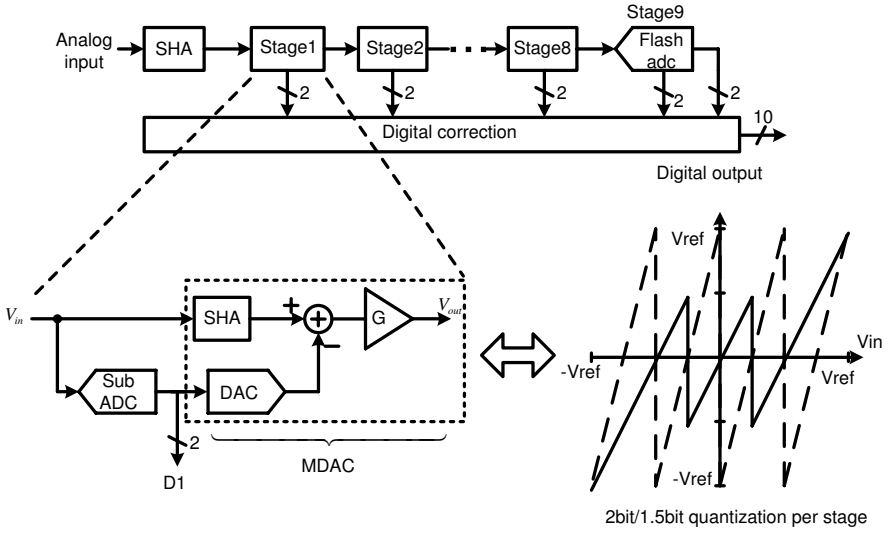


Figure 4.1: Block diagram of a 10-bit pipeline ADC

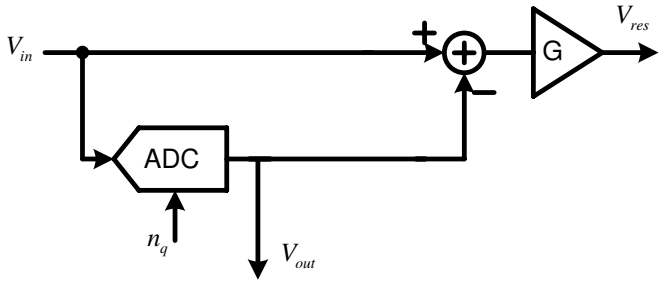


Figure 4.2: pipeline ADC stage model with ideal DAC

$$V_{res} = -Gn_q \tag{4.1b}$$

Where V_{out} represents output of an ideal DAC following sub-ADC. Residue of pipeline ADC stage is equal to minus stage gain times sub-ADC's quantization noise as shown in Eq4.1b. If a two bit sub-ADC is used here, the quantization noise and residue plot is shown in Fig. 4.3. To model overall ADC algorithm, it is often convenient to look at pipeline as single stage plus backend ADC [11] as shown in Fig. 4.4. From Fig. 4.4, it is easy to illustrate the equations to describe overall ADC's characteristics as

$$V_{out} = V_{in} + \cancel{\left(1 - \frac{G}{G_r}\right) n_{q1}} + \frac{n_{q2}}{G_r} \tag{4.2}$$

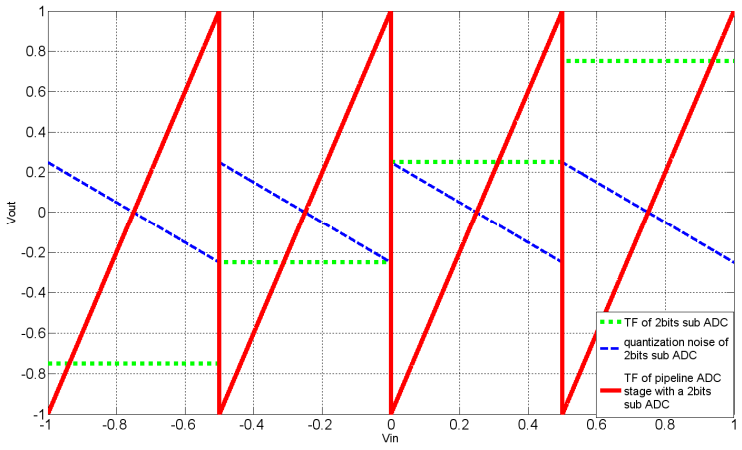


Figure 4.3: TF of pipeline ADC with 2bits sub ADC

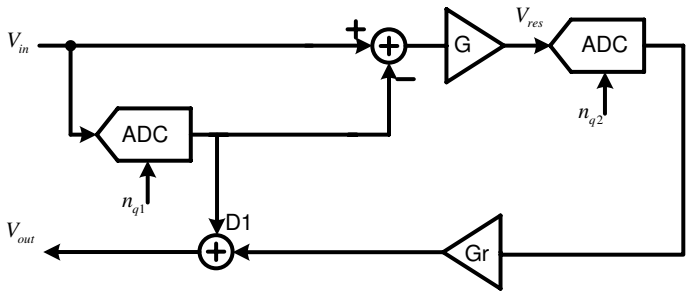


Figure 4.4: ADC model with a single stage and a single backend ADC

Where G is stage gain, G_r is ideal DAC bit weight which is used to recover analog value. It obvious that if stage gain is equal to effective bit weight, final quantization noise of overall ADC is backend ADC's quantization error divided by bit weight. Now let's extend the architecture above to unlimited stages as shown in Fig. 4.5

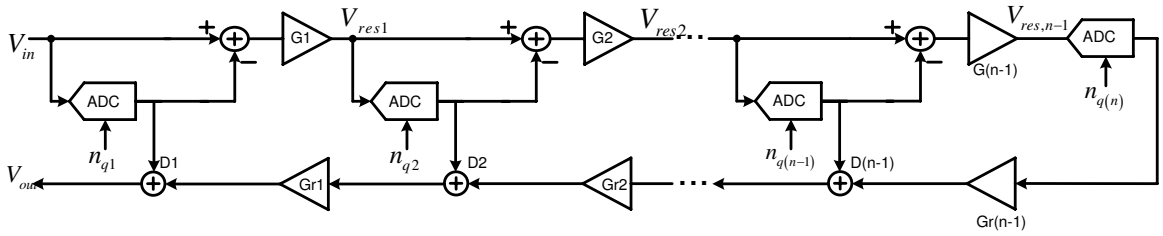


Figure 4.5: Extension of multi stages architecture of pipeline ADC

Using the same approach, output analog value can be calculated as follows

$$V_{out} = V_{in} + \cancel{n_{q1}\left(1 - \frac{G_1}{G_{r1}}\right)} + \cancel{\frac{n_{q2}}{G_{r1}}\left(1 - \frac{G_2}{G_{r2}}\right)} + ... + \cancel{\frac{n_{q(n-1)}}{\prod_{j=1}^{n-2} G_{rj}}\left(1 - \frac{G_{n-1}}{G_{r(n-1)}}\right)} + \frac{n_{q(n)}}{\prod_{j=1}^{n-1} G_{rj}} \tag{4.3}$$

From Eq4.3 there are several important conclusion as follows: 1) first stage has most stringent precision requirements. 2) the algorithm condition is that all the DACs are ideal which means transfer function is equal to one and each stage operates at the same full scale range. Finally with ideal stage gain ($G_i = G_{ri}$), equation is obtained.

$$\begin{aligned} V_{out} &= V_{in} + \frac{n_{q(n)}}{\prod_{j=1}^{n-1} G_{rj}} \\ \Rightarrow N_{adc} &= N_n + \sum_{j=1}^{n-1} \log_2 G_j \end{aligned} \tag{4.4}$$

Where N_{adc} is ADC's quantization resolution, N_n is last stage quantization resolution. For example, there are 4 stage whose gain and stage resolution are 4 and 2 respectively. A 2bits flash ADC as last stage, overall ADC's resolution $N_{adc} = 2 + \sum_{j=1}^{4} 2 = 10$ bit, $n_q = (V_{FS}/2^2)/4^4 = V_{FS}/2^{10}$. The only error in V_{out} is that of the last ADC, divided by aggregation gain. The stage gain is defined by effective resolution of j^{th} stage.

$$G_j = 2^{N_{eff,j}} \tag{4.5}$$

4.3 1.5bit pipeline stage and digital correction

Several techniques to improve the speed and accuracy of the pipeline A/D converter architecture have been developed after the basic concept of cascading of low-resolution stages was introduced. A sophisticated digital correction algorithm with 1 bit of redundancy in each stage is commonly used in the pipeline A/D converters to relax the quantization accuracy specifications in sub-ADCs.

Adding a redundant bit means increasing the stage resolution by one bit meanwhile reducing a comparison level based on added architecture. Considering a pipeline stage

with N bits effective resolution, adding one bit redundancy means now output resolution is N+1 bits and there are $2^{N+1}-2$ comparison levels. To clarify stage with redundancy, some definition is given as follows

$$\begin{aligned} N_{red} &= 1 \\ N_{sub,out} &= N_{eff} + N_{red} \\ N_{comp} &= 2^{N_{sub,out}} - 1 - 1 \\ N_{sub,eq} &= \log_2 (N_{comp} + 1) \end{aligned} \tag{4.6}$$

where N_{red} is redundant bit which is equal to one in common. $N_{sub,out}$ is sub-ADC's output bits. N_{comp} counts number of comparators needed at some redundancy. $N_{sub,eq}$ is equivalent number of bits referred to flash ADC. The offset effect on 2 bits stage is sensitive and can be obtained from Fig. 4.6. Any tiny error in sub ADC decision level from comparator offset which can not be reduced obviously unless cost much power will overload backend ADC and therefore deteriorate ADC's transfer function's linearity. Now 1.5bit stage with one bit redundancy is proposed to compensate offset in Fig. 4.6. Fig. 4.7 shows that with 1.5 bit stage transfer function, $\pm 0.25 V_{ref}$ offset at most can be tolerated without introduce any overload for next stage[23]. Sub ADC's offset is absorbed in the same way as their inherent quantization error. And OTA's offset would also only cause boundary saturation without degradation linearity which would be shown in next section. Meanwhile Fig. 4.8 illustrates that 1.5bit keeps all the information compared to 2bit stage. By shifting right 0.5 LSB on the original transfer function of 2bits stage (dashed line), the region '11' of the initial transfer function can be obtained again by next stage correction. Because next stage is flash ADC, all the regions where 1.5 bit stage output is positive would be corrected by one contrarily by zero resulting in right code compared to 2bit stage without redundancy. Finally a 1.5 + 2bit pipeline with digital correction operates as a 3bit flash.

As a core cell of pipeline ADC, effective resolution of 1.5 bit stage is one and it has 2bit output and two comparators. The transfer function can be described based on

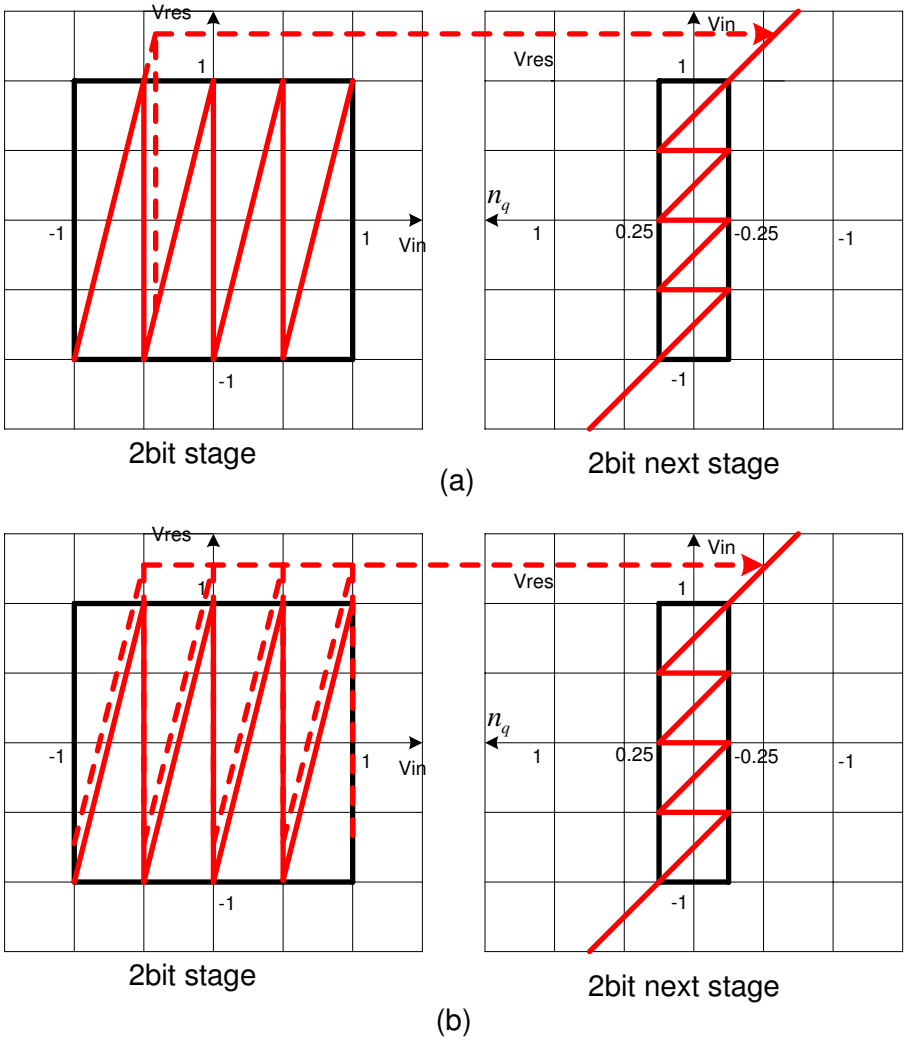


Figure 4.6: 2+2bit residue signal transfer with overload: (a) comparator offset (b) DC offset

Fig. 4.7 which is realized by switch-capacitor circuit.

$$V_{out} = \begin{cases} 2V_{in} + V_{ref}, & if \ -1/4V_{ref} \geq V_{in} \geq -V_{ref} \quad d = 0 \ (00)_2 \\ 2V_{in}, & if \ 1/4V_{ref} \geq V_{in} \geq -1/4V_{ref} \quad d = 1 \ (01)_2 \\ 2V_{in} - V_{ref}, & if \ V_{ref} \geq V_{in} \geq 1/4V_{ref} \quad d = 2 \ (10)_2 \end{cases} \tag{4.7}$$

Reconstruction of 1.5 bit redundancy code is performed by adding up the properly delayed stage outputs with one bit overlap: the MSB of stage i is added to the LSB of the previous stage i-1, as indicated in Fig. 4.9. The output of last stage is not

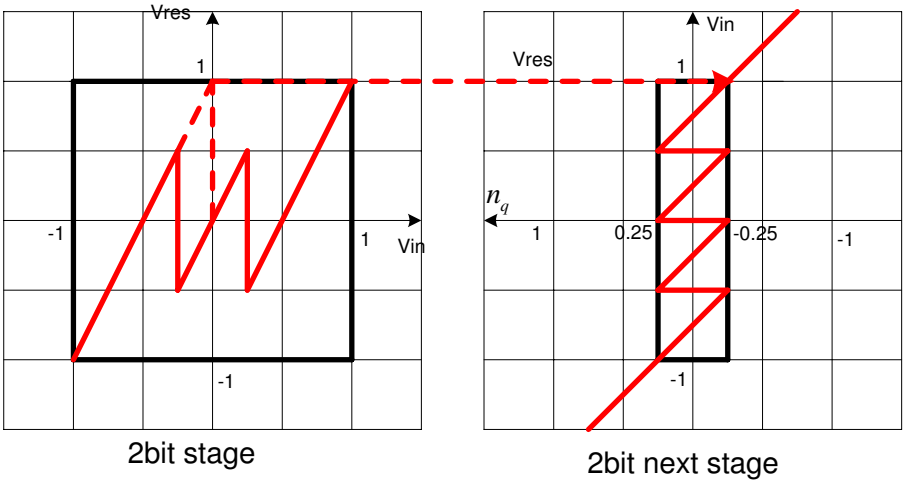


Figure 4.7: 1.5+2bit residue signal transfer with large offset tolerance

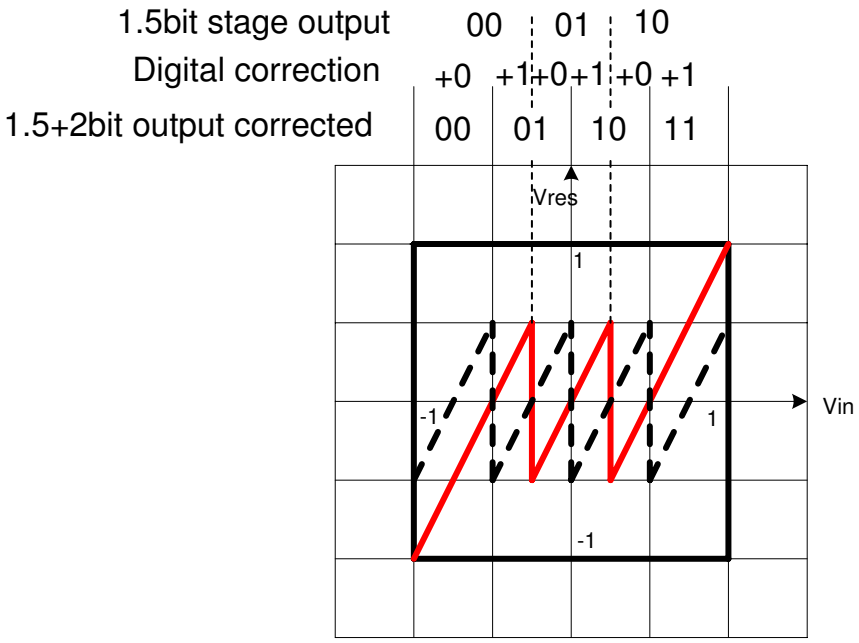


Figure 4.8: 1.5bit transfer function algorithm

corrected which suggests that the last stage must be a full flash without redundancy. The excess in hardware caused by 1.5 bit stage and digital correction is very small. In a pipeline stage, the number of comparators of the sub-ADC is approximately doubled compared to 1 bit stage, but in the MDAC, only a few extra switches are required, while the total capacitance and amplifier specifications remain unchanged. However,

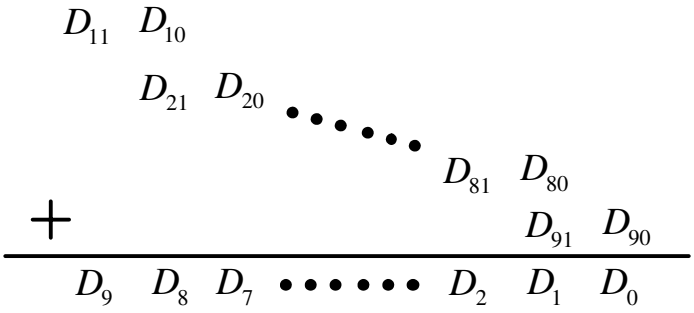


Figure 4.9: Outline scheme for digital correction

as the comparator specifications are simultaneously relaxed significantly, the effects on area and power minimization are positive. For the reconstruction in the digital domain, only a small adder is required.

There are another important reason for 1.5 bit stage is to maximize SC circuit closed loop bandwidth at a fixed power consumption. Since this bandwidth depends on feedback factor resulting from stage gain and stage gain depends on effective stage resolution, choosing lower per-stage resolution allows faster settling behavior. With the resolution of 1.5bit stage, the closed loop gain of only two allows large feedback factor (of about 1/2) resulting in large closed loop bandwidth.

4.4 linearity degradation due to stage error source

4.4.1 Model for switch capacitor stage

The most critical block of pipeline stage is multiplying DAC (MDAC), which performs the DA conversion of sub ADC output, subtraction of the resulting analog signal from SHA input signal and amplification of the residue. Traditionally the core of MDAC is implemented using switch capacitor technology, MDAC being essentially an SC integrator formed around an full differential OTA as shown in Fig. 4.10 showing single end mode analysis. This circuit operates on two phases, a sampling phase and a hold phase. During sampling phase shown in Fig. 4.11a, the input signal is sampled onto both C_s and C_f. During hold phase shown in Fig. 4.11b the capacitors are then switched to one of three voltages, $+V_{ref}$, $-V_{ref}$, and ground.

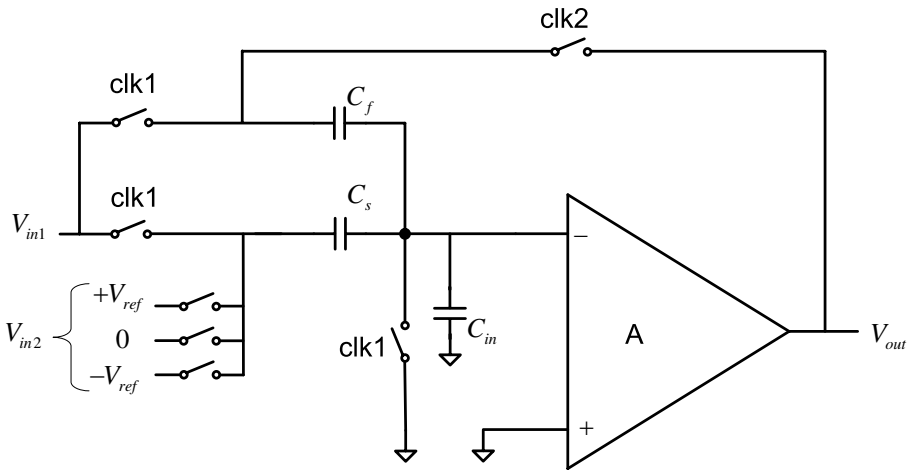


Figure 4.10: Half circuit of switch capacitor stage

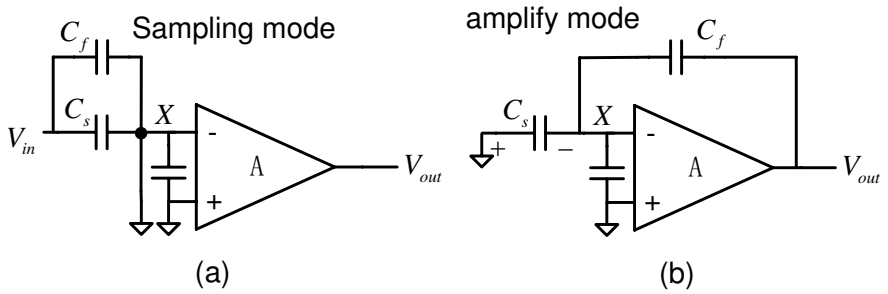


Figure 4.11: Circuit configuration of SC stage in two phases: (a) sampling phase (b) amplify phase

Based on charge redistribution view, static transfer function of stage can be derived as follows:

$$V_{out} \approx \left[V_{in1} - V_{in2}\left(\frac{C_s + C_{in}}{C_s + C_f}\right)\right]\left(1 + \frac{C_s}{C_f}\right)\left(1 - \frac{1}{A\beta}\right) \tag{4.8a}$$

$$\beta = \frac{C_f}{C_s + C_f + C_{in}} \approx \frac{1}{2} \tag{4.8b}$$

Above equation includes, parasitic input capacitor, OTA gain error. β is feedback factor. Settling behavior due to slew rate and GBW can be included also by adding an item $1-\varepsilon_{settle}$ to Eq4.8a. If DC loop gain and settling error are un-correlating, transfer

function can be obtained as

$$V_{out} \approx \left[V_{in1} - V_{in2}\left(\frac{C_s + C_{in}}{C_s + C_f}\right)\right]\left(1 + \frac{C_s}{C_f}\right)(1 - \varepsilon_{gain}) \tag{4.9}$$

If parasitic capacitor C_{in} is ignored and capacitor ratio between C_s and C_f is modeled as $1 + \delta$, then static transfer function can be simplified further as

$$\begin{aligned} V_{out} &= \left[V_{in1} - V_{in2}\left(\frac{1+\delta}{2+\delta}\right)\right](2+\delta)(1-\varepsilon_{gain}) \\ &= \left[V_{in1}(2+\delta) - V_{in2}(1+\delta)\right](1-\varepsilon_{gain}) \end{aligned} \tag{4.10}$$

From Eq4.10, we can model some un-idealities such as mismatch, OTA gain error, OTA linearity, OTA offset, sub ADC offset and DAC reference error using simulink and matlab as tools which are discussed as follows[24][25].

4.4.2 Sub ADC offset

The performance of a low resolution flash ADC as sub-ADC is limited primarily by accuracy of comparators and secondarily by the accuracy of reference. Both of these can be modeled as an offset in the comparator threshold voltage. The largest comparator offset allowed is $\pm 0.25 V_{ref}$ which is in order of hundreds of millivolts if $N_{eff} \leq 3$, even for a low supply voltage design. The effect of threshold level shifting on the transfer function of 1.5 bit stage is presented in Fig. 4.12 Where non-zero comparator offset is assumed to be the only non-ideality. Dashed line shows the ideal transfer function and real line includes a large offset even not being tolerated by digital correction at positive half region and a small offset less than one forth Vref being tolerated contrarily. Fig. 4.13 shows that linearity degradation would be introduced by offset in overall ADC which happens where overloading takes place.

4.4.3 OTA error

The performance of OTA in MDAC is the most critical non-ideality affecting both the static and dynamic linearity of stage, and thus the whole ADC. The amplifier output of MDAC must settle to accuracy of the remaining pipeline ADC within half of a clock

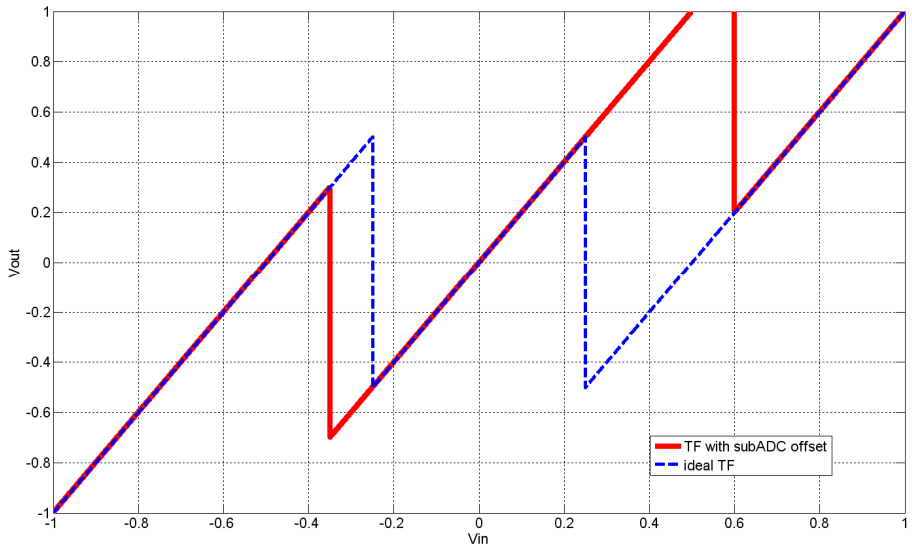


Figure 4.12: 1.5bit stage transfer function with comparator offset

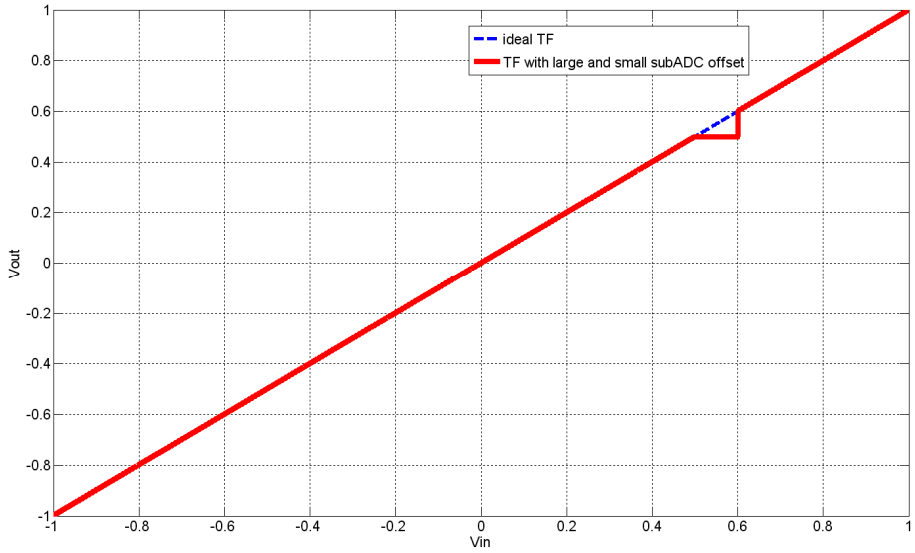


Figure 4.13: ADC transfer function with sub ADC offset

cycle. The essential non-ideality related to OTA is offset, gain error including settling behavior, linearity. Note that in system level view, settling behavior can be modeled as one kind of dynamic OTA gain error.

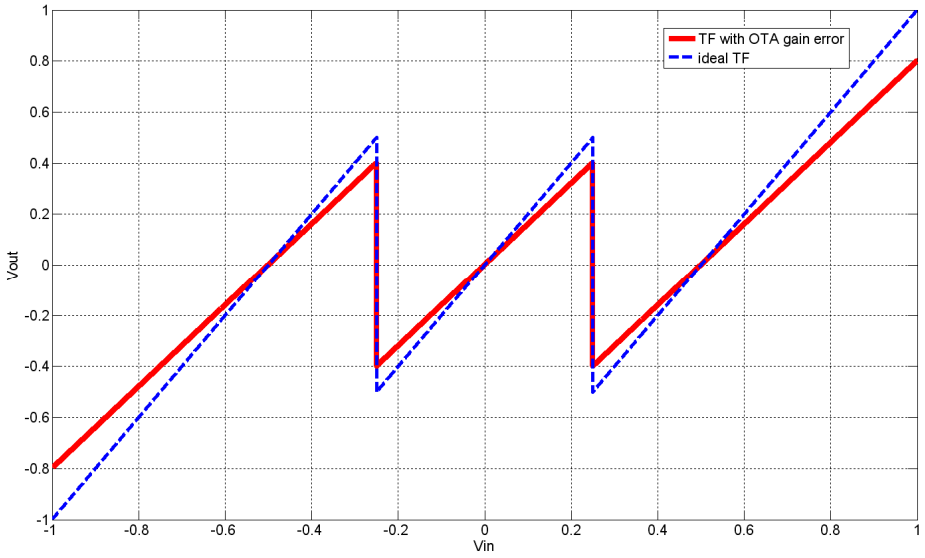


Figure 4.14: 1.5bit stage transfer function with OTA gain error

4.4.3.1 stage gain error including OTA settling

Gain errors result from the static settling (finite open loop DC gain), which is given by $G_m R_{out}$, and from the parasitic capacitor C_{in}, which changes feedback factor of stage also from dynamic settling behavior, which limited by slew rate and GBW. The effect of stage gain error on the transfer function of 1.5 bit stage is presented in Fig. 4.14 Where gain error composed of OTA gain, feedback factor and settling behavior is assumed to be the only non-ideality. Dashed line shows the ideal transfer function and real line includes gain error. Fig. 4.15 shows that what linearity degradation would be introduced by gain error in overall ADC.

4.4.3.2 Stage linearity error from OTA harmonic

OTA is a linear system ideally. But in fact there is other order harmonic component which degrades MDAC's linearity. Since pipeline stage is realized by full differential mode, main odd order harmonic remains especially for 3rd harmonic. The effect of OTA 3rd harmonic on the transfer function of 1.5 bit stage is presented in Fig. 4.16 where 3rd harmonic is assumed to be the only non-ideality. Dashed line shows the ideal transfer function and real line includes harmonic. Fig. 4.17 shows that what linearity

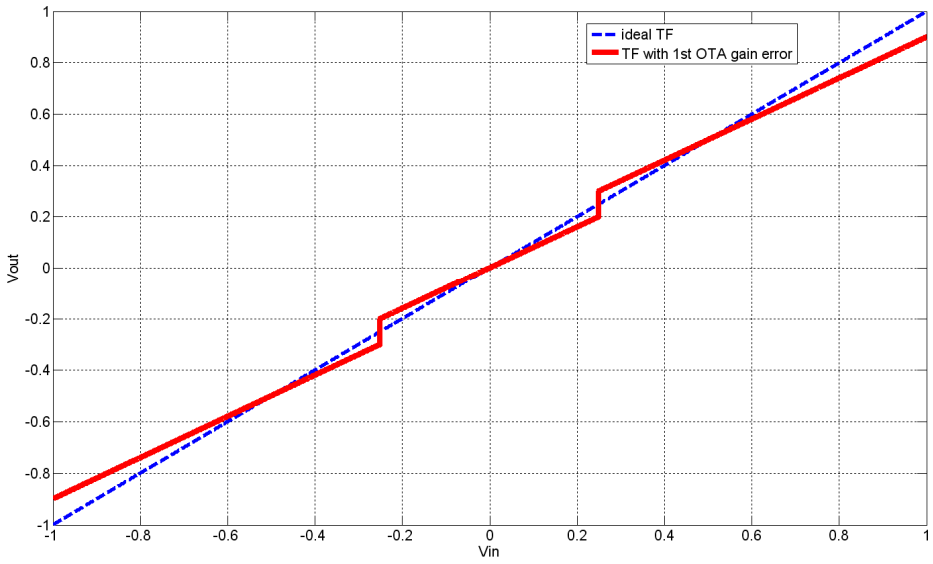


Figure 4.15: ADC transfer function with OTA gain error

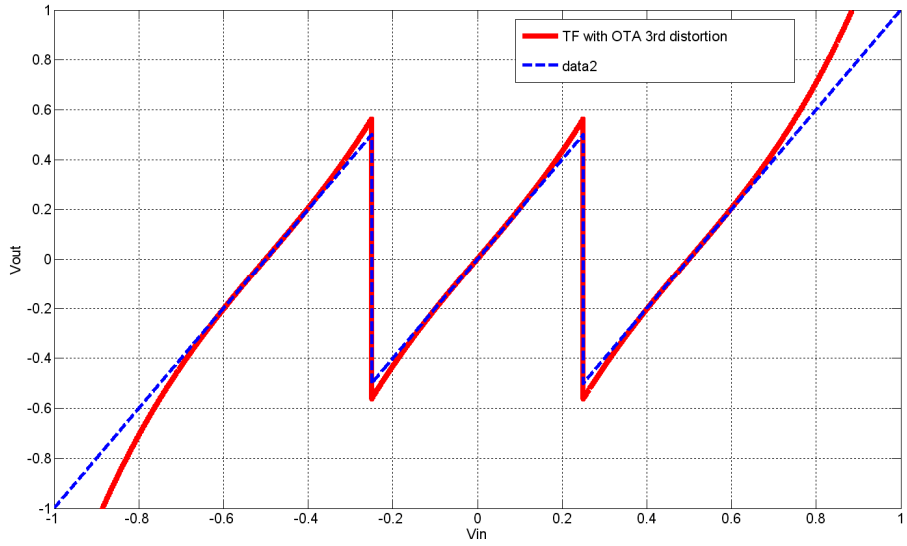


Figure 4.16: 1.5bit stage transfer function with OTA non-linearity

degradation would be introduced by harmonic in overall ADC.

4.4.4 Stage offset from OTA

The effect of the stage offset coming from amplifier offset voltage in MDAC can be obtained using the schematic of Eq4.7, 4.8, 4.9, 4.10. OTA's offset mainly comes from input transistors' mismatching. The effect of stage offset on the transfer function of

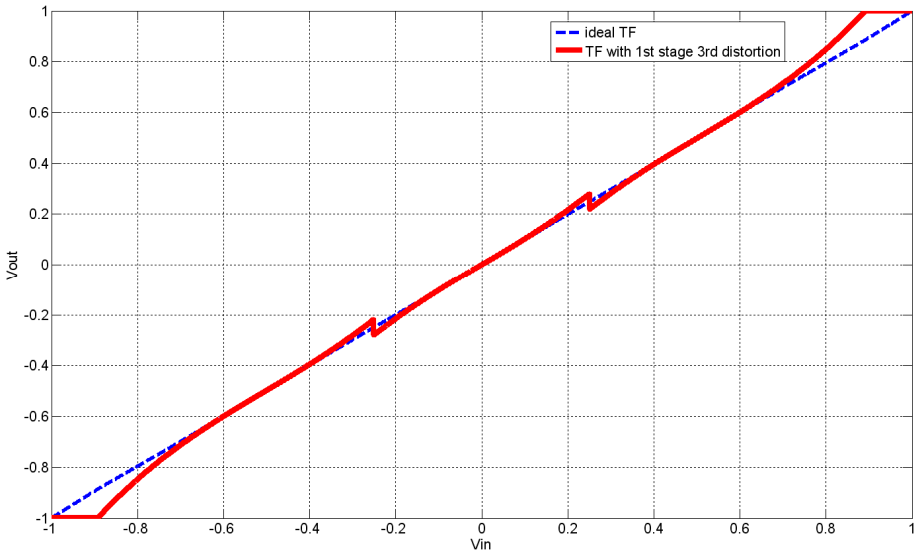


Figure 4.17: ADC transfer function with OTA non-linearity

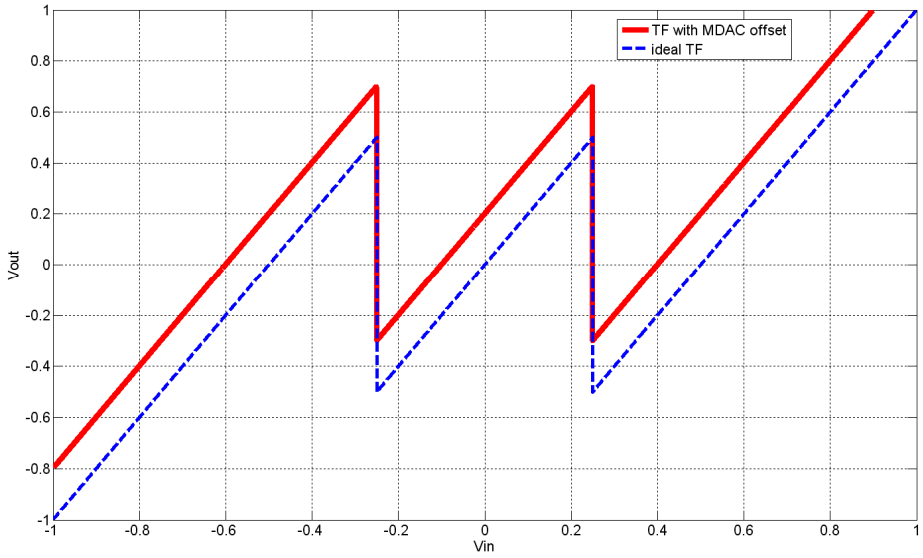


Figure 4.18: 1.5bit stage transfer function with OTA offset

1.5 bit stage is presented in Fig. 4.18 where stage offset is assumed to be the only non-ideality. Dashed line shows the ideal transfer function and real line includes offset. Fig. 4.19 shows that no linearity degradation would be introduced by offset in overall ADC. The shift can cause the stage output to saturate the remaining pipeline stages. The effect of this offset voltage can be minimized by using well known circuit techniques like auto-zeroing, i.e. connecting the amplifier in unity gain feedback during the sample

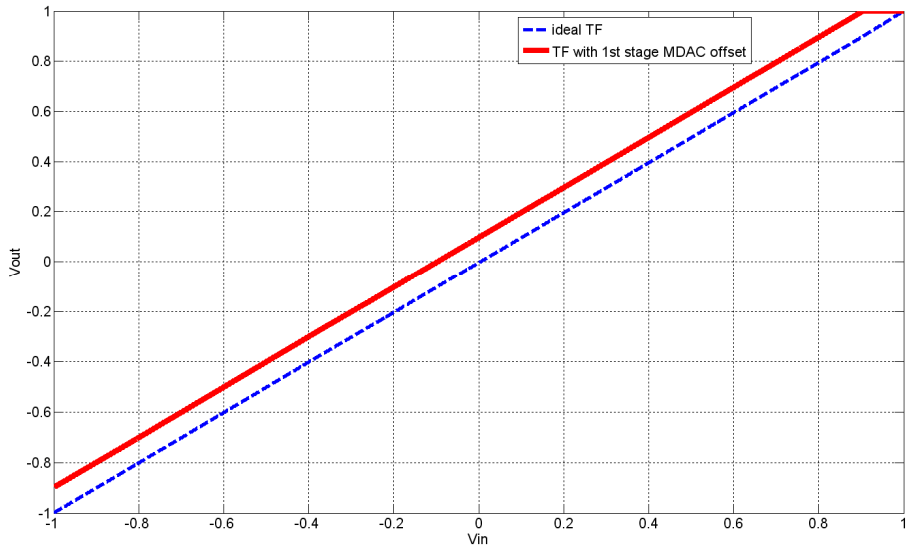


Figure 4.19: ADC transfer function with OTA offset

phase which would include thermal noise in both clock phases.

4.4.5 Stage gain error and reference error from capacitor mismatch

In switched capacitor MDACs, mismatch of sampling capacitor C_s and feedback capacitor C_f is a another major error source which degrades ADC's linearity. This problem is serious because mismatch would degrade not only stage gain error but also reference error. As mentioned before this error is described as a factor δ. The effect of the capacitor mismatch on the 1.5 bit stage transfer function is depicted in Fig. 4.20. It is noticed that when $V_{in} = \pm V_{ref}$, there is no error. Fig. 4.21 shows that linearity degradation would be introduced by mismatch in overall ADC. Due to the finite resolution of lithographic process, capacitor mismatch comes mainly from variations at the edges of the capacitor plates. Therefore, capacitors with large area to perimeter ratios will tend to have better matching. Variations in oxide thickness between the capacitor plates also affect the matching, but to a less degree (especially for small, adjacent capacitors). The standard deviation of the fractional matching error between two adjacent square capacitors can be modeled as

$$\delta = \frac{A_C}{S} \tag{4.11}$$

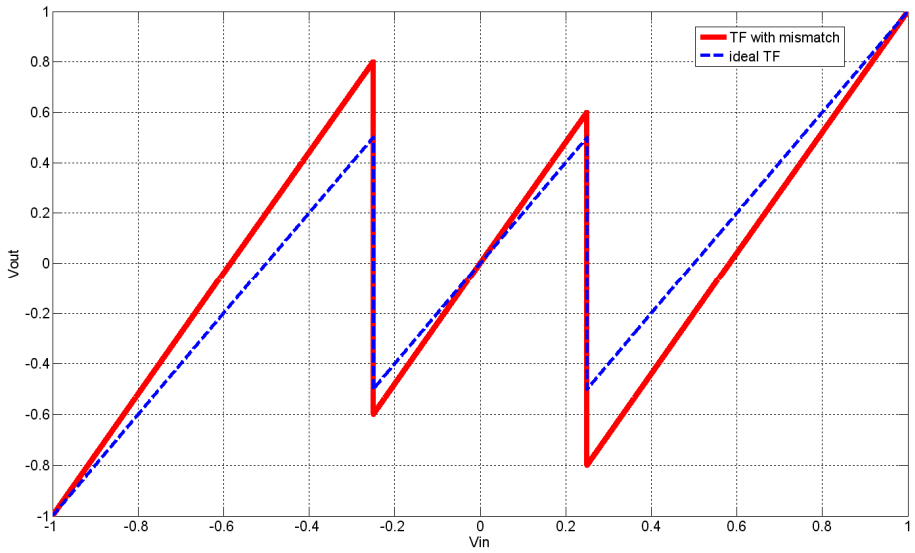


Figure 4.20: 1.5bit stage transfer function with capacitor mismatch

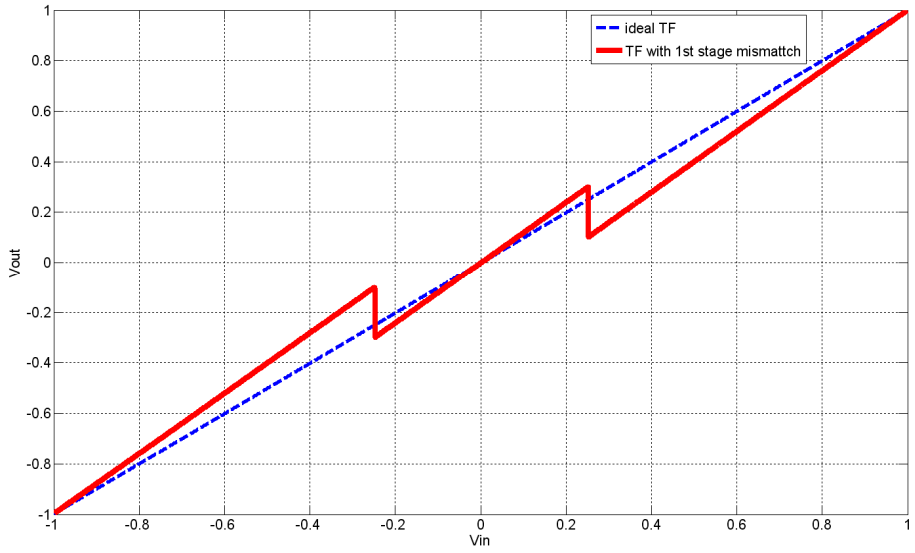


Figure 4.21: ADC transfer function with capacitor mismatch

Where S is one side length of capacitor in um. The value of A_c is technology dependent, but can typically range from $2 - 5\% um$.

4.4.6 DAC reference error

DAC reference is commonly realized by resistor string or capacitor array. Process variation and devices mismatch would generate reference voltage shifting from ideal

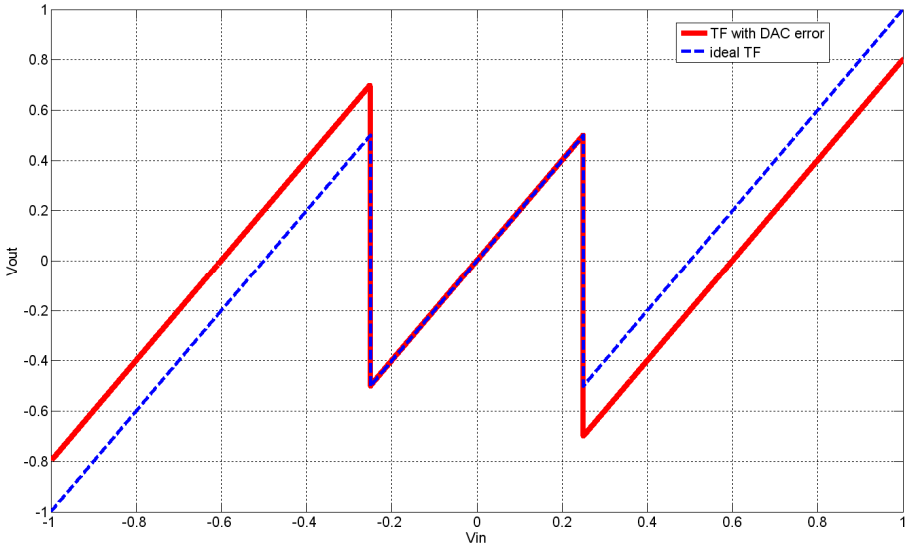


Figure 4.22: 1.5bit stage transfer function with DAC reference error

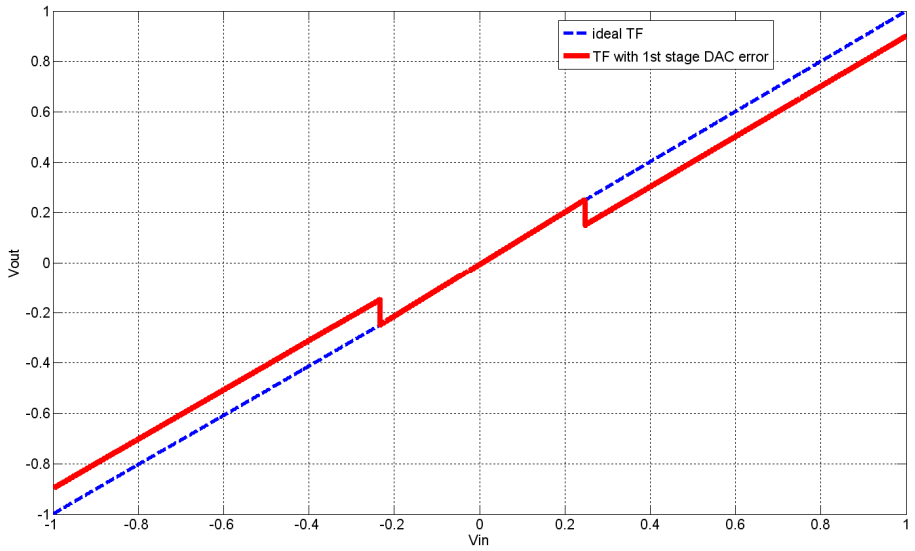


Figure 4.23: ADC transfer function with DAC reference error

value. 1.5bit stage transfer function with DAC reference error is shown in Fig. 4.22. where DAC offset is assumed to be the only non-ideality. Dashed line shows the ideal transfer function and real line includes offset. Fig. 4.23 shows what linearity degradation would be introduced by DAC reference error in overall DAC.

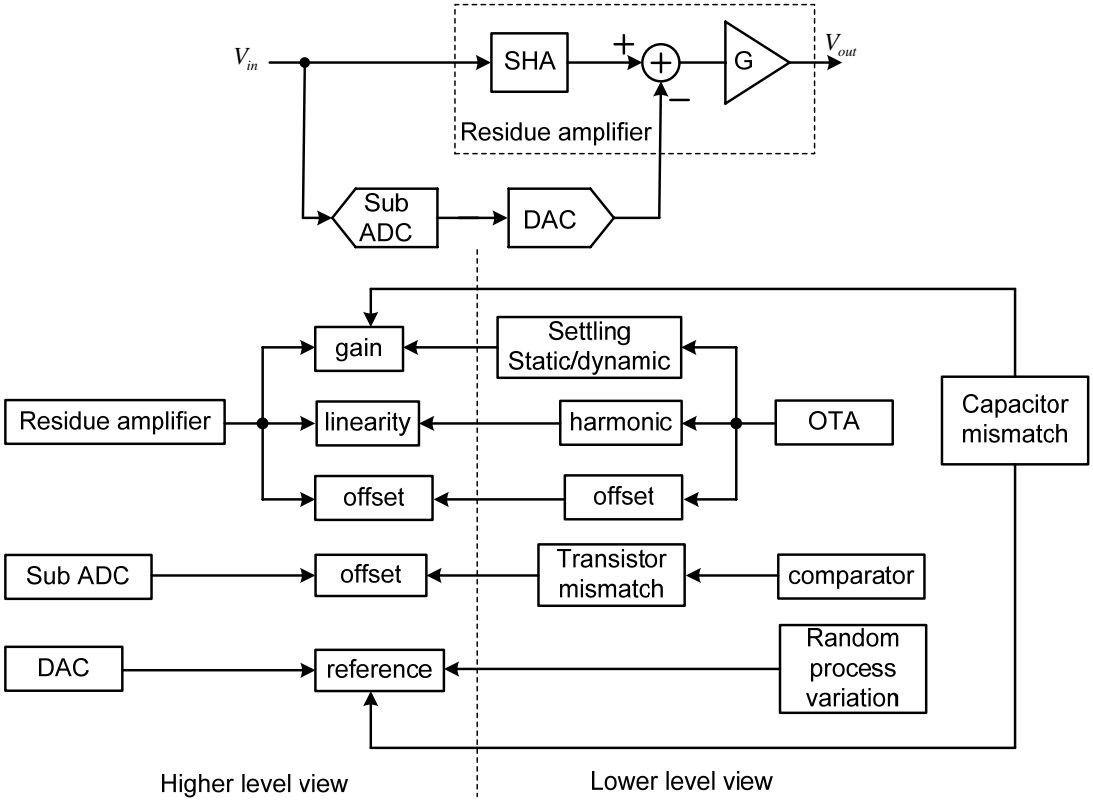


Figure 4.24: Pipeline stage and stage error source contribution scheme

4.4.7 Summary

Sections above have given the analysis of error sources in pipeline stage which degrade ADC's linearity from a system level view. The view directs the stage design based on Eq4.10 which means higher DC gain, faster settling and lower capacitor mismatch. It can be concluded that any single error happening at latter stage has less effect than the one happening at previous stage. Fig. 4.24 shows the overall relationship of stage blocks and error sources. A more detail investigation from circuit view would be given in Chapter 5 to connect sources mentioned here to circuit parameters which constrain ADC's design.

5 Pipeline ADC implementation

As demonstration of the pipelined ADC's architecture described in the previous chapters, a 1.2V, 10-bit, 25Msps pipelined ADC prototype was designed in a 0.13um CMOS technology. This chapter discusses specific implementation details including Sample and hold amplifier, residue stage, OTA, comparator and digital components.

5.1 Sampling switch

In MOS technology, sampling is implemented by storing the input signal voltage on a sampling capacitor followed by holding the voltage through some active feedback circuit such as SC amplifier. Since the achievable precision is limited by the initial accuracy of the sampled signal, sampling switch should be as ideal as possible.

The limitations of sampling can be modeled by one MOS transistor and one capacitor as shown in Fig. 5.1, which is usually called top plate sampling. A clock control signal is given to the gate of switch transistor. During the sampling phase of the clock, the voltage on the sampling capacitor C_s tracks the input voltage through the MOS transistor switch. Then, in the next clock phase when the clock goes low, the transistor turns off and the input voltage is held on the capacitor for further processing.

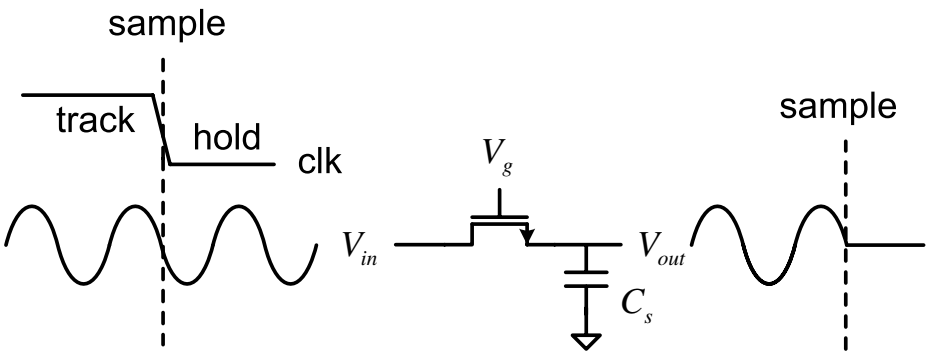


Figure 5.1: Top plate sampling principle

Table 5.1: Deterministic error and solution

Error source	Solution
Finite Bandwidth	Lower switch on-resistance; Bootstrapping/CMOS/clock boost
Input dependant distortion	Bootstrapping
Charge injection	Bottom sampling; Dummy transistor
Clock feedthrough	Differential path

In this real circuit, a number of non-idealities due to the switch introduce errors, and they can be categorized into two groups: deterministic components and random components.

5.1.1 Deterministic error

The deterministic component refers to an error source whose relationship with the signal is known to be consistent from sample to sample, such as the finite bandwidth of sampling switch, the signal-dependant charge injection from the MOS transistor, clock feedthrough, etc. Various circuit techniques have been developed to cancel or to suppress these effects to achieve high sampling accuracy. In Table. 5.1, error sources and possible solutions/techniques are shown. Deterministic components do not set the fundamental limitation to the first order at 8-12 bits resolution. Brief discussions on the deterministic error components are presented as follows.

5.1.1.1 On resistance

In actual implementations of SC circuits, on-resistance of the MOS switch can have a significant effect on the settling time of the circuit. High on-resistance in MOS switch not only slows down the circuit but also make the feedback system poorly damped or unstable if it is in the feedback loop as shown in Fig. 5.2. This results from the increase in phase shift by increasing the delay and thereby reducing the phase margin. In order to avoid this type of situation, low enough on-resistance of the switch is required. Using a too large switch, however, adds significant amount of drain/source junction parasitic

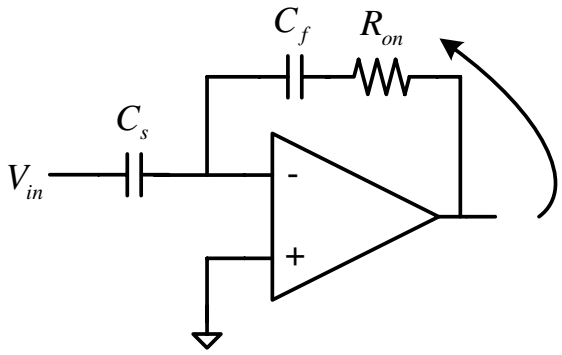


Figure 5.2: Switch resistor in the feedback loop can make the system unstable

capacitance at the output reducing the overall bandwidth.

Another point is input signal dependant distortion which comes from signal variation and affects the switch's on-resistance. This distortion will be transferred to the output of SHA degrading ADC's overall linearity. Based on transistor large signal operation equations in linear region, on-state resistance for NMOS, PMOS and CMOS switch can be derived as

$$\begin{aligned} R_{on,N} &= \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{tn})} \\ R_{on,P} &= \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{in} - |V_{tp}|)} \\ R_{on,eq} &= R_{on,N} || R_{on,P} \end{aligned} \tag{5.1}$$

Where μ is carrier mobility of semiconductor, C_{ox} is gate oxidation capacitor and V_{tn} , V_{tp} are the threshold voltages of NMOS and PMOS transistor respectively. It can be concluded that 1) NMOS switch only transfers lower voltage levels 2) PMOS switch only transfers higher voltage levels and 3) when $\mu_n C_{ox} (W/L)_N = \mu_p C_{ox} (W/L)_P$ is satisfied, input signal distortion in CMOS switch can be cancelled and it could only transfer moderate voltage levels.

On-resistance changes as input voltage increasing as shown in Fig. 5.3. Although CMOS gate provides enough performance, there is a serious problem in low power supply design. If $V_{DD} < V_{tn} + |V_{tp}| + Swing_{in}$, representing input signal swing, general CMOS gate can not used as switch unless clock is boosted. This happens at modern

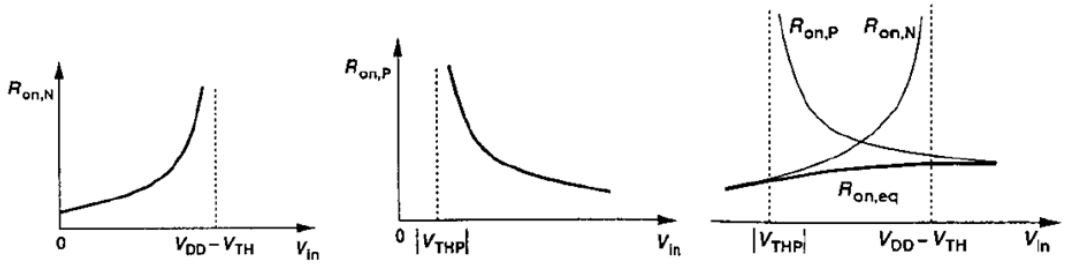


Figure 5.3: On resistance changes with input signal variation [6]

CMOS technology such as channel length less than 130nm with power supply less than 1.2V.

Assume top plate sampling as ideal first order system with a sine wave input signal, the error can be illustrated as

$$\begin{aligned} \varepsilon_{settling} &= V_{ref} e^{-\frac{t_s}{\tau}} < \frac{V_{FS}}{2^{N+m-i}} \times \frac{1}{2} \\ \Rightarrow R_{on} &< \frac{t_s/C_s}{(N+m-i)\ln 2} \end{aligned} \tag{5.2}$$

where τ is time constant of RC network, V_{ref} is signal amplitude, t_s is required settling time for the switch and N+m-i represents stage resolution with margin bit m. Note that most switches have a reset phase, which means the maximum step being V_{ref} not full scale voltage V_{FS}.

Track mode distortion can be analyzed by Volterra Series analysis allowing us to calculate the frequency domain response of nonlinear circuits. For example, relation between 3^{rd} harmonic and signal amplitude can be illustrated as[29]

$$|HD_3| \approx \frac{1}{4} \frac{V_{ref}^2}{(V_{GS}-V_t)^2} 2\pi f_{in} R_{on} C_s \tag{5.3}$$

Making overdrive voltage of the switch much larger than the signal amplitude, or the time constant of the switch much less than signal period, helps to suppress harmonics at the cost of lower voltage swing and huge switch size[30].

Table 5.4: Thermal noise contribution through analog chain

	OTA Pnoise stage Input referred $[V^2]$	OTA Pnoise ADC Input referred $[V^2]$	Stage Pnoise stage Input referred $[V^2]$
SHA	1.215E-08	1.22E-08	1.458E-08
MDAC1	1.864E-08	1.86E-08	2.796E-08
MDAC2	3.894E-08	9.74E-09	1.460E-08
MDAC3	3.894E-08	2.43E-09	3.650E-09
MDAC4	3.894E-08	6.08E-10	9.126E-10
MDAC5	4.469E-08	1.745E-10	2.618E-10
MDAC6	4.469E-08	4.364E-11	6.546E-11
MDAC7	4.469E-08	1.091E-11	1.636E-11
MDAC8	4.469E-08	2.727E-12	4.091E-12

5.4.3 Dynamic comparator

Since redundancy is applied to relax the comparator offset requirements, dynamic comparators are used in low-resolution pipeline stages because of their potential for low power and small area. The concept of a dynamic comparator is restricted to single-stage topologies without static power dissipation[26]. Since a dynamic comparator is turned off whenever inactive and small transistors are preferred to minimize power and area, it is inevitably sensitive for larger offsets. A widely used dynamic comparator in pipeline ADC, presented in Fig. 5.31, was used. Transistors $M_1 - M_4$, biased in linear region, adjust the threshold and above them transistors $M_5 - M_{12}$ form a latch. The operation of dynamic comparator is as follows. Here N-input configuration is used as example and P-input circuit is similar in operation. Because $M_1 - M_4$ work in linear region as a resistor, their conductance can be illustrated as

$$\begin{aligned} G_1 &= \mu_n C_{ox} \left[\frac{W_{in}}{L} (V_{inp} - V_t) + \frac{W_{ref}}{L} (V_{refn} - V_t) \right] \\ G_2 &= \mu_n C_{ox} \left[\frac{W_{in}}{L} (V_{inn} - V_t) + \frac{W_{ref}}{L} (V_{refp} - V_t) \right] \end{aligned} \tag{5.33}$$

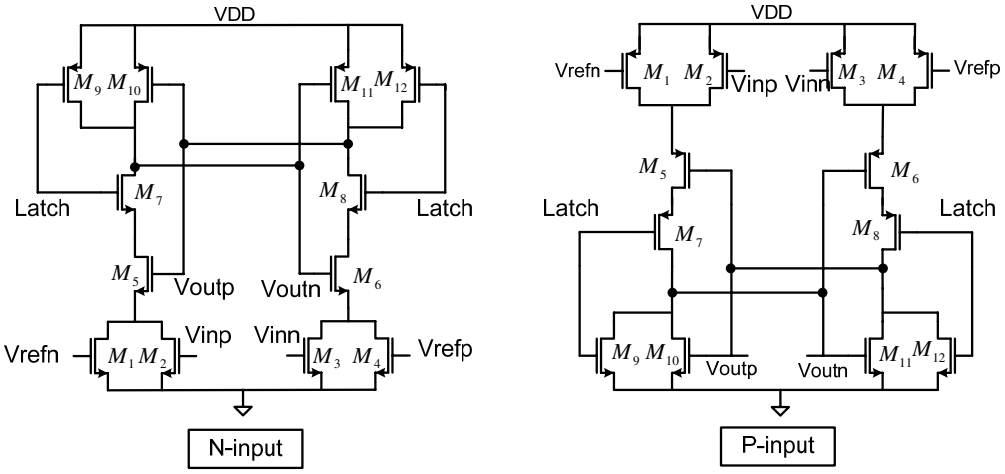


Figure 5.31: Dynamic comparator with N-input and P-input style

Where '1' represents positive input half side, '2' represents negative input half side. The difference of conductance is

$$\begin{aligned} \Delta G = G_1 - G_2 &= \mu_n C_{ox} \frac{W_{in}}{L} \left[(V_{inp} - V_{inn}) - \frac{W_{ref}}{W_{in}} (V_{refp} - V_{refn}) \right] \\ &= \mu_n C_{ox} \frac{W_{in}}{L} (V_{in} - V_{t,comp}) \\ V_{t,comp} &= \frac{W_{ref}}{W_{in}} (V_{refp} - V_{refn}) \end{aligned} \tag{5.34}$$

From Eq5.34 if $V_{refp} - V_{refn}$ equals ADC's V_{ref} , $W_{ref}/W_{in} = 0.25$, the transition level is ideally at $\pm 0.25 V_{ref}$, as required. Based on the relationship set above, if $V_{in} > 0.25 V_{ref}$, positive half resistor R_1 is smaller than negative half side R_2 . Since output at previous phase is high resulting from non-latched condition, M10 and M11 keeps off and currents on two path becomes equal at latching instant. So drain voltage of M7 is smaller than M8's drain voltage and positive feedback drives V_{outp} to high and V_{outn} to low. There are two aspects should be mentioned: 1) M7 and M8 is latch switches which turn off the DC path current when latch equals low. 2) after this comparator, a SR latch has to be used to keep output constant without changing as latch. The Monte Carlo simulation results are shown in Fig. 5.32. From this figure, it can be observed that the mismatches in the circuits does not affect offset of the output very much. Thus this design is not

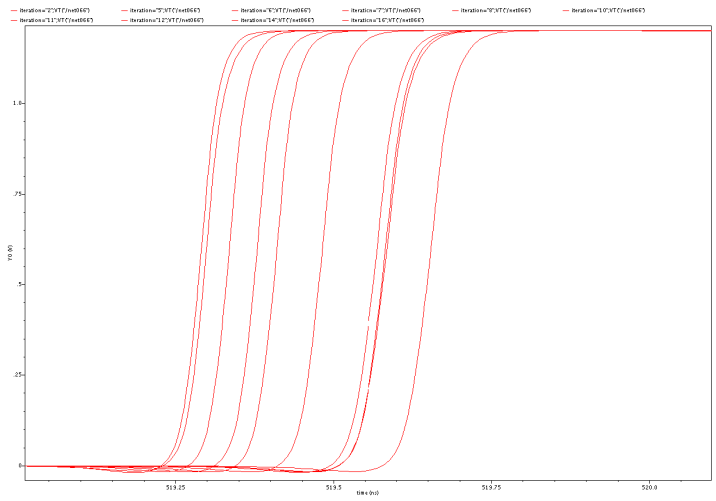


Figure 5.32: Dynamic comparator transition level offset due to process variation and mismatch

sensitive to mismatches in components. On the other hand, 1.5bit stage configuration can tolerate this small offset due to digital correction.

5.4.4 2bit flash ADC

So far 1.5bit pipeline stage and SHA have been described. The last analog part circuit of the ADC is the last stage of the pipeline chain. The last stage is a flash ADC as sub-ADC but it has less offset tolerance because there is no digital correction for this stage. A very popular way to implement this comparator is using an input sensing preamplifier followed by a regenerative latch[39]. The offset voltage, generated by the component mismatch and process parameter variations, is reduced by the pre-amplification and can be further minimized by applying special techniques, for example, auto-zeroing. In this design, a comparator with pre-amplifier and auto-zeroing technique is used to increase offset tolerance as shown in Fig. 5.33. The pre-amplifier shown in Fig. 5.34 does not need very high DC gain. Generally the difference between reference and Vin is enlarged by 4 6 times. Auto-zero technique is often used to reduce offset in switch capacitor circuit. In reference phase, circuit configuration is shown in Fig. 5.35. Pre-amplifier's offset voltage is stored on the capacitor in sampling phase as follows:

$$V_{C+} - V_{C-} = (V_{ref+} - V_{ref-}) - V_{os} \tag{5.35}$$

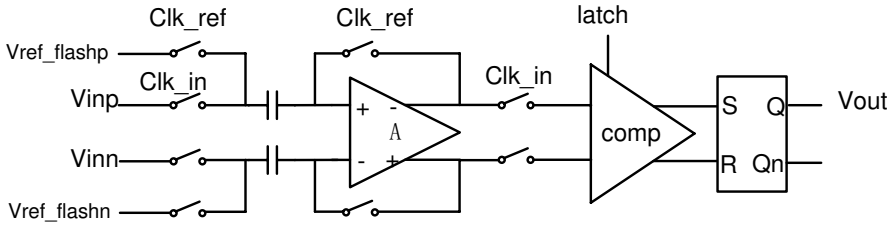


Figure 5.33: Comparator used in last stage flash ADC

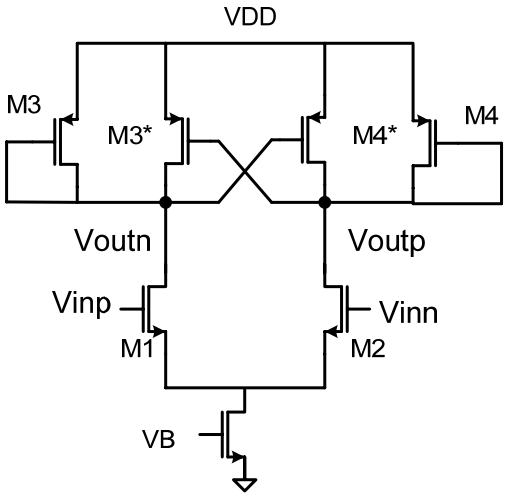


Figure 5.34: Pre-amplifier used in accurate comparator

In comparison phase, circuit configuration is shown in Fig. 5.35, operation is this phase is

$$\begin{aligned} V_{out} &= AV_d \\ V_d &= (V_{in+} - V_{C+} - V_{os} - (V_{in-} - V_{C-})) \\ &= (V_{in+} - V_{C+} - V_{os} - V_{in-} + V_{C-}) \\ &= (V_{in+} - V_{in-} - (V_{C+} - V_{C-}) - V_{os}) \\ &= (V_{in+} - V_{in-} - (V_{ref+} - V_{ref-})) \\ &= V_{in} - V_{ref} \end{aligned} \tag{5.36}$$

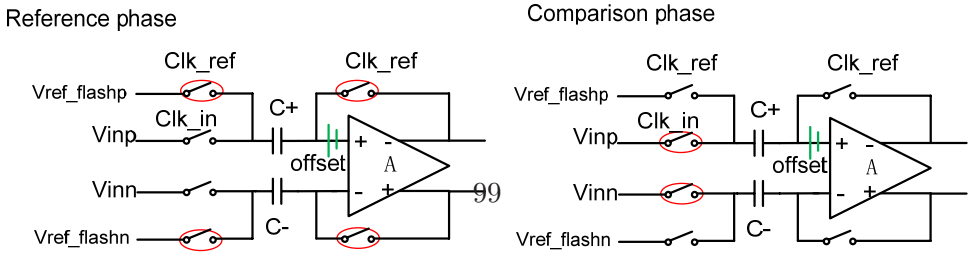


Figure 5.35: Circuit configuration of SC comparator using auto-zeroing in different phase

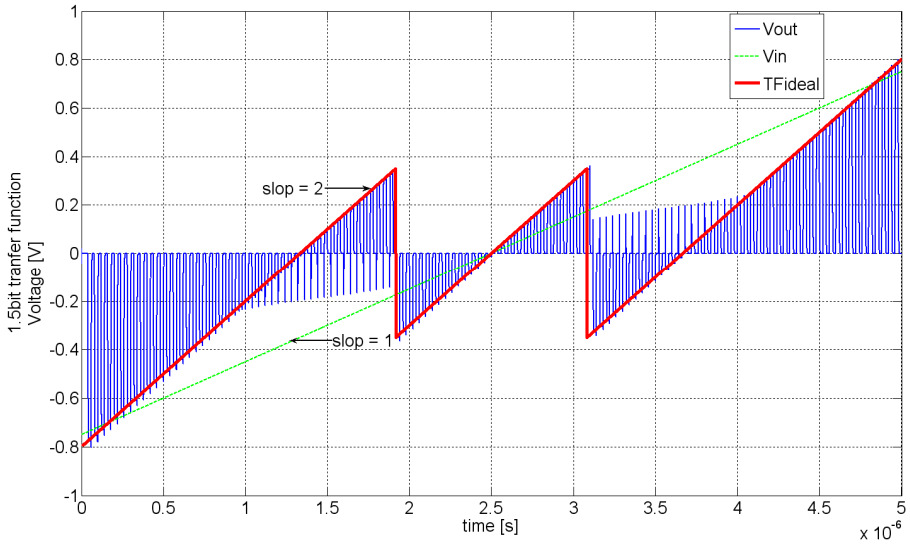


Figure 5.36: Transfer function of 1.5bit pipeline stage using SC technology

5.4.5 summary

From Fig. 5.36, 1.5bit pipeline stage operates according to requirement. The thin line is circuit output at a slow ramp input. Heavy line is ideal transfer function of 1.5bit stage. Dashed line is straight with slope equal to one.

5.5 Digital components

In this design, digital circuit is used to realize clock generator and expander after ADC core to recover compressing filter's output.

5.5.1 Clock generator

All the pipeline stages operate on a two-phase, non-overlapping clock. All the odd stages sample during phase $clk2$ and present a valid residue output to the next stage during phase $clk1$[23]. The even stages work on the opposite phases, so that all stages operate concurrently. Fig. 5.37 shows the clock wave forms. Being different from general non-overlapping realization, latch signal falling edge is set even a little earlier than bottom-plate-sampling clock to avoid transient gain unstable. Simulation shows that this operation increase SNDR by extra 1.5dB. But in high speed analog to digital

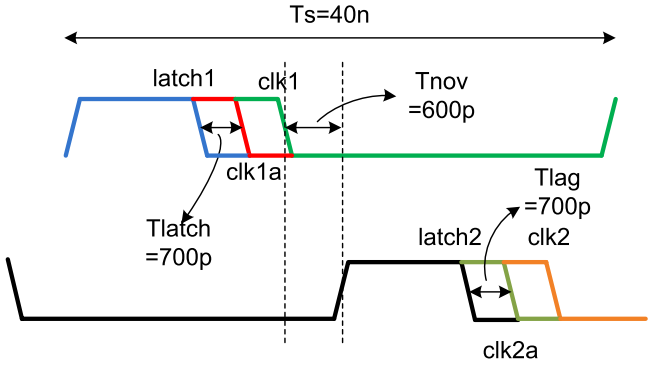


Figure 5.37: Two phase non-overlapping clock scheme

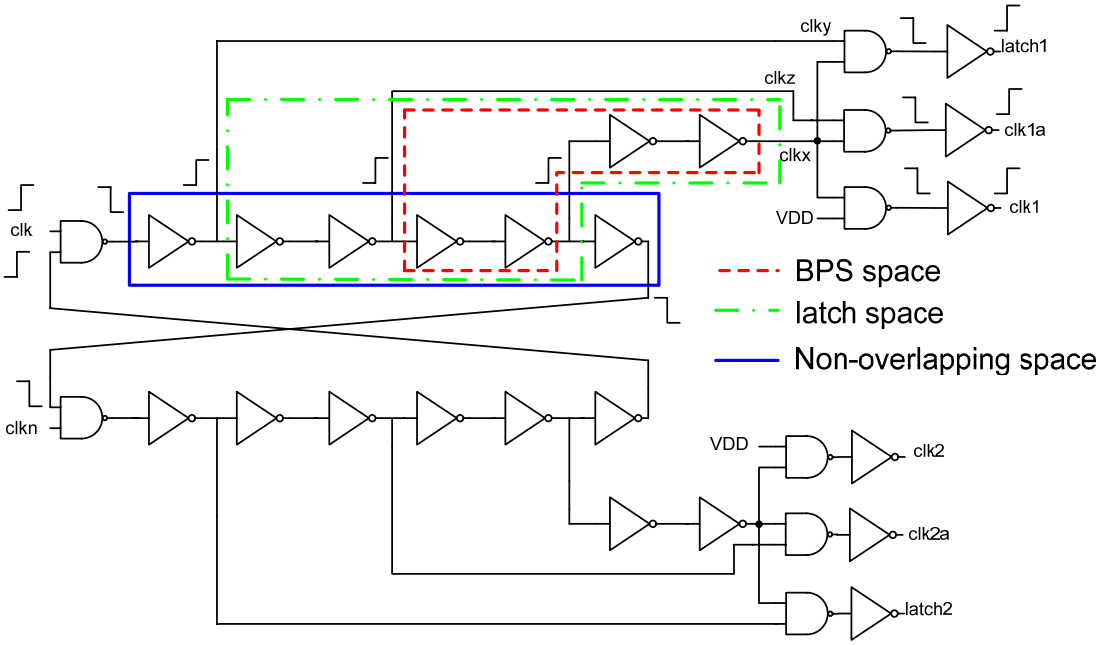


Figure 5.38: Clock generator circuit realization

converter this would cost some settling time margin for OTA. The circuit shown in Fig. 5.38 was used in the prototype. An external 50% duty-cycle reference clock drives input *clkin*. Latch, *clka* and *clk* have rising edge at the same time because the last NAND gate force to wait for synchronous rising edge of *clkx*, *clky* and *clkz*. Opposite to rising edge, the instant of falling edge of latch, *clka* and *clk* are different because the last NAND responses to individual activation of falling edge. All the delays are generated by using NAND and NOT gates.

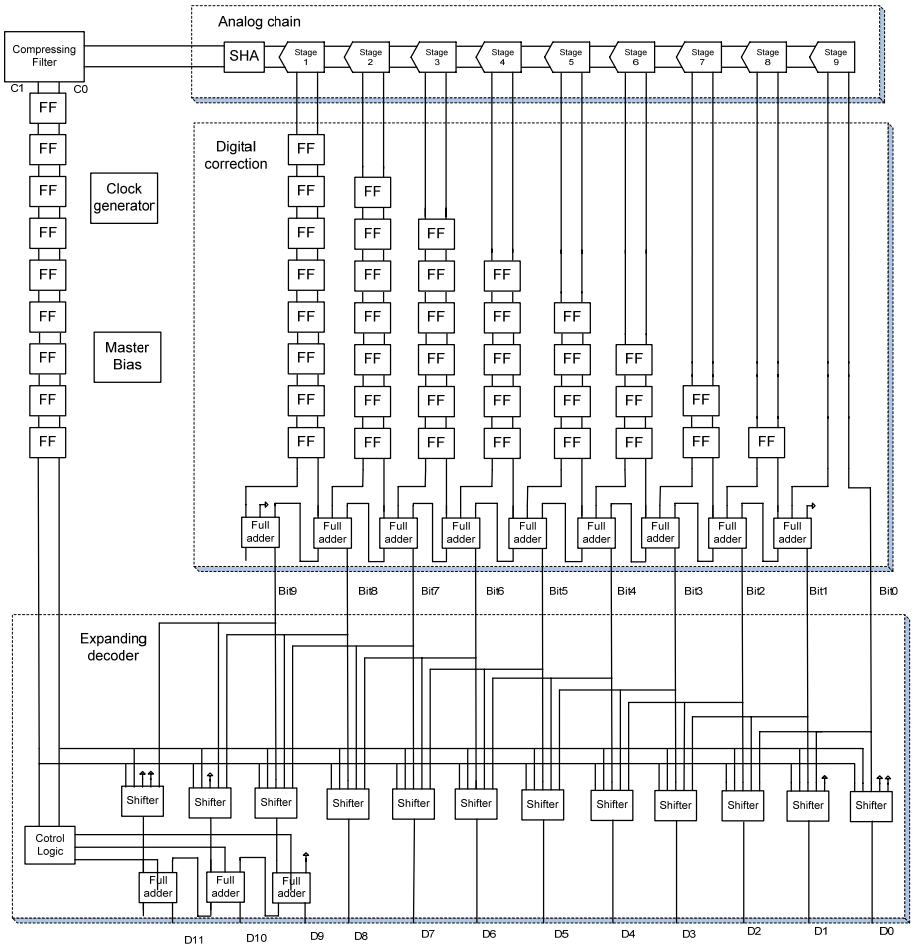


Figure 5.39: Pipeline ADC including analog chain, digital correction and companding decoder

5.5.2 Digital correction and Companding decoder

To correct the output of analog chain, delay elements and full adders are included, as the digital correction. Although each stage generates 2bit output codes, they are not time synchronous. Every output of single stage is delayed by half of clock cycle compared to its previous stage. This delay should be compensated before add them together. Flip-flop is used as delay element. Entire pipeline ADC with expanding decoder is shown in Fig. 5.39.

The expanding decoder turns pipeline ADC core's 10-bit output Bit9 Bit0 to new 12bit code D11 D0, where D11 and D10 as companding bits. The algorithm is illustrated as follows: assume that there is a analog input value V_{analog}. It is quantized by ADC

core to integer X including quantization error. Considering bipolar transfer function of ADC, the recovered analog value of X is

$$\begin{aligned} V_{analog,out} &= X \times \Delta_{core} - 0.5V_{FS,core} \\ \Delta_{core} &= \frac{1.4}{1024} \\ V_{FS,core} &= 1.4 \end{aligned} \tag{5.37}$$

Where full scale range represents 1.4 V_{pp} of ADC core.To keep the same quantization error and take the output corresponding to 5.6 V_{pp} as the initial condition, the new conversion relation is

$$V_{analog,out} = X \times \Delta_{companding} - 0.5V_{FS,companding} \tag{5.38}$$

where

$$\begin{aligned} \Delta_{core} = \Delta_{companding} &= \frac{1.4}{1024} \\ V_{FS,companding} &= 5.6 \end{aligned} \tag{5.39}$$

If state=00, input signal ranges small, then

$$V_{analog,out} = X \times \frac{1.4}{1024} - 2.8 \tag{5.40}$$

Here output X is the same as ADC core. But there is a DC offset 2.1V compared with the true value. So output codes of decoder need to be add another 011 at MSB side. Similarly if state=01, input signal ranges moderate, then

$$V_{analog,out} = 2X \times \frac{1.4}{1024} - 2.8 \tag{5.41}$$

Here output X is enlarged by 2 times and the offset is 1.4V. So output codes of decoder need to be add another 010 at MSB position. Finally if state=11, input signal ranges high, then

$$V_{analog,out} = 4X \times \frac{1.4}{1024} - 2.8 \tag{5.42}$$

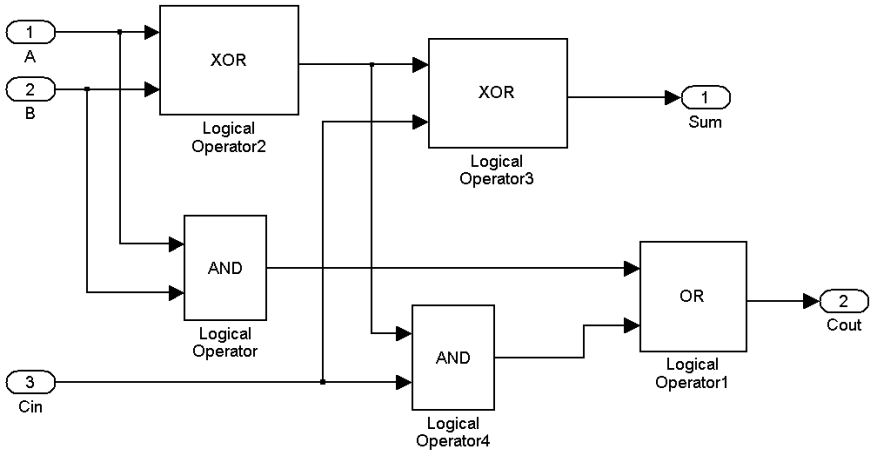


Figure 5.40: Full adder circuit realization

Here output X is enlarged by 4 times and the offset is zero. All of the algorithm mentioned above can be realized by logic circuit shown in Fig. 5.39. Times 2 logic circuit is a bit shifter in binary code.

Compressing filter gives the filtered output and statement variables C1 and C0 which contains state information as mentioned in Chapter 1. Based on C1 and C0 there are 12 shifters and a simple logic generates control signal building up decoder. Fig. 5.40 shows the realization of full adder. Here A and B is addend and augend. C_{in} is carry from lower stage. C_{out} is carry given to high stage.

As all of the circuit blocks have been designed, in next chapter, dynamic performance of the entire ADC with or without expanding decoder would be given.

6 ADC's simulation result

6.1 Introduction

This chapter discusses the performance characteristics of the designed ADC. In order to test the functionality and performance of the schematic, an ideal DAC is set after ADC's output. The dynamic performance of the ADC was simulated by using a 1024 points Fast-Fourier Transform (FFT) of the DAC's output for the single and two input tones.

6.2 Dynamic Performance

The linearity and noise performance of the converter can be characterized by a signal-to-noise-plus-distortion (SNDR) measurement. The SNDR is defined as the ratio of signal power to all other noise and harmonic power in the spectra. This characteristic determines the smallest signal that can be detected in the presence of noise, and the largest signal that does not overload the converter. The peak SNDR is highest achievable SNDR for a given converter, which usually occurs for an input signal near full scale. Ideally, if an N-bit converter has no distortion and is noiseless, the peak SNDR is given by (6×N+1.72)dB. The peak SNDR for a Nyquist rate sine wave input was measured at 60.3dB with a clock frequency of 25MHz including thermal noise as shown in Table 5.4. SFDR between signal and the largest spur is 78dB. The result of single tone test in 1024 point FFT is shown in Fig. 6.1. At the same time two tone test is also done and result is shown in Fig. 6.2. Here IMD3 is measured as 76.2dB at Nyquist rate. So dynamic linearity of ADC core satisfies specification given in Chapter 3.

To verify the companding principle, the dynamic performances with and without companding are compared as follows. Firstly, SNDR and SFDR depending on different input frequency at both modes are plotted in Fig. 6.3. Fig. 6.4 shows SNDR and SFDR

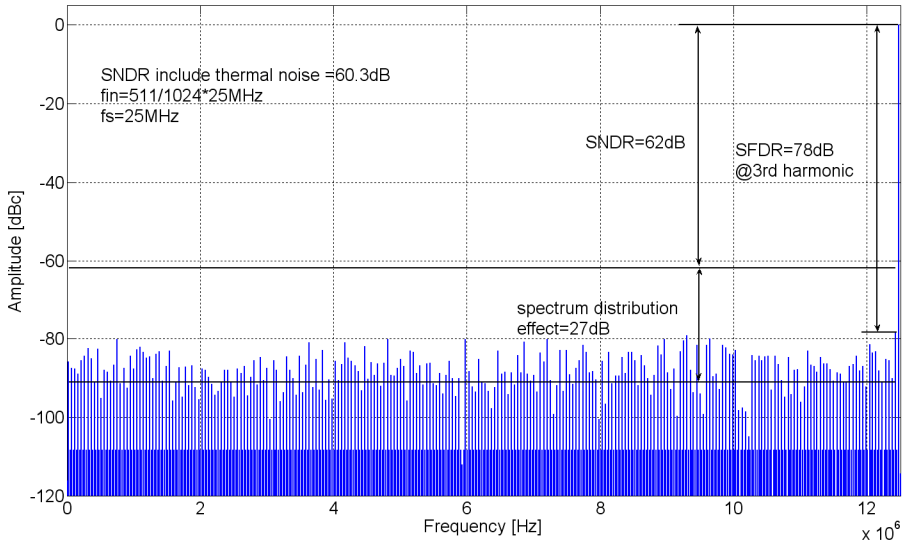


Figure 6.1: 1024 single tone FFT of Pipeline ADC core

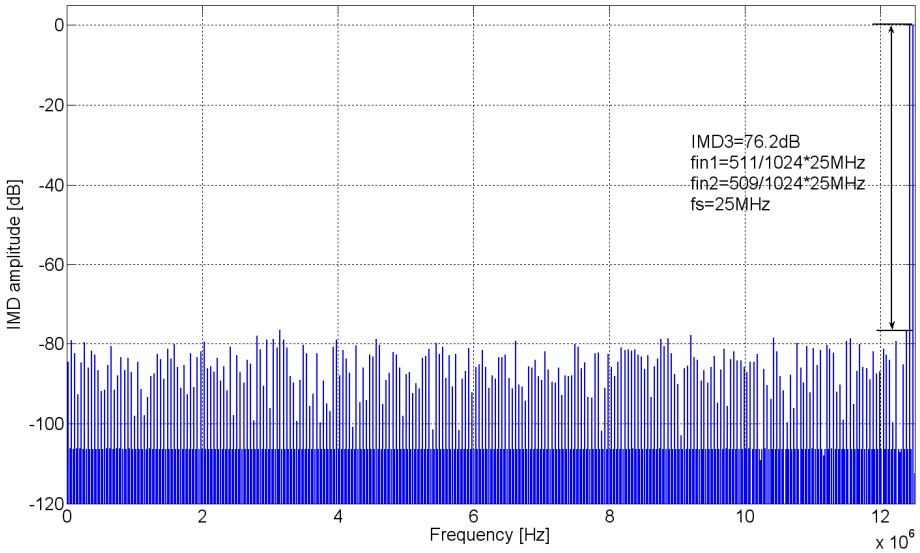


Figure 6.2: 1024 two tone FFT of Pipeline ADC core

with different input ranges at both modes.

From Fig. 6.3, we can find that companding ADC and ADC core has similar dynamic performance which is slightly dependent on input frequency. In Fig. 6.4, ADC core's SNDR and SFDR increase linearly as input signal increasing while companding ADC processing system follows this characteristics but it is divided into three segments according to statements. When input signal is small, output performance follows ADC

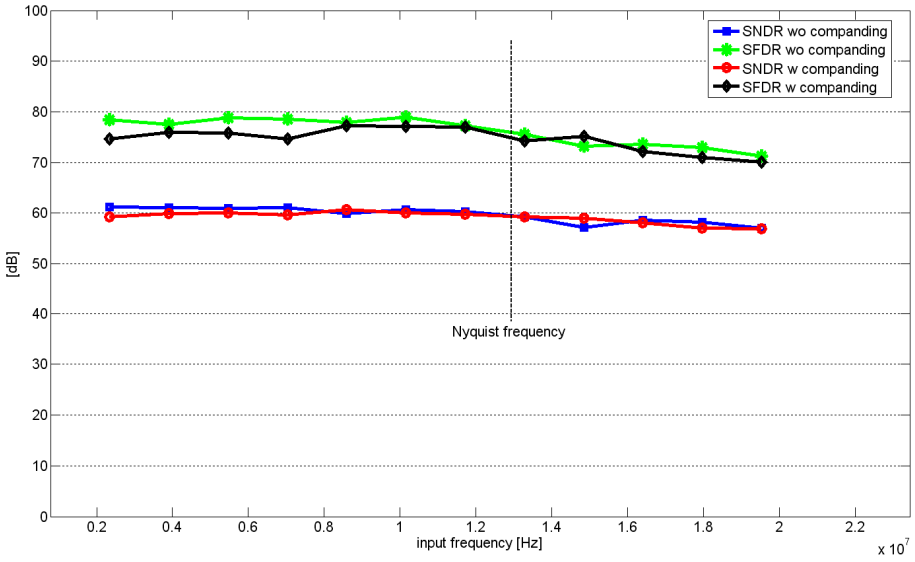


Figure 6.3: Simulated dynamic performance versus input frequency

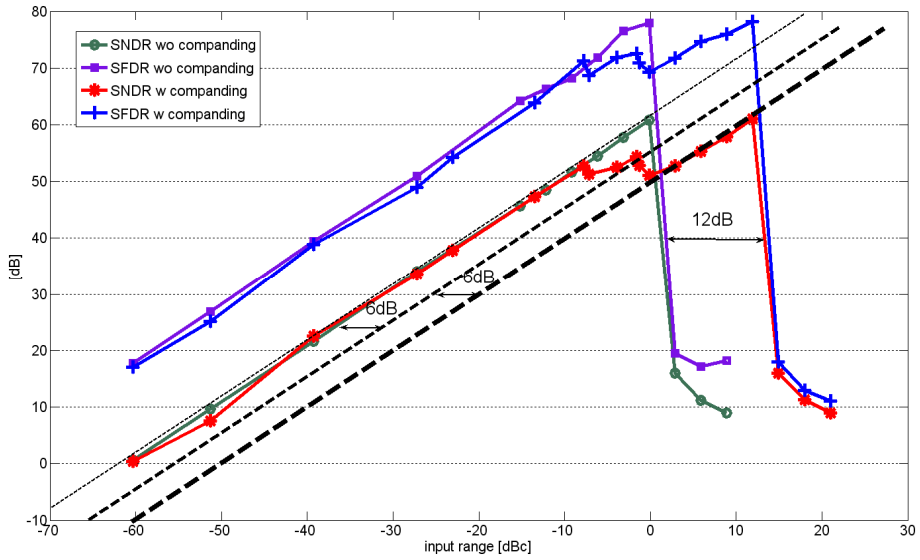


Figure 6.4: Simulated dynamic performance versus input signal range

core's behavior. If state equals to 01, output DR is enlarged by 6dB. When input signal is even larger, another 6dB DR is obtained by companding. Finally DR is increased by 12dB totally with the same quantization resolution.

7 Conclusion

Design of the compressing ADC in companding baseband interface is demonstrated including a 10-bit 25Msps sampling rate pipeline ADC and expanding back-end digital processing circuit for 802.11a/g application. Main ADC specifications, such as, SNDR, SFDR, IMD3 and speed requirement are derived from communication standard and the receiver budget link. As a pipeline ADC, main error sources which degrade linearity and noise performance of ADC are investigated. Using bootstrapping switch improves sampling linearity up to around 80dB. The switched OTA technique saves around 30% bias current. Gain-boosting is used to boost DC gain of the OTA up to 94dB. Dynamic comparator is used to implement sub-ADC without any DC current resulting in less power compared to flash ones. After digital correction, output codes are transferred to expanding decoder, which keeps the same resolution performance as the operation without companding but improving 12dB dynamic range. A performance summary of ADC core is given in Table7.1. Table7.2 shows the comparison of this work and some other ADCs [40], [41],[42], with comparable parameters. This design shows the standout FOM in this category at the cost of two companding bits.

Table 7.1: Summary of ADC core performance

Technology	0.13um CMOS
Power supply	1.2V
Sampling frequency	15MHz
SNDR	60.3dB
SFDR	78dB
IMD3	76.2dB
ENOB	9.7bit
Power	28mW
FOM	1.34pJ/step

Table 7.2: ADC performance comparison

	Process	Sampling frequency [MHz]	Resolution [bits]	Power [mW]	FOM [pJ/step]
Ahmed[40]	1.8V 0.18um	50	10	35	1.57
Yun[41]	1.8V 0.18um	10	14	112	2.85
Treichler[42]	1.2V 0.13um	50	12	111	1.98
This work	1.2V 0.13um	25	10	28	1.34

Bibliography

[1] V. Maheshwari, W.A. Serdijn, and J.R. Long, "Companding baseband switched capacitor filters and adcs for wlan applications," *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pp. 749–752, May 2007.

[2] A. Behzad, "Wireless lan radios: System definition to transistor design," 2008.

[3] LAN/MAN Standards Committee of the IEEE Computer Society, "Wireless lan medium access control (mac) and physical layer (phy) specifications: Higher-speed physical layer extension in the 2.4 ghz band," 1999.

[4] LAN/MAN Standards Committee of the IEEE Computer Society, "Wireless lan medium access control (mac) and physical layer (phy) specifications high-speed physical layer in the 5 ghz band," 1999.

[5] F.Malberti, "Data converters," Pavia University 2007.

[6] B. Razavi, "Design of analog cmos integrated circuit," UCLA 2001.

[7] W. Eberle, "Wireless transceiver systems design," 2008.

[8] LAN/MAN Standards Committee of the IEEE Computer Society, "Wireless lan medium access control (mac) and physical layer (phy) specifications amendment 4: Further higher data rate extension in the 2.4 ghz band," 2003.

[9] A. Baschirotto V. Giannini, J. Craninckx, "Baseband analog circuits for software defined radio," 2008.

[10] M.T. Ozgun, Y. Tsividis, and G. Burra, "Dynamic power optimization of active filters with application to zero-if receivers," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 6, pp. 1344–1352, June 2006.

[11] L.reza, "Lecture of nyquist analog to digital converters," Delft University of Technology 2008.

[12] L. Barrandon, S. Crand, and D. Houzet, "Systematic figure of merit computation for the design of pipeline adc," *Design, Automation and Test in Europe, 2005. Proceedings*, pp. 277–278 Vol. 1, March 2005.

[13] R.Plassche, "Cmos integrated analog to digital and digital to analog converters," 2003.

[14] B.Razavi, "Principles of data converters system design," UCLA 1995.

[15] R.H. Walden, "Analog-to-digital converter survey and analysis," *Selected Areas in Communications, IEEE Journal on*, vol. 17, no. 4, pp. 539–550, Apr 1999.

[16] B.Razavi, "Rf microelectronics," UCLA 1998.

[17] P. Malla, H. Lakdawala, R. Naiknaware, S. Krishnamurthy, and K. Kornegay, "Sigma-delta adc design considerations for wifi/wimax receivers," *Signals, Circuits and Systems, 2007. ISSCS 2007. International Symposium on*, vol. 1, pp. 1–4, July 2007.

[18] S. Reekmans, P. Rombouts, and L. Weyten, "Sigma-delta adc design considerations for an umts receiver," *Circuits and Systems, 2006. MWSCAS '06. 49th IEEE International Midwest Symposium on*, vol. 2, pp. 659–663, Aug. 2006.

[19] Yangjin Oh and B. Murmann, "System embedded adc calibration for ofdm receivers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, no. 8, pp. 1693–1703, Aug. 2006.

[20] V. Giannini, J. Craninckx, S. D'Amico, and A. Baschirotto, "Flexible baseband analog circuits for software-defined radio front-ends," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 7, pp. 1501–1512, July 2007.

[21] O. Jeon, R.M. Fox, and B.A. Myers, "Analog agc circuitry for a cmos wlan receiver," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 10, pp. 2291–2300, Oct. 2006.

[22] S.H. Lewis, H.S. Fetterman, Jr. Gross, G.F., R. Ramachandran, and T.R. Viswanathan, "A 10-b 20-msample/s analog-to-digital converter," *Solid-State Circuits, IEEE Journal of*, vol. 27, no. 3, pp. 351–358, Mar 1992.

[23] A.M. Abo and P.R. Gray, "A 1.5-v, 10-bit, 14.3-ms/s cmos pipeline analog-to-digital converter," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 5, pp. 599–606, May 1999.

[24] K. Hadidi and G.C. Temes, "Error analysis in pipeline a/d converters and its applications," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 39, no. 8, pp. 506–515, Aug 1992.

[25] E. Bilhan, P.C. Estrada-Gutierrez, A.Y. Valero-Lopez, and F. Maloberti, "Behavioral model of pipeline adc by using simulink(r)," *Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on*, pp. 147–151, 2001.

[26] T.B. Cho and P.R. Gray, "A 10 b, 20 msample/s, 35 mw pipeline a/d converter," *Solid-State Circuits, IEEE Journal of*, vol. 30, no. 3, pp. 166–172, Mar 1995.

[27] R. Schreier, J. Silva, J. Steensgaard, and G.C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.

[28] H. Ishii, K. Tanabe, and T. Iida, "A 1.0 v 40mw 10b 100ms/s pipeline adc in 90nm cmos," *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, pp. 395–398, Sept. 2005.

[29] Wei Yu, Subhajit Sen, and B.H. Leung, "Distortion analysis of mos track-and-hold sampling mixers using time-varying volterra series," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 46, no. 2, pp. 101–113, Feb 1999.

[30] T.W. Brown, T.S. Fiez, and M. Hakkarainen, "Prediction and characterization of frequency dependent mos switch linearity and the design implications," *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE*, pp. 237–240, Sept. 2006.

[31] K.-L. Lee and R.G. Mayer, "Low-distortion switched-capacitor filter design techniques," *Solid-State Circuits, IEEE Journal of*, vol. 20, no. 6, pp. 1103–1113, Dec 1985.

[32] K. Bult and G.J.G.M. Geelen, "A fast-settling cmos op amp for sc circuits with 90-db dc gain," *Solid-State Circuits, IEEE Journal of*, vol. 25, no. 6, pp. 1379–1384, Dec 1990.

[33] H. Aminzadeh, M. Danaie, and R. Lotfi, "Design of two-stage miller-compensated amplifiers based on an optimized settling model," *VLSI Design, 2007. Held jointly with 6th International Conference on Embedded Systems., 20th International Conference on*, pp. 171–176, Jan. 2007.

[34] S.H. Lewis R.G. Meyer P.R. Gray, P.J. Hurst, "Design of analog cmos integrated circuit," UC Berkeley 2001.

[35] J. Crols and M. Steyaert, "Switched-opamp: an approach to realize full cmos switched-capacitor circuits at very low power supply voltages," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 8, pp. 936–942, Aug 1994.

[36] M. Waltari and K.A.I. Halonen, "1-v 9-bit pipelined switched-opamp adc," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 1, pp. 129–134, Jan 2001.

[37] W. Yang, D. Kelly, L. Mehr, M.T. Sayuk, and L. Singer, "A 3-v 340-mw 14-b 75-msample/s cmos adc with 85-db sfdr at nyquist input," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 12, pp. 1931–1936, Dec 2001.

[38] C.C. Enz and G.C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov 1996.

[39] I. Mehr and D. Dalton, "A 500-msample/s, 6-bit nyquist-rate adc for disk-drive read-channel applications," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 7, pp. 912–920, Jul 1999.

[40] I. Ahmed and D.A. Johns, "A 50-ms/s (35 mw) to 1-ks/s (15 w) power scaleable 10-bit pipelined adc using rapid power-on opamps and minimal bias current variation," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 12, pp. 2446–2455, Dec. 2005.

[41] Yun Chiu, P.R. Gray, and B. Nikolic, "A 1.8 v 14 b 10 ms/s pipelined adc in 0.18 m cmos with 99 db sfdr," *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pp. 458–539 Vol.1, Feb. 2004.

[42] Jurg Treichler, Qiuting Huang, and Thomas Burger, "A 10-bit enob 50-ms/s pipeline adc in 130-nm cmos at 1.2 v supply," *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European*, pp. 552–555, Sept. 2006.