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Cavallo, Daniele; Syed, Waqas H.; Neto, Andrea

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Artificial Dielectric Enabled Antennas for High Frequency Radiation From Integrated Circuits

Daniele Cavallo[1], Waqas H. Syed[1], Andrea Neto[1]
[1]Microelectronics dept., Delft University of Technology, Delft, The Netherlands, d.cavallo@tudelft.nl

***Abstract*—At millimeter and sub-millimeter wave frequencies, electronic circuits and antennas are often located on the same semiconductor chip to facilitate their interconnection. However, on-chip antennas are characterized by very poor radiation efficiency and extremely narrow bandwidth. This is because they are situated at small electrical distance from a ground plane that shields the antenna from the lossy bulk. High-permittivity superstrates can be located above the antennas to improve the impedance properties, but they support the propagation of surface waves which reduce the efficiency. Here we propose the use of artificial dielectric (AD) superstrates above the antennas to improve significantly their performance. Because of their anisotropy, AD slabs do not support surface waves, thus enabling high-efficiency designs. To clarify the concept, we investigate the properties of a simple dipole antenna on chip in terms of impedance and efficiency. Full-wave simulations predict efficiency up to 87% with the presence of the AD.**

***Index Terms*—artificial dielectric, integrated antenna, on-chip antenna.**

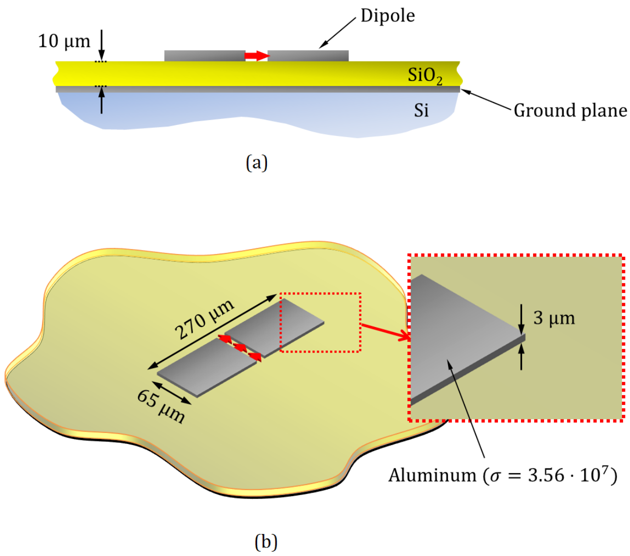

Fig. 1. Resonant dipole antenna on chip with dimensions and material description: (a) side view, (b) three-dimensional prospective view.

I. Introduction

Several of today's radar and wireless communication applications are shifting their operation to higher frequency to fulfill more demanding requirements on resolution, compactness and data rates. For this reason, there is a growing need to develop low-cost and efficient integrated circuit transceivers working in the low terahertz (THz) frequency range. While the cutoff frequency of CMOS transistors continues to increase so that sufficient power can be generated on CMOS chips at THz frequencies, the main limitation remains the poor performance of on-chip antennas, which are responsible of extracting the power from the chip through radiation.

On-chip antennas are intrinsically inefficient. A typical layer stack of a silicon chip is shown in Fig. 1(a) and consists of a thin layer of silicon dioxide (SiO_2), about 10 μm thick, on which the antenna is situated (e.g., a planar dipole antenna). A metal ground plane separates the SiO_2 slab from the silicon (Si) substrate, to shield the antenna from the highly lossy silicon.

When a dipole antenna is located at a small electrical distance from a metal plane, the electric currents on the dipole arms tend to cancel out with the image currents and the antenna can be matched only over an extremely narrow bandwidth. A solution to mitigate this problem was proposed in [1]: by including a superstrate above the chip, the radiated power tends to be coupled directly in such material, mitigating the negative impact of the proximity to the ground plane. However, dielectric slabs have the disadvantage to support the propagation of surface waves, i.e. the power remains trapped within the slab rather than being radiated, with consequent reduction of efficiency.

In this work, we propose to exploit artificial dielectric layers (ADLs) to realize the superstrate in place of real homogeneous dielectrics [2]. The ADLs are obtained by embedding a cascade of planar layers made of printed metal patches within a host material, to realize an equivalent anisotropic medium [3]. The effective electric parameters can be engineered by varying the size of the metal patches and their spatial density. Unlike real dielectrics, the ADLs enable high-efficiency radiation because they can synthesize very high equivalent permittivities (e.g. $\varepsilon_{r,\text{eff}} > 30$) and at the same time they do not support surface waves. The use of ADLs in combination of on-chip arrays of connected dipoles located in the close vicinity of a ground plane was shown in [4]. Here, we further analyze the beneficial property of ADLs by investigating the performance enhancement of a single resonant antenna in terms of bandwidth and efficiency.

To clarify the advantages of the ADLs we compare, by means of simulations, three cases: (1) an on-chip dipole antenna alone, (2) a dipole with a dielectric superstrate and (3) a dipole with an ADL superstrate. All the three antennas are designed to operate at a frequency around 280 GHz.

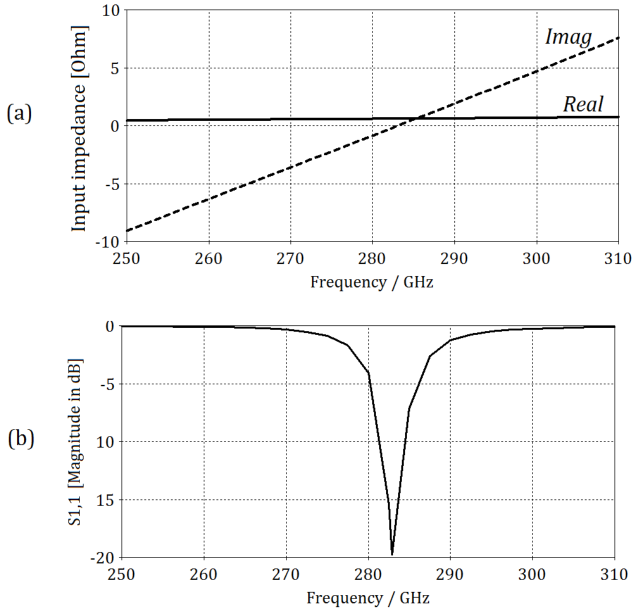

Fig. 2. (a) Input impedance and (b) reflection coefficient, normalized to 0.16 Ω, of the dipole antenna depicted in Fig. 1.

Simulations show that a maximum efficiency of 87% can be achieved by exploiting ADLs.

II. On-Chip Dipole Antenna

To highlight the limits of on-chip antennas, we first analyze a simple example consisting of a planar dipole, as shown in Fig. 1. The dipole is 270 μm long, 65 μm wide and fed at the center with a 10 μm delta-gap. The dipole thickness is assumed to be 3μm and the metal is Aluminum, with conductivity $\sigma = 3.56 \cdot 10^7$ S/m. The antenna is on a grounded slab of SiO_2 slab, with relative permittivity $\varepsilon_r = 4$ and thickness 10 μm. The dimensions of the dipole have been selected to resonate at about 280 GHz.

A CST [5] simulation of the dipole has been performed and the results are shown in Fig. 2. The input impedance in Fig. 2(a) exhibits a very low radiation resistance $< 1\ \Omega$, which would make the feeding network impractical. Also, the imaginary part varies rapidly with the frequency. Consequently, such an antenna can only be matched over an extremely narrow band of about 1%, as shown in Fig. 2(b). Moreover, since the antenna is very close to the ground plane, high electric currents are present on the dipole arms, which lead to rather high Ohmic losses (calculated to be 4.4 dB at 283 GHz).

III. Real Dielectric Superstrate

A solution to improve the performance of on-chip antennas was proposed in [1] and consists of including an electrically dense material (superstrate) above the chip. When the antenna is loaded with a high permittivity slab, it tends to radiate predominantly in the direction of such material. For example, Fig. 3 shows a similar antenna structure, with a low-loss high-resistivity silicon slabs situated at 5 μm distance from the top

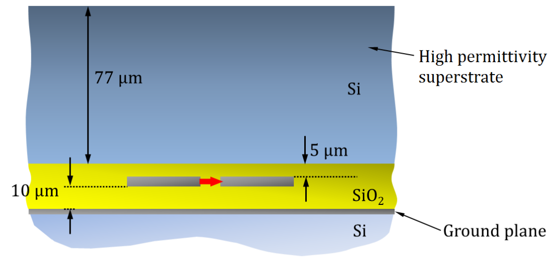

Fig. 3. Resonant dipole antenna on chip loaded with a dielectric superstrate.

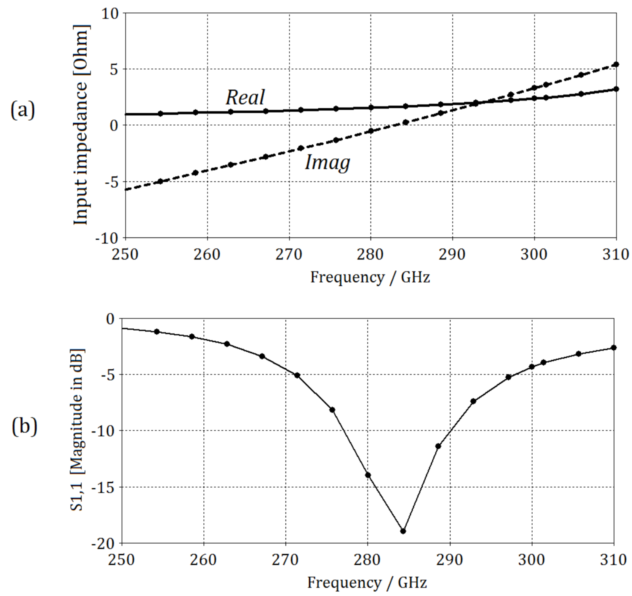

Fig. 4. (a) Input impedance and (b) reflection coefficient, normalized to 2 Ω, of the dipole antenna depicted in Fig. 3.

of the dipole. The slab is characterized by thickness of 77 μm and relative dielectric constant $\varepsilon_r = 11.9$. The impedance and reflection coefficient for this configuration are presented in Fig. 4. It can be noted that higher radiation resistance is achieved in this case ($\approx 2\ \Omega$) compared to the isolated dipole, and also wider bandwidth can be achieved (5%). The simulated Ohmic losses are also lower than the previous example, about 0.6 dB at 283 GHz. However, the high density of the superstrate causes strong reflections at its top surface, resulting in a large portion of the power to be lost in surface waves, rather than being radiated. The surface wave losses are calculated to be 2.3 dB.

IV. Artificial Dielectric Superstrate

As a final example, we consider a similar dipole antenna radiating in the presence of an ADL superstrate. The ADL slab is composed of 7 metal layers of Aluminum separated by 5 μm of SiO_2, with a total height of 35 μm. The fabrication of such ADLs can be performed with a CMOS back-end compatible integrated circuit process, as demonstrated in [2].

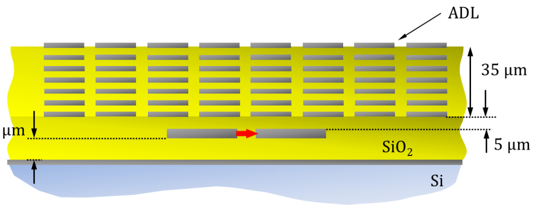

Fig. 5. Resonant dipole antenna on chip loaded with artificial dielectric layers.

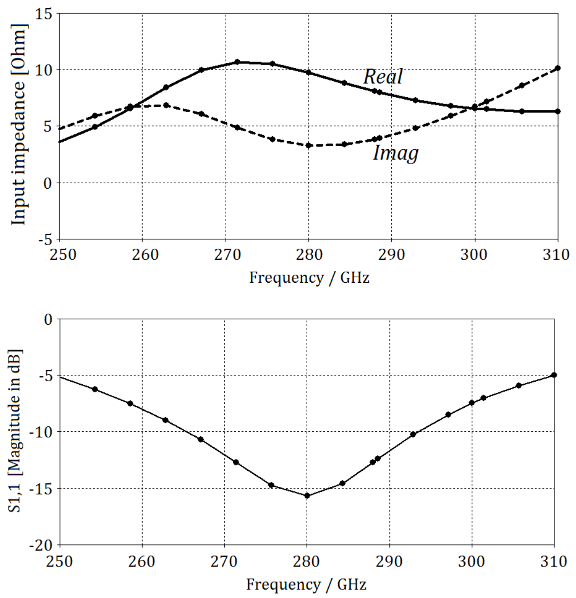

Fig. 6. (a) Input impedance and (b) reflection coefficient, normalized to 10 Ω, of the dipole antenna depicted in Fig. 5.

The dimensions of the patches are the same as in [2] and allow to synthesize an equivalent permittivity of $\varepsilon_r = 32$, for plane waves propagating normal to the stratification.

The simulated performance is shown in Fig. 6. The bandwidth is greatly improved (about 10%) and the real part of the input impedance is now about 10Ω. Moreover simulations show an total Ohmic loss of 0.6 dB and negligible surface wave losses. It is known that ADL yield very low Ohmic losses because of the electrically small dimensions of the metal patches, which support very low electric current. Also, due to its anisotropy, the ADLs synthesize a slab with very high permittivity for rays that travel normal to the stratification, but low effective permittivity for angles tending to grazing. Thus total internal reflection at the interface between ADL and air hardly occurs, with very low power being launched into surface waves [6].

The performance comparison is summarized in Table I.

TABLE I
PERFORMANCE COMPARISON OF THE THREE ANTENNAS AT 283GHZ

	Input resistance	Bandwidth	Efficiency
Dipole alone	0.16 Ω	1%	36%
With Si superstrate	2 Ω	5%	51%
With ADLs	10 Ω	10%	87%

V. CONCLUSION

A concept to enhance the efficiency and the bandwidth of on-chip antennas was presented. This consists in placing ADL superstrates above the on-chip antenna. The ADL can be used as an add-on component that can be glued on the chip without requirements on the alignment. As an example, a simple resonant dipole was selected as the radiator and its performance were investigated by means of full-wave simulations. The predicted performance indicated that a bandwidth of 10%, maximum total efficiency of 87% and maximum gain of 6.8 dBi is achieved by the dipole with the proposed concept, at a frequency of 280 GHz.

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