A True Rail-to-Rail Input & Output Amplifier

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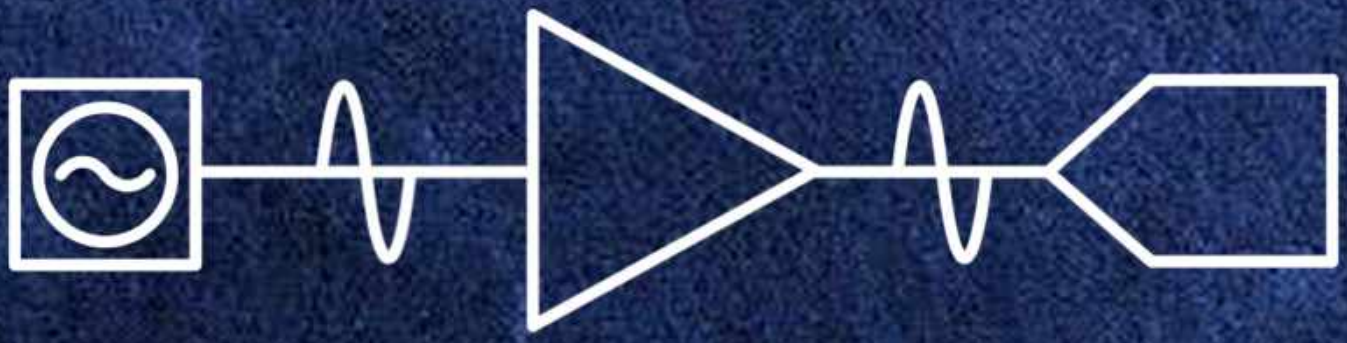

TU Delft

A True Rail-to-Rail Input & Output Amplifier

by

S. A. Khandelwal

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Abstract

Operational amplifiers are basic building blocks of an analog system. As a system is only as good as its building blocks. There exists a constant need for developing a high-performance amplifier. Especially if they are configured as a buffer for analog front-end applications, as the system performance is highly dependent on the quality of input signal. Hence, they are critical for signal conditioning.

This thesis presents a unity-gain stable operational amplifier for an ADC front-end application. The op-amp focuses on delivering high linearity with low noise and offset while driving a switched capacitor load. To accomplish this the op-amp employs Current Spillover, Chopping and Gain-Boosting techniques. The op-amp achieves THD of -108 dB at 10kHz, offset of 2.7μV and input noise density of 19.3 nV/$\sqrt{Hz}$ while consuming 504μW; resulting in a NEF of 12.28. The op-amp is fabricated in 0.16μm CMOS technology and occupies 0.1mm^2 area.

Keywords: Rail-to-Rail, Buffer, Low Noise, Low Offset, Low Distortion, Gain Boosting, Chopping.

Acknowledgements

Pursuing a master's was just an idea a couple of years ago and now, I'm finally concluding it. Last year couldn't have been more educative and fulfilling. The work carried out in this thesis wouldn't have been possible without the assistance and advice of numerous people. I would like to take a moment to acknowledge them all.

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S. A. Khandelwal
Eindhoven, September 2019

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1 Introduction

Our surroundings consist of an ocean of signals, and often they are in the analog domain. Over the years, several integrated circuits (IC) have been developed to sense, condition and process these signals. These ICs cover a wide spectrum of analog electronics, from sensors to amplifiers to analog-to-digital converters (ADC). Moreover, they are tailored for application and differ in specifications and input-output requirements. This makes it difficult to directly couple these individual blocks together. For example, a sensor may not have sufficient drive capability and/or common-mode voltage level to meet the input requirements of the ADC. This makes it difficult to couple these individual blocks together directly.

A buffer is a unity-gain amplifier with high impedance input and low impedance output. Its functionality is to provide sufficient drive capability to pass a signal to a succeeding stage without deteriorating it's quality. A buffer can be implemented in either the voltage domain or the current domain. In the voltage domain, it provides sufficient current to establish the input voltage across the load. Whereas, in the current domain it does the exact opposite, by providing enough voltage to keep input and output currents the same. Due to these characteristics, a buffer is a critical link between various blocks.

1.1. Motivation

In analog circuits, there is always a trade-off between noise, speed, and power, hence the specification of buffer changes with the application. The main application of this design is as a front-end buffer for ADCs. Since the ADC's performance is highly dependent on the quality of its input signal, this put a stringent requirement on the performance of the buffer. The target specifications are set by evaluating the input requirements of the ADC while taking the input signal bandwidth into account. The buffer is designed to drive a zoom ADC for audio applications [2]. This ADC has a switched capacitor network input, which means that the buffer must be able to deliver large current spikes. The specifications of the buffer must also be maintained over the audio bandwidth (20Hz – 20 kHz). This means that the buffer can also be used in other low frequency applications, such as the readout of sensor and biomedical signals.

In such applications, the signal swing can range from 1 μV to 1 V. This translates into a dynamic range (DR) of more than 110 dB. Since the input signal should not be compro-

mised by the buffer, high linearity is also required. Furthermore, low noise and offset performance is required to handle small signals. In many applications, the input signal may swing quite close to the supply rails to maximize the signal-to-noise ratio (SNR). To handle such signals, the buffer should either have a rail-to-rail input range or a non-rail-to-rail range with a supply voltage that exceeds the signal swing. Having a supply that exceeds the input signal swing often requires the use of special high voltage processes and results in a higher power consumption. Hence, having a rail-to-rail input stage is a more attractive alternative. Similarly, the buffer should have a rail-to-rail output stage, which should also be capable of driving a switched capacitor load. The specified load is switching at 2.5 MHz with a 50% duty cycle. Lastly, the buffer should also be power and area efficient. The target specification of the design are listed in Table 1.1.

Table 1.1: Target specification of the design

Parameters		**Target**	**Unit**
Technology		0.16	μm
Area		$\leq$ 0.1	mm^2
Input range		Rail-to-Rail	
Output range		Rail-to-Rail	
V_{dd}	Positive Supply	1.8	V
V_{os}	Offset	50	μV
e_n	Input noise density	14	nV/$\sqrt{Hz}$
THD	Total harmonic distortion	-110	dB
C_{Load}	Load capacitor	15	pF
f_s	Switching frequency	2.5	MHz
I_Q	Quiescent Current	$\leq$ 250	μA

1.2. Thesis Organization

The thesis consist of 5 chapters. A summary of each chapter is given below:

Chapter 2 provides an introduction to rail-to-rail amplifiers and addresses common issues associated with them. Different architectures and circuit techniques are discussed to mitigate these limitations and achieve the target specifications. Additionally, an overview of the various source of noise, offset and non-linearity is also presented.

Chapter 3 presents a detailed description of the circuit design and layout of the proposed buffer. Furthermore, different trade-offs and design choices are discussed. The chapter concludes with the simulation results.

Chapter 4 focuses on characterizing the buffer's performance. Measurement setup and results are presented. In the end, a performance comparison is carried out between the buffer and other amplifiers for a similar application.

Chapter 5 concludes the thesis and proposes some topics for future work.

2

Rail-to-Rail Amplifiers

In this chapter, we briefly review the basic architectures used in the input and output stages of rail-to-rail amplifiers, and compare their noise, offset, and linearity.

2.1. Input Stage

The purpose of the input stage is to process the differential input signal while rejecting common-mode voltages. An input stage will only adequately amplify differential signals that fall within its input-common mode range (ICMR). Outside this range, its ability to reject common-mode signals will deteriorate. In the target application, a rail-to-rail ICMR is required, thus requiring a rail-to-rail input stage.

The simplest way to realize a rail-to-rail (RTR) input stage is to place a PMOS and an NMOS differential pair in parallel with each other as shown in Fig. 2.1. The ICMR of the NMOS differential pair extends above the positive rails, while that of the PMOS pair extends below negative rail. To ensure that the ICMR of the PMOS and NMOS differential pairs overlap near $V_{dd}/2$ (Fig. 2.2a), the supply voltage (V_{dd}) must fulfil the following criterion [3],

$$V_{dd} \geq 4V_{dsat} + V_{thn} + V_{thp} \tag{2.1}$$

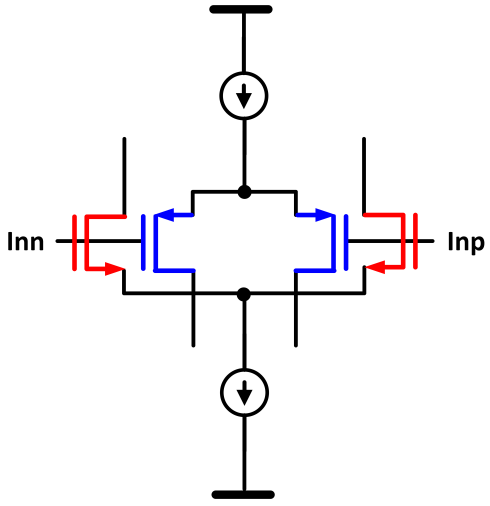
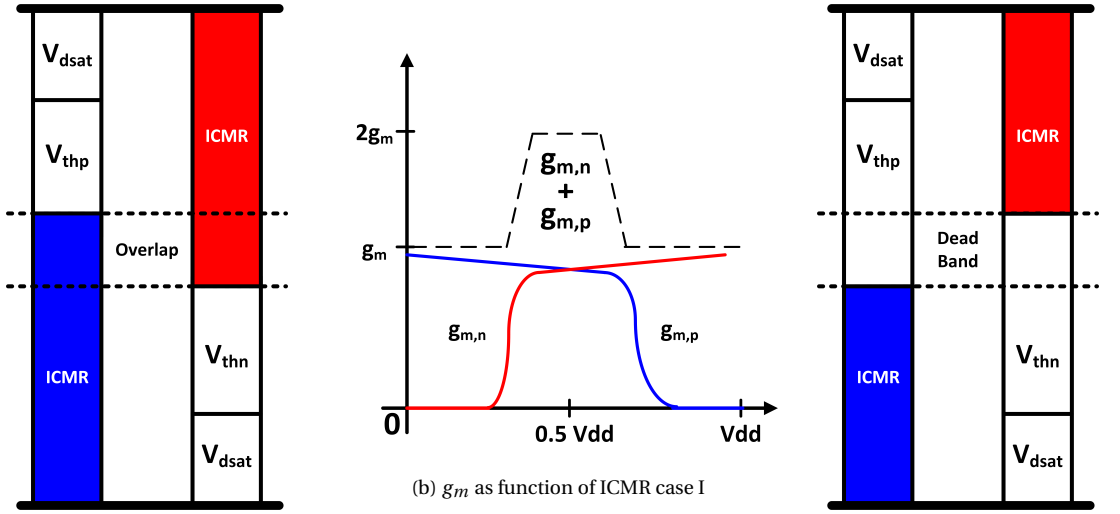


Figure 2.1: RTR input stage

where V_{dsat} is the saturation voltage, V_{thn} and V_{thp} are the threshold voltages of the PMOS and NMOS transistors respectively. In the overlap region, both differential pairs are active and so the circuit provides twice the designed transconductance (g_m) (Fig. 2.2b). If V_{dd} does not satisfy equation 2.1, however, then there will be an ICMR dead band in which both differential pairs are turned off (Fig. 2.2c). The second scenario mainly occurs in low voltage design. Since this buffer is designed for a 1.8 V supply, it falls into the first category.



(a) ICMR as a function of V_{dd} case I

(b) g_m as function of ICMR case I

(c) ICMR as a function of V_{dd} case II

Figure 2.2: Rail-to-Rail output stage configurations

When both input pairs are active, g_m of the amplifier doubles, so does its unity-gain frequency. This degrades the phase-margin of the system as the non-dominant pole comes two times closer to the dominant pole. In the absence of sufficient phase-margin, the amplifier will start ringing and require more settling time. But more importantly, this limits the design of an optimized frequency compensation for the system [4]. Additionally, the linearity of the system is also affected, as the differential loopgain will be a function of the input common-mode voltage. Therefore, it is essential to implement a circuit that regulates g_m when the input common-mode voltage (V_{incm}) of the amplifier changes.

There are multiple g_m regulation circuits available in literature: complementary current circuit to keep sum of tail currents constant [5] [6], a circuit to keep the square root sum of tail currents constant [7], switching circuits to change the value of the tail current [8] [9], minimum / maximum current selection circuits [10], circuits to regulate the gate-to-source voltage of the input pair using electronic zener diodes [11], DC level shifting circuits [12] and, the current spillover g_m control technique [13]. A comparison between these circuits is shown in Table 2.1. This design employs the current Spillover g_m control technique [13], because of its fast switching between the NMOS and the PMOS input pairs, minimal variation of g_m over ICMR and its simple implementation.

Table 2.1: Comparison of different g_m control circuits

Principal	$\Delta\ g_m$	Comment	Limitation
$I_P + I_N$ = constant [5]	≤ 5%	Input pair biased in W.I	As the current regulation involves mirroring it not suitable for high speed application.
	40%	Input pair biased in S.I	
$\sqrt{I_P} + \sqrt{I_N}$ = constant [7]	6%	Works on MOS quadratic characteristic	Suitable for input pair operating in S.I.
4x tail current [8]	15%	Systematic variation	Theoretical limitation of 15% g_m variation
Min /Max selection [10]	5%	Input pair biased in S.I	Complex circuit implementation
	20%	Input pair biased in W.I	
Electronic zener [11]	8%		Suitable for input pair operating in S.I.
Level shift [12]	4%		Sensitive to V_{th} and power supply variation
Current spillover [13]	≤ 2%	Input pair biased in W.I	Sensitive to mismatch

2.1.1. Current Spillover g_m Control

The Current spillover (CSO) technique is a robust way to obtain rail-to-rail ICMR. The corresponding circuit is shown in Fig. 2.3 [13]. As V_{incm} swings rail-to-rail, the control transistors M_{SW1} - M_{SW2} divert the unnecessary current from the complimentary input pair to the supply rails. Since the control transistor divert the entire tail current ($I_{tail} = 2I_{d,M1,M2}$) to the supply, it is twice the size of the input transistors. This current regulation is achieved by two trans-linear loops, whose operation is described by equations 2.2 and 2.3 [4].

$$V_{gs,M1} + V_{gs,M3} = V_{gs,M_{SW1}} + V_{gs,M_{SW2}} \tag{2.2}$$

$$V_{gs,M2} + V_{gs,M4} = V_{gs,M_{SW1}} + V_{gs,M_{SW2}} \tag{2.3}$$

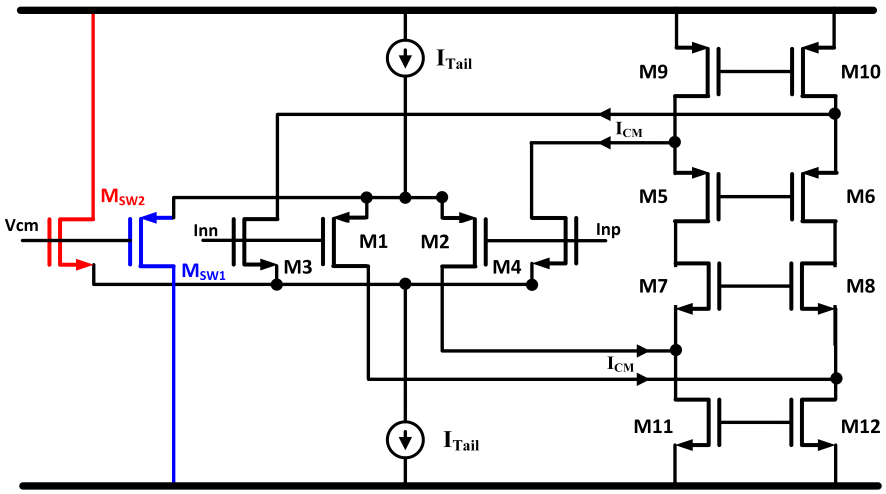


Figure 2.3: Current spillover g_m control circuit

When the input common-mode is in the middle i.e., $V_{incm} = V_{dd}/2$, then the drain current (I_d) is given by equations 2.4 and 2.5 [4]. Whereas, when the input common-mode is at extremes, either $I_{d,M1,M2} = I_{tail}$ and $I_{d,M3,M4} = 0$, or $I_{d,M3,M4} = I_{tail}$ and $I_{d,M1,M2} = 0$. Then, the ICMR is given by equation 2.6 [4].

$$I_{d,M1} = I_{d,M2} = I_{d,M3} = I_{d,M4} = I_{tail}/2 \tag{2.4}$$

$$I_{d,M_{SW1}} = I_{d,M_{SW2}} = I_{tail} \tag{2.5}$$

$$I_{d,M1,M2} + I_{d,M3,M4} = I_{tail} \tag{2.6}$$

The total transconductance $g_{m,Total}$ over the ICMR is also dependent on the operating region of the complementary input pairs. When the input pairs are operating in weak inversion, their g_m is a linear function of their drain current. But, when operating in the strong inversion region, their g_m is a quadratic function of their drain current. Therefore, the total transconductance $g_{m,Total}$ in weak inversion and strong inversion can be derived from equation 2.6, and is given by equation 2.7 and 2.8 respectively [4]. It can be seen that due to its quadratic dependency the $g_{m,Total}$ in strong inversion region varies by 40% in the middle of the ICMR. In low bandwidth applications, it is therefore beneficial to bias the complementary input pairs in weak inversion.

$$g_{m,Total,WI} = g_{m,M1,M2} + g_{m,M3,M4} \tag{2.7}$$

$$g_{m,Total,SI} = 2\sqrt{2}\,(g_{m,M1,M2} + g_{m,M3,M4}) \tag{2.8}$$

Since the CSO circuit doesn't involve a mirror current control and/or complex current regulation loop, it switches between input pairs faster than other g_m control circuits [5] [9] [10]. This helps in tracking signal with fast common-mode swing. However, it also consumes two times more tail current than other g_m control circuits. The ICMR range of the rail-to-rail input stage is calculated from equation 2.9, to be V_{dd} + 200 mV and V_{ss} − 200 mV. One drawback (typical of most rail-to-rail input stages) is that as V_{incm} changes, the common-mode output current (I_{CM}) varies from 0 to I_{tail} for each input pair. As this current is sourced from the summing stage, it may cause a V_{incm} dependent offset.

$$V_{ss} - V_{dsat,M11} + V_{thp} \leq V_{incm} \leq V_{dd} - V_{dsat,M9} + V_{thn} \tag{2.9}$$

To mitigate this issue, the CSO circuit can be adapted as shown in Fig. 2.4 [4]. The control transistors M_{SW1} and M_{SW2} are split into four switches M_{SW1a}, M_{SW1b}, M_{SW2a} and M_{SW2b}. The size of the new switching transistors are the same as that of the input transistor. The drains of the switching transistors are now connected to the summing circuit. The operating principal remains the same: the switching transistors spill the current into the summing circuit in place of the supply rails. Thus, the common-mode output current from the current summing circuit is always constant irrespective of V_{incm}.

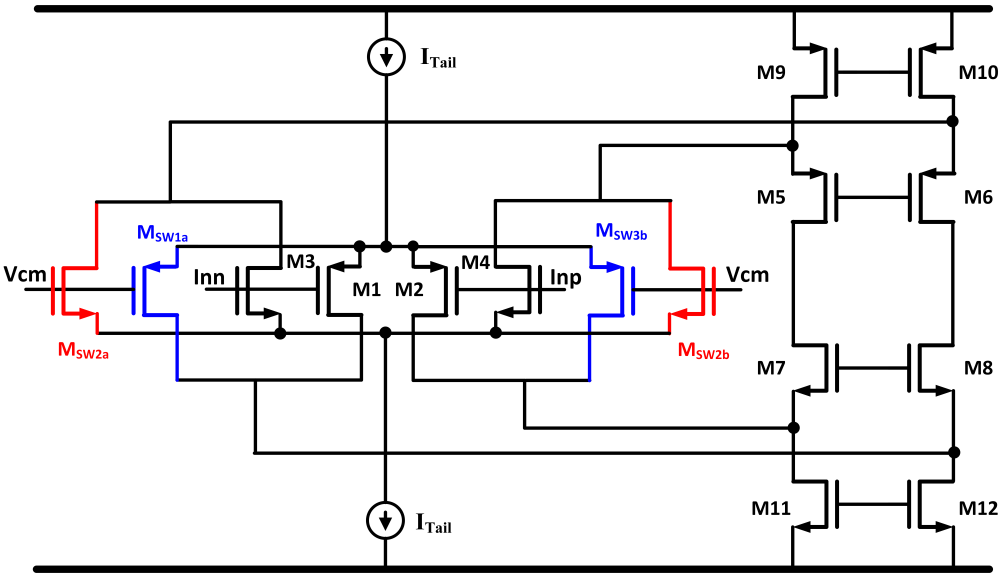


Figure 2.4: Modified current spillover g_m control circuit.

2.1.2. Folded Cascode Input stage

Since the input stage consist of a folded cascode structure with complementary input pair, it becomes essential to discuss its operation. A conventional folded cascode amplifier (FCA) is shown in Fig. 2.5. It consists of a PMOS input pair M1a-M1b, the cascode transistors M3-M6 and the current sources M7-M9. The FCA is a suitable input stage for this design because of its high ICMR and output swing given by equation 2.10 and 2.11 respectively [14].

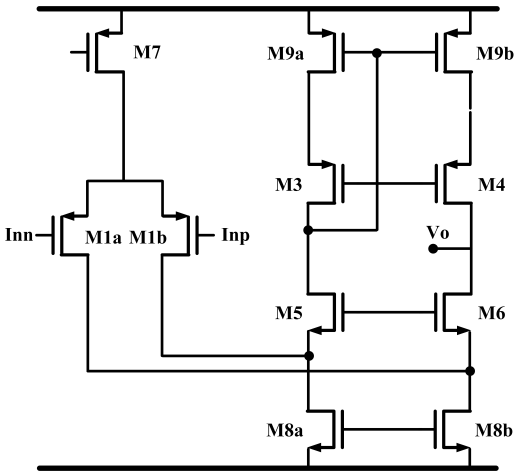


Figure 2.5: Folded cacode input stage

$$V_{ss} - V_{dsat,M8} + V_{thp} < V_{incm} < V_{dd} - V_{dsat,M7} - V_{gs,1} \tag{2.10}$$

$$V_{out,pp} = V_{dd} - (V_{ov,M9b} + V_{ov,M4} + V_{ov,M6} + V_{ov,M8b}) \tag{2.11}$$

where V_{dsat}, V_{ov} and V_{gs} denote the saturation voltage, overdrive voltage, and gate-to-source voltage of various transistors, respectively. The small-signal gain of a FCA is A =

$G_m R_{out}$, where G_m is the transconductance and R_{out} output impedance of FCA. of FCA. The G_m is equivalent to the transconductance of a single input transistor i.e., g_{m1}. Whereas, the R_{out} is given by equation 2.12 [14]. Therefore, the small-signal gain of an FCA is given by equation 2.13 [14]. It can be observed that higher gain can be obtained from FCA by optimizing the g_m and r_o of the input pair, cascode transistors and current sources.

$$R_{out} = (g_{m,M4} + g_{mb,M4}) r_{o4} r_{o9} \,||\, [(g_{m,M6} + g_{mb,M6})(r_{o1} \,||\, r_{o8}) r_{o6}] \tag{2.12}$$

$$A \approx g_{M1}[(g_{m,M4} + g_{mb,M4}) r_{o4} r_{o9} \,||\, [(g_{m,M6} + g_{mb,M6})(r_{o1} || r_{o8}) r_{o6}]] \tag{2.13}$$

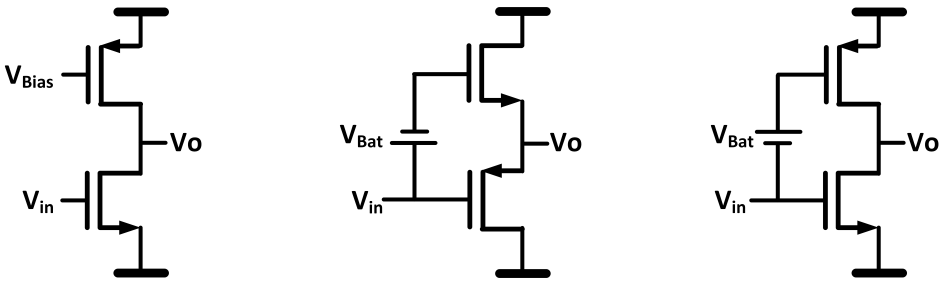
Sometimes, it is preferred to implement the mirroring node at the NMOS side as it offers a higher frequency response. This is due to the lower total gate capacitance ($C_g = C_{gd} + C_{gs} + C_{gb}$) of the NMOS current source transistors. However, to deliver a symmetrical current equal to two times the current of the input transistors, the PMOS current sources must carry two times the tail current. Hence, the NMOS sources must carry three times the value of tail thereby making the influence of noise and offset of the NMOS current sources three times larger. Thus, increasing the noise efficiency factor (NEF) of FCA. This additional noise can be reduced by increasing the overdrive voltages of the current sources [4].

2.2. Output stages

The purpose of the output stage is to provide sufficient current to the load impedance to maintain the desired voltage at the output. There are several key attributes of an output stage such as high linearity, the ability to supply positive and negative output currents and, support a rail-to-rail output swing.

In literature [4], multiple classes of output stages available, each with their own pros and cons. For example, a Class-A output stage has high linearity but poor efficiency, whereas, a Class-C output stage is superior in power efficiency but is not suitable for low distortion performance. As low distortion is one of the main specifications of this design, henceforth only Class-A and Class-AB output stages are considered.

Rail-to-Rail output swing can be achieved by using three the different configurations as shown in Fig. 2.6. The first is a Class-A common-source (CS) output stage (2.6a), the second is a Class-AB common-drain (CD) output stage(2.6b), and the third is a Class-AB common-source output stage (2.6c). In a Class-A CS stage, the maximum bias current is fixed by the current source transistor, it lacks the ability to provide dynamic current. The capability to provide dynamic current to the load is important since the buffer is required to drive a switched capacitor load. The Class-AB CD configuration can provide dynamic output current, but its output swing is limited to V_{dd} - V_{gs} and V_{ss} + V_{gs}. The Class-AB CS stage have larger output swing limited to V_{dd}-V_{dsat} and V_{ss}+V_{dsat}. Since $V_{dsat} < V_{gs}$, the output can swing to within 50 mV of the rails. Therefore, a Class-AB common-source configuration is selected for the design of the rail-to-rail output stage.



(a) Class-A CS stage (b) Class-AB CD stage (c) Class-AB CS stage

Figure 2.6: Rail-to-Rail output stage configurations

2.3. Design for Linearity

In operational amplifiers both the input and output stages contribute towards non-linear distortion. The cause of distortion in the input stage is either due to the input pair being close to the slewing limit and/or the complementary input pairs are not being matched. Whereas, the output stage suffers from the cross-over distortion of the Class-AB stage. Of the two stages, the output stage is dominant cause of distortion since the signal swing is largest at the output.

To understand the origin of cross-over distortion in the second stage, let us look at a conventional Class B output stage shown in Fig. 2.7. The circuit provides excellent power efficiency due to the absence of any quiescent current. However, when the input is in the middle i.e., $V_{thp} < V_{in} < V_{thn}$, both the output transistors are off. This leads to high distortion at the output and is called cross-over distortion.

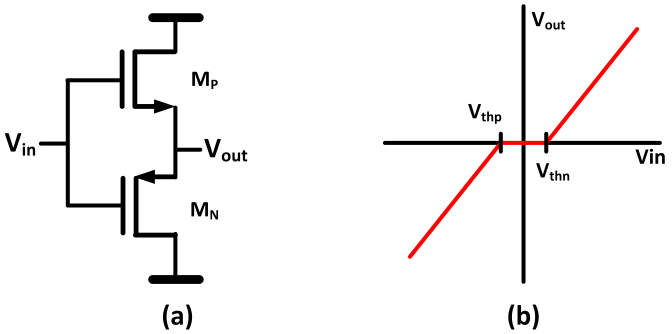


Figure 2.7: Cross-over distortion in output stage, (a) Class B output stage and (b) input-output characteristic

The cross-over distortion in Class-AB output stage can be reduced in two ways. Firstly, the output transistors can be biased at a quiescent current (I_Q). The value of I_Q can be determined such that it prevents the output transistors from turning off while maintaining good power efficiency. Secondly, it can be achieved by matching the g_m of the PMOS and the NMOS output transistors, as the difference in current gain between the output transistors also give rise to distortion. Additionally, the distortion of the output stage is also suppressed by the loop-gain of the amplifier. Furthermore, Miller compensation provides better linearity than some other frequency compensation schemes, e.g. parallel compensation. This is because the Miller capacitor establishes an extra internal feedback loop across the output

transistor [4].

In a rail-to-rail input stage, the second-order distortion can be lowered by improving the matching of the complementary input pair. This can be explained by noting that an fully differential signal only consists of odd harmonics, and that the signals in the amplifier remains fully differential until the current summing stage (Fig. 2.4). Therefore, any mismatch between the complementary pair increases the second-order distortion of the current summing stage. The slewing limitation in the input stage occurs because the input transistors deviate from linear operation when the input signal is in the vicinity of the minimum and maximum extremes of the input range. This causes third-order distortion at the output which can be referred to the input as an additional series voltage along with the differential signal. A higher unity-gain frequency can mitigate the distortion from the slewing limit. Therefore, the input pair must be either biased in strong inversion or must have sufficient high unity-gain frequency [4].

2.4. Design for Offset

To identify the dominant sources of offset in an amplifier, let us consider the FCA shown in Fig. 2.8. The offset voltage of the FCA can be determined from equation 2.14 [15].

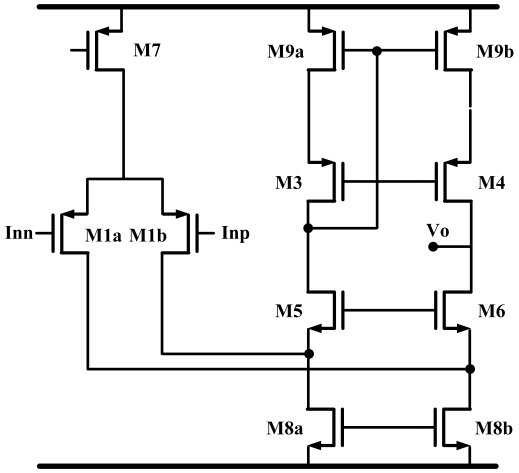


Figure 2.8: Folded cacode input stage

$$V_{os} = \Delta V_{th,1} + \frac{g_{m,8}}{g_{m,1}}\Delta V_{th,8} + \frac{g_{m,9}}{g_{m,1}}\Delta V_{th,9} + \frac{1}{g_{m,1}}\left(\frac{\Delta\beta_1}{\beta_1} + 2\frac{\Delta\beta_9}{\beta_9} + \frac{\Delta\beta_8}{\beta_8}\right) \tag{2.14}$$

where $V_{th,x}$ is the threshold voltage of transistor Mx, β_x is the transconductance factor of transistor Mx and g_m, x is the transconductance of transistor Mx. Equation 2.14 can be modified for a rail-to-rail input stage, assuming the g_m from complimentary pair remains constant over ICMR i.e., $g_{m,1} + g_{m,2} = g_{m,in}$ = constant. The modified equation is given by:

$$V_{os} = \Delta V_{th,1} + \Delta V_{th,2} + \frac{g_{m,8}}{g_{m,in}}\Delta V_{th,8} + \frac{g_{m,9}}{g_{m,in}}\Delta V_{th,9} + \frac{1}{g_{m,in}}\left(\frac{\Delta\beta_1}{\beta_1} + 2\frac{\Delta\beta_9}{\beta_9} + \frac{\Delta\beta_8}{\beta_8}\right) \tag{2.15}$$

where $\Delta V_{th,1}$ and $\Delta V_{th,2}$ are threshold mismatch of the PMOS and the NMOS input pairs

respectively. It can be observed that the dominant sources of offset in the FCA are the input transistors and the current sources. To reduce the offset, the ratio of current source g_m to input pair g_m should be minimized. Additionally, increasing area of the transistor reduces the threshold mismatch [16], which further reduces the offset. By this approach offset as low as 1m can be achieved [17].

To achieve micro-volt levels of offset, dynamic offset cancellation techniques (DOC) are required such as chopping and auto-zeroing. The working principle together with a comparative analysis on both of these DOC techniques is presented in [1]. A summary of a comparative analysis is shown in Table 2.2 [1].

Table 2.2: Comparison between auto-zeroing and chopping DOC [1].

Parameter	Auto zeroing	Chopping
$1/f$ noise	+	+
Power-noise efficiency	-	+
Output ripple	+	-
Residual offset	+	++

While both chopping and auto-zeroing offer lower residual offset and $1/f$ noise, implementing auto-zeroing in the continuous-time domain requires two low-noise input stages [4]. This consumes more power as well as area. Therefore, the chopping DOC technique is used in this design.

2.5. Design for Noise

In CMOS technology, the input noise source of a transistor comprises of two components as shown by equation 2.16 [18]. The first component is thermal noise, which occurs due to the thermal agitation of charge carriers (electrons). Whereas, the second component is flicker noise also known as $1/f$ noise, which occurs due to interface defects at the poly-substrate interface.

$$v_n^2 = 4kT\frac{2}{3g_m}\Delta f + \frac{K_f}{C_{ox}^2 WL}\left(\frac{\Delta f}{f}\right) \tag{2.16}$$

where k is the Boltzmann's constant, T is temperature in Kelvin, Δf is bandwidth, C_{ox} is oxide capacitance per unit area, K_f is the flicker noise coefficient and WL is area of the transistor. In low bandwidth designs, flicker noise is more dominant than thermal noise. Since this buffer focuses on audio-bandwidth signals, it falls under medium bandwidth designs. However, flicker noise can still contribute significantly to the design's noise budget. As mentioned earlier, chopping also reduces the $1/f$ noise of the design. Thus, the design can be still made thermal noise limited. It is essential to analyze the design and effectively reduce its flicker and thermal noise to meet the target noise specifications. Let us consider the FCA in Fig. 2.8 again to investigate the dominant sources of noise in an amplifier. The input-referred thermal and flicker noise of FCA is given in equation 2.17 and 2.18 respectively [15].

$$v_{n,th}^2 = 4kT\frac{4}{3g_{m,1}}\left(1+\sqrt{2\frac{\mu_n}{\mu_p}\frac{W_9 L_1}{L_9 W_1}}+\sqrt{\frac{W_8 L_1}{L_8 W_1}}\right)\Delta f \tag{2.17}$$

$$v_{n,1/f}^2 = \frac{K_p}{C_{ox}^2 W_1 L_1}\left(1+2\frac{\mu_n}{\mu_p}\frac{K_n L_1^2}{K_p L_8^2}+\frac{L_1^2}{L_9^2}\right)\frac{\Delta f}{f} \tag{2.18}$$

In both the equations above, the first term expresses the noise contribution of the input pair and the second term represents the noise contribution of the current sources. It can be concluded that increasing the input pair transconductance $g_{m,1}$, the input pair width (W_1) and the current sources length (L_8 and L_9) will reduce the thermal noise. Whereas, increasing the transistor gate area ($W_1 L_1$) reduces flicker noise. Additionally, as mentioned in Table 2.2, chopping also reduces the $1/f$ noise by up-modulating it to chopping frequency [1]. These aspects are crucial design criteria to obtain the target noise specification of the design.

2.6. Block level Implementation

The final block level diagram of the design is shown in Fig. 2.9. The amplifier used for the buffer is a two-stage design. The first stage consists of a complementary differential pair that enables rail-to-rail ICMR. The second stage is a Class-AB output stage to provide high output current and rail-to-rail output swing. A g_m control circuit is incorporated into the first stage to provide a constant g_m over ICMR. Chopping is used to reduce offset and $1/f$ noise. Gain-boosting is integrated into the first stage to aid chopping functionality and is discussed in section 3.3.7. A complimentary clock generator is included in the design to provide a 50% duty cycle chopping clock. Lastly, the amplifier is Miller compensated as it improves linearity (section 2.3).

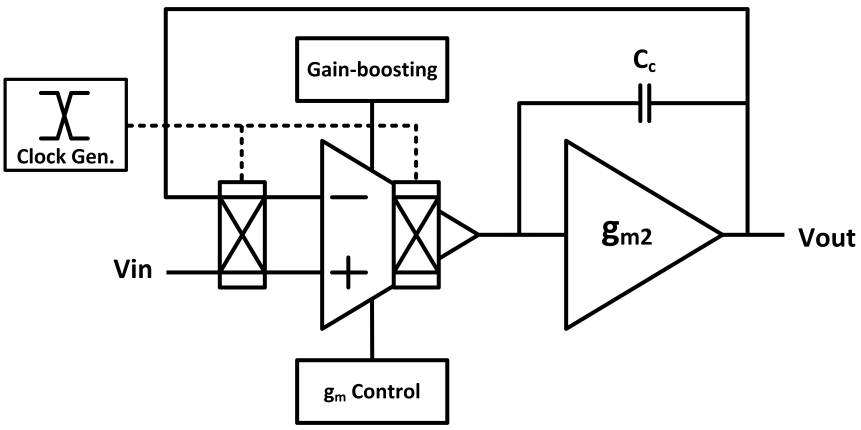


Figure 2.9: Block level implementation

3

Overall Design and Optimizations

In this chapter, the implementation of the rail-to-rail amplifier is presented in detail. The effectiveness of the architectures and circuit techniques introduced earlier are demonstrated with the help of simulations.

3.1. Trans conductance Requirement

In a general design flow, the first stage is designed for noise and settling performance whereas the subsequent stages are designed for bandwidth. As shown in the table 1.1, the target input noise density of the design is 14 nV/$\sqrt{Hz}$, which translates to a signal-to-noise ratio (SNR) of 110 dB. Therefore, the total integrated input-referred noise to achieve 110 dB of SNR can be calculated from equation 3.1 [19].

$$V_{n,rms} = \frac{V_{pp}}{2\sqrt{2}} * \frac{1}{10^{(\frac{SNR}{20})}} \tag{3.1}$$

where V_{pp} is peak-to-peak output swing and $V_{n,rms}$ is the total integrated noise. The required noise was calculated to be 2 μV_{rms}. Equation 3.2, gives an approximate transconductance (g_m) required for the input pair [19].

$$g_m = \sqrt{\frac{4kTB}{V_{n,rms}}} \tag{3.2}$$

where k is the Boltzmann's constant, B is bandwidth, and T is temperature in Kelvin. The required transconductance was calculated to be 100 μS. Since other transistors in the folded cascode structure also contribute noise, this value of g_m is not sufficient and needs to be over designed to meet noise specification.

To maximize the g_m of the input pairs, the current budget of the design is split between the input and output stage of the amplifier. Following this, the maximum available current, the maximum allowed overdrive voltage and the maximum attainable g_m can be determined for the input pairs.

The total current budget of the amplifier is 250 μA, of which 30 μA is reserved for biasing, gain-boosting amplifiers and clock generators. The remaining 220 μA is split between the two stages of the amplifier. For stability requirements discussed in section 3.2, the current is divided as 100 μA and 120 μA between the input and output stage respectively. The input stage current is further divided into the folded cascode branches and from section 3.3.2, the maximum attainable transconductance was calculated to be $g_m \approx 450$ μS.

3.2. Bandwidth Requirement

The bandwidth of the amplifier is governed by two important specifications. First being the switched-capacitor load driving capability. Since the switching frequency (f_s) of load is set at 2.5 MHz ($t_p = 400ns$) with 50% duty cycle, the amplifier should be able to attain 120 dB of settling in 200 ns as shown in Fig. 3.1. As settling goes 8.6 dB/τ, we require 14τ for 120 dB of settling. Therefore, the minimum required unity-gain frequency (f_{unity}) of the amplifier as calculated using equations 3.3 - 3.5 is 11 MHz [19].

$$n = \frac{120\ dB}{8.6\ dB} \approx 14 \tag{3.3}$$

$$\tau = \frac{1}{2nf_s} \approx 14ns \tag{3.4}$$

$$f_{unity} = \frac{1}{2\pi\tau} \approx 11MHz \tag{3.5}$$

Secondly, the linearity specification of the system also influences the bandwidth requirement of the amplifier. Since the suppression of amplifier's distortion at a given frequency is related to its loop-gain at that frequency (section 2.3). The required bandwidth to meet the switching frequency and linearity requirement was found to 18 MHz.

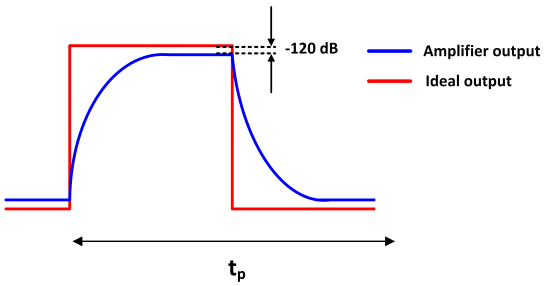


Figure 3.1: Settling requirement

As mentioned in section 3.1, the output stage consumes 120 μA of current. This is approximately 50% of the entire current budget. This power is primarily spent on making the amplifier unity-gain stable i.e., pushing the second dominant pole to four times the unity-gain frequency. By doing this we keep the phase margin of the amplifier above 60°. The unity-gain frequency is given by equation 3.6 [19]. Whereas, the location of the second dominant pole is determined by the equation 3.7 [19]. As the load capacitance (C_{load}) is fixed to 15 pF, the transconductance of the output stage defines the position of the second dominant pole. Thus, the higher the transconductance of the output transistors, higher the frequency

of the second dominant pole of the amplifier. In this design the second dominant pole is at $f_{2^{nd}pole} \approx 72$ MHz.

$$f_{unity} = \frac{g_{m,in}}{2\pi C_M} \tag{3.6}$$

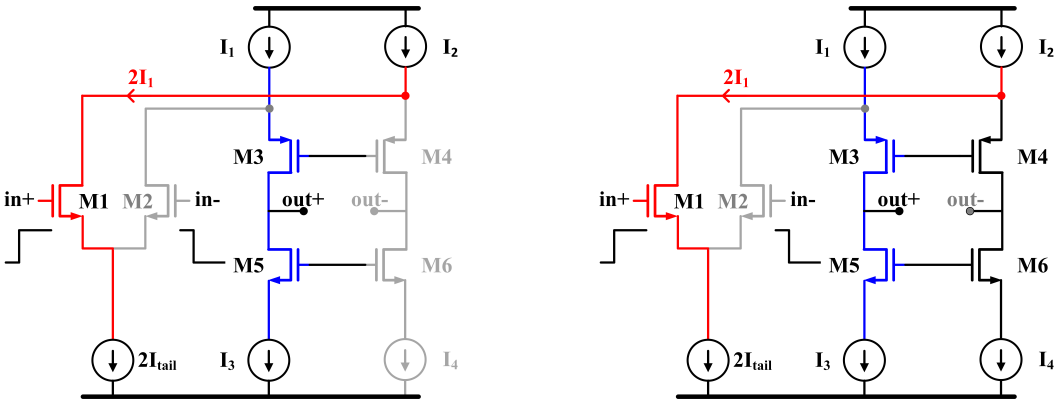
$$f_{2^{nd}pole} = \frac{g_{m,2^{nd}stage}}{2\pi C_{load}} \tag{3.7}$$

3.3. Rail-to-Rail Input Stage

The input stage should have large g_m and high open-loop gain in the audio-bandwidth to meet noise and linearity specification. The complementary input pair is designed to provide sufficient g_m for low input referred noise, whereas, the summing stage is designed to give large R_{out} for high open-loop gain.

3.3.1. Current Allocation

As mentioned in 3.1, the input stage consume approximately 100 μA of current. This current is divided between three sources, one input pair tail current source and two summing stage current sources. To understand the allocation of the current among these current sources, let us take an example. Figure 3.2 shows a FCA with NMOS input pair M1-M2 and cascode transistors M3-M6. A large differential voltage step is applied at the input of FCA. This would result in large differential current flow into the input pair. For instance, if the current $I_1 = I_2 < I_{Tail}$, then starvation of current in a cascode branch will be trigger slewing and in turn causing distortion (Fig. 3.2a). This situation can be circumvented if the current sources carry current $I_1 = I_2 > I_{Tail}$ as shown in Fig. 3.2b. Therefore, the the current division within the first stage of amplifier is $I_{Tail} = 30$ μA and $I_1 = I_2 = I_{cs} = 36$ μA.



(a) Case I: $I_1 = I_2 < 2I_{Tail}$

(b) Case II: $I_1 = I_2 > 2I_{Tail}$

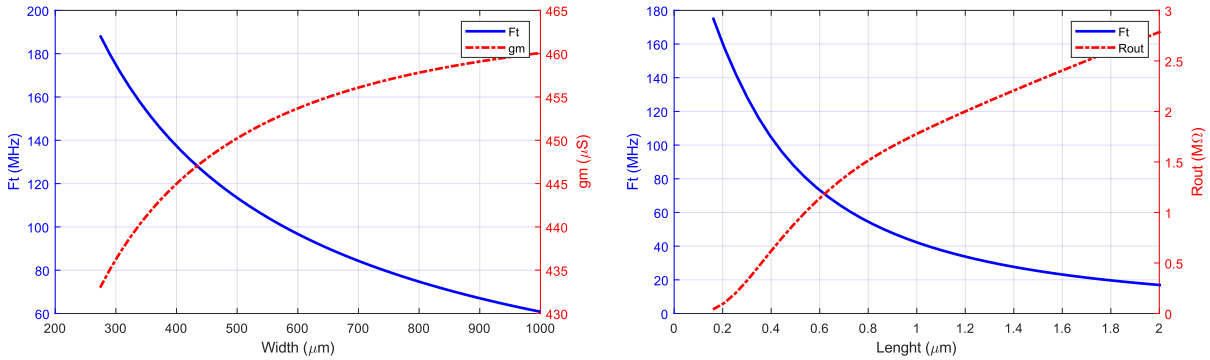
Figure 3.2: Effect of a transient step on different configurations of folded cascode

3.3.2. Complimentary Input Pairs

In section 2.1.1, it was established that the current spillover architecture provides better g_m regulation over ICMR when both of the input pairs are operating in weak inversion. Also, the maximum allowed drain current I_d for each input transistor was determined to be 15 μA. The maximum attainable g_m for this current is determined by the PMOS input pair because of their lower mobility. Figure 3.3a shows relation between g_m and width (W) of the

PMOS input transistor in weak inversion region for I_d of 15 μA and length 0.3 μm. It can be noticed that above a width of W $\approx$ 400 μm the value of g_m saturates. Thus, further increase in width doesn't affect value the g_m much. Therefore, the value of g_m was found to be approximately 450 μS.

Similarly, Fig. 3.3b shows the relationship between R_{out} and the length of the PMOS input transistor for a width of 400μm. It can be noticed that at minimum length the r_o of input transistor is quite low. Since the r_o of the input transistor is in parallel with with the r_o of current source (eq. 2.12), it is important to ensure the r_o of the input transistor does not limit the R_{out} of the summing stage. Hence, the length of the PMOS input transistors is increased to 0.3 μm to get an r_o of approximately 400 kΩ. Therefore, the sizing of the PMOS input pair was be determined to be W/L = 432/0.3 μm. It is important to note that increasing width as well as the length of the transistors lowers their transit frequency (f_t) making them slow.



(a) g_m vs W vs f_t characteristics

(b) R_{out} vs L vs f_t characteristics

Figure 3.3: PMOS input transistor characteristics

Since the NMOS transistors have higher carrier mobility, they have higher g_m and lower R_{out} compared to the PMOS transistors. Adopting a similar approach as above, the g_m of the NMOS input pair was matched with that of the PMOS pair and the size of NMOS input pair was calculated to be W/L = 120/0.6 μm. The overdrive voltages for the PMOS and the NMOS input pair was calculated to be V_{ov} $\approx$ -70 mV and V_{ov} $\approx$ -40 mV respectively. The Fig. 3.4 shows half of the complementary input differential pair, and their respective sizing is given in Table 3.1.

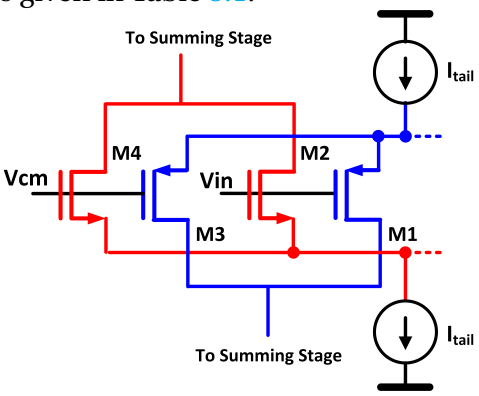


Figure 3.4: Rail-to-Rail input pair half circuit

Transistor	W (μm)	L (μm)	M
M1	13.5	0.3	32
M2	7.5	0.6	16
M3	13.5	0.3	32
M4	7.5	0.6	16
Parameter		Current (μA)	
I_{tail}		30	

Table 3.1: Parameters of Rail-to-Rail input pair transistors

3.3.3. Input pair Layout

An essential aspect of the complementary input pair with CSO g_m control circuit is the matching between the input transistors and their switches. Any mismatch between the four can directly affect the distortion performance of the amplifier (section 2.3). To reduce the mismatch between transistors, layout techniques such as the common-centroid layout scheme, drain-source sharing, and dummy transistors are used. In Fig. 3.5, the layout of the NMOS input pair is given, where A-B is the input pair and C-D are their respective switches.

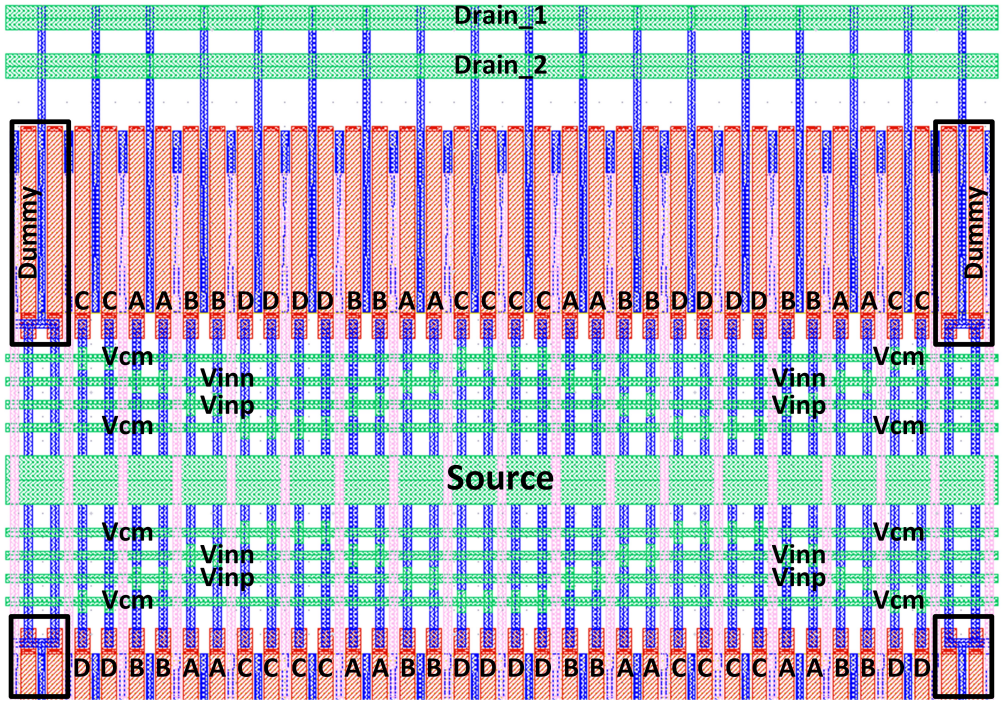


Figure 3.5: Half layout of NMOS differential pair and its switches

3.3.4. Current Summing Structure

The current summing structure of the first stage is shown in Fig. 3.6. The transistors M5-M6 and M12-M13 are current sources, M7-M11 are cascodes, and M14-M15 forms the floating battery source. To convert the differential input to a single-ended output, mirroring is done at node X. As discussed in section 2.1.2, mirroring at the NMOS side offers a higher frequency response due to lower total gate capacitance ($C_g = C_{gd} + C_{gs} + C_{gb}$) of the NMOS transistor. However, since the area (WxL) of the PMOS and the NMOS current sources are equal in this design, their total gate capacitance is also equal. Hence, mirroring at the NMOS side will increase the power, noise and offset of the design (sec.2.1.2). The location of the mirror pole can be approximated by equation 3.8, where C_g is equal to 0.8pF.

$$f_{Mirror\ pole} = \frac{g_{m,eff}}{2\pi(\ C_{g,M5} + C_{g,M5} + C_{gd,M7} + C_{db,7})} \tag{3.8}$$

To get the most performance out of the current summing stage, all the transistors were optimized for either g_m or R_{out} and/or noise. The output impedance of the current sources

should be maximized, concurrently their noise contribution should be minimized. As discussed above, $I_1 = I_2 = I_{cs} > I_{tail} = 2I_d$ as a consequence the noise and offset contribution of the current sources would be two times stronger when referred back to the input. To reduce this effect the current sources can be biased in extreme strong inversion but at the cost of loss in output swing[1], ICMR[2] and R_{out}. Therefore, to optimize the noise, ICMR and R_{out}, the length of the current sources were increased. Additionally, their overdrive voltage is kept at $V_{ov} \approx 200$ mV while their drain-source voltage $V_{ds} = 300$ mV. The sizing of these current sources are given in Table 3.2.

The cascode transistors' length was kept at a minimum while they were sized to operate at the edge of weak inversion with V_{ov} = -10 mV and V_{ds} =200 mV. By doing this the cascode transistor contributes towards the gain of the amplifier while keeping the parasitic capacitance minimum. The sizing of the PMOS and the NMOS cascode transistors are given in Table 3.2.

The sizing of the transistors M9, M14, and M15 plays a crucial role in determining the biasing of the Class AB output stage. So these transistors are discussed in section 3.4

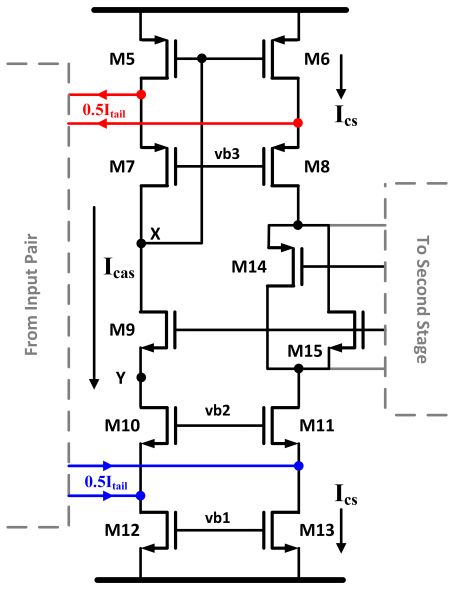


Figure 3.6: Current summing stage

Transistor	W (μm)	L (μm)	M
M5	12	2	6
M6	12	2	6
M7	12	0.16	4
M8	12	0.16	4
M10	6	0.16	4
M11	6	0.16	4
M12	6	4	6
M13	6	4	6

Parameter	Current (μA)
I_{tail}	30
I_{cs}	36
I_{cas}	21

Table 3.2: Parameters of current summing stage transistors

3.3.5. Choppers

In chapter 2, it was shown that chopping is an elegant technique to mitigate the $1/f$ noise and reduce the effect of offset in the amplifier. Chopping has been incorporated only in the first stage because it dominates in noise and offset, and also the signal is converted from differential to signal ended at its output. The location of the input and output choppers are shown in Fig. 3.7.

[1] Extreme strong inversion signify a higher V_{ov} and consequently a higher V_{ds} of the current sources
[2] As shown by equation 2.9, as the V_{ds} of current mirror increases the ICMR can not reach the rails.

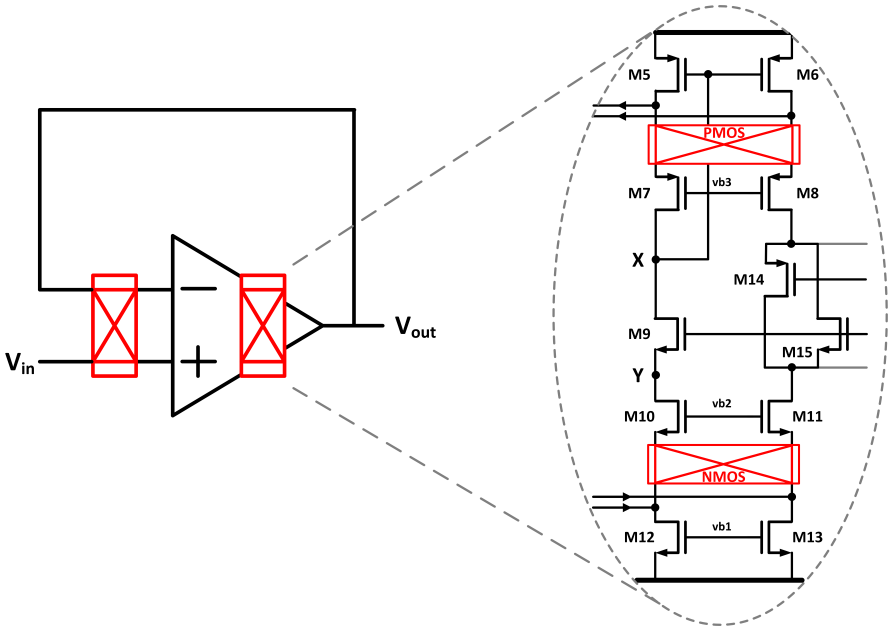


Figure 3.7: Position of input and output choppers

At the input, a conventional NMOS or PMOS switch chopper is not suitable as the input signal swings from rail-to-rail. Due to this, a conventional chopper will be out of operation in one of the halves of the signal. There are two solutions to mitigate this issue. The first solution being to use bootstrapped NMOS switches and the second being to use transmission gate switches. Although, bootstrapped NMOS switches are good for linearity, they consumes large area, as each bootstrapped switch is associated with a capacitor. As the area is a critical aspect of this design (Table 1.1), the input chopper is formed using transmission gate switches as shown in Fig. 3.8 [4]. A drawback of transmission gate switches is that their on-resistance is a function of input voltage swing due to the difference in on-resistance of the PMOS and the NMOS transistors. This effect can be reduced by sizing the PMOS transistors larger than the NMOS transistors, but this also increases the charge injection at the input. The size of the PMOS and the NMOS switches are kept minimum to reduce charge injection which results in a large transient spikes at the output. The on-resistance of the chopper at common-mode voltage is approximately 1kΩ. The sizing of the input chopper switches is given in the Table 3.4.

The output chopper is a combination of two individual PMOS and NMOS choppers as shown by Fig. 3.9 and 3.10 respectively [20]. These choppers are located at a low impedance node of the current summing stage as shown in Fig. 3.7. The cascode transistors isolate the choppers from the high signal swing at nodes A and B (Fig. 3.18). As these choppers are chopping in the current domain the sizing of their switches is critical. The switch must be designed to have low on-resistance otherwise large current flowing through them will result in a substantial potential drop. Such a potential drop introduces can offset due to mismatch between the switches, thereby lowering the offset performance of the amplifier. However, increasing the size of choppers switches also increases their gate capacitance (C_g) which again increases the charge injection and in turn the transient spikes at the output. The sizing of the PMOS and the NMOS chopper switches are given in Table 3.3.

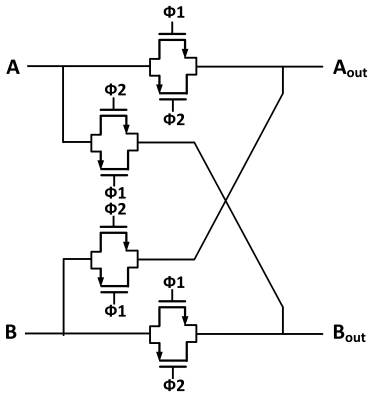


Figure 3.8: Input chopper

Input chopper			
Transistor	W (μm)	L (μm)	M
NMOS	1	0.16	1
PMOS	1	0.16	1
Output chopper			
Chopper	W (μm)	L (μm)	M
NMOS	3	0.16	1
PMOS	3.5	0.16	2

Table 3.3: Parameters of output stage transistors

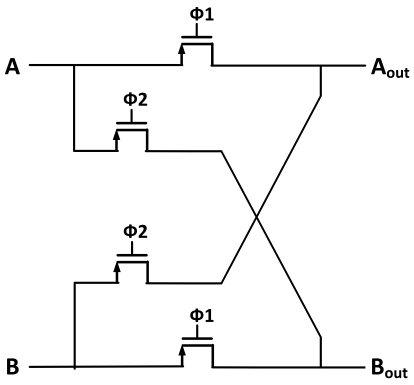


Figure 3.9: Output PMOS chopper

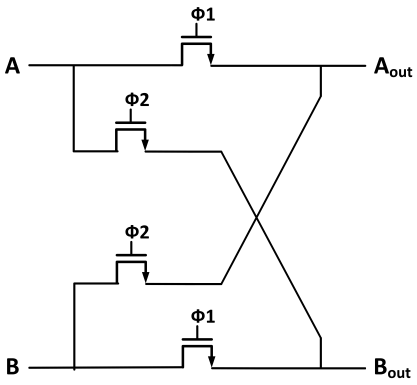


Figure 3.10: Output NMOS chopper

3.3.6. Chopper Layout

As choppers are quite sensitive to mismatch, special care has to be taken during layout to keep the parasitics low and balanced at both the inputs and outputs. A reference layout of the transmission gate chopper is given in Fig. 3.11. To prevent any interference from clock lines (ϕ1 and ϕ2) to the input signal (A and B), the input signals are kept at maximal distance from clock lines. Also, to isolate the clock from other analog signals, the clock signal propagates inside a coaxial structure, where the clock line is shielded with the ground on all sides. To keep the parasitics well matched the surroundings of each switch are made identical. To reduce mismatch and Shallow Trench Isolation stress (STI) multiple dummy transistors are used. To reduce parasitic capacitance at switches the separation between poly and source-drain contacts is also increased. By using these techniques the parasitic capacitance can be restricted to few femtofarads while keeping them balanced at both the input nodes as well as at both the output nodes for symmetry.

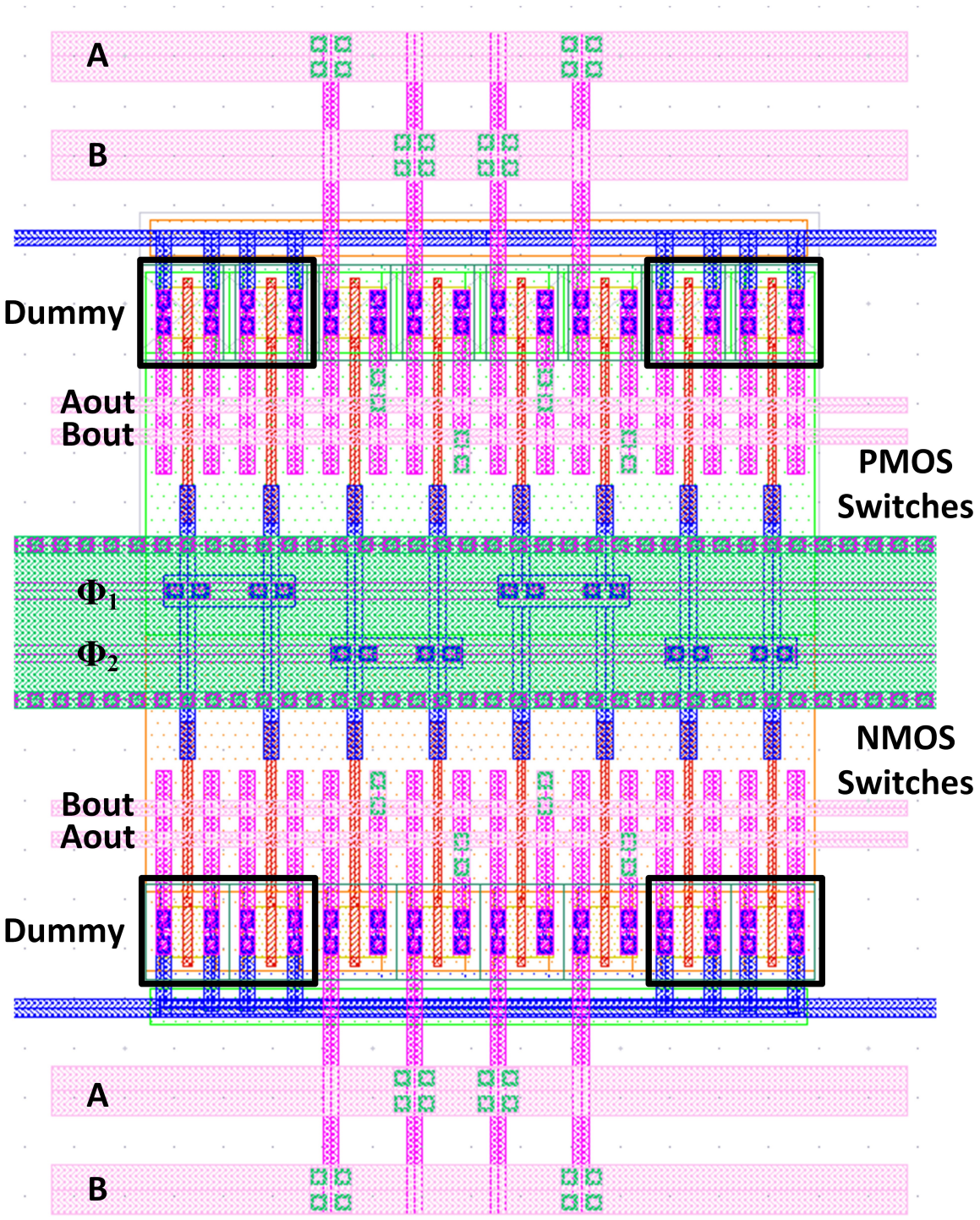


Figure 3.11: Transmission gate chopper layout

3.3.7. Gain-Boosting Amplifier

Gain-boosting has been incorporated in the design to aid the choppers [18]. As the output choppers are located at low impedance nodes in the current summing stage, any voltage difference between the outputs of the chopper (for eg: due to mismatched cascode transistors) will be converted into a chopped current waveform due to the finite on-resistance of the switches. The current has to be sourced from the input pair. This introduces ripple at the output and also decreases the effectiveness of the chopping. Hence, it is essential to boost the R_{out} at chopping frequency at these low impedance nodes.

The location of the gain-boosting PMOS and NMOS amplifiers are shown in Fig. 3.12 and 3.13 respectively. As the feedback loop involves the cascode transistors, gain-boosting mitigates the above-mentioned issue by controlling the gate voltage of the cascode transistors to eliminate the voltage difference. This essentially makes the input node of the chopper a virtual ground. Thus, the higher the gain of the gain-boosting amplifier, the lower the potential difference and better the virtual ground effect. Also, by using gain-boosting the effective R_{out} of the summing stage increases by a factor A[3], which contribute to higher first-stage gain.

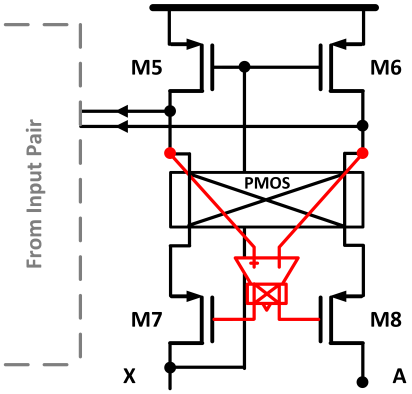


Figure 3.12: Gain-boosting amplifier PMOS

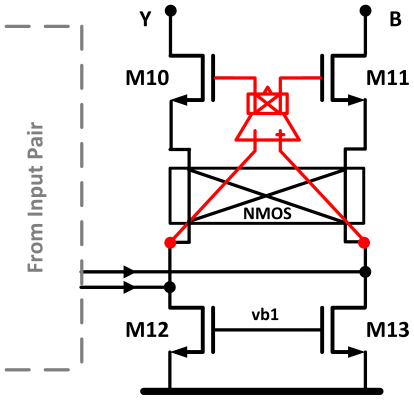


Figure 3.13: Gain-boosting amplifier NMOS

The gain-boosting amplifier (GBA) employs a of pseudo-differential folded cascode single-stage topology. Although this topology has a higher current consumption, it is essential for mainly three reasons. Firstly, we need high gain (≈ 40dB) from the GBAs to meet the offset requirement of the design. Secondly, as the input and output, common-mode voltages are different folded cascode topology is necessary. Lastly, it improves the stability of the entire amplifier. As gain-boosting already gives a doublet[4], this topology gets rid of the current mirroring pole of a single-ended folded cascode. Additionally, it does not require a common-mode feedback (CMFB) circuit to regulate the output.

To ensure stability, optimal speed and performance the unity gain frequency of the GBA (ω_{GB}) should lie between $\beta\omega_1 < \omega_{GB} < \omega_{2^{nd}pole}$ [18]. As the feedback factor β is 1 for the amplifier, the optimum range of the GBA's unity gain frequency is $\omega_{unity,amp} < \omega_{GB} \ll \omega_{2^{nd}pole,amp}$. The unity gain frequency can be calculated from equation 3.6, where load

[3] 'A' is the open-loop gain of the gain-boosting amplifier.
[4] A pole and a zero in the vicinity of each other.

capacitance, for instance of the PMOS GBA, is given by equation 3.9. As the GBA does not drive a high capacitive load its transconductance can be kept quite low and it still achieves a large bandwidth. Furthermore, as the gain is given by the product of g_m and R_{out}, it achieves high gain due to high R_{out}. The unity gain frequency of the GBAs was designed to be 19MHz.

$$C_{load} = C_{gb,M7} + (1+A)C_{gd,M7} + (1+A_o)C_{gs,M7} \tag{3.9}$$

where $C_{gb,M7}$, $C_{gd,M7}$ and $C_{gs,M7}$ are gate-to-bulk, gate-to-drain and gate-to-source capacitance of transistor M7. 'A' is the intrinsic gain from gate to drain and A_o is the gain from gate to source which is approximately one, due to the body effect.

The PMOS GBA consists of the NMOS differential pair (M22-M25), current sources (M26-M30), cascodes (M31-M35), compensation capacitors C_{c1}-C_{c2} and the PMOS output chopper as shown in Fig. 3.14 [4]. Similarly, the NMOS GBA consist of the PMOS differential pair (M36-M39) current sources (M40-M44), cascodes (M45-M349), compensation capacitors C_{c3}-C_{c4} and the NMOS output chopper as shown in Fig. 3.15 [4]. As the input of the GBA is chopped, its output is also chopped to maintain negative feedback. Additionally this also reduces the $1/f$ noise contribution of the GBAs. As the choppers are present at high impedance nodes, they consist of minimum size switches.

The dual input pair compares the Vin+ and Vin- with a reference voltage (V_{refn} or V_{refp}) to regulate the output voltage. The input pair should be sized such that it provides sufficient g_m and it's total gate capacitance C_g is low. This is true especially for the PMOS GBA, as it contributes to C_{gd} of M5 and M6, which reduces the mirror pole frequency as shown by equation 3.8. The current sources and the cacode transistors are scaled down with the current such that they have the same Vov as the main amplifier's current sources and cascode transistors. The sizing and currents of the PMOS and NMOS GBAs are given in Table 3.4 and 3.5 respectively.

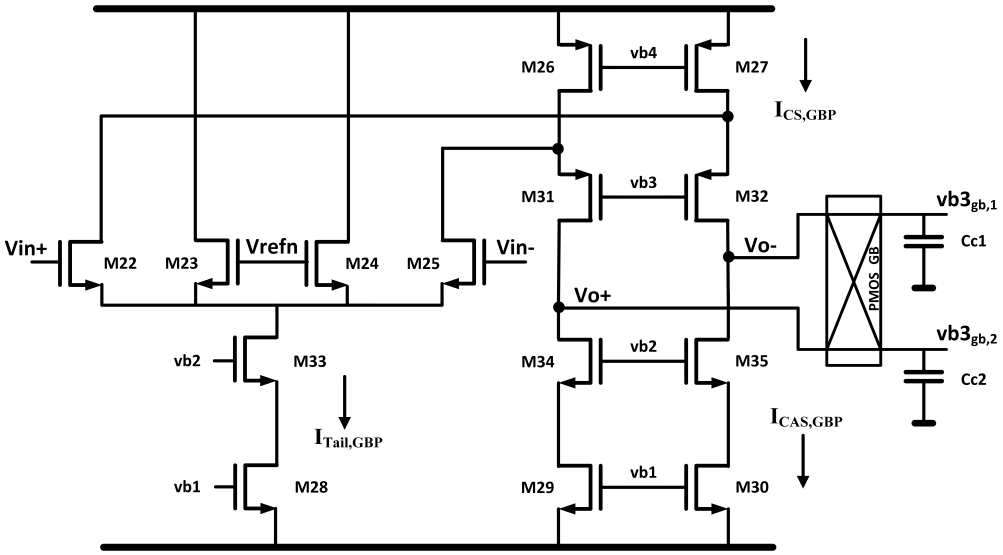


Figure 3.14: PMOS GBA schematic

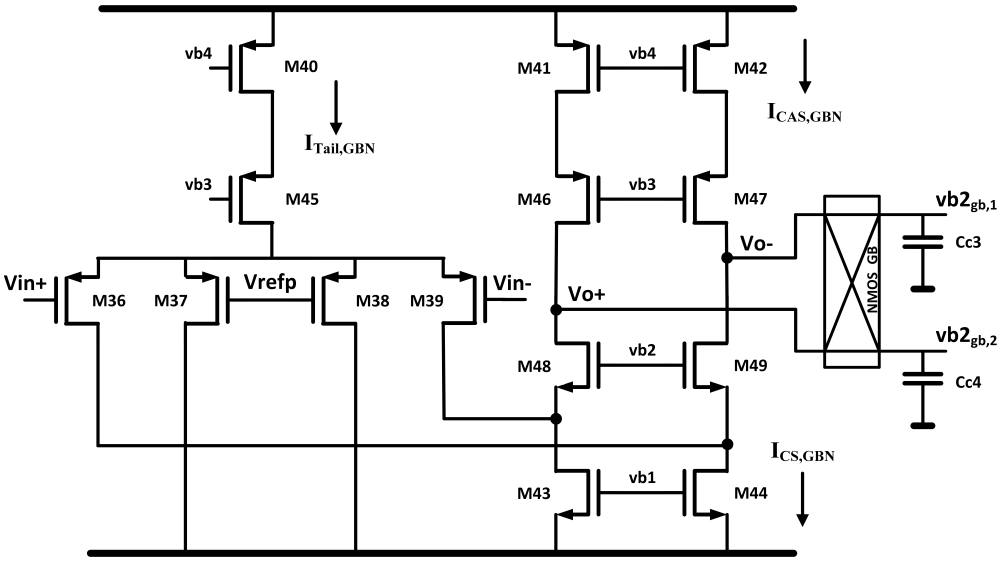


Figure 3.15: NMOS GBA schematic

Transistor	W (μm)	L (μm)	M
M22-M25	1	0.16	1
M26-M27	2	2	2
M28	1	4	4
M29-M30	1	4	1
M31-M32	2	0.16	1
M33	1	0.16	4
M34-M35	1	0.16	1
Parameter		Current (μA)	
$I_{tail,GBP}$		4	
$I_{CS,GBP}$		2	
$I_{CAS,GBP}$		1	
Parameter		Voltage (V)	
V_{refn}		1.492	
Parameter		Capacitance (fF)	
C_{c1}		50	
C_{c2}		50	
Output chopper			
Switch	W (μm)	L (μm)	M
PMOS	1	0.16	1

Table 3.4: Parameters of gain-boosting amplifier PMOS

Transistor	W (μm)	L (μm)	M
M36-M39	1	0.16	1
M40	2	2	4
M41-M42	2	2	1
M43-M44	1	4	2
M45	2	0.16	4
M46-M47	2	0.16	1
M48-M49	1	0.16	1
Parameter		Current (μA)	
$I_{tail,GBN}$		4	
$I_{CS,GBN}$		2	
$I_{CAS,GBN}$		1	
Parameter		Voltage (V)	
V_{refp}		0.314	
Parameter		Capacitance (fF)	
C_{c3}		100	
C_{c4}		100	
Output chopper			
Switch	W (μm)	L (μm)	M
NMOS	1	0.16	1

Table 3.5: Parameters of gain-boosting amplifier NMOS

3.4. Rail-to-Rail Output Stage

The rail-to-rail output stage given in Fig. 3.18 comprises of a Monticelli Class-AB topology [21], where transistor M20-M21 are common-source stage while transistors M14-M19 are its biasing circuitry. To deliver dynamic current to the output load the common-source stage is connected in push-pull configuration. The biasing circuitry is used to generate two in-phase signals separated by a constant voltage to drive the output transistors.

The functionality of the Class-AB stage is as follows, the current that propagates to nodes A and B from the current summing stage comprises a big signal (I_o) and a small signal (i_o) term. As nodes A and B are connected to all high impedance nodes (all gates and drains) they can be driven by small signals quite effortlessly. Hence, any variation in i_o can easily vary the potential at those nodes. For example, any positive variation in i_o will result in an increase in voltage at node B (V_B). Due to this $V_{gs,21}$ increases, whereas $V_{gs,15}$ and $I_{d,15}$ decreases as M15's gate is connected to a fixed potential. As $I_{d,14}$ + $I_{d,15}$ is a constant, decrease in $I_{d,15}$ increases $I_{d,14}$ and so does the $V_{gs,14}$ and voltage at node A (V_A). Therefore, V_A follows V_B and transistor M14-M15 behaves like a floating voltage source.

Also, the output stage consists of two trans-linear loops given by equations 3.10 and 3.11, which prevents the output transistor from entering the cut-off region. For instance, to deliver a larger amount of current to the load the gate-source voltage of M21 transistor must be high. Due to this M15 turns off, diverting all the current to M14. This makes node B a low impedance node while node A is still at high impedance. As a result, all the input current is steered into node A and the gate voltage of transistor M21 is clamped preventing it from entering the cut-off region.

$$V_{gs,16} + V_{gs,17} = V_{gs,15} + V_{gs,21} \tag{3.10}$$

$$V_{gs,19} + V_{gs,18} = V_{gs,14} + V_{gs,20} \tag{3.11}$$

To increase the efficiency [5] of the second stage, the output transistors M20-M21 should operate in weak inversion. However, biasing the output transistors in weak inversion will push their V_{gs} below their respective threshold voltages i.e., V_{thn} = 420 mV and V_{thp} = 450 mV. This indicates that the potential difference between the rails and node A and B can not be higher than 450 mV, which in turn limits the maximum headroom for the cascode transistors M8 M11 and current sources M6 & M13 (Fig. 3.6).

Since we have a minimum requirement on the headroom at nodes A and B, the minimum required gate-source voltage for the output transistors is $V_{gs} \geq$ 500 mV. As overdrive voltage is a function of V_{gs} and V_{th}, we can optimize the threshold voltage of the transistors to bias them as close as possible to weak inversion. Fig. 3.16 shows the variation of the NMOS threshold voltage as a function of its length, it can be observed that as the length of the transistor increases the threshold voltage also starts to increase, it peaks around L = 0.25 μm and then decreases. Hence the length of the second stage transistors was fixed at 0.248 μm, whereas, the width of the transistors is dependent on the required gate-source

[5] The efficiency here refers to obtaining higher g_m/I_d value.

voltages. The output stage burns 120 of quiescent current to keep the amplifier unity-gain stable. Whereas the output stage delivers a peak current of ±8 mA to the 15pF switched capacitor load (Fig. 3.17). The sizing of output transistors and their respective gate-source voltages are given in Table 3.6.

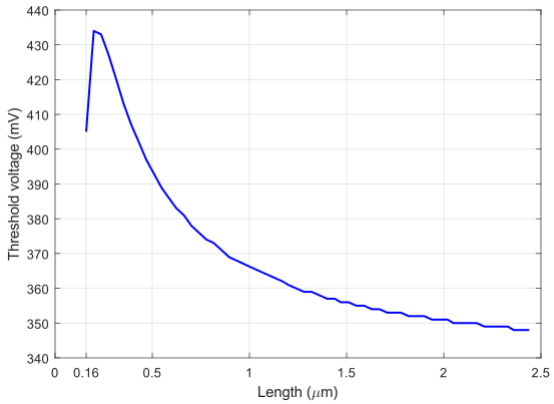


Figure 3.16: V_{th} vs L characteristics of NMOS transistor

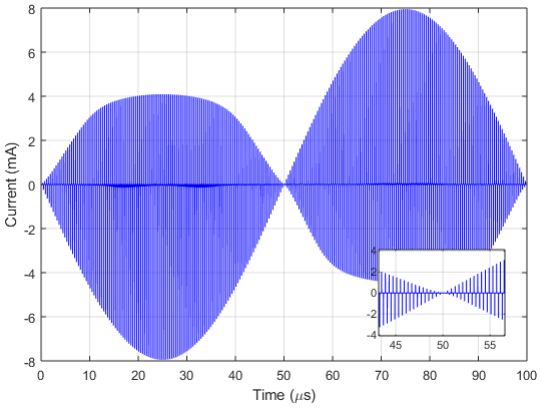


Figure 3.17: Class AB output current

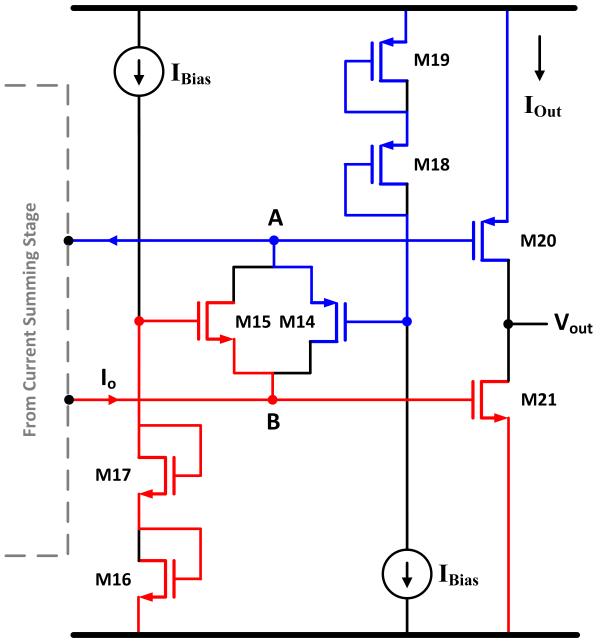


Figure 3.18: Class AB output stage

Transistor	W/L	M	V_{gs} (V)
M9	1.2/0.248	4	0.6
M14	6.0/0.248	2	0.5
M15	1.2/0.248	2	0.6
M16	1.2/0.248	1	0.5
M17	1.2/0.248	1	0.6
M18	6.0/0.248	1	0.5
M19	6.0/0.248	1	0.5
M20	6.0/0.248	16	0.5
M21	1.2/0.248	16	0.5

Parameter	Current (μA)
I_{Out}	120
I_{bias}	6

Table 3.6: Parameters of output stage transistors

3.5. Frequency Compensation

Miller compensation [19] is used to make the two-stage amplifier unity-gain stable because of three main reasons, Firstly, Miller compensation provides smooth 20 dB/dec roll-off making it suitable for designs requiring fast settling. Secondly, the gain attenuated by the Miller capacitor is utilized in reducing the output impedance and distortion of the output stage. Lastly, as the Miller capacitor is magnified by the gain in the Miller loop, the size

of the compensation capacitor can be quite small, hence making it area-efficient [4]. The Miller capacitor can be calculated from equation 3.12 [19] to be 4.3pF i.e., $C_{M1} = C_{M2} = 2.15$ pF.

$$C_M = \frac{g_{m,in}}{2\pi f_{unity}} \tag{3.12}$$

However, Miller compensation also introduces a right half plane (RHP) zero (f_z) given by equation 3.13. Presence of RHP zero reduces the phase margin and may cause total phase reversal if $f_z < f_{2^{nd}pole}$ [4]. This effect is of more concern in CMOS due to their low g_m as compared to BJTs.

$$f_z = \frac{g_{m,2^{nd}stage}}{2\pi C_M} \tag{3.13}$$

where $g_{m,2^{nd}stage}$ is the transconductance of the output stage and C_M is the Miller capacitor. To mitigate this issue active Miller compensation is used where cascode transistor is part of the Miller loop as shown in Fig. 3.19 [4]. This has two advantages, firstly, the Miller loop has higher gain due to which two times higher bandwidth can be achieved for the same power consumption. Also, the RHP zero is pushed to higher frequencies. Secondly, the Miller capacitor is now connected to the virtual ground of gain-boosting amplifier, which has negligible voltage swing. Hence this improves the linearity of the amplifier while the Miller effect is active [4]. To further improve the phase-margin nulling resistor (R_{null}) is connected in series with the Miller capacitor. The R_{null} attenuates the feed-forward path by the exact ratio by which the output stage amplifies it. Hence, $R_{null} = 1/g_{m,2^{nd}stage} \approx 800$ Ω.

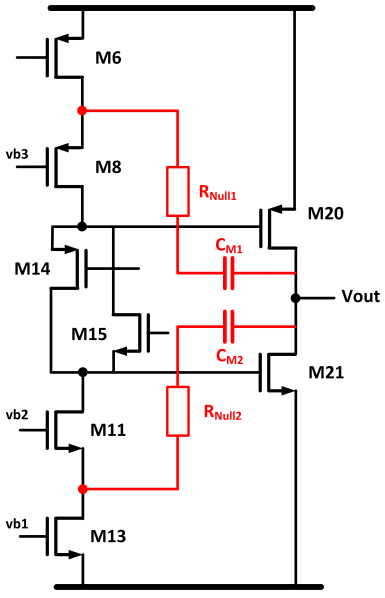


Figure 3.19: Active Miller compensation

3.6. Clock Generator

The clock generator circuit is used to generate a complementary overlapping clock signal for the choppers. The clock generator circuit is shown in Fig. 3.20 consists of a type-D flip-flop (D1), an SR latch made-up from inverter I_1-I_5 and two output buffers (B_1 and B_2). The D flip-flop provides a 50% duty cycle complementary clock signal of half the clock

frequency which is 200 kHz. Whereas, the SR latch controls the intersection point of the complementary signals. The buffer is used to drive the capacitive load. In inverters I_1 to I_3, the drive strength of the PMOS and the NMOS transistor are matched closely to have similar rise and fall time (≈ 100 ps). By doing so we ensure the intersection of the complementary clock signals at $V_{dd}/2$, which is essential for a smooth transition from one chopping phase to another as shown in Fig. 3.32. The circuit is built from standard digital cells specially tuned for clocking circuits, and shows worst-case clock skewing of 300 ps for slow corner.

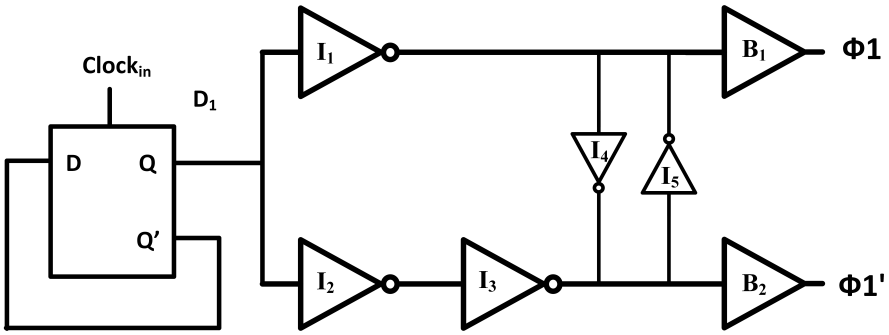


Figure 3.20: Complimentary clock generator circuit

3.7. Bias Circuit

To ensure the circuit's performance over PVT, the biasing circuit is designed to deliver current proportional to absolute temperature (PTAT). The biasing circuit is given in Fig. 3.21 consists of a core and a start-up circuit [2]. The core is a beta multiplier circuit designed to provide constant g_m over PVT. As given by equation 3.14 if the drain current of N1 and N2 are well-matched then their g_m is a function of R_{Bias} and K only.

$$g_m = \frac{2}{R_{bias}}(1 - \frac{1}{\sqrt{K}}) \tag{3.14}$$

where K is the ratio of W/L of N1 and N2 and is set to be 1:2. The core has two stable operating states, one where all the biasing node are tied to the rails and another when all the nodes are at the desired bias voltages. A start-up circuit is used to provide a push to the circuit and then the positive feedback of the loop sets the circuit to its desired operating point. To increase the gain in the loop, cascoding is incorporated into the beta multiplier circuit.

The biasing voltages for the core as well as for the main amplifier and GBAs are generated by a resistive ladder. Furthermore, the resistive ladder is also used to generate reference voltage (V_{CM}) for the rail-to-rail input pair. This is done as N-poly resistance show very low deviation in bias voltages over temperature. Transistor N9 and N10 form a backup startup circuit that is controlled using external voltage Vc1. The value of sizing, currents, and resistances of the biasing circuit are given in Table 3.7.

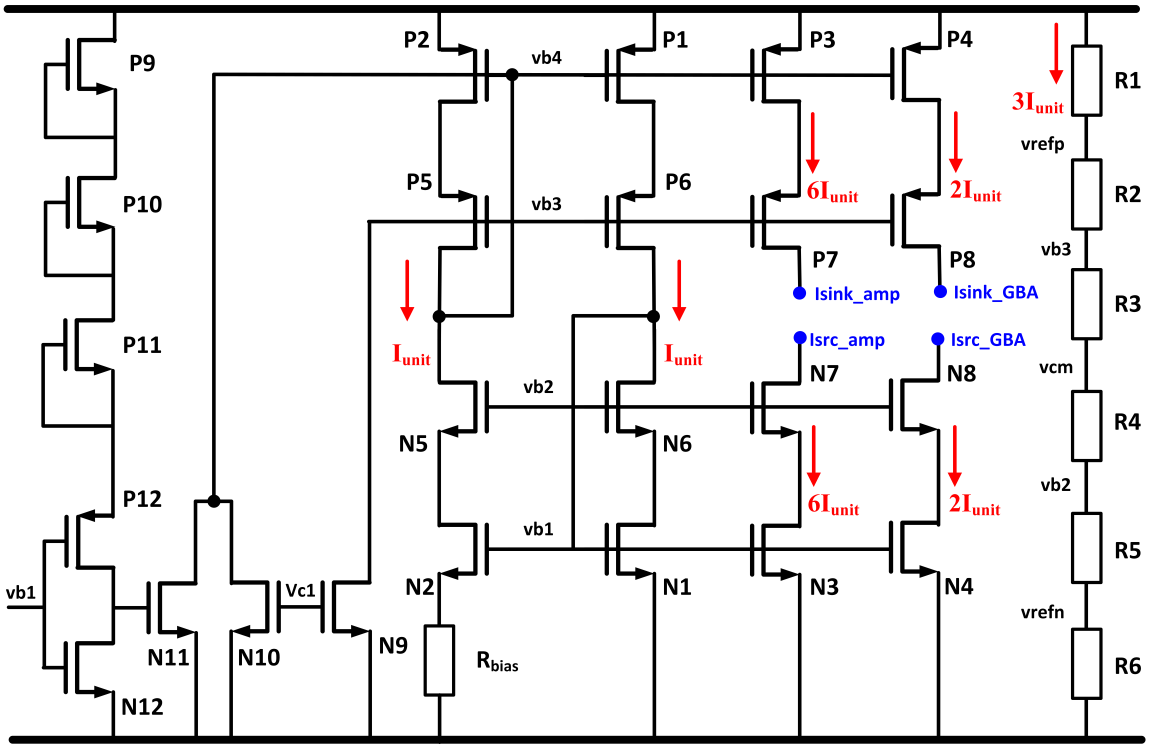


Figure 3.21: Biasing circuit

Table 3.7: Parameters of the constant g_m biasing circuit.

Transistor	W (μm)	L (μm)	M	Transistor	W (μm)	L (μm)	M
N1	1	4	1	P1	2	2	1
N2	1	4	2	P2	2	2	1
N3	1	4	6	P3	2	2	6
N4	1	4	2	P4	2	2	2
N5	1	0.16	1	P5	2	0.16	1
N6	1	0.16	1	P6	2	0.16	1
N7	1	0.16	6	P7	2	0.16	6
N8	1	0.16	2	P8	2	0.16	2
N9, N10, N11	1	8	1	P9, P10, P11	1	1	1
N12	0.568	0.16	1	P12	1	0.16	1

Parameter	Resistance (kΩ)	Parameter	Resistance (kΩ)
R_{Bias}	50.81	R4	51.63
R1	104.35	R5	14.31
R2	159.83	R6	104.83
R3	35.33		

Parameter	Current (μA)
I_{unit}	1

3.8. Final Schematic

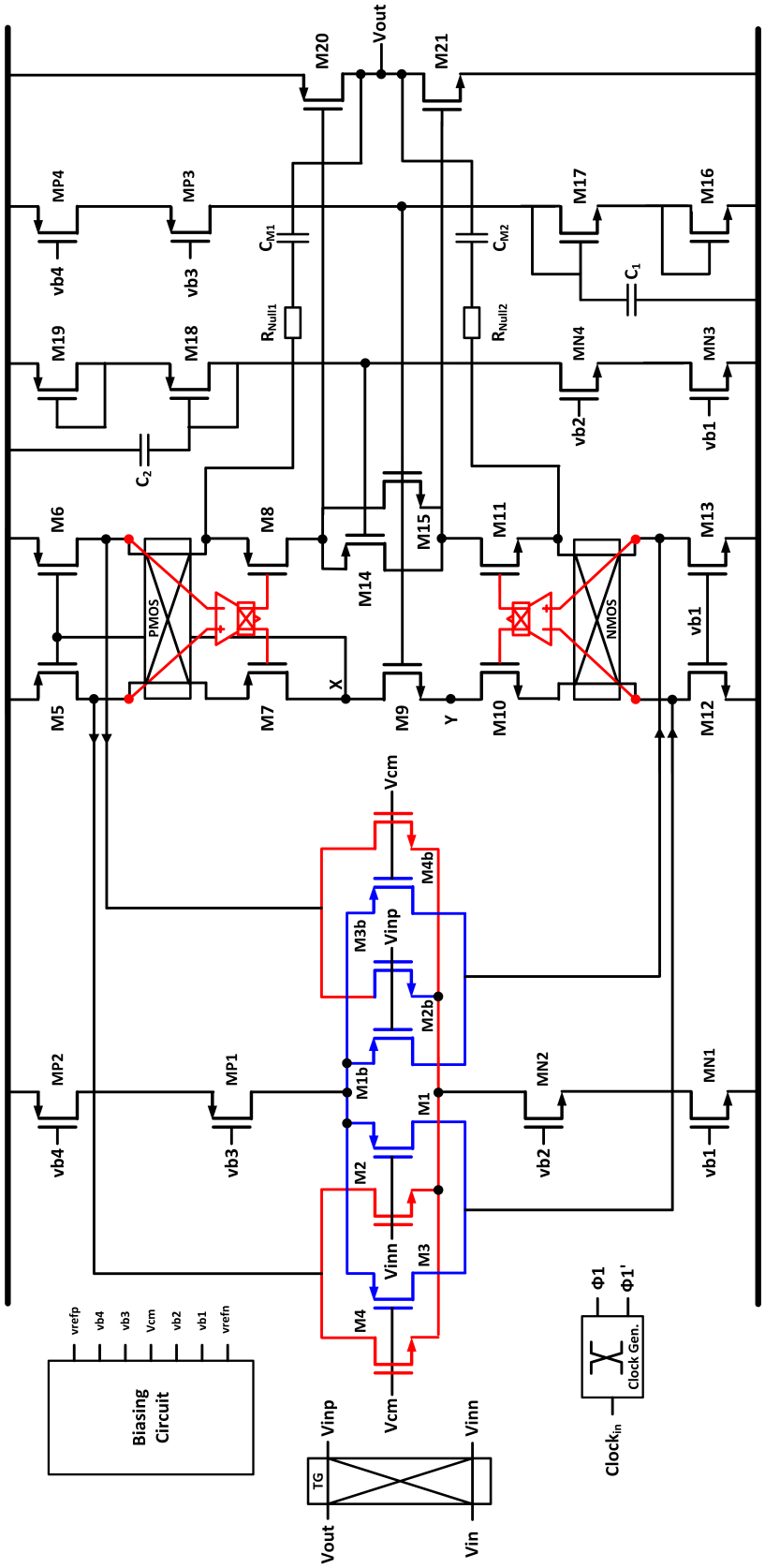


Figure 3.22: Full schematic of the buffer

3.9. Simulations

The loop-gain and phase response of the amplifier at three different input common-mode voltages for a load capacitance of 15 pF is shown in Fig. 3.23. The amplifier achieves a unity-gain frequency of ≈ 18 MHz with an open-loop gain of ≈ 140 dB. The unity-gain frequency, gain margin (GM) and phase margin (PM) at those points are given in Table 3.8.

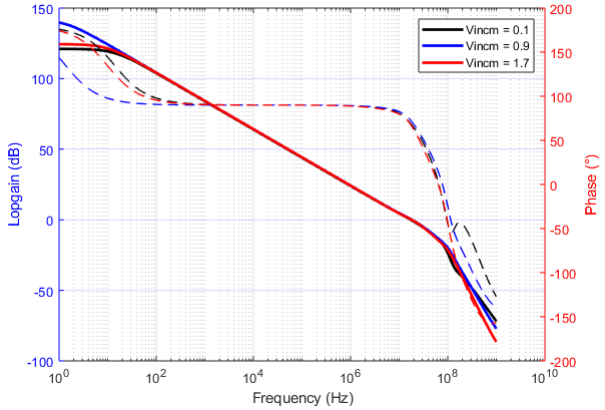


Figure 3.23: Loop-gain and phase of the amplifier

Parameter	V_{incm} (V)	Value
f_{unity}	0.1	17.6 MHz
PM		67°
GM		13.6 dB
f_{unity}	0.9	18.5 MHz
PM		70°
GM		15 dB
f_{unity}	1.7	18.3 MHz
PM		65°
GM		14 dB

Table 3.8: Stability parameters of the amplifier

The noise performance of the amplifier shown in Fig. 3.24. The noise density (en) before and after chopping is enabled are 70 nV/$\sqrt{Hz}$ and 17 nV/$\sqrt{Hz}$ respectively. The SNR achieved is 108 dB which is close to the target specification and the system is thermal noise limited.

The offset histogram of the amplifier with chopping enabled is given in Fig. 3.25. The offset is found to be 2.5 μV (sigma) with a mean of -31.5 nV, while the offset without chopping is 3mV.

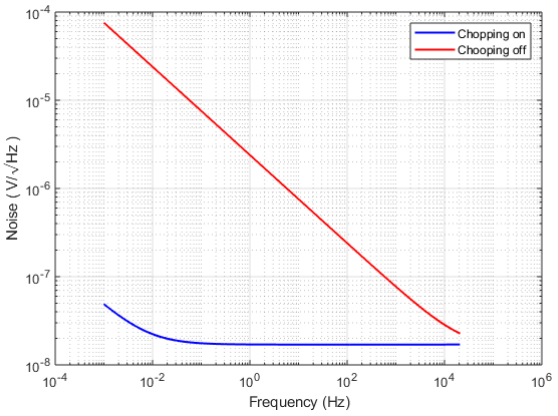


Figure 3.24: Simulated input noise density

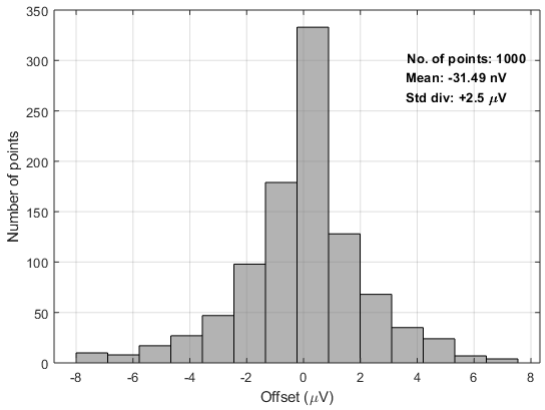


Figure 3.25: Simulated offset histogram

The amplifier achieves a THD is below -110 dB with input signal of 1 kHz and 10 kHz as shown in Fig. 3.26. This is also verified with Monte Carlo simulations as shown in Fig. 3.27.

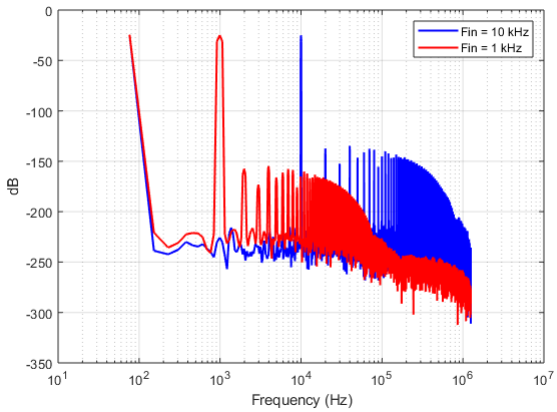


Figure 3.26: Simulated THD performance at 1kHz and 10 kHz.

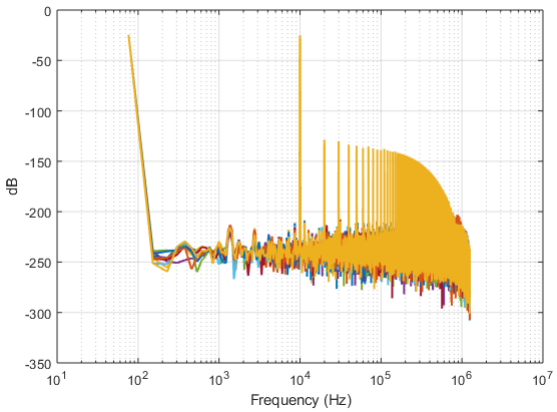


Figure 3.27: Monte Carlo simulation for THD at 10 kHz.

Lastly, the step response of the amplifier is shown in Fig. 3.28. Although the amplifier has critically damped response to the step input, ringing is observed when output transitions from 0.9V to 0.1 V. This is due capacitive feed-forward effect caused by the large parasitic capacitor of PMOS input pair.

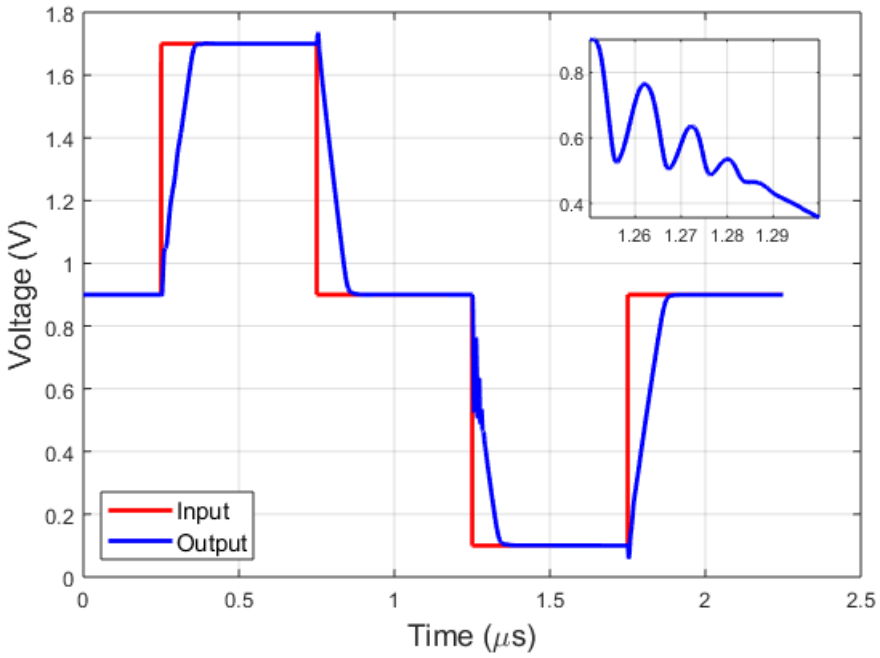


Figure 3.28: Step response of the amplifier

3.9.1. Miscellaneous Simulations

The g_m variation over the ICMR is shown in Fig. 3.29. The total variation in g_m of less than 2 % shows the effectiveness of CSO g_m control architecture.

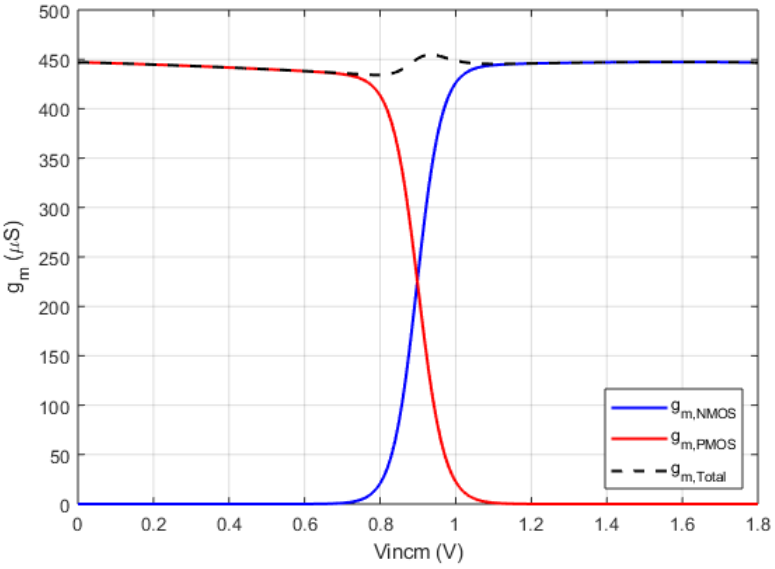


Figure 3.29: g_m variation over the ICMR

Figure 3.30 and 3.31 shows the loop-gain and phase response of GBA NMOS and PMOS respectively. The GBAs stability parameters are given in Table 3.9 and Table 3.10.

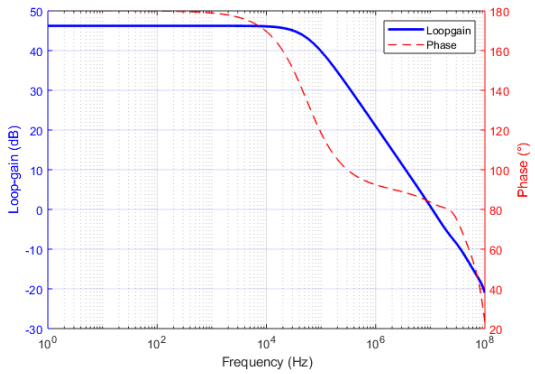


Figure 3.30: GBA NMOS loop-gain and phase

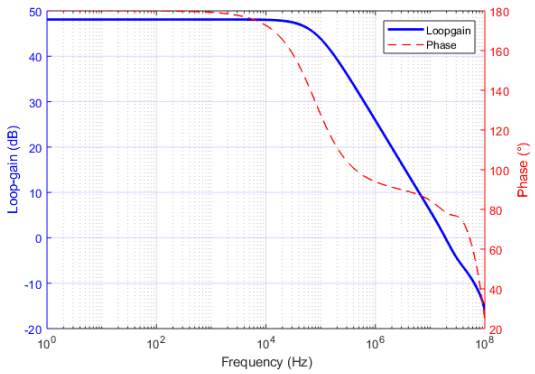


Figure 3.31: GBA PMOS loop-gain and phase

Parameter	V_{incm} (V)	Value
f_{unity}	0.3	19 MHz
Phase Margin		83°
Gain Margin		46 dB

Table 3.9: Stability parameters of GBA NMOS.

Parameter	V_{incm} (V)	Value
f_{unity}	1.5	19 MHz
Phase Margin		78°
Gain		48 dB

Table 3.10: Stability parameters of GBA PMOS.

Figure 3.32 shows that the complimentary clocks ($\phi 1$ and $\phi 1'$) crosses over at 0.9 V. The clock is immune to process, mismatch and temperature variations and shows a maximum

deviation in cross-over voltage by 0.9 V ± 50 mV.

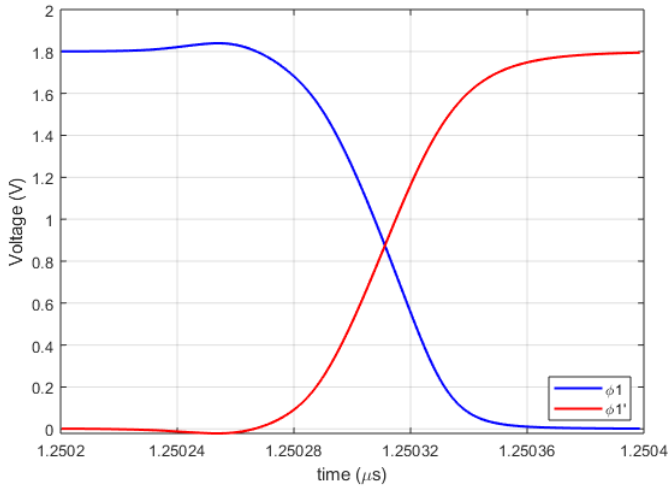


Figure 3.32: Overlapping complimentary clock

The g_m variation over process and temperature of the biasing circuit is shown in Fig. 3.33. It can be seen that the circuit maintain the nominal g_m over temperature range of -50 °C to 150 °C. However, the circuit shows large deviation of approximately ± 25% from the nominal value of g_m in fast and slow corners due to the spread in resistor R_{bias}.

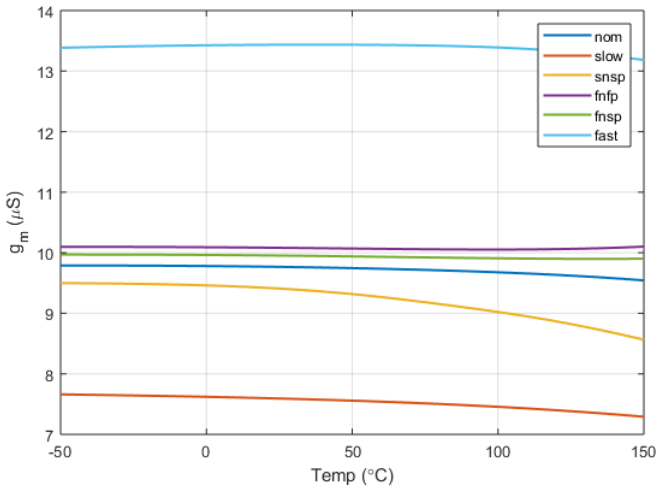


Figure 3.33: g_m variation over the temperature and process

4

Measurements

Since the amplifier aims to achieve low noise, offset and distortion specifications, it is essential to ensure that its performance is not compromised by external factors such as off-chip components, power supply, and printed circuit board (PCB).

4.1. Measurement Setup

The buffer is unity-gain stable and is therefore also stable at higher gain settings. For ease of measurement, the inverting terminal of the buffer is intentionally left unconnected so that it can be configured as an amplifier with variable gain. The input signal, feedback, and clock signal are three critical signals for the accuracy in measurements. The measurement setup is shown in Fig. 4.1.

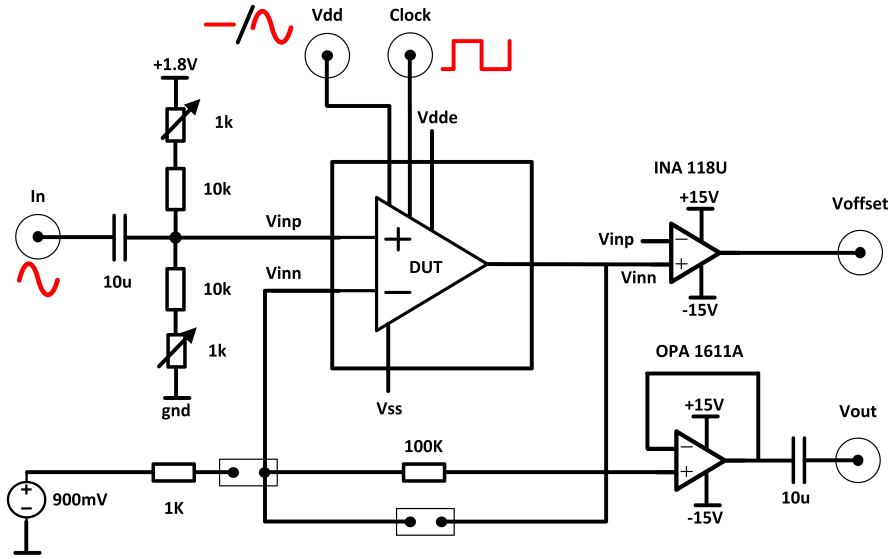


Figure 4.1: Measurement setup

4.1.1. PCB Design

A four-layer PCB is designed for prototype measurement. As the ground becomes the reference of all the signals, it's essential to keep it low ohmic. Hence an entire layer is used as a ground plane. Also, to avoid crossing of the analog ground loop with power and digital ground loops, the individual ground planes are isolated from each other using a star connection. Similarly, other layers are dedicated to carrying power and signal lines.

The input capacitance of the audio analyzer (≈ 30 pF) and the parasitic capacitance of PCB can easily exceed the maximum load capacitance of the amplifier (≈ 50 pF). This may cause oscillation in the amplifier. In addition, the transient step from chopping may lead to sustained oscillations. Therefore a low distortion, low noise, and a high capacitive load driving capable output buffer (OPA 1611) is used to drive the analyzer [22].

Linear regulators (LDO) are used to generate all the required voltages. Separate LDOs are used to power the device under test (DUT), output buffer and the pad-ring. The PSRR of LDOs and the filtering capacitors placed close to the chip greatly reduce the noise and decouple the high-frequency signal from the supply. To avoid non-linearity from off-chip components, thin metal film resistors and polypropylene capacitors are used on the PCB.

4.2. Measurement Results

The rail-to-rail input-output amplifier is realized in 0.16 μm technology and occupies 0.1 mm^2. The die micro-graph of the chip is given in Fig. 4.2. The amplifier consumes 272 μA from 1.8 V power supply.

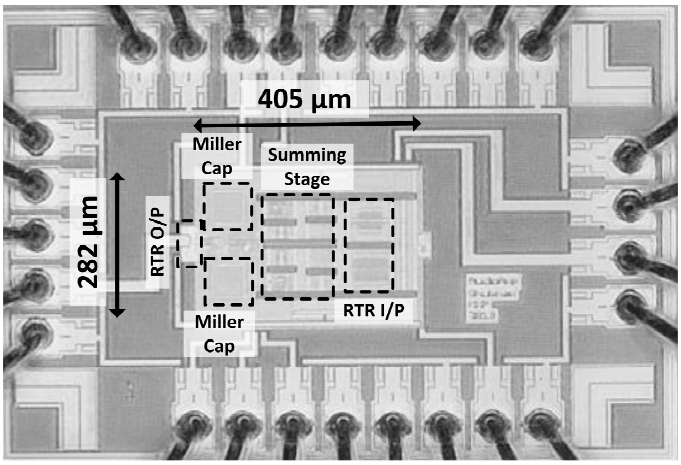


Figure 4.2: Die micro-graph

4.2.1. Rail-to-Rail Output

A sine wave of 1 kHz with a swing of 0.6 V_{rms} over 0.9 V common-mode is applied at the input of the DUT in unity-gain configuration. The output waveform of the buffer authenticates the rail-to-rail input and output capability of the buffer and is shown Fig. 4.6.

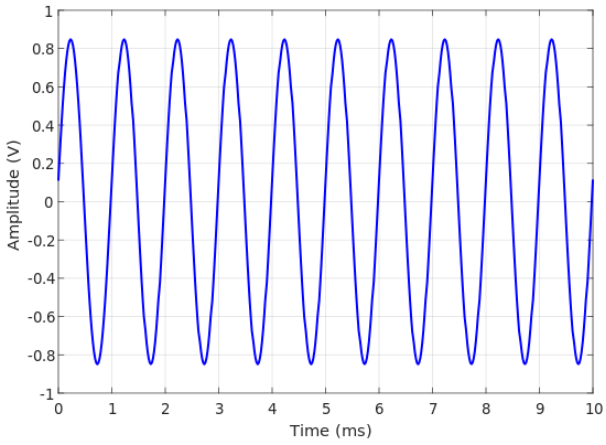


Figure 4.3: Output waveform of the buffer.

4.2.2. Linearity

For measuring the distortion, the DUT is configured in the unity-gain configuration. Since the signal generator provides a low distortion sinusoidal input with common-mode at 0 V, the input signal is AC coupled to the DUT. Whereas, to mitigate the offset of the output buffer, the output is also AC coupled to the audio analyzer. To ensure the linearity measurement is not limited by the output buffer, it's THD+N is 10 dB below the target specification. The output buffer have a THD+N of -123 dB for a input signal of 0.6 V_{rms} at 1 kHz [22].

The linearity performance of the amplifier is characterized at two frequencies, first at 1 kHz to account for 20 in-band harmonics and second at 10 kHz which is the highest signal frequency with at least one harmonic in the audio bandwidth. The FFT at 1 kHz and 10 kHz are shown in Fig. 4.4. The amplifier achieves a THD of -114 dB and -108 dB at 1 kHz and 10 kHz respectively. The DUT meets the THD target specification at 1 kHz, while it fall short by 2 dB at 10 kHz. Furthermore, it achieves THD+N of -104.3 dB and -99.7 dB at 1 kHz and 10 kHz respectively.

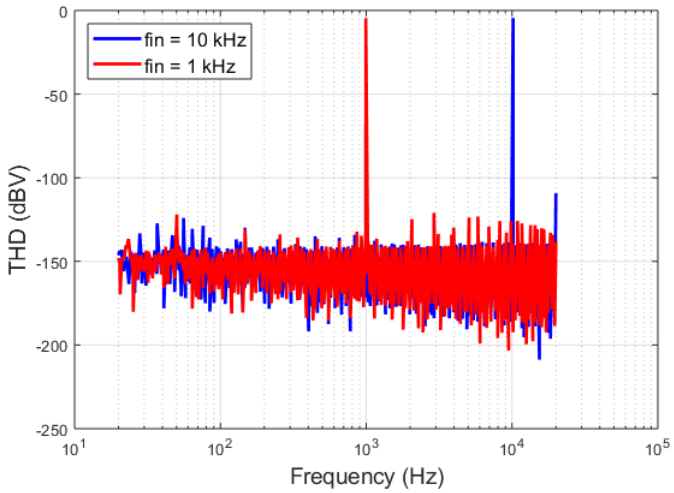


Figure 4.4: THD at 1 kHz and 10 kHz.

4.2.3. Offset

To measure the offset of the DUT a low offset instrumentation amplifier is used [23]. The instrumentation amplifier (INA) measures the difference between input and output voltage (Vinp and Vinn) differentially. As the target specification has offset in micro-volts, the instrumentation amplifier is set at a gain of 1000x for reliable measurements. The offset of INA was first measured separately and subtracted from the final measurement to get offset of the DUT. The offset histogram of 26 samples is shown in Fig. 4.5. The effectiveness of chopping can be observed from the maximum offset of 7 μV and the standard deviation is 2.7 μV. Also, the buffer shows a mean offset of 1.08 μV, this can be perceived as a systematic offset since it is a single-ended design.

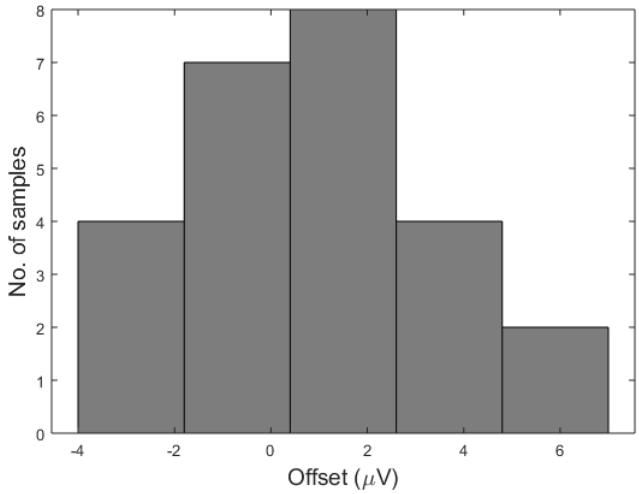
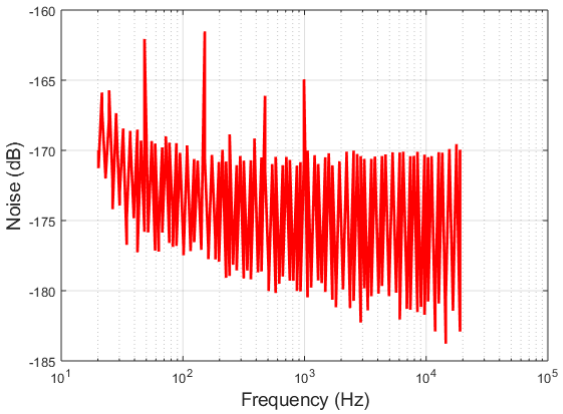


Figure 4.5: Offset histogram

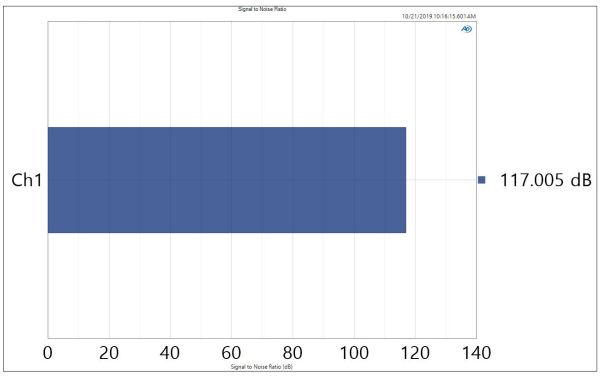
4.2.4. Noise

The noise floor of the Audio Precision (APx500) signal analyzer is shown in Fig. 4.6 and is found to be 10 dB lower than the target noise specification. Also, the input noise density of the output buffer is 1.1 nV/$\sqrt{Hz}$ which is 17x smaller than the DUT's target noise density [22]. This ensure an accurate noise floor measurement of the DUT.

For measuring the noise floor of the design, the DUT is again configured in the unity-gain configuration. The efficacy of chopping in up-modulating the $1/f$ noise can be seen from Fig. 4.7. A SNR of 106.8 dB and 96.1 dB is achieved for input signal of 0.6 V_{rms} with and without chopping respectively. This results noise density of 19.3 nV/$\sqrt{Hz}$ and a total integrated noise of 2.7 μV in audio bandwidth. The noise performance of the amplifier is degraded by the presence of power-line noise and its harmonics which are originating from the measurement setup. Thus, the measured noise performance is off by 1.3 dB from the target specification and is probably limited by measurement setup.

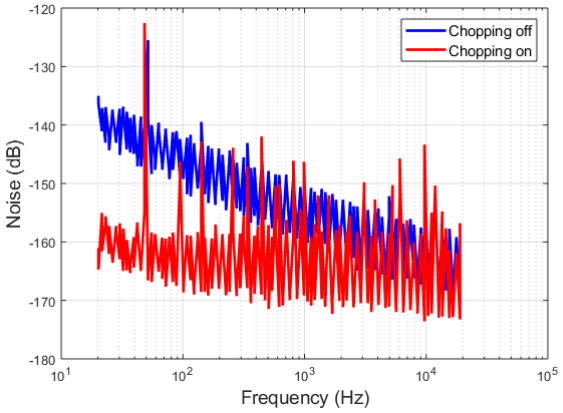


(a) Noise floor of the signal analyzer

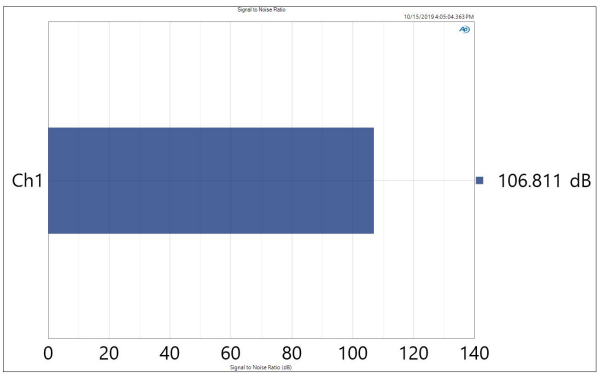


(b) SNR of the analyzer for an input signal of 0.6 V_{rms}

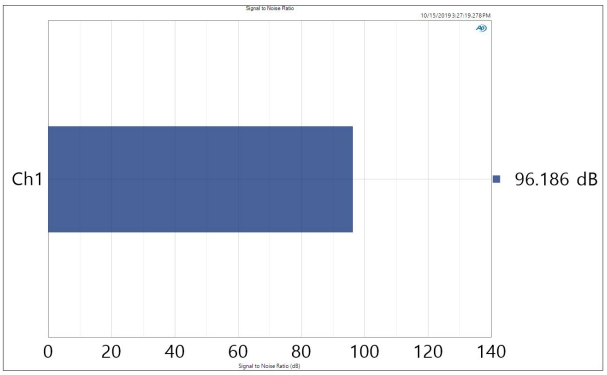
Figure 4.6: Noise performance of audio analyzer APx500.



(a) Noise floor with and without chopping at 1x gain



(b) SNR with chopping for an input signal of 0.6 V_{rms}



(c) SNR without chopping for an input signal of 0.6 V_{rms}

Figure 4.7: Noise performance of the DUT

4.2.5. PSRR

To measure power supply rejection, the V_{dd} of the DUT is supplied with a 200 mV_{pp} sine wave with an offset of 1.8 V. The inputs are biased at common-mode voltage (Vcm = 0.9V) and the variation at the output of the amplifier is measured. The PSRR of the DUT is shown

in Fig. 4.8. Over the audio bandwidth the DUT achieves a PSRR of greater than 80 dB, and more than 100 dB at DC.

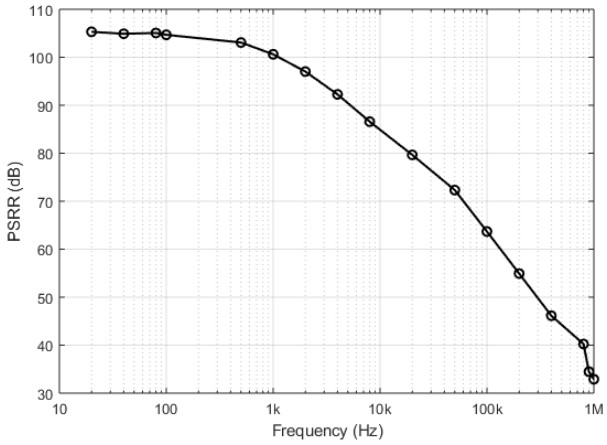


Figure 4.8: PSRR of the DUT

4.3. Performance Summary and Comparison

Trade-off are an integral part of analog circuit design. Most analog circuits are limited by the trade-off between power, noise, and speed. There exist several figures of merits (FoM) to judge the system's performance on various parameters. For amplifiers, the most common FoM is the Noise Efficiency Factor (NEF) and is given by equation 4.1 [24].

$$NEF = V_{n,rms}\sqrt{\frac{2I_{total}}{4\pi kTV_T BW}} \tag{4.1}$$

From measurement results the NEF of the amplifier is 14.81. A Comparison of the prototype's performance with other amplifiers with similar specifications is given in table 4.1

Table 4.1: DUT performance comparison table

Parameter		[25]	[26]	[27]	**This work**	**Unit**
RTR Input and Output		Yes	Yes	Yes	Yes	
V_{dd}	Positive Supply	5	3.3	3.3	1.8	V
V_{os}	Offset (1-sigma)	0.3	0.025	3.7	0.002	mV
e_n	Noise density	6*	12	94	19.3	nV/$\sqrt{Hz}$
THD	fin = 10 kHz	—	—	-94	-108	dB
THD+N	fin= 1 kHz	-114	-108	—	-104	dB
PSRR	Power supply rejection ratio	90	90	—	80	dB
C_{Load}	Capacitive Load	—	100	15	15	pF
I_Q	Quiescent Current	3.25	0.81	0.11	0.272	mA
P	Power	5.06	2.6	0.38	0.504	mW
NEF	Noise efficiency factor	13.15*	16.31	37.90	12.28	
* The noise density and NEF provided in the datasheet is A-weighted.						

5

Conclusion and Future Work

5.1. Conclusion

An amplifier with high linearity, low noise, low offset and with switched capacitor driving capability is presented in this thesis. Using a top-down design approach, the target specifications were defined to outperform the previous designs [27] as well as being a good candidate for driving a high-performance zoom ADC [2]. A block-level architecture was realized after identifying and tackling all the possible sources of non-linearity, offset and noise. These blocks were then implemented at the transistor level. The amplifier was designed, simulated and fabricated in standard CMOS 160 nm process. For characterization of IC performance, a measurement setup was developed.

Measurement results match the simulation results and are only limited by the measurement setup. The amplifier's input can track and deliver rail-to-rail input and output signals respectively. The linearity measurements prove that the CSO technique effectively controls the g_m of the complementary input pairs. The combination of gain-boosting and chopping demonstrates its ability to achieve micro-volts level offset. Also, chopping is effective in reducing the in-band $1/f$ noise. The work presented in this thesis clearly shows proper optimization of design can deliver high performance and efficient amplifiers.

5.2. Future Work

While the measured signal-to-noise ratio is sufficiently high and quite close to the target specification, a higher SNR can be achieved by using a different g_m control circuit. This is because the current control switch's noise contribution in CSO architecture is equally to that of the input transistors. This adds four extra dominant sources of noise in the design. Thus, the noise performance can be improved by using an alternate g_m control circuit such as tail current regulation [5] [6].

Secondly, as the majority of power is spent to keep amplifier unity-gain stable, the amplifier can be clocked to reduce the power consumption. Especially for zoom ADCs, the amplifier can be synced with f_s to provide a bulk charge to the capacitor in one phase and then be switched-off in other. This will significantly reduce its average power consumption.

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