A Cryo-CMOS Smart Temperature Sensor for the Ultrawide Temperature Range From 5 K to 296 K

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***Abstract*— This work presents a cryo-CMOS smart temperature sensor operating from room temperature down to 5 K. By adopting sensing elements (CMOS bulk diodes, pMOS/DTMOS in weak inversion) that circumvent the poor cryogenic performance of Si BJTs, a robust switched-capacitor second-order sigma–delta readout and cryogenic-aware design techniques, the sensor achieves a maximum error of ±0.73 K (four samples and two-point trim), a resolution below 0.05 K for a 102.4-ms readout duration, and a power consumption of 15.5 µW (93.5 µW) at 5 K (296 K).**

***Index Terms*—Analog to digital conversion, bulk CMOS, CMOS, cryo-CMOS, cryogenic, diode, oversampled, reference, temperature sensor.**

I. Introduction

The demand for cryogenic electronics is continuously increasing in medicine, space applications, and the emerging fields of quantum sensing and quantum computing [1], [2]. As quantum processors typically require cryogenic operation, the availability of an extensive cryogenic electrical interface is a crucial element to enable the scaling of quantum computers to the levels required by practical applications. In those large systems on chip (SoC's), typically operating at 4 K, self-heating and thermal crosstalk can lead to hot spots with a temperature increase of tens of kelvins [3], [4], thus hindering the performance of individual circuit blocks and even affect the performance of the nearby fragile temperature-sensitive qubits. Those effects would only exacerbate with the expected complex hybrid integration schemes currently being developed [5]. For these reasons, on-chip thermal monitoring with individual diodes and off-chip readout is becoming more and more common in cryo-CMOS chips [3], [6]. However, mimicking the dense arrays of temperature sensors used in traditional CPUs would require compact smart sensors [7].

Discrete temperature sensors, such as resistors and diodes, can offer high resolution and high accuracy down to sub-K temperatures after extensive calibration. However, they are bulky, expensive, and extremely challenging to integrate. Thus, the poor thermal contact with the silicon introduces measurement uncertainty. Although CMOS temperature sensors would be the perfect alternative, their operating range is limited to above −70 °C. Prior works have explored the potential of sensing elements at deep cryogenic temperatures [1], [8], [9], [10], [11], but they did not demonstrate the necessary integrated readout [1], [8], [9], required external references [11], or showed characterization limited to one sample [10].

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To bridge this gap, this work demonstrates a cryo-CMOS temperature sensor operating from 5 K to 296 K. The goal is to explore its limitations over such a wide range while attempting to match the sub-1-K accuracy of similar state-of-the-art room-temperature sensors.

II. Proposed Temperature Sensor

A. Sensing Elements

The typically adopted Si BJT's cannot be used below 70 K due to the severely reduced current gain and excessive nonlinearity [12]. Integrated resistors, such as unsilicided polysilicon resistors, diffused resistors, and gate resistors, show a too low sensitivity ($< 0.01\,\%/\mathrm{K}$) below 10 K. Although silicon diodes show a similar drop in performance, their sensitivity remains above $0.2\,\%/\mathrm{K}$ even at 4.2 K with a small enough bias current, making them a potential candidate.

As an alternative, MOSFETs biased in weak inversion emulating the exponential bipolar junction transistor (BJT) behavior can generate a complementary to absolute temperature (CTAT) voltage and a proportional to absolute temperature (PTAT) voltage [9], [12]. Inspired by the cryo-CMOS voltage references in [13], $M_{1,2}$ in Fig. 1 are biased with a constant current ratio p by current mirror $M_{3,4}$. The PTAT voltage $V_{\mathrm{GS2}} - V_{\mathrm{GS1}} = kT/q\,\ln(p)$ drop across R_1 generates a PTAT current mirrored to the output branches to generate the PTAT output voltage V_{ptat} on the matched resistor R_3, and, in combination with the CTAT voltage V_{GS6}, the reference voltage V_{ref}. Separate output branches are used for faster driving of the readout. Similar to [13], dynamic element matching (DEM), omitted from Fig. 1 for clarity (see [13, Fig. 3]), is used to reduce the effect of mismatch, which is expected to worsen at cryogenic temperatures [14]. The resistors R_2 and R_3 are programmable resistor ladders that trim V_{R2}, V_{R3}, for making optimum use of the ADC input range.

The readout digitizes the pMOS-based sensing element in Fig. 1 and a similarly-built P-type DTMOS element. nMOS-based versions have been integrated, but they are not reported because of an unexpected kink at deep cryogenic temperatures degrading their sensitivity and accuracy. In addition, the voltage drop across a 40 µm × 40 µm N+/P-well diode V_{dio} biased by an external current of 100 nA is digitized with respect to an external reference $V_{\mathrm{EXT}} = 1.6$ V.

B. Readout ADC Topology

Fig. 1 shows the second-order switched-capacitor (SC) sigma–delta modulator (SDM) used to sense the generated analog voltages. An SDM has been chosen for its high resolution, as we are targeting an accuracy in the order of 1 K, and compatibility with DEM techniques for the sensing elements. Moreover, an SDM can tradeoff speed and resolution, so as to achieve a more accurate temperature sensor without the need for a change in the design. The SDM can achieve a resolution of 0.03 K for a 102.4-ms conversion time with 10 kHz clock to ensure the SDM does not limit the sensor performance. An SC-adder implements a feed-forward path from the

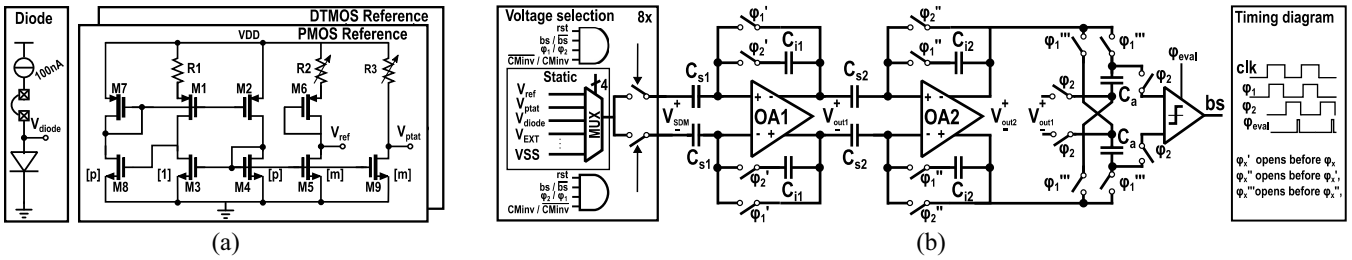

Fig. 1. (a) Overview of proposed sensing elements and (b) readout architecture. The start-up circuit in the pMOS reference in (a) is not shown.

output of the first integrator to the output of the second integrator, thus avoiding the reference required in feedback topologies and minimizing the SDM input loading. An excessive input capacitance could limit the readout speed at cryogenic temperatures due to the low PTAT current delivered by the sensing element.

The charge-balancing scheme presented in [15] is adopted and presented in the timing diagram in Fig. 1. For each of the 1024 SDM cycles used for the readout, the differential SDM input V_{SDM} in φ_1 is reversed in φ_2, so that the integrated voltage is $2V_{\mathrm{SDM}}$, while also canceling the offset. Eight different single-ended voltages are needed to generate the input: two differential inputs for each of the two clock phases for each of the 2 bit streams values. They are statically selected by 8 multiplexers from 16 (4-bit control) possible signals generated by nMOS (2 ×), pMOS (4 ×), DTMOS (4 ×), and external (3 ×) references and 3 × diode types. Digital logic driven by φ_1, φ_2, and the output bit stream bs, dynamically selects the readout input. The same common-mode inversion technique used in [15] is implemented with the CM_{inv} signal. The full digitization cycle is repeated sequentially for each DEM phase of the references and combined in post-processing. Under the charge balancing principle, this leads to an average output bit stream μ given by

$$\mu = \frac{V_0}{V_0 - V_1} \tag{1}$$

where V_0 (V_1) is the input selected when $bs = 0$ ($bs = 1$). Choosing $V_0 = V_{\mathrm{ptat}} - V_{\mathrm{ref}}$, and $V_1 = -V_{\mathrm{ref}}$, for the pMOS/DTMOS element, the digitized ratio is $(V_{\mathrm{ptat}} - V_{\mathrm{ref}})/V_{\mathrm{ptat}}$. The final μ is computed as the average across the different DEM phases. The digitization of the diode voltage is achieved without using DEM techniques by choosing $V_0 = V_{\mathrm{dio}}$, and $V_1 = V_{\mathrm{dio}} - V_{\mathrm{EXT}}$, such that the digitized ratio is $V_{\mathrm{dio}}/V_{\mathrm{EXT}}$.

C. SDM Circuit Implementation

SC implementation is more robust and suitable for designing without a cryogenic compact model. Nevertheless, switches can become limiting at cryogenic temperatures due to the increase of their on-resistance in the mid-rail voltage because of their threshold voltage increase [16]. This design uses thick-oxide nMOS devices supplied with 2.5 V that ensure the on-resistance is sufficiently low in the voltage range of operation (from 0 to 1.6 V) and across temperature. The charge injection introduced by thick-oxide devices was mitigated by adding a thick-oxide pMOS switch, resulting in a pass-gate. Moreover, switches driving common-mode signals are turned off slightly prior to those handling differential signals, by means of a nonoverlapping clock generator. In this way, charge injection errors represent a common-mode error and are effectively canceled.

The lack of accurate simulations at cryogenic temperatures for charge injection mismatch, leakage currents, and other nonidealities, lead to oversize integration capacitors to have sufficient error margin above military range estimations. Moreover, the vast range of possible sensing element signals in this test chip increases the input range of

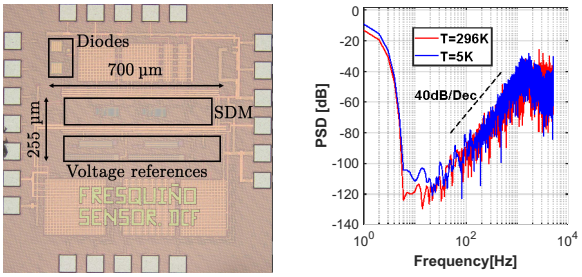

Fig. 2. (a) Chip micrograph and (b) FFT of the output of the DTMOS sensor $(V_{\mathrm{ptat}} - V_{\mathrm{ref}})/V_{\mathrm{ptat}}$. Bitstream measured with a clock frequency of 10 kHz, 10 000 points, Kaiser window.

the SDM and, therefore, the output swing of the operational amplifiers (OAs). The large integrating capacitor also helps circumvent the limitations on the OA's output swing due to the increase of the threshold voltage at cryogenic temperatures. The above considerations lead to $C_{s1} = 1$ pF and $C_{i1} = 10$ pF. The input referred errors of the second OA are less critical, and the swings are attenuated by the first integrator, allowing to scale down the capacitors to $C_{s2} = 0.2$ pF and $C_{i2} = 0.8$ pF. Lastly, the SC adder creates a feedforward coefficient of 2, requiring $C_a = 100$ fF.

The OAs are implemented as conventional folded cascodes architectures with an nMOS input pair, thus ensuring a wide output range and hence smaller integration capacitors. At 300 K, they achieve an open loop gain of 57 dB for a maximum output swing of 300 mV, so that an integrating error of −40 dB can be achieved efficiently and with sufficient margin. A loop gain above 80 dB should keep the leakage error introduced by the amplifiers below 0.03 K when integrating for 1024 cycles, which is sufficiently below the target SDM resolution of 0.1 K. Moreover, the simulated GBW is 25 MHz at 300 K, which provides sufficient settling time when operating the SDM at a clock speed of 10 kHz. At 4 K, the MOS transconductance approximately increases by 2× and the output impedance approximately decreases by 2× [17]. Therefore, a PTAT bias current network similar to the nMOS references presented in [13] was used to bias the amplifiers across temperature. In this way, the changes in transconductance and output impedance will be partially compensated, such that the gain and GBW will not change significantly compared to simulations. The OAs were simulated at 300 K and have an input referred offset of 1.45 mV (3σ), which is reduced by auto-zeroing and by reversing the polarity of the input signals during the two clock phases.

After the SC-adder, a diode-loaded nMOS differential preamplifier is employed to reduce the kickback from the StrongARM comparator, reducing charge injection in the integrating capacitors.

III. Measurement Results

The circuit was fabricated in a 40-nm bulk CMOS technology with an active area of 0.19 mm^2 [Fig. 2(a)] and characterized inside

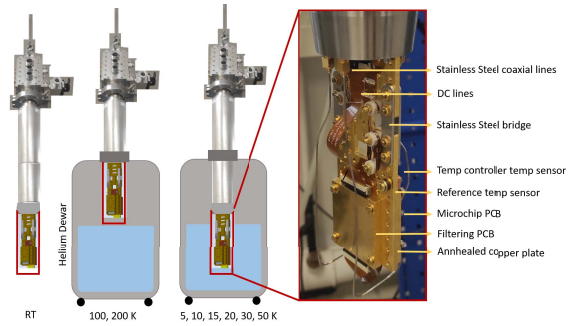

Fig. 3. Measurement setup and close-up of the bottom of the dipstick.

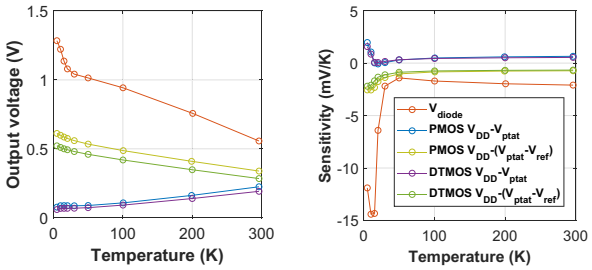

Fig. 4. (a) Sensing element output voltages and (b) sensitivity of each sensing element signal across temperature.

a helium dewar. The measurement data and analysis files are found in [18]. To minimize the temperature measurement errors, the samples were mounted directly on an annealed copper plate for low thermal impedance to the reference temperature sensor. A PCB, a reference temperature sensor, and a resistive heater controlled by a PD controller were also mounted on top of this plate. The plate was attached to a dipstick via a stainless steel bridge for thermal isolation and placed in a vacuum can with pressures below 2 mbar of helium gas in order to keep a weak thermal contact with the helium bath. Thus, the temperature control results from the cooling power given by the liquid helium bath, and the heating power given by the PD-controlled resistive heater. The thermal isolation of the plate and the high thermal conductivity of the annealed copper (residual resistivity ratio higher than 500), ensures that the estimated thermal gradients across the thermal plate are bounded below 12 mK in steady state, as estimated by a thermal analysis considering the geometry and the thermal properties of the materials.

The reference Lakeshore Cernox resistive sensor, calibrated for a 2σ accuracy of ± 4 mK (± 46 mK) at 4.2 K (300 K), has been monitored by a Kelvin connected SMU (Keithley 2636B). Moreover, to reduce the Seebeck effect and the offset of the SMU, the resistance was obtained using reversed current polarities and then averaged. Given the above considerations, the temperature uncertainty of the setup is expected to be below 0.1 K, allowing for accurate measurement of the device under test.

For measuring over such a wide temperature range, measurement close to 296 K was first acquired. Then, the dipstick was introduced into the dewar filled with liquid helium. Inside the dewar, a gradient from 4.2 K (right above the liquid helium surface) to more than 200 K (on the very top of the dewar) is present. The mid-temperature points (100 K and 200 K) were measured by placing the sample PCB at the height of the helium gas. Coarse tuning of the temperature was achieved by varying the height of the sample PCB across the temperature gradient of the helium gas. Fine-tuning was possible thanks to the PD-controlled resistive heater. Lastly, the ultralow

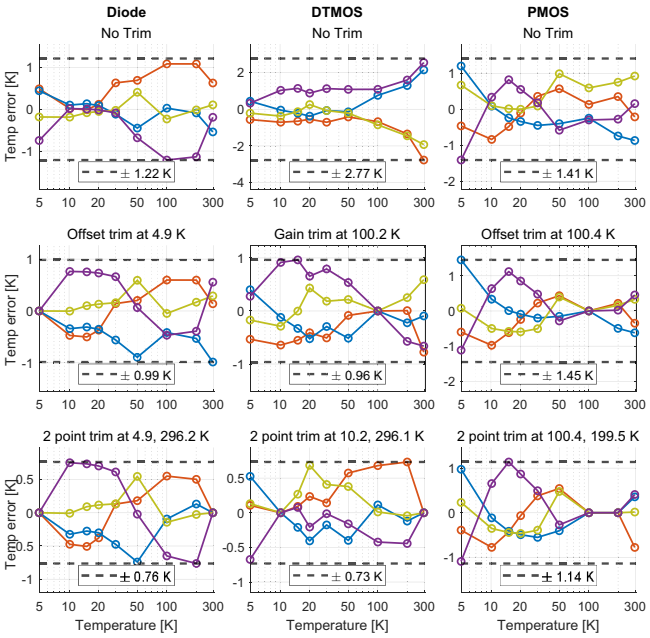

Fig. 5. Temperature to digital conversion accuracy for each sensing element.

TABLE I
MAXIMUM ABSOLUTE ERROR PER SENSING ELEMENT

	Diode		DTMOS[b]		PMOS[b]	
Range (K)	5-296	10-200	5-296	10-200	5-296	10-200
No Trim	±1.22	±1.22	±2.77	±1.6	±1.41	±0.99
1pt trim[a]	±0.99	±1.43	±0.96	±0.96	±1.45	±1.2
2pt trim[a]	±0.76	±0.70	±0.73	±0.46	±1.14	±1.2

[a] Fig.5 shows the trimming points used.
[b] Ratio $(V_{ptat} - V_{ref})/V_{ptat}$.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work			[10]	[11]	[19]
Technology	40 nm			22 nm	130 nm	180 nm
Sensing Element Type	Diode	DTMOS	PMOS	Superconducting	MOS	NPN
External references	Current	None		Current, voltage	Voltage	None
Readout Type	SDM	Bandgap/SDM		Comparator	CTIA+TDC	Bandgap/SDM
Area (mm^2)	0.19			0.015	0.084	0.05
Supply (V)	1.1, 2.5			0.8	1.2 / 3.3	1.4 to 2.2
Temperature Range (K)	5 - 296			0.015 - 1	10 - 410	203 - 398
Resolution RT (5K) in mK	33 (12)	39 (20)	44 (24)	150	295	0.79
Conversion time (ms)	102			-	20	51
Power (μW)	93.5 (RT), 15.5 (5K)			1.5	41	2.5
Energy/Conversion (nJ)	9574 (RT), 1587 (5K)			-	820	128
Trimming points	2			-	2	1
Inaccuracy (K)	±0.76	±0.73	±1.14	-	±1.1 (3σ)	±0.1 (3σ)
Relative PP Inaccuracy (%)	0.5	0.5	0.8	-	0.5	0.1
Samples	4			1	32	40

temperature points (5 K, 10 K, 15 K, 20 K, and 30 K, 50 K) were measured by submerging the structure in the liquid helium, and then controlling the temperature with the PD-controlled resistive heater.

The measured power consumption from the 1.1 V supply decreases at cryogenic temperatures from 93.5 to 15.5 µW due to the PTAT biasing. The (simulated) current drawn from the 2.5-V supply is 137 nA at room temperature (RT). The low power dissipation makes self-heating negligible [4]. By extrapolation of simulations carried out at 300 K, each OA consumes approximately 32.1 µW at 300 K and 5.2 µW at 5 K. All sensing elements are continuously enabled, so as to keep the chip as close as possible to thermal equilibrium. The current in the V_{ref} and V_{ptat} branches in Fig. 1 is estimated to go from 465 to 207 nW over temperature. Because the pMOS/DTMOS sensing outputs are supply-referenced but measured by the SDM with respect to ground, a poor supply rejection of 480 K/V (450 K/V) from 1 V to 1.6 V is obtained at RT (5 K). The SDM achieves a supply sensitivity of -0.1494 K/V (0.0765 K/V) over the same range for the diode readout. The output bitstream spectrum is shown in Fig. 2(b).

The sensing-element outputs measured with an external multimeter and their sensitivity are reported in Fig. 4, showing a largely constant sensitivity down to 50 K, as expected. Most notably, the diode achieves a sensitivity higher than $6\,\mathrm{mV\,K^{-1}}$ at temperatures below 20 K, potentially due to the larger diode size used, leading to reduced self-heating effects. The average bit stream of the conversion ranges from 0.80 to 0.35 (Diode), 0.50 to 0.31 (DTMOS), and 0.60 to 0.39 (pMOS). The sensor accuracy is reported in Fig. 5 and Table I, while Table II compares the results to the state-of-the-art. Results shown for DTMOS and pMOS were obtained using DEM techniques, which improve accuracy by a factor $2\times$ to $8\times$.

IV. Conclusion

This work explores the feasibility of cryo-CMOS smart temperature sensors, showing that accuracy below 2 K can be achieved by bandgap-like sensors that do not require any external references even over the ultrawide range from RT down to 5 K, thus extending the state-of-the-art lower operating range from 200 K to 4 K. Those advances are enabled by the use of weak-inversion MOS sensing elements and a robust SC SDM readout. Although further research is needed to investigate the limits of this approach, the proposed architecture is a promising candidate for the efficient thermal monitoring in cryo-CMOS SoCs as required in future large-scale quantum computers.

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