On-chip output stage design for a continuous class-F power amplifier

Kumaran, Anil Kumar; Pashaeifar, Masoud; D'Avino, Marco; de Vreede, Leo C.N.; Alavi, Morteza S.

DOI
10.1109/ISCAS51556.2021.9401788

Publication date
2021

Document Version
Final published version

Published in
2021 IEEE International Symposium on Circuits and Systems (ISCAS)

On-Chip Output Stage Design for a Continuous Class-F Power Amplifier

Anil Kumar Kumaran*, Masoud Pashaeifar*, Marco D'Avino†, Leo C.N. de Vreede*, and Morteza S. Alavi*
* Electronic Circuits and Architecture (ELCA) Research Group, Delft University of Technology
† Catena B.V., Delft, The Netherlands
Email: a.k.kumaran@tudelft.nl

2021 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-7281-9201-7/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISCAS51556.2021.9401788

***Abstract*—Continuous Class F (CCF) power amplifiers (PAs) overcome Class–F PA's disadvantage of narrow bandwidth by relaxing the short-circuit requirement at the 2^{nd} harmonic while still maintaining 90.7% peak efficiency over the band of interest. This paper proposes four different CCF output networks, with their design procedure, suitable for on-chip implementation in the 2.1–2.7GHz band. The output stage with 2^{nd} harmonic trap and no RF choke is favoured due to its flat real impedance, low fundamental reactance, and compact layout. Using a 40nm CMOS process, a passive efficiency of 68% at 2.4GHz for this structure is in reach.**

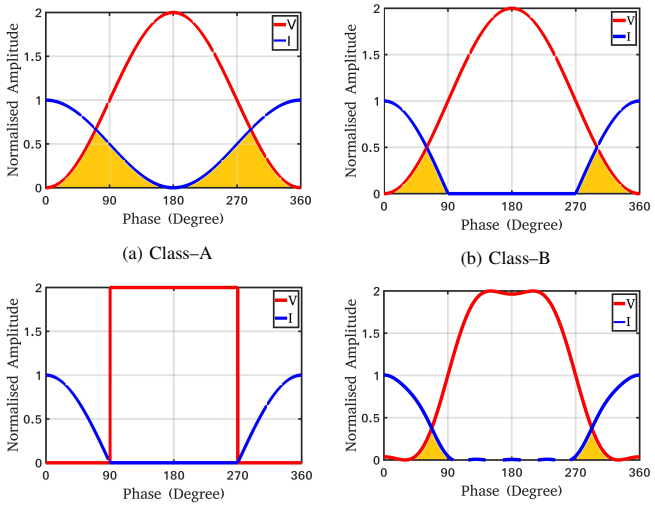
***Index Terms*—Continuous class F (CCF), Output matching network, Power amplifier (PA), Harmonic termination, Differential-mode analysis, Common-mode analysis.**

I. Introduction

Today, there is an increased demand for high-speed, low-cost transceivers in cellular/WLAN wireless networks. A CMOS-based solution is considered to be a viable option to address these requirements since it can facilitate the implementation of a System-on-Chip (SoC) solution at a low cost. However, the TX power amplifier (PA) is generally considered as the most challenging block in a CMOS SoC since it must offer high-efficiency operation while meeting the stringent spectral mask requirements of wireless standards. Currently, most TXs employ linear class A/B PAs. Nevertheless, their ideal peak efficiencies are constrained to 50/78.5%, respectively, due to the relatively large overlap in their drain voltage/current waveforms (Fig. 1a/b).

On the other hand, class–F PAs ideally achieve a peak efficiency of 100% by utilizing harmonic-frequency resonators to short-circuit at even harmonics and open-circuit at odd harmonics leading to non-overlapping drain voltage/current waveforms (Fig. 1c). Nonetheless, in reality, controlling all harmonics is challenging and increases the network complexity and component losses, as such degrading its passive efficiency. Therefore, practical implementation of class–F PAs employ up to three harmonics and can ideally achieve a peak efficiency up to 90.7% (Fig. 1d) [1]. The generalized drain-source-voltage (V_{DS}) containing all frequencies up to 3^{rd} harmonic [2] is given by:

$$V_{DS} = \underbrace{1}_{\text{DC}} - \underbrace{\frac{2}{\sqrt{3}}\cos\theta}_{1^{st}\text{ harmonic}} + \underbrace{\frac{1}{3\sqrt{3}}\cos 3\theta}_{3^{rd}\text{ harmonic}} \quad (1)$$



(a) Class–A (b) Class–B (c) Ideal Class–F (d) Practical Class–F

Fig. 1: Class–A/B/F drain voltage/current (V/I) waveforms.

The drain current (I_D), which is a half-sine wave, is given by

$$I_D = \underbrace{\frac{1}{\pi}}_{\text{DC}} + \underbrace{\frac{1}{2}\cos\theta}_{1^{st}\text{ harmonic}} + \underbrace{\frac{2}{3\pi}\cos 2\theta}_{2^{nd}\text{ harmonic}} - \underbrace{\frac{2}{15\pi}\cos 4\theta}_{4^{th}\text{ harmonic}} \quad (2)$$

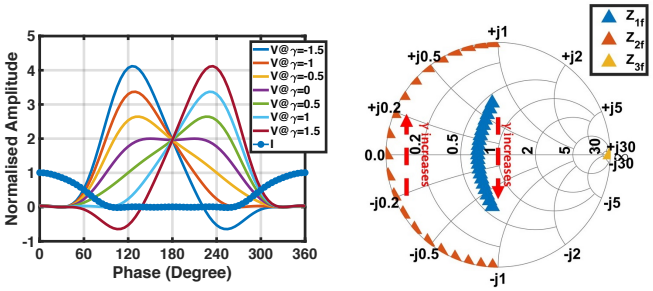
where θ is the fundamental phase. The load impedances at the 1^{st}, 2^{nd}, and 3^{rd} harmonic are represented by $Z_{1f} = \frac{4}{\sqrt{3}}$, $Z_{2f} = 0$, and $Z_{3f} = \infty$, respectively. As depicted in Fig. 1d, one of the key advantages of class–F PAs is that its normalised peak drain voltage is two. Nonetheless, these traditional class–F PAs suffer from bandwidth limitations (typically up to 10% relative bandwidth) due to their dependence on ideal short and open circuit harmonic terminations. To realize larger bandwidths, the continuous class–F (CCF) PA has been proposed [3]. In this work, we present and evaluate four different output network topologies, all suited to implement CCF operation.

This paper is organized as follows. Section II briefly explains the equations governing the operation of CCF. Section III discusses the design procedure of different CCF output networks. Section IV compares the proposed four output stages, and presents layout of the chosen design. Section V concludes this paper.

II. Continuous Class-F

Compared to class–F, the CCF operation allows an extra imaginary part at both its 1^{st}/2^{nd} harmonic of the voltage

978-1-7281-9201-7/21/$31.00 ©2021 IEEE



(a) (b)

Fig. 2: (a) V_{DS} and I_D waveform for CCF with -1.5 < γ < 1.5, and (b) Variation of Z_{1f}, Z_{2f}, Z_{3f} for -1 < γ < 1.

waveform. Thus, the generalized V_{DS} for CCF is given by [4]:

$$V_{DS} = \underbrace{1}_{\text{DC}} - \underbrace{\frac{2}{\sqrt{3}}\cos\theta - \gamma\sin\theta}_{1^{st}\text{ harmonic}} + \underbrace{\frac{7\gamma}{6\sqrt{3}}\sin 2\theta}_{2^{nd}\text{ harmonic}} + \underbrace{\frac{1}{3\sqrt{3}}\cos 3\theta}_{3^{rd}\text{ harmonic}} \tag{3}$$

where γ is an empirical parameter. As in class–F, I_D is a half sinusoid [given in (2)]. These equations indicate that V_{DS}/I_D are chosen so that no power is dissipated at higher harmonics. Also, mathematically, γ in (3) does not affect the drain efficiency (η_D), but it does affect the peak drain voltage, as depicted in Fig. 2a. However, I_D depends on V_{DS}, degrading η_D as γ increases.

Fig. 2a implies that at γ = 0, the waveform is like class–F. For the γ values between -1 and 1, V_{DS} remains positive, enabling CCF PA to meet linearity requirements. However, CCF PAs suffer from large peak drain voltage swings, which can be as high as 3.34 times the supply (V_{DD}) when γ = -1 or 1. Using (3) and (2), the load impedances of CCF are $Z_{1f} = \frac{4}{\sqrt{3}} + j2\gamma$, $Z_{2f} = 0 - j\frac{\pi}{2}\frac{7\sqrt{3}}{6}\gamma$, and $Z_{3f} = \infty$ [5].

In CCF, Z_{3f} remains open-circuited similar to class–F. Meanwhile, Z_{1f} and Z_{2f} have a reactive part, unlike class–F. From CCF load impedances and Fig. 2b, it is perceived that if the reactive part of Z_{1f} changes from inductive (+) to capacitive (-), then the reactive part of Z_{2f} needs to change from capacitive (-) to inductive (+) or vice-versa across the bandwidth, to achieve CCF operation. In the next section, the design procedure for the proposed four output networks is meticulously presented.

III. Design of Output Network for CCF

In this work, the push-pull (differential) structure is chosen for the PA, mainly because it decouples the odd harmonics (1^{st}/3^{rd}) from even harmonic (2^{nd}) impedance. Moreover, it suppresses supply/substrate noise, second-order nonlinearities and doubles the RF output power for a given breakdown voltage. In this work, the targeted peak RF power is 27dBm while its operational bandwidth is 2.1–2.7GHz with V_{DD} = 2.7V. To achieve this, a fundamental differential impedance of 38.7Ω should be presented to the drains of the transistors across the 2.1–2.7GHz band, which can be obtained as follows:

TABLE I: OUTPUT NETWORK SPECIFICATIONS.

Class of Operation	First Harmonic (ω)	Second Harmonic (2ω)	Third Harmonic (3ω)
Class F (2.4GHz)	$\Re(Z_D)$ = 38.7Ω	$\Re(Z_D)$= 0Ω	$\lvert Z_D\rvert \approx$ 1000Ω
	$\Im(Z_D)$ = 0Ω	$\Im(Z_D)$ = 0Ω	
CCF (2.1–2.7GHz)	$\Re(Z_D)$ = 38.7Ω	$\Re(Z_D)$ = 0Ω	$\lvert Z_D\rvert \approx$ 1000Ω
	$\Im(Z_D) \rightarrow$ + to - OR $\Im(Z_D) \rightarrow$ - to +	$\Im(Z_D) \rightarrow$ - to + OR $\Im(Z_D) \rightarrow$ + to -	

$$V_{FUND-diff} = 2 \times V_{FUND-single} = 2 \times \frac{2}{\sqrt{3}} V_{DD} = 6.24\ V$$
$$R_{D-diff} = \frac{V^2_{FUND-diff}}{2 \times P_{OUT_{max}}} = 38.7\ \Omega \tag{4}$$

The requirements of the output network for CCF are exhibited in Tab. I. The PA operates in class–F mode at the center frequency ω_0 (2.4GHz) with a short at $2\omega_0$ (4.8GHz) and an open at $3\omega_0$ (7.2GHz). But, for all other frequencies, the PA performs in the CCF mode.

The four different output networks proposed are based on lumped passive components, see Fig. 3a/b/c/d. All the designs include a balun and load capacitance (C_L). The balun converts the balanced (differential) signal to its single-ended companion, whereas C_L adjusts the 3^{rd} harmonic impedance. The power transistor's drain-source capacitance (assumed C_{DS} = 1.87pF) is absorbed into the output network to reduce its impact on the PA performance. The balun is modeled using an ideal transformer, consisting of magnetizing inductance (L_m), leakage inductance (L_k), primary inductance (L_P), and coupling coefficient (k_m) [6].

A. Design A (no RF Choke & with L_2C_2)

Design A (Fig. 3a) includes a 2^{nd} harmonic trap (L_2C_2), which provides short at $2\omega_0$. The V_{DD} is supplied through the balun's center tap, and L_{BND} is used to model the bond-wire inductance (≈1nH). Analysis of the schematics is performed in differential-/common-mode scenarios by utilizing the equivalent circuits depicted in Fig. 3a.1/a.2, respectively, to calculate the unknown parameters: transformer's coupling factor (k_m) and turn ratio (n) along with L_P, C_2, L_2, and C_L. Fig. 3a.1 shows that the drain impedance (Z_D) is given by

$$Z_D = \left(\frac{1}{\frac{j\omega C_{DS}}{2}} + \frac{1}{Z_{SB}}\right)^{-1} = 38.7\ \Omega \tag{5}$$

The value of Z_{SB} [impedance of L_2C_2 and balun given by (6)] that will provide Z_D of 38.7Ω can be calculated from (5) and the value is $\Re(Z_{SB})(\omega_0) = 29.8\Omega$ and $\Im(Z_{SB})(\omega_0) = 16.6\Omega$.

$$Z_{SB} = \left(\frac{1}{Z_B} + \frac{1}{Z_S}\right)^{-1} \text{ where, } Z_S = 2j\omega L_2 + \frac{1}{\frac{j\omega C_2}{2}},$$
$$Z_B = \left(\frac{1}{R_P} + \frac{1}{2j\omega L_m} + j\omega C_P\right)^{-1} + 2j\omega L_k, \tag{6}$$
$$R_P = R_L\left(\frac{k_m}{n}\right)^2, C_P = C_L\left(\frac{n}{k_m}\right)^2$$

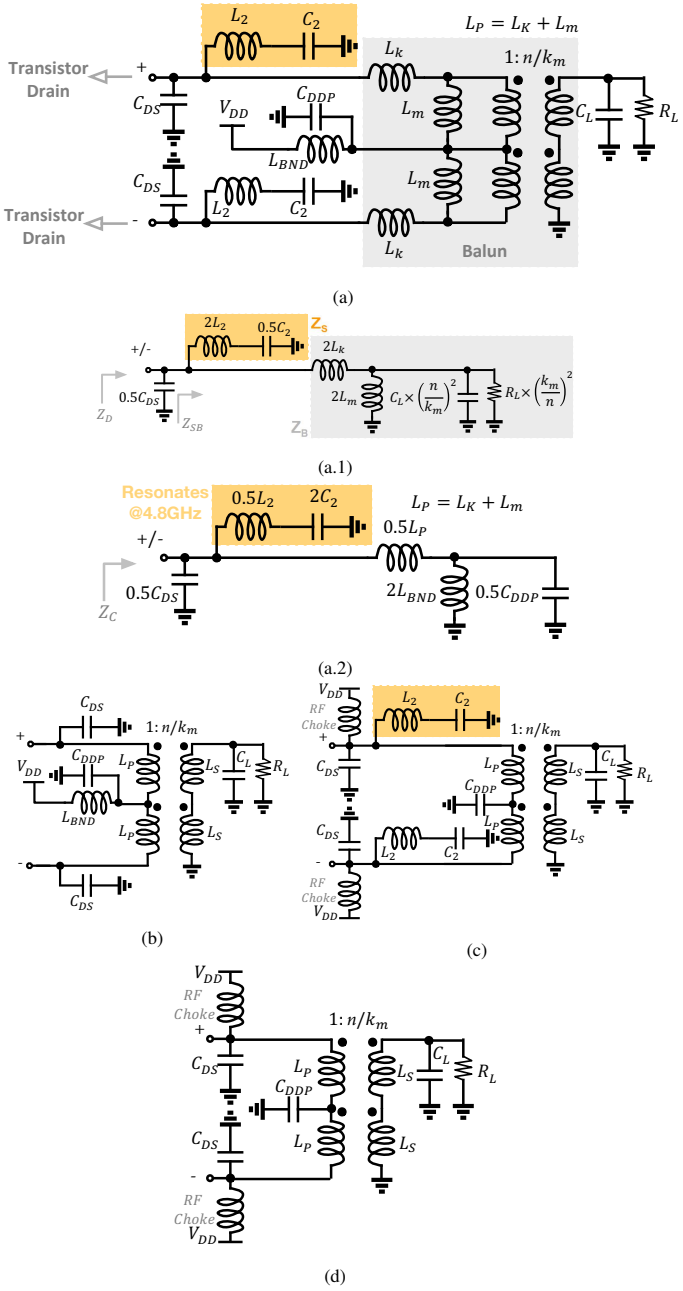
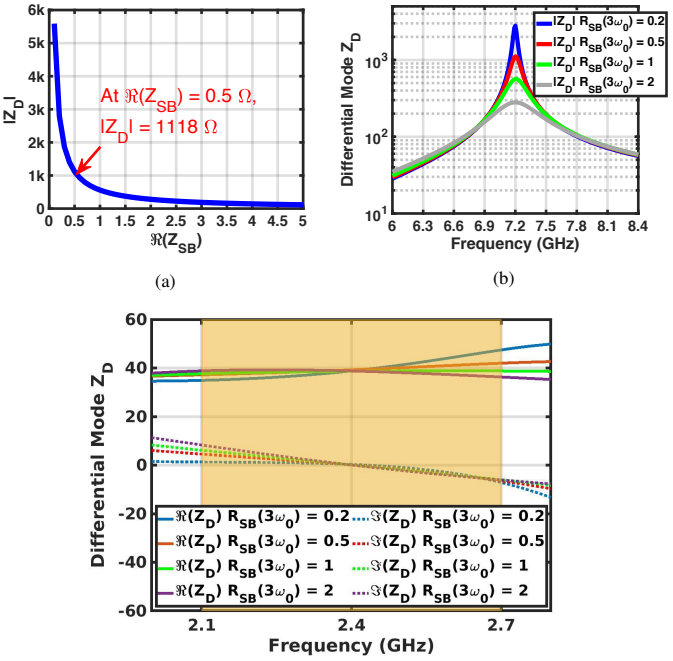


Fig. 3: (a) Design A (Balun, L_2C_2 and C_L), (a.1) odd-mode, (a.2) even-mode equivalent circuit (b) Design B (Balun and C_L), (c) Design C (Balun, RF choke, L_2C_2 & C_L), and (d) Design D (Balun, RF choke & C_L).

It is evident from (5) that C_{DS} should resonate with $\Im(Z_{SB})$ to attain high drain impedance at $3\omega_0$. This implies $\Im(Z_{SB})(3\omega_0) = 24.96\Omega$. Ideally, $\Re(Z_{SB})(3\omega_0)$ should be 0Ω to achieve high 3^{rd} harmonic impedance. However, Fig. 4c depicts that having a larger $\Re(Z_{SB})(3\omega_0)$ contributes to a constant P_{OUT} across the operational bandwidth by flattening the real part at the fundamental. Another benefit is that it has a more linear reactive part at the fundamental, which is essential in CCF operation. However, this leads to a lower 3^{rd} harmonic impedance, as showcased in Fig. 4b. This also emphasizes the significance of C_L. Thus, to achieve an open circuit at the 3^{rd} harmonic, an impedance of approximately 1000Ω is required



(a) (b) (c)

Fig. 4: (a) Magnitude of Z_D vs real part of Z_{SB} ($\Re(Z_{SB})$) at $3\omega_0$, (d) Magnitude of Z_D at 3^{rd} harmonic for various $R_{SB}(3\omega_0)$, and (c) Z_D at fundamental for various $R_{SB}(3\omega_0)$.

which is obtained with $\Re(Z_{SB})(3\omega_0) = 0.5\Omega$ (Fig. 4a). Fig. 3a.2 proves that L_2 should have a series resonance with C_2 to get short at $2\omega_0$.

$$L_2 = \frac{1}{4 \times \omega_0^2 \times C_2} \tag{7}$$

The five unknowns in the circuit: k_m, n, L_P, C_2, and C_L can be calculated by assuming one of them and using four equations [$\Re(Z_{SB})(\omega_0) = 29.8\Omega$, $\Im(Z_{SB})(\omega_0) = 16.6\Omega$, $\Re(Z_{SB})(3\omega_0 = 0.5\Omega$ and $\Im(Z_{SB})(3\omega_0) = 24.96\Omega$]. In this work, $k_m = 0.69$ is assumed and the remaining unknowns ($n = 1$, $L_P = 0.8$nH, $C_L = 2.4$pF, $C_2 = 0.8$pF, $L_2 = 1.4$nH) are calculated. k_m can be varied to get different sets of results in which L_P is minimal and thereby making the layout friendly.

B. Design B (no RF Choke & no L_2C_2)

In this design (Fig. 3b), L_2C_2 is removed, reducing the number of unknowns. Like the previous case, differential mode analysis yields four equations, and there are four unknowns, thus leading to a single set of values for $k_m = 0.72$, $n = 0.9$, $L_P = 0.63$nH, $C_L = 3.96$pF, unlike design A. C_{DDP} is tuned to provide a short at $2\omega_0$ such that C_{DDP} resonates with L_P, L_{BND}, and C_{DS}, which is obtained from the common-mode analysis. Moreover, C_{DDP} provides RF ground and blocks DC.

C. Design C (with RF Choke & with L_2C_2)

In this design (Fig. 3c), V_{DD} is supplied through a RF choke, unlike the previous designs. RF chokes are assumed to have a fixed value of 5nH. The differential mode analysis yields four equations similar to design A. Assuming $k_m = 0.73$, the other unknowns are calculated as $n = 0.93$, $L_P = 0.95$nH, $C_L = 2.5$pF, $C_2 = 0.61$pF. Like design A, C_2 should resonate out with L_2 to get short at $2\omega_0$. Thus, $L_2 = 1.8$nH.

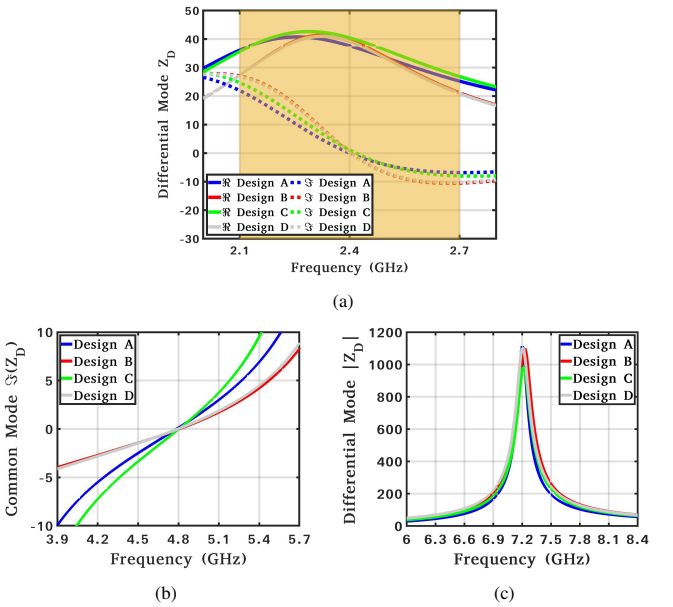


Fig. 5: (a) Impedance (Z_D) at 1^{st} harmonic, (b) Reactive part of Z_D ($\Im(Z_D)$) at 2^{nd} harmonic, and (c) Magnitude of Z_D ($|Z_D|$) at 3^{rd} harmonic.

D. Design D (with RF Choke & no L_2C_2)

Unlike design C, L_2C_2 is removed in this design (Fig. 3d). Also, the RF choke should be calculated, assuming C_{DS} resonates with it at ω_0 (RF choke = 2.35nH). The differential mode analysis yields four equations and the four unknowns ($n = 0.84$, $L_P = 0.86$nH, $C_L = 3.95$pF, $k_m = 0.77$) can be calculated. C_{DDP} can be tuned to provide a short at $2\omega_0$.

IV. Results

Fig. 5 shows that all the four designs satisfy the main CCF requirement, which is a decreasing trend of the reactive part at the fundamental and increasing trend of the reactive part at 2^{nd} harmonic. As illustrated in Fig. 5a, the real part in the desired frequency band is flatter for design A/C, which leads to constant P_{OUT}, unlike design B/D. Moreover, to fully accomplish CCF operation, the series L_2C_2, which resonates at the 2^{nd} harmonic, acts as a capacitor at the desired band. The designs B/D have a higher reactive part at the fundamental than other designs, contributing to a larger γ value and, thus, higher peak drain voltage (Fig. 2a). Fig. 5b/c show that all designs have a similar response at $2^{nd}/3^{rd}$ harmonics. Nevertheless, design A generates a more constant P_{OUT} in the band of interest and allows the use of compact passive components.

To verify the proposed output passive stage design approach, design A is laid out in an LP 40nm CMOS process (Fig. 6) with a $600\mu m$ balun. Subsequently, design A is simulated in three different ways: as a lossless network, with losses using a quality factor of 7/13/100 for the inductors/balun/capacitors, respectively, and as the proposed layout. The ADS (Momentum) simulation results are depicted in Fig. 7, which indicates a good agreement between the lossy and the proposed layout, reaching 68% passive efficiency at 2.4GHz. Moreover, using an ideal push-pull PA, the proposed design achieves peak

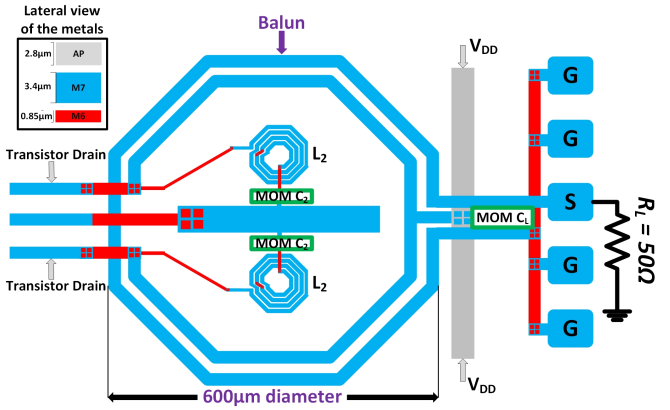


Fig. 6: Layout of the design A (balun, L_2C_2 and C_L).

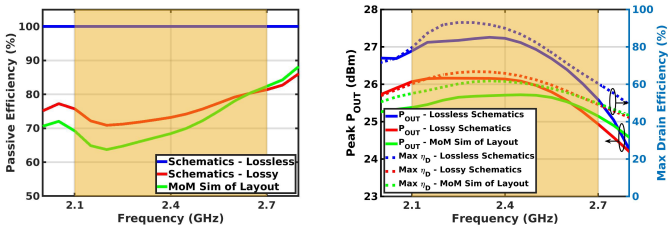


Fig. 7: (a) Passive efficiency, and (b) Maximum P_{OUT} and drain efficiency versus frequency band.

RF output power/drain efficiency of more than 25dBm/62%, respectively, over the desired frequency band.

V. Conclusion

In this paper, the primary advantage of CCF PAs over its class–F companion, as well as the critical requirement needed for the output network to operate in CCF mode are presented. Furthermore, the design procedure of various output networks for the 2.1–2.7GHz band is presented, and the proposed passive output stages are synthesized. The 2^{nd} harmonic trap, which acts as a varying capacitor at 1^{st} harmonic, helps in maintaining constant output RF power in the desired frequency band for the design A/C. Consequently, design A, with no RF choke and a 2^{nd} harmonic trap is chosen since it has minimal on-chip passive components. This design is laid out in a 40nm CMOS while achieving a 68% passive efficiency at 2.4GHz.

References

[1] F. H. Raab, "Maximum efficiency and output of class-F power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1162–1166, June 2001.

[2] S. C. Cripps, *et al.*, "On the Continuity of High Efficiency Modes in Linear RF Power Amplifiers," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 10, pp. 665–667, 2009.

[3] J. Chen, *et al.*, "Design of Broadband High-Efficiency Power Amplifiers Based on a Series of Continuous Modes," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 9, pp. 631–633, Sep. 2014.

[4] V. Carrubba, *et al.*, "On the Extension of the Continuous Class-F Mode Power Amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1294–1303, May 2011.

[5] S. N. Ali, *et al.*, "A 25–35 GHz Neutralized Continuous Class-F CMOS Power Amplifier for 5G Mobile Communications Achieving 26% Modulation PAE at 1.5 Gb/s and 46.4% Peak PAE," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 2, pp. 834–847, Feb 2019.

[6] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, 2000.