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ABSTRACT

We grow ^{28}Si/SiGe heterostructures by reduced-pressure chemical vapor deposition and terminate the stack without an epitaxial Si cap but with an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. As a result, ^{28}Si/SiGe heterostructure field-effect transistors feature a sharp semiconductor/dielectric interface and support a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 mm wafer. At $T = 1.7$ K, we measure a high mean mobility of $(1.8 \pm 0.5) \times 10^5$ cm^2/V s and a low mean percolation density of $(9 \pm 1) \times 10^{10}$ cm^{-2}. From the analysis of Shubnikov–de Haas oscillations at $T = 190$ mK, we obtain a long mean single particle relaxation time of (8.1 ± 0.5) ps, corresponding to a mean quantum mobility and quantum level broadening of $(7.5 \pm 0.6) \times 10^4$ cm^2/V s and (40 ± 3) μeV, respectively, and a small mean Dingle ratio of (2.3 ± 0.2), indicating reduced scattering from long range impurities and a low-disorder environment for hosting high-performance spin-qubits.

Strained ^{28}Si/SiGe heterostructures are a compelling platform for scalable qubit tiles based on gate-defined quantum dots.[1,2] In these ^{28}Si buried quantum wells, electron spins experience a quiet electrical and magnetic environment. The electronically noisy semiconductor/dielectric interface is far away, separated from the quantum well by a SiGe epitaxial barrier, and the nuclear spins have been removed by isotopic enrichment. Continuous advances in the materials science of ^{28}Si/SiGe and improved device fabrication have enabled quantum logic with spin qubits crossing the surface code threshold,[3–5] coherent coupling of two electron spins at a distance via virtual microwave photons,[6] and CMOS-based cryogenic control of quantum circuits.[7] In the mainstream approach to quantum dot fabrication, the last step in the heterostructure growth cycle comprises the heteroepitaxial deposition of a thin epitaxial Si cap on the SiGe barrier.[8] This is to avoid the formation of low-quality Ge-based oxides upon exposure of SiGe to air. After the Si cap deposition, a high-κ dielectric is deposited *ex situ* and at low-temperature (≈300 °C) to insulate the gate from the buried and undoped quantum well. This low-temperature process preserves the strain in the quantum well but induces large concentrations of impurities at the critical semiconductor/dielectric interface. These impurities can influence the electrostatic confining potential landscape induced by the gates, leading to the formation of unintentional quantum dots[9] and are a source of charge noise limiting qubit performance.[10,11] While efforts have focused on achieving uniform and high-purity ^{28}Si quantum wells with sharp interfaces,[12–14] now much attention is needed to optimize the step, which terminates the heterostructure deposition cycle and has a critical role in defining the semiconductor/dielectric interface.

In this Letter, we explore ^{28}Si/SiGe heterostructures terminated by exposure to dichlorosilane (DCS) gas at a temperature well below the threshold for epitaxial growth of Si. By avoiding the growth of an epitaxial Si cap altogether, we obtain ^{28}Si/SiGe heterostructure field effect transistors (H-FETs) with a sharp semiconductor/dielectric interface. We show that the ^{28}Si quantum well supports a two-dimensional electron gas (2DEG) with less disorder and improved quantum transport properties compared to heterostructures with an epitaxial Si cap.

Figure 1(a) illustrates the workflow to fabricate ^{28}Si/SiGe H-FETs. We grow ^{28}Si/SiGe heterostructures on 100 mm Si(001) wafers using an Epsilon 2000 (ASMI) reduced-pressure chemical vapor deposition reactor. We use isotopically enriched $^{28}SiH_4$ for growing the ^{28}Si quantum well [residual ^{29}Si concentration of 0.08% (Refs. 3, 7, and 15)] and DCS (H_2SiCl_2) and GeH_4 for all other layers. The heterostructure comprises a 3 μm step-graded $Si_{1-x}Ge_x$ layer

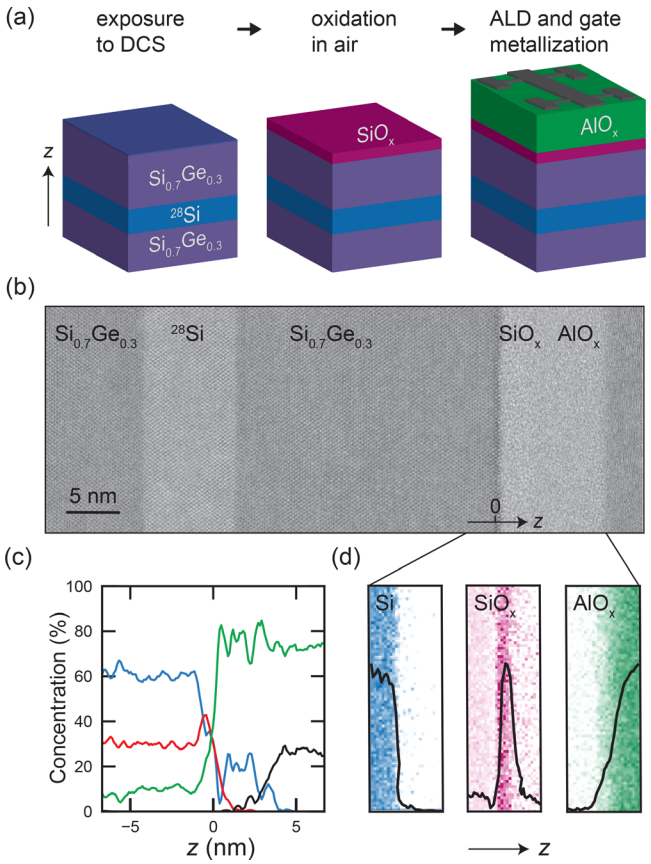

FIG. 1. (a) Schematics of the ^{28}Si/SiGe heterostructure and formation of the dielectric interface in a Hall-bar heterostructure field effect transistor. *z* indicates the heterostructure growth direction. The heterostructure is terminated by exposure to dichlorosilane (DCS) gas at a temperature below the threshold for growing an epitaxial Si cap and the dielectric stack comprises a SiO_x layer formed by exposure of the heterostructure to air at room temperature and an AlO_x layer formed by atomic layer deposition (ALD). (b) BF-STEM image of the active layers of the ^{28}Si/SiGe heterostructure field effect transistor showing, from left to right, the $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer layer, the tensile-strained ^{28}Si quantum well, the $Si_{0.7}Ge_{0.3}$ barrier, followed by the SiO_x/AlO_x dielectric stack. (c) Electron energy loss spectroscopy (EELS) semi-quantitative concentration depth profiles across the semiconductor/dielectric interface for Si (blue), Ge (red), O (green), and Al (black). (d) 15×45 nm^2 wide 2D maps by EELS using low-energy edges to recognize differences between the different bonding states: Si (blue), SiO_x (magenta), and AlO_x (green). We do not detect any Cl or H signal above the background noise in our EELS data.

(final $x \simeq 0.3$), a 2.5 μm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer, a 8 nm tensile-strained ^{28}Si quantum well, and a 30 nm $Si_{0.7}Ge_{0.3}$ barrier[16] and in the SiGe barrier is $\simeq 4 \times 10^{17}$ cm^{-3}. To achieve sharp interfaces and minimize Si/Ge interdiffusion at the quantum well–barrier interface,[12] the temperature is decreased from 750 °C for growing the quantum well to 625 °C for the barrier. We now introduce a major difference compared to our previous experiments. In Refs. 3, 7, 12, and 17, we deposited a thin epitaxial Si cap at 675 °C using DCS. Here, we reduce the substrate temperature to 500 °C, below the desorption temperature of chlorine from the surface (600–650 °C),[18,19] under the same conditions of the DCS flow and pressure. According to the literature,[20–26] we expect that exposure to DCS at 500 °C essentially suppresses crystalline growth but creates an amorphous Si-rich layer on $Si_{0.7}Ge_{0.3}$. After terminating the deposition cycle with this step, the heterostructure is removed from the growth reactor and a native oxide is formed upon exposure to air at room temperature. We identify the native oxide as SiO_x based on the chemical analysis in Figs. 1(c) and 1(d). Then, we fabricate Hall-bar shaped H-FETs using the process described in Ref. 12. In short, the process comprises the implantation of Ohmic contacts and rapid thermal annealing at 700 °C, the atomic layer deposition (ALD) at 300 °C of a 10 nm Al_2O_3 dielectric layer on the SiO_x, and the final deposition of a Hall-bar shaped metallic gate, electrically insulated from the heterostructure by the SiO_x/Al_2O_3 dielectric stack.

Figure 1(b) shows a bright-field scanning transmission electron microscopy (BF-STEM) image of the heterostructure and of the dielectric stack under the gate stack at the end of the H-FET fabrication process. The Si quantum well is uniform, without extended defects, and is characterized by sharp top and bottom interfaces to the $Si_{0.7}Ge_{0.3}$ layers, in agreement with our previous reports.[3,7,12] The semiconductor/dielectric interface is similarly sharp, highlighted by the perfect atomically sharp semiconductor surface as imaged by BF-STEM. Two distinct amorphous layers, which we identify as the SiO_x and AlO_x layers, appear on the dielectric side of the interface. We gain insights over the nature of the semiconductor/dielectric interface and of the dielectric stack by performing electron energy loss spectroscopy (EELS) (supplementary material). In Fig. 1(c), we show the semi-quantitative concentration profiles using the Si–K (1839–2084 eV), Al–K (1560–1700 eV), O–L (532–660 eV), and Ge–L (1220–1400 eV) high energy edge. The Si (blue) and Ge (red) concentration profiles decrease together while the oxygen (green) signal is increasing. We deduce that oxidation of the $Si_{0.7}Ge_{0.3}$ barrier with on top an amorphous Si-rich layer results in a sharp SiGe/SiO_x semiconductor/dielectric interface. This is confirmed by the minor Ge pileup on the semiconductor side of the interface,[27,28] which appears as a dark line in BF-STEM [Fig. 1(b)] and suggests that the top of the single crystalline $Si_{0.7}Ge_{0.3}$ barrier has been oxidized and that Ge oxides at the interface are absent.[29,30] Furthermore, the Al signal (black line) rises after the Si signal from SiO_x has trailed, indicating that the dielectric stack retains the two distinct SiO_x and AlO_x layers.

In Fig. 1(d), we show the chemical mapping by EELS of Si (blue), SiO_x (magenta), and AlO_x (green) along and across the semiconductor/dielectric interface, together with the intensity profiles. To recognize differences between the different bonding states, we use the low-energy Si–L edge (96.3–100.8 eV) for the semiconductor phase and a shifted Si–L edge (101.4–107.1 eV) for the oxide phase, and Al–L (73.8–79.5 eV) for the oxide Al phase. The SiGe/SiO_x interface is sharp throughout the image, whereas the SiO_x/AlO_x interface shows some interdiffusion. By fitting the intensity profiles with exponential functions,[31] we characterize the size of the interfaces with the leading (towards the surface) and trailing (from the surface) exponential slopes λ_L and λ_T. We find $\lambda_L^{Si} = (1.0 \pm 0.1)$ nm and $\lambda_T^{SiO_x} = (0.8 \pm 0.1)$ nm. Conversely, we find $\lambda_L^{SiO_x} = (1.9 \pm 0.1)$ nm and $\lambda_T^{AlO_x} = (3.1 \pm 0.2)$ nm. Overall, the transition from epitaxial SiGe to amorphous SiO_x interface is sharper than the transition between SiO_x and AlO_x, pointing to a degree of intermixing at the latter interface.

We characterized the H-FETs by magnetotransport measurements at a temperature of 1.7 K and 190 mK (Ref. 32) in refrigerators equipped with cryo-multiplexers.[33] With this approach, we measure

multiple devices from a wafer in the same cooldown. The devices are operated in accumulation mode in which electrons populate the undoped ^{28}Si quantum well by applying a positive DC gate voltage (V_G). We measure the longitudinal and transverse components of the resistivity tensor, ρ_{xx} and ρ_{xy}, by using standard four-probe lock-in techniques at fixed AC source-drain bias of 100 μV. We calculate the longitudinal σ_{xx} and transverse σ_{xy} conductivity via tensor inversion. We measure electron density (n) and mobility (μ) with the classical Hall effect at low perpendicular magnetic field B.

Figure 2(a) shows for a typical device the turn-on and pinch-off source-drain current I_{SD} as a function of increasing and decreasing V_G, respectively. Above a threshold voltage ($V_G = 350$ mV), the current starts flowing in the channel and increases monotonically. If the gate voltage is operated within the operational gate voltage range ΔV_G (red curve), I_{SD} is stable and the threshold and pinch-off voltages overlap. At higher V_G, I_{SD} saturates due to charge build-up at the semiconductor/dielectric interface, triggering hysteresis and, consequently, a shift in pinch-off voltage. As shown in Fig. 2(b), if V_G is swept within the operational gate voltage range, n increases linearly with V_G up to 6×10^{11} cm^{-2}. From the slope $\frac{dn}{dV_G}$, we derive an effective capacitance per unit area $C \simeq 205$ nF/cm^2 using the relationship $C = e\frac{dn}{dV_G}$.[33] This capacitance characterizes the parallel-plate capacitor where the 2DEG in the ^{28}Si quantum well and the metallic top gate are insulated by a SiGe/SiO_x/AlO_x dielectric stack. Figure 2(c) shows the density-dependent mobility measured in the same density range as in Fig. 2(b). In the low density regime ($n \leq 3 \times 10^{11}$ cm^{-2}), the mobility rises steeply due to the increasing screening of Coulomb scattering from remote charged impurities located at the semiconductor/dielectric interface.[34] At higher density ($n \geq 5 \times 10^{11}$ cm^{-2}), the mobility approaches saturation at a value above 2.5×10^5 cm^2/V s. This weaker density-dependence is typical of a high-quality 2DEG, where the maximum mobility is limited by short-range scattering from impurities within or near the quantum well.[33,35,36]

In Figs. 2(d)–2(f), we plot the distributions of the maximum electric field (E_z^{max}), the percolation density (n_p), and the mobility at high density for heterostructures terminated with an amorphous Si-rich layer (blue) and, as a benchmark, for heterostructures with an epitaxial Si cap (red). These three metrics are obtained from the analysis of measurements in Figs. 2(a)–2(c), repeated on multiple H-FETs on dies that are randomly selected from different locations across the 100 mm wafer. E_z^{max}, calculated as $C\Delta V_G/\epsilon_0\epsilon_r$, where $\epsilon_r = 11.68$ is the dielectric constant of Si, indicates the maximum electric field that we can apply to the quantum well in the H-FETs before hysteresis. Large E_z^{max} are desirable for device stability, increased tunability, and large valley splitting.[12,14,37,38] n_p characterizes disorder in low density regime, relevant for quantum dot operation, and is obtained by fitting the density-dependent σ_{xx} to percolation theory.[39] Finally, the mobility at high density is a probe for disorder arising from within or nearby the

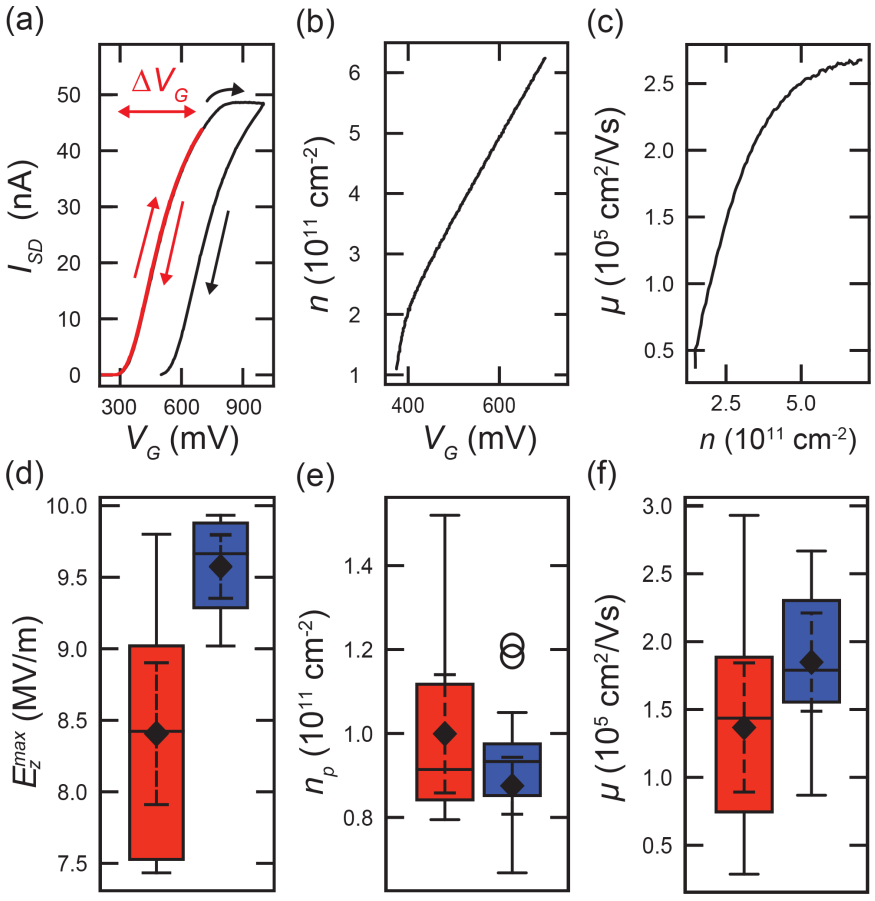

FIG. 2. (a) Source–drain current I_{SD} measured at $T = 1.7$ K as a function of gate voltage V_G for a typical Hall bar heterostructure field effect transistor (H-FET). The operational gate voltage range ΔV_G indicates the range over which an I_{SD}–V_G curve (red line) can be measured repeatedly without hysteresis and drift. (b) Density n as a function of gate voltage V_G and (c) electron mobility μ as a function of n measured within the operational gate voltage range. (d)–(f) Distributions of maximum electric field applicable before hysteresis E_z^{max}, percolation density n_p, and μ measured at $n = 6 \times 10^{11}$ cm^{-2} for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 14 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 16 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.

quantum well.[34–36] Overall, H-FETs perform better when the SiGe barrier is terminated with an amorphous Si-rich layer. We measure a 9% increase in mean E_z^{max}, 7% decrease in mean percolation density, and a 40% increase in mean mobility. Most importantly, we observe a reduction in the spread of E_z^{max}, n_p, and μ of $\simeq$300%, $\simeq$200%, and $\simeq$30%, respectively, pointing to an increased uniformity on a 100 mm wafer scale.

We further characterize disorder in the ^{28}Si/SiGe heterostructure at 190 mK by measuring the single-particle relaxation time τ_q[40] in the quantum Hall regime. From τ_q, we derive the quantum mobility $\mu_q = e\tau_q/m^*$, where e is the elementary charge and m^* is the effective mass, and the quantum level broadening of the momentum eigenstates $\Gamma = \hbar/2\tau_q$, where $\hbar$ is the reduced Planck constant. μ_q, associated with τ_q, is influenced by all scattering events and is different from the mobility $\mu = e\tau_t/m^*$, where the scattering time τ_t is unaffected by forward scattering. Therefore, τ_q and μ_q qualify the disorder in the heterostructure more comprehensively than τ_t and μ.

Figure 3(a) shows for the H-FET with the highest mobility a measurement of ρ_{xx} plotted for clarity against the Landau level filling factor $\nu = hn/eB$, where h is the Plank constant. This measurement was performed at fixed density $n = 4.75 \times 10^{11}$ cm^{-2} by keeping V_G constant and sweeping B. Onset of Shubnikov–de Haas oscillation, Zeeman splitting, and valley splitting occurs at 0.125, 0.43, and 1.15 T, respectively, corresponding to ν = 152, 42, and 17. The observation of Shubnikov–de Haas oscillations, Zeeman, and valley splitting at these high filling factors indicates a very low level of disorder.[41] Figure 3(b) shows the normalized oscillation amplitude $\Delta\rho_{xx}/\rho_0 = (\rho_{xx} - \rho_0)/\rho_0$ in the low magnetic field regime after polynomial background subtraction. $\rho_0 \simeq 63$ Ω/square is the longitudinal resistivity at zero magnetic field from which we extract a mobility of 2.7×10^5 cm^2/V s.

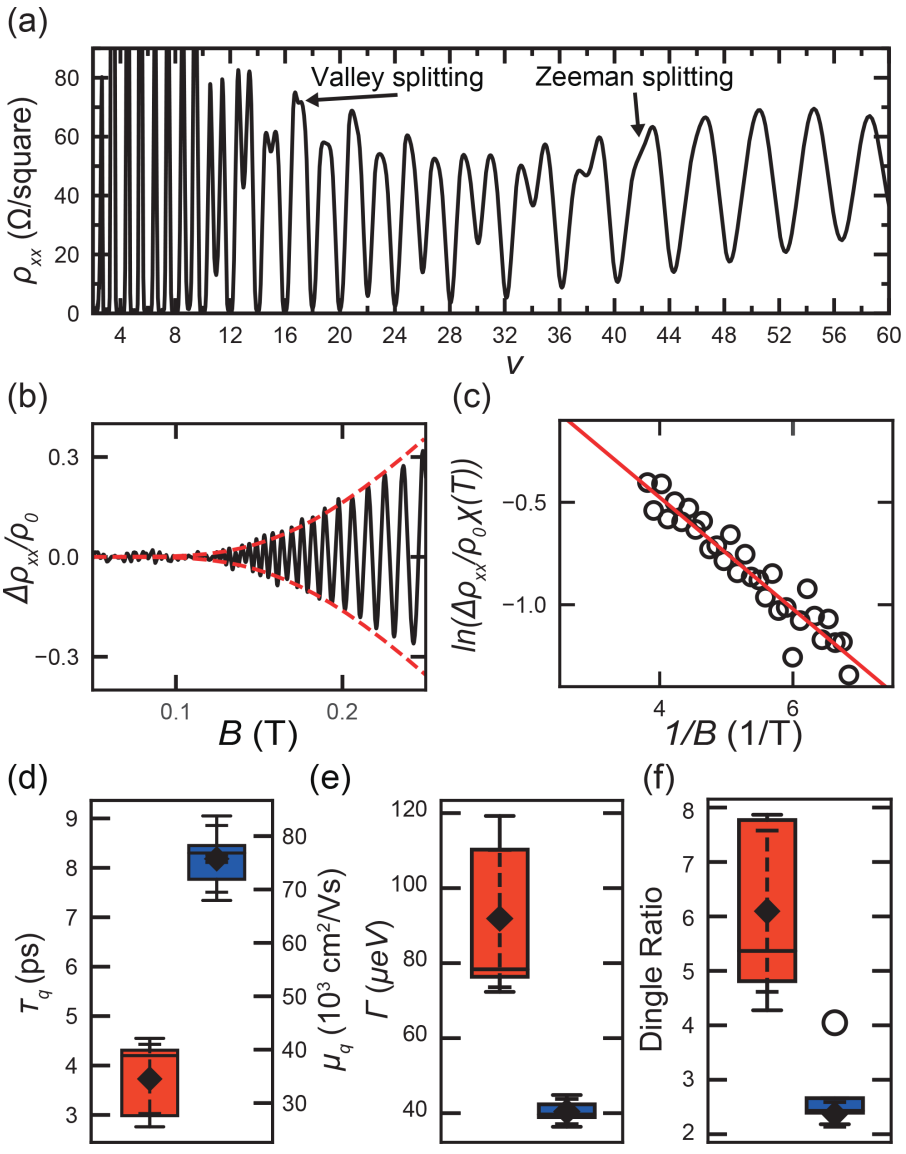

FIG. 3. (a) Longitudinal resistivity ρ_{xx} measured at $T = 190$ mK as a function of Landau level filling factor ν. These measurements are performed at fixed $n = 4.75 \times 10^{11}$ cm^{-2} while sweeping the perpendicular magnetic field B. Spin and valley degenerate Landau levels correspond to $\nu = 4k$ ($k = 1, 2, 3, \ldots$), Zeeman split levels to $\nu = (4k - 2)$, whereas valley split levels correspond to odd integer filling factors ν. Arrows indicate the filling factors at which Zeeman spin splitting and valley splitting are resolved. (b) Normalized resistivity oscillation amplitude (black curve) as a function of B after polynomial background subtraction. The arrow indicates the magnetic field at which Shubnikov–de Haas oscillations are resolved. The red dashed line is the theoretical fit of the oscillations envelope from which we extract τ_q. (c) Dingle plot (open circles) from the first twenty most resolved resistivity oscillation maxima and minima and theoretical curve (solid red line) computed using τ_q from the analysis in (b). (d)–(f) Distributions of τ_q, μ_q, Γ, and Dingle ratio measured at $n = (5 - 6) \times 10^{11}$ cm^{-2} for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 5 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 7 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.

We estimate $\tau_q = (7.4 \pm 0.1)$ ps from a fit of the Shubnikov–de Haas oscillation envelope to the function $\Delta\rho_{xx} = 4\rho_0\chi(T)\exp(-\pi/\omega_c\tau_q)$, where $\chi(T) = (2\pi^2 k_B T/\hbar\omega_c)/\sinh(2\pi^2 k_B T/\hbar\omega_c)$. Here, $T = 190$ mK, k_B is the Boltzmann constant, and ω_c is the cyclotron frequency calculated using a fixed $m^* = 0.19\, m_e$.[41,42] From τ_q, we derive $\mu_q = (6.8 \pm 0.1) \times 10^4$ cm^2/V s, $\Gamma = (44 \pm 1)$ μeV, and find a Dingle ratio $\tau_t/\tau_q \simeq 3.8$. The Dingle plot of Fig. 3(c) highlights the high number of oscillation maxima and minima used in the fitting procedure.

In Figs. 3(d)–3(f), we plot the distributions for τ_q (and μ_q), Γ, and the Dingle ratio τ_t/τ_q, measured in the high density regime [$n = (5-6) \times 10^{11}$ cm^{-2}]. As in Figs. 2(d)–2(f), we consider heterostructures terminated with an amorphous Si-rich layer (blue, 5 H-FETs measured) and heterostructures with an epitaxial Si cap (red, 7 H-FETs measured). Heterostructures with an amorphous Si-rich layer have a mean τ_q of (8.1 ± 0.5) ps and consequently a mean μ_q of $(7.5 \pm 0.6) \times 10^4$ cm^2/V s and Γ of (40 ± 3) μeV, representing a $\simeq 2\times$ improvement compared to heterostructures with an epitaxial Si cap. Consistent with the trend in Figs. 2(d)–2(f), we find a significant reduction in spread for τ_q (30%), and consequently for μ_q, Γ. Furthermore, in heterostructures with an amorphous Si-rich layer, we find a mean Dingle ratio of (2.3 ± 0.2). This mean value is $\simeq 300\%$ smaller and has an 80% reduction in spread compared to heterostructures with an epitaxial Si cap. This low value of the Dingle ratio indicates that short-range scattering from impurities within or near the quantum well is the dominant scattering mechanism,[34] in agreement with the analysis of the mobility-density curve. Scattering from remote impurities is reduced thanks to a better semiconductor/dielectric interface. Our mean value for τ_q in ^{28}Si/SiGe is also on par with the best value reported in Ref. 35 from H-FETs in Si/SiGe heterostructures featuring an epitaxial Si cap. However, in our samples, the semiconductor/dielectric interface is much closer to the channel (30 nm compared to 50 nm in Ref. 35). Therefore, this comparison confirms that scattering from remote impurities is limited in our devices as a consequence of a high-quality and uniform semiconductor/dielectric interface associated with the termination process at 500 °C.

In summary, we challenged the mainstream approach to deposit an epitaxial Si cap on ^{28}Si/SiGe heterostructures and, instead, we terminated the SiGe barrier with an amorphous Si-rich layer, obtained by exposure to DCS at 500 °C. Compared to previous heterostructures that feature an epitaxial Si cap and that have already produced high performance spin qubits,[3,7] we demonstrate an improvement in performance of H-FETs in terms of mean value and spread of mobility, percolation density, maximum electric field before hysteresis, and single particle relaxation time (and hence quantum mobility). We speculate that performance improves because the amorphous Si-rich layer gets completely oxidized compared to the epitaxial Si cap (supplementary material), thereby creating a more uniform SiO_x layer with less scattering centers. By having a better semiconductor/dielectric interface and wafer-scale uniformity, we expect that this material stack may lead to Si spin qubits with improved yield and performance. In this direction, charge noise measured in quantum dots on these heterostructures will be very informative as these measurements probe the dynamics of charge fluctuations that transport experiments are not very sensitive to. These results motivate new studies, for example, by varying the temperature and/or time of exposure to DCS to understand in detail the nature of the amorphous Si-rich layer on the SiGe barrier, the role of Cl and H upon oxidation in air, and to use this knowledge as a tool for further optimizing the semiconductor/dielectric interface.

See the supplementary material for an extended Fig. 1 and measurements of the electron temperature.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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