Stellingen behorende bij het proefschrift

PROGRAMMABLE SURFACE ACOUSTIC WAVE DETECTION IN SILICON

Design of Programmable Filters

van

Jacobus Cornelis Haartsen

1. Voor een goed begrip van de detectoren beschreven in dit proefschrift is het voldoende om alleen de elektrische velden, die aan de (akoesto-elektrische) oppervlaktegolven gebonden zijn, te beschouwen. In dit verband is het voor een elektrotechnisch ingenieur aantrekkelijker te spreken van elektrische oppervlaktegolven (Surface Electric Waves) dan van akoestische oppervlaktegolven.

2. Het vergroten van het rendement van transducenten op piëzoelektrische substraten door de toevoeging van een dunne, niet-piëzoelektrische laag kan uitsluitend toegeschreven worden aan de verandering in de akoestische eigenschappen van het nieuwe, gelaagde medium. De verandering in de diëlektrische eigenschappen als gevolg van de toegevoegde laag zal altijd een verlaging van het rendement tot gevolg hebben.

   Dit proefschrift, hoofdstuk 2.

3. Indien in een programmeerbare oppervlaktegolf detector hoge eisen gesteld worden aan signaal-ruisverhouding, regelbereik en onderdrukking van storende invloeden zoals regeneratie en elektromagnetische overspraak, moet men van een actief detectiemechanisme gebruik maken.

   Dit proefschrift, hoofdstuk 3.

4. Zonder compensatiemethoden wordt de ondergrens van het regelbereik in een actieve detector bepaald door het passieve detectiemechanisme.

   Dit proefschrift, hoofdstuk 4 en 5.

5. Om reflecties aan oppervlaktegolf detectoren in ZnO-SiO_2-Si structuren te vermijden kunnen gediffundeerde of ionen-geïmplanteerde junctie-elektroden toegepast worden, mits van een actief detectiemechanisme gebruik gemaakt wordt.

   Dit proefschrift, hoofdstuk 3.

6. Voor het voortbestaan van het menselijk ras is een mondiale geboorteregeling een eerste vereiste.

7. Koken is één van de weinige hobby's waarbij het aangename met het nuttige gecombineerd wordt. Bovendien profiteren van deze hobby in het algemeen meer personen dan de hobbyist alleen.

8. De welvaart van een land is af te leiden uit de grootte van het per hoofd van de bevolking geproduceerde hoeveelheid afval van (nog) hoge kwaliteit.

9. Onze werkelijkheid reikt zover onze sensoren reiken.

10. Veel van het hedendaagse wetenschappelijk onderzoek is eerder grensbepalend dan grensverleggend.

11. Coïncidentieproblemen in digitale fasevergelijkers kunnen opgelost worden door een scheiding te maken tussen de toestandsvariabelen van het sequentiële circuit en de daadwerkelijke uitgangsvariabelen.

    J.C. Haartsen and R.C. den Dulk: "Novel circuit design and implementation of adaptive phase comparators," Electr. Lett. 23, pp. 551–552, 1987.

12. Modelvorming speelt een belangrijke rol in de hedendaagse wetenschap; dit is een direct gevolg van het gelimiteerde perceptie- en bevattingsvermogen van de mens.

PROGRAMMABLE SURFACE ACOUSTIC WAVE DETECTION IN SILICON

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Design of Programmable Filters

Programmeerbare akoestische oppervlaktegolf detectie
in silicium. Ontwerp van programmeerbare filters.

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus,
prof. drs. P. A. Schenck,
in het openbaar te verdedigen
ten overstaan van een commissie
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door

Jacobus Cornelis Haartsen

elektrotechnisch ingenieur
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Dit proefschrift is goedgekeurd door de promotor prof. dr. ir. S. Middelhoek.

Dr. ir. A. Venema heeft als toegevoegd promotor in hoge mate bijgedragen aan het totstandkomen van het proefschrift.

Leden van de promotiecommissie:

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Action induces Reaction

Voor Marjan

CONTENTS

Chapter 1

INTRODUCTION

Filtering is one of the most important functions of modern signal transmission systems. Optimal signal detection requires a careful selection of the desired signal and rejection of all unwanted signals. Continuous progress in modulation and coding techniques not only improves the transfer of information, but at the same time requires sophisticated signal-processing techniques. The flexibility of the system can greatly be enhanced by making the filters real-time programmable in order to be able to alter the filter characteristics at will, which enables it to switch arbitrarily between different transmission channels. In addition, it allows adaptive filtering, which enables the adjustment of the system to unknown and time-varying conditions in the transmission channel.

The gradual shift to higher operating frequencies and broader bandwidths is a continuous trend in radar and communication systems; they increase the speed of information transfer in communication systems and improve the resolution in radar systems. Surface Acoustic Wave devices operating in the VHF and UHF range can, to a large extent, perform the required wideband signal-processing functions. This thesis contributes to the development of wideband, programmable filters in which surface acoustic wave technology is employed.

1.1 PROGRAMMABLE TRANSVERSAL FILTERS

1.1.1 Matched and Adaptive Filtering

In general, the flexibility and application range of a filter are enhanced when some kind of programmability is included in the design. However, adding programmability always results in an increase in complexity, and usually performance degradation, of the filter. Before considering the realization and implementation of programmable filters, two types of filters will be discussed in which programmability is highly desirable and even indispensible. These filters, which are extensively used in communication and radar systems are the *matched* filter and the *adaptive* filter.

A matched filter provides the maximal signal-to-interference ratio when the detection of pulse-shaped signals embedded in noise of a known spectral density is involved [1]. If the interfering noise is white, the required impulse response is the time-reversed replica of the signal pulse to be detected. Under matched conditions, the filter produces the autocorrelation of the incoming signal and is, therefore, also called a correlation filter. The matched filter is extensively used in pulsed radar and digital communication systems in which Spread-Spectrum techniques are employed. In these systems the transmitted signals are encoded making use of wideband, phase-modulated codes. Usually, FM chirp or binary Phase-Shift-Keyed (PSK) codes are used. Matched filters are the obvious elements to employ to demodulate such signals.

In the design of radar systems, two basic concepts must be taken into account: resolution and signal-to-interference ratio (SIR). For a high resolution, a short pulse is required, whereas a large SIR requires a large energy content in the pulse. The ultimate performance of the radar is limited by the maximal allowable, instantaneous output power of the transmitter. Pulse-compression techniques can improve the radar performance considerably [2]. Before transmission, the pulse is modulated with an FM or PSK waveform, which produces a very wide bandwidth that is not related to the pulse duration. Therefore, the bandwidth and the duration of the transmitted pulse can be fixed independently. In the radar receiver, the reflected pulse is fed into a pulse-compression filter, which is basically a filter that is matched to the waveform of the coded pulse. The received pulse is compressed into a very short correlation pulse, the duration of which is only determined by the bandwidth of the code. By using transmitters with different codes and receiver units with corresponding matched filters, several radar systems can operate without mutual interference [3].

The expansion of the signal bandwidth before transmission is also

widely used in digital communication systems. In Direct-Sequence Spread-Spectrum systems, each data symbol is transmitted as a binary PSK code sequence [4]. Usually, a pseudonoise (PN) code is used. Because the bandwidth of a PN code sequence is much larger than the symbol rate, the signal power is spread over a wide range in the frequency spectrum. The power density per Hz becomes very low and signal-to-noise ratios much lower than 0 dB are present in the transmission channel. Therefore, the signal is difficult to detect and quite insensitive to narrowband interference. Since the signal is uniquely determined by its code, several communication channels can be accommodated in the same frequency band, provided they use different codes. Demodulation of the spread signal is achieved by the correlation of the received signal with a reference signal, which contains the same binary code as is used in the transmitter. Correlation is a synchronous process, and a strict timing relation between the incoming and reference signals is mandatory. Synchronizing the reference signal to the incoming signal is a time-consuming task. However, in the matched filter, the correlation process is performed instantaneously. The matched filter provides an asynchronous detection of the coded information, and long search times are avoided. Although the matched filters cannot adequately be used when very long code sequences are involved, they do have an important task in reducing the acquisition time in Spread-Spectrum receivers. Since the Spread-Spectrum systems produce a secure means to transfer information, which is protected against interference, interception and multipath echoes, there is an increasing interest in using these systems, e.g. in (mobile) digital radio [5], indoor wireless digital communication [6], packet radio [7].

Programmability in matched filters, both for radar and communication applications, is highly desirable. Since different channels are distinguished by different codes (code-division multiplexing), the receiver can switch between different channels by changing the code of its matched filter. In addition, security is increased by using different codes sequentially in the same transmission channel. Only the receiver which is continuously adjusted to the rapidly changing code sequences can demodulate the signal.

In practice, the transmission channels are not optimal. Distortions and all kinds of interfering signals disturb the transfer of information. In many cases, these distortions and interferences are time variant and are not known in advance; then adaptive filtering is required: the filter function is periodically updated, until a maximal SIR is obtained. In the following, some specific adaptive filters are considered.

Adaptive bandpass filters are applied in transmission systems in which the center frequency of the signal changes. This can be an unintended shift which is caused by drift or Doppler phenomena, or an intended shift, for example in frequency-multiplexed and in Spread-Spectrum frequency-hopping systems. When the shift is intended and thus known in advance, real-time adjustment of the pass band can be achieved.

Adaptive whitening filters are used to reject time-varying interfering signals. These kinds of filters are extensively used in transmission channels, where continuous-wave (CW) interferences are present. The adaptive filter algorithm will eventually produce a bandstop filter function with the notch exactly situated on the CW tone.

Equalizers are adaptive filters which restore the signal when distortions have been incurred in the transmission channel. An equalizer can be considered as an inverse filter with a filter function, which is reciprocal to the transfer function of the channel. Used as an echo canceller, the equalizer can enormously improve the signal detection in a multipath environment [5].

The need for programmability in adaptive filters is quite obvious. Usually a lot of post processing has to be performed to find the optimal filter characteristic. For this purpose, computer-based algorithms are employed [8]. As a consequence, only slowly varying interferences can be suppressed.

1.1.2 Basic Transversal Filter Structure

Sophisticated filters of the types discussed above cannot be constructed with lumped network elements such as, for example, those encountered in *LC* filters. The realization of filter functions like these can conveniently be carried out using the transversal filter concept. This concept was first described by H.E. Kallmann [9]. In Fig. 1.1 the basic realization of a transversal filter is shown. It consists of three elements: a tapped delay line, a weight circuit in which each tap output is multiplied by a certain tap weight factor, and finally a summation circuit in which all weighted tap signals are superposed. The transversal filter is a linear filter with a finite impulse response (FIR). The filter operation is completely asynchronous and produces a fixed timing relation between the input and output signals.

The impulse response $h(t)$ of the filter is given by

$$h(t) = \sum_{n=1}^{N} a_n \delta(t - \sum_{m=1}^{n} T_m) \tag{1.1}$$

in which a_n is the tap weight factor and $\sum_{m=1}^{n} T_m$ the time delay which corresponds to the n^{th} tap. Because of the discrete nature of the tapping,

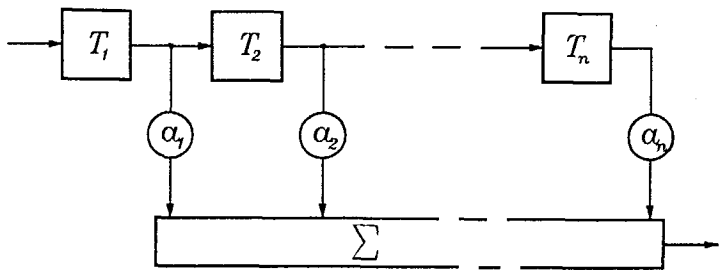


Figure 1.1: *Functional diagram of a transversal filter.*

the signal in the delay line is sampled at a rate which is determined by the inter-tap delay. For programmable filters, a uniform sampling is used, which results in a constant inter-tap delay ΔT and simplifies the impulse response to

$$h(t) = \sum_{n=1}^{N} a_n \delta(t - n\,\Delta T) \tag{1.2}$$

With Fourier Transform techniques the frequency response $H(f)$ of the filter can be derived

$$H(f) = \sum_{n=1}^{N} a_n e^{-j\omega n \Delta T} \tag{1.3}$$

Because the transversal filter is a nonminimum phase filter, a wide variation in both the amplitude and phase characteristics can be obtained simply by choosing the tap weight factors appropriately. For filtering at baseband, the tap values are real and the weight factor a_n is a real number; for IF signals on the other hand, complex weight factors can be applied, since both the magnitude and the phase of the tap output can be varied.

Several technologies have been adopted for the implementation of transversal filters [10, 11]. The largest extent of flexibility is obtained with digital filters. The rapid progresses in IC technology during the past decades allows Very Large Scale Integration. However, digital signal processing is not very attractive for broadband systems which require a large dynamic range. In these applications, a high clock frequency combined with a long word length (> 10 bits for a 60 dB dynamic range) are required, which results in high power dissipations. In particular, the analog-to-digital conversion process imposes difficulties. In practice, this limits the bandwidth of digital transversal filters to a few hundred kHz. A method which consumes much less power is achieved with analog Charge-Transfer devices (CTD). The signal is represented by an amount of charge, which is shifted and nondestructively detected along a delay line [12]. Typ-

ically, CTD transversal filters operate with filter bandwidths up to a few MHz.

Digital and Charge-Transfer filters operate at baseband. Because the input signal is sampled, a clock frequency of twice the bandwidth is required to prevent aliasing. For the implementation in silicon, typically filter bandwidths up to 10 MHz are feasible. Continuous progress in the GaAs technology will move these bandwidths into the 100 MHz–1 GHz range. However, an attractive alternative for wideband filters in this frequency range is the Surface Acoustic Wave (SAW) technology. Analog filters employing SAW techniques operate at IF frequencies in the range of 10 MHz–10 GHz. Bandwidths up to 30 or 40 % of the operating frequencies are feasible. Because SAW filters are passive devices, low-power operation results. In the next section the realization of programmable SAW filters is discussed.

1.2 SURFACE ACOUSTIC WAVE FILTERS

1.2.1 Acoustic Signal Processing

Acoustic or elastic waves in a solid result from mechanical vibrations around an equilibrium position. This vibration can be in the direction of the wave propagation which corresponds to a longitudinal mode, or normal to the propagation direction which corresponds to a transverse or shear mode. Acoustic waves have a propagation velocity which typically lies between 10^3 and 10^4 m/s. This is about five orders of magnitude slower than electromagnetic waves. Therefore, acoustic waves are very attractive for delay line applications: one microsecond of delay only requires a few mm of propagation path.

An important subject of research has always been the link between the electrical and the acoustical domain. How are the electric signals converted into acoustic signals and vice versa? The key to this problem is piezoelectricity. This phenomena couples the elastic strains to electric fields and occurs in anisotropic materials that lack a center of symmetry in their atomic structure. By using resonating structures, which are constructed with metal electrodes and piezoelectric materials mechanically connected with the propagation medium, an efficient in and out coupling of acoustic waves can be achieved.

The simplest types of waves are Bulk Acoustic Waves (BAW). These waves propagate in an infinite homogeneous medium and have either a longitudinal or transverse motion. An efficient bulk-wave excitation is achieved in a sandwich structure consisting of a piezoelectric plate placed

between two metal electrodes of opposite RF polarity. By placing this structure at the beginning and the end of an oblong object, a BAW delay line can be constructed.

At the stress-free boundary of a semi-infinite solid another type of wave can exist: the Surface Acoustic Wave (SAW). This wave sticks to the surface and the penetration depth into the medium is in the order of one wavelength. One type of SAW, the Rayleigh wave, had already been described mathematically by Lord Rayleigh in 1885 [13]. The Rayleigh wave has both a longitudinal and a transverse component, and has a propagation velocity which is smaller than the corresponding longitudinal and shear wave velocities [14]. Although many other types of SAWs can exist at the surface, in this thesis only the Rayleigh type is considered and the term "SAW" is restricted to this type of wave.

The use of SAWs for signal-processing functions was postponed because of the lack of an efficient method to couple the electric signals to the SAW. A breakthrough was accomplished by the introduction of the Interdigital Transducer (IDT), the application of which was first published in open literature by White and Voltmer [15]. The IDT can be considered to be the basic element of all SAW devices applied today. It consists of an array of metal electrodes of alternate RF polarities placed at the surface of the propagation medium, see Fig. 1.2. The piezoelectricity is added by using piezoelectric crystals like quartz or lithium niobate as the propagation medium, or by covering the nonpiezoelectric propagation medium with a piezoelectric film. When a time-varying electric voltage is applied across the transducer terminals, a standing wave pattern is built up in the interdigital pattern. This standing wave pattern can be considered as the superposition of two contra-directed traveling waves which leave the IDT at the edges. Since piezoelectricity is a reciprocal phenomenon, the conversion process is reversible and the IDT can also convert traveling

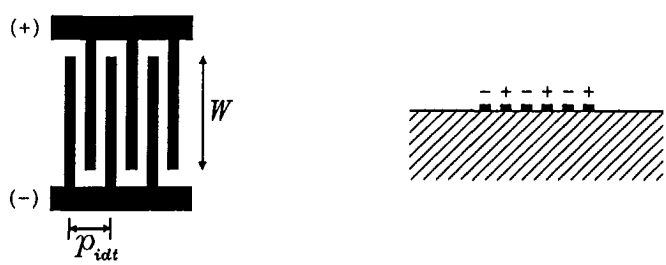


Figure 1.2: *Top view (left) and cross section (right) of an Interdigital Transducer.*

mechanical waves into electric signals. An optimal conversion occurs when the wavelength of standing acoustic wave pattern corresponds to the period of the electrode pattern. The resonance frequency f_0 is determined by the SAW phase velocity v_{ph} and the transducer period p_{idt}

$$f_0 = \frac{v_{ph}}{p_{idt}} \tag{1.4}$$

Electrode spacings in the order of 10 μm amount to operation frequencies of several decades of MHz.

The acoustic signal is concentrated at the surface of the delay medium and can therefore be reached anywhere in the delay path. Therefore, sophisticated filter functions can be realized by designing appropriate metal ID structures. Since the dimensions and the planar fabrication techniques of the metal ID patterns are compatible with modern IC technology, the SAW technology is well established and allows mass fabrication of SAW filters.

1.2.2 Programmable Tapped Delay Lines

Since low-power and small-sized delay functions can readily be obtained with SAW technology, this technology is very suitable for the implementation of tapped delay lines. In Fig. 1.3 the generalized implementation of a programmable SAW filter is depicted, which corresponds to the basic transversal filter structure shown in Fig. 1.1. The electric input signal is converted into an acoustic wave by using a conventional IDT structure. In the propagation path of the traveling wave, SAW detectors are placed to sample the wave. The wave which is transmitted in the opposite direction is absorbed by an acoustic absorber at the edge of the delay line. The detector outputs are electronically weighted, and then accumulated in a collective summation circuit. Basically, this structure is a tapped delay line with programmable tap outputs, and is, therefore, denoted as *Programmable Tapped Delay Line.*

The key elements of the programmable tapped delay line (PTDL) are the programmable taps. In these taps two functions are performed: signal conversion from the acoustical into the electrical domain at the sampling positions, and controlling the electric output signal to obtain the desired tap weight factor. For the acoustoelectric conversion process, two detection mechanisms are available: a *passive* and an *active* mechanism. In the passive detector, the electric output signal results directly from the mechanically induced electric fields. The weight function must be applied afterwards in an electronic circuit, which is located outside the SAW

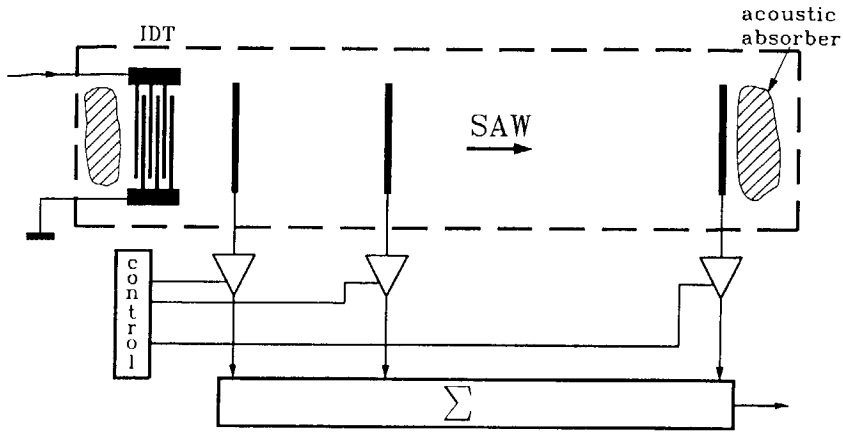


Figure 1.3: *General structure of a programmable SAW Tapped Delay Line.*

propagation path. Because the detection and the control functions are separated, this type of tap is denoted as *Separated-Control Tap.* In the active detector, the mechanically induced electric fields modulate a much larger electric signal within the detector, which is supplied by an auxiliary electric source. By varying the signal supplied by this auxiliary source, the output signal is controlled directly at the origin. In fact, the detection and control functions are merged into a single, active element which is located in the propagation path. Therefore, this tap is denoted as *Integrated-Control Tap.*

In the previous discussion, linear detection processes were assumed. A detection mechanism, which uses a nonlinear process, is the parametric detection. The parametric detector can be considered as an active detector in which the auxiliary source is not electric but acoustic. This auxiliary or pump signal is present as an acoustic CW signal in the propagation path. Because of nonlinear effects in the detector or in the control circuitry, the output signal is the product of the main and the pump signal. By controlling the nonlinear coefficients, a programmable tap can be obtained. An elaborated discussion of passive, active and parametric detectors is presented in Chapter 3.

Various technologies have been adopted for the PTDL fabrication. The very first PTDLs were merely extensions of the fixed TDLs: passive taps, located in a conventional delay line on a piezoelectric substrate, were individually connected to a control circuit by use of bonding wires [16]. Initially, the control circuitry of these hybrid, separated-control taps was

very simple, consisting of only a few discrete diodes [17]. However, continuous progress in IC technology yielded more complex circuitry, making use of MOS [18] and bipolar LSI [19] in a Silicon-on-Sapphire (SOS) and full silicon technology, respectively. SOS technology seems to be an attractive approach because of the low capacitances of the electronic devices, which yield high on-off ratios, high RF tap-to-tap isolation, and low-loss RF switching in the control circuitry. At the beginning of the eighties, GaAs was introduced in high-speed control electronics in hybrid PTDL configurations [20]. The piezoelectric media generally applied in hybrid PTDLs are ST-X Quartz or YZ-$LiNbO_3$, which provide temperature-stable and low-loss delay media, respectively.

The hybrid PTDL is an attractive configuration, because both the acoustical and electrical properties of the system can be optimized simultaneously. However, the hybrid technology prevents the implementation of active detectors, and the use of wire connections between delay line and electronics becomes very unattractive when the frequency and the number of taps increases. Bonding wires can be circumvented by using an air-gap structure. In this structure, a piezoelectric medium is placed upside down and very close to a semiconducting medium. Usually, a spring assembly and SiO_2 spacer rails on the semiconductor are applied in order to maintain a uniform air gap of a few hundred nm [21]. SAWs travel along the surface boundary facing the semiconductor. Because the air gap is very small, the fringing electric fields induced in the piezoelectric medium couple directly to detectors located at the semiconductor surface.

Several laboratories demonstrated the feasibility of wideband PTDLs with reasonable performance by using a hybrid technology. However, hybrid configurations do have disadvantages with respect to compactness, reliability, and price-to-performance ratio when large volumes are involved. Monolithic integration of the SAW delay line and the control electronics is preferable, and should ultimately give the best performance. However, the fabrication complexity of this monolithic integration has always hindered its progress. For the integration of SAW devices and electronic circuitry, both piezoelectric and semiconducting properties must be combined in a single chip. Two methods are available: a piezoelectric semiconductor, or a nonpiezoelectric semiconductor covered with a piezoelectric film.

Piezoelectric semiconductors like ZnO and CdS have extensively been investigated because of the acoustoelectric phenomena which occur in these materials. However, if electronic circuitry must be added, only GaAs provides the required properties [22]. A full monolithic integration of a PTDL in GaAs with passive taps is reported in Reference [23]. Much

attention has been paid to parametric detectors which employ MESFETs [24]. GaAs is only weakly piezoelectric, and IC fabrication on GaAs is expensive and not a trivial task. Although the use and knowledge of GaAs IC fabrication is steadily growing in all areas of the industry, the wide use of silicon and the experience in handling this material makes it highly attractive for monolithic PTDL implementations.

Since silicon is not piezoelectric, silicon implementations always require a piezoelectric overlay in order to enable the acoustoelectric conversion processes to occur. Several films like AlN, ZnO and CdS have been applied. Programmable matched filters, that use AlN in combination with an SOS technology, are reported in Reference [25]. However, AlN does not have attractive delay properties because of the high wave velocities and strong dispersive behavior [26]; CdS films, on the other hand, are difficult to manufacture. Therefore, ZnO is the most attractive material to use as piezoelectric overlay in integrated SAW devices. Because the ZnO-Si combination provides a much stronger piezoelectric coupling than GaAs, much higher conversion efficiencies can be achieved. A full silicon implementation of a PTDL which uses a ZnO film, was first reported by Hickernell in 1973 [27]. In this filter the piezoresistive effect in MOSFETs is applied. ZnO is only required in the IDT region, where the SAWs are to be excited. A ZnO-Si implementation, in which piezoelectricity is used in both the SAW generation and detection, is described in Reference [28], where passive detectors in the SAW propagation path are connected to external dual-gate FETs for tap control.

1.2.3 Alternative Programmable Filter Techniques

Although the Programmable Tapped Delay Line is the most direct realization of a filter with a programmable filter function, several other techniques which perform the same function were investigated. Two important ones will be discussed briefly: the Convolver and the Fourier Transform Processor. Basically, these two realizations produce the convolution of two input signals. Since filtering is merely the convolution of the input signal with the filter impulse response, the Convolver and the Fourier Transform Processor (FTP) can be used as filters if one of the input signals is a reference signal which contains the required filter function. Since this reference signal is applied externally, its format can readily be changed and the filter becomes programmable.

In a convolver, two contra-directed SAWs travel in a common delay medium. Because of nonlinear effects in the overlap region, product terms appear. These nonlinearities can be caused by the elastic medium itself

[29], or by the nonlinear interaction with charge carriers, which are located in a nearby semiconductor [30]. The latter effects are strongly related to the afore-mentioned parametric detection mechanism. By using a conventional IDT (the nondegenerate case) or an electrode plate (the degenerate case) in the interaction region, the output signal can be coupled out at the sum or difference frequency of the input and reference signals.

The Fourier Transform technique is a general method to perform signal-processing functions in the frequency domain instead of in the time domain. Because convolution in the time domain corresponds to multiplication in the frequency domain, filter functions can be realized by first transforming the input signals into the frequency domain, performing the multiplication in the frequency domain, and then transforming the result back into the time domain. For the transformation from the time to the frequency domain and vice versa, the chirp Z-transform can be employed [31]. SAW chirp filters are extremely suitable to perform this transformation in the high frequency range. A complete FTP contains several of these chirp filters [32].

The fundamental difference between the direct realization of the PTDL and the indirect techniques, is shown in Fig. 1.4. The PTDL is a two-port device which operates completely asynchronously. There is a fixed timing relation between the input and the output signals. The filter response $h(t)$ is embedded in the device itself. The Convolver and FTP are three-port devices. The filter response is provided externally as a reference signal $r(t)$. An exact timing relation between the input signal $g(t)$ and the reference signal $r(t)$ is required, which yields a synchronous filter operation. The timing relation between the input and the output signals depends on the timing of the reference signal. In the convolver a time contraction takes place ($\alpha = 2$).

A great deal of effort was put into realizing the asynchronous and continuous operation of the Convolver and FTP by the use of repetitive

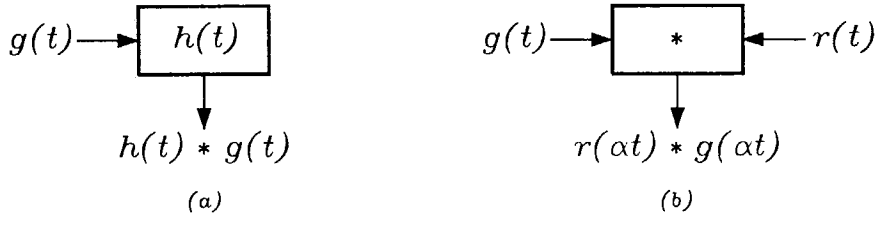


Figure 1.4: *Functional diagrams of (a) a PTDL, and (b) indirect techniques such as the Convolver ($\alpha = 2$) or the Fourier Transform Processor ($\alpha = 1$).*

reference signals combined with time gating [33] or a special signal transfer protocol [34], and by the use of parallel channels for signal interlacing [35]. In a number of applications, an acceptable asynchronous operation can be achieved, however, at the expense of additional hardware complexity, power consumption and volume of the required timing circuits and waveform-generation circuits that provide the RF reference signals. For comparison, the PTDL, although its programmability is limited, only requires control circuitry to set the tap weight factors.

A new and promising development, which should be mentioned here, is the Acoustic-Charge-Transfer (ACT) technique. This technique, which was first introduced by Gaalema [36], is comparable to the operation of conventional Charge-Coupled techniques. However, the traveling potential wells, which contain the charge, do not arise from clocked electrodes, but from the traveling electric potential of the SAW itself. The device operates at baseband, but bandwidths up to 150 MHz were realized. At the moment, the research focusses on buried-channel devices in GaAs, in which very high transfer efficiencies can be achieved [37]. Recently, a monolithic programmable PTDL, based on ACT techniques in GaAs, was presented and it has some very promising features [38].

Silicon was also investigated for the implementation of ACT techniques. ZnO-SiO_2-Si structures were applied to realize surface-channel ACT devices [39], but charge trapping at the SiO_2-Si interface severely deteriorated the transfer operation [40]. Buried-channel devices are not likely to be developed in silicon, because the depletion layer, which must be applied from the surface, is difficult to realize in ZnO-SiO_2-Si structures.

1.3 OBJECTIVES OF THIS WORK

If, in the future, the SAW technology must compete with other analog and digital technologies, the merging with electronic circuitry is indispensable. It is believed that monolithic integration will in the end provide the most compact, reliable and cost-effective solution. Silicon has been chosen as the starting material, because of the advanced IC fabrication experience and the excellent electronic circuitry that can be obtained. In addition, acceptance by industry is likely to be more rapid, if merging SAW and electronics only involves a few extra steps in a standard fabrication process.

A full, monolithic integration in a ZnO-SiO_2-Si structure of a conventional SAW filter and electronic circuitry for mixing and amplification was

presented by Visser [26]. However, the combination of SAW and semiconductor technology not only provides a means to combine acoustical and electronic devices on a single chip but, in addition, new acoustoelectric devices can be designed, in which both acoustic and electronic signal-processing functions are merged into a single element. This functional integration, which can be denoted by the name *piezotronics*, offers a wide range of new devices and potential applications. One application is the tapped delay line with a programmable filter function. Piezotronic elements in the SAW propagation path, electronic control and impedance-matching circuitry to link to the external world, and other electronic signal-processing circuitry, are all contributing to the development of a truly monolithic, smart filter.

The main object of research in this thesis is the synthesis, realization and implementation of programmable SAW detectors in ZnO-SiO_2-Si layered structures. New semiconductor elements in silicon are investigated, in which the charge carriers are directly influenced by the electric fields which are mechanically induced by the SAW. The ZnO-SiO_2-Si configuration offers the possibility to fabricate these elements with highly conductive, diffused or implanted regions in the silicon substrate, thus avoiding metal parts in the propagation path of the SAW. In this method of fabrication, a smooth surface above the detector results, which improves the growth of ZnO, and reduces reflections which are caused by mechanical and topological discontinuities. Sensitive taps with a wide control range require active detection mechanisms.

From scientific point of view, the combination of SAW and semiconductor technology is very attractive, because it provides almost limitless possibilities. Challenging research projects result from the inherent multidisciplinary field where SAW physics, semiconductor physics, and IC technology meet. However, monolithic integration of SAW and semiconductors has continuously been hindered by technological problems, and the choice for a monolithic solution instead of for an alternative technology always seems to exchange hardware complexity for technological complexity. For the ZnO-SiO_2-Si structure in particular, this relates to the growth of high-quality ZnO layers, which is not yet as state-of-the-art as the silicon technology. However, encouraging results have been achieved, and the history of IC technology shows that if effort is put into the improvement of the technology, these problems will eventually be surmounted. The author hopes that this thesis will motivate and encourage many co-workers in the field to achieve this aim, which will eventually lead to high-performance, integrated acoustics.

1.4 ORGANIZATION OF THIS THESIS

The contents of this thesis can roughly be divided into three parts and follows a bottom-to-top approach. The first part is a theoretical discussion concerning acoustoelectric effects, and the detection mechanisms that are based on these effects. In Chapter 2, all the phenomena are considered that occur when a SAW travels through a ZnO-SiO_2-Si layered structure and its penetrating electric fields interact with the mobile charge carriers in the silicon. In addition, the influences of depletion layers, accumulation layers, and interface states are examined. In Chapter 3, the realization of controllable SAW detectors which use the phenomena discussed in Chapter 2 is investigated. Both passive and active detectors are considered. The active detectors which can be implemented merely by using junction structures in the silicon are of particular interest.

In the second part, two implementations of programmable taps are presented. Chapters 4 and 5, respectively, discuss the Barrier-Modulated Tap and the piezoelectric Junction FET, which are both active junction devices with an electronically controllable output. These chapters include the discussion on physical operation, modeling, implementation, and verification by experimental results. In addition, technological aspects are considered.

The final part discusses the architecture of the complete programmable filter in the ZnO-SiO_2-Si layered structure. In Chapter 6, a general discussion about the structure of a programmable filter, which uses the detectors presented in Chapters 4 and 5, is given. Attention is paid to the generation of SAWs and a new IDT configuration is introduced, which is compatible with the new detector structures.

Chapter 2

THE ACOUSTOELECTRIC SYSTEM

2.1 INTRODUCTION

In this chapter, the combined acoustic and electric phenomena which originate when a Rayleigh wave travels along the surface of a ZnO-SiO_2-Si layered structure are considered. The investigation of SAWs in a layered system involving piezoelectric and semiconducting layers is not a trivial one. The mechanical displacements induce electric fields in the piezoelectric ZnO layer, which penetrate into the semiconducting silicon substrate. As a consequence, an interaction takes place between the acoustic wave and the mobile charge carriers in the semiconductor, which not only results in a perturbation of the charge carrier distribution, but also in a perturbation of the wave propagation itself.

Initially, the interactions between (bulk) acoustic waves and charge carriers were investigated in piezoelectric semiconductors [41, 42]. In this case, a one-dimensional approach can be applied. Two-dimensional wave-carrier interactions involving SAWs were first investigated in piezoelectric insulators covered with a thin, semiconducting film [43], and in air-gap structures [44]. Although many interesting acoustoelectric phenomena can be observed, three effects have been given most attention because of their practical applicability. These are the acoustic amplification caused by linear, wave–carrier interactions; the transverse acoustoelectric voltage (TAV) caused by nonlinear effects, which induce DC terms in the wave–

carrier interaction; and the parametric effects caused by nonlinear effects, which induce AC terms at the sum and the difference frequencies of two SAWs. Especially in the latter field, the ZnO-SiO_2-Si structure has successfully been applied to obtain the required acoustoelectric interactions [45].

In the theory described in this chapter, the weak-coupling approximation is used. Under weak-coupling conditions, it is assumed that the mechanical field variables, stress and strain, are not disturbed by the presence of free charge carriers or other electrical conditions. This assumption, which is valid when the piezoelectric coupling is small, simplifies the theory considerably. In addition, it is assumed that $kl_{free} \ll 1$, where k is the SAW wavenumber ($k = \omega/v_{ph}$, with v_{ph} the SAW phase velocity), and where l_{free} is the mean free path of the charge carriers. This implies that the carriers undergo many collisions when moving one wavelength, and a macroscopic theory can be applied. The charge carriers are then approached collectively, and mobility and effective carrier mass are meaningful concepts. This assumption is valid in silicon for frequencies below 5 GHz. If $kl_{free} > 1$ a microscopic theory must be used, where the individual phonon–electron interaction requires a quantum-mechanical treatment [46].

In the next section, a general discussion of the acoustoelectric field problem in the layered structure is given. Firstly, the basic equations of the individual layers are considered. Then a method to solve the equations is discussed, in which the polarization charge in the ZnO layer is replaced by a surface charge at the ZnO-SiO_2 interface. This method reduces the acoustoelectrical problem to a mere electrical one. In sections 2.3 and 2.4, the solution is considered for homogeneous silicon substrates of zero and arbitrary conductivity, respectively. In the latter section, the interaction phenomena between the SAW and the mobile charge carriers are examined; both linear and nonlinear phenomena are considered. In section 2.5 the theory is extended to inhomogeneous substrates, which involves the presence of active devices in the semiconductor. This theory is later used in the discussion of the active SAW detectors, which are described in Chapters 4 and 5. The influence of charges and traps in the layered structure is discussed in section 2.6. Besides the piezoelectric coupling mechanism in the ZnO layer, there is an additional coupling mechanism in the silicon substrate: the deformation potential coupling. This coupling mechanism is described in section 2.7.

2.2 THE ACOUSTOELECTRIC FIELD PROBLEM

2.2.1 Layered Configuration

The general layered configuration which is considered in this chapter is shown in Fig. 2.1. A Cartesian coordinate system x_1,x_2,x_3 is introduced such that the SiO_2-Si interface is located at the plane $x_3 = 0$.

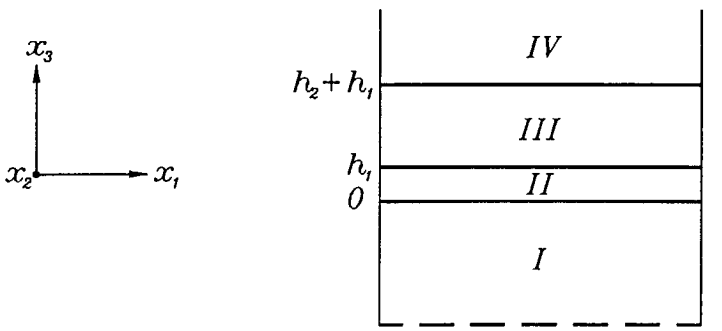


Figure 2.1: *The considered layered configuration.*

The semi-infinite substrate (region I) is a nonpiezoelectric, semiconducting silicon layer. Silicon has a cubic crystal lattice, which is anisotropic and of class *m3m*. On top of the silicon substrate an amorphous SiO_2 layer (region II) with thickness h_1 is present. This layer can be considered as an isotropic medium. The surface of the structure is covered with a piezoelectric ZnO layer (region III) of thickness h_2. The sputtered ZnO layer has a hexagonal crystal lattice of class *6mm* with a preferred c-axis orientation perpendicular to the surface. Above the ZnO layer a semi-infinite vacuum is assumed (region IV).

The elastic and electrical properties of this layered structure are determined by the material constants and the thicknesses of the individual layers. The dominant parameters are the stiffness tensor c^E_{ijkl} (determined at constant electric field), the dielectric permittivity tensor ϵ^S_{ik} (determined at constant strain), and the mass density ρ_m. The acoustoelectric coupling is determined by the piezoelectric tensor e_{kij}. The values of the constants for the various layers at room temperature are given in Table 2.1, in which the Voigt notation for the tensor parameters is used. The values for the Si and SiO_2 layers are from Ono *et al.* [47]. The ZnO constants are from Carlotti *et al.* [48], who derived the data from sputtered ZnO films. The ZnO film constants are 10% to 25% lower than the corresponding

bulk constants. All theoretical results presented in this thesis have been obtained using the material constants of Table 2.1.

Table 2.1: *Material constants at $T = 300K$ of silicon, silicon dioxide (fused quartz), and thin-film ZnO.*

		Si	SiO_2	ZnO
ρ_m	10^3 kg/m^3	2.33	2.20	5.72
c_{11}^E	10^{11} Pa	1.66	0.785	1.57
c_{13}^E		0.639	0.161	0.83
c_{33}^E		1.66	0.785	2.08
c_{44}^E		0.796	0.312	0.38
e_{31}	C/m^2			−0.51
e_{33}				1.22
e_{15}				−0.45
ϵ_{11}	10^{-10} F/m	1.03594	0.33468	0.737
ϵ_{33}		1.03594	0.33468	0.782

2.2.2 Basic Equations

The SAW propagation and the acoustoelectric interactions in this layered structure can be determined by solving a set of differential equations which describe the relationships between the mechanical field variables, stress and strain, and the electrical variables, electric field and electric displacement. The structure is assumed linear, time invariant and locally reacting. A coupling between the mechanical and electrical variables takes place through the piezoelectric behavior of the ZnO layer. In the following, the basic equations of each individual region are given. The tensor notation is used, and the summation convention on repeated subscripts is employed. A list of notations can be found at the end of this thesis.

For the solution of the wave propagation problem, the equation of motion, which is valid for the regions I to III, is essential

$$\rho_m \frac{\partial^2 u_i}{\partial t^2} = \frac{\partial T_{ij}}{\partial x_j} \qquad i,j = 1,2,3 \tag{2.1}$$

where

ρ_m	mass density	(kg/m^3)
u_i	particle displacement	(m)
t	time	(s)
T_{ij}	stress tensor	(Pa)
x_j	position in Cartesian coordinates	(m)

For the solution of the electric field, Poisson's equation must be applied

$$\frac{\partial D_i}{\partial x_i} = \rho_e \tag{2.2}$$

in which

D_i	electric displacement vector	(C/m^2)
ρ_e	electric charge density	(C/m^3)

The electric charge density ρ_e includes both the mobile charge carriers and the ionized atoms. Equation 2.2 is valid in all regions, but only in the conductive silicon substrate can the charge density be nonzero. Since the acoustic wave velocities are five orders of magnitude lower than the velocity of light, the magnetic fields can be ignored and electrostatic conditions can be assumed. In this case, the electric field components E_k (V/m) can be derived from a scalar potential ϕ (V)

$$E_k = -\frac{\partial \phi}{\partial x_k} \tag{2.3}$$

Equations 2.1 and 2.2 are the fundamental relations of the acoustoelectric field problem. The following equations specify the electrical and elastic characteristics of the layers. The piezoelectric and elastic properties of regions I to III are described by the constitutive relations

$$T_{ij} = c^E_{ijkl} S_{kl} - e_{kij} E_k \tag{2.4}$$

$$D_i = e_{ikl} S_{kl} + \epsilon^S_{ik} E_k \tag{2.5}$$

with $i, j, k, l = 1, 2, 3$, and the strain S defined as

$$S_{kl} = \frac{1}{2}\left(\frac{\partial u_k}{\partial x_l} + \frac{\partial u_l}{\partial x_k}\right) \tag{2.6}$$

and the material constants

c_{ijkl}^{E}	stiffness tensor at constant electric field	(Pa)
e_{kij}	piezoelectric tensor	(C/m^2)
ϵ_{ik}^{S}	dielectric permittivity tensor at constant strain	(F/m)

The symmetry in T_{ij} and S_{kl} leads to $c_{ijkl} = c_{jikl} = c_{ijlk} = c_{jilk}$ and $e_{kij} = e_{kji}$. For the nonpiezoelectric regions I and II, e_{kij} is zero, and the Eqs. 2.4, 2.5 reduce to Hooke's law and the definition of electric displacement, respectively.

In the conductive substrate (region I), mobile charge carriers are present, and the current equations must be added. Applying the Boltzmann approximation [49, p. 84] the free hole and electron densities at thermal equilibrium are given by

$$p = n_i \exp\left[\frac{q(\psi_F - \psi_i)}{k_B T}\right] \tag{2.7}$$

$$n = n_i \exp\left[\frac{q(\psi_i - \psi_F)}{k_B T}\right] \tag{2.8}$$

with

p	free hole density	(m^{-3})
n	free electron density	(m^{-3})
n_i	intrinsic electron density	(m^{-3})
q	electron charge; $q = 1.602 \cdot 10^{-19}$	(C)
ψ_F	potential associated with semiconductor Fermi level	(V)
ψ_i	potential associated with intrinsic Fermi level	(V)
k_B	Boltzmann constant; $k_B = 1.38 \cdot 10^{-23}$	(J/K)
T	temperature	(K)

As a result of the mobile charge carriers and electric fields in the silicon region, currents flow which are described by

$$J_{p,i} = pq\mu_p E_i + qD_p \frac{\partial p}{\partial x_i} \tag{2.9}$$

$$J_{n,i} = nq\mu_n E_i - qD_n \frac{\partial n}{\partial x_i} \tag{2.10}$$

with $i = 1, 2, 3$, and

$J_{p,i}$	hole current-density vector	(A/m^2)
$J_{n,i}$	electron current-density vector	(A/m^2)
μ_p	hole mobility	(m^2/Vs)
μ_n	electron mobility	(m^2/Vs)
D_p	hole diffusion coefficient	(m^2/s)
D_n	electron diffusion coefficient	(m^2/s)

and by the continuity equations for holes and electrons (generation and recombination effects are ignored)

$$\frac{\partial J_{p,i}}{\partial x_i} = -q\frac{\partial p}{\partial t} \tag{2.11}$$

$$\frac{\partial J_{n,i}}{\partial x_i} = q\frac{\partial n}{\partial t} \tag{2.12}$$

In addition to the equations given above, the boundary conditions at the interface planes between the different regions must be taken into account. At the interface between ZnO and the vacuum ($x_3 = h_1 + h_2$), a traction-free surface is assumed. Therefore, the normal component of the stress T_3 vanishes here. At all other interfaces, the normal stress component must be continuous. This also applies to the particle displacement u_i and the potential ϕ. Since no surface charges are assumed, the normal component of the electric displacement field D_3 must be continuous at each interface plane. Finally, since the SiO_2 and ZnO layers are insulating, no current is assumed for $x_3 > 0$ and the normal component of the current density must vanish at the silicon surface.

An analytical solution to the problem is severely hindered by the nonlinear relations, which describe the semiconductor properties, see Eqs. 2.7 to 2.12. A strong reduction of complexity is obtained when an insulating substrate is assumed. In this case, the semiconductor and current equations vanish, and a lossless propagation medium results. A solution to the propagation problem can then be obtained by determining the zeros of the determinant, which is constituted by the equations. Venema [50] has shown that pure Rayleigh-wave propagation is possible in this system, provided a proper wave direction with respect to the anisotropic silicon crystal is adopted. The general solutions are time-harmonic plane waves of the form

$$A \exp(jkbx_3) \exp[j(kx_1 - \omega t)] \tag{2.13}$$

in which k is wavenumber and ω the angular frequency. Since the considered layered system is dispersive, the wavenumber is not constant, but depends on ω. The wave motions described in Eq. 2.13 are confined to the sagittal (x_1, x_3) plane and have no components in the x_2-direction. With these straight-crested waves, the problem is reduced to a two-dimensional one. The constant factors A and b are fixed by the boundary conditions, the piezoelectric coupling, and the power of the wave. For (100) silicon, pure Rayleigh-wave propagation is possible in the [001] direction, whereas the (111) cut requires a $[11\bar{2}]$ propagation direction. The theoretical and experimental results given in this thesis are all based on the (100)[001] silicon system. The layered structure gives rise to higher-order wave modes with subsequent higher phase velocities. In this chapter, the term SAW is restricted to Rayleigh waves of which only the first mode is considered.

A more rigorous solution method is described by Ghijsen and Van den Berg [51, 52], who reduce the problem to a dual-boundary-value problem in ϕ and J at one of the interfaces. All numerical results in this thesis of the SAW velocity in a lossless configuration have been obtained using computer programs based on this method. With the inclusion of mobile charge carriers which interact with the SAW, a lossy medium results, and the complexity of the problem is highly increased.

Other methods, such as the perturbation [53] and the normal mode theory [54] can be applied, but these methods are limited to homogeneous substrates. When diffused and implanted regions are added, which represent active SAW detectors or other piezotronic elements, the problems become formidable and untractable when using the above-mentioned solution methods. For the investigation of such devices, only the potential distribution in the silicon region is of importance. Therefore, another method has been developed, in which the influence of the acoustic wave is reduced to a surface charge, which is located at the ZnO-SiO_2 interface. The problem is then reduced to a mere electrical one, in which only Poisson's equation has to be solved. This method is described in the next section.

2.2.3 Equivalent-Surface-Charge Method

The acoustoelectrical problem can be reduced to an electrical one, provided the weak-coupling approximation can be applied. This approximation assumes that the mechanical field variables are virtually unperturbed by the presence of free charge carriers in the silicon [55]. It can be applied as long as the piezoelectric coupling is small, which is the case in the considered ZnO layered structures.

Because of the piezoelectricity in the ZnO layer, the stress component S_{kl}, which is of the form of Eq. 2.13, creates a periodic piezoelectric polarization charge distribution ρ_{pe} in this layer. This charge distribution can be obtained with Eqs. 2.2 and 2.5. Since the ZnO layer is assumed insulating ($\rho_e = 0$)

$$\frac{\partial}{\partial x_i}(\epsilon_{ik}^S E_k) = -\frac{\partial}{\partial x_i}(e_{ikl} S_{kl}) \tag{2.14}$$

in which $\partial(\epsilon_{ik}^S E_k)/\partial x_i$ represents the dielectric polarization charge ρ_ϵ, and $\partial(e_{ikl}S_{kl})/\partial x_i$ the piezoelectric polarization charge ρ_{pe}. The piezoelectric polarization charge can be obtained by determining S_{kl} using one of the afore-mentioned analytical methods, assuming an insulating silicon substrate. In the weak-coupling approximation the mechanical variable S_{kl} is not perturbed by the presence of mobile charge carriers in the silicon, nor is the piezoelectric polarization charge ρ_{pe}. Therefore, the acoustoelectric interaction can be determined by inserting this piezoelectric charge in region III of the layered structure, which may now contain active junction devices and mobile charge carriers in the substrate. The electrical problem can be solved with the two-dimensional Poisson equation

$$\frac{\partial}{\partial x_i}(\epsilon_{ij}^S \frac{\partial \phi}{\partial x_j}) = \begin{cases} -q(p - n + N_{D+} - N_{A-}) & \text{in region I} \\ 0 & \text{in region II} \\ \dfrac{\partial}{\partial x_i}(e_{ikl} S_{kl}) & \text{in region III} \\ 0 & \text{in region IV} \end{cases} \tag{2.15}$$

in which N_{D+} and N_{A-} represent the ionized donor and acceptor densities, respectively.

This two-step method requires the solution of the mechanical field variable S_{kl} in the ZnO layer, in order to determine ρ_{pe} in the electrical solution method. However, for the interaction under consideration, we are only interested in the potential distribution in the SiO_2 and Si regions, or $x_3 < h_1$. For this situation a much simpler method can be applied, in which the piezoelectric polarization charge ρ_{pe} is replaced by an equivalent surface charge ρ_s, which is located at the ZnO-SiO_2 interface. This fictitious surface charge ρ_s is chosen such that it causes the same potential distribution for $x_3 < h_1$ as the volume charge ρ_{pe}.

The equivalent surface charge can be determined by placing an infinitesimally thin, perfectly conducting metal sheet at the plane $x_3 = h_1$.

This metal sheet completely screens the electric fields induced in the ZnO layer. As a result, the electric field E_k vanishes for $x_3 < h_1$. The screening is accomplished by an induced (surface) charge distribution ρ_{screen} at the metal shield, which exactly cancels the electric fields for $x_3 < h_1$. Because all relations are assumed linear, the resulting system can be considered as a superposition of a system only containing ρ_{pe} and a system only containing ρ_{screen}. Since $E_k = 0$ for $x_3 < h_1$ in the superposed system, ρ_{pe} and ρ_{screen} create an equal but opposite potential distribution in the SiO_2 and Si regions, as is illustrated in Fig. 2.2. As a result, the volume charge

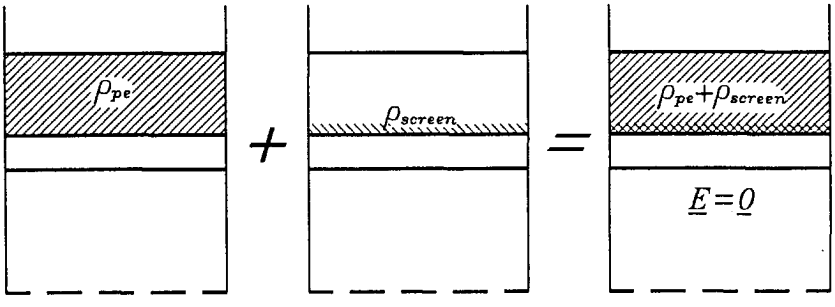


Figure 2.2: *Superposition of volume charge ρ_{pe} and screening charge ρ_{screen}.*

ρ_{pe} and the surface charge $-\rho_{screen}$ give the same potential distribution for $x_3 < h_1$, and the desired equivalent surface charge ρ_s is given by

$$\rho_s = -\rho_{screen} \tag{2.16}$$

The magnitude of ρ_s can be obtained analytically, provided the power of the wave and the piezoelectric coupling strength are known. This is discussed in the next section. The method described here is denoted as the *Equivalent-Surface-Charge* method.

It is here emphasized that the Equivalent-Surface-Charge (ESC) method assumes electrostatic conditions. When mobile charge carriers are involved, their dynamic properties should be taken into account. The static approach can be applied as long as the response or transit time of the carriers is much shorter than the wave period $1/\omega$. The ESC method can be applied at any interface below the ZnO layer. However, it must be taken into account that only the electrical solution beneath this interface is significant.

Summarizing, the Equivalent-Surface-Charge method reduces the acoustoelectric field problem in the semiconducting substrate of the ZnO-SiO_2-Si structure to a mere electric field problem. The polarization phenomena induced by the SAW in the ZnO layer are represented by an equivalent surface charge, which is located at the ZnO-SiO_2 interface. Since the weak-coupling approximation is assumed, this surface charge is not influenced by the electrical conditions in the silicon substrate. Therefore, it can most easily be determined in a layered structure with a homogeneous, insulating substrate. This is performed in section 2.3.1. With this equivalent surface charge, the acoustoelectrical problem in a layered structure with a complex substrate structure can be solved. The problem is reduced to solving the Poisson equation. This method can be implemented in numerical solution methods using finite-element or finite-difference techniques, which are commonly used for the two-dimensional calculations on active semiconductor devices. In the next subsection, the strength of the equivalent surface charge ρ_s is derived.

2.2.4 Piezoelectric Coupling

The coupling between the mechanical and electric field variables is determined by the strength of the piezoelectric phenomenon. The coupling strength determines the transduction efficiency of SAW generation and detection, and determines the strength of the interaction between the acoustic wave and the mobile charge carriers. The coupling strength can be represented by the piezoelectric or electromechanical coupling factor κ^2, which is proportional to the piezoelectric tensor e_{kij}, and is inversely proportional to the stiffness and dielectric tensors c_{ijkl} and ϵ_{ik} [56]. In the one-dimensional case of longitudinal bulk waves, it can be shown that this coupling factor is the ratio between the electric potential (or stored) energy and the total potential energy [57]. The coupling factor can be determined by observing the change in the phase velocity v_{ph} when the insulating piezoelectric medium is replaced by a perfectly conducting piezoelectric medium. In the latter case, the electric fields are short-circuited, which results in an unstiffening of the elastic material and in a decrease of the wave velocity. Therefore, the velocity change is a measure of the electric field strength in the unperturbed case. For weak-piezoelectric materials, $\Delta v/v \ll 1$, and the coupling factor can be approximated with $\kappa^2 \approx 2\Delta v/v$.

Essentially, the piezoelectric coupling factor is a bulk parameter. Therefore, it is not very convenient to use it in the SAW case. However, the piezoelectric coupling strength can still be determined by measuring the

relative velocity change $\Delta v/v$ when an infinitesimally thin, perfectly conducting plate is placed at the surface of the propagation medium [58]. Therefore, only the factor $\Delta v/v$ is used throughout this work. In the layered configuration, the coupling strength $\Delta v/v$ can be determined at any interface by inserting a conductive plate at the interface plane under consideration. The value of $\Delta v/v$ depends on the material parameters and the layer thicknesses. Computer programs, based on Ghijsen's method [52], have been developed to predict the $\Delta v/v$ value.

Two parameters, which are strongly related to $\Delta v/v$, and are of importance for the description of the coupling mechanism in the layered structure, are the potential ϕ and the equivalent surface charge ρ_s, both normalized to the SAW power flow P_a (W/m). It is assumed that they are plane wave solutions of the form

$$\phi = \phi_0(x_3) \exp[j(kx_1 - \omega t)] \tag{2.17}$$

$$\rho_s = \rho_{s0}(x_3) \exp[j(kx_1 - \omega t)] \tag{2.18}$$

These strongly related parameters can be derived from the normal mode theory [59]. This was performed by Kino and Wagers in order to determine the admittance of a transducer in a layered structure [60]. By using their theory, the values of ϕ_0^2/P_a and ρ_{s0}^2/P_a can be determined at any interface. The following discussion is restricted to the plane at $x_3 = h_1$. From [60] it can be derived that

$$\left.\frac{\phi_0^2}{P_a}\right|_{h_1} = \frac{4}{v_{ph}} \frac{\phi_0}{\rho_{screen,0}} \left.\frac{\Delta v}{v}\right|_{h_1} \tag{2.19}$$

where v_{ph} is the SAW phase velocity, and $\rho_{screen,0}$ the magnitude of the screening charge. A similar expression was found by Lakin [53], who applied the perturbation theory. The ratio $\phi_0/\rho_{screen,0}$ is a constant, which only depends on the material constants and the layer thicknesses. Because $\rho_{s0} = -\rho_{screen,0}$, Eq. 2.19 suffices to obtain both ϕ_0^2/P_a and ρ_{s0}^2/P_a.

In order to evaluate ϕ_0/ρ_{s0}, it is convenient to introduce an effective dielectric permittivity [61] in each layer, which is defined by

$$\epsilon_{eff}(x_3) = \frac{D_3(x_3)}{k\phi(x_3)} \tag{2.20}$$

These effective constants are purely electrical, and can be derived by solving the Poisson equation. The effective permittivity is continuous across each interface plane, except for the one which contains the equivalent surface charge. The equivalent surface charge causes a discontinuity in the

normal displacement field, and is thus related to the effective permittivities

$$\begin{aligned} \rho_s|_{h_1} &= \lim_{x_3 \downarrow h_1} D_3 - \lim_{x_3 \uparrow h_1} D_3 \qquad (2.21) \\ &= (\epsilon_{eff,U} - \epsilon_{eff,L}) \cdot k\phi(h_1) \end{aligned}$$

in which $\epsilon_{eff,U}$ and $\epsilon_{eff,L}$ are the upper and lower effective dielectric permittivities above and below the plane of interest (here $x_3 = h_1$) defined by

$$\epsilon_{eff,U}(h_1) = \lim_{x_3 \downarrow h_1} \frac{D_3(x_3)}{k\phi(x_3)} \qquad (2.22)$$

$$\epsilon_{eff,L}(h_1) = \lim_{x_3 \uparrow h_1} \frac{D_3(x_3)}{k\phi(x_3)} \qquad (2.23)$$

Equation 2.21 fixes the relation between the equivalent surface charge and the potential at $x_3 = h_1$, and is the central equation of the Equivalent-Surface-Charge method. By using Eqs. 2.19 and 2.21, the parameters ϕ_0^2/P_a and ρ_{s0}^2/P_a at $x_3 = h_1$ can now be expressed in the upper and lower effective permittivities at $x_3 = h_1$

$$\left.\frac{\phi_0^2}{P_a}\right|_{h_1} = \frac{4}{v_{ph}} \frac{1}{k(\epsilon_{eff,U} - \epsilon_{eff,L})_{h_1}} \left.\frac{\Delta v}{v}\right|_{h_1} \qquad (2.24)$$

$$\left.\frac{\rho_{s0}^2}{P_a}\right|_{h_1} = \frac{4}{v_{ph}} k(\epsilon_{eff,U} - \epsilon_{eff,L})_{h_1} \left.\frac{\Delta v}{v}\right|_{h_1} \qquad (2.25)$$

The ratio ρ_{s0}^2/P_a can be considered as a new coupling factor. It should be noted, that in the weak-coupling case, ϕ_0 is affected by the presence of free charge carriers, but ρ_{s0} is not. By using Eq. 2.25 in the unperturbed case to obtain ρ_{s0}, and inserting this in Eq. 2.21 with the effective permittivities of the perturbed case, the potential distribution in the perturbed case can be calculated. In the next section, the unperturbed case (homogeneous substrate, free of charge) is considered in order to evaluate ρ_{s0} in the layered structure. This ρ_{s0} can then be used in the subsequent sections 2.4 and 2.5, where the acoustoelectric field problem for conductive and inhomogeneous substrates is examined.

2.3 HOMOGENEOUS INSULATING SUBSTRATE

2.3.1 Equivalent Surface Charge

The equivalent surface charge ρ_{s0} can most easily be determined in a layered structure with a homogeneous, insulating substrate. The configuration shown in Fig. 2.1 is considered. For the determination of ρ_{s0}, the upper and lower effective dielectric permittivities at $x_3 = h_1$ must be known. Starting point is the Poisson equation given in 2.15. Because there are no free charge carriers, and the piezoelectric polarization charge is replaced by an equivalent surface charge, the right-hand side of Eq. 2.15 equals zero for all regions. The current equations can be ignored. Since the materials under consideration either have a cubic (region I), an isotropic (region II) or an hexagonal lattice (region III), only $\epsilon_{ii} \neq 0$. Only plane wave solutions as given in Eq. 2.17 are considered, which results in the Laplace equation

$$\epsilon_{33}\frac{\partial^2\phi}{\partial x_3^2} - k^2\epsilon_{11}\phi = 0 \tag{2.26}$$

The general solution of this differential equation, ignoring the harmonic factor $\exp[j(kx_1 - \omega t)]$, is

$$\phi^l = A_1^l \exp(\gamma^l x_3) + A_2^l \exp(-\gamma^l x_3) \qquad l{=}\mathrm{I,II,III,IV} \tag{2.27}$$

with

$$\gamma^l = k\frac{\epsilon_p^l}{\epsilon_{33}^l}; \quad \epsilon_p^l = \sqrt{\epsilon_{11}^l \epsilon_{33}^l}$$

By using Eqs. 2.22, 2.23 and the proper boundary conditions, it can be shown that for $x_3 = h_1$

$$\epsilon_{eff,L} = \epsilon_p^{II}\frac{\epsilon_p^{II} - \epsilon_{eff}^I \coth(\gamma^{II}h_1)}{\epsilon_{eff}^I - \epsilon_p^{II}\coth(\gamma^{II}h_1)} \tag{2.28}$$

$$\epsilon_{eff,U} = \epsilon_p^{III}\frac{\epsilon_p^{III} + \epsilon_{eff}^{IV} \coth(\gamma^{III}h_2)}{\epsilon_{eff}^{IV} + \epsilon_p^{III}\coth(\gamma^{III}h_2)} \tag{2.29}$$

in which ϵ_{eff}^I, ϵ_{eff}^{IV} are the lower and upper effective permittivities of regions I and IV, defined at $x_3 = 0$ and $x_3 = h_1 + h_2$, respectively. In the current situation, regions I and IV are semi-infinite and contain no free charge. In this case, the effective permittivities reduce to the conventional dielectric constants: $\epsilon_{eff}^I = -\epsilon_p^I$, and $\epsilon_{eff}^{IV} = \epsilon_p^{IV}$. By using Eq. 2.25, the

equivalent surface charge at the reference plane can now be obtained

$$\left.\frac{\rho_{s0}^2}{P_a}\right|_{h_1} = \frac{4}{v_{ph}} k(\epsilon_p^{III} \frac{\epsilon_p^{III} + \epsilon_p^{IV} \coth(\gamma^{III} h_2)}{\epsilon_p^{IV} + \epsilon_p^{III} \coth(\gamma^{III} h_2)} + \\ + \epsilon_p^{II} \frac{\epsilon_p^{II} + \epsilon_p^{I} \coth(\gamma^{II} h_1)}{\epsilon_p^{I} + \epsilon_p^{II} \coth(\gamma^{II} h_1)}) \left.\frac{\Delta v}{v}\right|_{h_1} \quad (2.30)$$

The piezoelectric coupling $\Delta v/v$ for the ZnO-SiO_2-Si structure under consideration can readily be obtained with the methods developed by Ghijsen [52]. In Fig. 2.3, $\Delta v/v$ is presented as a function of the normalized ZnO thickness ωh_{ZnO} for two constant, normalized SiO_2 thicknesses: $\omega h_{ox} = 60$ and 1200 rad m/s. An optimal piezoelectric coupling results, if $\omega h_{ZnO} \approx 8000$ rad m/s. By using the $\Delta v/v$ information presented in Fig. 2.3, the equivalent surface charge given in Eq. 2.30 can be determined. Since the layer thicknesses are normalized to ω, it is convenient to normalize ρ_{s0} also to ω. The resulting $\rho_{s0}^2/\omega P_a$ as a function of the ωh_{ZnO} is shown in Fig. 2.4. The charge ρ_{s0} can now be implemented in the Equivalent-Surface-Charge method to obtain the electric field distribution below the ZnO layer in a layered structure with an arbitrary Si substrate.

2.3.2 Potential Solution

In this section, the Equivalent-Surface-Charge method is applied in order to solve the electric field problem for $x_3 < h_1$ in the layered structure shown in Fig. 2.1 with a homogeneous, insulating substrate. The general solution of the potential distribution is given in Eq. 2.27. The coefficients $A_{1,2}^l$ can uniquely be determined for each region by using the boundary conditions and the equivalent surface charge. Calculations like these, for a number of different boundary conditions in the three-layered configuration, were presented by Venema *et al.* [62] in order to determine the static capacitance of an IDT.

In the following discussion, the potential distribution in the substrate and the SiO_2 layer is calculated using the ESC method with the plane $x_3 = h_1$ as reference. The boundary conditions involve the continuity of the potential ϕ and of the normal electric displacement component D_3 at the interfaces $x_3 = 0$ and $x_3 = h_1 + h_2$. The potential is also continuous at $x_3 = h_1$, but since this plane contains the equivalent surface charge, the displacement field is discontinuous. For $x_3 \to \infty$ and $x_3 \to -\infty$, the potential must vanish. With these conditions, the potential distribution for $x_3 < h_1$ can be derived.

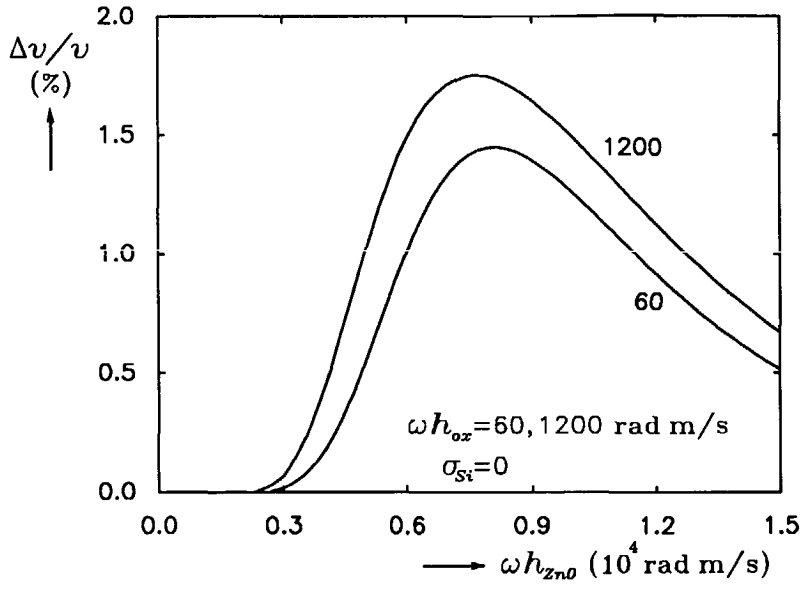


Figure 2.3: *The piezoelectric coupling $\Delta v/v$ vs. ωh_{ZnO} for different ωh_{ox} values.*

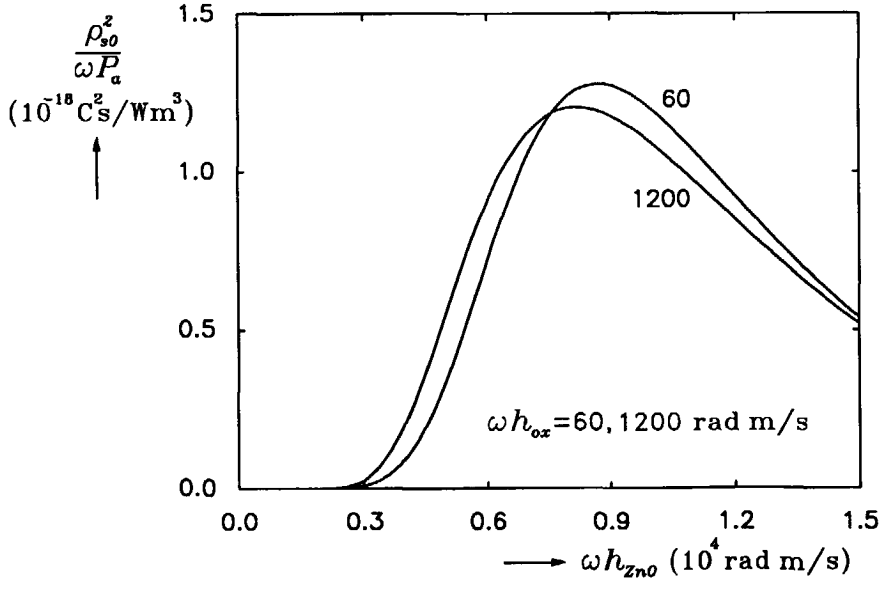


Figure 2.4: *The normalized, equivalent surface charge $\rho_{s0}^2/\omega P_a$ vs. ωh_{ZnO} for different ωh_{ox} values.*

For the insulating Si substrate, this becomes ($x_3 < 0$):

$$\phi(x_3) = \phi(0)\exp(\gamma^I x_3) \tag{2.31}$$

and for the silicon-dioxide layer ($0 < x_3 < h_1$):

$$\phi(x_3) = [\cosh(\gamma^{II} x_3) - \frac{\epsilon^I_{eff}}{\epsilon^{II}_p} \sinh(\gamma^{II} x_3)]\phi(0) \tag{2.32}$$

in which ϵ^I_{eff} is the lower effective permittivity of region I defined at $x_3 = 0$. In the silicon region, $\epsilon_{11} = \epsilon_{33}$, and the decay factor γ^I is identical to k. As a consequence, the normal and longitudinal electric fields in the silicon have equal magnitudes, but are 90 degrees out of phase. Their penetration depth is in the order of one wavelength.

The remaining unknown in Eqs. 2.31 and 2.32 is the potential $\phi(0)$ at $x_3 = 0$. This variable can be derived from the equivalent surface charge ρ_{s0} given in section 2.3.1. By using Eq. 2.21 with the effective permittivities given in Eqs. 2.28 and 2.29, $\phi(h_1)$ is obtained. The required $\phi(0)$ can then be found using Eq. 2.32, which concludes the solution process.

A similar method can be followed to obtain the potential distribution for $x_3 < h_1$ for a homogeneous, semiconducting substrate. One has to find the proper upper and lower effective permittivities, and use them in Eq. 2.21, together with the ρ_{s0} given in section 2.3.1. This results in the $\phi(0)$ in the perturbed case which is described in the next section.

2.4 HOMOGENEOUS SEMICONDUCTING SUBSTRATE

In this section, the acoustoelectric field problem is considered when there are mobile charge carriers in the substrate. A homogeneous substrate is assumed with a uniform carrier density, which corresponds to a uniformly doped semiconductor under flat-band conditions.

Because of the penetrating electric fields induced by the SAW, a force acts on the mobile charge carriers (electrons and holes), which causes a redistribution of the carrier density. As a result, a periodic space-charge distribution is created. In fact, the moving charge carriers tend to cancel the acoustically induced fields. Because the SAW fields have both a longitudinal and transverse component, two-dimensional charge bunches originate, which try to screen the electric field components from penetrating into the substrate.

The screening of the induced fields by the mobile carriers is limited by two factors: *diffusion* and *relaxation*. The static bunching of carriers

is counteracted by diffusion, which is caused by the thermal motion of the carriers. Because of this thermal motion, the minimum dimensions of charge bunches are limited by the Debye screening length L_D. For n-type silicon the Debye length is given by

$$L_D = \sqrt{\frac{\epsilon_{Si} k_B T}{q^2 N_D}}$$

where N_D is the donor concentration, and ϵ_{Si} the dielectric permittivity of silicon ($\epsilon_{Si} = \epsilon_{11} = \epsilon_{33}$ for silicon). Under flat-band conditions, this characteristic length represents the minimum length which is required by the space charge, in order to decrease the external fields by exp (-1). If the SAW wavelength is less than this characteristic length, the charge bunches are smeared out, which is caused by thermal motion, and no screening is achieved. For the SAW field, the substrate then acts as an insulator.

The dynamic properties of the bunches are limited by the response time of the charge carriers. The response of the charge carriers to the external fields is not instantaneous, but depends on the dielectric and conductive properties of the semiconductor. The dynamic screening is determined by the dielectric relaxation frequency ω_c defined as

$$\omega_c = \frac{\sigma_{Si}}{\epsilon_{Si}}$$

where σ_{Si} ($= N_D q \mu_n$ for n-type silicon) is the silicon conductivity (S/m). For SAW frequencies much smaller than ω_c, the response of the carriers can be considered to be instantaneously, and a static approach is legitimate. The screening is then only limited by diffusion effects. For SAW frequencies much higher than ω_c, the response of the carriers is too slow to screen the penetrating fields. For the SAW fields, the substrate can then again be considered as an insulator.

Thus far, the average velocity of the carriers has been assumed to be zero. However, when an external bias field is present, the carriers have an average drift velocity. Because of the absence of a DC current path normal to the layered structure, only drift fields in the x_1-direction can occur. For the acoustoelectric interactions, it is convenient to use a reference frame which moves at the carrier drift velocity $v_{d,1}$. Because the drift velocities are much smaller than the velocity of light, relativistic effects can be ignored and a Galilean transformation can be applied. This results in a Doppler shift of the SAW frequency which the carriers experience locally

$$\omega_{eff} = \left|1 - \frac{v_{d,1}}{v_{ph}}\right| \omega = |\delta| \omega$$

When a drift field is present, the dynamic screening must be related to this ω_{eff}.

In the previous discussion, it was assumed that only mobile carriers are involved in the redistribution of the charge density. Hutson [41] pointed out that part of the space-charge distribution may involve charge in bound states in the energy bandgap. However, at room temperature, it can be assumed that all donor and acceptor levels are ionized, and only the redistribution of mobile charge has to be considered. The carrier trapping and its effect on acoustoelectric phenomena are discussed in section 2.6.

2.4.1 Small-Signal Theory

For the determination of the potential distribution in the semiconducting substrate, the Boltzmann relations and current equations given in section 2.2.2 must be applied. From the exponential relationships between the potential and the carrier densities in the Boltzmann relations, and from the product terms between the modulated carrier densities and the modulating electric field in the current equations, it can readily be observed that the problem is highly nonlinear. In addition, the currents in the substrate make this region a lossy medium.

However, if the RF potential induced by the SAW is small, and if the losses per wavelength are negligible, a linear theory can be applied. This theory was originally developed by Hutson *et al.* [41]. In the following discussion, ϕ represents the small-signal SAW potential, which is assumed to vary as in Eq. 2.17. External DC bias fields are not treated explicitly, but are taken into account in the drift velocity of the carriers $v_{d,1}$. Because of the small-signal approach, the exponential relations $\exp(q\phi/k_BT)$ in Eqs. 2.7 and 2.8 can be replaced by $1+q\phi/k_BT$. In this case, the relations are represented by

$$p, n = p_0, n_0 + p_1, n_1$$

in which p_0, n_0 are the equilibrium densities, and p_1, n_1 the variations in the densities, which are proportional to the RF potential. The current equations can be linearized by ignoring all second-order terms

$$J_{p,i} = p_0 q\mu_p E_i + p_1 q v_{d,i} - qD_p \frac{\partial p_1}{\partial x_i} \tag{2.33}$$

$$J_{n,i} = n_0 q\mu_n E_i - n_1 q v_{d,i} + qD_n \frac{\partial n_1}{\partial x_i} \tag{2.34}$$

with $i = 1, 3$. The total small-signal charge density is $q(p_1 - n_1)$, and is

inserted in Poisson's equation

$$\frac{\partial^2\phi}{\partial x_1^2} + \frac{\partial^2\phi}{\partial x_3^2} = -\frac{q(p_1 - n_1)}{\epsilon_{Si}} \tag{2.35}$$

The current equations 2.33, 2.34 and the current continuity equations 2.11, 2.12 together with Poisson's equation, compose a sixth-order system of linear differential equations. The general solution of this system is given by (ignoring the $\exp[j(kx_1 - \omega t)]$ term)

$$\phi = \sum_{m=1}^{6} A_m \exp(\gamma_m x_3) \tag{2.36}$$

It is not possible to compose one sixth-order differential equation in ϕ explicitly, but by assuming that the carrier densities have the same format as ϕ, the decay variables γ_m can be found [63].

The treatment of both majority and minority carriers is required, when their concentrations are of comparable magnitude. For the flat-band condition, this means that the semiconductor must be near intrinsic. However, the doping concentrations commonly used for IC fabrication are generally larger than 10^{20} m^{-3}. In this case, the concentrations of majority and minority carriers in silicon differ by more than seven orders of magnitude. The influence of the minority carriers can then be ignored. To obtain more insight into the problem, only majority carriers are now considered, and an extrinsic n-type silicon substrate is assumed. By inserting Eqs. 2.34 and 2.35 into the continuity equation for electrons given in Eq. 2.12, a fourth-order differential equation in ϕ results

$$\frac{\partial^4\phi}{\partial x_3^4} - k^2(1+\alpha^2)\frac{\partial^2\phi}{\partial x_3^2} + k^4\alpha^2\phi = 0 \tag{2.37}$$

$$\alpha^2 = (1 + \frac{\omega_c\omega_{Dn}}{\omega^2} - j\frac{\delta\omega_{Dn}}{\omega})$$

The parameters ω_c and δ are the dielectric relaxation frequency and the Doppler shift, whereas ω_{Dn} is the diffusion frequency for electrons defined as

$$\omega_{Dn} = \frac{v_{ph}^2}{D_n}$$

The general solution corresponds to Eq. 2.36, with m ranging from 1 to 4. The decay constants in the silicon substrate γ_m are given by

$$\gamma_{1,2} = \pm k$$

$$\gamma_{3,4} = \pm\alpha k$$

Since the RF potential must vanish for $x_3 \rightarrow -\infty$, the negative values of γ_m must be rejected. An extra boundary condition at the SiO_2-Si interface is set by the current: since no currents flow in the insulating oxide, the normal component of the conduction current density J_3 must vanish at $x_3 = 0$. This results in the condition (at $x_3 = 0$)

$$\frac{\partial^3 \phi}{\partial x_3^3} - k^2\left(\frac{\omega_c \omega_{Dn}}{\omega^2} + 1\right)\frac{\partial \phi}{\partial x_3} = 0 \tag{2.38}$$

With the general solution of ϕ, and the boundary conditions, the potential distribution for $x_3 < h_1$ can now be determined. The potential distribution in the SiO_2 layer is identical to the insulating substrate case, and is given in Eq. 2.32. The potential in the semiconducting substrate is quite different:

$$\phi(x_3) = \frac{\exp(\alpha k x_3) - j\xi \exp(k x_3)}{1 - j\xi}\phi(0) \tag{2.39}$$

with

$$\xi = \alpha \frac{\delta\omega}{\omega_c}$$

For frequencies below 500 MHz and doping levels higher than 10^{20} m^{-3}, $\omega^2 \ll \omega_c \omega_{Dn}$ which corresponds to $kL_D \ll 1$. The variables α and ξ can then be approximated by

$$\alpha \approx \frac{1}{kL_D}$$

$$\xi \approx \delta\sqrt{\frac{\omega_{Dn}}{\omega_c}} \approx \alpha\frac{\delta\omega}{\omega_c}$$

When considering Eq. 2.39, it is observed that the potential distribution in the semiconducting substrate is composed of a component with a decay constant corresponding to the Debye length L_D, and a component with a decay constant corresponding to the SAW wavelength. The ratio between the components is fixed by ξ. If no drift field is present, the second component is very small, and can usually be ignored. The resulting field penetration is in the order of a Debye length, which is smaller than 0.5 μm for $N_D > 10^{20}$ m^{-3}. Because the charge bunch dimensions are determined by the penetration depth and the wavelength, the condition $kL_D \ll 1$ implies that the bunches are practically planar. From Eq. 2.39 it can be derived that

$$|E_1| = kL_D|E_3|$$

which indicates that the normal fields dominate in the acoustoelectric interaction.

In order to find the remaining unknown $\phi(0)$ in Eq. 2.39, the Equivalent-Surface-Charge method is used. Therefore, the upper and lower effective permittivities at $x_3 = h_1$ must be determined. It should be noted that the ESC method assumes electrostatic conditions. In order to use this method for the conductive substrate, the relaxation time of the charge carriers must be much shorter than the wave period. This implies $|\delta|\omega \ll \omega_c$. The effective permittivity of the semiconductor at $x_3 = 0$ can be obtained using Eq. 2.39

$$\epsilon^I_{eff} = \lim_{x_3 \uparrow 0} \frac{D_3(x_3)}{k\phi(x_3)} = -\epsilon_{Si} \frac{\alpha - j\alpha\, \delta\omega/\omega_c}{1 - j\alpha\, \delta\omega/\omega_c} \tag{2.40}$$

The effective permittivity contains an imaginary term, which is caused by the lossy behavior of the medium. This imaginary term determines the attenuation and amplification properties of the layered structure, which are discussed in the next section. If the conditions $|\delta|\omega \ll \omega_c$ and $kL_D \ll 1$ are valid, the effective permittivity at $x_3 = 0$ can be approximated by a real value

$$\epsilon^I_{eff} \approx -\epsilon_{Si}\alpha \approx -\frac{\epsilon_{Si}}{kL_D} \tag{2.41}$$

By inserting this value in Eq. 2.28, the $\epsilon_{eff,L}$ at $x_3 = h_1$ can be found. The upper effective permittivity $\epsilon_{eff,U}$ has not changed, and is identical to the insulating substrate case given in Eq 2.29 with $\epsilon^{IV}_{eff} = \epsilon^{IV}_p$. By using these effective permittivities, together with ρ_{s0} which was derived in section 2.3.1, $\phi(h_1)$ and thus $\phi(0)$ can be obtained by using Eq. 2.21. In Fig. 2.5 the penetration of the potential for different silicon conductivities is shown. This case was calculated for a configuration with normalized layer thicknesses of $\omega h_{ZnO} = 8000$ rad m/s and $\omega h_{ox} = 60$ rad m/s, at a frequency of 100 MHz, and a SAW power flow of 1 mW/m.

2.4.2 Acoustoelectric Phenomena

In this section, the physical effects that originate from the acoustoelectric interaction are discussed. These effects are dominated by the nonlinear properties of the semiconductor. For small power levels, the second-order terms $n_1 E_i$ and $p_1 E_i$ $(i = 1, 3)$ in the electron and hole current densities (Eqs. 2.33, 2.34) give rise to nonlinear effects. At low power levels, these effects can be evaluated by an extension of the linear theory [64, 65]. At high power levels, the nonlinearities in the carrier densities, given by the Boltzmann relations, dominate.

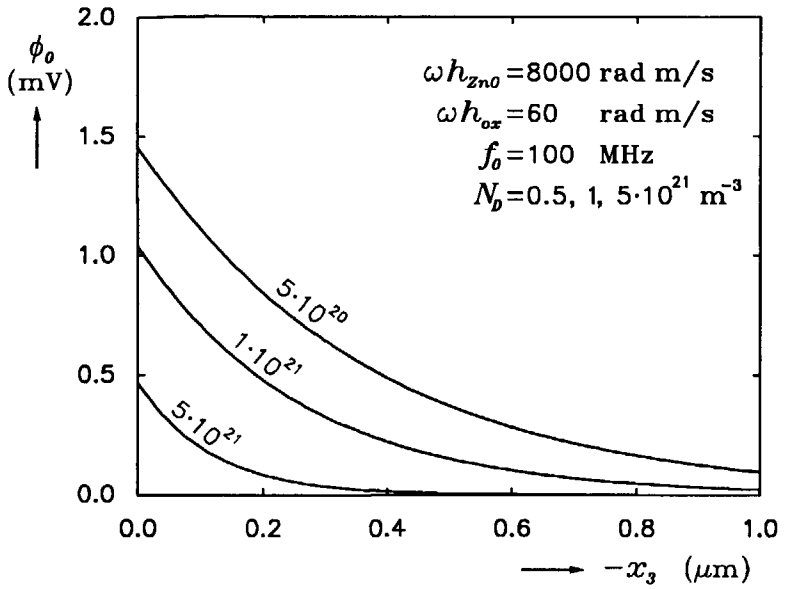


Figure 2.5: *Potential penetration in silicon substrate at 100 MHz for various doping concentrations.*

The mixing terms give rise to DC effects and to effects at twice the operating frequency. If more than one wave is involved, parametric coupling between the waves is possible, which produces signals at the sum and difference frequencies of the waves. In the following text an overview is given of the most important acoustoelectric phenomena.

(i) Velocity perturbation

The screening of the penetrating electric fields by the mobile charge carriers results in an unstiffening of the elastic material, which produces a decrease of the phase velocity. The screening effect shows up as a change in the elastic tensor c_{ijkl}. The linear theory can be applied to calculate this change [42]. Since the velocity change depends on the amount of screening, it is affected by diffusion, relaxation and drift of the mobile charge carriers.

(ii) Attenuation and amplification

Because the semiconductor is a lossy medium, the wave loses power during propagation, which results in a gradual decrease of the wave amplitude.

Because of the finite response time of the mobile carriers, the phase difference between the electric fields and the induced currents becomes less than 90 degrees, which results in Joule heating and attenuation of the SAW amplitude. However, when a drift field is applied parallel to the direction of the wave, the phase shift becomes more than 90 degrees when the carrier drift velocity exceeds the SAW phase velocity. In this case, power is transferred from the drifting carriers to the wave, which results in an amplification of the SAW. The (bulk) wave attenuation was first described by Hutson *et al.* [41], who applied the linear theory, and was further extended by White [66] for the wave amplification. The theory of SAW amplification in layered structures was presented by Ingebrigtsen [43], and was further evaluated by Visser *et al.* [67] in the ZnO-SiO_2-Si layered configuration.

The attenuation and amplification can be treated by constructing a dispersion relation which contains the effective permittivities. However, since the effects are maximal when the effective frequency is comparable to the dielectric relaxation frequency, the static approach of the Equivalent-Surface-Charge method cannot be used. Instead the piezoelectric effect must be included in the upper effective permittivity [67].

Because the SAW has a transverse component, amplification can also be realized by applying a drift field normal to the wave propagation [68]. However, because of the absence of a DC current path normal to the surface of a layered structure, this mechanism is restricted to pulsed operation, or to piezoelectric semiconductors.

(iii) Acoustoelectric field

It has already been mentioned that the nonlinear terms give rise to DC electric fields. This DC electric field was first described by Weinreich [69], who related the DC field strength to the attenuation factor in the case of longitudinal bulk waves. In this case, the generated DC field can be explained by considering the conservation of momentum: as the wave is attenuated it loses momentum, which is transferred to the mobile charge carriers. When the wave is amplified, the field direction reverses. Because the Acoustoelectric (AE) Field adds to the external, longitudinal drift field, a nonohmic behavior is found, and a kink in the IV-characteristic occurs when the attenuation changes into amplification [70].

In the case of a SAW, in addition to a longitudinal AE field, a transverse AE field is experienced, which is caused by the normal component of the SAW. Because of the absence of a normal DC current path, the transverse AE field in the layered configuration appears as a Transverse

Acoustoelectric Voltage (TAV), which can only be measured under transient (pulsed) operation conditions. The direction of the field is such that it induces a weak depletion of the semiconductor surface. Both the longitudinal and transverse acoustoelectric field can be related to the attenuation factor, as was pointed out by Gulyaev *et al.* [71]. Since the acoustoelectric field strongly depends on the electronic conditions of the semiconductor surface, it can be used for the characterization of this surface [72].

(iv) Parametric interaction

When more than one wave is present in the layered system, a nonlinear coupling occurs between the electric fields of one wave, and the charge modulation induced by another wave. This parametric effect produces signals at the sum and difference frequencies of the initial waves. It was shown by Wang *et al.* [64] that longitudinal parametric effects, introduced by the interaction between the longitudinal electric fields and the charge carriers, only occur when there is a longitudinal drift field. In practice, only the transverse parametric effects are employed, which can be detected with IDTs having a proper spatial periodicity, placed in the interaction region. When the waves are counterpropagating, a convolution between the two input waves is obtained [73]. When the two frequencies of the waves are identical, the spatial periodicity of the product term at twice the input frequency vanishes, and the normal convolution field can capacitively be coupled to a metal plate electrode on top of the layered structure. A detailed description of such a degenerate convolver in the ZnO-SiO_2-Si structure is given in Reference [74]. At high signal levels, the parametric interaction is caused mainly by the nonlinearity of the space-charge layer capacitance, in which case the operation is similar to a distributed varactor.

When the metal electrode in the interaction region is excited at twice the input frequency, a parametric coupling is obtained between the traveling waves and the normal electric fields of the pump signal. Thus, time reversal and parametric amplification of the traveling-wave input signal can be achieved. A parametric amplifier in the ZnO-SiO_2-Si structure is described in Reference [75].

(v) Charge transfer

When high power levels are applied ($\phi \gg k_B T/q$), the mobile carriers become trapped in the propagating potential wells. This results in high peaks in the charge distribution. In the case of bulk waves, the majority

carriers can no longer move freely but are transferred by the wave at the phase velocity v_{ph} [76]. For SAWs the trapping is not possible because of the absence of a potential barrier for carriers normal to the wave direction. However, if an inversion layer is created, the minority carriers are trapped at the surface and a transfer of charge becomes feasible. This was first described by Gaalema *et al.* [77] and resulted in the development of Acoustic-Charge-Transfer devices.

The nonlinear phenomena, which are determined by the interactions between the charge bunches and the electric fields, are maximal when the effective frequency is of the same order of magnitude as the dielectric relaxation frequency. For frequencies much higher than ω_c, the mobile carriers are hardly perturbed, and the currents drop to zero. For frequencies much lower than ω_c, the electric field drops to zero because of screening which restricts the ranges of operation frequencies and doping levels. For frequencies below 500 MHz, rather high-resistivity semiconductors ($\sigma_{Si} < 1$ S/m) are required to observe the nonlinear effects [78]. However, by applying an external DC bias field normal to the surface, a weakly depleted layer can be created at the silicon surface, in which the conditions for acoustoelectric interactions are optimized. The effect of band bending is discussed in the next section.

2.5 INHOMOGENEOUS SEMICONDUCTING SUBSTRATE

2.5.1 Band Bending

In the previous section, flat-band conditions were assumed and the conductivity is uniform throughout the semiconductor. However, if a DC field is applied normal to the layered structure, the energy bands in the semiconductor will bend. As a result, the equilibrium charge distribution, and thus the conductivity, vary and the silicon substrate becomes inhomogeneous in the x_3-direction.

The band bending is induced by the static potential ψ (V) measured with respect to the intrinsic Fermi level. In the bulk, $\psi = 0$ V, whereas at the semiconductor surface $\psi = \psi_s$. The static space charge induced by the band bending, can be obtained by solving the one-dimensional Poisson equation. For the sake of simplicity, four extreme cases where the surface potential is shifted from a positive to a negative value are discussed. For an n-type semiconductor, this shift subsequently results in an accumulation, a flat-band, a depletion, and an inversion condition.

(i) Accumulation

When the band bending in an n-type semiconductor surface is positive, the majority carrier density at the surface increases, and an accumulation of electrons at $x_3 = 0$ results. The effective conductivity experienced by the RF electric fields is increased, and leads to a larger amount of screening. When there is a strong accumulation, the silicon substrate can be considered to be a perfect conductor, and the field penetration drops to zero.

(ii) Flat-band

Under flat-band conditions, the carrier concentration in the silicon substrate is uniform and it can, therefore, be considered homogeneous. This case was examined in the previous section.

(iii) Depletion

When the surface is negatively biased, the majority carriers are driven from the surface into the bulk, and a fixed space-charge region of ionized donors remains. This region is completely depleted of mobile charge carriers, and can be considered to be an extra insulating layer between the SiO_2 layer and the silicon substrate. This layer can simply be included in the small-signal theory presented in section 2.4.1. The effective permittivity at $x_3 = 0$ of the lower part is derived from Eq. 2.28 with ϵ_p^{II} replaced by the dielectric permittivity of silicon ϵ_{Si}, and h_1 replaced by the depletion layer thickness h_{depl}. If the abrupt depletion approximation is assumed, the depletion layer directly adjoins the neutral part of the substrate, and at the interface plane $x_3 = -h_{depl}$ the effective permittivity of Eq. 2.40 can be used.

The potential distribution in the depletion layer is similar to that of the SiO_2 layer (Eq. 2.32). As a result of the additional dielectric layer, the potential at $x_3 = 0$ increases. However, as a result of the increasing distance between polarization charges and the mobile carriers, the wave–carrier interaction for $x_3 < -h_{depl}$ decreases.

(iv) Inversion

If the band bending is so large that the intrinsic Fermi potential ψ_i crosses the semiconductor Fermi potential ψ_F, the surface is inverted and minority carriers are pulled from the bulk to the surface. A thin inversion layer of holes with a thickness in the order of 10^{-3}–10^{-2} μm results.

The minority carriers in the inversion layer are not in thermal equilibrium. Because the supply of holes from the bulk is very slow compared to the SAW frequencies, the holes will not be able to respond to the normal component of the electric field. This corresponds to the high-frequency behavior of a MOS capacitance which does not return to the oxide capacitance when an inversion layer is created. In order to describe the field problem by using the small-signal theory, a method is adopted, which was proposed by Kino *et al.* [54]. The inversion layer is considered to be a very thin, semiconducting layer of thickness h_{inv}, which is located on top of the insulating depletion layer. It is assumed that this semiconducting layer has a uniform conductivity $\sigma_{inv} = p_{inv}\mu_{p,inv}q$. Since the inversion layer is thinner than the mean free path of the carriers, the mobility is strongly influenced by the surface. The surface mobility $\mu_{p,inv}$ depends on the static transverse field and is typically half the bulk mobility [79].

The hole current $J_{p,3}$ in the x_3-direction is zero, whereas $J_{p,1}$ is given by Eq. 2.33 with $p_0 q\mu_p$ replaced by σ_{inv}. When it is assumed that all RF variables vary as $\exp[j(kx_1 - \omega t)]$, and using the current continuity equation for holes (Eq. 2.11), a relation between the modulated hole density p_1 and the RF potential ϕ can be obtained

$$p_1 = \frac{\sigma_{inv}k^2}{j\omega q(\delta + j\omega/\omega_{Dp})}\phi \tag{2.42}$$

in which δ and ω_{Dp} represent the Doppler shift and diffusion frequency of the holes, respectively.

Because h_{inv} is very small, the modulated inversion layer charge can be considered as a surface charge $\rho_{s,inv} = p_1 q h_{inv}$, which is located at $x_3 = 0$. This charge causes a discontinuity of the normal displacement field D_3. When only the small-signal fields are considered, and the relation between ϵ_{eff} and D_3 is taken into account (Eq. 2.20), the effective permittivities just above and below the inversion layer can be related to the modulated hole density p_1 in the inversion layer

$$\epsilon_{eff,inv} = \epsilon_{eff,depl} + \frac{\sigma_{inv}kh_{inv}}{j\omega(\delta + j\omega/\omega_{Dp})} \tag{2.43}$$

where the effective permittivities are defined as

$$\epsilon_{eff,inv} = \lim_{x_3 \downarrow 0} \frac{D_3(x_3)}{k\phi(x_3)}; \qquad \epsilon_{eff,depl} = \lim_{x_3 \uparrow 0} \frac{D_3(x_3)}{k\phi(x_3)}$$

The product $\sigma_{inv}h_{inv}$ in the second term on the right of Eq. 2.43 is, in fact, the total equilibrium charge per unit area in the inversion layer. In the case of strong inversion ($|\psi_s| \gg |\phi_F - \phi_i|$) this charge Q_{inv} can be approximated by [49, p. 369]

$$Q_{inv} \approx \sqrt{2}qn_iL_D\exp(-q\psi_s/k_BT)$$

In the case of weak inversion, the second term on the right side of Eq. 2.43 can be ignored, and the situation is reduced to the depletion layer case *(iii)*. With decreasing ψ_s the inversion charge rises, and the $\epsilon_{eff,inv}$ ultimately goes to infinity. The inversion layer then acts as a perfectly conducting sheet at $x_3 = 0$, which screens the RF fields completely.

Because the discussed acoustoelectric phenomena depend greatly on the mobile carrier concentration at the silicon surface, they are all affected by the band bending. Since the perturbation of the wave velocity is directly related to the screening effect of the mobile carriers, it is maximal under accumulation and strong inversion conditions. By controlling the band bending with an external, transverse bias voltage, the phase velocity can be controlled electronically. A phase shifter built in this way in the ZnO-SiO_2-Si layered structure is described by Urabe *et al.* [80].

The conductivity which is required for maximal attenuation or amplification is given by [43]

$$\sigma_{Si} = (\epsilon_p^{ZnO} + \epsilon_{Si})|\delta|\omega \tag{2.44}$$

This condition can be achieved at the silicon surface under proper band bending conditions. The attenuation factor as a function of the surface potential ψ_s depends on the bulk conductivity of the semiconductor. An optimal wave-carrier interaction with majority carriers is obtained under conditions of weak depletion or accumulation, whereas a maximal interaction with minority carriers occurs at the onset of inversion. A detailed experimental and theoretical description is presented by Motamedi [78].

Because the generated acoustoelectric fields are related to the attenuation factor, conditions similar to that of the attenuation and amplification phenomena are required. However, in contrast to the attenuation factor which is a scalar, the acoustoelectric fields have a direction, which depends on the type of mobile carriers that dominate in the interaction process. When the surface goes from depletion into inversion, the type of carriers changes (from electrons to holes for n-type silicon) and, therefore, the sign of the longitudinal AE currents [81] and the TAV [82] changes. Pronounced maxima are observed at the ψ_s values corresponding to the

conditions of optimal interaction between the SAW and majority and minority carriers.

For parametric interactions, the nonlinearity of the depletion layer capacitance dominates, and a different approach is required. This nonlinearity is maximal when the slope of the high-frequency capacitance-to-voltage characteristic of the depletion layer capacitance is maximal. The parametric mechanism is optimized when the system is biased at the point just before inversion. This was shown experimentally for convolvers [83] and parametric amplifiers [75] in the ZnO-SiO_2-Si structure. A detailed description is given by Khuri-Yakub *et al.* [74].

The band bending can be induced by an externally applied DC bias field normal to the surface of the layered structure. However, the bending can also be caused by fixed charges and traps in the layered structure. Although the fixed charges and traps do not respond to the RF fields, they do affect the acoustoelectric interactions through their influence on the band bending. This will be discussed in more detail in section 2.6.

2.5.2 Active Semiconductor Devices

In the previous section, only inhomogeneities in the x_3-direction were assumed. However, when active devices are embedded in the semiconductor, implanted and diffused regions are present at the silicon surface. As a consequence, the substrate conditions change in all three dimensions. To keep the problem manageable, no variations in the x_2-direction are assumed. The problem is now a truly two-dimensional one, with boundary conditions both in the x_1 and x_3-directions.

The solution of the Poisson and current equations is not trivial in the nonuniform, two-dimensional domain with complicated boundaries. To find the solution, numerical methods must be employed. In the past, much attention was paid to these problems, mainly in order to accurately model the MOS transistor; see for instance Engl *et al.* [84] or Selberherr [85].

In general, the solution method involves three steps:

1. Partitioning: the two-dimensional domain is partitioned into a finite number of subdomains. Each subdomain contains a grid point in which the solution is approximated with the desired accuracy. Depending on the applied solution method, a rectangular or triangular mesh is used. In general, the mesh is nonuniform: locally, the density of grid points is increased in areas where a higher accuracy is required.

2. Discretization: the partial differential equations which characterize the problem are approximated by discrete equations. In this way, the variable in one grid point is related to the variables in its adjoining grid points. Most common are the finite-difference and finite-element methods.

3. Solving the equations: the partitioning and discretization yield a coupled system of aN discretized equations, with N the number of grid points and a the number of unknown variables. In general, the unknown variables can be found by employing matrix methods. However, taking into account that usually the number of grid points is considerable ($> 10^4$), these methods become unattractive, and relaxation methods must be employed [86]. In these iterative methods, the value of each grid point is subsequently updated using a term, which is weighted by the values of the adjacent grid points. The updating is repeated, until the desired accuracy is reached. Thus, the unknown variables relax to their equilibrium solution at $t \rightarrow \infty$. If the equations considered are nonlinear, iterative methods are indispensable.

The effect of the SAW can easily be included in the device modeling methods by making use of the Equivalent-Surface-Charge method developed in section 2.2.3. The equivalent surface charge is first determined for a layered system with a homogeneous, nonconducting substrate, as has been described in section 2.3.1. This charge is then inserted in the original system, which contains the semiconductor devices. Special attention must be paid to the boundary conditions at the ZnO-SiO_2 interface, where the equivalent surface charge causes a discontinuity of the electric field variables.

It should be remembered that the ESC method assumes static conditions. The interaction of the SAW electric fields with the currents flowing in the active semiconductor device can only then be determined accurately when the transit time of the carriers in the current path is much shorter than the wave period $1/\omega$.

2.6 CHARGES AND TRAPS

2.6.1 Classification

In practice, the ZnO-SiO_2-Si layered structure shown in Fig. 2.1 is not ideal. There are fixed charges in the oxide layers and trapped charges at the interface planes. The main causes are the defects which arise during

the fabrication of the layers, and the discontinuities at the boundary of two media of different materials. An overview is given of the different charges and traps in the layered structure shown in Fig. 2.1.

(i) Silicon substrate ($x_3 < 0$)

The silicon substrate is assumed to be neutral. No charge resides in this medium, provided there is no band bending.

(ii) SiO_2-Si interface ($x_3 = 0$)

At this interface, there is an interruption of the silicon lattice, which gives rise to fast surface or Tamm-Shockley states. Their distribution is characterized by a continuum of states in the silicon bandgap [49, pp. 380–390]. For the interface under consideration, the charge in the states is positive, which causes an accumulation in the case of a n-type substrate.

The charge density associated with the states Q_{ss} (C/m^2), depends on the silicon crystal orientation and the subsequent processing steps. For (100) silicon, Q_{ss} is about an order of magnitude smaller than for (111) silicon. The increase in the amount of surface states after the deposition of ZnO, which is reported by many researchers, can be attributed to the temperature step accompanying the ZnO deposition and radiation damage [87]. The occupation of a surface state depends on its position with respect to the silicon Fermi level. When the energy bands are bent by an external bias field, the Fermi level scans through the trap levels, thereby filling or emptying the states. As a result of the changing charge density in the states, which is caused by this process, the bending potential itself is affected by the states. The relaxation time of the surface traps for n-type silicon is given by [49, p. 386]

$$\tau_{ss} = \frac{1}{\sigma_n \bar{v}_{th} N_D} \exp\left[\frac{-q\psi_s}{k_B T}\right] \tag{2.45}$$

in which

τ_{ss}	surface-state time constant	(s)
σ_n	electron capture cross section	(m^2)
$\bar{v}_{th}$	average thermal velocity	(m/s)
N_D	donor concentration	(m^{-3})

and ψ_s is the potential at the silicon surface, as was defined in section 2.5.1. Since this response time is six orders of magnitude larger than the dielectric relaxation time $1/\omega_c$ of the majority carriers, the interaction

between the SAW and the surface states can be ignored. For the electric fields of the SAW, the surface-state charge is transparent. Only for very low frequencies ($\omega < 10\,\mathrm{MHz}$) can an influence of the surface states be expected [88].

(iii) SiO_2 layer ($0 < x_3 < h_1$)

A thin sheet of immobile, positive charge is situated in the SiO_2 layer within a distance of about 20 nm above the SiO_2-Si interface. The amount of charge depends on the oxidation and annealing processes, and on the silicon orientation. This charge also originates from the discontinuities at the SiO_2-Si interface. The charge density Q_f (C/m^3) is not affected by the SiO_2 thickness. Since the charge is fixed, it cannot respond to the SAW electric fields.

The oxide layer also contains mobile, ionic charge Q_m (C/m^3), which consists of Alkali ions such as Na^+, K^+ and Li^+. These ions can move back and forth through the oxide and are influenced by the temperature and the bias voltages. Their movement is too slow to respond to the RF fields, but they can give rise to instable DC bias conditions.

An additional fixed, positive charge Q_{ot} (C/m^3) is present throughout the SiO_2 layer and consists of trapped holes. The traps are associated with defects in the oxide layer. Although they are generally neutral, they can be charged by radiation or hot-electron injection. Pierret *et al.* [89] reported a strong increase of Q_{ot} after the ZnO deposition. This effect is attributed to the radiation damage, caused by the ZnO sputter process. Since Q_{ot} is caused by traps in the entire layer, the influence of this charge is reduced when the SiO_2 thickness decreases.

(iv) ZnO-SiO_2 interface ($x_3 = h_1$)

At this interface, deep-level surface traps which can be negatively charged are present [89, 90]. The relaxation time of these slow traps is considerable: up to one day has been reported [83]. The traps can be filled by the injection of electrons from a metal electrode on top of the layered structure. The electrode on top of the ZnO constitutes a low-impedance contact. When the electrode is negatively biased, an electron current flows through the semiconducting ZnO, until all traps are filled. Although these negatively charged traps can compensate the positive charges in the SiO_2-Si system, their presence is usually undesirable, because they cause instabilities in the DC operation. With dedicated anneal steps, the instability problems can be suppressed [91].

(v) ZnO layer ($h_1 < x_3 < h_1 + h_2$)

Pierret *et al.* [89] also reported the presence of a space charge in the ZnO layer, which is caused by bulk traps. The distribution of this positive bulk charge is not well known. According to Pierret *et al.* [89], this bulk charge is confined to the near vicinity of the ZnO-SiO_2 layer. However, experiments described by Sakai *et al.* [90], indicate a definite influence of the ZnO thickness.

2.6.2 Influence on the Acoustoelectric Phenomena

Because all the charges which were presented in the previous section are fixed, or have time constants which are much larger than the wave period $1/\omega$, there is no direct interaction between these charges and the electric fields of the SAW. However, the acoustoelectric interactions are indirectly affected, because they induce a DC band bending.

The fixed charges merely cause a shift in the bending characteristics, which were discussed in section 2.5.1. For the SiO_2-Si surface states it should be taken into account that the occupation of the trap levels and the band bending are strongly coupled. This results in a broadening of the convolution peak vs. the applied bias voltage [74], but also offers the possibility of measuring the relaxation times of the traps. When the bias field is changed abruptly, the occupation of the surface traps is adjusted, and a new equilibrium situation is reached. This situation is not reached instantaneously, but within a time duration that is characteristic of the considered surface traps. The rearrangement of the surface state occupation is accompanied by a proper change of the energy bands. The change in the band bending, in its turn, is reflected in the strength of the AE fields (or TAV) and the attenuation factor. By measuring the transient responses of the acoustoelectric interactions, information about the relaxation time of the traps is obtained [72].

The slow surface states at the ZnO-SiO_2 interface cause instabilities in the DC bias operation of the layered structure when a top electrode which is in direct contact with the ZnO layer is applied. When this electrode is negatively biased, electrons are injected and fill the traps at the ZnO-SiO_2 interface. After a change in the bias voltage, the new equilibrium situation is reached within a time duration determined by the relaxation time of the traps. This causes an hysteresis in the convolver characteristics [83].

2.6.3 Acoustoconductivity

Trapping phenomena also give rise to a change in the DC conductivity of silicon [92]. During each cycle of the wave, the majority carriers are alternately pushed away from and attracted to the silicon surface by the transverse fields of the SAW. At high power levels, this charge modulation is nonlinear and there is a net increase of charge carrier density at the surface. Under these conditions, majority carriers accumulate at the silicon surface, the density of which can deviate considerably from the equilibrium density. This phenomena can be considered as a transverse acoustoelectric field effect [93], which has a sign opposite to that of the AE field discussed in section 2.4.2.

Because of the accumulation at the silicon surface, the capture rate of the surface traps rises strongly (see Eq. 2.45), and the conductivity of the surface layer decreases. This is observed as a change in the DC conductivity of this layer, and is indicated as the *acoustoconductive* effect. Under pulsed operation, the conductivity change returns to its initial value within a time duration determined by the relaxation time of the traps.

2.7 DEFORMATION POTENTIAL COUPLING

2.7.1 Physical Mechanism

In this section, a coupling mechanism between acoustic waves and mobile charge carriers that is present in any conductive solid, not necessarily piezoelectric, is discussed. The electronic energy bands in a solid result from the periodic lattice structure of the crystal. When the lattice is spatially deformed, for instance by a mechanical wave motion, the energy bands are spatially perturbed. As a consequence, the charge carriers are redistributed, occupying the lowest available energy levels.

The effect of an elastic strain on the potential energy of the carriers is expressed by the deformation potential tensor. The shift dW in the energy is given by [94]

$$dW = \Xi_{kl} S_{kl}$$

in which Ξ_{kl} is the second-rank deformation potential tensor (J).

As a result of the redistribution of the mobile carriers, a nonuniform space charge is created. However, the deformation potential coupling is a very weak phenomenon, and the charge bunching is strongly opposed by electrostatic repulsion. Weinreich [95] pointed out that the repulsive forces are absent when the medium contains an equal number of electrons and holes, as in an intrinsic semiconductor. In this case, both the

holes and electrons can be bunched without affecting the charge neutrality. Electrostatic repulsion is also avoided in multivalley semiconductors like germanium or silicon. For silicon, it is found that the conduction band consists of six distinct regions which are located along the [001] axes in the k-space, see Fig. 2.6. The constant energy surfaces of these regions

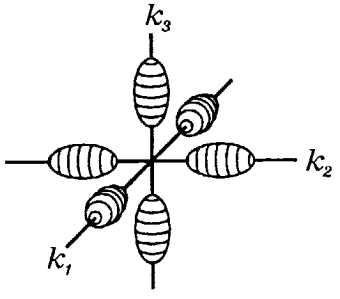


Figure 2.6: *Multivalley energy surfaces for n-type silicon.*

are ellipsoidal in shape [96]. When a strain is applied along one of the axes, the energy valleys rise and fall. However, the change in the valleys located on the strained axis is opposite to the change experienced on the other axes. Because the electrons are forced to occupy the lowest energy levels, an exchange of electrons between the valleys on the different axes takes place. In this rearrangement in the k-space no space charge is induced: the increase of the electron density in one valley is compensated by a decrease of the density in another valley.

In p-type materials similar processes take place, but the theory is much more difficult because of the complexity of the valence band. In the k-space, three energy surfaces, centered around k=0, are found. Since the curvatures of the three surfaces differ, the corresponding effective masses of the holes differ, i.e. heavy and light holes must be distinguished.

2.7.2 Acoustoelectric Phenomena

Similar to the piezoelectric potential, the deformation potential introduces a coupling between the acoustic waves and the mobile charge carriers. As a consequence, the same kind of acoustoelectric phenomena as described in section 2.4.2, are observed. In fact, many wave–carrier interaction phenomena were first described in nonpiezoelectric solids. The acoustoelectric field in n-germanium, which is induced by the deformation potential coupling, was described by Parmenter [97], and later experimentally verified

by Weinreich [95]. Experimental and theoretical results on the attenuation and amplification mechanisms can be found in References [98], and [46, 99], respectively.

However, even in the absence of space-charge formation the observed phenomena are very weak. The deformation potential coupling is much weaker than the piezoelectric coupling. In the frequency range 100–500 MHz, the deformation potential phenomena are 5 to 6 orders of magnitude smaller than the piezoelectric phenomena. In contrast to the piezoelectric coupling, the deformation potential coupling is proportional to ω^2 [46], so that this mechanism will dominate in the very high frequency range, but only for frequencies higher than 100 GHz.

In the considered layered structure, the phenomena caused by the deformation potential coupling can practically all be ignored. However, two effects are of importance, and are discussed in the next sections: velocity perturbation and piezoresistance.

2.7.3 Velocity Perturbation

An important phenomenon caused by the deformation potential coupling is the electronic effect on the elastic tensor c_{ijkl}. Keyes pointed out that when the carriers are redistributed among the different valleys, a change in the total electronic energy content of the crystal results [94]. As a consequence, the total elastic energy changes, which shows up as a change in the elastic tensor c_{ijkl} and thus in the SAW velocity.

The electronic effect on the wave propagation is anisotropic. In the cubic system of silicon, the elastic tensor elements that are affected are the three independent constants c_{11}, c_{12} and c_{44}. The change in these constants depends on the type of free carriers (electrons or holes), the doping level and the deformation potential tensor. The theoretical calculations for n-type semiconductors are well established. However, for p-type material, they are severely hindered by the warped nature of the valence bands. It can be shown that the changes in c_{11} and c_{12} are coupled for both n-type and p-type silicon [98]

$$dc_{12} = -\frac{dc_{11}}{2}$$

The relative changes in c_{11}, c_{12} and c_{44} for n-type and p-type silicon are depicted in Fig. 2.7 and 2.8, which were obtained from experimental data presented in References [100, 101, 102]. The data for the deviations in c_{11} and c_{12}, which were obtained from [101], were measured at 78 K. However, above 50 K the c_{ij} values vary little with temperature [98].

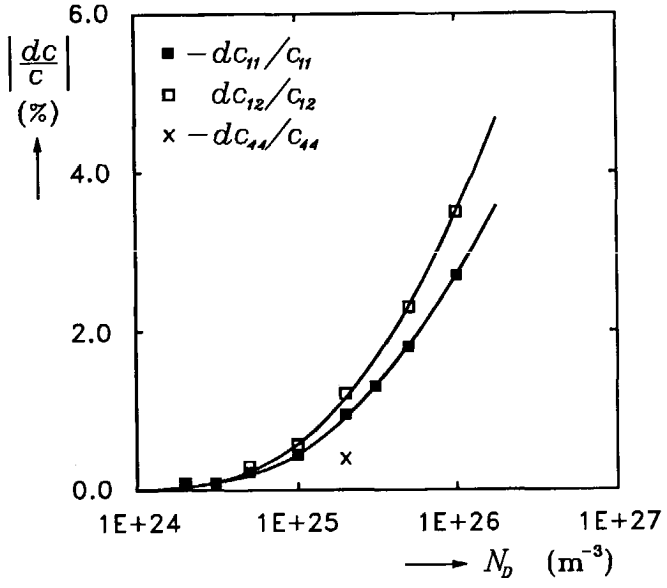


Figure 2.7: *Relative changes in the elastic constants vs. the donor concentration in n-type silicon.*

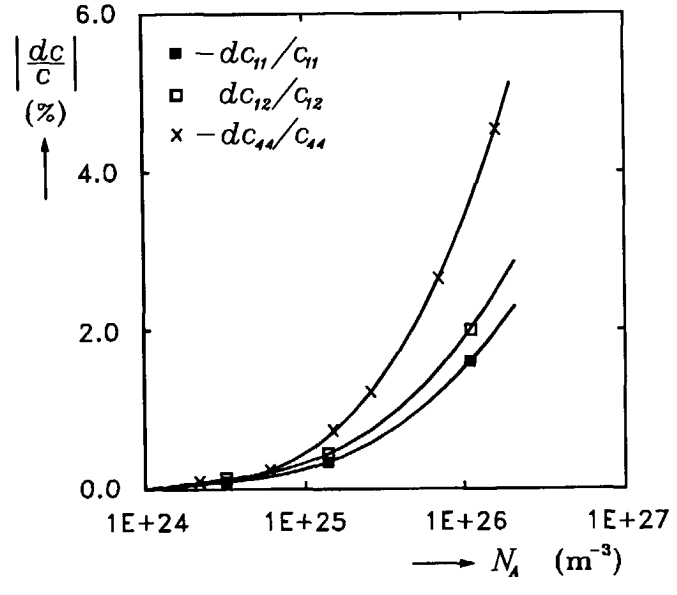


Figure 2.8: *Relative changes in the elastic constants vs. the acceptor concentration in p-type silicon.*

Anyhow, the variations in c_{ij} caused by the doping effect decrease when the temperature increases, and Fig. 2.8 can, therefore, be considered as a worst case. The dependence of the elastic constants on the doping concentration is important with respect to wave reflections. Because of this phenomenon, diffused or implanted regions at the silicon surface will produce deviations in the wave velocity, which gives rise to reflections. This effect is further described in section 3.4.

2.7.4 Piezoresistive Effect

In Fig. 2.6, the ellipsoidal shape of the constant energy surfaces is shown. Because the effective electron mass is determined by the curvature of the energy surface, this shape results in different effective electron masses for directions along and perpendicular to the axes. Since the electron mobility is inversely proportional to the effective mass, this also results in different values of the mobility along and perpendicular to the [001] axes. When the material is strained, an exchange of carriers takes place between the valleys. As a result, the average mobility changes, which is reflected in a variation of the resistivity [103].

With respect to acoustic wave motion, the piezoresistive effect can be considered as a kind of acoustoconductive effect. However, in contrast to the DC phenomenon described in section 2.6.3, the piezoresistive effect is an AC modulation effect which operates locally: during each wave period the material is contracted and expanded, which causes opposite resistivity changes. Therefore, the piezoresistive effect can be used in active, programmable SAW detectors as is described in section 3.2.

The piezoresistive effect is anisotropic, and is described by a fourth-rank tensor π. This tensor relates the relative resistivity change to the stress. In the cubic system of silicon, the piezoresistance is completely described by three constants π_{11}, π_{21} and π_{44}, the values of which can be found in Reference [103].

2.8 CONCLUSIONS

In this chapter, the acoustoelectric system, which involves a SAW propagating in a three-layered ZnO-SiO_2-Si configuration, was described. The solution of the acoustoelectric field problem was considered, and an overview was given of the acoustoelectric phenomena encountered. The acoustoelectric field problem can be reduced to an electric field problem by representing the mechanically induced polarization charges in the piezoelectric ZnO layer by an equivalent surface charge, which is located at the

ZnO-SiO_2 surface. By employing this Equivalent-Surface-Charge method, no restrictions are placed on the silicon substrate. The solution is restricted to the region below the ZnO-SiO_2 interface. This is sufficient for the active SAW detectors described in Chapters 4 and 5, which are completely embedded in the silicon substrate.

The penetration depth of the electric fields into the silicon is in the order of the Debye length, which is very small for the doped semiconducting substrates commonly used in the IC fabrication. Only a depletion of the silicon surface allows the electric fields to penetrate deeper into the semiconductor. Although many acoustoelectric phenomena originate from the interaction between the SAW and the mobile charge carriers in the semiconductor, they generally require high-resistivity semiconductors and are not attractive for use in SAW detectors. Effects that do have potential detector applications are the parametric effect and the piezoresistive effect.

Fixed charges and traps in the layered structure do not influence the RF fields of the SAW because of their low relaxation times. However, they should be taken into account in the SAW detector design since they may influence the DC operation of the detector.

Chapter 3

CONTROLLABLE SAW DETECTION

3.1 INTRODUCTION

In the previous chapter, several aspects of the interaction between the acoustical and electrical properties of the ZnO-SiO_2-Si layered structure were highlighted. In this chapter, the design of electronically controllable SAW detectors in the structure is investigated. These detectors are the key elements of the programmable filter.

In general, SAW detectors consist of conductive electrodes located in the acoustoelectric system. In the considered layered structure, the electrodes can be placed at three different levels, see Fig. 3.1. In the following, it is assumed that the operation frequencies are much smaller than the relaxation frequency ($\omega \ll \omega_c$). In this case, the silicon substrate can be considered perfectly conducting, and can act as one terminal of a detector. In configurations A and B, the electrodes consist of metal structures, usually aluminum or gold. Because the electrodes in configuration C are located in the semiconductor, diffused or ion-implanted structures can be used, thereby avoiding metal electrodes in the SAW propagation path. An electrical separation between these diffused electrodes and the conductive semiconductor is obtained by using *pn*-junction structures. Because the junction electrodes are entirely embedded in the silicon substrate, they hardly perturb the SAW propagation, and are preferably used to achieve

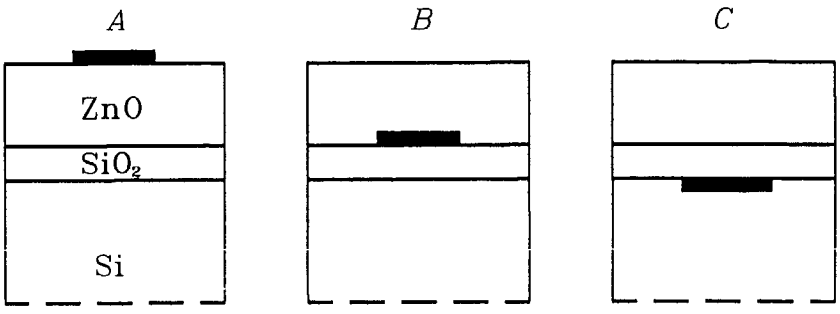


Figure 3.1: *Detector position levels.*

an undisturbed detection of SAWs.

In the controllable SAW detector, two functions must be realized: 1. conversion of the acoustic signal into an electric signal, and 2. electronically controlling the output signal of the detector. This chapter starts with a description of the various detection mechanisms available. In section 3.3. the control function is considered. Finally, the use of junction electrodes is discussed in section 3.4.

3.2 SAW DETECTION MECHANISMS

In the programmable SAW detector, a linear conversion must be realized in order to obtain an electric output signal which accurately represents the information signal embedded in the acoustic wave. This requires a proper acoustoelectric conversion process. Three detection mechanisms can be distinguished: the *passive*, *active* and *parametric* detection mechanisms. The passive detection mechanism is a direct capacitive coupling between the electric fields induced by the SAW, and the conductive electrodes located nearby the piezoelectric medium. The strength of the output signal of the passive detector is solely determined by the SAW input power P_a^i, and by the conversion efficiency. In the active detector, the output signal results from an electric power source, which is modulated by the SAW electric fields. The output strength is not only determined by the acoustic power of the incoming wave, but also by the power of the auxiliary, electric power source P_e^{aux}. The functional diagrams of the passive and active detection mechanisms are illustrated in Fig. 3.2. The parametric detector can be considered as an active detector, in which the auxiliary source is not electric but acoustic. This auxiliary, or pump, power is present as an acoustic, continuous-wave (CW) signal in the SAW propagation path. Because of nonlinearities in the parametric detector, an output term results,

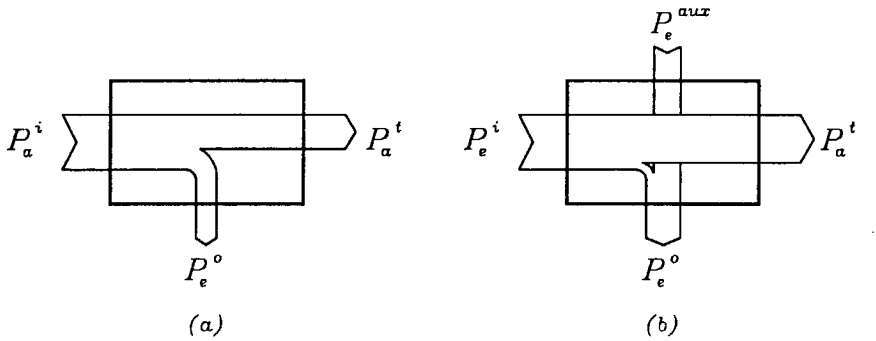


Figure 3.2: *The passive (a) and active (b) detection mechanisms.* P_a^i *and* P_a^t *are the acoustic power levels of the incoming and passing SAW.* P_e^o *is the electric output power and* P_e^{aux} *represents the auxiliary, electric power.*

which is the product of the CW and main acoustic signal.

In the following sections, the three detection mechanisms are further evaluated. In the ZnO-SiO_2-Si structure under consideration, the piezoelectric coupling is the dominant driving force for these mechanisms. For the frequency range considered in this work, the deformation potential coupling in silicon is very weak. However, it can be applied in an active detector, as is described in section 3.2.2.

In practice, the summing circuit of a programmable tapped delay line (see Fig. 1.3) consists of a simple bus-bar, onto which all programmable taps are connected in parallel. This configuration involves the current summation of the tap outputs. Therefore, the programmable detector elements are most conveniently represented by a current source i_d (A) in parallel with an output admittance Y_d (S), see the equivalent circuit in Fig. 3.3. The small-signal current i_d represents the short-circuited detector current. In this chapter, all programmable taps are represented by this circuit.

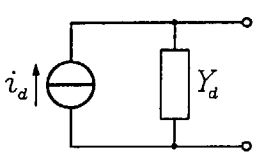


Figure 3.3: *General small-signal circuit of a programmable SAW detector.*

3.2.1 Passive Detection

When two, or more, conductive electrodes are placed in the ZnO-SiO_2-Si layered system, the piezoelectric polarization in the ZnO layer induces a voltage across the electrodes. There is a capacitive coupling between the acoustically induced electric fields and the free charges on the electrodes. This coupling mechanism is reversible: a voltage across the electrodes induces electric fields, which will excite acoustic waves. The relation between the reception and the launching of waves is described by the reciprocity relation [104]. The reception and launching processes can be characterized by an acoustic radiation conductance $G_a(\omega)$ (S) and a radiation susceptance $B_a(\omega)$ (S) in parallel, similar to those encountered in antenna systems [105]. For SAW transducers, $B_a(\omega)$ can usually be ignored, since the static capacitance C_T (F) dominates. The radiation conductance G_a and the detector current amplitude i_{d0} of Fig. 3.3 are related by

$$i_{d0}^2 = 4G_a P_a W \tag{3.1}$$

where P_a is the power per unit width of the incident acoustic wave, and W is the effective detector aperture (m).

The simplest implementation of a passive SAW detector is a single electrode. In this case, the electrode is one side of the detector, whereas the other side is created by a conductive plane at one of the interfaces in the ZnO-SiO_2-Si structure, or by the conductive silicon substrate. The radiation conductance of this single-electrode detector is determined by the location of the electrode in the layered structure, the normalized layer thicknesses and layer permittivities, and the piezoelectric coupling strength. The acoustic bandwidth is determined by the electrode length, and is very wide for a single-electrode detector (note that in this thesis, the electrode length is measured in the SAW propagation direction, whereas the width is measured normal to this direction).

A more efficient SAW detector is obtained when both the positive and negative electrodes are placed in the same plane, which results in the Interdigital Transducer, see section 1.2.1. The IDT in three-layered media was extensively investigated by Venema [106] and Ghijsen [107]. The acoustic bandwidth of the IDT is determined by the number of periodic ID sections (see section 6.3).

The electrodes of the passive detector can be placed at several locations within the ZnO-SiO_2-Si structure, see Fig. 3.1. The various configurations are described separately below.

(i) Electrodes on top of the ZnO layer

In configuration A of Fig. 3.1, metal electrode structures are placed on top of the ZnO layer. The piezoelectric coupling has a maximum for a small ZnO thickness ($\omega h_{ZnO} \approx 1000\,\mathrm{rad\,m/s}$), but reaches only moderate strengths. Therefore, the efficiency of this detector is rather low. In addition, the thin ZnO layers give a high velocity dispersion, as will be explained in Chapter 6.

The deposition and etching of the metal layers on top of the ZnO layer are not very attractive from a technological point of view. In addition, the interconnection between the detector and external electronics may be hindered by the step discontinuity, which is introduced by the ZnO layer.

(ii) Electrodes at the ZnO-SiO_2 interface

By using the electrode positioning in configuration B, a much higher piezoelectric coupling can be achieved, provided the dielectric layer beneath the electrodes is sufficiently thick to prevent the conductive substrate to short-circuit the electric fields at the ZnO-SiO_2 interface. This dielectric layer can be the SiO_2 layer, or a depletion layer at the silicon surface. The coupling $\Delta v/v$ as a function of the normalized dielectric layer thickness for a ZnO thickness of $\omega h_{ZnO} = 8000\,\mathrm{rad\,m/s}$ is presented in Fig. 3.4. The radiation conductance and static capacitance of IDTs in this configuration have been described by Venema *et al.* [108].

Technologically, configuration B is quite attractive. After finishing the processing of the electronic (and piezotronic) circuitry, the ZnO layer is deposited as the final process step. In this way, the ZnO, which is a very reactive material, cannot contaminate the process equipment. The IC compatibility is further enhanced by the planarization of the metal layers: the interconnection between the metal electrodes of the detector and the electronics outside the propagation path can readily be accomplished.

(iii) Electrodes at the silicon surface

The same advantages also apply to configuration C in Fig. 3.1, in which the detecting electrodes are placed underneath the SiO_2 layer. In this case, the electrode does not consist of a metal stripe, but of a diffused or ion-implanted region. A separation between the conductive electrode and the conductive silicon is obtained by using *pn* structures which are reversely biased. The created depletion region produces a nonconductive dielectric medium around the detecting electrode.

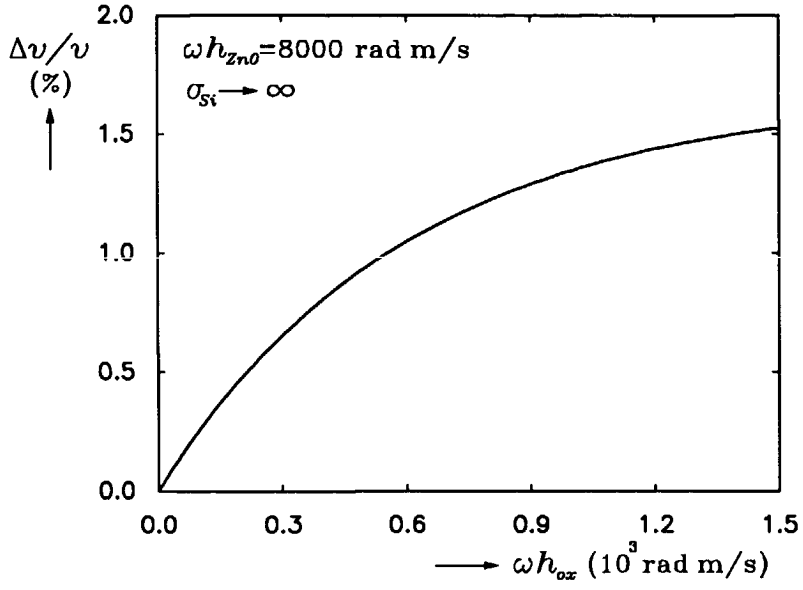


Figure 3.4: *Coupling strength $\Delta v/v$ at ZnO-SiO_2 interface vs. ωh_{ox} with $\sigma_{Si} \rightarrow \infty$.*

The output capacitance of the junction detector is mainly determined by the depletion layer capacitance of the reverse-biased *pn* junction. It is determined by the doping levels and the bias voltages. In contrast to the metal electrodes, the junction electrodes have a finite series resistance which cannot be ignored. Therefore, a resistive part must be included in the output admittance Y_d. This resistive part has a deteriorating influence on the efficiency and noise behavior of the detector.

In the past, passive junction transducers were investigated as replacements for the conventional metal IDTs. In References [109] and [110], junction structures are described, in which the silicon substrate acts as one side of the transducer. Interdigital junction structures are described in Reference [111], and experimental results can be found in Reference [112]. However, the high electrode series resistances and the large electrode capacitances give rather low efficiencies in these passive devices.

3.2.2 Active Detection

In the active detector, the origin of the detector current is not the acoustic wave power itself, but a modulation process, induced by the SAW, of an auxiliary power flow. In the devices considered in this work, this

auxiliary source is a DC bias current. Because of the penetration of the SAW fields into the silicon, there is a direct interaction between the SAW and the mobile charge carriers in the bias current. Since the output signal of the detector is proportional to the power supplied by the auxiliary (current) source, higher efficiencies can be obtained than with passive detectors. An internal gain effect is present, which is comparable to that encountered in conventional transistors. However, unlike passive detectors, there is a DC power dissipation in the active detection mechanism, which should be taken into account when considering the merits of the active detector. Since the detection process in the active detector is a modulation effect, the acoustoelectric conversion process is irreversible. Therefore, the admittance Y_d in the equivalent circuit of Fig. 3.3 does not contain a radiative part.

Since the acoustoelectric coupling is maximal at the SiO_2-Si interface, the devices which can be applied for active SAW detection have FET-like features with current channels, which are located close to this interface. Since for active detectors, the C configuration of Fig. 3.1 is applied, they can be implemented by merely using junction electrodes. The flow of the mobile carriers can be perturbed in two ways: 1. by using the electric fields induced in the ZnO layer, 2. by using the change in mobility, which is caused by the lattice deformations. These effects correspond to a piezoelectric and piezoresistive coupling, respectively. In the following subsections, some examples of active SAW detectors using the piezoelectric and piezoresistive effects are examined.

(i) Active, piezoelectric SAW detectors

Active detectors which are sensitive to the electric fields of the SAW can be made with Field-Effect Transistor structures located at the silicon surface. The first Piezoelectric FET (PI-FET) applied for SAW detection was described by Greeneich and Muller [113, 114]. They used a MISFET configuration, in which the insulator between the gate and the channel is created by a thin layer of piezoelectric ZnO. The efficiency and frequency response can be improved by the use of double-diffused MOS transistors [115], in which the effective gate length is strongly reduced. Conversion efficiencies of −50 dB at 28 MHz under power matched conditions were reported. In the PI-FET, the metal gate is located on top of the ZnO layer, and the FET is biased through this layer. Therefore, only thin ZnO layers can be applied. The sputtering of the ZnO layer deteriorates the channel region. Together with the channel biasing through the ZnO layer, this gives rise to instabilities (see section 2.6), and causes drifting bias

conditions.

A better configuration results if the gate is placed at the silicon surface. In this case a *pn*-junction gate can be applied, which results in a piezoelectric Junction FET (PI-JFET). The SAW electric fields do not directly interact with the mobile charge carriers, but modulate the potential of the junction gate, which gives a modulation of the drain bias current. Because the channel is located beneath the gate, a buried channel results, which is insensitive to the ZnO deposition process. Thick ZnO layers for an optimal piezoelectric coupling can be used. The piezoelectric JFET can be fabricated using standard IC fabrication techniques, and is technologically much more attractive than the PI-FET. A detailed investigation of the JFET as a programmable SAW detector is presented in Chapter 5.

Quite a different active SAW detector, which is presented in this thesis, can be made with a lateral reach-through device. Its structure resembles a FET, however, it has no gate. An injection current of minority carriers, the magnitude of which depends on the potential barrier in the channel, flows from the source to the drain. Because this potential barrier is perturbed by the SAW electric fields, a modulation of the current results. This device, the operation of which resembles that of a bipolar junction transistor (BJT) more than that of a FET, has been given the name Barrier-Modulated Tap (BMT), and is described in Chapter 4. Complete monolithic filters using an array of active, piezoelectric detectors have not been reported yet.

(ii) Active, piezoresistive SAW detectors

The mobility variation in silicon caused by the acoustic deformation (see section 2.7.4) can efficiently be detected with a MOSFET, since the drift current is linearly proportional to the carrier mobility μ. The first experiments of SAW detection using piezoresistive FETs were reported by Clairborne *et al.* [116]. Programmable matched filters using piezoresistive MOSFET were extensively studied by Hickernell *et al.* [117, 118, 119].

The piezoresistivity is an anisotropic phenomenon, and depends on the type of charge carriers. The highest gauge factor is obtained with *n*-channel FETs on (110) silicon using a [110] SAW propagation direction [120]. Conversion efficiencies at 100 MHz up to −35 dB were reported under optimal power matched conditions [119]. However, since the efficiency is proportional to the bias current squared, rather high bias currents per unit width (about 30 A/m) are required to obtain this efficiency. The corresponding power dissipation per tap of 100 mW and more is not very attractive for programmable filters with a large number of taps.

The advantage of the piezoresistive detection technique is the absence of a piezoelectric layer above the detectors. The active taps are not affected by thin-film sputter processes, and typical SAW properties related to the use of thin films such as propagation loss and dispersion, can be ignored. Although the piezoresistive MOSFET can be fabricated using standard fabrication techniques, attention must be paid to topological discontinuities in the device, which give rise to SAW reflections [118, 119].

3.2.3 Parametric Detection

In the previous discussion, linear detection mechanisms were considered. A detection mechanism which uses nonlinear processes is the parametric detection mechanism. In the parametric detector, two SAW signals are involved. One signal is the information carrier $S_i(\omega_1, k_1)$, whereas the other signal $S_p(\omega_2, k_2)$ is merely a CW tone, and can be considered as the pump signal of the parametric operation. This pump signal can have the same [121] or the opposite propagation direction [122] as the main signal. In the parametric detector, both SAW signals are converted into electric signals, and they are mixed as a result of the detector's nonlinear characteristics. As a consequence, product terms at $(\omega_1 \pm \omega_2, k_1 \mp k_2)$ are produced. The output signal can be detected at the sum or difference frequencies. Since the output strength is proportional to the power of the pump SAW, the parametric detector can be considered as an active detector in which the auxiliary supply signal is not electric but acoustic.

The conversion efficiency of a parametric tap is determined by the acoustoelectric conversion processes and the strength of the nonlinearity. The efficiency is characterized by a bilinearity factor F_p:

$$F_p = \frac{P_e^o}{P_a^i \, P_a^p} \tag{3.2}$$

in which P_e^o is the electric output power, and P_a^i, P_a^p represent the acoustic power of the SAWs carrying the main and pump signals, respectively. The configuration of a programmable, parametric tapped delay line strongly resembles a tapped convolver [123]. However, in the parametric tapped delay line, the reference signal does not contain information, but is a single CW tone supplied by a local oscillator. Therefore, the signal processing is completely asynchronous. Since the carrier frequencies of the input, pump and output signals are all different, the spurious level caused by reflections and electromagnetic feedthrough can be kept low by filtering.

The mixing process can be caused by the nonlinear interaction between the SAW and mobile charge carriers (see section 2.4.2), or by the

nonlinear characteristics of the detector element itself. In the latter case, the nonlinearities in the *CV*- or *IV*-characteristics can be employed. In the ZnO-SiO_2-Si layered structure, parametric taps can be made using an (metal) electrode structure on top of the ZnO [124], or at the ZnO-SiO_2 interface, in which case the nonlinear *CV*-characteristic of the created MOS capacitance to the substrate is employed. Reverse-biased junction electrodes at the silicon surface can also be applied for this purpose [125]. Parametric taps, in which the nonlinearity in the *IV*-characteristic is used, can be made with forward-biased diodes and transistors. Hybrid configuration are described in References [121, 122]. Although monolithic configurations, containing floating-gate MESFETs, have been built on GaAs [126], no monolithic implementations with active, parametric devices in the ZnO-SiO_2-Si system are known.

Because the operating frequencies differ at each port of the parametric filter, problems in the three-layered structure arise with respect to optimal ZnO thicknesses. In addition, because the tap periodicity is determined by both the wavenumber of the main signal and of the pump signal, the parametric PTDL is more sensitive to layer thickness variations than the direct PTDL. In this thesis, only the direct PTDL is considered.

3.2.4 Detector Efficiency

The dynamic range of a filter is, on the one hand, determined by the insertion loss from input to output, and, on the other hand, by the noise and spurious signals in the system. A high dynamic range requires a high conversion efficiency in the taps.

For the detector efficiency, usually the power conversion efficiency CE_p is used, which is defined as the ratio between the electric power P_l (W) delivered to the load and the total acoustic input power $P_a \cdot W$. Considering the circuit depicted in Fig. 3.3, the CE_p becomes

$$CE_p = 10 \log \frac{P_l}{P_a \cdot W} = 10 \log \left(\frac{G_l}{2|Y_d + Y_l|^2} \frac{i_{d0}^2}{P_a \cdot W} \right) \tag{3.3}$$

in which Y_l is the load admittance, and G_l its real part. It is clear that the conversion efficiency is strongly influenced by the load admittance Y_l: an optimal power conversion efficiency is obtained when the load admittance is the complex conjugate of the detector admittance, $Y_l = Y_d^*$. The load is said to be electrically matched to the detector. The power, dissipated in the load, then corresponds to the available power. However, the consequences of this matching for a passive or active detector are quite different.

In the passive detector, the available power is fixed by the acoustic power P_a of the incident wave. Under power matched conditions, CE_p reaches a maximum of –3 dB: half the incident power is delivered to the load, whereas the other half is reradiated as an acoustic wave. This latter process is called regeneration, and results from the reversible conversion mechanism in the passive detector. Since the regenerated wave is radiated in two directions, part of the waves travel back to the launching transducer, and can, therefore, be considered as reflected waves. These reflected waves give rise to multiple transit echoes between the taps, and can severely distort the filter function of the PTDL [127]. In the equivalent circuit, the regeneration is represented by a radiative part G_a of Y_d. It was found theoretically [128, pp. 80–81] and verified experimentally [129] that the regeneration strength is inversely proportional to $|Y_l + Y_d|$. Regeneration can be avoided by preventing a voltage build-up across the detector terminals, which is accomplished by short-circuiting the output ($G_l \to \infty$).

Apart from the regeneration, mismatching is also desired in the passive detectors for another reason. Since the output power of the passive detector is completely determined by the SAW power, high power efficiency consequently results in a considerable power extraction from the wave. Each time the SAW passes a tap, it loses energy, and the SAW amplitude is attenuated. As a result, an amplitude droop in the impulse response is observed. Mismatching is required to prevent this phenomenon.

For the active tap, the situation is quite different. In this tap, only a modulation process takes place, and a high output power can be achieved by extracting only a little power from the wave. Because of the internal gain mechanism, power conversion efficiencies larger than 0 dB can be achieved. In addition, the active detection mechanism is irreversible, and the regeneration effect is not present. In the equivalent circuit, this is expressed by the absence of a radiative component in the output admittance Y_d of the active detector. As a result, the restrictions on the load admittance as described for the passive detector are not encountered here. High power efficiency can be achieved without the deteriorating effects of regeneration and SAW attenuation. For the active detector, more freedom in the loading conditions is obtained.

A final matter of concern is the bandwidth-limiting effect, which is caused by matching, and is present in both the passive and active detector. The acoustic bandwidth $\Delta\omega_a$ of a detector is inversely proportional to its length L, measured in the SAW propagation direction: $\Delta\omega_a \sim v_g/L$ (v_g is the group velocity in the layered structure, and is further described in

Chapter 6). The detector dimensions are kept small (in the order or less than one wavelength), and the acoustic bandwidth is usually very large. The total bandwidth of the detector is then determined by the electric bandwidth of the loading circuitry. The matched detector represents a parallel resonating circuit with a quality factor Q_e given by

$$Q_e = \frac{\omega C_d}{G_l + G_d} \tag{3.4}$$

in which C_d and G_d are the detector capacitance and conductance, and G_l is the load conductance. Since the electric bandwidth is inversely proportional to this Q_e, a high G_l is required to prevent a bandwidth-limiting effect imposed by the load circuit.

In conclusion, it appears that one should pursue an optimal signal transfer rather than an optimal power transfer. With respect to the passive detector, this requires a short-circuiting of the detector output, which can be obtained with a current-sensing load circuitry. For the active detector, a larger amount of freedom is achieved because of the irreversible detection process. In conventional SAW applications, it is common practice to apply impedance matching to 50 Ω in order to minimize power losses. Inside the monolithically integrated filter, there is no need for a 50 Ω standardization. Impedance transformation circuits can be integrated on chip in order to match the filter to the system outside. For current-sensed detectors, the CE_p definition is not adequate. In this case, a better figure of merit is the current conversion efficiency CE_i defined as

$$CE_i = 10 \log \frac{i_{d0}^2}{2P_a \cdot W} \tag{3.5}$$

which gives a direct relationship between the detector short-circuit current and the acoustic power incident on the detector.

3.3 TAP WEIGHTING

SAW devices are typically bandpass filters operating at IF. As a consequence, the tap weight factors can be complex and both the amplitude and the phase can be varied. For a proper control of the filter function, the amplitude and the phase weighting of the programmable tap must be strictly separated in order to vary them independently.

3.3.1 Amplitude Control

Considering the SAW detector representation shown in Fig 3.3, it can be derived that the magnitude of the output signal can be controlled in two different ways:

1. by using an external weight circuit, following the detector.

2. by direct adjustment of the detector current i_d or the output admittance Y_d.

In the first option, the detection function and the control function are completely separated, which results in a *Separated-Control Tap.* In the second option, the control function takes place internally in the detector itself. Because the detection and control functions are then integrated into a single element, it is called the *Integrated-Control Tap.*

(i) Separated-control tap

In the Separated-Control tap, the control function takes place in a control circuit, which is located outside the SAW propagation path. This type of tap is typically encountered in hybrid filter configurations, where the acoustical and the electronic parts are located on separate media. Advantages of this structure are the ability to use conventional (passive) SAW detectors to which additional electronic control circuitry is added, and the ability to optimize both the detection and control parts separately.

In the past, several electronic circuits were considered for use in the weight circuitry. For a simple on-off control of the taps, diode switches are sufficient [130]. A more extended amplitude control can be accomplished with capacitance ladder networks [131], dual-gate FETs [132], or FETs used as varistors [133]. When passive detectors are applied, the detector loading conditions, which are determined by the input impedance of the control circuit, are of importance. With respect to regeneration, high input-impedance weight circuitry, for instance, encountered in dual-gate FETs [127], are not attractive. Basically, the controlling circuit in a separated-control tap is a programmable attenuator. Since it is fed by a constant detector output signal, which is maximized in order to achieve high efficiency and a wide control range, attention should be paid to electromagnetic (EM) feedthrough in the attenuating circuitry, which will ultimately limit the tap on-off ratio and the RF tap-to-tap isolation.

(ii) Integrated-control tap

In the Integrated-Control Tap, the detection and control functions are merged into a single element, which is located in the SAW propagation path. The output signal is controlled by varying the DC bias conditions of the detector. This change may affect the output admittance Y_d, or the acoustoelectric detection mechanism itself. The latter case results in a direct control of the detector current i_d.

When the detector output is not short-circuited but loaded with Y_l, the current i_l through the load becomes

$$i_l = \frac{Y_l}{Y_l + Y_d} i_d \tag{3.6}$$

The load current i_l can be varied by changing Y_d. This control mechanism can be applied in order to make integrated-control taps which employ the passive detection mechanism. The output admittance of the passive detector is dominated by the static capacitance between the electrodes and the conductive silicon. In the A or B configuration, this capacitance is a MOS capacitance, the value of which can be varied by changing the DC bias voltage. In fact, the detector acts as a varactor element. The load admittance at the detector output must be purely capacitive, otherwise the variation in Y_d will not only change the output amplitude but the output phase as well. Current-sensing of the detector output ($Y_l \rightarrow \infty$) cannot be applied, since it would eliminate the controlling action of Y_d completely.

In the MOS varactors, only a limited control range can be obtained. The control range is determined by the minimum and maximum capacitance values that can be reached. The maximum capacitance is the oxide capacitance under accumulation conditions. Depleting the silicon surface decreases the capacitance, but the lower limit is determined by the onset of inversion. In Reference [134], a control range in a single MOS tap of only 4 dB is reported. A larger control range can be obtained using the junction structures (configuration C). A very small off-value of the output signal is obtained, when the *pn* structure is biased in the forward direction. In this case, the electrode is completely short-circuited to the conductive substrate. In Fig. 3.5, the normalized amplitude and phase responses of a p^+ junction electrode are shown as a function of the bias voltage. The p^+ electrode is located in an *n*-type substrate with a conductivity of 10 S/m. The responses were measured at 95 MHz, and the load impedance was 50 Ω. Reverse biasing the junction electrode only gives an amplitude change of about 3 dB. When the junction is forwardly biased,

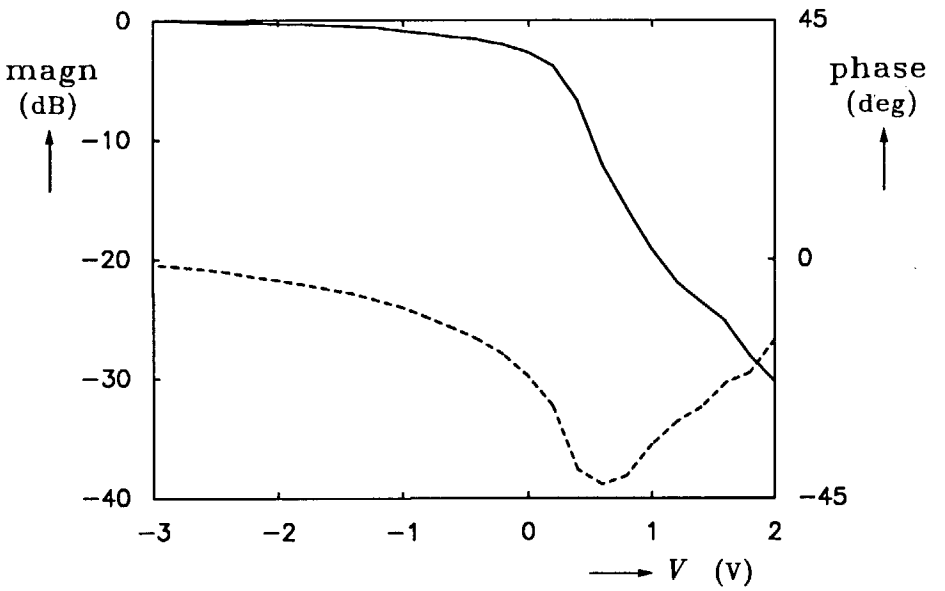


Figure 3.5: *Normalized amplitude (solid) and phase (dashed) responses at vs. the bias voltage of a junction electrode (f_0 is 95 MHz, load impedance is 50 Ω).*

the amplitude drops by more than 30 dB. However, one should note the large phase deviation accompanying the controlling action, which is not only caused by the resistive load, but also by the resistive components in the electrode itself.

The integrated control in the active detector is realized quite differently. Since the output signal is directly determined by the auxiliary electric power source, the output amplitude of the active detector can effectively be controlled by simply varying the supplied electric DC power. One actually controls the efficiency of the acoustoelectric conversion process itself. In the active detectors discussed in section 3.2.2, this corresponds to a control of the DC bias current. Because only the detector efficiency is varied, no phase variations occur. Therefore, the active detection mechanism is very attractive for the realization of Integrated-Control Taps.

Because the active detection mechanism can be suppressed completely by a removal the bias signal, very low off-values can be obtained. In the active, piezoelectric SAW detector the off-value is limited by the passive coupling, which is present in any piezoelectric detector: a passive detection signal results from the capacitive coupling of the SAW to the source and drain electrodes of the active detector. If the active detection mechanism

is suppressed completely, a residual output signal caused by this passive coupling mechanism still remains, and causes a bad off-value of the active tap. In the PI-FET for example, only a control range of 8 dB is reported [115]. This phenomenon should be taken into account when designing an active tap, and is further dealt with in the following chapters. It should be noted that this residual passive coupling is not present in the active, piezoresistive SAW detector.

In the parametric detector, the auxiliary power source cannot be employed for amplitude control because the auxiliary acoustic power supply serves all taps. The individual tap strengths must be controlled by varying the bias conditions, and thus the mixing efficiencies, of the taps themselves.

The integrated-control concept eliminates the need for complex RF weight circuitry. Since the RF signal processing is restricted to a small area, parasitic effects such as crosstalk, and losses in the RF connecting leads and in the weight circuitry itself, are minimized. The detector signal is controlled directly at the origin, which yields higher off-values and better RF tap-to-tap isolation.

3.3.2 Phase Control

In practical filter realizations, two cases concerning the tap phase control must be distinguished. In the first class of filters, only a phase switch between 0 and 180 degrees is required, thus defining the RF polarity of the tap output. This is encountered in digitally coded, matched filters. Taps that can produce both positive and negative weight factors are called *bipolar*. Bipolar, separated-control taps can be constructed using diode switches [130], whereas the RF polarity of some integrated-control taps can be changed by reversing the bias conditions [126]. A polarity control with *unipolar* devices can only be obtained by using two detectors, which provide signals of opposite RF polarity. The total tap output is the weighted sum of the two detector outputs. The 180 degree phase difference can be obtained by displacing the detectors by $\lambda/2$ in the SAW propagation path, thereby doubling the detector density. One can also use two parallel PTDL channels, the outputs of which are fed into a differential amplifier. This latter, dual-channel configuration has additional advantages with respect to common-mode rejection, and is further examined in Chapter 6.

In the second class of filters, a continuous phase control between 0 and 360 degrees is required. This is, for example, encountered in adaptive filters. Although in theory it is possible to control the detector phase

directly, in practice it is very difficult to adjust the phase without affecting the amplitude as well. To the author's knowledge, no direct phase control in SAW detectors has yet been reported. Again the problem can be solved by using two detectors per tap, which are now 90 degrees out of phase. A vector addition produces the required result, see Fig. 3.6. An arbitrary tap phase (and tap amplitude) between 0 and 90 degrees can be obtained by adjusting the (real) output amplitudes a_i and a_q of the in-phase and quadrature detectors, respectively. A 360 degrees phase control is obtained with four TDL channels, which provide signals at 0, 90, 180 and 270 degrees [135].

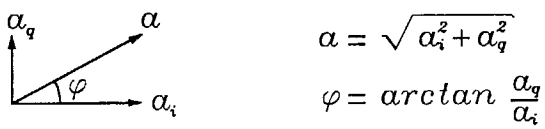


Figure 3.6: *Vector phase control.*

3.4 JUNCTION STRUCTURES

In the introduction, it was mentioned that by using the C configuration shown in Fig. 3.1, the detector electrodes can be made with *pn*-junction structures at the silicon surface. These junction structures are created by diffusion or ion-implantation processes. Junction electrodes minimize the mechanical disturbances in the SAW propagation path. These disturbances give rise to wave reflections. An elaborate study of reflections at the junction electrode is presented in the next section. Another advantage of the junction electrode is the flat surface that remains above the detector. This improves the growth of high-quality piezoelectric layers. The growth of ZnO layers strongly depends on the conditions of the underlying substrate. Irregularities of the substrate surface disturb the initial growth process. Metal electrodes underneath the film (configurations B and C) are such growth disturbances. The nonzero height of the electrodes prevents a uniform growth above the detector structure. In addition, the local substrate conditions at the metal electrodes (for instance the thermal conductivity) differ from the surroundings, which also give rise to deviations in the film growth. In Chapter 6, the growth of ZnO and its quality under different conditions are further examined. Junction electrodes provide a smooth surface on which high-quality film deposition is feasible. As a consequence, in the region above the junction detector, a high piezoelectric coupling strength and a low propagation loss can be achieved.

3.4.1 Junction Electrode Reflections

The detectors located in the SAW propagation path represent an array of periodic reflection centers. They cause multiple SAW reflections between the taps, triple-transit SAW echoes between the transmitting transducer and the tapped array, and bulk wave scattering. These effects can severely distort the filter performance because of spurious echo signals and attenuation of the SAW amplitude [118].

The reflections are caused by a change in the electrical conditions (electrical loading), a change in the elastic conditions (mechanical or mass loading) and by topological (step) discontinuities, all introduced by the presence of the electrodes of the SAW detectors. For a first-order approximation, the change in acoustic impedance caused by the loading effects can be derived from the velocity change $\Delta v/v$ [136]. The electrical and mechanical reflection coefficients r_e and r_m at the edge of the electrode can be estimated with

$$r_{e,m} = \frac{Z_1 - Z_0}{Z_1 + Z_0} = \frac{v_1 - v_0}{v_1 + v_0} \approx \frac{1}{2}\frac{\Delta v}{v}\bigg|_{e,m} \tag{3.7}$$

in which Z_1, v_1 and Z_0, v_0 are the acoustic impedances and SAW phase velocities under loaded and unloaded conditions, respectively. The fractional deviations $\Delta v/v|_e$ and $\Delta v/v|_m$ refer to the perturbations in the SAW velocity, which are caused by the electrical and mechanical loading, respectively. They can readily be found with the programs mentioned in section 2.2.4, by using infinitely thin, perfectly conducting sheets for the determination of the electrical loading effects, and by varying the elastic material constants for the mechanical loading effects. For the step discontinuity of height h_{step} the derivation of the reflection coefficient is more complicated [137], but can be approximated by

$$r_{step} = C_{step}\frac{h_{step}}{\lambda} \tag{3.8}$$

where λ is the average SAW wavelength. C_{step} is a constant which depends on the material constants and the wave direction with respect to the crystal orientation.

When a complete electrode is considered, the reflections from both the leading and trailing edges must be taken into account. For the mechanical loading, the total reflection coefficient R_m, referred to the center of the electrode of length L, becomes

$$R_m = j\,\frac{\Delta v}{v}\bigg|_m \sin(kL) \tag{3.9}$$

The electrode reflection caused by the electrical loading is more complicated because of the acoustoelectric interactions in the conductive electrode. A detailed theory is given in Reference [128, appendix E], and shows that the electrical reflection coefficient R_e is

$$R_e = jF(kL)\left.\frac{\Delta v}{v}\right|_e \tag{3.10}$$

F is composed of a number of Legendre functions. It depends on the electrical conditions around the electrode, and is different for floating and for short-circuited electrodes. In practice, F has a value somewhere between 0 and 2. For the step discontinuity the total reflection coefficient R_{step} becomes:

$$R_{step} = 2jC_{step}\frac{h_{step}}{\lambda}\sin(kL) \tag{3.11}$$

For step discontinuities in piczoelectric substrates like $LiNbO_3$ and quartz, a $C_{step} \approx 0.5$ to 0.7 is reported [137]. For the layered configuration under consideration, no values are reported, but it is reasonable to assume they are of the same order of magnitude.

It can be shown that the reflections of junction electrodes are far smaller than those of metal electrodes. As a reference, a quarter-wave electrode ($L = \lambda/4$) is considered, in which case the reflections caused by the mechanical and topological discontinuities at the leading and trailing edges are in phase.

For a comparison of the mechanical reflections, an aluminum and a junction electrode at the silicon surface are considered. For the Al electrode, the $\Delta v/v|_m$ can be obtained by adding an extra layer in the layered system with the material constants of aluminum, which is isotropic. The reflection coefficient R_m of an aluminum electrode as a function of the normalized aluminum thickness h_{Al} is presented in Fig. 3.7. It was calculated for a ZnO layer thickness of $\omega h_{ZnO} = 8000\,\mathrm{rad\,m/s}$, whereas the SiO_2 thickness was ignored. The material constants presented in Table 2.1 were used. In order to mask the electrical loading effect, the perturbed and unperturbed velocities were both determined by using an infinitely thin, perfectly conducting plane between the ZnO and the aluminum layer. For the mechanical reflections caused by a junction electrode, the influence of doping on the elastic constants must be considered. In section 2.7.3 it was shown that the stiffness tensors c_{11},c_{12} and c_{44} of the semiconductor are related to the deformation potential, and depend on the doping concentrations. The reflection of the junction electrodes can be determined by adding an extra silicon layer between the SiO_2 layer and the Si substrate.

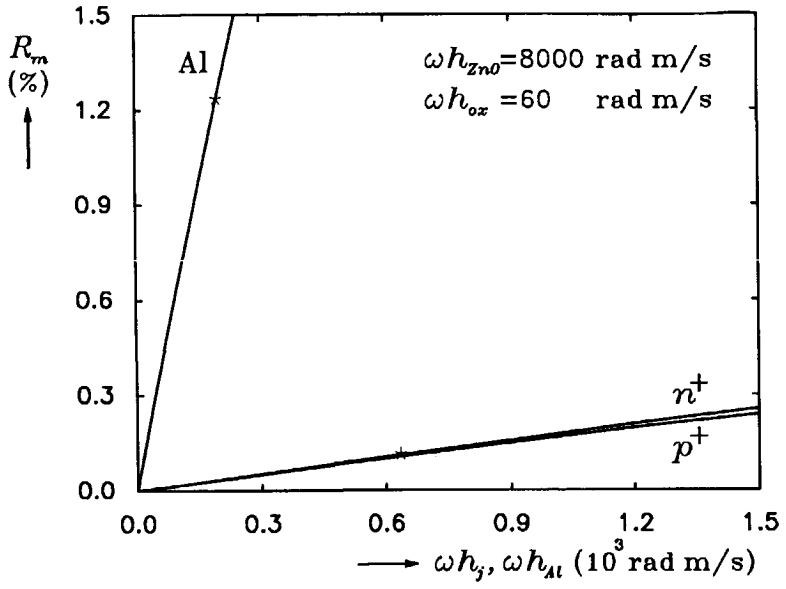


Figure 3.7: *Comparison of mechanical reflection coefficients of an aluminum and junction $\lambda/4$ electrode.*

In this extra layer the deviations in the stiffness tensors, which are given in Fig. 2.7 and 2.8, are incorporated. The thickness of this layer corresponds to the junction depth h_j. Assuming a doping level in the junction electrodes of 10^{26} m^{-3}, the mechanical reflection coefficients of quarter-wave p^+- and n^+-junction electrodes as function of ωh_j are shown in Fig. 3.7. The background doping of the Si substrate is assumed to be less than 10^{22} m^{-3}. The deviations in the stiffness tensors, which were used in the simulations, are shown in Table 3.1. The deviation in c_{44} in the n-type material was extrapolated from the measured value given in Fig. 2.7. In the simulation, the SiO_2 thickness was ignored, and $\omega h_{ZnO} = 8000$ rad m/s was taken. Comparing the results at f_0=100 MHz for an Al electrode of

Table 3.1: *Relative deviations in stiffness tensors for p^+ and n^+ silicon with $N_A, N_D = 10^{26}$ m^{-3}.*

dc/c	p^+ (%)	n^+ (%)
dc_{11}/c_{11}	−1.5	−2.7
dc_{12}/c_{12}	+1.9	+3.5
dc_{44}/c_{44}	−3.4	−0.8

about $0.3\,\mu$m thickness and a junction electrode with a junction depth of about $1\,\mu$m (both indicated by $\star$ in Fig. 3.7) it can be concluded that the junction electrode produces reflection levels of more than an order of magnitude smaller than the Al electrode. It can be derived that the edge reflection coefficient of the junction electrodes with the indicated doping level is about $r_m \approx 0.015 h_j/\lambda$.

For the electrode reflections which result from electrical loading, no straightforward treatment can be given. They strongly depend on the detector structure in which the electrode is used. A good representation of the electrical conditions surrounding a junction electrode is shown in Fig. 3.8. Since the surrounding silicon is conductive ($\omega \ll \omega_c$), it can be considered as a conductive plane. The nonconductive parts between the electrode and the substrate are created by the depletion layer around the junction electrode. These nonconductive parts induce an electrical perturbation, but for depletion widths much smaller than λ, small reflection levels result.

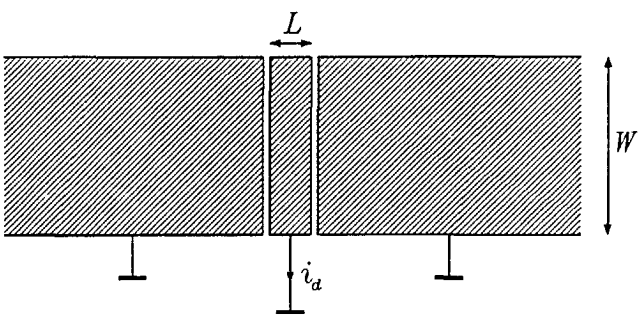


Figure 3.8: *Schematic of the electrical conditions around a junction electrode.*

The topological discontinuities at the edges of a metal electrode are proportional to the thickness of the metal layer (Eq. 3.8). The reduction of the metal layer thickness is limited by the electrode resistance. In the devices presented in this work, the metal layer thickness is about $0.3\,\mu$m. The topological discontinuities at the edges of the diffusion electrodes are caused by the different growth of the SiO_2 layer on doped and undoped regions. However, in a proper processing sequence, it can be achieved that the differences become negligible. The junction devices discussed in Chapter 4 are created by ion-implantation through a thin SiO_2 layer, in which case no step discontinuities are measurable.

3.4.2 SAW Detectors using Junction Electrodes

For an unperturbed SAW propagation, the programmable SAW detectors should preferably be constructed by using junction electrodes; metal parts in the propagation path must be avoided. In this section, the consequences of applying junction structures in passive and active detectors is examined. Since the detection process of detectors which are composed of junction electrodes takes place at the SiO_2-Si interface, the acousto-electric conversion efficiency is influenced by the SiO_2 thickness h_{ox}. This is illustrated in Fig. 3.9 in which the Equivalent-Surface-Charge method has been applied with the plane $x_3 = 0$ as a reference, in order to obtain the equivalent surface charge ρ_{s0} at the SiO_2-Si interface. As expected, the charge decreases with increasing (normalized) thickness of the SiO_2 layer. Therefore, only thin SiO_2 layers are allowed above SAW junction detectors.

A passive junction detector is simply created by a reversed-biased *pn* electrode at the silicon surface. The short-circuited detector current of a single electrode of length L can be calculated using the ESC method. The piezoelectric action of the SAW, which is represented by the equivalent surface charge at the SiO_2-Si interface, induces a screening charge at the conductive electrode and the planes of Fig. 3.8. If the separation between

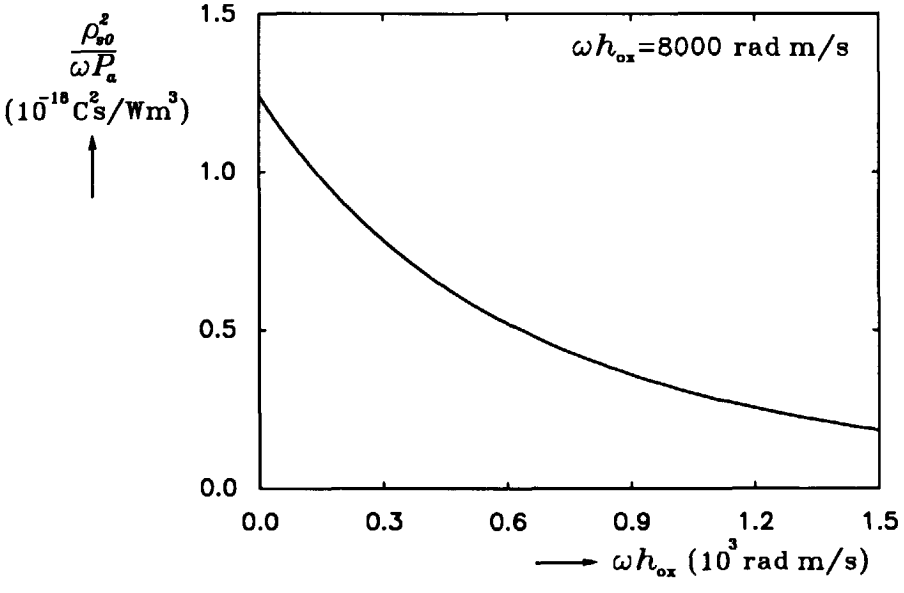


Figure 3.9: *Equivalent surface charge ρ_{s0} at SiO_2-Si interface vs. ωh_{ox}.*

the electrode and the planes, which is determined by the depletion layer width, is much smaller than λ, an harmonic charge distribution on the conductive elements can be assumed. In this case, the equivalent surface charge at the SiO_2-Si interface is completely compensated by the free charges induced at the electrode and the conductive planes. As a consequence, the charge induced at the electrode is identical to the equivalent charge above the electrode, except for a sign change. The short-circuit current can be obtained by determining the total free charge at the electrode, and taking the time derivative. Assuming the equivalent surface charge varies as $\rho_{s0}\sin(kx_1 - \omega t)$ the detector current i_{d0} (A/m) becomes

$$i_{d0}^2 = \left| j\omega \int_0^L \rho_s dx \right|^2 = 4v_{ph}^3 P_a \left(\frac{\rho_{s0}^2}{\omega P_a} \right) k \sin^2(kL/2) \qquad (3.12)$$

The normalized surface charge $\rho_{s0}^2/\omega P_a$ was evaluated in section 2.3 (see Fig. 2.4). When the gap between the electrode and the adjacent planes in Fig. 3.8 becomes comparable to the wavelength, the induced charge can no longer be assumed harmonic. In this case, Fourier techniques must be applied similar to those described by Morgan for piezoelectric substrates [128, ch. 3 and 4].

A disadvantage of junction electrodes compared to Al electrodes is the rather high series resistance. For junction electrodes, the sheet resistance is in the order of 5–50 $\Omega/\square$, whereas in Al electrodes a couple of m$\Omega/\square$ are involved. The series resistance in the electrode increases the RF losses and deteriorates the signal-to-noise ratio (SNR) of the detector. The junction electrode has to be represented by a distributed RC network like that shown in Fig. 3.10. The inductive parts are ignored. The resistances are

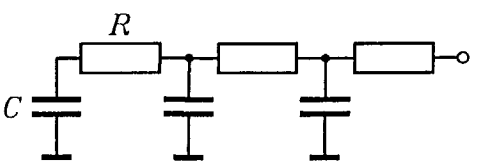


Figure 3.10: *Distributed RC network representing the junction electrode.*

determined by the sheet resistivity of the implanted region, whereas the capacitances are determined by the depletion layer capacitance of the *pn* junction. The small length of the junction electrodes in the junction IDT ($L = \lambda/4$) was the main reason for the high losses. The length of the single-electrode detector can be increased provided L measures an odd number times $\lambda/2$ (see Eq. 3.12), however, at the expense of the acoustic bandwidth.

For active detectors composed of junction detectors, the situation is quite different. The drain and source electrodes that lead the RF signals out of the propagation path, are not involved in the actual SAW detection process, and can, therefore, be of any length without deteriorating the bandwidth or the detection efficiency. In addition, the internal gain, exactly at the detection location, is advantageous with respect to the SNR. If a SAW detector is required, which has to be composed of junction electrodes in order to minimize the SAW propagation perturbations, the active detection mechanism is indispensable.

3.5 CONCLUSIONS

In order to minimize tap reflections in the PTDL, the programmable taps must be realized using *pn*-junction electrodes. The junction structures can be made using standard IC processes, and the interconnections between the tap and peripheral electronics are readily attained. The ZnO sputter deposition can be postponed till the final process step.

To minimize losses and maximize the SNR, the junction detectors require an active detection mechanism. In the active detector, the electric fields accompanying the SAW merely modulate an electric bias signal. Because of the internal gain, high efficiencies can be expected without a large power extraction from the acoustic wave. Because the mechanism is irreversible, SAW regeneration is absent and the detection process is insensitive to the load impedance. The output amplitude can be simply controlled by an adjustment of the bias signals. The merging of detection and control functions results in an Integrated-Control tap, and provides a compact programmable detector with low EM feedthrough deterioration and high RF tap-to-tap isolation. The absence of the active detection mechanism when the auxiliary bias signal is removed ensures a low off-value and a large control range. Although the piezoresistive coupling mechanism is attractive for use in the acoustoelectric conversion process, the coupling strength is weak and the DC power dissipation becomes rather large for acceptable efficiency levels. Therefore, in this work only the piezoelectric coupling mechanism is considered.

In the following chapters two implementations of an active, piezoelectric junction detector are presented: the Barrier-Modulated Tap (BMT) and the Piezoelectric Junction FET (PI-JFET). These piezotronic elements are very suitable for the construction of monolithic, full-silicon PTDLs in the ZnO-SiO_2-Si layered structure.

Chapter 4

THE BARRIER-MODULATED TAP

4.1 INTRODUCTION

In Chapter 2, it was shown that the penetration of the SAW electric fields in a semiconducting medium depends strongly on the concentration of mobile charge carriers. Under flat-band conditions, the penetration depth is in the order of the Debye length. The field strength and penetration depth can be increased considerably by depleting the silicon surface. This can be achieved by placing a field plate on top of the ZnO layer to deplete the silicon surface from above. This is, for instance, encountered in Acoustic-Charge-Transfer devices. However, the metal plate requires extra deposition and etching steps after the ZnO deposition. In addition, applying a bias voltage through the ZnO layer is not very attractive as was discussed in section 2.6.

The active, piezoelectric junction detector presented in this chapter uses the lateral depletion region between two closely spaced junction electrodes. When the junctions are reversely biased, the depletion regions not only expand vertically but also laterally. When the lateral depletion region boundaries in the gap between the electrodes touch, the gap region is completely depleted, and the SAW electric fields can freely penetrate into this gap. A current of minority carriers flows between the electrodes, and is modulated by the SAW electric fields. Since the injection of minority carriers is controlled by a potential barrier at the forward-biased

junction, the acronym BMT for *Barrier-Modulated Tap* is used throughout this chapter.

In the next section, the basic operation of this reach-through device is explained. Firstly, the potential distribution and the current transport in a one-dimensional case are discussed. Then a two-dimensional treatment is given. In section 4.3, the SAW detecting capabilities of the reach-through detector are investigated, followed by a discussion of an equivalent circuit model in section 4.4. Finally, in section 4.5 the device fabrication is discussed, and in section 4.6 the experimental results are presented.

4.2 REACH-THROUGH OPERATION

4.2.1 One-Dimensional Case

The basic structure of the BMT consists of two *pn* diodes in series, resulting in a *pnp* or *npn* configuration. In this two-terminal device, the middle region is not connected; it can, therefore, be considered as a bipolar transistor with a floating base. In this section only the *pnp* configuration is considered.

The structure under consideration is depicted in Fig. 4.1a. Highly doped p^+ regions create the contacts of the device. The central n^- region is uniformly doped with a low doping concentration N_D. The junctions are considered abrupt, and the depletion regions around the junctions are mainly located in the n^- region. When a voltage is applied across the terminals, one of the p^+n junctions is reversely biased. In Fig. 4.1 the right junction is assumed to be reversely biased, and is denoted as drain D, whereas the other junction is denoted as source S. No current can flow because of the blocking action of the drain junction. When the applied voltage is increased, the depletion region of the drain junction expands through the n^- region, and eventually reaches the depletion region of the opposite junction. At this point, a *reach-through* or *punch-through* condition has occurred, and the central n^- region is completely depleted. For moderate doping levels N_D, and a small distance L between the junctions, avalanche multiplication can be avoided and the reach-through voltage remains substantially below the breakdown voltage of the reverse-biased drain junction.

The electric field and potential distribution at reach-through (RT) can be obtained by using Poisson's equation

$$\frac{dE}{dx} = \frac{qN_D}{\epsilon_{Si}} \tag{4.1}$$

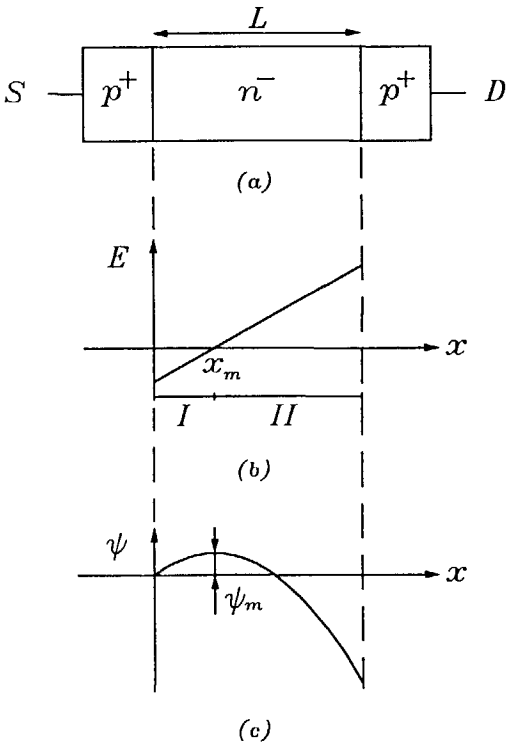


Figure 4.1: *Basic RT diode: (a) one-dimensional structure; (b) electric field distribution with injection region (I) and drift region (II); (c) potential distribution.*

The electric field and the potential are depicted in Fig. 4.1b and c. The potential distribution in the n^- region is characterized by a small potential barrier in front of the source junction. Up to RT, the barrier height ψ_m ($=\psi(x_m)$) measured with respect to the source potential, equals the built-in potential V_{bi} of the source p^+n junction. Beyond RT the relationship between the applied voltage V_{DS} and the barrier height becomes [138]

$$\psi_m = \frac{(V_{DS} - V_{FB})^2}{4V_{FB}} \tag{4.2}$$

in which V_{FB} is the flat-band voltage defined as

$$V_{FB} = \frac{qN_D}{2\epsilon_{Si}} L^2 \tag{4.3}$$

and represent the drain-to-source voltage for which the barrier height ψ_m has been reduced to zero. The RT voltage V_{RT} can be derived from Eq. 4.2

with $\psi_m = V_{bi}$. A further increase of the applied voltage beyond RT lowers the potential barrier; the source junction is forwardly biased and starts to inject holes, which drift through the depleted gap and are collected by the drain of the RT diode.

When the device is biased towards RT, the electrons (majority carriers) are extracted from the n^- region. Injection of electrons is prevented by the high potential barrier at the reverse-biased drain junction. Small electron currents only originate from leakage and electron-hole generation in the depleted n^- region. In this analysis, the electrons are ignored. The RT diode can be considered as a unipolar device, in which minority carriers (holes) dominate the current transport. It should be noted, however, that recombination and storage effects which are normally encountered in minority-carrier devices, can be ignored.

Beyond RT the n^- region can be divided into two regions:

1. the *injection region* beside the source junction, which includes the potential barrier.
2. the *drift region* where the injected charge carriers are accelerated by the electric field of the drain.

The two regions are separated by the injection plane at x_m, where the barrier reaches its maximum, and the electric field becomes zero and changes sign.

(i) The injection region ($0 < x < x_m$)

The injection region ranges from the source junction ($x = 0$) up to the barrier maximum ($x = x_m$). At $x = x_m$ the holes are injected into the drift region. The position of x_m is not constant, but depends on the applied voltage and the current density. For small current densities, the concentration of injected holes is much smaller than the concentration of ionized donors, and x_m can easily be derived from Eq. 4.1. However, for higher current densities, the space charge of the injected holes must be incorporated into the calculations, and the slope of the electric field increases

$$\frac{dE}{dx} = \frac{q(N_D + p)}{\epsilon_{Si}} \tag{4.4}$$

where p is the injected hole density which is associated with the current. Because the electric fields are small, both the diffusion and the drift components of the hole current density J_p must be taken into account

$$J_p = pq\mu_p E - qD_p \frac{dp}{dx} = -\mu_p qp \frac{d\psi_{Fp}}{dx} \tag{4.5}$$

in which ψ_{Fp} is the quasi-Fermi potential for holes. Because of the nonlinear behavior, equations 4.4 and 4.5 can only be solved numerically. The electric field distribution resulting from the numerical analysis carried out by Sjölund [139] shows a decrease of x_m for increasing current densities, see Fig. 4.2a. Characteristic for the injection region is the retarding electric

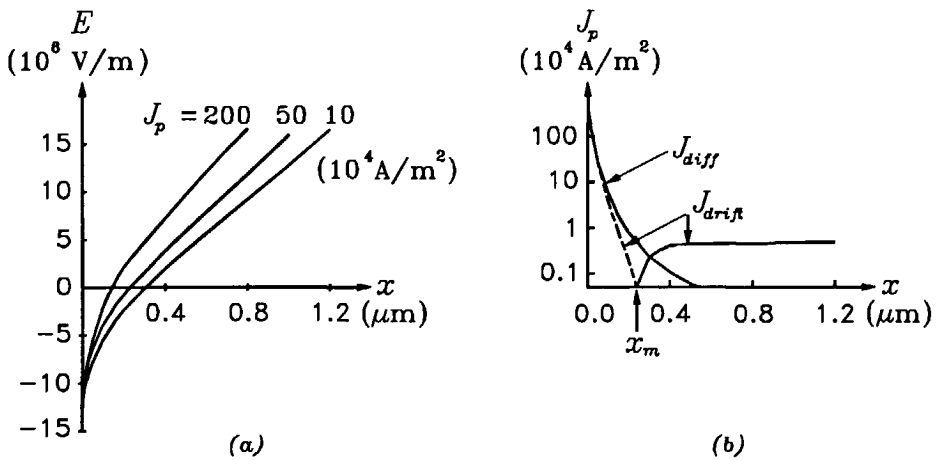


Figure 4.2: *(a) Influence of space charge on E with J_p as parameter; (b) current distribution in injection region; the dashed line represents a negative drift current.*

field, which causes a drift current towards the source junction. This drift current opposes the diffusion current as is shown in Fig. 4.2b. The net current represents the hole current which is injected across the barrier. For all practical bias currents, the gradient in the quasi-Fermi potential ψ_{Fp} is very small in the injection region [140, 141], and the holes in the injection region can be considered in thermal equilibrium with the source. The hole density can then be approximated with

$$p = N_v \exp\left(-\frac{q\psi(x)}{k_B T}\right) \tag{4.6}$$

where $\psi(x)$ is the static potential in the injection region relative to the source potential. In Eq. 4.6, it is assumed that the Fermi level in the highly doped p^+ source coincides with the edge of the valence band, in which case the number of free carriers in the source equals the density of states N_v in the valence band.

The description of the hole injection across the potential barrier is not obvious. At the barrier maximum the electric field is zero, and the current

is driven by a thermal diffusion process. The majority of authors describing the carrier injection in *pnp* RT diodes use the thermionic emission theory, which was originally developed to describe the current transport across a Schottky barrier [142, pp. 254–270]. However, the thermionic emission theory assumes a barrier width which is much smaller than the mean free path of the carriers, in which case carrier collisions can be neglected. In the considered *pnp* structure this condition only holds at low temperatures or at high doping levels ($N_D > 10^{23}$ m^{-3}) of the central n region. The diffusion theory of Schottky includes the carrier collisions, but predicts current levels considerably above the levels found experimentally [143]. A combined thermionic emission-diffusion theory is described by Crowell *et al.* for Schottky barriers [144], and further elaborated by Persky for *pn* barriers [145]. In the latter theory, the diffusion currents are limited by including a thermionic saturation effect, which prevents the currents from rising above the thermionic emission limit. In any case, the evolving current relations in the various theories look very similar: the current density J_p exponentially depends on the barrier height ψ_m

$$J_p = J_{ps} \exp\left(-\frac{q\psi_m}{k_B T}\right) \tag{4.7}$$

and only the saturation current density J_{ps} differs in each case. In the following analysis, the injection current is assumed to be barrier controlled as indicated by Eq. 4.7, and independent of the shape of the barrier. For the devices described in this work, the mean free path of the holes is much smaller than the barrier width, and the saturation current proposed by Persky is used [145]

$$J_{ps} = \frac{qD_p N_v}{\sqrt{2\pi} L_D} \tag{4.8}$$

where L_D is the Debye length in the n^- region.

(ii) The drift region ($x_m < x < L$)

In the drift region, the electric field rises rapidly. At x_m the holes are injected at a finite thermal velocity [140], and are subsequently accelerated by the drift field. As a consequence, the diffusion component of the hole current drops rapidly, and drift becomes the dominant current mechanism, see Fig. 4.2b. Ignoring the small part of the drift region next to the injection region where the diffusion currents are important, the electric field and potential distribution for $x > x_m$ can be obtained from Eq. 4.4

by replacing p with J_p/qv_d

$$\frac{dE}{dx} = \frac{qN_D}{\epsilon_{Si}} + \frac{J_p}{\epsilon_{Si}v_d} \tag{4.9}$$

where v_d is the hole drift velocity. The solution of this equation is hindered by the field-dependence of the hole mobility μ_p, which determines v_d

$$v_d = \mu_p(E)\, E \tag{4.10}$$

At higher field levels, μ_p decreases, and the hole velocity approaches the saturation velocity v_s ($v_s \approx 10^5$ m/s). In a crude approximation, the drift region can be divided into a low-field part, in which μ_p is constant, and a high-field part, in which the holes move at their scattering velocity v_s. Since J_p is constant in Eq. 4.9, the slope of E will be largest at x_m, gradually decrease in the low-field region as a result of the rising velocity, and finally stabilize in the high-field region. When the current rises, the low-field part decreases, because the critical field at which velocity saturation takes place is reached more rapidly.

Using the description of the current and potential relations in the injection and drift regions, the relation between the current and the applied drain-to-source voltage V_{DS} can readily be obtained. When the applied voltage is increased from zero to its maximum value, three current ranges are passed through: the sub-RT range, the RT range, and the space-charge-limited range. A typical IV–characteristic is shown in Fig. 4.3. For voltages smaller than V_{RT}, the device acts as a bipolar p^+np^+ transistor with floating base. In the sub-RT range, the potential barrier at the source junction remains at the built-in voltage V_{bi}. In this range, the current is dominated by leakage and electron–hole pair generation in the "base" region. Although the currents are small, they can be worse than expected from simple diode theories because of the amplification mechanism in the transistor. For voltages a little larger than V_{RT}, injection of holes takes place, and the current rises rapidly with increasing V_{DS}. At low injection, the space charge of the injected holes can still be ignored, and the drain potential is directly related to the impurity concentration N_D in the n^- region. In this region, ψ_m is proportional to V_{DS}^2, see Eq. 4.2. In the RT range, the current density J_p becomes exponentially dependent on V_{DS}^2, see Eq. 4.7.

At high bias currents, the space charge of the injected holes becomes comparable to the impurity concentration N_D, and the strong relationship between ψ_m and V_{DS} lessens. The current is now mainly determined by

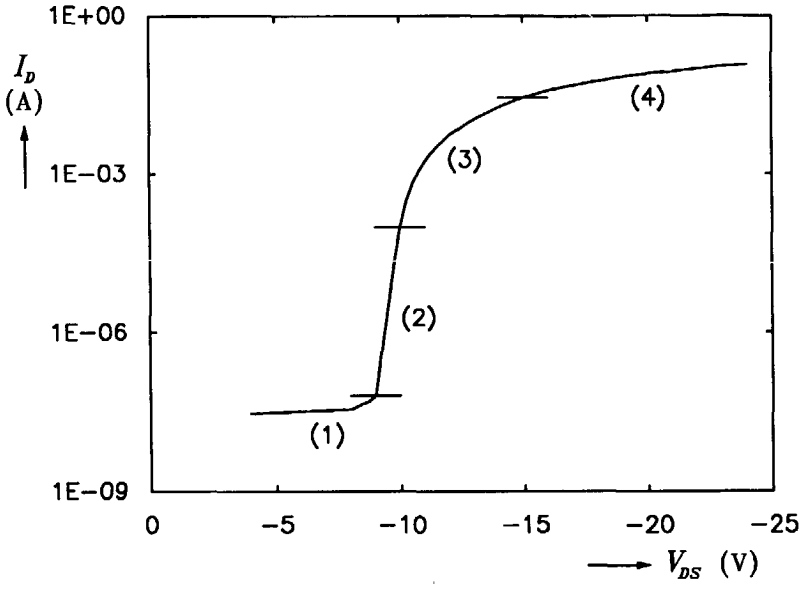


Figure 4.3: *Typical IV-characteristic of RT diode showing the sub-RT* (1), *RT* (2), *SCL with* $v_d = \mu_p E$ (3), *and SCL with* $v_d = v_s$ (4) *ranges.*

the concentration of (mobile) space charge in the n^- region, which can be supported by the applied voltage. The current is said to be *space charge limited.* The exact relation between the space-charge-limited (SCL) current and V_{DS} depends on the velocity of the charge carriers [146]. If the electric field is sufficiently low, the mobility can be considered constant, and the current becomes proportional to V_{DS}^2. This quadratic relationship was first described by Mott and Gurney for SCL currents in insulators [147]. A further rise of V_{DS} increases the electric field strengths, and a high-field region originates at the drain side, in which hot carriers move at their saturation velocity. In the end, the high-field condition prevails in the entire gap region, and a linear relationship between J_p and V_{DS} results. The drift region then acts as a space-charge resistance [142, pp. 575–577]. It should be mentioned that, although the applied voltage in the SCL case is completely determined by the mobile space charge in the drift region, it is assumed that the injection current is still exponentially related to the barrier height ψ_m as indicated by Eq. 4.7.

In the RT range the applied voltage has a negative temperature coefficient [138]. For a degenerate source, the saturation current described by Eq. 4.8 is proportional to T^2 [145]. However, in the SCL range the

temperature dependence is strongly reduced, and excellent temperature stabilities are reported with voltage sensitivities of less than 0.1 mV/°C at a constant bias current [148].

Another aspect of concern is the noise behavior of the RT diode. In the RT diode two noise mechanisms are present [139]: shot noise of the injected charge carriers, and random velocity fluctuations of the carriers in the drift region. The noise current i_n ($A/\sqrt{Hz}$) is given by

$$i_n^2 = 2qI_D\Gamma^2 \tag{4.11}$$

in which I_D is the bias current. The shot noise is reduced by a space-charge suppression factor Γ ($\Gamma < 1$). This factor represents the smoothing effect, which is caused by the space charge of the injected carriers. For low currents, no SCL effects occur and $\Gamma \approx 1$. However, for large current levels, the space-charge smoothing must be taken into account. In the SCL range, the suppression factor can be approximated by [149]

$$\Gamma \approx \frac{2k_BT}{qV_{DS}} \tag{4.12}$$

At high current levels, the contribution of the shot noise is small because of the space-charge smoothing. In this case, the velocity fluctuations in the drift region become dominant [150]. Space-charge smoothing of this noise source only takes place in the low-field part of the drift region. It can be concluded that the RT diode operating in its SCL range has low-noise behavior [151], and a good noise performance from reach-through SAW detectors is expected.

Much attention has been paid to the microwave performance of the RT diode. As a result of the combination of a barrier-controlled charge injection and a finite transit time through the drift region, a phase difference of more than 90 degrees between the current and voltage can occur. In this case, a negative resistance originates and the device acts as an oscillator. In practice, the negative resistance effects in these BARITT (BArrier Injection Transit Time) diodes takes place for frequencies in the GHz range [140, 152]. The devices considered in this work lack the proper dimensions to obtain a negative resistance. In addition, they mainly operate in the SCL range, which is not the optimal current range for microwave oscillations.

4.2.2 Two-Dimensional Case

The source and drain contacts of the Barrier-modulated Tap described in the introduction are created by two diffused or implanted p^+ regions in

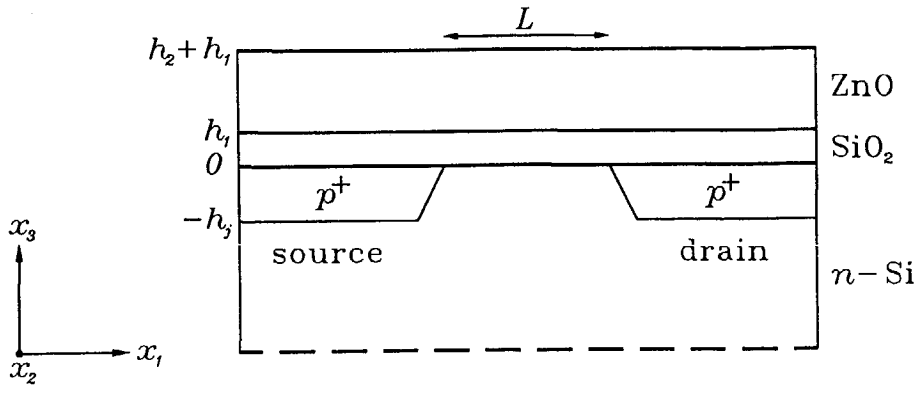


Figure 4.4: *2D structure of lateral RT diode.*

an n-type (epi)layer. This results in a planar configuration as depicted in Fig. 4.4 (not to scale). When a voltage is applied across the source and drain terminals, the depletion region around the drain electrode expands both vertically and laterally, and first reaches the source depletion region at the SiO_2-Si interface. Since the barrier lowering induced by the drain is maximal at this interface, the current transport is expected to be concentrated near the silicon surface.

Although the basic operation of the planar reach-through diode is similar to the one-dimensional case described before, the actual potential and current distributions are quite different, and a two-dimensional treatment is required. Conventional numerical methods can be applied to solve the two-dimensional Poisson equation [153]. A computer program was developed in order to obtain an impression of the potential distribution in the planar diode. A nonuniform, rectangular mesh is applied for partitioning. In the gap region, the grid density is locally increased to enhance the accuracy. The two-dimensional Poisson equation is discretized using a finite-difference method [154]. A five-point difference scheme is adopted. In this scheme the potential at a grid point is linearly related to its four adjacent grid points. At the interface planes $x_3 = 0, h_1$ and $h_1 + h_2$, a modified difference equation is required to include the discontinuity of the dielectric permittivity [154]. The normal component of the electric displacement field D_3, and the potential must be continuous across these interfaces. No doping profiles are included: the n layer is assumed to have a uniform impurity concentration N_D, whereas the p^+ junctions are assumed to have an infinite conductivity, and are treated as Dirichlet boundaries with fixed potentials. At the vertical boundaries, Neumann

conditions are applied, which results in vanishing lateral electric fields. Therefore, the vertical boundaries can be considered as mirror planes.

When the space charge of the injected holes is ignored, the charge distribution in the silicon is completely determined by the impurity concentration and the shape of the depletion layer boundaries. Since the abrupt depletion approximation is assumed, the space charge equals N_D in the depleted areas and is zero in the neutral areas. The set of finite-difference equations is iteratively solved using a point-by-point successive over-relaxation (SOR) method [155]. When the desired accuracy is reached, the solution is examined for self-consistency: if the normal fields at the depletion edges do not vanish, the depletion edges are adapted by a rearrangement of the fixed space charge and a new relaxation process is started. This method is repeated until a self-consistent solution is obtained.

It should be mentioned here that the resulting program is not optimal with respect to accuracy and computational speed. Other discretization schemes can be used [156], and faster relaxation methods can be implemented [157]. However, the approximated results give a good insight into the device behavior. In addition, the program excels by simplicity and flexibility, and unconventional phenomena like the SAW equivalent surface charge (see section 2.2.3) can readily be included.

In the following simulations, a fixed ZnO thickness of $h_2 = 10\mu$m and SiO_2 thickness of $h_1 = 0.1\mu$m are used. The impurity concentration of the n^- layer is set at $N_D = 5 \cdot 10^{20}$ m^{-3}, which corresponds to a conductivity of 10 S/m. Variable geometric parameters are the channel length L and the junction depth h_j. The highly doped p^+ regions are assumed to be implanted. The lateral out-diffusion is assumed to be linearly related to h_j, with a maximum of $h_j/2$ at the SiO_2-Si interface. The source potential V_S is fixed at 0 V, whereas the drain potential V_{DS} and the bulk potential V_{BS} of the n-layer with respect to the source can be chosen arbitrarily. It should be noted that the n-layer is not floating, but fixed at a proper potential V_{BS}. In fact, the n-layer represents an epilayer which is held at a fixed potential, as is discussed in section 4.6. Although V_{BS} influences the potential distribution in the gap, it does not change the RT operation substantially as long as $V_{BS}, V_{BD} > 0$. However, it is easily derived that it reduces V_{RT} and increases V_{FB}.

A calculated potential distribution for $h_j = 1\,\mu$m, $L = 5\,\mu$m, $V_{DS} = -10$ V and $V_{BS} = +4$ V is shown in Fig. 4.5. A built-in voltage of 0.8 V is assumed at the p^+n junctions. Only the region in the silicon area ($x_3 < 0$) is shown. From this illustration it is clear that the potential barrier in

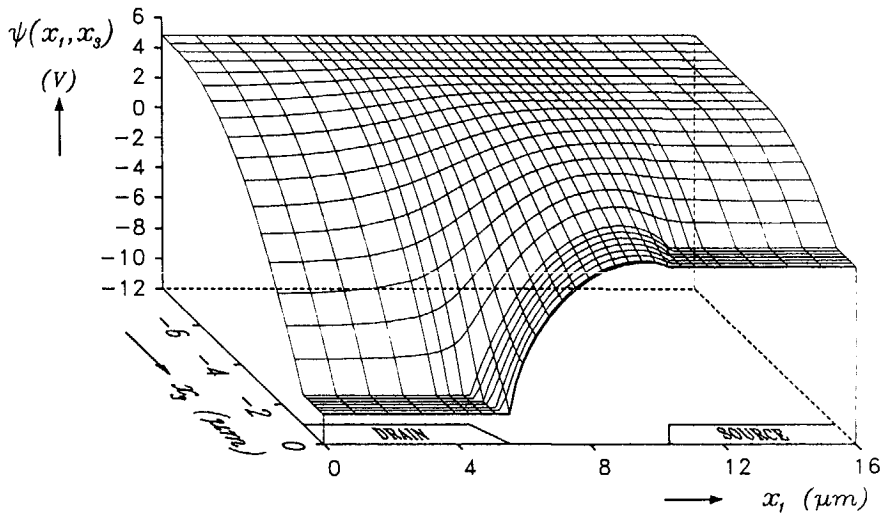


Figure 4.5: *Simulated 2D potential distribution in the BMT.*

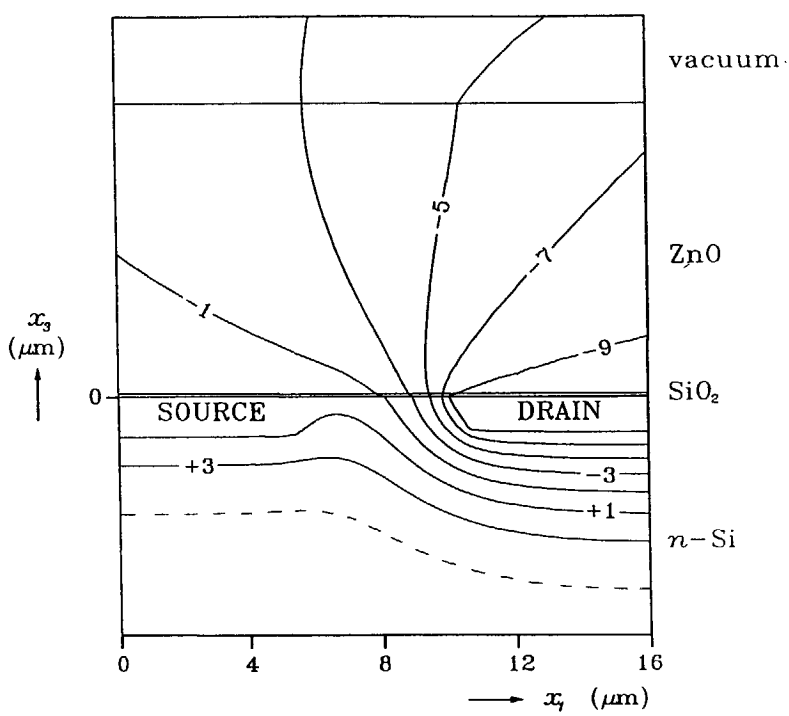


Figure 4.6: *Equipotential lines (V) in the gap region of the BMT.*

in front of the source is minimal at the silicon surface ($x_3 = 0$), and rises nearly linearly to the bulk potential $V_{BS} + V_{bi}$ when x_3 is decreased. When a barrier-injection process as expressed by Eq. 4.7 is assumed, it can be deduced that the current density in the gap decreases exponentially when moving from the silicon surface into the bulk. In Fig. 4.6, some equipotential lines around the gap are shown. This figure clearly shows the influence of the drain potential in the insulating area above the planar diode.

Next, the sensitivity of the device behavior for variations in the different parameters is considered. This is shown in Fig. 4.7. Since the flat-band

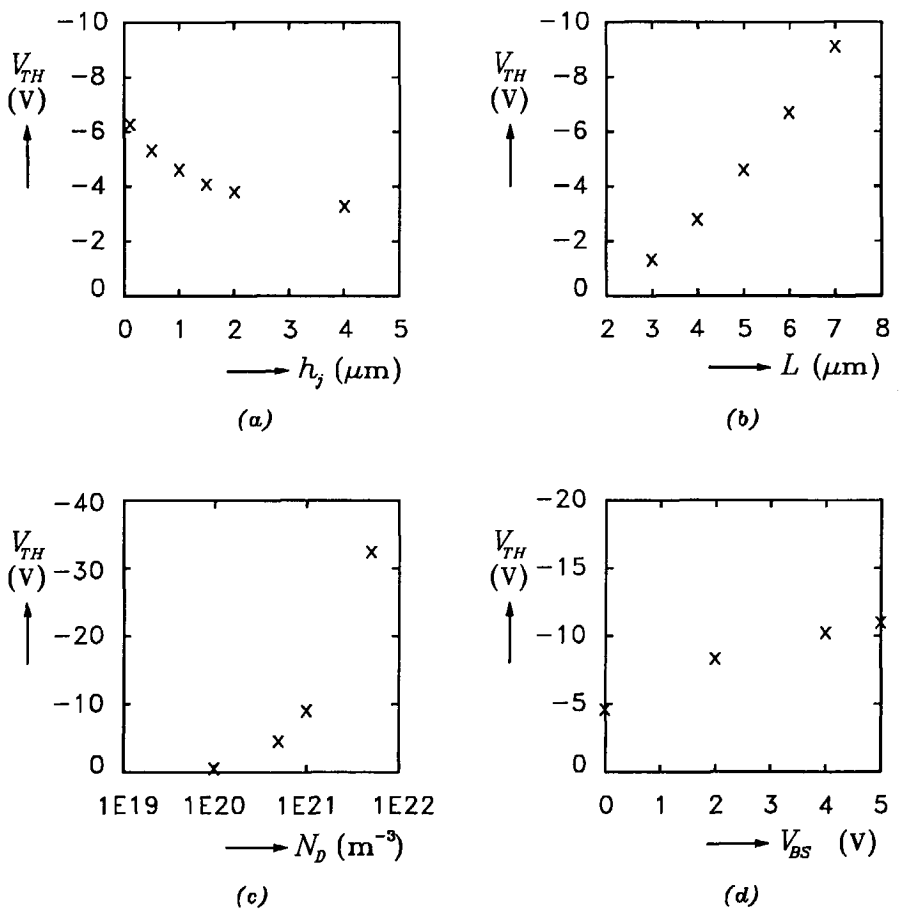


Figure 4.7: *Influence of junction depth h_j (a), of gap length L (b), of doping concentration N_D (c) and of bulk voltage V_{BS} (d) on the threshold voltage V_{TH}.*

voltage ignores SCL effects, whereas the RT voltage only gives information with respect to the depletion layer boundaries, a new threshold voltage V_{TH} is defined. The V_{TH} is defined as the drain voltage for which the potential barrier at $x_3 = 0$ has been reduced to half the built-in voltage: $V_{TH} = V_{DS}$ at $\psi_m(0) = 0.5V_{bi}$. For the given impurity concentration level, the injected hole density at $V_{DS} = V_{TH}$ is about five orders of magnitude below N_D, and can, therefore, be ignored. In Fig. 4.7 a to d the sensitivity of V_{TH} for variations in the junction depth h_j, the channel length L, the impurity concentration N_D, and the bulk voltage V_{BS} are given. The absolute accuracy in the calculations is 0.01 V. From Fig. 4.7 it can be deduced that the threshold voltage in the two-dimensional situation is strongly influenced by the conditions above and below the channel. The potential in the insulating space above the RT diode is mainly determined by the negative drain potential, see Fig. 4.6. As a result, the barrier at the silicon surface is pulled downward, thereby decreasing V_{TH}. However, this action is opposed by the bulk potential $V_{BS} + V_{bi}$ which is positive and tends to increase the potential barrier in the channel.

Once the potential distribution is obtained, the electric field distribution follows from the derivatives to x_1 and x_3. The lateral and normal electric field components E_1, E_3 at the silicon surface for the configuration of Fig. 4.5 are given in Fig. 4.8. Since the highest field strengths occur at this interface, it can be concluded from Fig. 4.8 that avalanche

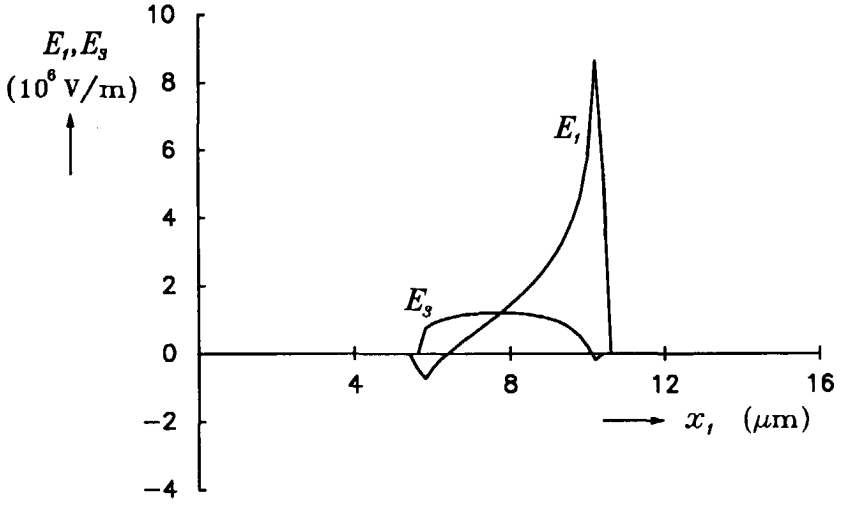


Figure 4.8: *Lateral (E_1) and normal (E_3) electric field distribution at SiO_2-Si interface in the gap.*

breakdown will not occur. In addition, it can be seen that the field in the major part of the channel is below the saturation field, which is about $E_s = 2 \cdot 10^6$ V/m [158]. For the geometries ($L \approx 3$–6 μm) and operating levels ($|V_{DS}| < 20$ V) of the devices discussed in this thesis, it is a good assumption to ignore the high-field part of the drift region, and to assume a constant hole mobility in the channel. Since the hole transport is concentrated at the silicon surface, the hole scattering at the surface must be taken into account, which results in a much lower mobility than the bulk mobility: $\mu_p \approx 0.021\,\mathrm{m}^2/\mathrm{Vs}$ [158]. The normal field E_3 in Fig. 4.8 is too low to affect the mobility seriously.

When the hole current density, which is injected at the SiO_2-Si interface, rises above the impurity level N_D, an inversion layer is created at the silicon surface and space-charge effects must be taken into account. Because of the increased amount of charge in the gap, the drain-induced barrier lowering is retarded, and SCL behavior must be expected. To simulate this effect in the computer model, Poisson's equation is extended by a current term $J_p/\epsilon_{Si}v_d$ similar to Eq. 4.9. An approximate solution is obtained by deriving J_p from Eq. 4.7, and using an average drift velocity of $-\mu_p V_{DS}/L$. The term $J_p/\epsilon_{Si}v_d$ is iteratively adjusted until a self-consistent solution is obtained. In Fig. 4.9a, the current density at the barrier ridge using the parameters of Fig. 4.5 is shown. This picture clearly shows the current crowding at the silicon surface, and the rapid decrease in current

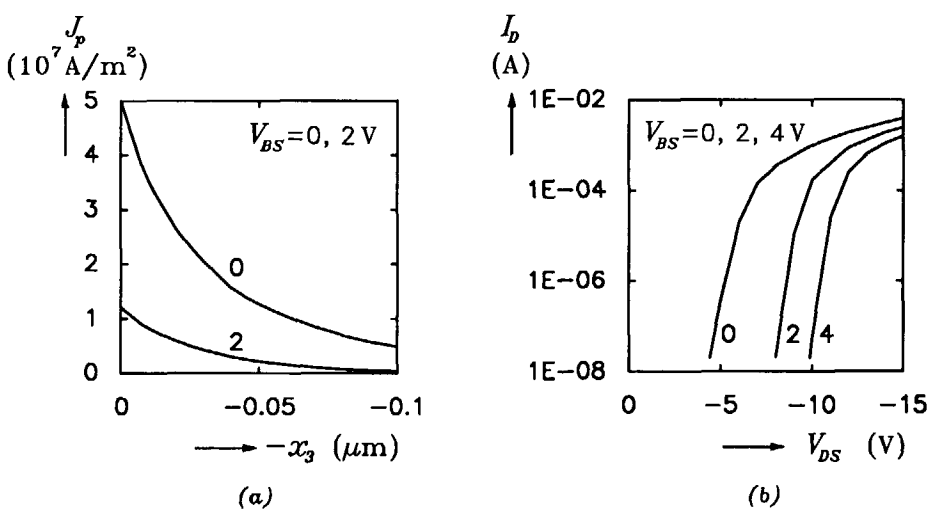


Figure 4.9: *(a) Current density vs. depth at barrier ridge; (b) simulated IV-relation with V_{BS} as parameter.*

density in the deeper parts of the gap. As a consequence, it can be expected that even for elongated channel widths SCL effects occur even at relatively low bias currents. The influence of V_{BS} is also shown: the back contact can be considered as a back gate, which modulates the current. If the total current is kept constant, the current density at the silicon surface rises when the back gate voltage V_{BS} is increased. In Fig. 4.9b, the IV–relationship is depicted when a channel width of $W = 1\,\text{mm}$ is assumed.

The configuration of the planar RT diode can, to a certain extent, be compared with a short-channel MOSFET operating in the subthreshold region. When the drain voltage is sufficiently large, punch-through occurs. However, because of the fixed potential of the gate ($|V_G| < V_{th}$) above the channel, the barrier is not minimal at the SiO_2-Si interface, but at some point below the surface. As a result, a saddle-shaped potential distribution is found, and carrier injection takes place in a buried channel [159]. The MOSFETs operating in this mode have triode-like characteristics because of the reduced output impedance [160, 161].

4.3 SAW DETECTION

4.3.1 Active Detection

When the potential distribution in the gap region of the planar RT diode is influenced by an external electric field, a change in the barrier-controlled injection current occurs. In this work, the SAW detecting capabilities of the RT diode are considered. Since the injection current in the planar structure is concentrated at the SiO_2-Si interface, a strong influence from the electric fields of the SAW can be expected. Because the SAWs only modulate the bias current in this Barrier-Modulated Tap (BMT), the device can be considered as an active detector as defined in Chapter 3.

In this section, the small-signal operation of the BMT is described. For low bias currents, the concentration of mobile carriers in the channel is small, and the SAW electric fields can freely penetrate into the gap. The SAW potential modulates the barrier height, which results in a modulation of the injection current. This is analogous to the variation of the emitter current in a bipolar junction transistor (BJT), which is induced by a modulation of the potential height of the emitter-base junction. For low bias currents, there are close formal similarities between the behavior of BMT and that of BJT. At higher current levels, more complex behavior occurs. The bias current becomes space-charge limited. Since the current injection is still assumed to be barrier controlled, in this range too

the modulation current can be derived from the variations in the barrier height. However, because the concentration of free carriers in the channel rises, the penetrating SAW fields are partly screened, and the SAW potential at the SiO_2-Si surface drops.

In the past, modulation of SCL currents in devices similar to the BMT were investigated. Wright introduced the SCL Surface-Channel Dielectric Triode [162], which is described theoretically in [163] and [164]. In Reference [165], experimental results are presented of a MOSFET operating in the triode region below the threshold level. However, in all cases, a gate is present on top of the channel, which keeps the surface potential constant. The small-signal behavior is described by using a gradual channel approximation, which results in a close relationship between the charge in the channel and the gate potential. In the RT device under consideration, no gate is present, and the potential above the channel is not constant. Since the field is mainly determined by the drain, a gradual channel approximation is not justified. A different theory was developed to describe the detection sensitivity of the BMT in the different current ranges.

In order to investigate the small-signal behavior of the BMT, the equivalent circuit model of Fig. 4.10 is proposed. Since the BMT is actually a

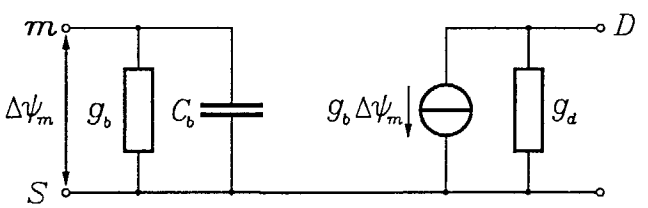


Figure 4.10: *Small-signal equivalent circuit of a SAW RT detector.*

two-terminal device, the node indicated by m is a fictitious point which represents the barrier maximum at the silicon surface. The injection region is modeled with a parallel connection of a conductance g_b and a capacitance C_b [139]. The transconductance g_b (S) can readily be obtained from Eq. 4.7

$$g_b = \frac{qI_D}{kT} \tag{4.13}$$

in which I_D represents the bias current. This transconductance is similar to the g_e of a BJT, and the sensitivity of the BMT is in a first-order approximation proportional to the bias current. In general, the RF current can be represented by $J_p = p\mu_p v_d$. In addition to a modulation in the

hole density p which is represented by g_b, a modulation in the velocity v_d must be considered. When a constant lateral AC field is assumed, the conductance which results from the velocity modulation is given by $g_v = \mu_p I_D/(x_m v_m)$ [140], in which x_m is the x_1-coordinate of the barrier maximum at the SiO_2-Si interface, and v_m is the injection velocity at this barrier maximum. For the devices presented in this work, g_v is about an order of magnitude smaller than g_b ($x_m \approx 0.3\,\mu$m, $v_m \approx 2 \cdot 10^4$ m/s) and is ignored. The capacitance C_b of the injection region consists of a static capacitance of about ϵ_{Si}/x_m (F/m^2), and a diffusion capacitance which represents the charge storage in the channel. Because of the negligible charge storage in the RT diode, the latter component can be ignored.

The feedback conductance g_d results from the drain-induced barrier modulation. The value of g_d depends on the bias current, and can be obtained from $\partial I_D/\partial V_{DS}$. In the RT range, there is a strong relationship between the drain and barrier potential. As a result, g_d rises sharply with increasing bias current. In the SCL range, the rise in g_d diminishes, and becomes linear if an unsaturated carrier velocity is assumed. Finally, the feedback conductance becomes constant for high current levels, where the carriers move at their scattering velocity. In this range, $1/g_d$ represents the SCL resistance of the drift region. As a consequence of this feedback conductance, the BMT behavior becomes triode like. The feedback capacitance represents the static capacitance of the depleted drift region, and can usually be ignored with respect to the total output capacitance C_d of the BMT, which is dominated by the depletion capacitance of the reverse-biased drain electrode.

From a physical point of view, it can be concluded that the reach-through detector has excellent high-frequency properties. Once the holes have crossed the barrier, they are pulled away by the strong drift field of the drain, and are hardly influenced by the modulating fields. Therefore, the effective transit time is determined by the injection region alone, and can be less than 0.1 ns. This should be compared with conventional Field-Effect transistors in which the transit time is determined by the entire channel length. The time constant τ_b determined by g_b and C_b was investigated by Sjölund [139] for the one-dimensional case, and is inversely proportional to I_D. Values of 0.1 ns and less were reported. The high-frequency properties of the BMT will, therefore, mainly be determined by the output capacitance at the drain.

The input signal at point m of the equivalent circuit is $\Delta\psi_m$, and represents the modulation of the barrier height. The determination of this

crucial potential is hindered by the presence of mobile carriers in the gap, and by the two-dimensional structure. For low bias currents, the mobile carriers can be ignored, and the potential modulation is determined by the geometric parameters L and h_j, and the depletion layer boundaries. In Fig. 4.11 the variation of the potential distribution in the silicon is shown. The finite-difference program described in the previous section is used, and the same conditions as in Fig. 4.5 are assumed. To simulate the modulation effect, the Equivalent-Surface-Charge method presented in Chapter 2 is applied. A fictitious surface charge of $7 \cdot 10^{-6}$ C/m^2 is placed at the ZnO-SiO_2 interface. It represents the equivalent surface charge of a SAW of 100 mW/m (see section 2.3). The charge has a cosine waveform with a period of 30 μm. Static conditions are assumed. In Fig. 4.12, the influence of the gap length L on the potential modulation (at $x_3 = 0$) in the center of the gap is depicted.

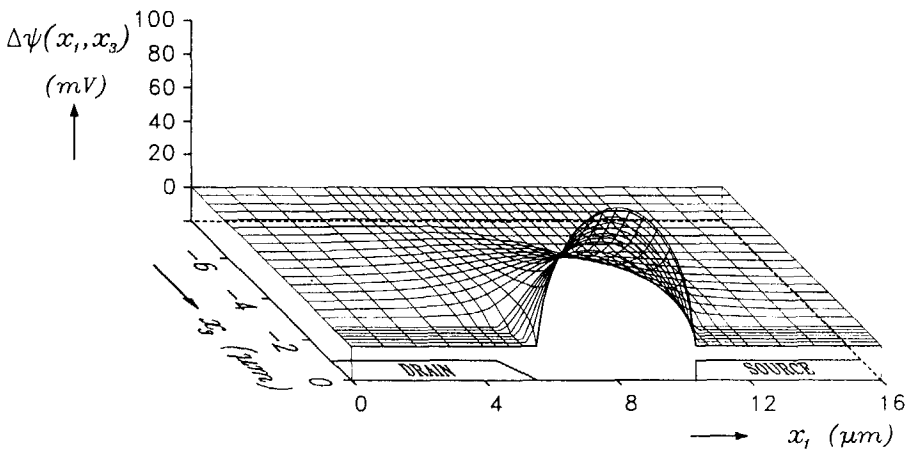


Figure 4.11: *Simulated potential modulation in the gap.*

From Fig. 4.11 it can be deduced that the location of the potential barrier is important. Fortunately, the region of the strongest modulation ($x_3 = 0$) corresponds to the largest current density. However, the x_1-coordinate of the potential barrier is also important. Since the modulation is strongest in the middle of the gap, $\Delta\psi_m$ is diminished when the barrier maximum moves towards the source at increasing bias currents. Two-dimensional simulations indicated that, indeed, the barrier maximum at the silicon surface shifts towards the source region when the drain voltage is increased. However, for higher drain voltages (in the SCL current range) the shift stabilizes ($x_m \approx 0.3\,\mu$m at the SiO_2-Si interface; $h_j = 1\,\mu$m).

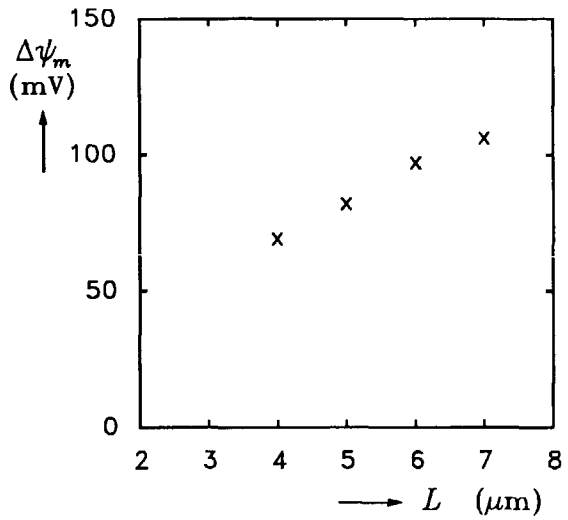


Figure 4.12: *Influence of L on the modulation potential.*

For devices operating in the SCL range, the x_1-coordinate of the barrier maximum is assumed constant, and its current dependence is ignored.

Of more importance is the influence of the mobile carriers on the penetrating SAW fields. In Chapter 2, it was shown that because of the screening action of the mobile carriers, the effective permittivity of the silicon experienced at the SiO_2-Si interface increases, and the small-signal potential decreases. In the next discussion, a similar method is used to describe the influence of the injection current on the modulation potential $\Delta\psi_m$. The layered structure presented in Fig. 2.1 is used. An equivalent surface charge ρ_s is assumed at the SiO_2-Si interface. Since the gap is usually much smaller than the SAW period, the surface charge is assumed to have no variation in the x_1-direction. In addition, the influence of the source and drain electrodes is ignored. This is, of course, a crude approximation, but enables us to use an analytical method. In the channel beneath the silicon surface, holes move at a constant injection velocity v_m. Since no variation in the x_1-direction is assumed, the small-signal potential variation ϕ, and hole density variation p_1, only depend on x_3. By using the current equation

$$J_{p,3} = p_0 q \mu_p E_3 - q D_p \frac{\partial p_1}{\partial x_3} \tag{4.14}$$

where p_0 is the stationary hole density in the channel, and by using the continuity equation and Poisson's equation, it can be derived that the

small-signal potential in the silicon becomes

$$\phi(x_3) = \phi(0) \exp\left(\frac{x_3}{L'_D}\right) \tag{4.15}$$

in which L'_D is given by

$$L'_D = \sqrt{\frac{\epsilon_{Si} D_p}{p_0 q \mu_p}} = \sqrt{\frac{\epsilon_{Si} k_B T}{q^2 p_0}} \tag{4.16}$$

and represents an effective Debye length which is determined by the local hole density p_0. In Eq. 4.16, the Einstein relation $D_p = \mu_p k_B T/q$ has been used. The surface charge ρ_s at $x_3 = 0$ induces a discontinuity in the electric displacement field

$$\rho_s = \lim_{x_3 \downarrow 0} D_3 - \lim_{x_3 \uparrow 0} D_3 \tag{4.17}$$

Because the potential is assumed zero far above the surface, and because the dielectric ZnO and SiO_2 layers are free of charge, the normal field above the $x_3 = 0$ plane can be ignored. Using Eqs. 4.15 to 4.17 the relationship between the potential $\phi(0)$ and ρ_s can be derived

$$\phi(0) = \sqrt{\frac{k_B T}{\epsilon_{Si} q^2}} \frac{\rho_s}{\sqrt{p_0}} \tag{4.18}$$

The stationary hole density p_0 is related to the bias current density J_0 through $p_0 = J_0/(q\mu_p v_m)$. As a result, $\phi(0)$ becomes inversely proportional to $\sqrt{J_0}$

$$\phi(0) = \sqrt{\frac{k_B T v_m}{\epsilon_{Si} q}} \frac{\rho_s}{\sqrt{J_0}} \tag{4.19}$$

The AC current, representing the detector current i_d, can be derived from the transconductance, and from the variations in the barrier potential. Although ϕ and J_0 depend on x_3, the current is concentrated at the silicon surface, and the channel at $x_3 = 0$ can be approximated by a shallow sheet, in which a constant current density and potential modulation which are independent of x_3 are assumed. In the RT current range, the concentration of mobile carriers is small. Screening can then be ignored, and $\Delta\psi_m$ is only dependent on ρ_s (section 2.3.2), and the geometric parameters L and h_j (see for example Fig. 4.11). The detector current is then proportional to the bias drain current I_D

$$i_d = \frac{q\xi_{RT}}{k_B T} I_D \tag{4.20}$$

In the SCL range, the modulating potential decreases as proposed in Eq. 4.19, and the detector current becomes

$$i_d = \xi_{SCL} \sqrt{\frac{q v_m}{\epsilon_{Si} k_B T}} \sqrt{I_D} \tag{4.21}$$

In Eqs. 4.20 and 4.21, the factors ξ_{RT} and ξ_{SCL} represent proportionality constants determined by ρ_s and by the influence of source and drain electrodes on the potential modulation. In both the RT and SCL range, the detector current depends on the bias current I_D, which shows the controlling action of the BMT.

It should be noted that in the derivation of the BMT sensitivity only the gap length L is of importance. The lengths of the source and drain electrodes are not related to the active SAW detection. Therefore, even at high frequencies their lengths can be chosen large in order to decrease the series resistances, without affecting the SAW detection process.

4.3.2 Passive Detection

In addition to the active detection mechanism described above, a passive detection occurs, which is caused by the capacitive coupling between the SAW and the source/drain electrodes of the BMT. These electrodes act as single-electrode detectors described in section 3.2.1. The source electrode is usually grounded, and here the passive coupling has little effect. However, at the drain side the passive detection seriously deteriorates the BMT performance, because: 1. the signals delivered by the passive and active detection mechanisms are usually not in phase, which results in an uncontrollable phase shift, and 2. the passive detection mechanism limits the control range of the BMT in the lower part. When the active detection is turned off by removing the bias current, the passive detection mechanism still gives a residual output signal.

The passive detection can be suppressed in two ways. Firstly, the drain electrode length can be designed to an integer times the SAW wavelength λ. In this case, the passive coupling is zero at the center frequency as indicated by Eq. 3.12. A more rigorous method is balancing, which is discussed in Chapter 6.

4.3.3 Secondary Effects

It was shown in section 4.2.2 that the current in the BMT is concentrated just below the silicon surface. Therefore, a strong interaction with the surface is expected. The surface influence on the hole velocity was already

incorporated in the mobility, which is typically half the bulk mobility. Another point of concern is the presence of surface states. There is an enhanced density of surface states, which is caused by the ZnO sputtering on top of the thin SiO_2 layer. In Chapter 2, it was mentioned that the surface states are transparent for the SAW fields because of the relatively small relaxation times. Therefore, an influence on the detecting current of the BMT is not to be expected. However, the surface states do affect the DC behavior of the device, and cause a shift in the *IV*-characteristics. Since the surface states usually represent an extra negative charge [166], a rise of the RT voltage is predicted. Because the RT voltage of the diode is not a very reproducible parameter (compare the collector-to-emitter voltage of a BJT), the BMT must be biased with a current. This biasing is compatible with the integrated-control mechanism as described in Eqs. 4.20 and 4.21.

Thus far, only a unilateral discussion, describing the effect of the propagating SAW on the charge carriers in the BMT channel has been presented. It was mentioned in section 2.4 that the wave–carrier interaction also affects the SAW itself. In particular, the SAW amplification effect is interesting, since the charge carriers in the BMT channel move with velocities greater than the SAW velocity. However, the interaction length is determined by the channel length L of the BMT, and is much smaller than a SAW wavelength. Since the amplification per wavelength is quite small [167], the SAW amplification in the BMT can be ignored.

4.4 EQUIVALENT CIRCUIT MODEL

In the previous sections, only a cross-sectional area of the BMT was considered, and the finite electrode and channel widths were ignored. In this section, the complete BMT is discussed. A top view of the complete device is given in Fig. 4.13a. The contacts to the p^+ electrodes are located at the ends of the electrodes, outside the SAW propagation path. The source and drain in the BMT are junction electrodes, and must be represented by distributed RC networks. In the following, an equivalent circuit model of the BMT is presented using lumped network elements. This model is not only required to investigate the influence of the electrode geometries on the DC and AC behavior, but also to include the effects of peripheral electronic circuitry.

The structure of Fig. 4.13a is divided into n identical sections. The sections are connected by series resistances R_s, which are determined by the sheet resistivity of the implanted p^+ electrodes. In addition, diodes

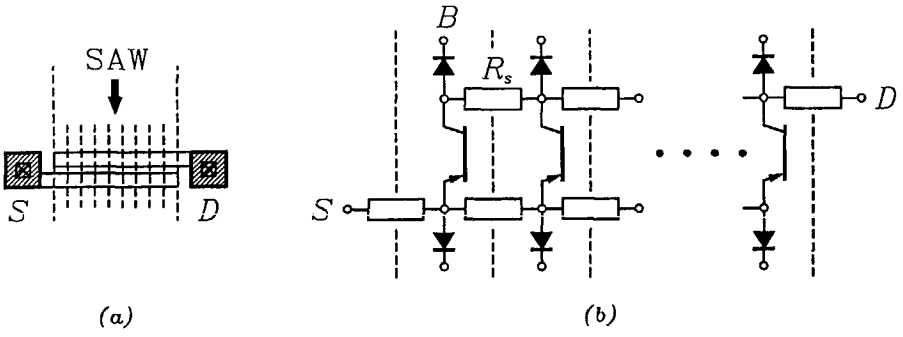


Figure 4.13: *Top view (a) and equivalent circuit model (b) of a BMT.*

are added to simulate the vertical *pn* junctions between the source/drain electrodes and the *n*-layer. Since these junctions are reversely biased, they hardly affect the DC bias; however, they add to the electrode capacitance caused by the depletion layer capacitance below the electrodes. The equivalent circuit of Fig. 4.13a is depicted in Fig. 4.13b.

The DC and AC characteristics of one section correspond to the triode-like characteristics of the BMT described earlier. The equivalent model used for one section is shown in Fig. 4.14. The coupling capacitance C_c

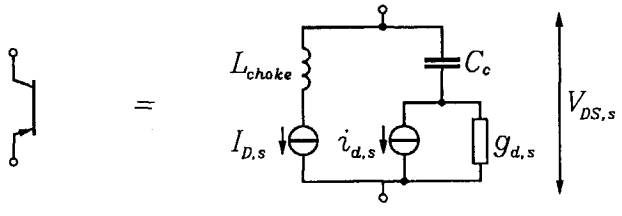


Figure 4.14: *Internal circuit model of a single section.*

and choke coil L_{choke} are inserted to separate the AC and DC parts of the model. Proper values are chosen in order to avoid any influence on the device operation. Since the RT devices discussed in this work mainly operate in the SCL current range, the DC current of a single section $I_{D,s}$ is approximated by

$$I_{D,s} = c_1(V_{DS,s} - V_0)^2 \tag{4.22}$$

where c_1 (A/V^2) is a constant, $V_{DS,s}$ the voltage drop across one BMT section, and V_0 the threshold voltage related to the SCL current and is close to V_{TH}. In the Mott-Gurney law, a value for c_1 is given [147]

$$c_1 = \frac{9\mu_p \epsilon_{Si}}{8L^3} A$$

in which A is the cross-sectional area of the current path. In the two-dimensional RT diode, such a derivation cannot be made, and, therefore, c_1 must be determined experimentally. For the small-signal current $i_{d,s}$ of one section, Eq. 4.21 is used

$$i_{d,s} = c_2 \sqrt{I_{D,s}} \tag{4.23}$$

The constant c_2 ($\sqrt{\text{A}}$) depends on ρ_s (see Eq. 4.21). Finally, the feedback conductance $g_{d,s}$ in a section is caused by the influence of the drain potential on the barrier height and is derived from Eq. 4.22

$$g_{d,s} = \frac{dI_{D,s}}{dV_{DS,s}} = 2c_1(V_{DS,s} - V_0) = 2\sqrt{c_1 I_{D,s}} \tag{4.24}$$

Because $g_{d,s}$ is relatively large, which yields to the triode behavior of the BMT, the signal loss caused by the loading of the ladder network by $g_{d,s}$ can severely decrease the output signal. The complete model, including the sectional structure of Fig. 4.14 and the ladder structure of Fig. 4.13b, was implemented in the circuit simulator SPICE [168].

Next, some circuit simulation results are presented. Firstly, the influence of the finite electrode resistance on the DC current is considered. Since the RC ladder structure is loaded by the RT sections, there is a gradual potential drop along the electrodes, causing a nonuniform channel current. In Fig. 4.15a, the currents through 10 sections are depicted for $R_s = 0$ (dashed line), and $R_s = 30, 300\,\Omega$. The following parameters were used: $V_0 = -5\,\text{V}$, $c_1 = 1 \cdot 10^{-5}\,\text{A/V}^2$. This picture gives an indication of the current distribution along the channel width. For increasing R_s, the current rises at the ends of the electrodes. Next, the R_s influence on the AC detector current i_d is considered. Therefore, both the source and drain contacts are AC grounded. The AC short-circuit current vs. the total bias current I_D is shown in Fig. 4.15b for several R_s values.

The circuit model presented in this section can be extended by the addition of other network components which, for example, represent a measurement set-up. In the next section, the model is used to compare the experimental results with theory.

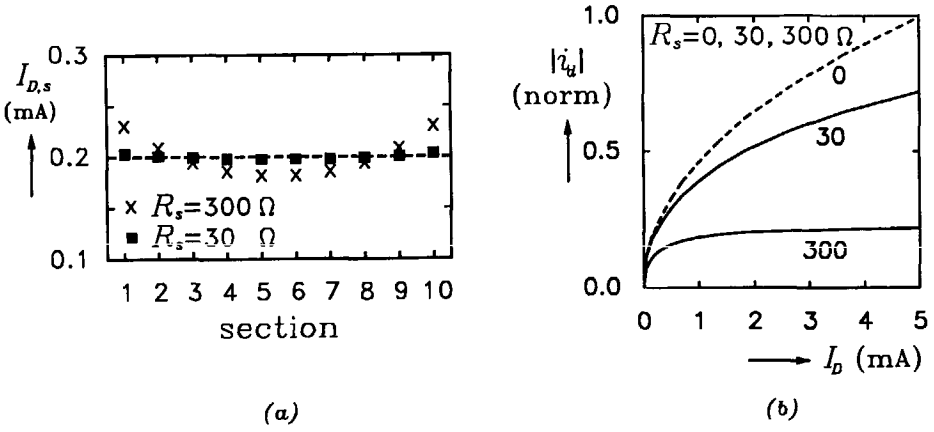


Figure 4.15: *Simulated effect of R_s on (a) the current distribution among sections, and (b) the RF detector current.*

4.5 FABRICATION TECHNOLOGY

To verify the BMT theory, test devices were fabricated. In order to integrate driving and loading circuitry together with the BMTs in future filter structures, an n^--type epitaxial layer grown on a p^--type substrate is used for the foundation of the BMTs. As a result, an extra pn junction beneath the BMT is introduced, and the possibility of a vertical reach-through from the source or drain electrodes to the substrate must be taken into account. Proper device dimensions, doping levels and bias conditions can prevent the vertical RT. In the following discussion, the device fabrication and process sequences are considered. Standard IC processes are applied.

(i) Substrate

All devices are fabricated on 2-inch silicon wafers. A (100) p^--type substrate with a conductivity of 3–5 S/m is used as a starting material. This resistivity corresponds to an impurity concentration N_B of $4\text{–}6 \cdot 10^{20}$ m^{-3}.

In this p^--type substrate, n^+pn^+ BMTs can directly be created by employing n^+ electrodes. However, the lateral RT operation in this type of devices is severely hindered by the interface and oxide charges described in section 2.6.1. These charges cause a surface inversion on p^--type substrates, which results in a short-circuiting of the n^+ electrodes. With an extra donor implantation compensation of the charges is feasible [166].

However, no such attempts were made in this work. The devices presented here use an n^--type epilayer to make p^+np^+ BMTs.

(ii) Epilayer

The voltage levels of the vertical and lateral RT operations are, to a large extent, determined by the epilayer doping concentration and thickness. The doping concentration N_E must be sufficiently low in order to obtain practical lateral RT voltages for BMT channel lengths in the range of 4–6 μm. With an impurity concentration of $5\text{–}6{\cdot}10^{20}\,\mathrm{m}^{-3}$ (about 10 S/m), reproducible devices can be obtained with operating voltages in the range of 0–20 V. The epilayer thickness h_{epi} should be chosen as large as possible, in order to increase the vertical RT voltages. On the other hand, the thickness is limited by the requirements set by the electronic circuitry. In particular, the p isolation diffusion must be deep enough to reach the substrate, and the collector resistance of a common vertical npn transistors should remain at an acceptable level. The epilayer thickness of the ultimate devices is about 7 μm, which was verified by RT measurements between a metal contact at the epi surface and the substrate.

Thinner epilayers can be obtained by using a buried n^+ layer (BN) underneath the p^+ electrodes. However, an exact alignment of the BN regions with respect to the BMT channel is hindered by lateral out-diffusion and pattern shifting [169]. In the high resistivity epilayer, autodoping effects seriously affect the epilayer concentration, and h_{epi} must be sufficiently thick to prevent an increased doping level in the BMT channel region. In addition, a rise of the leakage currents must be expected because of the increased number of defects.

(iii) Silicon-dioxide layer

After the growth of the epilayer, a 2 μm thick SiO_2 layer is thermally grown (wet oxidation, 1200 °C for 320 min., 90 min. cool-down to 800°, oxygen). As a result of this oxidation, the epilayer thickness is reduced by about 1 μm. The oxide layer of 2 μm thickness is only required beneath the SAW generating transducers, as is discussed in Chapter 6. For the acoustoelectric interactions in the BMT, this oxide thickness is far too large (see Fig. 3.9). Therefore, all SiO_2 outside the regions intended for the SAW transducers is etched away, and a new thin SiO_2 layer of 0.1 μm thickness is thermally grown (dry oxidation, 1000 °C for 160 min., 30 min. cool-down to 900°, nitrogen).

(iv) Implantation of p^+ electrodes

The p^+ source and drain electrodes of the BMT are created by an implantation of BF_2^+ ions. To prevent any topological discontinuities at the electrode edges, the ions are shot through the thin SiO_2 layer of 0.1 μm. A photoresist layer is used for masking. The oxide reduces the amount of channeling, which would cause an implantation tail below the p^+ regions, and thus a reduction of the vertical RT voltage. A proper implantation energy must be chosen in order to get the implantation profile maximum close to the SiO_2-Si interface. For the desired projected range of 0.1 μm ($= h_{ox}$), an implantation energy of 150 keV is required [170]. An implantation dose of $5 \cdot 10^{19}$ ions/m^2 is used. After the implantation, the wafers are annealed at 1050 °C for 30 minutes in nitrogen.

With the process simulator SUPREM [171], a junction depth of 1 μm and a sheet resistivity of 28 $\Omega/\square$ are predicted. For the profile maximum, a doping concentration of 10^{26} m^{-3} is given. Since the actual impinging energy of the B^+ ion is about 23 % of the energy of the BF_2^+ ion, an implantation energy of 35 keV has been used in the simulations. It should be mentioned here that channeling is not included in these simulations. The simulated junction depth of 1 μm agrees well with measurement results, which have been obtained by determining h_{epi} using a Schottky diode and the p^+n diode and subtracting the results afterwards. The measured sheet resistivity of the p^+ electrodes is $30 \pm 2\,\Omega/\square$.

After the removal of the resist, a flat surface above the BMT remains. Step measurements using a Tencor alpha-step 200 and observations through a scanning electron microscope showed that this, indeed, is the case. In order to obtain a pure Rayleigh-wave propagation in this (100) system, a SAW propagation direction on the [001] axis is required. Therefore, the p^+ electrodes are aligned on the wafer flat.

(v) Metallization

After etching away the oxide above the contact holes, a 0.3 μm thick aluminum layer is deposited by vacuum evaporation. Wet etching is employed to obtain the interconnection patterns, the bonding pads and the SAW generating transducers. The annealing is postponed until the ZnO sputter process.

(vi) ZnO deposition

The final fabrication step is the ZnO deposition. The piezoelectric ZnO layers are deposited with a DC S-gun magnetron sputter unit (Varian, 3119 R & D). This system is described in more detail in [172]. In this work, a fixed set of sputter parameters is used, as listed in Table 4.1. With these parameters high-quality piezoelectric films are obtained on

Table 4.1: *ZnO DC magnetron sputter conditions.*

Target composition	Zn
Sputtering gas	100 % O_2
Sputtering gas pressure	1 Pa
Substrate heater temperature	400 °C
Target-to-substrate distance	9 cm
DC power	1.5 kW
Deposition rate	6 μm/h

SiO_2-Si substrates with a SiO_2 thickness larger than 0.5 μm. However, the ZnO film on the thin (0.1 μm) SiO_2 regions is hazier, and has a less regular grain structure than the ZnO film on the thick (2 μm) oxide regions. The quality of the ZnO on the different regions is further evaluated in Chapter 6. It is believed that by changing the sputter conditions high-quality films can also be obtained on the thin SiO_2 regions. This shall be the subject of future research. ZnO layer thicknesses between 5 and 15 μm have been fabricated.

A summary of the fabrication process is given in Table 4.2. The initial epilayer thickness of 8 μm is reduced to a final thickness of 7 μm as a result of the thermal oxidation steps. In addition to the steps mentioned above, a standard p-isolation diffusion which reaches into the substrate, and an n^+-diffusion to contact the epilayer are shown. These steps are not critical for the BMT operation. A photograph of the fabricated chip (measuring 10 × 10 mm) is shown in Fig. 4.16. The photograph was taken before the ZnO deposition. The upper part contains a SAW delay line with test devices, whereas the lower part contains a complete, monolithic PTDL using BMTs. The fabricated chips were mounted in 18-pins dual-in-line IC packages. A conductive silver in methyl-isobutyl-ketane glue (Electrodag 1415 from Acheson) was used to bond the die to the package. An acoustic absorbing material (Rhodorsil Silicones CAF4 from Rhône-Poulenc) was placed at the ends of the acoustic propagation paths in order to prevent edge reflections.

Table 4.2: *BMT processing scheme.*

substrate	(100) p-type, 3–5 S/m
epitaxial layer	n-type, 8 μm, 10 S/m
oxide growth	thermal oxidation, 2 μm
p–diffusion	boron diffusion
n–diffusion	phosphorus diffusion
oxide etch	at regions for BMTs
p^+ implantation	BF_2^+ implantation, 150 keV, $5 \cdot 10^{19}$ ions/m^2
anneal	1050 °C, 30 min.
oxide etch	contact windows
Al evaporation	0.3 μm, interconnect
ZnO deposition	see Table 4.1

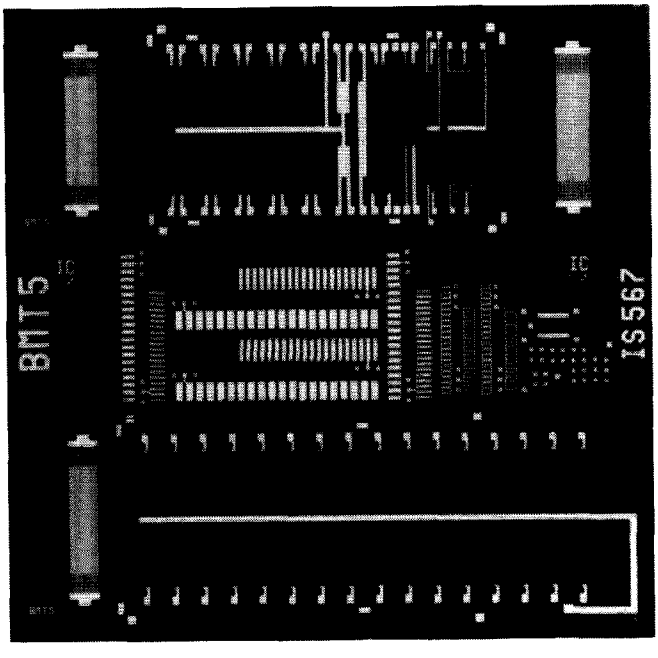


Figure 4.16: *Photograph of the fabricated chip, measuring 10 × 10 mm. The ZnO layer is not yet deposited.*

4.6 EXPERIMENTAL RESULTS

4.6.1 DC Measurements

The DC measurements were performed on a parameter analyzer (type HP 4125A). The addition of the extra p^- substrate underneath the BMT complicates the DC operation, and may lead to parasitic currents from the p^+ electrodes to the substrate, or, when the substrate is floating, can cause a RT current from source to drain via the substrate. In the latter case, the lateral RT operation is hindered, and the SAW detecting capabilities are deteriorated. In the following, the reach-through operation of the parasitic, vertical p^+np^- RT diodes is considered first. Then the lateral DC operation is described. In all measurements, the source is fixed at 0 V and is RF grounded.

(i) Vertical reach-through

In this part, the vertical RT between a p^+ (source or drain) electrode to the substrate is examined. Because the doping levels of the p^+ electrodes and the p^- substrate differ largely, the RT operation of the vertical diode is not symmetric. When the p^+ electrode acts as the source, it can be derived that the flat-band voltage is given by [173]

$$V_{FB} = \frac{q}{2\epsilon_{Si}}(h_{epi} - h_j)^2 N_E^2 \left(\frac{1}{N_E} + \frac{1}{N_B}\right) - V_{biB} + V_{biT} \qquad (4.25)$$

in which h_{epi} is the epilayer thickness, h_j is the p^+ junction depth, and N_E,N_B are the doping concentrations of the epilayer and substrate, respectively. The voltages V_{biT}, V_{biB} are the built-in voltages at the p^+ – epi and epi – substrate junctions, respectively. Low doping concentrations in the epilayer and the substrate, and a wide distance between the p^+ electrode and the substrate, are desirable. When the p^+ electrode acts as the drain, V_{biT} and V_{biB} must be exchanged, and N_B must be replaced by the doping concentration of the p^+ regions N_T. This results in a much lower V_{FB}, because $N_T \gg N_B$. For the RT from substrate to drain, the low substrate doping has no advantages.

The asymmetric behavior of the vertical RT diode is shown in the measured IV-characteristics of Fig. 4.17, which gives the drain current I_D vs. the voltage across the p^+-electrode and the substrate, $|V_{BS}|$. In curve (1), the p^+ electrode acts as the drain (electrode dimensions: $800 \times 64\ \mu$m). The depletion region around the drain is completely located in the epilayer, and the RT voltage is fixed by the epilayer doping N_E and the epilayer

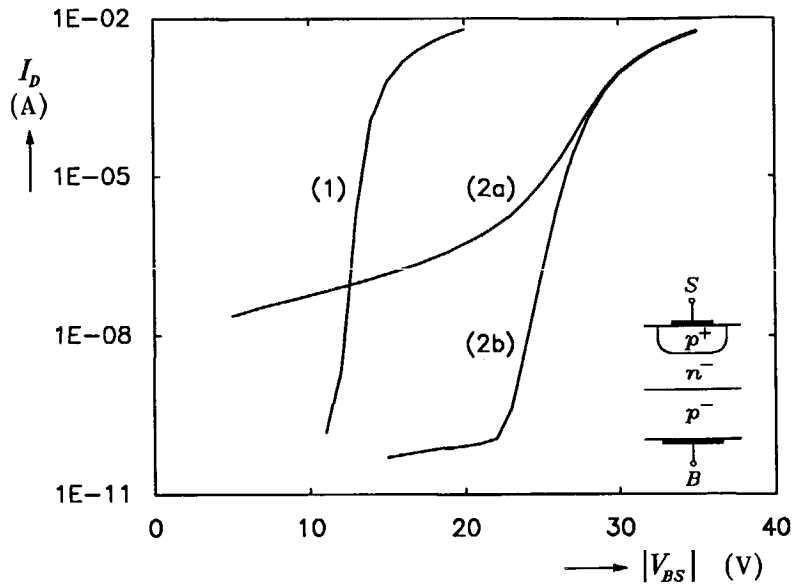


Figure 4.17: *Vertical RT characteristics with* (1) *injection by substrate,* (2a) *injection by* p^+ *electrode with epilayer floating and* (2b) $V_{ES} = 0\,\mathrm{V}$.

thickness beneath the p^+ region. The location of the curve corresponds to the one-dimensional theory (see Eq. 4.3). The epi-to-source voltage V_{ES} has no influence on curve (1). The saturation of the IV-characteristic at higher current levels is believed to be caused by the series resistance of the substrate rather than by SCL effects. When the source and drain connections are exchanged, curve (2) results. In this case, the p^- substrate acts as the drain. Since the substrate has a low doping level, the depletion region around the epi–substrate junction stretches out both in the epilayer and the substrate. Therefore, the RT voltage is much larger than in the previous case. By using Eq. 4.25, and noting that the epilayer and substrate doping levels are approximately equal, a doubling of the RT voltage is predicted. This is confirmed by the measurements. In contrast to the previous case, the epi voltage in this case strongly influences the RT operation. In curve (2a) the epilayer is floating, whereas in curve (2b) $V_{ES} = 0\,\mathrm{V}$. At a further increase of V_{ES}, the p^+ – epi junction is reversely biased, but no significant change in the DC operation is observed. The influence of V_{ES} can be understood by considering the p^+np^- combination as a transistor with a large collector area consisting of the large epi–substrate junction, and a highly doped p^+ emitter.

From the measurements presented in Fig. 4.17, the limitations on the

drain voltage of the lateral RT diode can be derived. If the substrate floats, a RT from one p^+ electrode to another p^+ electrode via the substrate occurs if the voltage across the electrodes is larger than about 34 V. If the substrate must be fixed at a constant voltage V_{BS}, then

$V_{BS} > -22\,\mathrm{V}$ to prevent a RT between the substrate and the source p^+ electrode of the BMT.

$V_{BS} < 12\,\mathrm{V} + V_{DS}$ to prevent a RT between the substrate and the drain p^+ electrode of the BMT.

(ii) Lateral reach-through

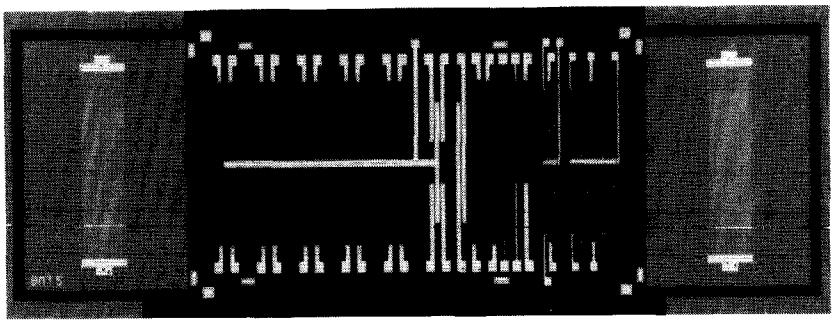
An important design parameter of the lateral RT diode is its gap length L. Devices have been fabricated with lengths in the range of 4–12 μm. However, for gap lengths longer than 6 μm, the variation in the RT voltages increases, and the general operating voltages increase ($> 30\,\mathrm{V}$), which results in a high power dissipation at the desired current levels. In addition, a large influence from the substrate is observed. For gap lengths below 6 μm reproducible results are obtained. For comparison, the operating voltages for the devices with gap lengths L of 4, 5 and 6 μm are shown in Table 4.3. These voltages have been measured under the condition of

Table 4.3: *BMT operation voltages.*

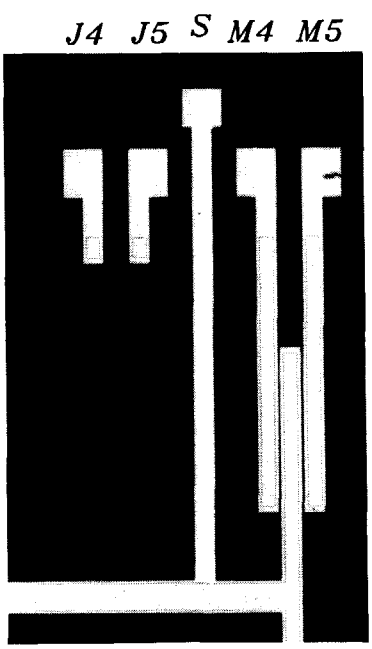
L	V_{DS}
4	5 ± 1
5	12 ± 1
6	21 ± 2

a floating substrate, $V_{ES} = 0\,\mathrm{V}$ and for a fixed current per unit width of 0.2 A/m. Although good results have been obtained with the 6 μm devices, their operating voltages are rather high, and at higher current levels a RT via the substrate cannot be prevented. Therefore, the results presented in this work are restricted to the 4 and 5 μm devices.

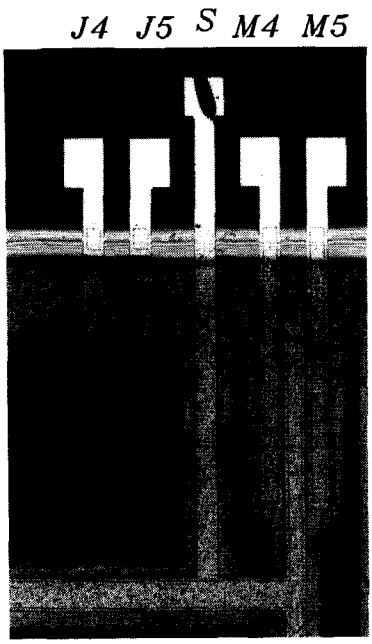
Four different devices are compared: $J4$ and $J5$ with only junction electrodes and gap lengths of 4 and 5 μm, respectively, and $M4$ and $M5$ in which the p^+ junction electrodes are covered with and contacted by metal electrodes. In the latter case, the influence of the p^+ series resistance vanishes. The upper part of the chip, which contains the test BMTs, is depicted Fig. 4.18a (no ZnO present yet). Figures 4.18 b and c give more detail. Note that for the junction BMTs $J4$, $J5$, no metal parts are



(a)



(b)



(c)

Figure 4.18: *(a) Photograph of the test chip part, and detailed views of the junction (J4, J5) and metal (M4, M5) BMTs in (b) and (c), without and with the ZnO layer, respectively.*

present in the SAW propagation path. The junction electrodes themselves are not discernable. In Fig. 4.18c, the BMTs are covered with a ZnO film of 8 μm thickness. The differences in the grain structure of the ZnO film above the junction and the metal BMTs are clearly discernable. The BMTs are connected to a common source bar. The electrode lengths (measured in the propagation direction) are 64 μm, and the aperture (or electrode overlap) W is 500 μm. Since the distance between the individual BMTs is usually much larger than the gap lengths L, lateral RT currents between different devices do not occur, and no isolation diffusions are required. This is advantageous when the BMTs are used in an array as in the PTDL. The devices are measured successively by applying a negative voltage on one of the drain contacts.

The measured relationship between the drain current I_D and the drain-to-source voltage V_{DS} is depicted in Fig. 4.19 for a floating substrate and $V_{ES} = 0$ V. At low currents, the results of the junction and metal devices are identical. More insight into the IV–relationship is obtained by measuring the output conductance dI_D/dV_{DS}. This option is available on the applied parameter analyzer, and the results are shown in Fig. 4.20. From the linear relationship of dI_D/dV_{DS} vs. V_{DS} for $M4$ and $M5$, it can be derived that in the operating range under consideration the IV–relation is quadratic. It can, therefore, be concluded that the current is space-charge limited and follows the Mott-Gurney law. The deviations in $J4$ and $J5$ from the linear relationship of dI_D/dV_{DS} are caused by the series resistance of the p^+ electrodes.

To compare the measurements with theory, the equivalent circuit model described in section 4.4 is applied. For the devices under consideration, 8 sections are used. Each section represents an electrode part of 64 μm in width. Since the electrode lengths of the source and drain electrodes are also 64 μm, the resistance R_s equals the p^+ sheet resistance of 30 Ω. For $M4$, $M5$ the series resistances vanish. From the measurements of $M4$ and $M5$ in Fig. 4.20, the threshold voltage V_0, and the constant c_1 of a section can be derived

M4: $V_0 = -4.5$ V $\quad c_1 = 8 \cdot 10^{-6}$ A/V^2
M5: $V_0 = -12.5$ V $\quad c_1 = 5 \cdot 10^{-6}$ A/V^2

These parameters have been implemented in the circuit model. However, for the junction devices $J4$ and $J5$, a better match with the experimental data is obtained when the threshold voltages are lowered by 1.5 V

J4: $V_0 = -6$ V $\quad c_1 = 8 \cdot 10^{-6}$ A/V^2
J5: $V_0 = -14$ V $\quad c_1 = 5 \cdot 10^{-6}$ A/V^2

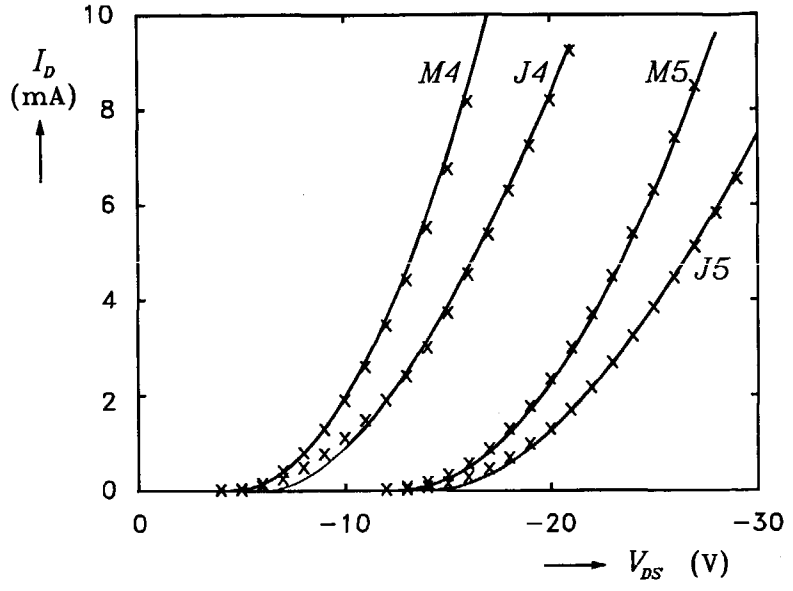


Figure 4.19: *Experimental IV–relations of the junction and metal BMTs with gap lengths of 4 and 5 μm.*

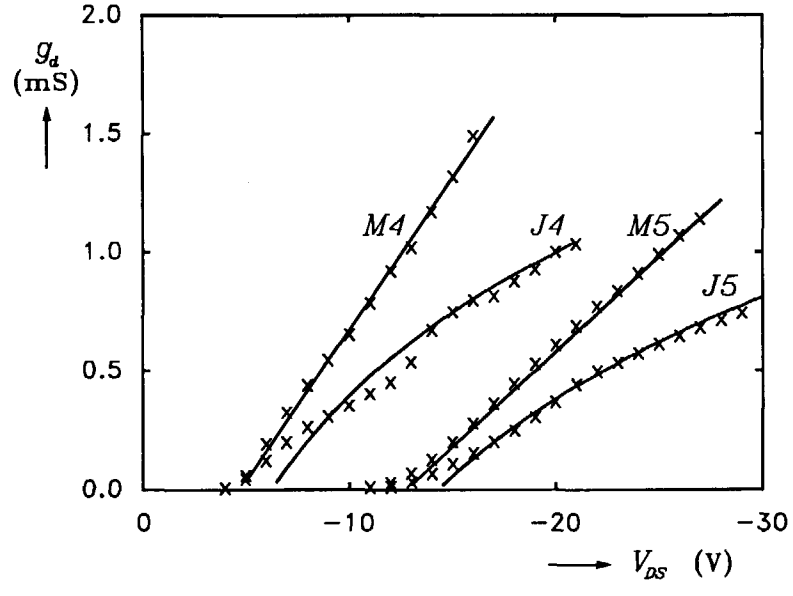


Figure 4.20: *DC output conductance of the junction and metal BMTs with gap lengths of 4 and 5 μm.*

In Fig. 4.19 and 4.20 the solid lines represent the simulation results using the above mentioned parameters. A good agreement between the model and experimental data is observed.

In the previous measurements, the V_{ES} was fixed at 0 V. Experiments with a floating epilayer gave no significant deviation in the results. However, by increasing the epi-to-source voltage, the barrier in the gap rises, and a strong influence in the lower current range is observed, see Fig. 4.21. In the SCL current range, no significant changes are observed.

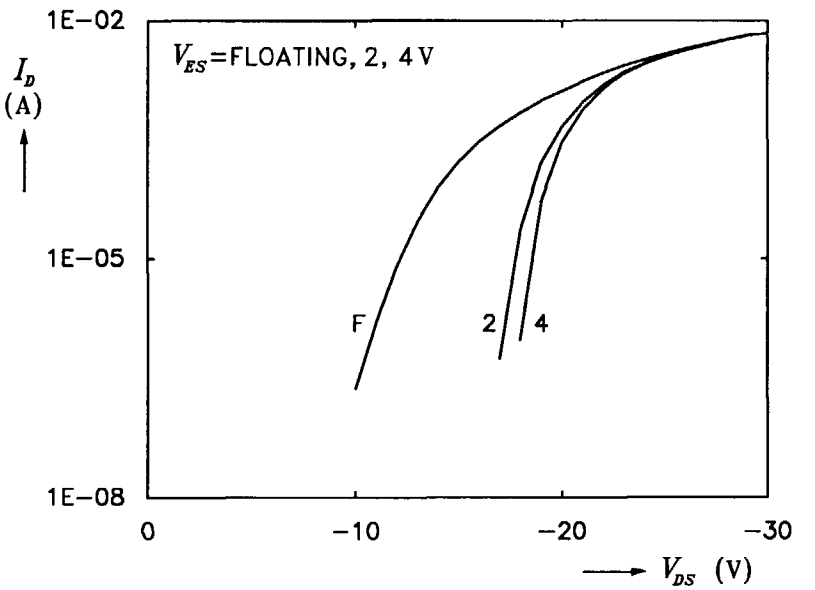


Figure 4.21: *Influence of V_{epi} on the lateral RT characteristic.*

4.6.2 RF Measurements

This section describes the experiments which confirm the SAW detection capabilities of the BMTs. The measurements are performed on a HP 8753A network analyzer, which has a Fast-Fourier-Transform option to map the results from the frequency domain into the time domain and vice versa. The SAWs are generated by a conventional metal IDT of 16 finger pairs with a period of 32 μm and an aperture of 1.7 mm. With the

8 μm thick ZnO layer, this IDT has a (–4 dB) bandwidth of about 5 MHz and a center frequency of 94.5 MHz. Two such transducers are used to make a delay line as shown in Fig. 4.18a. In the propagation path between the IDTs, the BMTs are present. The electric power delivered to the transmitting IDT is 0.5 mW. From insertion loss measurements on the untuned delay line, the SAW power per unit width is estimated to be 0.7 mW/m.

In section 4.3, it was mentioned that the output of the BMT consists both of an active and a passive response. These responses can be separated by the use of reciprocity. Since the reciprocity relations are valid only for the passive mechanism, no change in the passive response is observed when the input and output ports of the RF measurement set-up are exchanged. A measurement method was developed to exploit this difference in the detection mechanisms. Firstly, the response from the BMT to the IDT is measured. In this measurement, the BMT launches the SAWs, and only the passive transduction mechanism is involved. Then the RF terminals are exchanged and the BMT acts as a detector, in which case both the passive and active transduction mechanisms are involved. By subtracting the two measurements, the response of the active detection mechanism remains. On the network analyzer mentioned above, an option is available which performs a vector subtraction on the complex data. The responses are time gated to eliminate RF feedthrough and other spurious signals, such as bulk waves and reflected waves from the other IDT. A sweep-to-sweep averaging over 10 sweeps is applied to reduce the receiver noise level to –110 dBm.

For the RF measurements, the BMTs are biased with a constant current. The load impedance is the 50 Ω input impedance of the network analyzer. The RF detector current i_d through the load impedance is measured at 94.5 MHz as a function of the biased drain current I_D. In Fig. 4.22a the active detection responses of $J4$ and $J5$ are shown. The responses rise sharply at lower bias currents, but saturate in the higher current range, which was predicted by the theory discussed in section 4.3.1. By varying the bias current between 0 and 5 mA, a control range of more than 25 dB is readily obtained. In Fig. 4.22b the phase responses are shown, which are quite flat. The solid lines in Fig. 4.22a represent the simulation results of the equivalent circuit model. The parameters used are

J4: $V_0 = -6$ V $\quad c_1 = 5.5 \cdot 10^{-5}$ A/V^2 $\quad c_2 = 4.2 \cdot 10^{-6}$
J5: $V_0 = -14$ V $\quad c_1 = 2.5 \cdot 10^{-5}$ A/V^2 $\quad c_2 = 4.2 \cdot 10^{-6}$

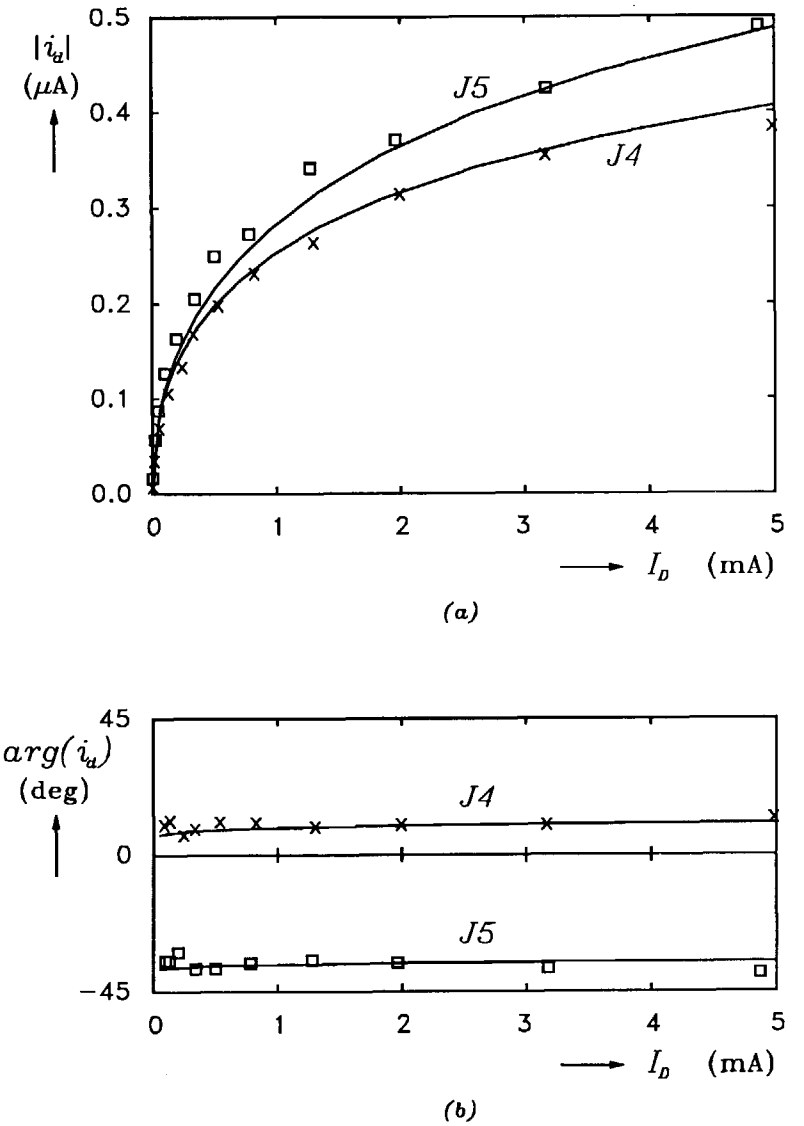


Figure 4.22: *Amplitude (a) and phase (b) responses of the 4 and 5 μm junction BMTs.*

The c_1 values are 5 to 6 times higher than used for the DC responses. These values are obtained from impedance measurements at 100 MHz on the BMT drain contacts of $M4$ and $M5$. In the model, these higher values approximate the experimental results more closely than the values obtained from the DC measurements. For the junction BMT $J5$, the detector current is about 0.5 μA at $I_D = 5$ mA. With an incident SAW power of about 0.35 μW at the 500 μm wide BMT, this corresponds to an untuned power conversion efficiency CE_p of –47 dB on 50 Ω. By matching the output with a complex load, this efficiency can be increased to –39 dB. Using Eq. 3.5 a current conversion efficiency CE_i of –64 dB is derived. The rather low efficiency can be attributed to the state of the ZnO. In the thin SiO_2 regions where the BMTs are located, the quality is not high, which can be concluded from the irregular texture as shown in Fig. 4.18c. In addition, the ZnO layer thickness of 8 μm corresponds to $\frac{2}{3}$ of the optimal value of 12 μm which is required for the optimal coupling at $\omega h_{ZnO} = 8000$ rad m/s. More about the ZnO state can be found in Chapter 6.

In Fig. 4.23a the influence of the electrode resistance is shown. Because of the different ZnO growing conditions around the metal electrodes, a quantitative comparison between $J5$ and $M5$ cannot be made. Therefore, the experimental data in Fig. 4.23 are normalized. Again the simulation results obtained with the equivalent circuit model are indicated by the solid lines. In Fig. 4.23b the influence of the epi voltage V_{ES} is shown. It is seen that for a fixed bias current, the detector current i_d is reduced when the epi voltage rises. When V_{ES} rises, the current density in the channel

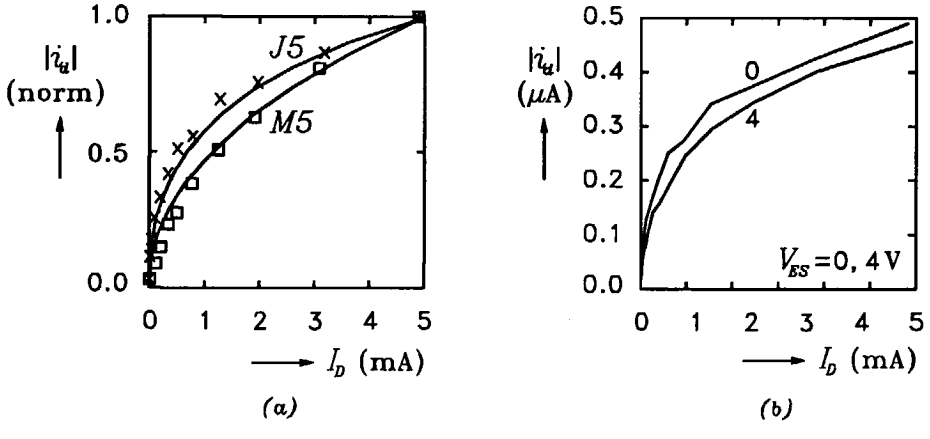


Figure 4.23: *Influence of electrode resistance (a) and epi voltage (b) on active BMT response.*

must increase, provided the bias current I_D is held constant. As a consequence, the SAW potential is reduced because of the rising concentration of mobile charge carriers at the SiO_2-Si surface. Figure 4.24 shows the measured detector output power as a function of the incident SAW power for a constant bias current of 2 mA. From this figure, it can be concluded that the BMT linearly converts the acoustic signals into electric signals. Measurements on symmetric devices with an identical source and drain configuration have revealed that no change is observed when the source and drain contacts are exchanged. This indicates that the direction of the RT current relative to the SAW direction is unimportant and the BMT is bidirectional.

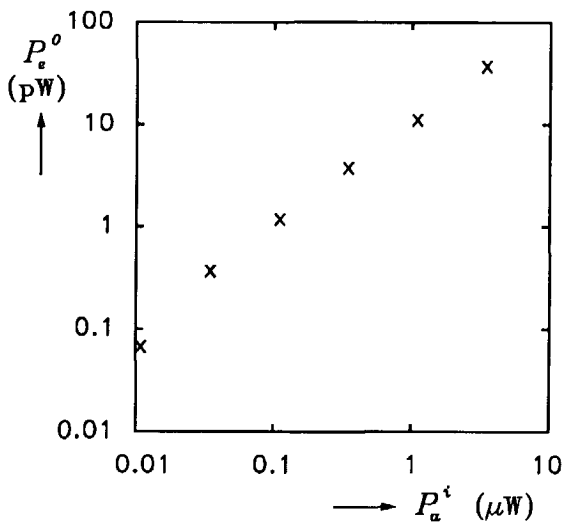


Figure 4.24: *The electric output power P_e^o (on 50Ω) vs. the acoustic input power P_a^i for $I_D = 2mA$.*

To investigate the influence of the passive detection, Fig. 4.25a shows the active, passive and accumulated responses. The passive detection decreases with increasing bias current, because the feedback conductance g_d of the RT channel which increases with increasing I_D shunts the drain electrode to ground. Although the electrode lengths are an integer number of the wavelength ($64\,\mu m = 2p_{idt} = 2\lambda$), a considerable passive output signal remains. As a result, the control range is reduced to about 11 dB. In Fig. 4.25b, the effect of the electrode length is shown. In this case, the electrode lengths are 2.5λ and a large sensitivity of the passive coupling mechanism results.

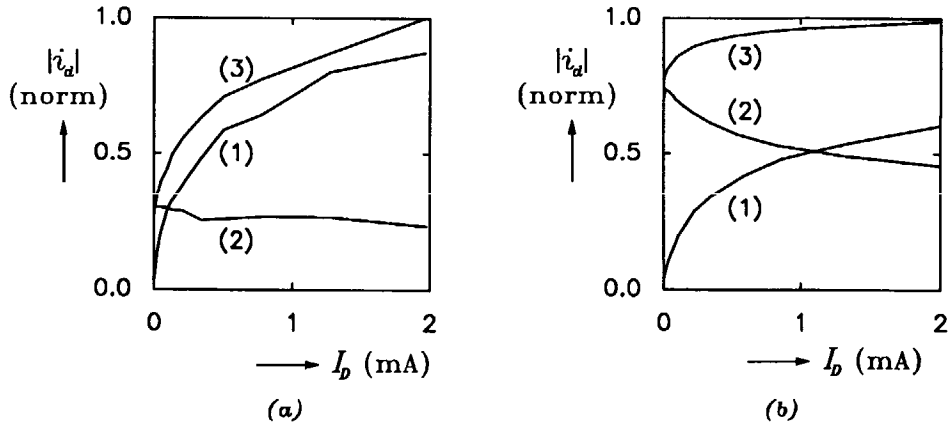


Figure 4.25: *Normalized detection responses of BMT with electrode lengths* 2λ *(a) and* 2.5λ *(b). The curves* (1), (2) *and* (3) *represent the active, passive and accumulated responses, respectively.*

4.6.3 Noise Measurements

The output noise of the BMT was measured with an HP 4195A spectrum analyzer. Since the input noise in the receiver section amounts to −150 dBm/Hz, two 20 dB HF amplifiers were cascaded before the spectrum analyzer in order to reduce the receiver noise. These amplifiers have a noise factor of 1.5 dB. With these amplifiers the ultimate receiver noise is reduced to −175 dBm/Hz. The noise measurements were taken at 100 MHz.

When the BMT, biased at 2 mA, is connected to the input of the analyzer, only a slight increase of about 5 dB in the noise spectrum is observed. From this measurement, it can be derived that the equivalent noise current is

$$i_n = 12\,\mathrm{pA}/\sqrt{\mathrm{Hz}} \tag{4.26}$$

In this derivation, the impedance of the cable between the BMT and the analyzer was included. The value given in Eq. 4.26 is much lower than predicted by the shot-noise theory, which gives a value of $25\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 2 mA. This may indicate the space-charge suppression of the noise.

4.7 CONCLUSIONS

In this chapter, a new active SAW detector which uses a planar RT diode has been introduced. The device is composed of junction electrodes only, the use of which produces a flat surface above the detector. The potential barrier between the source and drain electrodes is modulated by the electric fields accompanying the SAW. This results in a modulation of the injection current. Since the detector transconductance is controlled by the bias current, a simple output control results. The potential distribution in this Barrier-Modulated Tap has been derived using a finite-difference program and it shows a minimum in the potential barrier at the SiO_2-Si interface. Therefore, the injection current is concentrated near this interface, ensuring a strong acoustoelectric interaction. Because the current is dominated by drift, and there is hardly any charge storage, this device has excellent high-frequency properties. In addition, space-charge smoothing provides low-noise behavior.

DC and RF measurements around 100 MHz have verified the operation of the BMT. The DC current-to-voltage characteristics are dominated by space-charge-limiting effects, and follow the quadratic relationships of the Mott-Gurney law. Because of screening by mobile charge carriers, the SAW RF potential in the gap decreases at increasing bias currents. This results in a square root relationship between the RF detector current and the DC bias current. A good agreement is observed between the experimental results and the simulation results, which are obtained using an equivalent circuit model incorporating lumped network elements. In a bias current range of 0–5 mA, a maximum (untuned) power efficiency of –47 dB, and an output control range of more than 25 dB are obtained. However, a rather high DC power of 50–100 mW is required to obtain this efficiency. In addition to the active detection mechanism, there is a passive detection mechanism caused by the capacitive coupling of the SAW to the drain electrode. This mechanism limits the control range, and must be suppressed by methods discussed in Chapter 6.

For future improvements, the detector efficiency and DC power dissipation are most important. The efficiency can be increased by improving the ZnO deposition on thin SiO_2 layers, and by shrinking the detector aperture. The shrinkage lowers the output conductance and capacitance. Simulations using the equivalent circuit model revealed an increasing efficiency for decreasing detector apertures, provided the total acoustic power incident on the BMT remains constant. The DC power dissipation can be reduced by shrinking the lateral gap length, which results in a decrease of

the RT voltage. Extra implantation steps in the gap region can lower the RT voltage (compare the adjustment of the threshold voltage in MOSFETs). The DC power dissipation is, to a large extent, caused by the parasitic current flowing underneath the channel. Since this current is screened by the mobile carriers in the channel, it does not contribute to the detection process. It is believed that, with a dedicated doping profile in the gap, the current distribution can be modified in such a way that the current density (and thus the screening) decreases.

Chapter 5

THE PIEZOELECTRIC JUNCTION FET

5.1 INTRODUCTION

In Chapter 3, the use of Field-Effect transistors as active SAW detectors was discussed. SAW detecting FETs reported thus far have been of the MIS (Metal-Insulator-Semiconductor) type. In this FET type a metal electrode serves as the gate. In the current chapter, the Junction Field-Effect transistor (JFET) is considered. In the JFET, the metal gate of the MISFET is replaced by a p or n-type junction electrode. Since this devices is completely embedded in the silicon substrate, a flat surface is obtained. In the final process step, the JFET is covered with a piezoelectric ZnO layer, which results in a piezoelectric JFET (PI-JFET), which can be applied as an active SAW detector.

In section 5.2, the basic PI-JFET configuration and its operation are discussed. In addition, the dominant device parameters are considered. The SAW detecting capabilities of the PI-JFET are discussed in section 5.3. In section 5.4, the fabrication technology is considered, followed by the experimental results in section 5.5.

5.2 THEORETICAL JFET OPERATION

5.2.1 Basic Structure

To investigate the SAW detection operation of the JFET, a configuration was sought which is technologically compatible with the fabrication of the BMTs described in the previous chapter. The most simple configuration which responds to this demand is the n-channel JFET shown in Fig. 5.1. Two gates are discernable: a top gate G_T composed of a highly doped

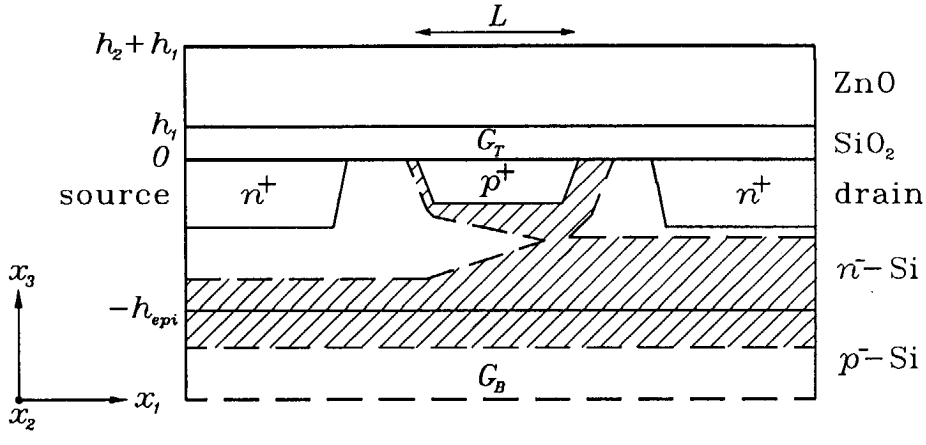


Figure 5.1: *Cross section of n-channel PI-JFET (hatched area represents depleted region).*

p^+ electrode, and a bottom gate G_B composed of the p^- substrate. In the epilayer between the top and bottom gates, an n^--type channel is created. Two n^+ diffusions have been added in order to obtain good ohmic contacts to the source and drain regions. Because the channel in the PI-JFET is buried underneath the pn gate, it is not affected by detrimental effects at the SiO_2-Si interface, for example, caused by the ZnO sputter process. When the gates are reversely biased with respect to the source, the depletion regions around the gate junctions expand, and the effective channel depth decreases. This gives a reduction of the channel conductance, and thus a reduction of the drain current. In this way, the drain current is modulated by a variation of the gate-to-source voltage. At a certain gate-to-source voltage the depletion regions of the top and bottom junctions meet, and the channel is pinched off.

The bottom gate is unattractive for high-frequency operation. It has a

large capacitance, and the lightly doped substrate represents a high series resistance. In addition, its controlling action on the channel is much less than that of the top gate, because the doping concentrations of the channel and the bottom gate are in the same order of magnitude. Therefore, in this work only the top gate is applied in the AC operation, which results in a *top-driven* JFET. The bottom gate is properly biased in order to acquire an optimal DC operation. The voltage difference between the top and bottom gates must remain below the vertical reach-through voltages as discussed in section 4.6, otherwise parasitic RT currents will flow through the gates.

The illustration in Fig. 5.1 only shows the JFET structure in the x_1 and x_3-directions. Since the top gate cannot extend to infinity in the x_2-direction, a proper means must be found to limit the channel region at the gate ends, otherwise the channel can never be pinched off completely. Since in this separated-gate JFET, an ohmic contact between the top gate and the substrate is prohibited, a p-isolation diffusion cannot be used for this purpose. Therefore, a ring-shaped structure of the top gate is required, thus separating the inner n-region from the n-region surrounding the ring. It is preferable to place the drain in the center of the ring for two reasons [174]:

1. minimizing the drain area, in order to minimize the detector output capacitance.

2. maximizing the source area, in order to minimize the source series resistance R_{SRC}.

These two considerations become especially important when the PI-JFETs are used in an array to make a PTDL. In this case, no p-isolation diffusions to separate the tap outputs are required, and the area outside the ring gates is one large, common source region.

5.2.2 JFET Parameters

In this section, the dominant parameters which characterize the PI-JFET are discussed.

(i) The pinch-off voltage

The pinch-off voltage V_P is defined as the gate-to-source voltage for which the edges of the gate depletion regions just meet [175, p. 317]. In this case, the channel region is completely depleted and the current from source to

drain vanishes. This definition is useful for the joined-gate JFET, and can be measured quite easily. This pinch-off voltage, indicated by V_{P0}, is completely fixed by the doping concentrations and vertical dimensions, and can be used to characterize the JFET device. However, for the separated-gate operation, this definition is not suitable, since in this case V_P is a function of both the top- and bottom-gate bias voltages, V_{GTS} and V_{GBS}. In this case, it is more convenient to redefine the pinch-off voltage V_P as that drain-to-source voltage V_{DS} for which the edges of the top- and bottom-gate depletion regions meet at the drain side. At this point, the current changes from its linear range into its saturation range. For joined-gate JFETs this drain-to-source voltage is also indicated by V_{DSsat}.

In the devices under consideration, the top-gate doping concentration N_T is much larger than the channel (= epilayer) doping concentration N_E, and an abrupt junction can be assumed. For the bottom gate $N_B \approx N_E$, and the depletion region around the bottom junction will expand both in the channel and the substrate. If the channel impurity concentration is assumed uniform, and the abrupt depletion approximation is used, it can be derived that V_P is implicitly given by

$$h_{ch} = \sqrt{\frac{2\epsilon_{Si}}{qN_E}} \left\{ \sqrt{V_P + |V_{GTS}| + V_{biT}} + \sqrt{\frac{N_B}{N_B + N_E}} \sqrt{V_P + |V_{GBS}| + V_{biB}} \right\} \tag{5.1}$$

in which h_{ch} is the channel depth defined as the distance between the top- and bottom-gate junctions ($h_{ch} = h_{epi} - h_j$), and V_{biT} and V_{biB} are the built-in voltages of the top and bottom gates, respectively. In Eq. 5.1, the influence of the bias voltages V_{GTS} and V_{GBS} is apparent. If these voltages are reduced to zero, the resulting V_P is identical to V_{P0}, which is the maximum value V_P can attain. To obtain a low output conductance, the JFET must be biased in the saturation region, which requires $V_{DS} > V_P$. For low operating levels, which are required for low-power detectors, a low pinch-off voltage is desirable.

(ii) The transconductance and channel conductance

The sensitivity of the drain current for variations in the gate potentials is described by the transconductance g_m (S). Since in the SAW detector only the top gate is used in the AC operation, only the transconductance g_{mT} related to this gate has to be evaluated.

The derivation of the transconductance of the top-driven JFET with different top-gate and bottom-gate conditions is much more difficult than that of an ordinary JFET. For the derivation of the top-gate transcon-

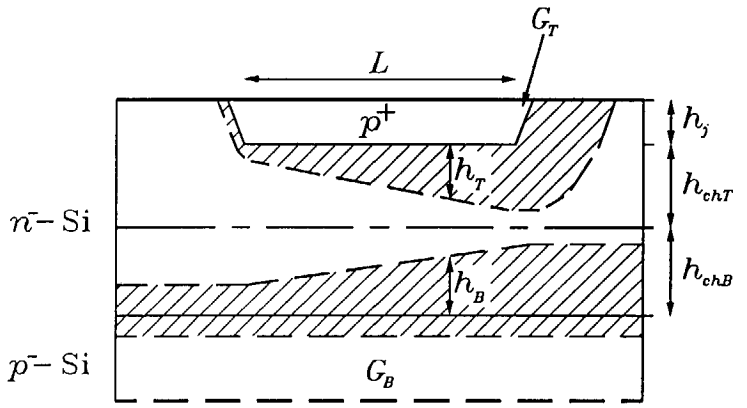


Figure 5.2: *Channel separation into an upper and lower part* ($h_{chT} + h_{chB} = h_{ch}$).

ductance g_{mT}, the configuration of Fig. 5.2 is applied. By using the gradual channel approximation [175, pp. 314-322], the channel current in this structure is given by

$$\begin{aligned} I_D\, dx_1 &= W_c N_E q \mu_n [h_{ch} - h_T - h_B] d\psi \\ &= W_c N_E q \mu_n [h_{chT} - h_T] d\psi + W_c N_E q \mu_n [h_{chB} - h_B] d\psi \quad (5.2) \end{aligned}$$

in which W_c is the channel width, μ_n the electron mobility in the channel which is assumed to be field-independent, and h_T, h_B are the top and bottom depletion layer widths given by

$$h_T = \sqrt{\frac{2\epsilon_{Si}}{qN_E}} \sqrt{\psi(x_1) + |V_{GTS}| + V_{biT}}$$

$$h_B = \sqrt{\frac{2\epsilon_{Si}}{qN_E}} \sqrt{\frac{N_B}{N_B + N_E}} \sqrt{\psi(x_1) + |V_{GBS}| + V_{biB}}$$

where $\psi(x_1)$ is the static potential in the channel. A uniform channel impurity concentration is assumed. In addition, the channel length L is assumed to be much longer than the channel depth h_{ch}. From Eq. 5.2, it can be derived that the current can be divided into a top and a bottom part: one current part flows in the upper region of the channel with depth h_{chT}, and the other current part flows in the lower region of the channel with depth h_{chB}. Integration of this current along the channel from $x_1 = 0$

to L, and assuming $N_T \gg N_E$, gives the total drain current

$$I_D = \frac{W_c}{L}\frac{\mu_n q^2 N_E^2}{\epsilon_{Si}}\left[\left(\frac{1}{2}h_{chT}(h_{TD}^2 - h_{TS}^2) - \frac{1}{3}(h_{TD}^3 - h_{TS}^3)\right) + \left(\frac{1}{2}h_{chB}(h_{BD}^2 - h_{BS}^2) - \frac{1}{3}(h_{BD}^3 - h_{BS}^3)\right)\right] \tag{5.3}$$

in which h_{TS},h_{BS} and h_{TD},h_{BD} are the gate depletion layer widths at the source and drain sides, respectively.

The top-gate transconductance g_{mT} follows from Eq. 5.3 by taking the derivative to V_{GTS}. However, this is not a trivial task, since the parameters h_{chT} and h_{chB} also depend on V_{GTS}. When this dependence is ignored, a simple expression for g_{mT} in the saturation range is found

$$g_{mT} = \frac{dI_D}{dV_{GTS}} = \frac{W_c}{L}\mu_n\sqrt{2\epsilon_{Si}qN_E}\left(\sqrt{V_P + |V_{GTS}| + V_{biT}} - \sqrt{|V_{GTS}| + V_{biT}}\right) \tag{5.4}$$

with V_P as defined in Eq. 5.1. The influence of V_{GBS} on g_{mT} enters via this V_P. The g_{mT} was numerically evaluated by calculating I_D vs. V_{GTS} as described in Eq. 5.3, and determining the derivative afterwards. This solution was compared to the g_{mT} given in Eq. 5.4, and it was found that for the JFETs described in section 5.5, the error made by using Eq. 5.4 is less than 10%.

The transconductance is maximal when the bias voltages on the gates are zero. However, it can severely be deteriorated by the source series resistance R_{SRC}

$$g'_{mT} = \frac{g_{mT}}{1 + g_{mT}R_{SRC}} \tag{5.5}$$

where g'_{mT} is the external top-gate transconductance, measured at the terminals of the device. Although the source was chosen outside the ring gate and may encompass a large area, the source resistance can still be considerable, because the channel is created in a high resistivity epilayer. Therefore, the n^+ electrode in the source region should be placed as close to the channel entrance as possible.

A computer program was developed to calculate g_{mT} under various bias conditions. In this program, the dependence of h_{chT} and h_{chB} on V_{GTS} is included. In Fig. 5.3, the variation in g_{mT} is shown when the gate bias voltages are varied. The following parameters were used: $N_E = N_B = 6 \cdot 10^{20}\,\mathrm{m}^{-3}$, $h_{ch} = 6\,\mu\mathrm{m}$, $W_c/L = 100$, $\mu_n = 0.13\,\mathrm{m}^2/\mathrm{Vs}$. The joined-gate operation produces the strongest control. In Fig. 5.4, g_{mT} vs. V_{GTS} with V_{GBS} as parameter is depicted.

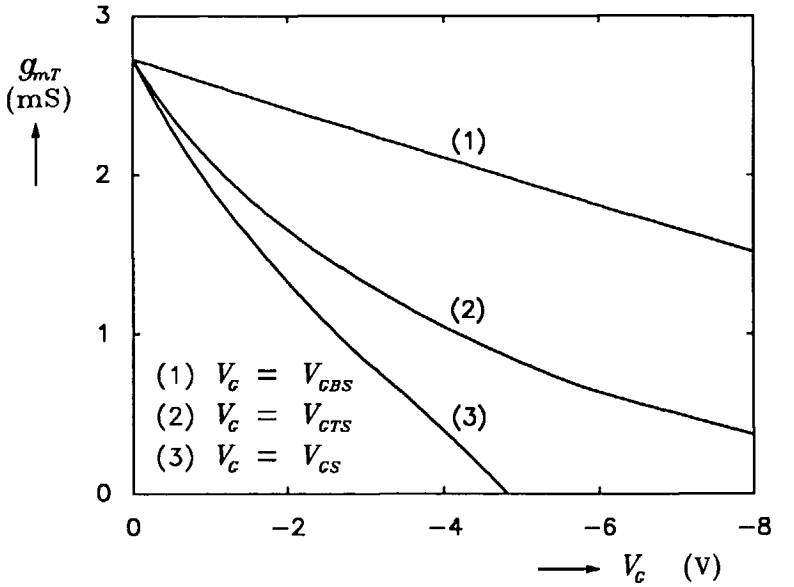


Figure 5.3: *Top-gate transconductance g_{mT} vs. V_{GTS} with $V_{GBS} = 0$ (1), vs. V_{GBS} with $V_{GTS} = 0$ (2), and vs. the joined-gate bias voltage (3).*

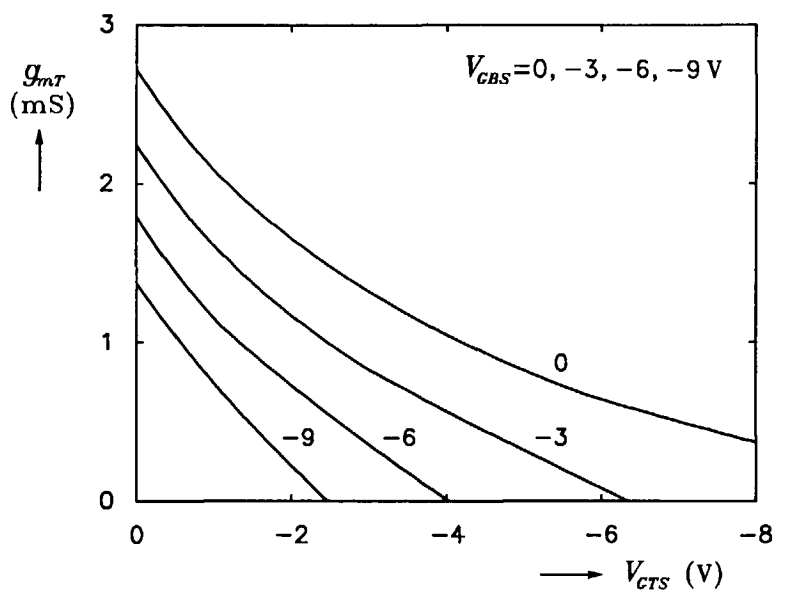


Figure 5.4: *Top-gate transconductance g_{mT} vs. V_{GTS} with V_{GBS} as parameter.*

The channel or drain conductance g_d (S) is derived from dI_D/dV_{DS}. In the linear range ($V_{DS} \ll V_P$), g_d can be derived from Eq. 5.3. For the JFET used as a detector, the linear range is of less importance because of the high output conductance involved. In the saturated range ($V_{DS} > V_P$), the channel is pinched off, and, theoretically, the output conductance goes to zero.

(iii) The saturation current I_{DSS}

The saturation current I_{DSS} is defined as the drain current flowing under saturation conditions ($V_{DS} > V_P$) when $V_{GTS} = V_{GBS} = 0$. It is the maximum attainable drain current. Its value can be derived from Eq. 5.3 by replacing h_{TD},h_{BD} by h_{chT},h_{chB}.

The saturation current is important with respect to the DC power dissipation of the PI-JFET. By employing the PI-JFET as programmable tap in the PTDL, this power dissipation must be minimized. An indication of the DC power dissipation is given by $I_{DSS} \cdot V_P$. It can be shown that there is a strong relationship between I_{DSS}, V_P and g_m

$$\frac{g_m V_P}{I_{DSS}} = \alpha \tag{5.6}$$

in which α is a constant, which is 2 for the ideal joined-gate JFET. In practice, a value between 1 and 3 is found [176]. By using Eq. 5.6 the DC power dissipation becomes proportional to $\alpha I_{DSS}^2/g_{mT}$. In order to minimize I_{DSS}, a low channel doping and small channel width W_c are preferable (see Eq. 5.3).

(iv) The gate and drain capacitances

The high-frequency behavior of a top-driven JFET is dominated by the top-gate capacitance C_{GT} and drain capacitance C_D. The top-gate capacitance of the JFET consists of the depletion layer capacitance around the p^+n junction electrode. Two parts must be distinguished: the channel capacitance C_{ch} between the gate and the channel, and the sidewall capacitances C_{sw} between the gate and the source/drain regions.

Since the capacitances are determined by the depletion layer widths around the top-gate electrode, C_{ch} and C_{sw} depend on the bias conditions. In the saturation range, the top-gate capacitance is dominated by the capacitance to the source, since there the voltage drop and thus the depletion layer width is smallest. For $V_{DS} > V_P$, the sidewall capacitances

per unit length (F/m) at the source and drain side, C_{swS} and C_{swD}, can be estimated by using

$$C_{swS} \approx h_j \sqrt{\frac{q\epsilon_{Si}N_E}{2(|V_{GTS}| + V_{biT})}} \tag{5.7}$$

$$C_{swD} \approx h_j \sqrt{\frac{q\epsilon_{Si}N_E}{2(V_{DS} + |V_{GTS}| + V_{biT})}} \tag{5.8}$$

where h_j is the junction depth of the top gate. In the channel itself the top-gate capacitance (in F/m^2) is given by

$$dC(x_1) = \sqrt{\frac{q\epsilon_{Si}N_E}{2(\psi(x_1) + |V_{GTS}| + V_{biT})}} dx_1 \tag{5.9}$$

and depends on the local potential $\psi(x_1)$ in the channel. If a linear potential distribution is assumed which rises from 0 to V_P along the channel, integrating Eq. 5.9 from $x_1 = 0$ to L gives the total channel capacitance per unit width

$$C_{ch} = \frac{L}{V_P^2}\sqrt{2q\epsilon_{Si}N_E}(\sqrt{V_P + |V_{GTS}| + V_{biT}} - \sqrt{|V_{GTS}| + V_{biT}}) \tag{5.10}$$

This is only a first-order approximation. Actually, the voltage distribution in the channel is not linear, and the expression for C_{ch} is more complex.

The drain capacitance C_D is determined by the reverse-biased epi–substrate junction. Because of the lightly doped substrate and the large drain reverse voltage, a small capacitance per unit area is obtained. Since this capacitance is linearly proportional to the drain area, a small area is desirable.

The capacitance of the source can be quite large because of its large area and the small gate-to-source voltages. However, since the JFETs considered in this work operate in the common-source mode, the large source capacitance has no detrimental effects on the HF detection behavior.

5.2.3 Small-Signal Model

The small-signal model for the top-driven JFET is shown in Fig. 5.5. In the saturated current range, the input capacitance C_{GTS} is determined by the channel capacitance and the sidewall capacitance at the source side

$$C_{GTS} = W_c \cdot (C_{ch} + C_{swS})$$

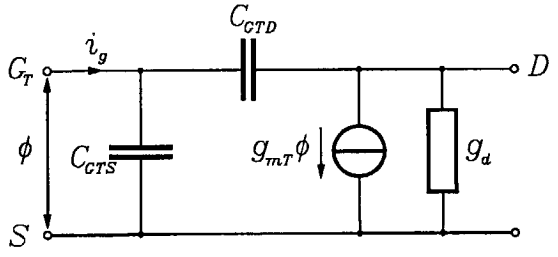


Figure 5.5: *Small-signal model of the top-driven JFET.*

whereas the capacitance between top gate and drain C_{GTD}, is only determined by the sidewall capacitance at the drain side

$$C_{GTD} = W_c \cdot C_{swD}$$

At the output terminal, the drain conductance g_d is located, which is usually very small in the saturation range. The direct capacitance between source and drain is very small and is ignored.

A commonly used figure of merit for the JFET is the cutoff frequency f_T. At this frequency, the current gain of a short-circuited JFET which operates in the common-source mode has been reduced to 1. From Fig. 5.5, it can be derived that this frequency is given by

$$f_T = \frac{g_{mT}}{2\pi(C_{GTS} + C_{GTD})} \tag{5.11}$$

For long-channel JFETs, the capacitance in the denominator is dominated by the channel capacitance C_{ch}. Using Eq. 5.4 and 5.10, the cutoff frequency can then be estimated by

$$f_T = \frac{\mu_n V_P}{2\pi L^2} \tag{5.12}$$

For short-channel JFETs the sidewall capacitance at the gate-source junction dominates, and the cutoff frequency can be approximated with

$$f_T = \frac{1}{\pi h_j}\frac{\mu_n}{L}\left(\sqrt{V_P(|V_{GTS}| + V_{biT}) + (|V_{GTS}| + V_{biT})^2} - (|V_{GTS}| + V_{biT})\right) \tag{5.13}$$

In both cases, decreasing L will improve the high-frequency performance. In addition, a large V_P value appears to be advantageous. This can be achieved by increasing the channel depth d_{ch}, and the channel impurity concentration N_E (see Eq. 5.1). However, because of the reduction of μ_n at higher doping levels [177], increasing N_E is not so effective. In addition, it increases I_{DSS}. Therefore, wide, lightly doped channels are preferable in the JFET design [176].

5.3 SAW DETECTION WITH PI-JFET

5.3.1 Active SAW Detection

The top-driven JFET described in the previous sections can be employed for the detection of SAWs. When the JFET is covered with a piezoelectric film and is placed in the propagation path of the SAW, the electric fields accompanying the acoustic waves capacitively couple to the top gate. As a result, the top-gate voltage is modulated, which gives a modulation of the drain current. In contrast to the BMT, the electric fields of the SAW do not directly interact with the mobile charge carriers. The detection mechanism consists of two stages: 1. modulation of the top-gate voltage, which in its turn gives 2. a modulation of the drain current. In fact, the first detection stage represents the passive detection of the SAW by the PI-JFET top gate, acting as a single-electrode detector (see section 3.2.1). The second detection stage involves the active gain of the PI-JFET.

Since only the gate parts perpendicular to the SAW propagation direction contribute to the detection process, rather elongated ring-shaped top gates are required to obtain an optimal SAW detection, see Fig. 5.6 (not to scale). The metal contacts to gate, source and drain electrodes are located outside the SAW propagation path. When the gate parts parallel to the propagation direction are ignored, the total channel width W_c is twice the acoustic aperture: $W_c = 2W$. For an optimal detection, the signals on the elongated gate electrodes on both sides of the ring must be in phase. Therefore, the distance between the gate electrodes perpendicular to the SAW must be an integer times the wavelength λ. The gate parts parallel to the SAW direction do not contribute to the SAW detection, and the bias current flowing through these parts is a parasitic current

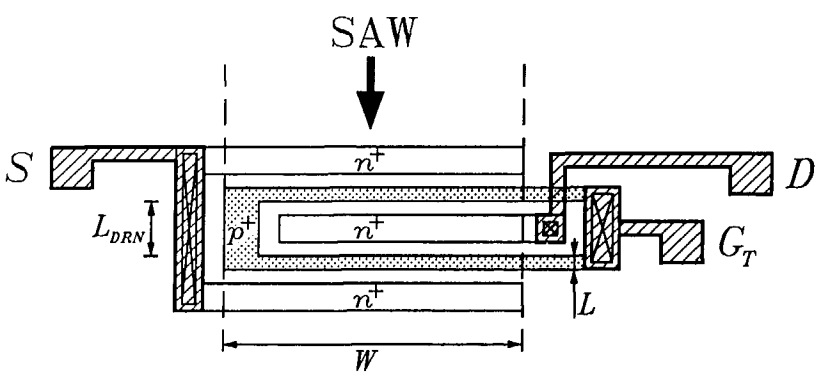


Figure 5.6: *Top view of PI-JFET detector.*

which must be minimized. This is achieved by designing the drain length L_{DRN} as small as possible. Since the separation between the elongated gate electrodes is limited to one wavelength, the minimal drain length is $\lambda - L$. A further reduction of the parasitic drain current can be obtained by increasing the gate length itself in these gate parts.

A maximal voltage swing on the top gate is achieved when it is floating. In addition, the capacitive coupling between the SAW and the top gate is maximized when the gate length L is an odd number of $\lambda/2$, see Eq. 3.12. This passive coupling mechanism in the first detection stage of the JFET seems to enhance regeneration phenomena. However, it will be shown that the combined passive and active detection mechanisms of the first and second detection stages require a gate length as small as possible. Although this will reduce the passive coupling, the overall efficiency is improved, and the regeneration effect is suppressed.

The AC detection sensitivity of the PI-JFET can be derived by using the small-signal circuit presented in section 5.2.3, and the passive detection theory of a junction electrode presented in section 3.4.2. In the latter section, the detection current of an electrode at the silicon surface was given in Eq. 3.12. This current can be considered as the input current i_g of the PI-JFET under consideration. Ignoring the gate-to-drain capacitance C_{GTD}, the amplitude of the total short-circuit current at the output of the JFET becomes

$$i_{d0}^2 = 16\,\omega\,W^2 \left(\frac{g_{mT}}{C_{GTS}}\right)^2 P_a \left(\frac{\rho_{s0}^2}{\omega P_a}\right) \frac{\sin^2(kL/2)}{k^2} \qquad (5.14)$$

in which W is the acoustic aperture ($= 0.5W_c$) of the PI-JFET. The ratio g_{mT}/C_{GTS} is related to the cutoff frequency. A high cutoff frequency is preferable. Since this ratio is inversely proportional to L or L^2, decreasing L will always improve i_{d0}, even at the expense of the passive detection strength of the gate (represented by the sine function).

It should be noted that in contrast to a general JFET employed for amplification purposes, the gate resistance in the SAW detecting JFET is of minor importance. The SAW electric fields locally act on the floating gate regions, and the AC signals are not supplied externally. Since no DC nor RF currents have to flow through the gate, even for high frequencies, a metallization of the junction gate is not required. The f_T mentioned in section 5.2.3 can, therefore, only be considered as an internal cutoff frequency, which cannot be measured externally. Because the top gate is essentially current driven, the high gate resistance does not deteriorate the noise performance of the PI-JFET.

In Eq. 5.14, it can be seen that the output current can be controlled by varying g_{mT}. In Fig. 5.3, it was shown that the g_{mT} changes most rapidly when the top and bottom gates are joined for DC operation. However, this is impossible if an array of PI-JFETs is used as in the PTDL. Since the bottom gate is created by the substrate, this would mean that all gates of the PI-JFET array are connected together, and a separated control of the individual taps is prohibited. Therefore, the PI-JFET can only be controlled by the top-gate bias voltage. A proper bias voltage on the substrate is required to obtain an optimal control range, see Fig. 5.4.

5.3.2 Passive SAW Detection

In addition to the desired capacitive coupling to the top gate, there is also a capacitive coupling to the drain electrode. Even when the channel is completely pinched off and the drain current vanishes, an output signal remains. The drain electrode is a single-electrode detector of length L_{DRN}. Because of the restrictions placed on the ring gate ($L_{DRN} = n\lambda - L$, with n an integer), this drain length L_{DRN} can never be exactly an integer number of wavelengths. The gate length L should be as small as possible to obtain a low passive SAW sensitivity of the drain. The use of balancing to suppress the passive detection is discussed in the next chapter.

5.4 FABRICATION TECHNOLOGY

In the test chip shown in Fig. 4.16, apart from BMTs also PI-JFETs were included. As was mentioned at the beginning of this chapter, the same fabrication technology for the PI-JFET detectors is applied as is used for the BMTs. The processing scheme is shown in Table 4.2. The thick, high resistivity epilayer results in a wide, lightly doped n-channel, which provides good HF properties. However, a relatively high source resistance must be expected. In contrast to the BMT, the epilayer thickness is a crucial parameter determining the JFET's DC and AC characteristics. A good control of this thickness is required.

The n^+ diffusions are more important than in the BMT case, since they create the source and drain electrodes of the PI-JFET. A standard n^+ diffusion was used, with a junction depth of about $2\,\mu$m, and a sheet resistivity in the order of 5–$6\,\Omega/\square$. After the final fabrication step, the step discontinuity at the n^+ edge was probed. A step of $0.16\,\mu$m is present in the SAW propagation path. This step is caused by the different etch and growth rates of the SiO_2 layer above the epi and n^+ regions. Although this topological discontinuity is only 0.5% of the SAW wavelength, it can be

prevented by replacing the diffusion step by an implantation step through the 0.1 μm SiO_2 layer, which is similar to the implantation of the p^+ regions.

The most important process step for the JFET detector is the fabrication of the top gate, which is obtained by the p^+ implantation. Although channeling is suppressed by the 0.1 μm oxide, an implantation tail beneath the p^+ electrode cannot completely be avoided. Because of this tail, the p^+ junction is not abrupt, and the effective epilayer doping in the vicinity of the top gate is reduced.

5.5 EXPERIMENTAL RESULTS

An enlarged view of the PI-JFETs is depicted in Fig. 5.7. Only one type of PI-JFET was designed with the following dimensions (see Fig. 5.6): $L = 16\,\mu$m, $L_{DRN} = 48\,\mu$m, and $W = 800\,\mu$m which corresponds to a total gate width of about 1600 μm. The gate parts parallel to the SAW have a gate length of 40 μm, and a gate width of 64 μm. The diffused n^+ source and drain electrodes have a length of 32 μm.

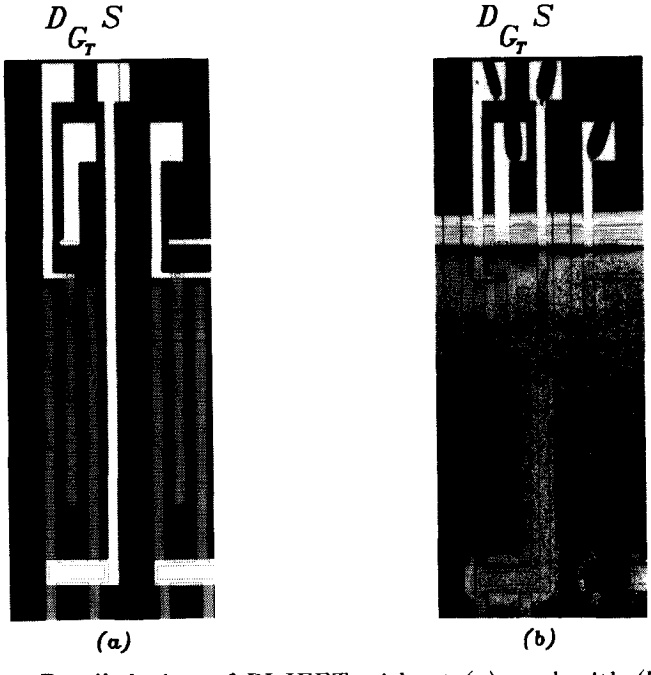


Figure 5.7: *Detailed view of PI-JFET without (a), and with (b) the ZnO layer.*

5.5.1 Parameter Analysis

The DC characteristics of the PI-JFET are mainly determined by the pinch-off voltage V_P. Since this parameter depends on the top-gate and bottom-gate bias voltages, for characterization it is better to determine V_{P0} for the joined-gate FET. In addition, the separated-gate pinch-off voltages V_{PT0} (with $V_{GBS} = 0\,\mathrm{V}$), and V_{PB0} (with $V_{GTS} = 0\,\mathrm{V}$) of the top and the bottom gate can easily be determined. In fact, V_{PT0} and V_{PB0} represent the vertical reach-through voltages when the top gate or bottom gate acts as the drain of a vertical RT diode, respectively.

The pinch-off voltages can best be obtained by measuring $\log(I_D)$ vs. the gate voltage V_G, and determining the transition point between the saturation (quadratic) and subthreshold (exponential) range. This transition point can be obtained from the intersection point of two lines tangent to the logarithmic I_D curve at $V_G = 0\,\mathrm{V}$ and to the I_D curve in the subthreshold region [176]. In this measurement method, V_{DS} can be kept very small, and influences from leakage currents and the source series resistance R_{SRC} are minimized.

The measured pinch-off voltages are given in Table 5.1 By using the assumed doping concentrations in the epilayer and substrate, the joined-gate pinch-off voltage corresponds to a channel depth h_{ch} of about $6.3 \pm 0.3\,\mu\mathrm{m}$, which is in the range mentioned in section 4.5. The vertical reach-through voltages mentioned in section 4.6 agree with the separated-gate pinch-off voltages V_{PT0} and V_{PB0} given in Table 5.1.

Table 5.1: *Measured pinch-off voltages.*

V_{P0}	5.1 ± 0.3	V
V_{PT0}	11.2 ± 0.6	V
V_{PB0}	20.4 ± 1.2	V

The transconductance in the saturation region can be obtained from $\partial I_D/\partial V_G$ for $V_{DS} > V_P$. In the devices under consideration, V_{DS} is fixed at 15 V. Three different transconductances are considered: the top-gate transconductance g_{mT0}, the bottom-gate transconductance g_{mB0}, and the joined-gate transconductance g_{m0}, all determined with zero bias conditions at the gates ($V_{GTS} = V_{GBS} = 0\,\mathrm{V}$). The measured values are given in Table 5.2. The measured channel conductance g_d at very small V_{DS} values is also given. From Table 5.2 can be concluded that $g_{m0} = g_{mT0} + g_{mB0}$, and that $g_d(V_{DS} \to 0) \approx g_m(V_{DS} > V_P)$ as is predicted by theory. However, the magnitudes of the measured transconductances are much lower

Table 5.2: *Measured pinch-off voltages.*

g_{m0}	2.2 ± 0.1	mA/V
g_{mT0}	1.4 ± 0.1	mA/V
g_{mB0}	0.8 ± 0.1	mA/V
g_d	2.0 ± 0.1	mA/V

than theoretically predicted. For example, when the g_{mT0} is calculated by using Eq. 5.4, a value results, which is about twice the experimental value. Two reasons can be given: the source series resistance R_{SRC} which causes an extra voltage drop and is further dealt with in the next section, and the implantation tail of the top-gate electrode. As a result of the latter effect, the top gate has a gradual doping profile, which gives a reduced sensitivity. Both R_{SRC} and the implantation tail have the largest influence at zero bias conditions on the gates.

For the determination of the gate capacitance, comb test structures are used [176]. In Fig. 5.8 a photograph of these test structures is shown.

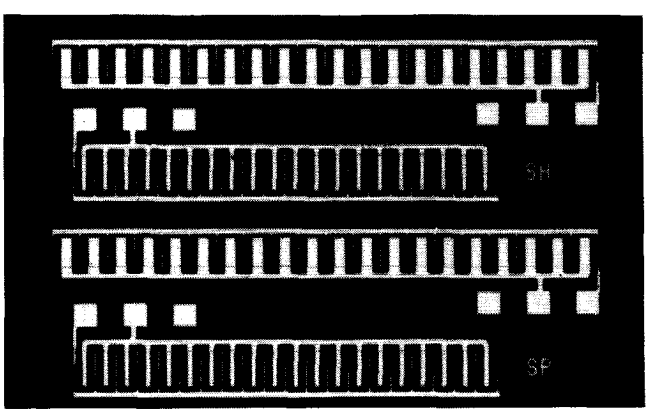


Figure 5.8: *Test structures for the CV measurements.*

Basically, these structures are large *pn* diodes, in which the anodes are created by a number of wide p^+ electrodes connected in parallel. These p^+ electrodes are interlaced with narrow n^+ electrodes contacting the epilayer, and create the cathodes of the diodes. From the *CV* measurements on these structures, the channel capacitance of the PI-JFET can be deduced. By using two types of test structures with the same overall perimeter but

with different areas, the sidewall and other parasitic capacitances cancel, and a good indication of the channel capacitance is obtained.

The CV measurements on these devices are not very accurate for two reasons. The structures are located on the thin SiO_2 regions ($h_{ox} = 0.1\,\mu$m). Therefore, a large MOS capacitance, created by the metal leads and bonding pads, is present in parallel to the pn capacitance. Although the measurements have been corrected for this parasitic capacitance, a considerable error results when the parasitic values are much larger than the measured ones. A second cause of disturbance is the high resistivity of the epilayer. This resistive part in the test structures cannot be ignored, and it perturbs the CV measurement. As a consequence of these effects, the accuracy is limited to about 10 to 20%.

For the channel capacitance C_{ch0} under zero bias conditions a value per unit area of

$$C_{ch0} = 8.7 \cdot 10^{-5}\ \mathrm{pF}/\mu\mathrm{m}^2$$

is found. This is about 15% higher than predicted by the depletion capacitance approximation. This value is obtained by considering the measurement results of two test structures with different areas. Using this result with the measurements on a single structure, the sidewall capacitance can be estimated

$$C_{sw0} = 1.3 \cdot 10^{-4}\ \mathrm{pF}/\mu\mathrm{m}$$

A crude approximation of the cutoff frequency defined in Eq. 5.11 can be obtained with the measured values of g_{mT} and C_{GTS}. The capacitance C_{ch0} presented above, has been measured at zero voltage conditions. Half this capacitance is a reasonable approximation of the top-gate capacitance in the saturation range. Ignoring C_{GTD} and the sidewall capacitances, the estimated f_T becomes

$$f_T = 160\,\mathrm{MHz}$$

5.5.2 DC Measurements

In this section, the DC characteristics of the PI-JFET are investigated. Firstly, the relationship between the drain current and the drain-to-source voltage is considered. Then the control of the transconductance by the gate voltages is examined.

A typical pentode characteristic of I_D vs. V_{DS} is shown in Fig. 5.9. The top-gate bias voltage V_{GTS} is stepped from 0 to -6 V, whereas the bottom-gate bias voltage V_{GBS} is held at a fixed level of -6 V. The slope of the curves in the saturation range is rather high. Close examination of the devices revealed that the effect was caused by a leakage current in the

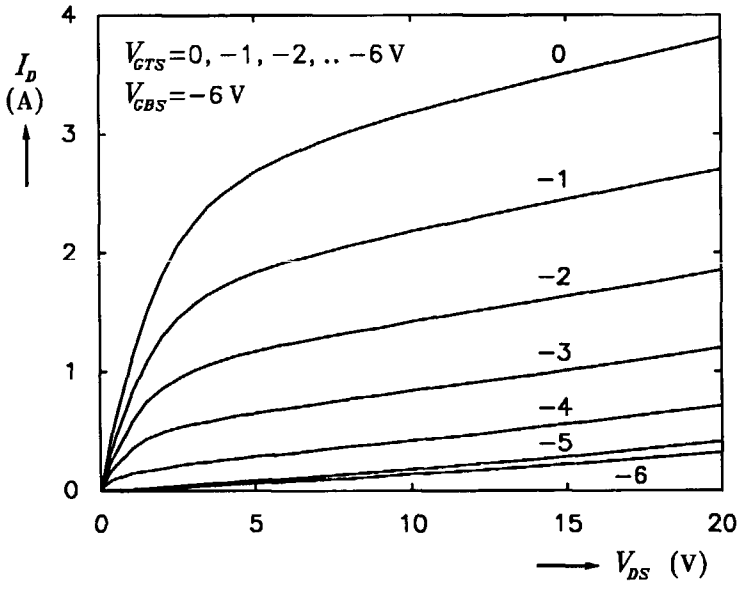


Figure 5.9: *Drain current I_D vs. drain-to-source voltage V_{DS}. The top-gate bias voltage V_{GTS} steps, the bottom-gate bias voltage V_{GBS} is fixed at −6 V.*

top gate, which induced a rather high bottom gate current. Measurements on JFETs without ZnO did not show these effects and it can, therefore, be concluded that the increased top-gate leakage current results from the ZnO sputtering. Further research on this phenomenon is required. As a result of the slope of the $I_D(V_{DS})$ curve, the output conductance g_d in the saturation range is limited to about 0.1 mS.

In the previous section, the top-gate transconductance was considered for zero bias conditions at the gates. In Fig. 5.10, the dependence of the top-gate transconductance g_{mT} on gate bias voltages is shown. This should be compared with the simulations in Fig. 5.3. A discrepancy for the higher g_{mT} values is observed. It was mentioned before that the source series resistance and the top-gate doping profile are the main causes of this deviation. When the doping profile is ignored, an estimation for R_{SRC} can be obtained by using Eq. 5.5. The solid lines in Fig. 5.10 show the simulation results under the same conditions as in Fig. 5.3, but with an additional R_{SRC} of 400 Ω.

From Fig. 5.10, it can be concluded that the optimal control of the top-gate transconductance is obtained under joined-gate bias conditions. However, this condition is unacceptable, since it prevents the individual control of PI-JFETs placed in an array. Therefore, only the top-gate bias

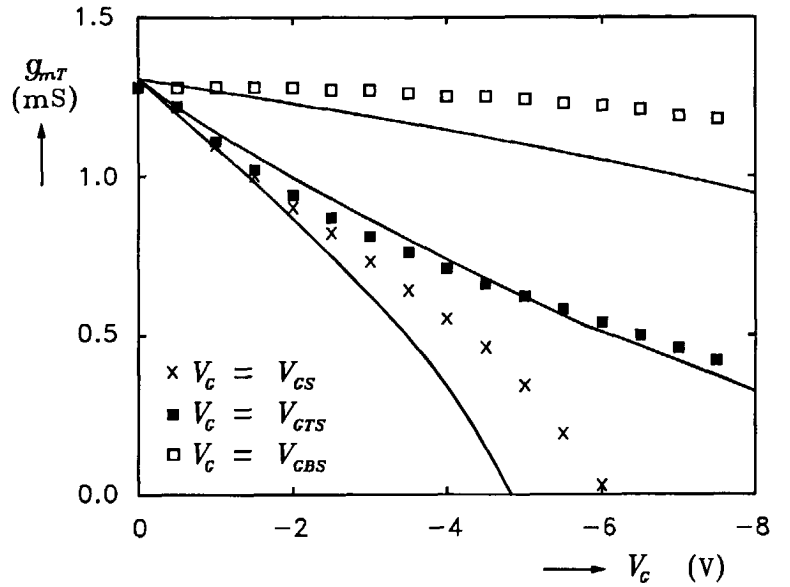


Figure 5.10: *Top-gate transconductance g_{mT} vs. V_{GTS} with V_{GBS} = 0 V (a), vs. V_{GBS} with V_{GTS} = 0 V (b), and vs. the joined-gate voltage V_{GTS} = V_{GBS} (c). The solid lines represent the simulation results.*

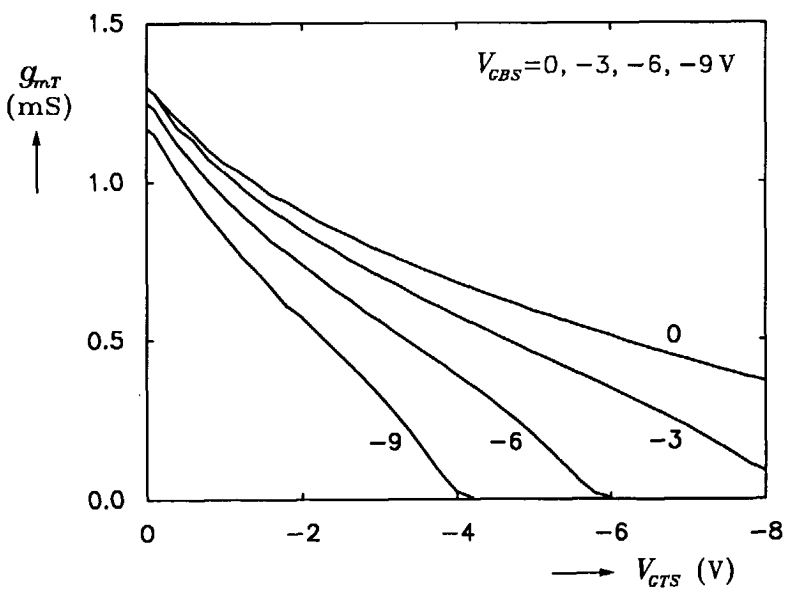


Figure 5.11: *Top-gate transconductance g_{mT} vs. V_{GTS} with V_{GBS} as parameter.*

voltage can be applied for the amplitude control, whereas the bottom-gate voltage must be held at a fixed bias voltage. In Fig. 5.11 the control of g_{mT} by V_{GTS} with V_{GBS} as parameter is shown. When V_{GBS} is comparable to the pinch-off voltage V_{P0}, an acceptable control swing for V_{GTS} results without sacrificing too much of the sensitivity at $V_{GTS} = 0\,\text{V}$.

5.5.3 RF Measurements

To investigate the SAW detecting properties of the PI-JFET, the devices are covered with a $8\,\mu\text{m}$ thick ZnO layer. SAWs with a center frequency of 94.5 MHz are generated with a conventional metal IDT, which has a period of $32\,\mu\text{m}$ and an aperture of 1.7 mm. The SAW power per unit width is 0.7 mW/m. These conditions are the same as for the BMT case, discussed in section 4.6.

Since the top gate must float for the RF signals, a high resistor of $10\,\text{k}\Omega$ is located between the top gate and the controlling voltage source. The measurement procedure is identical to the case of the BMTs. The detection current i_d caused by the active detection at 94.5 MHz in an untuned $50\,\Omega$ load is shown in Fig. 5.12a. The drain-to-source voltage is fixed at 10 V, which results in a drain bias current of $I_D = 3\,\text{mA}$ at $V_{GTS} = 0\,\text{V}$, $V_{GBS} = -6\,\text{V}$. For a fixed bottom-gate bias voltage of –6 V, the control range is more than 30 dB. In Fig. 5.12b, the corresponding phase relation is depicted, which is reasonably constant. The total top-gate width W_c is $1600\,\mu\text{m}$. Therefore, the total SAW power incident on the PI-JFET is $1.1\,\mu\text{W}$, and the untuned power efficiency at $V_{GTS} = 0\,\text{V}$, $V_{GBS} = -6\,\text{V}$ is –52 dB. By using Eq. 5.14 and the ρ_{s0} obtained from Fig. 2.4, the theoretical efficiency becomes –30 dB. The discrepancy can be attributed to the state of the ZnO, and to the additional capacitive loading of the top gate by the leads and the bonding pad, which were added for testing purposes.

Figure 5.12 also shows the detector current when the substrate is connected to the source ($V_{GBS} = 0\,\text{V}$). Although the variation in i_d corresponds to the variation in g_{mT} vs. V_{GTS} for $V_{GTS} < -4\,\text{V}$, in the lower range ($-4\,\text{V} < V_{GTS} < 0\,\text{V}$) the curve for $V_{GBS} = 0\,\text{V}$ behaves quite differently. This is more clearly shown in Fig. 5.13a, in which the detector current is given vs. V_{GBS} with V_{GTS} fixed at 0 V. Although g_{mT} decreases slowly with decreasing V_{GBS}, see Fig. 5.10, the detector current rises. By considering Eq. 5.14, it must be concluded that the top-gate capacitance C_{GTS} decreases when the bias voltage on the bottom gate is increased. This can readily be understood by considering the cross section of the

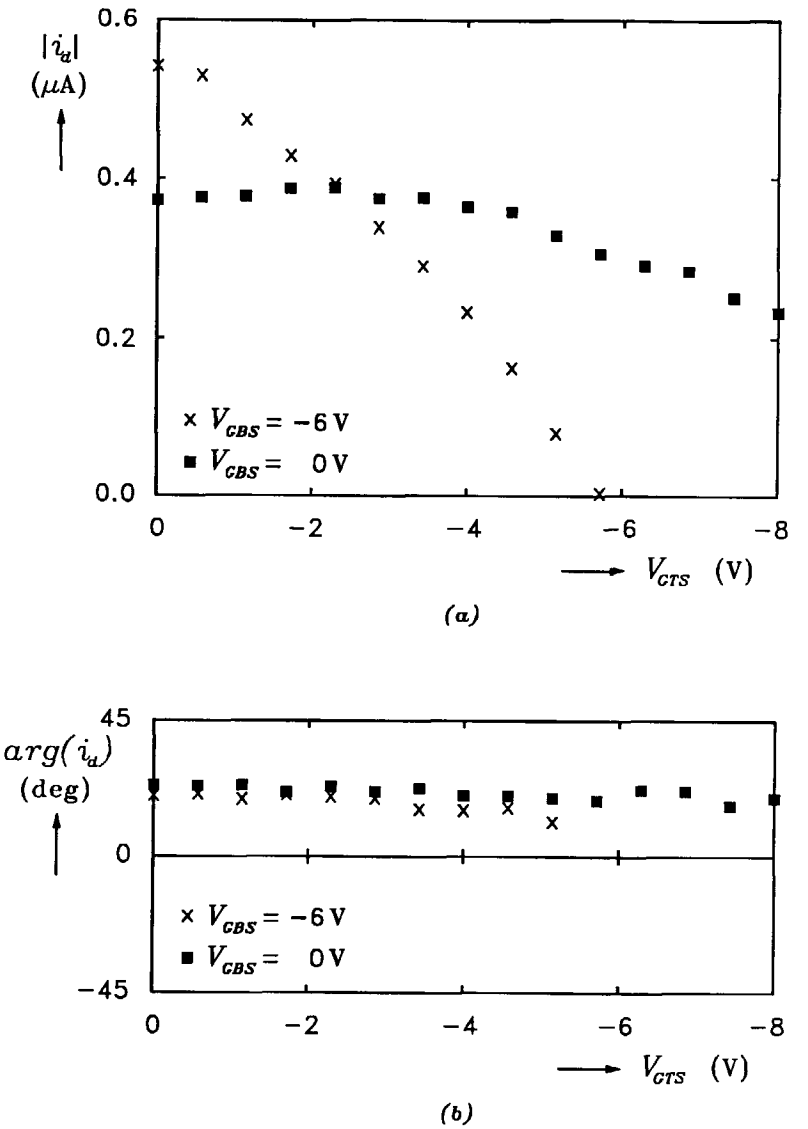


Figure 5.12: *Amplitude (a) and phase (b) responses of PI-JFET at 94.5 MHz.*

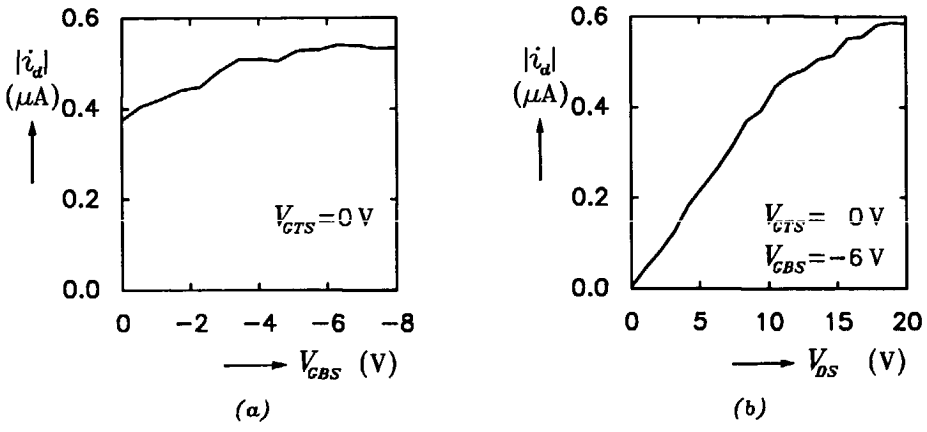


Figure 5.13: *PI-JFET detector current vs. V_{GBS} with $V_{GTS} = 0$ V (a), and vs. V_{DS} with $V_{GTS} = 0$ V and $V_{GBS} = -6$ V (b).*

PI-JFET in the saturation range, see e.g. Fig. 5.1. Under saturation conditions a part of the channel at the drain side is pinched off and is completely depleted. The top-gate capacitance is mainly determined by depletion capacitance between the top gate and the nondepleted channel region. By increasing the bottom-gate reverse voltage, the depleted region at the drain side expands at the expense of the nondepleted part. As a consequence, the gate capacitance decreases. A similar phenomenon occurs when the drain-to-source voltage is varied, see Fig. 5.13b. In addition to a decrease of the top-gate capacitance, the decrease of the depletion capacitance of the drain region must now be taken into account.

In addition to the active detection caused by the piezoelectric effect in the PI-JFET, the piezoresistive effect must be considered. Since g_{mT} is proportional to μ_n, a modulation of the mobility is sensed in the detector current i_d. Measurements on PI-JFETs from above which the ZnO film was locally removed did not show an output signal. Therefore, no contribution from the piezoresistive effect is present in the measured detector current.

The influence of the capacitive coupling of the SAW to the drain electrode is shown in Fig. 5.14. Because of the passive detection mechanism, the control range is limited to 14 dB. With respect to this figure, it should be remembered that the total response is a vector addition of the passive and active responses. Therefore, the overall response can be lower than the passive or active responses separately.

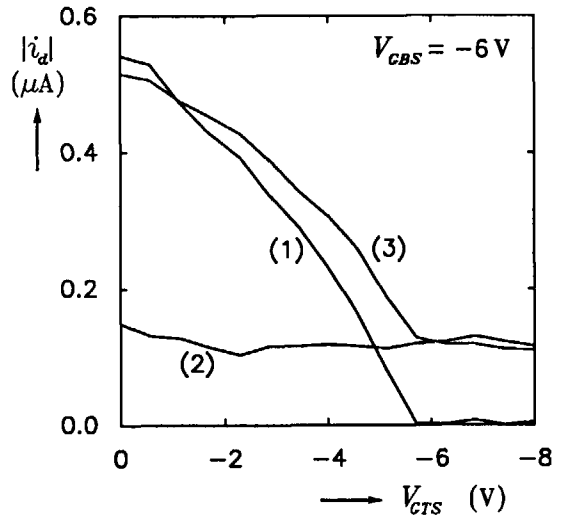


Figure 5.14: *Active (1), passive (2), and accumulated (3) detection responses of PI-JFET.*

The presented devices were designed to achieve a maximal top-gate voltage modulation. Therefore, the gate length L was designed to be half the wavelength. However, as was explained in section 5.3, this only maximizes the first detection stage of the PI-JFET, whereas the overall detection sensitivity is increased by decreasing the gate length as was shown in Eq. 5.14. If L is reduced, the internal cutoff frequency will in first instance increase sharply, since it is inversely proportional to L^2. For small gate lengths, the increase in f_T is reduced, because the sidewall capacitances become dominant. Cutoff frequencies into the GHz range are feasible. If, in addition, the capacitive loading on the top gate is prevented and the ZnO film quality is improved (see Chapter 6), an improvement in the power conversion efficiency of the PI-JFET of more than 25 dB is feasible.

5.5.4 Noise Measurements

Because the PI-JFET is current driven on a gate which is practically floating, the main noise source in the detector results from the thermal noise in the channel. This noise current source, measured at the output of the PI-JFET, is given by $i_n = \sqrt{4kTc_n g_{m0}}$ A/$\sqrt{\text{Hz}}$, in which c_n is a

constant which is about 0.66 [178]. If the induced gate noise is also taken into account, c_n increases to 0.78. In the worst case, a noise current at the detector output of $8\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ can be expected. For a reasonable noise measurement on a single PI-JFET, the noise figure of the measuring ($50\,\Omega$) system must be lower than 0.2 dB. No attempt was made to create such a system.

5.6 CONCLUSIONS

Although the results of the n-channel JFETs are quite reproducible, the strong dependence of the DC behavior on the epilayer thickness and impurity concentration is not advantageous. In particular, for applications in a programmable tapped delay line, where a large number of taps and a large area is involved, variations in the tap characteristics are unavoidable. However, for the PI-JFET detector any (standard) JFET process can be used, provided the SiO_2 layer thickness above the detector is kept small. With p-channel JFETs, the influence of the epilayer can be avoided, and characteristics can be obtained which are more reproducible [176]. However, for the high-frequency performance, no improvement must be expected because of the lower mobility of the holes in the p-channel.

In the PI-JFET design presented here, the capacitive coupling from the SAW to the top gate was optimized. The conversion efficiency is comparable to that of the piezoresistive FET and the PI-FET, however at a lower DC power dissipation of about 30 mW. Decreasing the gate length will improve the overall sensitivity of the Junction FET. Decreasing the gate width, while keeping the total acoustic input power constant, will not alter the efficiency. However, as a result of a reduction in I_{DSS}, a decrease of the DC power dissipation is achieved.

Chapter 6

FILTER ARCHITECTURE

6.1 INTRODUCTION

In the previous chapters, a detailed discussion of programmable SAW detectors was given. In this final chapter, the overall construction of a programmable filter is evaluated. The structure is based on the programmable tapped delay line which was introduced in Chapter 1 (see Fig. 1.3). This filter configuration can be divided into a generation part and a detection part. In the generation part, the electric input signal is converted into an acoustic wave. The SAW excitation is discussed in section 6.3. The detector part, in which the actual filter operation takes place, consists of an array of programmable taps. This part contains the junction taps presented in Chapters 4 and 5, and is considered in section 6.4. Finally, the last section of this chapter gives an overview of the electronic circuitry that must be added in order to obtain a dedicated, monolithic programmable filter. However, before discussing the separate parts of the filter, the wave propagation in the structure is examined. Since the propagation path comprises both the generation and detection parts, it is considered first.

6.2 SAW PROPAGATION PATH

Surface acoustic wave propagation in layered media is quite different from that in semi-infinite substrates. Firstly, the layered configuration behaves dispersively: the SAW velocity is a function of the frequency. In addition, the use of thin films like ZnO introduces extra propagation losses not

encountered in conventional substrates like quartz or lithium niobate. In the following discussion, Rayleigh-wave propagation in the ZnO-SiO_2-Si structure is considered for frequencies much lower than the relaxation frequency of the silicon substrate ($\omega \ll \omega_c$). In this case, the substrate can be considered perfectly conducting. The disturbances induced by the transducers and detectors are ignored, and the propagation path is assumed to be uniform.

6.2.1 Dispersion

The SAW phase velocity v_{ph} in the ZnO-SiO_2-Si layered structure depends on the normalized layer thicknesses. This effect is illustrated in the velocity curves shown in Fig. 6.1. In the calculations, a (100)[100] Si orientation has been assumed, and the material constants given in Table 2.1 have been used. Dispersion originates from the different elastic constants in the individual layers. At low ωh_{ZnO} values, the wavelength is much larger than the ZnO layer thickness, in which case the SAW power is mainly present in the silicon substrate (for the layered configurations in this work h_{ox} can be ignored). In this case, the velocity approaches the Rayleigh-wave phase velocity of silicon ($v_{ph,Si} = 4917\,\mathrm{m/s}$). For large ωh_{ZnO}, the wave motion is

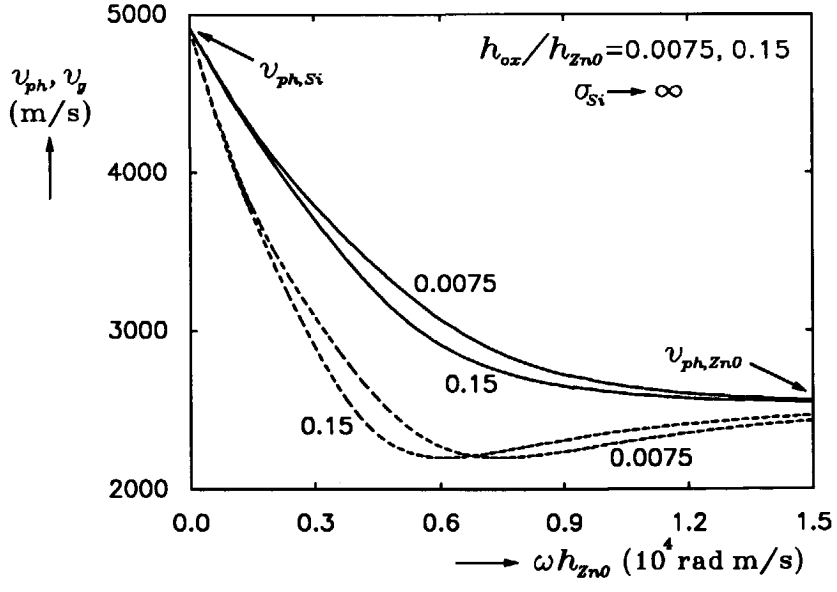


Figure 6.1: *SAW phase (solid) and group (dashed) velocity vs. ωh_{ZnO} for two different h_{ox}/h_{ZnO} ratios.*

mainly concentrated in the ZnO layer ($\lambda \ll h_{ZnO}$), and the velocity is determined by the elastic properties of the ZnO layer ($v_{ph,ZnO} = 2525\,\mathrm{m/s}$).

Dispersion deteriorates the filter performance, and causes signal distortion and intersymbol interference. However, undisturbed signal processing in a dispersive system can be achieved, provided the group velocity in the frequency band of interest is constant. The group velocity v_g is defined as

$$\frac{1}{v_g} = \frac{\partial k}{\partial \omega} = \frac{1}{v_{ph}} - \frac{\omega}{v_{ph}^2}\frac{\partial v_{ph}}{\partial \omega} \tag{6.1}$$

In Fig. 6.1 the group velocities are given by the dashed curves. For $\omega h_{ZnO} > 6000\,\mathrm{rad\,m/s}$, the group velocity is fairly constant, and an undisturbed, wideband signal processing can be achieved. In the following, optimal layer thicknesses are assumed, which provide a maximal coupling for junction structures at the filter center frequency ω_0: $\omega_0 h_{ZnO} \approx 8000\,\mathrm{rad\,m/s}$ and $\omega_0 h_{ox}$ is small ($\approx 60\,\mathrm{rad\,m/s}$), see sections 2.3 and 3.4. The variation in the relative change in the group delay $\partial\tau_g/\tau_g$ for different fractional bandwidths $\Delta\omega/\omega_0$ can be derived from Fig. 6.1 and is presented in Table 6.1. For example, in a PTDL with a center frequency

Table 6.1: *Fractional change in group delay for three different fractional bandwidths where $\omega_0 h_{ZnO} = 8000\,\mathrm{rad\,m/s}$ and $\omega_0 h_{ox} = 60\,\mathrm{rad\,m/s}$.*

$\Delta\omega/\omega_0$ (%)	$\partial\tau_g/\tau_g$ (%)
10	0.77
20	1.4
50	3.6

of 100 MHz and a bandwidth of 10 MHz, the variation in the group delay in a 10 mm propagation path is less than 35 ns. Thicker ZnO layers are attractive with respect to dispersion, but result in a lower piezoelectric coupling and higher propagation losses.

6.2.2 Higher-order Modes

In addition to the fundamental Rayleigh-wave mode, higher-order modes can exist in the layered configuration. Higher-order modes only occur above a certain value of ωh_{ZnO}. The fundamental ($R1$) and second-order ($R2$) pure Rayleigh-wave modes in the ZnO-SiO_2-Si configuration are shown in Fig. 6.2. For even larger ωh_{ZnO} values, the third- and higher-order modes appear. In the configuration under consideration, $R2$ seriously disturbs the filter operation, since a second pass band appears at

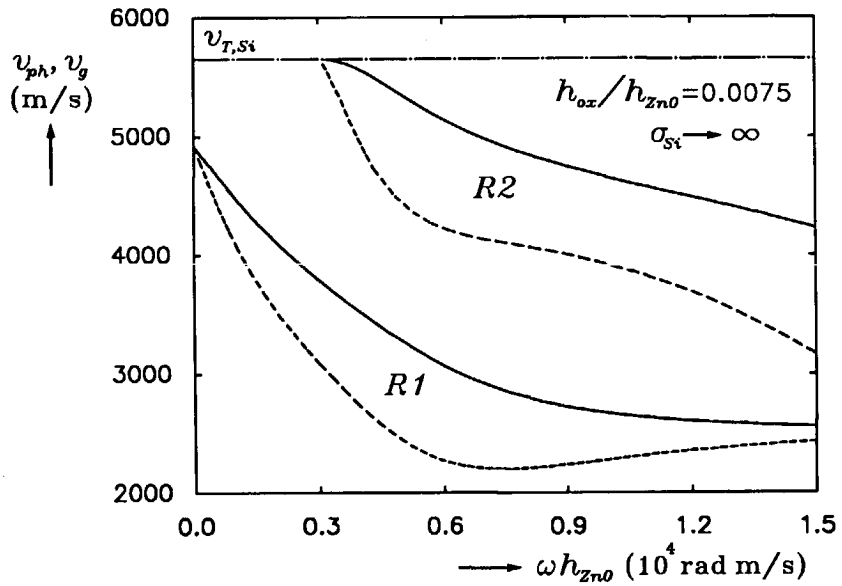


Figure 6.2: *The phase (solid) and group (dashed) velocities vs. ωh_{ZnO} for the Rayleigh-wave modes R1 and R2; $v_{T,Si}$ represents the transverse wave velocity in silicon.*

a frequency of about 1.7× the fundamental center frequency. Although the $\Delta v/v$ of $R2$ is about half of $R1$ [179], the coupling efficiency represented by the formula for the equivalent surface charge ρ_s^2/P_a (Eq. 2.25) is proportional to k ($k = \omega/v_{ph}$), and is, therefore, about the same for the fundamental and second-order mode. This was experimentally verified by measurements on the BMT and PI-JFET devices.

The second-order mode can only be avoided by limiting the ZnO layer thickness to $\omega h_{ZnO} < 3000$ rad m/s. However, this range is quite unattractive because of the low coupling and corresponding low efficiency. Whether the second-order mode can be allowed depends on the application. For matched filters, there seems to be no problem. Since the group velocity of $R2$ is about twice that of $R1$, the duration of its impulse response is divided by two and its bandwidth is doubled. Therefore, only the impulse response of the fundamental mode is matched to the waveform it was designed for. In programmable notch (bandstop) filters an extra notch appears at a higher frequency. Notch filters are usually applied to suppress strong CW interfering components in broadband signals (for example FM and Spread-Spectrum signals). Because the energy of the desired signal is spread over a wide frequency range, it has a high degree of redun-

dancy, and suppression of a small part of the spectrum by an extra notch will not be very harmful. For variable bandpass filters, the second-order mode is more serious. However, it will be shown in section 6.4 that the frequency response of an ordinary bandpass filter produces various pass bands, which are caused by the sampling process. The $R2$ mode will add extra pass bands, which results in a decrease of the programming range of the filter.

In addition to higher-order wave modes, bulk acoustic waves (BAW) may cause extra spurious bands. BAWs are generated by the launching transducer, and result from SAW scattering at discontinuities located in the propagation path. Because the BAW velocities are about twice as high as the SAW velocities, the BAWs generated by the transducer usually produce disturbances at much higher frequencies than the frequency range of interest. However, BAWs which originate from scattering have the same frequency as the original SAW, and may, therefore, disturb the filter pass band seriously.

6.2.3 Propagation Loss

As a result of internal losses in the solid, the SAW amplitude gradually decreases during propagation. For single crystal substrates, the dominant loss mechanisms are acoustic power leakage to the gas above the propagation surface ("air loading") and SAW interaction with thermal phonons. These effects are proportional to ω and ω^2, respectively, and only have to be taken into account at high frequencies (GHz range). For the ZnO-SiO_2-Si configuration, two loss mechanisms must be added: the acoustoelectric interaction with the mobile charge carriers in the semiconductor, and losses in the ZnO film. The SAW attenuation by mobile charge carriers was considered in Chapter 2, section 2.4.2. This mechanism becomes important when the SAW frequency approaches the silicon relaxation frequency ω_c. For the devices considered in this work, the operating frequencies and doping levels are such that this loss mechanism can be ignored.

The dominant loss in layered structures is encountered in the films. The loss depends on the relative thickness of the film and on its microstructure, and is generally much higher than the corresponding bulk counterpart. In the structure under consideration, the SiO_2 thickness is very small ($\omega h_{ox} < 60\,\mathrm{rad\,m/s}$), and its contribution can be ignored. The polycrystalline ZnO film produces the dominant loss factor. Much theoretical and experimental work on sputtered ZnO films was done by

Hickernell [180, 181, 182]. The sputtered ZnO film has a fiber-grain structure of aligned crystallites with their c-axes oriented perpendicular to the surface. Because 80% of the film loss is caused by shearing motion [181], poor boundary interconnections between the grains result in a high damping factor. In addition, it was found that defects in the film cause wave scattering, and play an important role in the propagation loss. The SAW attenuation in ZnO films appears to be proportional to ω^2. In general, the loss in the ZnO film depends on the film quality, which is in its turn dependent on the sputtering conditions and on the type of substrate. With high-quality, DC sputtered ZnO layers, damping factors of less than 1 dB/μs at 100 MHz were reported [183].

Propagation loss can simply be compensated by an appropriate adjustment of the tap weight factors. However, it places an upper limit to the maximal achievable insertion loss to one tap, and, therefore, on the dynamic range of the filter. Therefore, the losses must be kept to a minimum.

6.2.4 Diffraction and Beam Steering

As a result of the finite aperture of the SAW generating transducer, the width of the wavefront broadens as the distance to the transducer increases. This is known as diffraction. Diffraction phenomena depend on the anisotropy of the substrate material. In considering diffraction effects, a near-field and a far-field region can be distinguished. If the distance between the transmitter and detector is much smaller than the Fresnel distance d_f, the near-field approximation can be used and diffraction phenomena can be ignored. The Fresnel distance for semi-infinite substrates is defined as [184]

$$d_f = \frac{W^2 k}{8\pi(1 + \partial\varphi/\partial\theta)\cos\theta} \tag{6.2}$$

where θ relates the propagation direction to the crystal orientation, and φ is the "walk-off" angle between the propagation vector $\underline{k}$ and power flow direction. For the layered configuration, both the anisotropy of the ZnO layer and of the silicon substrate must be taken into account. The ZnO layer, which contains most of the SAW energy, is transverse isotropic, which involves $\partial\varphi/\partial\theta = 0$. In addition, the propagation path in the experimental devices was aligned along the [100] axis in the (100) Si substrate, which involves $\theta = 0$ and $\varphi = 0$, and gives a pure Rayleigh-wave propagation. Therefore, Eq. 6.2 gives a good approximation of the Fresnel distance in the layered structure, provided θ and $\partial\varphi/\partial\theta$ are set to zero.

In Chapters 4 and 5, it was derived that for an optimal efficiency in the BMTs and the PI-JFETs, it is desirable to keep the detector width W as small as possible. Equation 6.2 puts a lower limit to W for a certain propagation path length. A further decrease can be accomplished by using waveguides. For the PTDL, waveguides are quite attractive because of the shrinking dimensions of the programmable detectors and the increase of the SAW power per unit width. An overview of SAW waveguides is given by Oliner [185]. The SAW power is strongly confined to the waveguide when the phase velocity in the guide is much smaller than that of the environment. In the ZnO-SiO_2-Si configuration, a slot waveguide can be made by using a thin SiO_2 layer in the propagation path and a thick SiO_2 layer in the surroundings. This is compatible with the thin SiO_2 layer requirements above the junction structures. Because of the short-circuiting effect of the conductive silicon, the material in the slot is unstiffened, and a decrease in the phase velocity results. However, the slot waveguides only weakly confines the SAW power to the guide. A stronger confinement is achieved in a ridge waveguide. This waveguide can be made by etching away all the ZnO but for a small ridge [186]. The velocity in the ZnO ridge is much smaller than that of the environment. However, this type of waveguide shows stronger dispersion behavior than the slot waveguide.

Anisotropic materials can exhibit beam steering. In this case, the propagation vector $\underline{k}$ does not coincide with the Poynting vector which is associated with the power flow direction. As a result, the waves are launched at an oblique angle from the transmitting transducer. By definition, beam steering is zero in the pure mode directions. Both beam steering and diffraction cause a gradual loss of the detected signal power, and add in this respect to the propagation loss. A proper alignment of the propagation direction on the crystal orientation minimizes diffraction and beam steering phenomena. For the (100) silicon substrate, this means an accurate alignment of the transducers and the detectors on the [100] direction. This is accomplished by a mask alignment on the wafer flat. However, because of the imperfections in the flat alignment itself, only a limited accuracy can be achieved.

6.2.5 Secondary Effects

(i) Layer thickness variations

In the above discussion, it was assumed that the ZnO and SiO_2 layer thicknesses are uniform both in the x_1- and x_2-directions. However, this is an ideal situation. In practice, the layer thicknesses have a tapering along

and normal to the propagation direction. As a result, the SAW phase velocity is not constant in the propagation path. This can have serious effects on the phase relations within the filter structure. The sensitivity of the phase velocity for variations in the layer thicknesses is represented by

$$\frac{\partial v_{ph}}{v_{ph}} = S \frac{\partial h}{h} \tag{6.3}$$

where S is the sensitivity factor, and h the layer thickness of the ZnO or SiO_2 layer. The sensitivity factor S_{ZnO}, related to the variations in h_{ZnO}, can be derived from the velocity curves vs. ωh_{ZnO} for constant ωh_{ox}, and is depicted in Fig. 6.3. For the propagation medium under consideration ($\omega h_{ZnO} = 8000\,\text{rad m/s}$; $\omega h_{ox} = 60\,\text{rad m/s}$), a value of $S_{ZnO} \approx -0.27$ results. A similar procedure can be applied to find the

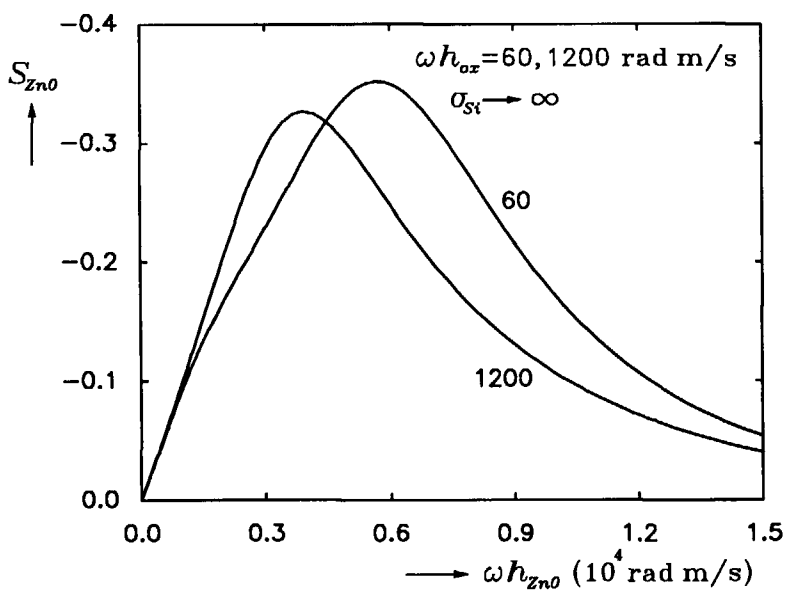


Figure 6.3: *Sensitivity factor S_{ZnO} vs. ωh_{ZnO} for two different values of ωh_{ox}.*

sensitivity factor S_{ox} related to the SiO_2 layer. However, since the applied SiO_2 layer thicknesses are much smaller than that of the ZnO layer, the resulting S_{ox} is at least an order of magnitude smaller than S_{ZnO}. In addition, the SiO_2 thickness can be fabricated more uniformly than the ZnO layer, and its effect on v_{ph} can, therefore, be ignored.

The tapering in the ZnO layer thickness affects the phase relations in the propagation path. This is most conveniently expressed in the frac-

tional change of the phase delay $\partial\tau_{ph}/\tau_{ph}$. For a thickness taper in the propagation direction, the SAW velocity gradually increases or decreases during propagation. As a result, there is a nonlinear rise or fall in τ_{ph}. Assuming a normalized taper α_1 (m^{-1}) ($\alpha_1 = \partial h_{ZnO}/h_{ZnO}$ per unit length in the x_1-direction), it can be calculated by integration along the propagation path that the fractional delay change becomes

$$\begin{aligned}\frac{\partial\tau_{ph}}{\tau_{ph}} &= -1 + \frac{1}{\alpha_1 S_{ZnO} v_{ph} \tau_{ph}} \ln(1 + \alpha_1 S_{ZnO} v_{ph} \tau_{ph}) \\ &\approx -\frac{1}{2}\alpha_1 S_{ZnO} v_{ph} \tau_{ph} \qquad (6.4)\end{aligned}$$

The latter approximation is valid, provided that $\alpha_1 S_{ZnO} v_{ph} \tau_{ph} \ll 1$. A ZnO thickness taper normal to the propagation direction results in a nonuniform phase along the wavefront. Assuming a normalized taper per unit length α_2 (m^{-1}) in the x_2-direction, the fractional delay change becomes

$$\frac{\partial\tau_{ph}}{\tau_{ph}} = \alpha_2 S_{ZnO} w \qquad (6.5)$$

where w is the distance in the x_2-direction.

The relations given in Eqs. 6.4 and 6.5 put stringent requirements on the thickness uniformity of the ZnO layer. An example is given for a SAW at 100 MHz with $v_{ph} = 3000\,m/s$. A propagation path is assumed of length 10 mm and width 2 mm, and a sensitivity factor of $S_{ZnO} = -0.27$. If a phase accuracy of 10 degrees is required, both between the beginning and end of the path, and in the wavefront at the end of the path, the maximal tapering values are $\alpha_1 < 0.062\,m^{-1}$ and $\alpha_2 < 0.15\,m^{-1}$. As a consequence, the allowable thickness variation between beginning and end is only 0.062%, whereas in the normal direction only 0.03% is allowed. In the experimental devices the α-values of the ZnO layer were measured with a Tencor alpha-step 200. For nominal thicknesses between 5 and 8 μm, α-values were found of $\alpha_1 \approx 1.7\,m^{-1}$ and $\alpha_2 \approx 4.0\,m^{-1}$. It is believed that these rather high values are caused by the ZnO patterning. The ZnO was sputtered through a stainless-steel sputter mask, in order to obtain a well-defined propagation path, and leaving the peripheral electronics and bonding pads free of ZnO. The mask opening was 1.9×11 mm. The tapering may be caused by shadowing effects, which result in a nonuniform growth rate of the ZnO. It is believed that a much better result can be achieved by growing ZnO on the entire wafer first, and etching the ZnO afterwards. ZnO etching techniques are described in Reference [187], but were not applied in the device processing presented in this work.

(ii) Temperature sensitivity

A final item discussed here concerns the temperature sensitivity of the SAW velocity. The material constants depend on temperature, and a temperature sensitivity of the SAW velocity must be expected. Temperature effects in ZnO-SiO_2-Si layered structures were investigated by Ono *et al.* [188]. Since the SiO_2 has a negative temperature coefficient (TC), whereas the TCs of Si and ZnO are positive, a zero TC of the velocity can be obtained when the layer thicknesses are chosen properly. In the junction devices considered in this work, the SiO_2 layer must be very thin, and only at very high frequencies can the required value of $\omega h_{ox} \approx 1600$ rad m/s be reached. For practical devices with the (100)[100] Si orientation, the worst-case TC of the phase and group velocity is about −25 ppm/°C [188].

6.3 GENERATION PART

At the input of the PTDL, the incoming electric signal is converted into an acoustic equivalent. For the transduction from the electrical into the acoustical domain, the two dominant parameters are the conversion efficiency and the bandwidth. To obtain a large dynamic range in the filter, transducer losses must be minimized. In addition, the bandwidth of the transducer must be equal to or larger than the bandwidth of the filter characteristic, which is realized in the detection part. Close to the resonance frequency f_0, a SAW transducer can conveniently be represented by the equivalent circuit model shown in Fig. 6.4. Ignoring resistive losses and the imaginary term in the radiation admittance, the model consists of the static transducer capacitance C_T in parallel to a radiation conductance G_a. The power dissipated in G_a represents the acoustic power of the generated waves.

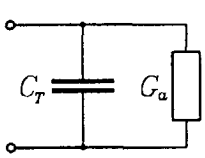


Figure 6.4: *Equivalent network circuit of the interdigital transducer close to the resonance frequency* f_0.

Assuming a fixed available power of the driving source at the input port of the PTDL, the conversion of electric into acoustic power is most efficient when the transducer admittance is matched to the internal output

admittance of the driving source. The IDT and driving source then make a parallel resonating network, the quality factor Q_e of which is proportional to C_T. Since the fractional bandwidth of this network is inversely proportional to Q_e, a wideband signal processing requires a C_T as low as possible. Regeneration phenomena at the transmitting transducer are of minor importance for two reasons: 1. signal distortion is small because of the wide bandwidth of the transducer, 2. triple-transit reflections are sufficiently suppressed by the low reflection coefficient of the detection part.

For a wideband excitation of SAWs, two transducer implementations can be used: the Interdigital Transducer (IDT) and the Edge-Bonded Transducer (EBT). The IDT was introduced in Chapter 1. This transducer type is most compatible with the monolithic technology used for the PTDLs which are described in this thesis. The IDT is examined in more detail in the next section. The EBT consists of a slab of piezoelectric material which is bonded at the edge of the propagation medium [189]. The advantages of the EBT are the high conversion efficiency combined with a wide bandwidth, and the low electromagnetic feedthrough [190]. However, from a technological point of view, the EBT is less attractive, and is not very suitable for monolithic integration.

6.3.1 Conventional IDT

A conventional IDT consists of a metal comb structure, see Fig. 1.2. In the PTDLs presented in this thesis, the metal pattern is placed at the ZnO-SiO_2 interface in order to obtain the highest efficiency attainable in the layered structure, and in order to postpone the ZnO deposition till the final process step. Important factors in the transducer design are the ID period p_{idt} which fixes the resonance frequency, the number of finger pairs N, and the aperture W. The number of finger pairs N determines the acoustic bandwidth $\Delta\omega_a$ of the IDT

$$\frac{\Delta\omega_a}{\omega_0} = \frac{1}{N}\frac{v_g}{v_{ph}} \tag{6.6}$$

Since the IDT is a bidirectional device, the conversion loss is minimally -3 dB. However, in practice, the conversion losses are much higher because of mismatching. The radiation conductance of the transducer is proportional to W, N^2 and the piezoelectric coupling [191]. The source impedance of the driving load is usually quite small in order to provide an available power which is as high as possible and a wide electric bandwidth. For a wide acoustic bandwidth, the number of finger pairs is limited and

exorbitant wide apertures would be required to match the IDT to the source impedance. Therefore, in practical implementations, a mismatch must be accepted, which deteriorates the conversion efficiency. The conversion efficiency and acoustic bandwidth place opposite requirements on the number finger pairs N, and in practice, a compromise must be found. For ZnO transducers, the transducer admittance is mainly capacitive. A low capacitance is required to minimize the bandwidth-limiting effect determined by Q_e, and to keep the driving currents as small as possible. If no tuning is applied, the static transducer capacitance will limit the bandwidth of the driving electronics.

A problem in monolithically integrated SAW devices is the electromagnetic feedthrough between launching and receiving transducers. Visser *et al.* [192] showed that the conductive silicon substrate is the main cause of this feedthrough. It can be suppressed by symmetrically driving the IDT, and by grounding the substrate. In addition, a highly doped (grounded) layer, directly underneath the IDT, can further decrease the feedthrough [193].

The IDTs used in this work have 16 periods and an aperture of 1.7 mm. Two different periods of 32 and 28 μm result in operating frequencies of about 95 and 115 MHz, respectively. The fractional bandwidth is 5% and the conversion efficiency is typically −25 dB for a 50 Ω source impedance. The low efficiency can be attributed to the low piezoelectric coupling, caused by the nonoptimal ZnO layer thicknesses which are between $\omega h_{ZnO} = 3600$ and 4800 rad m/s.

The static capacitance C_T of the IDT under consideration is mainly determined by the capacitance between the electrodes via the conductive silicon substrate. To keep the capacitance to the substrate as small as possible, a thick SiO_2 layer is required directly underneath the IDT. In Fig. 3.4, it was shown that the coupling strength $\Delta v/v$ of a passive transducer at the ZnO-SiO_2 interface increases with increasing ωh_{ox}. However, the junction detectors in the detection part require a thin SiO_2 layer thickness as was illustrated in Fig. 3.9. As a consequence, the thickness requirements, imposed on the SiO_2 layer by the generation and the detection parts, are in contradiction. In the devices described in this work, a thick SiO_2 layer of about 2 μm is used underneath the IDTs employed for SAW excitation, whereas in the detection part where the BMTs and PI-JFETs are located, a thin SiO_2 layer of 0.1 μm is used. This nonuniformity in h_{ox} in the SAW propagation path has several detrimental effects. The step in the layered structure introduces reflections and causes bulk wave generation. In the fabricated devices an interfering wave was observed, with

a group velocity which was 1.5 times as high as the Rayleigh-wave group velocity. In some of the devices, this wave was only 15 dB below the main wave. After experiments using a wave-absorbing material in the propagation path, the interfering wave was identified as a BAW. It is believed that this BAW results from wave scattering at the oxide step. Since the frequency of the scattered BAW corresponds to the frequency of the main SAW, its influence will be observable in the filter characteristic. Another disadvantage of the thickness nonuniformity is related to dispersion. In Fig. 6.1 it is seen that the phase and group velocities depend on ωh_{ox}. In Fig. 6.1, the curves are shown for $h_{ox}/h_{ZnO} = 0.0075$ and 0.15 rad m/s, which corresponds to $h_{ox} = 0.1$ and 2 μm for the optimal ZnO thickness of 12 μm at 100 MHz. At $\omega h_{ZnO} = 8000$ rad m/s the phase velocity difference between the thin- and thick-oxide regions is about 4%. To match the resonance frequencies of the generation and detection parts, adjustment of the period of the IDT or the tapped array in the design stage is required. The adjustment depends on the ultimate SiO_2 and ZnO layer thicknesses.

The most far-reaching consequence of the change in SiO_2 thickness is the nonuniform growth of the ZnO. The quality of the sputtered ZnO layers is influenced by the underlying substrate [181, 194]. Other parameters that affect the ZnO growth are the substrate temperature, the sputtering gas pressure and the growth rate. In addition, the sputter method and installation greatly influence the process. For the devices presented in this thesis, a fixed sputter recipe was adopted as described in section 4.5. This recipe provided high-quality ZnO films on the 2 μm thick SiO_2 region, but a poor and hazy film on the thin SiO_2 regions. The SEM photograph in Fig. 6.5 clearly shows a rough surface and grainy film in the thin-oxide region. X-ray diffraction analysis revealed a standard deviation angle in the c-axis normal orientation, which was about twice as high (±6 degrees) as in the thick-oxide region (±3 degrees). In addition, the ZnO layer on the thin-oxide region contained more random oriented crystals. A possible explanation for the observed texture deviations might be the difference in heat conductivity which occurs in the thick-oxide regions and in the thin-oxide regions. Therefore, the substrate temperature under sputter conditions changes locally and affects the polarity of the ZnO fiber grains [195]. The orientation of the underlying substrate also influences the ZnO growth [194], and this may also contribute to the observed differences in the film quality. Further research is required to find the optimal sputter parameters to obtain high-quality films on thin SiO_2 layers. However, finding optimal parameters that produce high-quality films on both the thick- and thin-oxide regions is very unlikely.

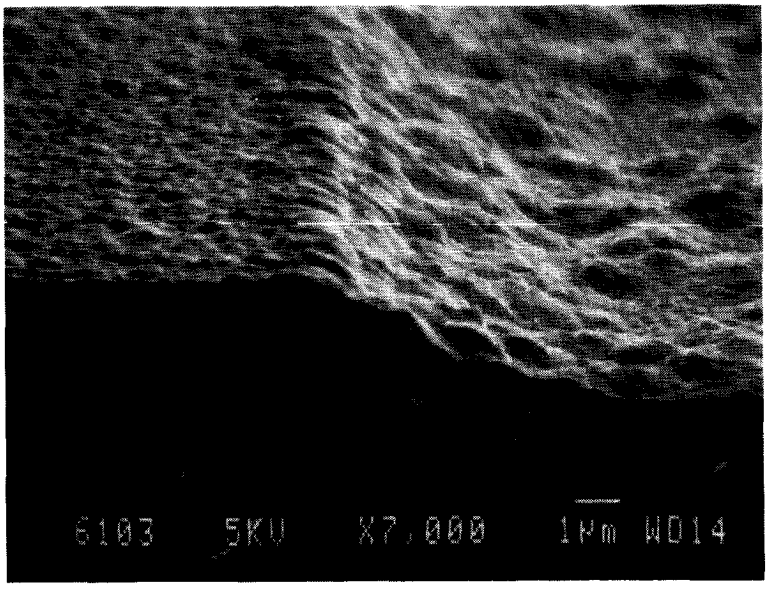


Figure 6.5: *SEM photograph showing the SiO_2 step. Note differences in ZnO texture on the thick-oxide region (left) and the thin-oxide region (right).*

The film quality determines the piezoelectric coupling factor and the propagation loss. In the measured devices, it can be expected that the coupling strength in the detection part, which is covered with the hazy film, will be much lower than in the generation part.

6.3.2 Combined Junction-Metal IDT

Because of the requirement of a thick SiO_2 layer underneath the conventional IDT, this transducer type is not attractive for implementation in a PTDL with active junction detectors. Therefore, a new transducer is introduced, which is compatible with the junction detectors, and which does not require a thick SiO_2 layer.

In section 3.4.2, passive junction transducers were described, consisting of reverse-biased *pn* electrodes at the silicon surface. At high frequencies, these structures become very inefficient because of the high series resistance of the junction electrodes. A new transducer configuration is presented which is a combination of a junction IDT located at the silicon surface and a conventional metal IDT located at the ZnO-SiO_2 interface. In Fig. 6.6, a cross section of this *Junction-Metal IDT* (JMIDT)

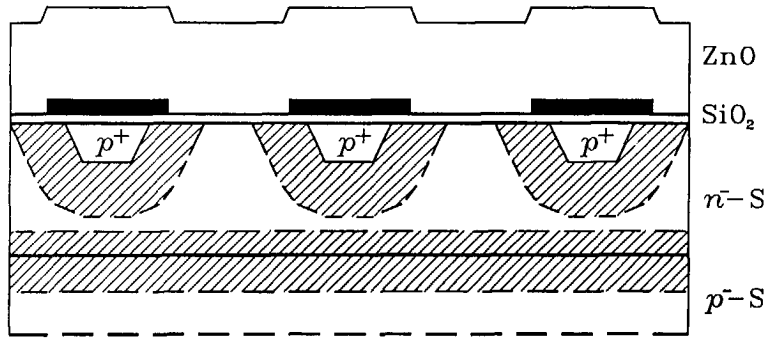


Figure 6.6: *Cross section of the Junction-Metal IDT (the hatched areas represent depleted regions).*

is shown. The metal pattern actually forms the low-loss transducer exciting the SAWs. The ID junction pattern does not contribute to the SAW generation, but by reverse-biasing the *pn* electrodes with respect to the substrate, a thick depletion region is created underneath the metal pattern. In this way, short-circuiting of the RF fields by the conductive silicon is prevented. Because the depletion region creates a thick dielectric layer, the SiO_2 layer can be very thin. Since the junction electrodes do not carry RF or DC currents, the series resistance is of no importance. A device similar to the JMIDT is used for SAW excitation in GaAs [196]. In this case no oxides are used: the metal IDT is directly placed on the weakly piezoelectric GaAs. The reverse-biased Schottky contact between the metal and the semiconductor provides the required depletion region.

By using the JMIDT, a dielectric layer underneath the transducer can be obtained which is much thicker than can be achieved with oxides. If an epilayer is applied, it can both be depleted from above by the junction IDT, and from below by the epi-substrate junction. Using this structure, the epilayer can completely be depleted, and a dielectric layer of $5\,\mu$m thickness or even more can be achieved. As a result, the capacitance of the JMIDT will be much smaller than that of the conventional IDT, and a higher degree of isolation from the conductive substrate is obtained, which will suppress the EM feedthrough.

The JMIDT appears to be a promising transducer to excite SAWs in a PTDL using junction detectors. It provides a flat and uniform propagation path on which the growth of high-quality ZnO films is feasible. The realization of this transducer is the subject of current research. At the time of completion of this thesis, no experimental results were yet available.

6.4 DETECTION PART

The detection part of the PTDL consists of an array of programmable SAW detectors which are connected in parallel to a common summing bus. Since the actual filtering takes place in this part, deteriorating effects like reflections, and influences from controlling and loading circuitry must be suppressed as much as possible. How this can be achieved with active junction detectors, of which the BMT and PI JFET are two examples, was discussed in Chapter 3. In this section, the construction and operation of an array of programmable taps is considered.

6.4.1 The Array Factor

The detection array fixes the filter characteristic of the PTDL. The most important parameters are the bandwidth B, and the impulse duration T. The time-bandwidth product TB is a general figure of merit of a filter, and expresses the measure of complexity of its impulse response. The bandwidth of the complete PTDL is determined by three factors: by the bandwidth of the input IDT, the bandwidth of the programmable tap, and by the bandwidth of the array itself. The bandwidths of the IDT and the taps are determined by their dimensions along the propagation direction. Since the array factor forms the desirable filter characteristic, the bandwidths of the IDT and tap must be larger than the bandwidth of the array. The bandwidth of the array is determined by the pitch p_{tap} between the detectors. Since the detection array forms a sampling system with a sampling rate f_s of

$$f_s = \frac{v_g}{p_{tap}} \tag{6.7}$$

the frequency characteristic is repetitive. In order to avoid aliasing, a maximum bandwidth of half the sampling rate can be allowed. The time duration T of the impulse response is determined by the length of the array

$$T = N\frac{p_{tap}}{v_g} \tag{6.8}$$

in which N is the number of taps. From Eqs. 6.7 and 6.8, it can be derived that the TB-product equals half the number of taps.

The array factor is determined by the weight factors of the individual taps. For three different applications the array factor is examined more closely.

(i) Bandpass filter

In a programmable bandpass filter, two parameters can be varied: the width of the pass band, and the center frequency. The width of the pass band is inversely proportional to the impulse duration, which can be varied by switching on or off more taps. The minimal bandwidth is obtained when all taps are in the on-status, and is inversely proportional to T given in Eq. 6.8. The center frequency can be varied by applying a weight sequence to the taps with a sinusoidal waveform. This is explained in the time and the frequency domain in Fig. 6.7, where $\bullet$ means multiplication, and $*$ means convolution. As a result of the sinusoidal weighting of the array tap factors, the pass bands split, and can be shifted by varying the period of the weighting sequence. From Fig. 6.7, it can be derived that the frequency range over which the pass band can be shifted without aliasing effects is $0.5f_s$. The deteriorating effect from the second-order Rayleigh-

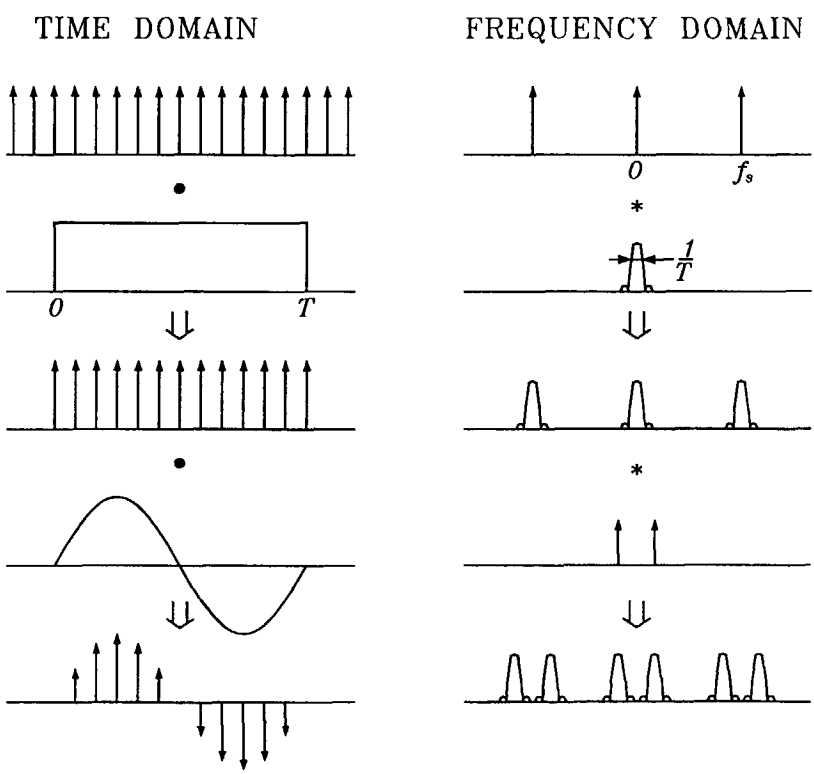


Figure 6.7: *Operation of array factor both in the time (left) and the frequency domain (right).*

wave mode $R2$ can also be examined. Since the group velocity of $R2$ is about $1.8\times$ higher than of $R1$, there is a correspondingly higher sampling rate. In addition to pass bands centered around $f_s, 2f_2 \ldots$, pass bands centered around $1.8f_s, 3.6f_s \ldots$ emerge. Because of the second mode, the frequency range of the fundamental pass band reduces to approximately $0.28f_s$.

(ii) Bandstop filter

The array factor of the bandstop filter is very similar to that of the bandpass filter. The weight factor of the tap in the center of the array is maximized. Using the remaining taps, a certain pass band is created by employing the techniques described before. The total insertion loss (IL) of the pass band is matched to the IL of the single tap in the center of the array. A bandstop characteristic results by subtracting the bandpass characteristic from the wideband characteristic of the single (central) tap. The dynamic range and notch depth of this filter are dominated by the IL of a single tap. Therefore, low losses are required.

(iii) BPSK matched filter

Phase-shift keying is a general, digital modulation technique. In binary-phase-shift keying (BPSK), the phase of a CW signal is switched to 0 or 180 degrees according to a certain digital sequence. PTDLs can be applied as BPSK matched filters by using tap weight factors of uniform amplitude, but with polarities which correspond to the digital code to be detected. The bandwidth of the BPSK signal is determined by the chip rate of the digital sequence. In the PTDL the inter-tap delay is identical to the chip duration. The processing gain of this filter is twice the TB-bandwidth product and amounts to N, the number of taps (and number of chips in the code sequence).

6.4.2 Dual-Track Configuration

The dual track has been mentioned several times as a means to suppress distortional effects, and to obtain phase weighting. Basically, the dual-track technique involves a splitting of the detection array into two parallel paths, see Fig. 6.8. Each path contains an identical array of programmable taps connected to a common summing bus. By subtracting the output signals of the two tracks, a balanced configuration results, which suppresses common-mode signals such as EM feedthrough, bulk waves, and signals

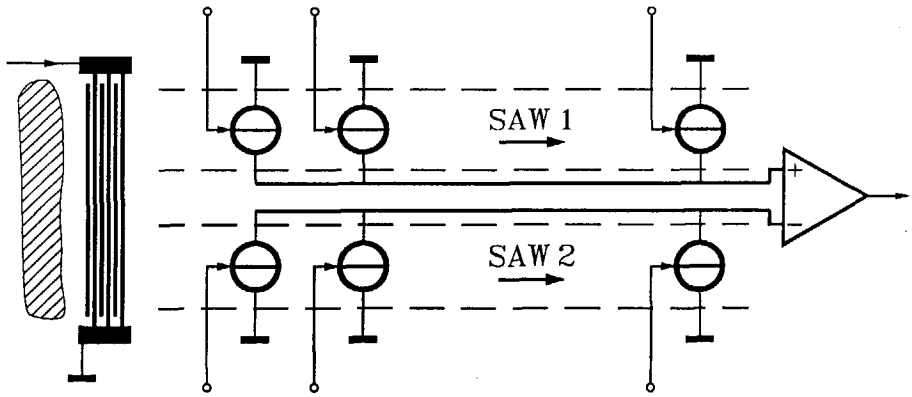


Figure 6.8: *Dual-track configuration of the detection part for common-mode rejection and bipolar tap weight factors.*

induced by the passive detection mechanism in active taps [190]. These deteriorating signals determine the residual output signal when the tap is in the off-status. If these residual signals on the two summing lines are indicated by s^+ and s^-, the balance B_{tr} in the dual-track structure becomes

$$B_{tr} = \frac{s^+ + s^-}{s^+ - s^-} \tag{6.9}$$

If the on-off ratio of a single tap is given by η_s, the on-off ratio in the dual-track configuration η_d is

$$\eta_d = \frac{\eta_s - 1}{2} B_{tr} \tag{6.10}$$

The dual-track array can be considered as a single array of taps, in which each tap is composed of two SAW detectors. When the locations of the detectors in the two tracks are identical, their output signals are identical apart from a phase reversal. This allows a limited phase control, i.e. the tap signal can be switched to either 0 or 180 degrees by switching on or off the corresponding SAW detector in one of the tracks. In this way, a bipolar weighting can be achieved in detectors in which only the magnitude is controlled (unipolar devices).

It should be noted that the cancellation effect of the dual-track structure works satisfactorily, provided the conditions in the detectors in the two tracks are identical. When different bias signals are applied to obtain a certain tap weight factor, the impedance levels in the detectors change

and the system is no longer symmetric, and the rejection becomes less effective. However, then the final output magnitude of the tap is also larger, and the interfering signals are less harmful. From a technological point of view, it is important to place the summing lines in the center of the two acoustic tracks, as is indicated in Fig. 6.8. In this way, the control leads from the peripheral electronics to the detectors do not cross the RF leads of the summing lines.

6.4.3 Detection Array of Active Detectors

The performance of the PTDL is dominated by the type of programmable SAW detector applied in the detection array. For these detectors, several devices can be used. To compare the different configurations, the conversion efficiency alone is not sufficient, since it does not reveal the DC power dissipation in the detector. Therefore, a new figure of merit F_p (W^{-1}) is introduced which is a bilinearity factor similar to the one used in the parametric detector

$$F_p = \frac{P_e^o}{P_a^i P_e^{aux}} \tag{6.11}$$

where P_e^o is the electric RF power dissipated in the load, P_a^i is the acoustic RF power incident on the detector, and P_e^{aux} is the electric DC power supplied by the auxiliary power source. In Table 6.2, the bilinearity factors for three different active detector types are given. They were determined at 100 MHz, and measured untuned on a 50 Ω load impedance. The figure

Table 6.2: *Bilinearity factors of three different active SAW detectors, measured at 100 MHz, untuned on a 50 Ω load.*

detector	F_p in W^{-1}
Piezoresisitive MOSFET	$1\text{–}4 \cdot 10^{-5}$
Barrier-Modulated Tap	$2\text{–}4 \cdot 10^{-4}$
Piezoelectric JFET	$7\text{–}9 \cdot 10^{-4}$

for the MOSFET was derived from Hickernell [193] and Defranould [197], whereas the figures for the BMT and PI-JFET were derived from Fig. 4.22 and Fig. 5.12, respectively. For the PI-FET, no definite figure could be derived from literature. However, its performance is worse than that of the piezoelectric MOSFET, see e.g. Reference [198]. It is believed that by optimizing the design (for example a shrinkage of the device dimensions)

and fabrication techniques (ZnO sputtering), the bilinearity factors of the BMT and the PI-JFET can be improved by more than a factor 10. For further details, the reader is referred to Chapters 4 and 5. In conclusion it can be stated that by using the newly presented active junction detectors, conversion efficiencies can be obtained which are comparable to those of former active detectors described in literature, but which have 10 to 100 times less DC power dissipation!

(i) Array of BMTs

The maximal bandwidth of the PTDL is determined by the pitch p_{tap} of the tap array. This pitch is limited by the dimensions of the detector along the SAW propagation direction. The BMT dimensions along the propagation path are mainly determined by the length of the source and drain electrodes. Since the sheet resistivity of the implanted electrodes is relatively high ($30\,\Omega/\square$), the length of these junction electrodes cannot be made too small with respect to their width (aperture), otherwise the losses caused by the series resistances become unacceptably high. Another point of concern is the passive detection. For a single detector, it is minimized when the electrode length equals one wavelength, resulting in a total tap pitch of at least 3λ. If the balancing in the dual-track configuration sufficiently rejects the passive detection mechanism, the requirements on the electrode lengths can be relaxed. Apart from the dimensions of a single detector, the region between adjoining detectors must be considered. A certain spacing is required for inter-tap isolation: reach-through between adjoining detectors must be avoided. An extra n^+ implantation in the isolation region can further suppress a parasitic reach-through current. Finally, the control circuitry must be considered. If a considerable amount of electronics is required per tap, sufficient space in the design is required to accommodate these circuits. However, with the continually shrinking dimensions of electronic components, this aspect will not seriously limit the inter-tap spacing. For a PTDL in the ZnO-SiO_2-Si configuration with a minimum pitch of 3λ, $\lambda = 30\,\mu$m ($f_0 \approx 100$ MHz), the bandwidth is about 16 MHz and a 128-tap array comprises 12 mm propagation path.

In Chapter 4, it was shown that the output signal of the BMTs is controlled by the biased drain current. Although for RF signals the taps are connected in parallel, this is not the case for the DC currents, since the individual tap weighting requires a separate control of each tap. A proper separation between the RF output and DC control signals must, therefore, be found. In the measurements given in Chapter 4, this was achieved by using a coupling capacitance. However, with respect to a

complete monolithic integration, this solution is not adequate. Since the output impedance of the BMT is not very high because of the triode-like characteristics, a rather large coupling capacitance is needed, which is difficult to realize in IC technology. Therefore, a circuit as shown in Fig. 6.9 must be used. All BMT drains are connected to the common drain line,

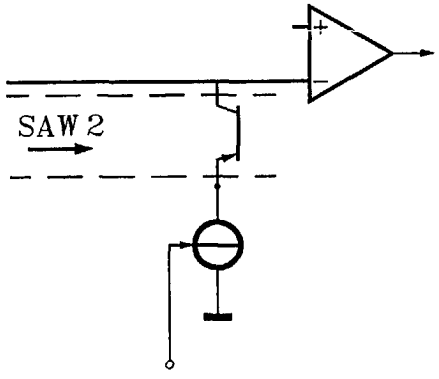


Figure 6.9: *Current control of BMT placed in an array.*

which is held at a fixed reverse voltage. Current sources at the source side provide the bias currents, and a separate control results. A disadvantage is the reduced efficiency of the BMTs as a result of the impedance level at the BMT source. The RF impedance at the source should be as small as possible in order to minimize the effect of the shunting feedback conductance in the BMT. This can be accomplished by increasing the source-to-epi capacitance and the output capacitance of the control current source. Since the output impedance of the BMT depends on the bias current, the impedance level seen at the common drain line depends on the weight function. The load impedance should, therefore, be as small as possible in order to avoid changing impedance conditions on the drain line caused by the tap control. Since the load impedance is formed by the input impedance of a differential amplifier as shown in Fig. 6.8, a current-sensing amplifier is preferred.

The photograph of an experimental 16-tap PTDL, to be applied as a BPSK matched filter, is shown in Fig. 6.10. It is the lower part of the total chip shown in Fig. 4.16. It is the first programmable SAW filter using active, piezoelectric detectors ever presented. A conventional IDT with $p_{idt} = 28\,\mu$m placed on a $2\,\mu$m thick SiO_2 layer is located on the left. The different texture of the ZnO layer on the thick and thin SiO_2 regions, and on the aluminum summing bus is clearly visible. The center frequency

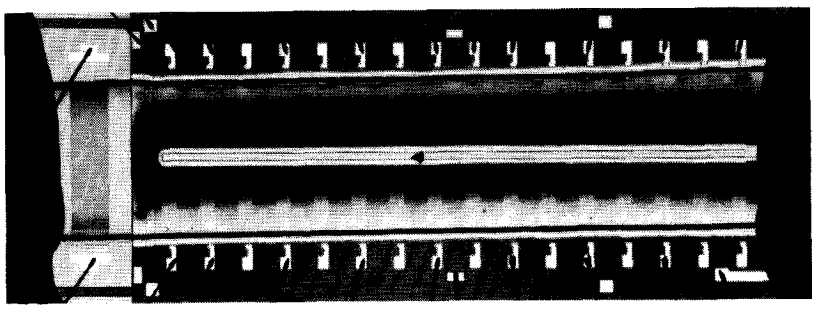


Figure 6.10: *Photograph of the experimental PTDL.*

is about 115 MHz, and the 16 finger-pair IDT provides a bandwidth of about 5 MHz, which corresponds to the sampling rate of the taps. Two tracks of BMTs are implemented, however, there is only one drain line present. The BMTs have an aperture of 500 μm and a gap length of 5 μm, whereas the electrode lengths are 3λ. DC measurements indicate a good uniformity in the characteristics of the detectors along the detection array. The common drain line is fixed at a voltage of −15 V. Figure 6.11 shows a time domain measurement on a 50 Ω system when the even-numbered detectors in a single track are sequentially turned on by grounding the source electrodes. In the on-status, a current of 1 mA flows, which results in a power dissipation per tap of 15 mW. The on-off ratio is 10 dB and is limited by the residual off-value of the output signal, which is caused by the accumulated, passive detection of the 32 detectors. Common-mode rejection could not be applied, since the nonuniformity of the ZnO layer thickness disturbed the phase relations in the tracks (see section 6.2.5). With proper design and a practical common-mode rejection of 25 dB, the on-off ratio can be enlarged to more than 25 dB.

A final matter to be considered is the programming speed, i.e. how fast the weight function can be adjusted. In practice, it is sufficient to have a programming delay smaller than the time delay of the filter. Then there is a complete, new set of tap weight factors present within the time duration T of the impulse response. There is practically no storage of charge carriers in the BMT, and the response to a change in the bias current is very fast. Measurements with programming rates of up to 200 kHz were performed without any notable problems.

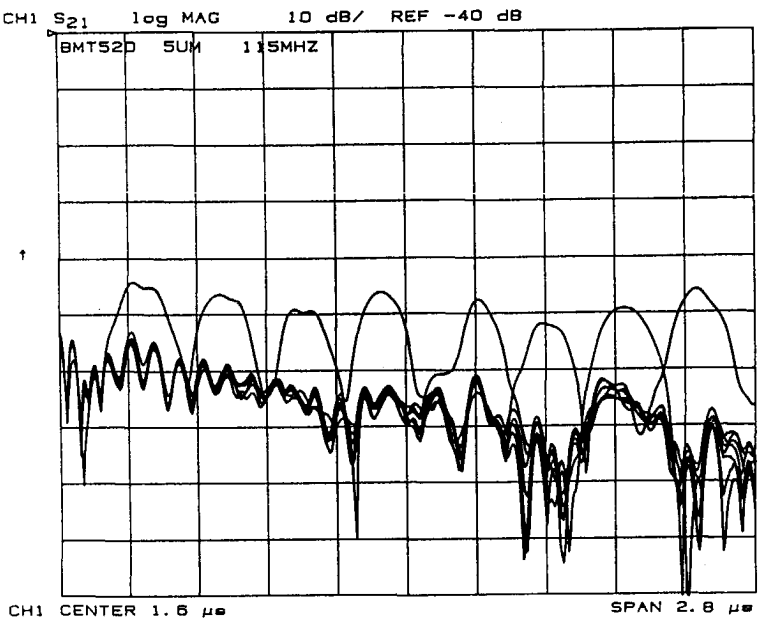


Figure 6.11: *Time domain response of an experimental PTDL when the even-numbered BMTs are sequentially turned on.*

(ii) Array of PI-JFETs

The minimal pitch of the PI-JFET array is determined by the requirements set on the ring structure of the top gate. For a proper phase relation between the ring part perpendicular to the SAW direction, a minimum distance of one wavelength is required. Therefore, the pitch can at most be reduced to 2λ.

Because the PI-JFET is essentially a three-port device, no difficulties arise in the separation of the DC and RF signals. In the array, all sources are grounded, and all drains are connected to a common drain line which is held at a fixed voltage. The individual control takes place through the gate terminals.

When the PI-JFET operates in the saturation range, its output impedance is very high and independent of the bias conditions on the gate. Therefore, there is a higher degree of freedom to choose a proper load impedance than for the BMT. Since no regeneration occurs, even power

matching can be considered. Since the PI-JFETs have not been implemented in a total array, no measurement results can be given of a complete PTDL.

The switching speed of the PI-JFET is limited by the distributed *RC* network representing the gate. For the devices described in Chapter 5, a −3 dB point at 100 MHz is estimated. This is much greater than required in ordinary PTDLs. The switching speed was examined experimentally up to 200 kHz without any observable problems.

(iii) Comparison between BMT and PI-JFET

At this point, a comparison will be made between the BMT and PI-JFET concerning their application in PTDLs. It should be stressed that the fabrication technology of both of the devices is very simple. However, since the PI-JFET has a buried channel underneath the *pn* gate, whereas the BMT has a surface channel at the SiO_2-Si interface, the PI-JFET is less liable to the effects that affect the silicon surface (for example ZnO sputtering), and, therefore, its characteristics are more reproducible. The pitch of the PI-JFET array is limited to 2λ. If the passive detection is suppressed, the pitch of the BMT array can be much smaller. The experimental bilinearity factors differ by about a factor 2 (see Table 6.2). Since no optimization was achieved in either the design or the technology, no final conclusions about this factor can be given at this stage. However, the techniques that can be used to improve the PI-JFET efficiency are more obvious, see Chapter 5. Because of the triode-like characteristics of the BMT, its output impedance is rather low (a few hundred Ω). In the saturation range, the output impedance of the PI-JFET is much higher (a few decades of kΩ). Therefore, the loading of the PI-JFET is less critical. In conclusion, at this moment it can be stated that the use of the PI-JFET seems to be more attractive.

6.5 PERIPHERAL ELECTRONICS

As a result of the semiconducting substrate in the ZnO-SiO_2-Si layered structure, in addition to tap control electronics, a large amount of supporting electronics can be included. It is clear that the type of circuitry to be used greatly depends on the application in which the PTDL is applied.

6.5.1 General Applications

A number of circuits are application independent. If for example a dual-track configuration is implemented, a differential amplifier is required. The bandwidth of this amplifier must be higher than the bandwidth of the detection array. Depending on the type of programmable detector, the input impedance must go to zero or must be matched to the array.

At the input of the PTDL, a driving circuit can be placed to drive the SAW generating IDT. In order to minimize feedthrough, a symmetrical output is required. The available power of this driving circuit must be as high as possible.

Finally, interface circuits can be included to match the off-chip impedance levels to the internal, on-chip impedance levels. For RF systems, it is common practice to use a $50\,\Omega$ impedance level. Within the chip, other requirements are set on the impedance levels. To obtain a transparent RF module with a $50\,\Omega$ input and output impedance, matching circuits can be applied.

6.5.2 BPSK Matched Filters

In these application, only the polarity of the tap has to be controlled. With a dual-track structure to provide the phase control, the control circuits are reduced to simple on-off switches. Digital circuits may be added to handle the code sequences and to drive the control switches. A register can be used to read in a new code serially, and apply it to the detection array in parallel. Between this register and the detection array, a holding register is required, in order to read in a new code without disturbing the present tap weighting. Finally, memory in the form of ROM or RAM can be added to store a number of frequently used codes.

6.5.3 Adaptive Filters

In the adaptive filter, a continuous control of the detector amplitude is required. Digital-to-analog converters are necessary to obtain a computer-controlled weighting system. The speed requirements are moderate, and correspond to the switching speeds as discussed in section 6.4. For a continuous phase control, four acoustic tracks are required, providing signals with a 0, 90, 180 and 270 degrees phase shift. RF circuits must be added to perform vector addition operations. Finally, intelligent circuitry can be added to carry out simple adaptation routines.

6.6 CONCLUSIONS

Because of the dispersive behavior of the ZnO-SiO_2-Si configuration, the SAW velocity depends on the frequency and the layer thicknesses. The phase relations in the PTDL are very sensitive to the ZnO layer thickness, and a uniform thickness in the entire propagation path is crucial. To avoid shadowing and windowing effects, the ZnO layer should preferably be deposited over the entire wafer after which part of it is removed by etching. The layered structure also gives rise to higher-order modes. In particular, the second-order Rayleigh-wave mode can disturb the operation of the PTDL. The seriousness of the disturbance depends on the application.

The programmable filter can be divided into a generation and a detection part. The SAWs are excited with an interdigital transducer. For a conventional IDT, a thick SiO_2 layer is required, which is not compatible with the oxide requirement imposed by the junction detectors. A combination of a junction and a metal transducer (JMIDT) provides a new device with which SAWs can be excited in the ZnO-SiO_2-Si configuration with a thin SiO_2 layer. The required dielectric medium underneath the metal IDT is provided by the depletion region around the reverse-biased junction IDT. A low capacitance and reduced feedthrough level are expected.

The detection part consist of an array of programmable SAW detectors connected in parallel. Since the actual filtering takes place in the detection part, disturbances in the propagation path must be avoided. The developed active junction detectors (BMT and PI-JFET) are quite suitable to perform this task. Their efficiencies are comparable to previously developed detectors, however, they have a 10 to 100 times lower DC power dissipation. The performances of the experimental BMTs and PI-JFETs do not differ much. However, if the design and fabrication technology are optimized, the PI-JFET seems to promise the most attractive SAW junction detector.

In order to suppress interfering signals like EM feedthrough, bulk waves and signals originating from the passive detection, common-mode rejection must be applied with a dual-track configuration. The pitch of the detection array determines the bandwidth of the PTDL. However, in practice, the bandwidth is limited by the transmitting IDT. For a moderate IDT efficiency, a considerable number of finger pairs is required, which limits the acoustic bandwidth.

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CHAPTER 2 — THE ACOUSTOELECTRIC SYSTEM

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LIST OF SYMBOLS

Symbol	Description	Unit
B_a	acoustic radiation susceptance	S
c^E_{ijkl}	stiffness tensor at constant electric field $(i,j,k,l = 1,2,3)$	Pa
C_b	static barrier capacitance	F
C_d	static detector capacitance	F
C_{ch}	channel capacitance	F/m
C_{sw}	sidewall capacitance	F/m
C_{GTD}	top gate to drain capacitance of JFET	F
C_{GTS}	top gate to source capacitance of JFET	F
CE_i	current conversion efficiency	A^2/W
CE_p	power conversion efficiency	
D_i	electric displacement vector $(i = 1,2,3)$	C/m^2
D_n	electron diffusion coefficient	m^2/s
D_p	hole diffusion coefficient	m^2/s
e_{kij}	piezoelectric tensor $(k,i,j = 1,2,3)$	C/m^2
E_k	electric field vector $(k = 1,2,3)$	V/m
f_0	resonance frequency	s^{-1}
f_T	cutoff frequency	s^{-1}
F_p	bilinearity factor	W^{-1}
g_b	transconductance of BMT	S
g_d	feedback conductance	S
g_m	transconductance of JFET	S
g_{mT}	top-gate transconductance of JFET	S
g_{mB}	bottom-gate transconductance of JFET	S
G_a	acoustic radiation conductance	S
h_{ch}	channel depth	m
h_{depl}	depletion layer thickness	m
h_{epi}	epilayer thickness	m
h_j	junction depth	m
h_{ox}, h_1	silicon dioxide layer thickness	m

h_{ZnO}, h_2	–	zinc-oxide layer thickness	m
i_d	–	small-signal detector current	A
i_n	–	noise current	$A\sqrt{s}$
I_D	–	drain bias current	A
$J_{n,i}$	–	electron current-density vector ($i = 1, 2, 3$)	A/m^2
$J_{p,i}$	–	hole current-density vector ($i = 1, 2, 3$)	A/m^2
k	–	wavenumber; $k = \omega/v_{ph}$	m^{-1}
k_B	–	Boltzmann constant; $k_B = 1.38 \cdot 10^{-23}$	J/K
l_{free}	–	mean free path of charge carriers	m
L	–	interaction length of active detector	m
L_D	–	Debye length	m
n	–	free electron density	m^{-3}
n_i	–	intrinsic electron density	m^{-3}
N_A	–	acceptor concentration	m^{-3}
N_B	–	substrate doping concentration	m^{-3}
N_D	–	donor concentration	m^{-3}
N_E	–	epilayer doping concentration	m^{-3}
N_T	–	p^+ doping concentration	m^{-3}
p	–	free hole density	m^{-3}
p_{idt}	–	IDT period	m
p_{tap}	–	tap period	m
P_a	–	acoustic power flow	W/m
q	–	electron charge; $q = 1.602 \cdot 10^{-19}$	C
Q_e	–	electrical quality factor	
R_s	–	series resistance of junction electrode	Ω
R_{SRC}	–	source series resistance	Ω
S_{kl}	–	strain tensor ($k, l = 1, 2, 3$)	
t	–	time coordinate	s
T_{ij}	–	stress tensor ($i, j = 1, 2, 3$)	Pa
T	–	temperature	K
ΔT	–	inter-tap delay	s
u_i	–	particle displacement vector ($i = 1, 2, 3$)	m
$v_{d,i}$	–	drift velocity vector ($i = 1, 3$)	m/s
v_{gr}	–	SAW group velocity	m/s
v_m	–	injection velocity at barrier maximum	m/s
v_{ph}	–	SAW phase velocity	m/s
v_s	–	scattering velocity	m/s
V_{bi}	–	built-in voltage	V
V_{BS}	–	substrate-to-source voltage	V
V_{DS}	–	drain-to-source voltage	V
V_{ES}	–	epi-to-source voltage	V
V_{GTS}	–	top-gate bias voltage	V
V_{GBS}	–	bottom-gate bias voltage	V

V_{FB}	–	flat-band voltage	V
V_P	–	pinch-off voltage of separated-gate JFET	V
V_{RT}	–	reach-through voltage	V
W	–	aperture of transducers and detectors	m
W_c	–	channel width	m
x_i	–	Cartesian coordinate ($i = 1, 2, 3$)	m
x_m	–	position of barrier maximum relative to source junction	m
Y_d	–	detector output admittance	S
α_i	–	fractional taper in ZnO layer thickness in x_i-direction	m^{-1}
Γ	–	space-charge suppression factor	
δ	–	Doppler shift; $\delta = 1 - v_{d,1}/v_{ph}$	
ϵ_{ik}^S	–	dielectric permittivity tensor at constant strain ($i, k = 1, 2, 3$)	F/m
ϵ_{Si}	–	dielectric permittivity of silicon	F/m
λ	–	average SAW wavelength	m
μ_n	–	electron mobility	m^2/Vs
μ_p	–	hole mobility	m^2/Vs
Ξ_{kl}	–	second-rank deformation potential tensor	J
ρ_e	–	electric charge density	C/m^3
ρ_m	–	mass density	kg/m^3
ρ_{pe}	–	piezoelectric polarization charge density	C/m^3
ρ_s	–	equivalent surface charge density	C/m^2
ρ_ϵ	–	dielectric polarization charge density	C/m^3
σ_{Si}	–	silicon conductivity	S/m
τ_{ph}	–	phase delay	s
τ_{gr}	–	group delay	s
ϕ	–	small-signal potential	V
ψ	–	static potential	V
ψ_F	–	potential associated with semiconductor Fermi level	V
ψ_i	–	potential associated with intrinsic Fermi level	V
ψ_m	–	potential barrier height	V
ψ_s	–	static potential at semiconductor surface	V
ω	–	angular frequency	rad/s
ω_c	–	relaxation frequency	rad/s
ω_{Dn}	–	diffusion frequency for electrons	rad/s
ω_{Dp}	–	diffusion frequency for holes	rad/s
$\Delta\omega$, B	–	bandwidth	rad/s

Commonly used abbreviations:

AC	–	Alternating Current
AE	–	AcoustoElectric
BAW	–	Bulk Acoustic Wave
BMT	–	Barrier-Modulated Tap
CW	–	Continuous Wave
DC	–	Direct Current
EM	–	ElectroMagnetic
ESC	–	Equivalent Surface Charge
IDT	–	InterDigital Transducer
IF	–	Intermediate Frequency
JMIDT	–	Junction-Metal InterDigital Transducer
PI-JFET	–	Piezoelectric Junction Field-Effect Transistor
PTDL	–	Programmable Tapped Delay Line
RF	–	Radio Frequency
RT	–	Reach-Through
SAW	–	Surface Acoustic Wave

Note that in this thesis the lengths of detectors and electrodes (L) are measured in the propagation direction (x_1-direction), whereas widths and apertures (W) are measured perpendicular to the propagation direction (x_2-direction). The letter h is reserved for thicknesses and depths (x_3-direction).

SUMMARY

The research work presented in this thesis involves the design and implementation of programmable, Surface Acoustic Wave (SAW) detectors in ZnO-SiO_2-Si layered structures. These detectors are the key elements in programmable SAW filters. The combination of SAW with semiconductor technology allows the design of new piezotronic components, in which an interaction takes place between the acoustical and electrical properties of the ZnO-SiO_2-Si structure. A theoretical study of the acoustoelectrical behavior of the layered structure is given, followed by an investigation of several controllable SAW detection concepts. By constructing the detectors with merely diffused or ion-implanted junction electrodes, mechanical and topological discontinuities in the SAW propagation path are avoided and, thus, spurious wave reflections are suppressed. Two realizations of active SAW detectors are presented. Experiments at 100 MHz confirm the operation of the new detection concepts. By controlling the DC bias conditions of the devices, the output amplitude can be varied within a wide range. Finally, the total programmable filter configuration employing the developed SAW detectors is evaluated. The work presented is a contribution to the development of monolithic programmable SAW filters, in which the acoustic and electric signal-processing functions are not only joined, but are even merged.

Chapter 1. An overview is given of the applications of programmable filters in radar and communication systems. The basic realization of an asynchronous programmable filter, which consists of a programmable tapped delay line, is discussed. Several implementations and technologies are evaluated. In the high-frequency range (50 MHz – 1 GHz), SAW technology is attractive. The fundamentals of SAW techniques are briefly reviewed.

Chapter 2. A thorough theoretical discussion of the acoustoelectric system in the ZnO-SiO_2-Si layered structure is given. A two-dimensional treatment of the fundamental acoustical and electrical rela-

tions is presented. A new method is introduced in which the acoustically induced, polarization charge in the piezoelectric ZnO layer is reduced to a surface charge at the ZnO-SiO_2 interface. In this Equivalent-Surface-Charge method, the acoustoelectric field problem is reduced to an electrical problem. By the use of this method, the influence of the SAW on the electronic components embedded in the silicon substrate can conveniently be investigated employing 2D-simulation programs commonly used for the investigation of semiconductor devices. Finally, an overview of the acoustoelectric effects which result from the interaction between the SAWs and mobile charge carriers is given.

Chapter 3. The realization of SAW detectors, the output of which can be controlled electronically, is investigated. Several SAW detection mechanisms such as passive, active and parametric mechanisms are highlighted. The most attractive mechanism to use is the active detection mechanism, in which the SAW merely modulates an auxiliary power supply. High efficiency and a low distortion level are feasible. The detection and control functions can be separated (Separated-Control Tap) or merged into a single component (Integrated-Control Tap). By using the integrated control, a compact programmable detector with low electromagnetic feedthrough and a high degree of RF tap-to-tap isolation can be obtained. In the active detector, an integrated control is accomplished simply by varying the auxiliary power supply level. The use of junction electrodes is discussed. The smooth surface and the absence of mechanical discontinuities ensure an undisturbed SAW propagation. The series resistance in the junction electrodes cannot be ignored. Therefore, in order to achieve a high signal-to-noise ratio, the active detection mechanism is indispensable.

Chapter 4. A new, active SAW detector composed merely of junction electrodes is presented. Basically, it consists of a lateral reach-through diode, the injection current of which is modulated by the SAW electric fields. Since the basic operation involves the modulation of the potential barrier at the source electrode, the name Barrier-Modulated Tap (BMT) is used. After discussing the operation in the one-dimensional configuration, the concept is extended to the two-dimensional configuration. 2D-simulation programs are developed to analyze the potential distribution in the device. In addition, a small-signal equivalent circuit model using lumped network elements is derived. The device is very simple to fabricate and can readily be obtained using standard IC processes. Experiments around 100 MHz on devices fabricated in the ZnO-SiO_2-Si structure

confirm the new detection concept, and agree very well with the simulation results. The active detection mechanism provides power conversion efficiencies in the order of –50 dB at an untuned load of 50 Ω. By varying the DC bias current between 0 and 5 mA, the active detection efficiency can be controlled within a range of more than 25 dB.

Chapter 5. A piezoelectric Junction FET (PI-JFET) is employed as an active SAW detector. The source, gate, and drain electrodes are composed of junction structures. Only the *pn*-junction gate at the silicon surface is applied in the SAW detection process. Both the operation and the dominant device parameters of the top-driven junction FET are theoretically evaluated. Experimental SAW detectors consisting of *n*-channel JFETs have been implemented. Experiments around 100 MHz demonstrate the SAW detecting and output control functions in the PI-JFET. The detection efficiency is in the same order of magnitude as that of the BMT. By varying the top-gate bias voltage between 0 and –6 V, the active detection mechanism can be controlled within a range of more than 30 dB.

Chapter 6. In the final chapter of this thesis, the complete, monolithic programmable filter is considered. Several disturbing effects such as dispersion and higher-order wave modes are evaluated with respect to the filter performance. In the filter architecture, a division is made between the wave generation and wave detection parts. A new type of SAW generating transducer, which is compatible with the fabrication technology developed for the junction detectors, is presented. In the detector array, which is composed of the controllable SAW detectors, the actual filter function takes place. A dual-track detection array is required to suppress common-mode disturbances. To compare the different SAW detectors, a bilinearity factor is used, which not only expresses the detector efficiency but also includes the DC power dissipation. With the developed BMTs and PI-JFETs, bilinearity factors can be realized which are 10 to 100 times larger than can be achieved with active detector types realized in the past. In addition, because of the absence of regeneration and wave disturbances in the SAW propagation path, the developed active junction detectors are highly suited for use in the detection array of the programmable tapped delay line. Finally, an overview of the electronic circuitry which can be added in future filter designs in the ZnO-SiO_2-Si layered structure is given. This final step concludes the design and realization of true smart SAW filters for wideband, high-frequency signal-processing functions.

SAMENVATTING

Het onderzoek, dat in dit proefschrift wordt gepresenteerd, behandelt het ontwerp en de vervaardiging van programmeerbare, akoestische oppervlaktegolf (Surface Acoustic Wave, afgekort SAW) detectoren in ZnO-SiO_2-Si gelaagde structuren. Deze detectoren vormen de sleutelcomponenten van programmeerbare SAW filters. De samenvoeging van SAW- en halfgeleidertechnologie maakt het mogelijk nieuwe piezotronische componenten te ontwerpen, waarin een interactie plaatsvindt tussen de akoestische en elektronische eigenschappen van de ZnO-SiO_2-Si structuur. Na een theoretische studie van het akoesto-elektrische gedrag van de gelaagde structuur worden verschillende, regelbare SAW detectieprincipes onderzocht. Door de detectoren op te bouwen met slechts diffusie of ionen-geïmplanteerde junctie-elektroden worden mechanische en topologische discontinuïteiten in het SAW propagatie pad vermeden. Hierdoor worden reflecties van de akoestische golven onderdrukt. Een tweetal uitvoeringen van actieve SAW detectoren wordt gepresenteerd. Experimenten rond 100 MHz bevestigen de werking van de nieuwe detectieprincipes. Het uitgangssignaal kan over een groot bereik gevarieerd worden door de DC instelling van de componenten te regelen. Ten slotte wordt een compleet, programmeerbare filterconfiguratie geëvalueerd waarin de ontwikkelde SAW detectoren worden toegepast. Het gepresenteerde werk draagt bij tot de ontwikkeling van monolitische, programmeerbare SAW filters waarin de akoestische en elektrische signaalbewerkingsfuncties niet alleen samengevoegd worden, maar bovendien in elkaar over gaan.

Hoofdstuk 1. Een overzicht wordt gegeven van de toepassingen van programmeerbare filters in radar- en communicatiesystemen. De basisuitvoering van een asynchroon, programmeerbaar filter bestaande uit een vertragingslijn met een rij van aftakkingen, wordt nader uitgewerkt. Verscheidene implementaties en technologieën komen aanbod. Het gebruik van de SAW technologie is aantrekkelijk in het hoogfrequent bereik (50 MHz – 1 GHz). Enkele basisbegrippen uit het SAW vakgebied worden summier behandeld.

Hoofdstuk 2. Een gedegen theoretische bechrijving wordt gegeven betreffende het akoesto-elektrische syteem dat gevormd wordt door de ZnO-SiO_2-Si gelaagde structuur. De fundamentele akoestische en elektrische relaties in twee dimensies worden beschouwd. Een nieuwe methode wordt geïntroduceerd, waarin de akoestisch opgewekte polarisatielading in de piezoelektrische ZnO laag teruggebracht wordt tot een oppervlaktelading op het ZnO-SiO_2 grensvlak. Met deze "Equivalent-Surface-Charge" methode wordt het akoesto-elektrische veldprobleem gereduceerd tot een elektrisch probleem. Door gebruik te maken van deze methode kan de invloed van de akoustische oppervlaktegolf op de elektronische componenten in het silicium substraat eenvoudig onderzocht worden met behulp van 2D-simulatieprogramma's, die gewoonlijk voor het onderzoek van halfgeleidercomponenten worden gebruikt. Ten slotte wordt er een overzicht gegeven van de akoesto-elektrische effecten die optreden als gevolg van de interactie tussen de akoestische oppervlaktegolf en beweegbare ladingdragers.

Hoofdstuk 3. De realisatie wordt onderzocht van SAW detectoren waarvan het uitgangssignaal elektronisch regelbaar is. Verschillende SAW detectiemechanismen worden besproken, zoals daar zijn de passieve, actieve en parametrische mechanismen. Het meest aantrekkelijke mechanisme is het actieve detectiemechanisme waarin de SAW slechts een extra toegevoerd vermogen moduleert. Hiermee kunnen hoge rendementen en lage vervormingsniveaus worden bereikt. De detectie- en regelfuncties kunnen gescheiden (gescheiden regelfunctie) of samengevoegd worden in één enkele component (geïntegreerde regelfunctie). Met de geïntegreerde regelfunctie zijn compacte, programmeerbare detectoren te realiseren waarin weinig last wordt ondervonden van elektromagnetisch overspraak. In de actieve detector kan de geïntegreerde regelfunctie gerealiseerd worden door het regelen van het extra toegevoerde vermogen. Het gebruik van junctie-elektroden wordt besproken. Het vlakke oppervlak en de afwezigheid van mechanische discontinuïteiten zorgen voor een vrijwel onverstoorde golfpropagatie. De junctie-elektroden hebben echter een niet te verwaarlozen serieweerstand. Voor het verkrijgen van een hoge signaal-ruis verhouding zijn daarom de actieve detectiemechanismen onontbeerlijk.

Hoofdstuk 4. Een nieuw type, actieve SAW detector die alleen uit junctie-elektroden bestaat, wordt geïntroduceerd. In feite wordt de detector gevormd door een laterale "reach-through" diode, waarvan de geïnjecteerde stroom gemoduleerd wordt door de elektrische velden van

de SAW. Omdat de werking betrekking heeft op de modulatie van een potentiaalbarrière naast de injectie-elektrode, wordt de detector de "Barrier-Modulated Tap (BMT)" genoemd. Na een verhandeling over de werking in een ééndimensionale structuur wordt het concept uitgebreid naar een tweedimensionale structuur. De potentiaalverdeling in deze structuur wordt geanalyseerd met 2D-simulaties. Bovendien wordt er een klein-signaal vervangingsmodel afgeleid, bestaande uit discrete netwerkcomponenten. De BMT is eenvoudig te vervaardigen gebruikmakend van standaard IC processen. Experimenten rond 100 MHz met componenten gefabriceerd in de ZnO-SiO_2-Si structuur bevestigen de werking van het nieuwe detectieconcept, en komen goed overeen met de simulatieresultaten. Het actieve detectiemechanisme verschaft vermogensrendementen rond de -50 dB in een niet-afgestemde belasting van $50\,\Omega$. Door het varieren van de DC ruststroom tussen 0 en 5 mA kan het actieve detectiemechanisme over een bereik van meer dan 25 dB geregeld worden.

Hoofdstuk 5. De Piezoelektrisch Junctie FET (PI-JFET) wordt toegepast als actieve SAW detector. De source, gate en drain elektroden worden opgebouwd met junctiestructuren. Voor het SAW detectieproces wordt alleen de *pn*-junctie gate aan het siliciumoppervlak gebruikt. Zowel de werking als de dominante parameters van deze top-gate gestuurde junctie FET worden theoretisch geanalyseerd. Experimentele SAW detectoren, bestaande uit *n*-kanaal JFETs, zijn vervaardigd. Experimenten rond 100 MHz tonen de SAW detectiefunctie en de regelbaarheid van het uitgangssignaal in de PI-JFET aan. Het detectie-rendement is in de zelfde orde van grootte als van de BMT. Door het varieren van de DC top-gate spanning tussen 0 en -6 V kan het actieve detectiemechanisme over een bereik van meer dan 30 dB geregeld worden.

Hoofdstuk 6. In dit laatste hoofdstuk wordt het complete, monolitische programmeerbare filter besproken. Verscheidene storende effecten, zoals dispersie en hogere-orde golfmodi worden geëvalueerd met betrekking tot de prestaties van het filter. In de filter architectuur wordt een verdeling gemaakt tussen het golfopwekkings- en golfdetectiedeel. Een nieuw type SAW-opwekkingstransducent wordt gepresenteerd die compatibel is met de fabricagetechnologie van de ontwikkelde junctiedetectoren. De uiteindelijke filter actie vindt plaats in de detectorarray bestaande uit regelbare SAW detectoren. De detectiearray dient in twee identieke, parallel gelegen delen te worden opgesplitst om common-mode verstoringen te onderdrukken. Om de verschillende SAW detectoren te kunnen vergelijken wordt een bilineariteitsfactor gebruikt die niet slechts het detectie-

rendement maar tevens de DC vermogensdissipatie omvat. Met de ontwikkelde BMTs en PI-JFETs kunnen bilineariteitsfactoren worden gerealiseerd die 10 tot 100 maal groter zijn dan verkregen kunnen worden met in het verleden gerealiseerde aktieve detectoren. Bovendien kunnen de ontwikkelde actieve detectoren uitstekend gebruikt worden in de detectiearray van het programmeerbaar filter, omdat ze geen golven regenereren en de golfpropagatie nauwelijks verstoren. Ten slotte wordt er een overzicht gegeven van de elektronische schakelingen die in toekomstige filter ontwerpen in de ZnO-SiO_2-Si gelaagde structuur toegevoegd kunnen worden. Met deze laatste stap wordt de realisatie van intelligente SAW filters voor breedbandige en hoogfrequente signaalverwerkingsfuncties afgesloten.

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ABOUT THE AUTHOR

Jacobus Cornelis Haartsen was born in 's-Gravenhage, the Netherlands, on February 13, 1963. In his early childhood he moved with his family to Monster. In 1981 he graduated from high school (Atheneum B) "Groen van Prinsterercollege" in 's-Gravenhage. He then started his studies in electrical engineering at Delft University of Technology, Delft. On November 20, 1986 he received (cum laude) his Master's degree (the Ingenieurs' degree). His thesis dealt with oscillator systems to be used in chemical sensors. During his studies he worked for one month with Siemens N.V. ('s-Gravenhage, the Netherlands) in 1982, and for three months with Philips N.V. (Eindhoven, the Netherlands) in 1985.

In December 1986 Jaap Haartsen started his Ph.D. research in surface acoustic wave (SAW) devices, carried out in the Microacoustics Group of the Laboratory of Electronic Instrumentation, Department of Electrical Engineering at Delft University of Technology. During the first year of his Ph.D. research he worked on SAW Spread-Spectrum demodulators to be used in indoor, wireless communication systems. This work was carried out in cooperation with NCR Systems Engineering B.V. (Nieuwegein, the Netherlands). At the same time, he started up a new project which involved the design and realization of novel SAW detectors to be applied in programmable SAW filters in ZnO-SiO_2-Si layered structures. This project ultimately led to this Ph.D. thesis.

Jaap Haartsen has published his research results in a number of papers, and has presented his work at several (international) conferences and companies in Europe and the USA. A patent was granted for his work on SAW demodulators. A list of publications and presentations has been included at the end of this thesis.

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Poster presentation: "A monolithic SAW physical-electronic system for sensors," at the *IEEE Ultrasonics Symp.*, Denver, USA, October, 1987.

Oral presentation: "The barrier-modulated tap: a new SAW detection method in silicon," at the *IEEE Ultrasonics Symposium*, Chicago (IL), USA, October 3, 1988.

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