Strained silicon quantum wells for spin qubits

Degli Esposti, D.

DOI
10.4233/uuid:a925b226-ca58-491e-8c6d-e0d4ff3d98fb

Publication date
2025

Document Version
Final published version

Citation (APA)
Degli Esposti, D. (2025). *Strained silicon quantum wells for spin qubits*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:a925b226-ca58-491e-8c6d-e0d4ff3d98fb

Strained silicon quantum wells for spin qubits

Davide Degli Esposti

STRAINED SILICON QUANTUM WELLS FOR SPIN QUBITS

STRAINED SILICON QUANTUM WELLS FOR SPIN QUBITS

Dissertation

Dissertation for the purpose of obtaining the degree of doctor
at Delft University ofTechnology
by the authority of the Rector Magnificus, prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
Monday 14 April 2025 at 17:30

by

Davide DEGLI ESPOSTI

Master of Science in Physics,
Università di Pisa, Pisa, Italy,
born in Teramo, Italy.

This dissertation has been approved by the promotors

promotor: prof. dr. ir. L.M.K. Vandersypen
copromotor: dr. G. Scappucci

Composition of the doctoral committee:

Rector Magnificus,	chairperson
prof. dr. ir. L.M.K. Vandersypen	Delft University of Technology, promotor
dr. G. Scappucci	Delft University of Technology, copromotor
Independent members:	
prof. dr L. DiCarlo	Delft University of Technology
dr. A. Chatterjee	Delft University of Technology
prof. dr. M. Friesen	University of Wisconsin-Madison, USA
prof. dr. K. De Greve	IMEC and KU Leuven, Belgium
Reserve member:	
prof. dr G.A. Steele	Delft University of Technology


Keywords: Si/SiGe heterostructure, Valley splitting, Charge Noise, Spin qubits

Printed by: Gildeprint - www.gildeprint.nl

Front & Back: Artistic impression of a STEM image of a strained Si quantum well & tilted SEM image of four quantum dots device on a Si/SiGe heterostructure.

ISBN 978-94-6384-734-6

An electronic version of this dissertation is available at
https://resolver.tudelft.nl/uuid:955fab3d-fc33-4ccb-8c58-c6eaf7b56c9c.

Felix qui potuit rerum cognoscere causas

Lucrezio, Geordiche, (2), 490

CONTENTS

SUMMARY

Spin qubits in semiconductor quantum dots hold great promises for quantum information processing thanks to their small footprint, long coherence time, and similarities with classical transistors. However, such a new technology comes with new challenges and requires considering new metrics to develop proof-of-principle devices into a technological platform at scale.

Here, we study Si/SiGe heterostructures developed to host single electron spin qubits. We characterize the heterostructure and material stack using different structural techniques and measure the performances of multiple quantum devices with statistical significance. We use classical and quantum metrics to identify the performance-limiting mechanisms and improve them upon modification of selected parameters of the material stack to enable the next generation of spin qubit devices.

The first experiment is about the electrostatics of undoped Si/SiGe heterostructures. We study the semiconductor/dielectric interface between the epitaxial SiGe spacer and the SiOx and AlOx dielectrics. Against the mainstream approach, we grow heterostructures without an epitaxial Si cap. We find an improved interface from a structural characterization and in the two-dimensional electron transport at low temperatures.

The second experiment concerns the charge noise in few-electron quantum dots. We build on the previous results and focus our attention on the thickness of the ^{28}Si quantum well. In thin quantum wells without a sacrificial Si cap, we find lower charge noise that we attribute to decreased density of remote impurities and misfit dislocations at the SiGe/Si and Si/SiGe interfaces arising from the local quantum well strain relaxation.

The third experiment finds the balance between disorder and the energy splitting of the nearly degenerate conduction band valleys (valley splitting) by fine-tuning the thickness of the ^{28}Si quantum well. We challenge the apparent dichotomy between these two parameters and demonstrate heterostructures with simultaneously low disorder and high valley splitting. Besides, we give a quantitative estimation of the amplitude of the strain fluctuations in the quantum well arising from the virtual substrate.

The advancements reported in this thesis confirm the steady progress of the Si/SiGe platform towards realizing a full-scale quantum computer. We summarize the results in the conclusion chapter, where we also highlight the general trends in the spin qubit community and suggest a few knobs to tweak to further improve the material platform.

SAMENVATTING

Spin qubits in halfgeleider quantum dots houden grote beloften in voor quantuminformatieverwerking dankzij hun kleine voetafdruk, lange coherentietijd en overeenkomsten met klassieke transistors. Zo'n nieuwe technologie brengt echter nieuwe uitdagingen met zich mee en vereist het overwegen van nieuwe metrieken om proof-of-principle apparaten te ontwikkelen tot een technologisch platform op schaal.

Hier bestuderen we Si/SiGe heterostructuren die zijn ontwikkeld om spin qubits met één elektron te bevatten. We karakteriseren de heterostructuur en de materiaalstapel met verschillende structurele technieken en meten de prestaties van meerdere kwantumapparaten met statistische significantie. We gebruiken klassieke en kwantummetrieken om de prestatiebeperkende mechanismen te identificeren en deze te verbeteren door geselecteerde parameters van de materiaalstapel aan te passen om de volgende generatie spin-qubitapparaten mogelijk te maken.

Het eerste experiment gaat over de elektrostatica van ongedoteerde Si/SiGe heterostructuren. We bestuderen de halfgeleider/diëlektrische interface tussen de epitaxiale SiGe spacer en de SiOx en AlOx diëlektrica. Tegen de gangbare aanpak in, kweken we heterostructuren zonder een epitaxiale Si kap. We vinden een verbeterde interface vanuit een structurele karakterisatie en in het tweedimensionale elektronentransport bij lage temperaturen.

Het tweede experiment betreft de ladingsruis in kwantumstippen met weinig elektronen. We bouwen voort op de vorige resultaten en richten onze aandacht op de dikte van de ^{28}Si kwantumput. In dunne kwantumputten zonder een Si opofferingskapje vinden we een lagere ladingsruis die we toeschrijven aan een verminderde dichtheid van onzuiverheden op afstand en misfit dislocaties bij de SiGe/Si en Si/SiGe interfaces als gevolg van de lokale rekrelaxatie van de kwantumput.

Het derde experiment vindt het evenwicht tussen wanorde en de energiesplitsing van de bijna ontaarde geleidingsbanddalen (dalsplitsing) door de dikte van de quantumput ^{28}Si nauwkeurig af te stellen. We bestrijden de schijnbare dichotomie tussen deze twee parameters en tonen heterostructuren met tegelijkertijd een lage wanorde en een hoge dalsplitsing. Bovendien geven we een kwantitatieve schatting van de amplitude van de vervormingsfluctuaties in de kwantumput die het gevolg zijn van het virtuele substraat.

De in dit proefschrift gerapporteerde vooruitgang bevestigt de gestage vooruitgang van het Si/SiGe platform in de richting van het realiseren van een full-scale quantumcomputer. We vatten de resultaten samen in het concluderende hoofdstuk, waar we ook de algemene trends in de spin qubit gemeenschap belichten en een paar knoppen suggereren om aan te draaien om het materiaalplatform verder te verbeteren.

1

INTRODUCTION

A digital computer is generally believed to be an efficient universal computing device...
...This may not be true when quantum mechanics is taken into consideration.

P. W. Shor, arXiv:quant-ph/9508027, 1995

Parts of this introduction follow a lecture from Steven Girvin [1].

1

1.1. THE FIRST QUANTUM REVOLUTION

Quantum mechanics describes nature's behaviour at atomic scales and low energies. The theory arose in the early decades of the 20th century to explain experiments on black-body radiation [2], light-matter interaction [3], and interference [4]. The experiments forced into play the idea of wave-particle duality – that matter particles can behave like waves and light waves can act like particles. This simple idea has proven to be an extremely precise description of physical reality. It underlines nearly all the scientific and technological breakthroughs associated with the *so-called first quantum revolution*.

This first quantum revolution took place in the first half of the 20^{th} century, with scientists busy with apparently useless and curiosity-driven experiments that ultimately led to technological inventions with a huge impact on society. The atomic clock was invented in 1955 [5] to test some specific hypotheses of special and general relativity [6]. However, it turned out that the possibility of measuring time within a few nanoseconds could be translated into the ability to measure position within a few meters, known today as the Global Positioning System (GPS). The inventors of the laser in 1960 [7] were trying to perform precise spectroscopic measurements of the hyperfine structure of atoms [8]. They did not expect their invention to be used to play music or to transport information across large distances through fiber optic communication. The transistor was created in 1947 to take over the vacuum tube [9, 10]. It led to the integrated circuit [11], and its exponential scale-down in price and size made it the most produced component in human history [12]. Today, we produce 20 trillion transistors per second ($20\,000\,000\,000\,000\,\text{s}^{-1}$).

All these inventions radically changed society and share some common characteristics. The founders of quantum mechanics did not foresee these quantum devices. The inventors of these quantum devices did not foresee their applications. Most importantly, these quantum devices do not take full advantage of the power of quantum mechanics.

1.2. THE SECOND QUANTUM REVOLUTION

Some years after the realization that nature is not classical, it was understood that simulations at the quantum level are resource-expensive and, especially, become exponentially demanding with the system size [13, 14]. From this, the idea of using quantum mechanics to simulate quantum mechanics [13] and to build a *quantum computing* machine. Basically, to fight fire with fire.

The possible applications of such a machine are extensive, ranging from pharmaceuticals (drug design) and agriculture (nitrogen fixation) to the sustainability of our planet (energy storage and transportation, and carbon capture) [15]. A quantum computer will be an extremely efficient machine also for the factorization in prime numbers[16], a problem at the basis of encryption, the calculus of logarithms, and the unstructured search [17]. Still, a quantum computer will probably be able to do much more than this, and as it happened with classical computers, the only way to find this out is to build it.

At the basis of quantum information processing, there is the quantum bit (qubit). Like classical bits, this is the smallest unit of information. It is implemented as a well-defined two-level quantum system in which the ground ($|0\rangle$) and excited ($|1\rangle$) states work as the substitutes for the "1" and "0" or "*True*" and "*False*" of classical bits. On the other side, qubits can leverage two quantum properties that make them much more powerful

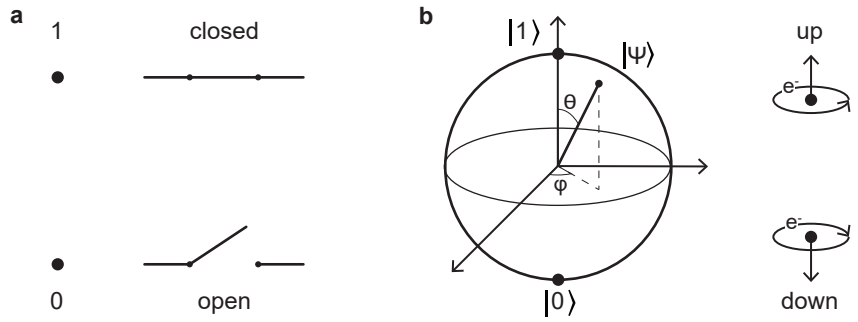


Figure 1.1: **Graphical representations of a classical and quantum bit. a** A classical bit can be either in a 1 (*True*) or 0 (*False*) state. This can be physically implemented using, for example, an electrical switch that can be either "open" *or* "closed." **b** A quantum bit (qubit) can be in any state $|\Psi\rangle$ superposition of the two states $|0\rangle$ and $|1\rangle$. This can be represented as a point on the surface of a sphere, so-called *Bloch sphere,* and parameterized by the angles θ and ϕ. It can be physically implemented by using the spin's state of an electron, which can be in any superposition of the "up" *and* "down" states.

than classical bits: *superposition* and *entanglement*.

Superposition is the property of a quantum system to be in multiple quantum states at the same time— for a qubit to be simultaneously in both the $|0\rangle$ and $|1\rangle$ states. Mathematically, any qubit state ($|\Psi\rangle$) can be expressed as:

$$|\Psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \tag{1.1}$$

where $|0\rangle$ and $|1\rangle$ are called basis states, and α and β are complex coefficients ($\alpha^2 + \beta^2 = 1$). Therefore, every quantum state can be visualized as a point on the surface of a sphere (fig. 1.1), commonly called *Bloch sphere*.

Superposition is a game-changer for computational power. While classical bits can be initialized in either one of the two states and have to perform the computation for each one, quantum systems can be initialized in both states at the same time and complete the computation only once. As the number of states scales exponentially with the number of qubits, a quantum computer could be exponentially more efficient. Already, 20 qubits can assume more than 1 million configurations in parallel (2^{20}).

Entanglement manifests as non-classical correlations affecting distant qubits. Let us imagine that a specific quantum state describing two qubits is:

$$|\Psi\rangle = \alpha\,|0\rangle\,|0\rangle + \beta\,|1\rangle\,|1\rangle \tag{1.2}$$

where α and β are complex coefficients, and the first number between brackets refers to the state of the first qubits and the second number to the second qubit. If we measure the first qubit in the $|0\rangle$ state, then we immediately know the second qubit to be in the $|0\rangle$ state. If we measure the first qubit in the $|1\rangle$ state, then we immediately know the second qubit to be in the $|1\rangle$ state. Entanglement acts as a magic wire connecting multiple qubits, allowing us to operate and measure them simultaneously without the need to "actually" act on all of them.

The combination of these two principles, superposition and entanglement, leads to a massive parallelism of the computation. Not because of computation speed but rather

because the computation power and the complexity of tasks scale differently with problem size.

However, the power of a quantum computer is also its Achilles' heel. While the only possible error in a classical bit is the bit flip — either a "0" misinterpreted as a "1" or vice versa — qubits are susceptible to an infinitely larger number of errors. Any unwanted rotation or movement on the Bloch sphere is a possible quantum error. As a consequence, it is very easy to leak the quantum information through a process known as *decoherence*. Decoherence sets how long the quantum information can be stored and, as a consequence, how many quantum operations can be performed in series. One of today's most researched problems in quantum information processing is to limit decoherence and preserve information losses. The challenge is to build a nearly perfect system out of very imperfect components.

1.2.1. THE DIVINCENZO CRITERIA

While the theory and motivation to pursue a quantum computer are clear, multiple physical platforms still compete to host a quantum processor. To be able to compare and evaluate different systems, David DiVincenzo formulated a series of requirements that a scalable quantum computing platform must satisfy [18]:

- A scalable physical system with well-characterized qubit.
- The ability to initialize the state of the qubits to a simple fiducial state, such as $|00000...\rangle$.
- Long relevant decoherence times, much longer than the gate operation time.
- A "universal" set of quantum gates.
- A qubit-specific measurement capability.

The first requirement asks that the two quantum states $|0\rangle$ and $|1\rangle$ are well separated from each other and that we can create multiple copies to scale the computer size. This sets a first constraint on all the energy scales involved. For example, thermal processes are activated at an energy scale of $E_T = k_B T$, where k_B is the Boltzmann constant. This corresponds to $E_{300K} = 25$ meV at room temperature. In principle, a "well-defined" two-level system will have an energy separation ΔE between the two quantum states $|0\rangle$ and $|1\rangle$ such that $\Delta E \gg E_T$.

Then, we are required to be able to choose the initial state of all the qubits so that the starting state of the computation is deterministic. In the case of spins, this could mean initializing all the qubits in the spin-down state, for example.

The third criterion is the necessary condition to be able to perform multiple quantum operations in series. Since quantum information cannot be stored for a long time, we require the single quantum operations to be much faster than the coherence time so that these are performed while the state of the qubits is still quantum mechanical. The ratio between coherence and operations' time, together with the number of qubits, ultimately sets the complexity of the algorithm that can be run on a specific quantum computer.

As it happens for classical logic operations, it turns out that all the possible quantum gates can be performed once we know how to perform a few particular single and two-qubit operations, forming together a *universal* set. We also have some freedom in choosing this set of quantum gates, so we can choose the most convenient for the specific physical implementation.

Finally, we demand to be able to measure each qubit independently to collect the results of the computation. In quantum mechanics, measuring is an active action. The measurement collapses the quantum state in one of the two states we choose as a basis for the computation, $|0\rangle$ or $|1\rangle$. Therefore, at the end of the computation, we can verify the final state of each qubit.

So far, many different physical platforms have been shown to fulfil some or most of these requirements, motivating scientists to implement qubits in different physical systems. The platforms pursued to date include superconducting circuits[19–21], cold ions[22–24], nuclear magnetic resonance[25, 26], topologically protected states[27, 28], color centers[29, 30], photons[31, 32], and spins[33–35].

1.3. DEVELOPMENT CYCLE OF SILICON-BASED MATERIALS FOR SPIN QUBITS

Classical modern electronics is made out of Silicon (Si). The possibility of reusing the expertise already developed to fabricate classical electronics motivated the development of quantum technologies in semiconductor materials, *e.g.* Si and Ge. Si/SiGe heterostructures confine electrons inside a strained Si quantum well sandwiched between two SiGe layers. Additional gate electrodes on top of the heterostructure stack further confine the electrons in an effective zero-dimensional system called *quantum dot*. Quantum dot spin qubits on Si/SiGe heterostructures are especially appealing thanks to their small footprint, resemblance with classical transistors, and long coherence times [34, 35]. However, despite the many similarities, the more stringent requirements of the quantum computing platform require considering new metrics to fully evaluate performance.

As with classical transistors, a careful engineering of the device architecture and material stack is necessary to obtain the best performance. This is achieved through the iteration of *feedback loops* in which multiple metrics are compared upon variation of others. Figure 1.2 depicts the three macro categories forming a development loop for the Si/SiGe platform. Ideally, a typical single loop gathers information about the crystalline structure and chemical composition of the material stack, the two-dimensional electron gas (2DEG) transport properties, and the measurement of few and single-electron metrics. For each stage, we show an example of a metric already used for classical electronics (left) and a metric that is relevant for spin qubits (right). The typical feedback cycle moves from left to right and starts with the growth of the heterostructure and the structural characterization, passes through the statistical validation of the classical and quantum transport properties, and ultimately seeks to enable a new generation of quantum devices and processors.

The structural and chemical characterization lays at the basis of every development loop. Scanning transmission electron microscopy is a powerful technique to characterize crystalline structures and is used routinely as an in-line diagnostic tool in modern

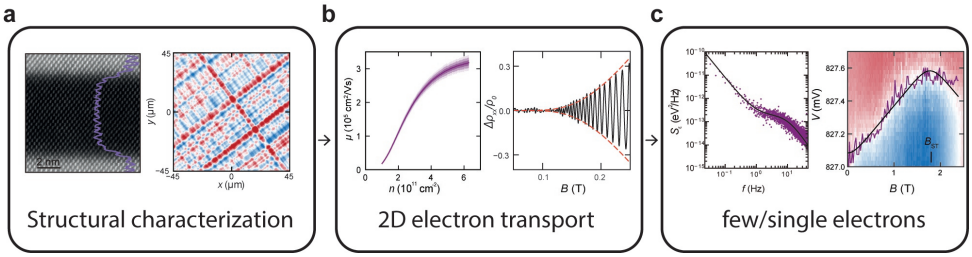


Figure 1.2: **Illustration of the three steps forming a complete material development loop.** Each loop gathers information about the crystalline and chemical composition (**a**), the two-dimensional electron gas (2DEG) transport properties (**b**), and proper metrics of few/single electrons and qubits (**c**). Although the development cycles take great advantage of techniques already developed for the classical electronic, such as STEM, mobility-density, and electrostatic noise (on the left of each box), the peculiarities of the spin qubits demand a more in-depth characterization and consider metrics such as strain fluctuations, quantum mobility, and Valley splitting (on the right of each box).

semiconductor foundries. Figure 1.2(a) shows on the left a high-resolution STEM image of a Si quantum well (dark) sandwiched between SiGe layers (light), with the brightness contrast due to the different chemical compositions. The single atoms forming the crystalline lattice can be recognized. On the right is an atomic force microscopy image of the surface of a Si/SiGe heterostructure. Strain fluctuations in the SiGe substrate arise as a morphological pattern at the surface aligned with the crystallographic directions.

Next, electron transport within the two-dimensional channel is used to characterize the disorder properties at the micrometer scale and validate the first fabrication steps, such as the ohmic contacts and the 2DEG accumulation. Probably the most common metric in classical electronics is electron mobility. Figure 1.2(b) shows a mobility-density curve of the 2DEG accumulated in a Si/SiGe heterostructure, albeit at cryogenic temperatures. At the same time, other properties of the 2DEG are required to fully characterize the material stack. The right panel displays a magnetoresistance curve, which is used to extract the single particle quantum lifetime and quantum mobility. Quantum mobility is influenced by scattering events at all angles; therefore, it is more sensitive than classical mobility to different scattering mechanisms.

Ultimately, the few/single electron properties and qubits metrics are used to benchmark the material. Electrostatic noise is a common problem in classical electronics. On the left is a low-frequency noise spectral density trace measuring the electrical noise power spectral density sensed by a quantum dot in the many-electrons regime. The few-electrons regime makes quantum dot qubits extremely sensitive to electric noise than classical transistors, where many electrons screen such a noise. The necessity to identify well-defined quantum states requires considering metrics such as the single electron valley splitting that are not necessary for classical transistors. On the right is a magnetospectroscopy trace used to evaluate the valley splitting in a quantum dot in the single electron regime.

The complete cycle of the material stack considers all of these parameters with the ultimate ambition of improving spin qubit performances by finding correlations between metrics at different stages of the characterisation loops.

1.4. THESIS OUTLINE

This thesis discusses recent advancements in the Si/SiGe platform tailored for spin qubit applications. The aim is to advance the Si/SiGe heterostructure and optimize disorder, charge noise, and valley splitting while using a comprehensive approach to the material stack to highlight the connection between material characteristics and device performances. This approach adopts metrics familiar to classical transistors as well as new ones that are relevant to single-electron spin qubits.

Chapter 2 reviews the relevant theoretical framework and introduces most of the common language used throughout the manuscript. Starting from the electronic band structure of bulk Si, we describe the effects of strain and confinement on the electronic wave function. We show how these knobs can be tuned to enhance spin qubits performances and focus the attention on a few specific arguments of interest, such as disorder, strain fluctuations, valley splitting, and electric and magnetic noise. At the end of the chapter, we describe the various devices used to quantify performances, the different metrics, and how they relate to each other and the material stack.

Chapter 3 describes the experimental techniques. We describe the growth of the Si/SiGe heterostructure, the device fabrication, and measurement setups. This constitutes a detailed description of the characterization methods adopted in the experiments.

The journey in the material development starts in chapter 4, where we focus on improving the semiconductor-dielectric interface and, thereby, the electrostatic control over charge carriers in the Si quantum well. We challenge the mainstream approach of depositing a sacrificial Si cap and instead terminate the growth with a self-terminating low-temperature exposure to dichlorosilane. As a result, we demonstrate a statistical improvement in uniformity and performance of the 2DEG transport on a 100 mm wafer-scale.

We build upon these results and study in chapter 5 the influence of the semiconductor/dielectric interface and quantum well thickness on the low-frequency charge noise measured statistically on a plethora of quantum dot devices. We find that both parameters affect the charge noise, indicating that both impurities in the dielectrics and amorphous layers and dislocations at the heterogeneous interfaces play a role in shaping the electrostatic landscape.

We complete the feedback loop in chapter 6 with the fine-tuning of the thickness of the ^{28}Si quantum well, where we also provide a quantitative estimation of the average strain and amplitude of the strain fluctuations in the quantum well. Here, we show that such a parameter strongly influences the disorder landscape and suggest a correlation with valley splitting, demonstrating heterostructures able to support low disorder and high valley splitting.

Finally, in chapter 7, we summarize the main results and suggest a few future possible directions of focus to develop the material properties further.

BIBLIOGRAPHY

[1] *Steven Girvin - The Race to Build Quantum Computers (February 12, 2020)*. it-IT. URL: https://www.youtube.com/watch?v=nhUKHf-GN_Y (visited on 12/01/2023).

[2] Max Planck. "Ueber das Gesetz der Energieverteilung im Normalspectrum". en. In: *Annalen der Physik* 309.3 (Jan. 1901), pp. 553–563. ISSN: 0003-3804, 1521-3889. DOI: 10.1002/andp.19013090310. URL: https://onlinelibrary.wiley.com/doi/10.1002/andp.19013090310 (visited on 12/01/2023).

[3] A. Einstein. "Über einen die Erzeugung und Verwandlung des Lichtes betreffenden heuristischen Gesichtspunkt". en. In: *Annalen der Physik* 322.6 (Jan. 1905), pp. 132–148. ISSN: 0003-3804, 1521-3889. DOI: 10.1002/andp.19053220607. URL: https://onlinelibrary.wiley.com/doi/10.1002/andp.19053220607 (visited on 12/01/2023).

[4] G. I. Taylor. "Interference Fringes with Feeble Light". In: *Concepts of Quantum Optics*. Ed. by P. L. Knight and L. Allen. Pergamon, Jan. 1983, pp. 91–92. ISBN: 9780080291604. DOI: 10.1016/B978-0-08-029160-4.50015-4. URL: https://www.sciencedirect.com/science/article/pii/B9780080291604500154 (visited on 12/01/2023).

[5] L. Essen and J. V. L. Parry. "An Atomic Standard of Frequency and Time Interval: A Cæsium Resonator". en. In: *Nature* 176.4476 (Aug. 1955), pp. 280–282. ISSN: 1476-4687. DOI: 10.1038/176280a0. URL: https://www.nature.com/articles/176280a0 (visited on 11/25/2023).

[6] J. C. Hafele and Richard E. Keating. "Around-the-World Atomic Clocks: Predicted Relativistic Time Gains". In: *Science* 177.4044 (1972), pp. 166–168. ISSN: 0036-8075. URL: https://www.jstor.org/stable/1734833 (visited on 11/25/2023).

[7] T. H. Maiman. "Stimulated Optical Radiation in Ruby". en. In: *Nature* 187.4736 (Aug. 1960), pp. 493–494. ISSN: 1476-4687. DOI: 10.1038/187493a0. URL: https://www.nature.com/articles/187493a0 (visited on 11/25/2023).

[8] Arthur L. Schawlow. "Spectroscopy in a New Light". en. In: *Science* 217.4554 (July 1982), pp. 9–16. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.217.4554.9. URL: https://www.science.org/doi/10.1126/science.217.4554.9 (visited on 11/25/2023).

[9] John Bardeen. "Surface States and Rectification at a Metal Semi-Conductor Contact". en. In: *Physical Review* 71.10 (May 1947), pp. 717–727. ISSN: 0031-899X. DOI: 10.1103/PhysRev.71.717. URL: https://link.aps.org/doi/10.1103/PhysRev.71.717 (visited on 11/25/2023).

[10] J. Bardeen and W. H. Brattain. "The Transistor, A Semi-Conductor Triode". In: *Physical Review* 74.2 (July 1948), pp. 230–231. DOI: 10.1103/PhysRev.74.230. URL: https://link.aps.org/doi/10.1103/PhysRev.74.230 (visited on 11/25/2023).

[11] Martin M. Atalla. "Semiconductor devices having dielectric coatings". US3206670A. Sept. 1965. URL: https://patents.google.com/patent/US3206670A/en (visited on 11/25/2023).

[12] Gordon E. Moore. "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff." In: *IEEE Solid-State Circuits Society Newsletter* 11.3 (Sept. 2006), pp. 33–35. ISSN: 1098-4232. DOI: 10.1109/N-SSC.2006.4785860. URL: https://ieeexplore.ieee.org/document/4785860 (visited on 11/25/2023).

[13] Richard P. Feynman. "Simulating physics with computers". en. In: *International Journal of Theoretical Physics* 21.6 (June 1982), pp. 467–488. ISSN: 1572-9575. DOI: 10.1007/BF02650179. URL: https://doi.org/10.1007/BF02650179 (visited on 11/26/2023).

[14] Paul Benioff. "The computer as a physical system: A microscopic quantum mechanical Hamiltonian model of computers as represented by Turing machines". en. In: *Journal of Statistical Physics* 22.5 (May 1980), pp. 563–591. ISSN: 1572-9613. DOI: 10.1007/BF01011339. URL: https://doi.org/10.1007/BF01011339 (visited on 11/26/2023).

[15] Sam McArdle et al. "Quantum computational chemistry". In: *Reviews of Modern Physics* 92.1 (Mar. 2020), p. 015003. DOI: 10.1103/RevModPhys.92.015003. URL: https://link.aps.org/doi/10.1103/RevModPhys.92.015003 (visited on 11/26/2023).

[16] P.W. Shor. "Algorithms for quantum computation: discrete logarithms and factoring". In: *Proceedings 35th Annual Symposium on Foundations of Computer Science*. Nov. 1994, pp. 124–134. DOI: 10.1109/SFCS.1994.365700. URL: https://ieeexplore.ieee.org/document/365700 (visited on 11/27/2023).

[17] Lov K. Grover. "A fast quantum mechanical algorithm for database search". en. In: *Proceedings of the twenty-eighth annual ACM symposium on Theory of computing - STOC '96*. Philadelphia, Pennsylvania, United States: ACM Press, 1996, pp. 212–219. ISBN: 9780897917858. DOI: 10.1145/237814.237866. URL: http://portal.acm.org/citation.cfm?doid=237814.237866 (visited on 11/27/2023).

[18] David P. DiVincenzo. "The Physical Implementation of Quantum Computation". In: *Fortschritte der Physik* 48.9-11 (Sept. 2000), pp. 771–783. ISSN: 00158208. DOI: 10.1002/1521-3978(200009)48:9/11<771::AID-PROP771>3.0.CO;2-E.

[19] Frank Arute et al. "Quantum supremacy using a programmable superconducting processor". en. In: *Nature* 574.7779 (Oct. 2019), pp. 505–510. ISSN: 1476-4687. DOI: 10.1038/s41586-019-1666-5. URL: https://www.nature.com/articles/s41586-019-1666-5 (visited on 12/01/2023).

[20] He-Liang Huang et al. “Superconducting quantum computing: a review”. en. In: *Science China Information Sciences* 63.8 (July 2020), p. 180501. ISSN: 1869-1919. DOI: 10.1007/s11432-020-2881-9. URL: https://doi.org/10.1007/s11432-020-2881-9 (visited on 12/01/2023).

[21] Jens Koch et al. “Charge-insensitive qubit design derived from the Cooper pair box”. In: *Physical Review A* 76.4 (Oct. 2007), p. 042319. DOI: 10.1103/PhysRevA.76.042319. URL: https://link.aps.org/doi/10.1103/PhysRevA.76.042319 (visited on 12/01/2023).

[22] Immanuel Bloch, Jean Dalibard, and Wilhelm Zwerger. “Many-body physics with ultracold gases”. In: *Reviews of Modern Physics* 80.3 (July 2008), pp. 885–964. DOI: 10.1103/RevModPhys.80.885. URL: https://link.aps.org/doi/10.1103/RevModPhys.80.885 (visited on 12/01/2023).

[23] J. I. Cirac and P. Zoller. “Quantum Computations with Cold Trapped Ions”. In: *Physical Review Letters* 74.20 (May 1995), pp. 4091–4094. DOI: 10.1103/PhysRevLett.74.4091. URL: https://link.aps.org/doi/10.1103/PhysRevLett.74.4091 (visited on 12/01/2023).

[24] Giacomo Roati et al. “Anderson localization of a non-interacting Bose–Einstein condensate”. en. In: *Nature* 453.7197 (June 2008), pp. 895–898. ISSN: 1476-4687. DOI: 10.1038/nature07071. URL: https://www.nature.com/articles/nature07071 (visited on 12/01/2023).

[25] Neil A. Gershenfeld and Isaac L. Chuang. “Bulk Spin-Resonance Quantum Computation”. en. In: *Science* 275.5298 (Jan. 1997), pp. 350–356. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.275.5298.350. URL: https://www.science.org/doi/10.1126/science.275.5298.350 (visited on 12/01/2023).

[26] Lieven M. K. Vandersypen et al. “Experimental realization of Shor’s quantum factoring algorithm using nuclear magnetic resonance”. en. In: *Nature* 414.6866 (Dec. 2001), pp. 883–887. ISSN: 1476-4687. DOI: 10.1038/414883a. URL: https://www.nature.com/articles/414883a (visited on 12/01/2023).

[27] A Yu Kitaev. “Unpaired Majorana fermions in quantum wires”. In: *Physics-Uspekhi* 44.10S (Oct. 2001), pp. 131–136. ISSN: 1468-4780. DOI: 10.1070/1063-7869/44/10S/S29. URL: https://iopscience.iop.org/article/10.1070/1063-7869/44/10S/S29 (visited on 12/01/2023).

[28] Chetan Nayak et al. “Non-Abelian anyons and topological quantum computation”. In: *Reviews of Modern Physics* 80.3 (Sept. 2008), pp. 1083–1159. DOI: 10.1103/RevModPhys.80.1083. URL: https://link.aps.org/doi/10.1103/RevModPhys.80.1083 (visited on 12/01/2023).

[29] M. Pompili et al. “Realization of a multinode quantum network of remote solid-state qubits”. en. In: *Science* 372.6539 (Apr. 2021), pp. 259–264. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.abg1919. URL: https://www.science.org/doi/10.1126/science.abg1919 (visited on 12/01/2023).

[30] Peter C. Humphreys et al. “Deterministic delivery of remote entanglement on a quantum network”. en. In: *Nature* 558.7709 (June 2018), pp. 268–273. ISSN: 1476-4687. DOI: 10.1038/s41586-018-0200-5. URL: https://www.nature.com/articles/s41586-018-0200-5 (visited on 12/01/2023).

[31] Han-Sen Zhong et al. “Quantum computational advantage using photons”. en. In: *Science* 370.6523 (Dec. 2020), pp. 1460–1463. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.abe8770. URL: https://www.science.org/doi/10.1126/science.abe8770 (visited on 12/01/2023).

[32] Jeremy L. O’Brien, Akira Furusawa, and Jelena Vučković. “Photonic quantum technologies”. In: *Nature Photonics* 3.12 (Dec. 2009), pp. 687–695. ISSN: 1749-4885. DOI: 10.1038/nphoton.2009.229.

[33] Daniel Loss and David P Divincenzo. *Quantum computation with quantum dots*. Tech. rep. 1998.

[34] R. Hanson et al. “Spins in few-electron quantum dots”. In: *Reviews of Modern Physics* 79.4 (Oct. 2007), pp. 1217–1265. ISSN: 0034-6861. DOI: 10.1103/RevModPhys.79.1217.

[35] Floris A. Zwanenburg et al. “Silicon quantum electronics”. In: *Reviews of Modern Physics* 85.3 (July 2013), pp. 961–1019. DOI: 10.1103/RevModPhys.85.961. URL: https://link.aps.org/doi/10.1103/RevModPhys.85.961 (visited on 05/27/2020).

2

SEMICONDUCTOR STACKS: THEORETICAL CONSIDERATIONS

If quantum mechanics hasn't profoundly shocked you,
you haven't understood it yet

Niels Bohr, Copenhagen, June 1952

2.1. MATERIAL STACKS FOR SEMICONDUCTOR QUANTUM DOTS

The joint effect of the band structure and device engineering produces the three-dimensional electrostatic potential to confine a single charge in a planar heterostructure. The energy band offset between different materials composing the heterostructure traps the charges in a two-dimensional electron (2DEG) or hole (2DHG) gas at the heterojunction. Next, a series of metallic gate electrodes electrically isolated from each other and from the charges at the heterojunction are fabricated on top of the heterostructure. Here, a series of voltages applied to each gate shape the in-plane electrostatic potential and trap the charge carrier in an effectively zero-dimensional system, defining a *quantum dot*.

To date, the most advanced heterostructure stacks hosting quantum dots spin qubits comprise: gallium-arsenide/aluminium-gallium-arsenide (GaAs/AlGaAs) [1], silicon metal-oxide-semiconductor (Si-MOS) [2, 3], silicon/silicon-germanium (Si/SiGe)[4, 5], and germanium/silicon-germanium (Ge/SiGe) [6, 7]. Figure 2.1 provides a schematic representation of these heterostructures and respective material stacks used to fabricate quantum dot spin qubit devices. The material stacks are compared considering the epitaxial and bandstructure properties of the host heterostructure, the quantum dot architectures, the electrical transport properties and the quantum dots and qubit performances. From top to bottom, the table follows the steps already described for the material development loops in fig. 1.2. The specific values compare LossDiVincenzo[8] qubits in the respective platforms that use the spin up ($\langle\uparrow\rangle$) and down ($\langle\downarrow\rangle$) states, separated by the Zeeman energy ($E_Z = 2\mu_B B$), that a charge in an external magnetic field (B) can occupy.

The epitaxy of the heterostructures differentiates in terms of the growth technique (Chemical Vapour Deposition (CVD)/Molecular Beam Epitaxy (MBE)), the nature of the heterointerface (epitaxial/amorphous), the presence of strain in the active channel, the compatibility with the CMOS manufacturing process, the thermal budget, and the possibility of isotopic purification. The properties of each heterostructure are reflected in the band structure and charge carrier properties, such as the effective mass, which influences the energy level spacing and hence the lateral dimensions of the confining potential; the presence of spin-orbit coupling, useful for local coherent manipulation; and the energy separation of the orbital states necessary to guarantee a well-defined two-level system for computation.

The thermal budget and the effective mass are two of the main factors constraining the integration, from a fabrication perspective, of quantum dot devices. Carriers with a large effective mass require tighter electric confinement to isolate the single electron or hole and, therefore, smaller gate electrodes to shape the electrostatic potential. A narrow gate pitch suffers more from dimension non-uniformities among gates and misalignment between different layers, complicating fabrication. The thermal budget constrains all the thermal processes taking place during the fabrication and, for example, forces the adoption of low-temperature techniques for the deposition of dielectrics, which are usually characterized by a high density of interface traps (D_{it}). Moreover, the possibility of contacting the charge carriers with metals diffusing throughout the heterostructure dramatically simplifies the fabrication process. It avoids the use of implantation, which is hard to integrate into small structures.

The two-dimensional (2D) transport properties of the channel offer a first overview

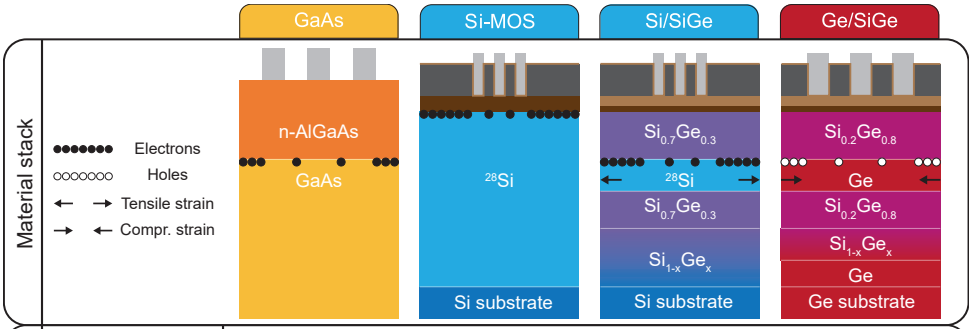
of the disorder present in the different structures. Maximum mobility is a widely used metric to quantify the disorder landscape already employed in classical electronics. However, mobility peaks at high carrier density due to electrostatic screening, a regime typically far away from the single charge occupancy of quantum dot qubits. Percolation density, on the opposite side of the density range, measures the minimum density required to establish a metallic conduction channel and is, therefore, considered a better metric to characterize disorder in the regime relevant for quantum dot spin qubits. In addition, the quantum mobility can be extracted from the envelope of the Shubnikov-de Haas oscillations in the quantum Hall regime and, differently from classical mobility, is affected by scattering from all angles. In particular, comparing classical and quantum mobility allows us to understand the location of the dominant scattering sources.

Ultimately, we benchmark the semiconducting platform using quantum dots and qubit metrics. In the few charges regime, we compare them in terms of a maximum number of dots, *i.e.*, the largest array able to operate single charges with controllable exchange interaction, and low-frequency charge noise at 1 Hz. We also report on the number of qubits, intended as the largest array of simultaneous coherent operations, and compare the relaxation time (T_1), the coherence time extracted from the Gaussian decay typically appearing in a Ramsey experiment and measuring the inhomogeneous dephasing (T_2^*), the coherence time measured under Dynamical Decoupling sequences filtering out low-frequency noise (T_2^{DynD}), the decay of coherent Rabi oscillations (T_2^{Rabi}), and single (F_{1Q}) and two (F_{2Q}) qubit gate fidelities.

The first quantum dots were demonstrated in modulation-doped GaAs/AlGaAs [1] heterostructures thanks to the maturity of the molecular beam epitaxy of III-V compounds [9] and availability of dislocation-free single crystal commercial substrate. High mobility [10, 11] ($10^6 - 10^7$ cm^2/Vs) and low percolation [12] ($< 10^{10}$ cm^{-2}) 2DEGs are easily produced thanks to the small lattice mismatch ($\simeq 0.01$ %) between GaAs and AlGaAs. The extremely clean disorder landscape is confirmed in the quantum Hall regime. Quantum mobility is also very high $\mu_q \approx 10^6$ cm^2/Vs correspondent to a single particle quantum relaxation time of $\tau_q \approx 24$ ps [13]. The single electrons are defined by selectively depleting the 2DEG with Schottky contacts on top of the heterostructure without the need for dielectric layers. The non-degenerate conduction band and light, effective mass ($m^* = 0.067$) allow the definition of the quantum dots using large gate electrodes (≈ 80 nm), easing the fabrication process. Moreover, the large spin-orbit coupling allows addressing single spins with full electrical control [14].

The development of spin qubits in GaAs/AlGaAs heterostructures has been challenging due to the absence of zero-spin isotopes and the incompatibility with the CMOS semiconductor manufacturing process. The former strongly limits coherence time (T_2^*) due to the hyperfine interaction of the electron's spin with the nuclear spin bath of the host material. The latter makes it difficult to leverage advanced semiconductor manufacturing and integrate such devices with on-chip classical electronics, which will probably be necessary to control practical large-scale quantum processors.

These two constraints motivated extensive effort in using Silicon as spin qubit host material. The isotopic purification of the naturally abundant ^{28}Si (≈ 93 %) drastically reduces the hyperfine interactions, boosting the coherence time of more than one order of magnitude [16]. Isotopic purification of a few hundred parts per million (ppm) is nowa-



		GaAs	Si-MOS	Si/SiGe	Ge/SiGe
Heterostructure	Growth technique	MBE	CVD	CVD	CVD
	Heterointerface	Epitaxial	Amorphous	Epitaxial	Epitaxial
	Strain	No	No	Yes	Yes
	CMOS compatible	No	Complete	Yes	Yes
	Thermal budget (°C)	600-800	>1000	750	500
	Isotopic purification	No	Yes	Yes	Yes
	Effective mass (m_e)	0.067	0.19	0.19	0.054
	Spin-orbit coupling	Yes	No	No	Yes
	Excited state energy (meV)	>1	0.3 - 0.8	0.2	>1
Device	Gates size (nm)	>100	30-40	30-40	80
	Dielectric/Dit (cm^{-2})	No	10^{10}	10^{12}	10^{12}
	Ohmic contacts	Metals	Implant	Implant	Metals
2D transp.	Mobility (cm^2/Vs)	10^6-10^7	10^4	10^5	10^6
	Percolation density (10^{10} cm^{-2})	>1	10-20	5	1-2
	Quantum mobility (cm^2/Vs)	10^6	10^4	$7{\cdot}10^4$	$3{\cdot}10^4$
Dots & qubits	Number of dots	3 x 3	2 x 2	9 x 1	4 x 4
	Charge noise ($\mu eV/Hz^{1/2}$)	8.5	0.61	0.9	0.6
	Number of Qubits	3 x 3	2 x 1	6 x 1	2 x 2
	T_1 (s)	57	9	5	0.032
	T_2^* (μs)	0.77	120	21	0.83
	T_2 (ms)	0.87	28	0.87	0.10
	$T_{2\pi}$ (ns)	1.3	110	7	
	F_{1Q} (%)	99.5	99.91	99.92	99.98
	F_{2Q} (%)	90	98.2	99.81	

Figure 2.1: **Material stacks for quantum dot spin qubits.** We compare GaAs/AlGaAs, Si-MOS, Si/SiGe, and Ge/SiGe heterostructures for spin qubits on multiple metrics related to the heterostructure, device fabrication, two-dimensional (2D) electron or hole transport, quantum dots, and spin qubits. Adapted from [15].

days commercially available [17], and a purity of 60 ppm has been demonstrated [18]. Single electron confinement can be implemented at the silicon/silicon-oxide interface in Si-MOS structures or in buried quantum wells in Si/SiGe heterostructures. The larger effective mass ($m^* = 0.19$) requires the quantum dots to have a much smaller dimension than in GaAs [19], making the device fabrication process more challenging. Moreover, the multiple metallic layers necessary to shape the electrostatic potential must be insulated with high-k dielectrics, often deposited at low temperatures via atomic layer deposition, further increasing device process complexity. Still, the compatibility of the Si-MOS platform with the semiconductor manufacturing process already enabled the demonstration of industry-fabricated spin qubits [2].

The presence of two quasi-degenerate conduction band valleys is the major limitation of Si, complicating the qubit initialization, manipulation, and readout[20]. The two-valley energy separation, called *valley splitting*, is a less stringent constraint in Si-MOS where the large electric field at the Si/Silicon-oxide interface permits to obtain reasonable values ($E_{VS} \simeq 1$ meV) [21]. These were the necessary requirements to demonstrate the operation of spin qubits at "hot" temperatures above 1 K [22], encouraging for the integration of the quantum processor with on-chip classical electronics. Unfortunately, the presence of the SiO_x amorphous layer forces the electrons to be close to impurities and charged defects responsible for a strong disorder landscape. For this reason, mobility ($\simeq 10^4$ cm^2/Vs) and percolation density ($\simeq 10^{11}$ cm^{-2}) are very limited in Si-MOS [17], and the control of large devices has proven difficult. The quantum mobility is also rather limited ($\mu_q \approx 13 \times 10^3$ cm^2/Vs equivalent to a quantum lifetime of $\tau_q \approx 1.4$ ps [23]).

Si/SiGe heterostructures overcome this main drawback by confining the electrons at the Si/SiGe epitaxial heterointerface buried 30-50 nm under the surface in an environment characterized by less disorder than Si-MOS. The tensely strained Si quantum well is sandwiched between two Si-rich $Si_{(1-x)}Ge_x$ ($x \approx 0.3$) layers of specific stoichiometric concentration. Here, the absence of pristine SiGe crystalline substrates of specific chemical concentration poses a major challenge to the growth of high-quality Si/SiGe heterostructures. This has been overcome by growing virtual substrates that, starting from Si wafers, increase the Ge concentration in subsequent steps to create the desired $Si_{(1-x)}Ge_x$ substrate under the active layer. The development of virtual substrate with a low density of threading dislocations enabled heterostructures with high mobility ($> 10^5$ cm^2/Vs) and low percolation density ($\simeq 10^{10}$ cm^{-2}) [24, 25] testifying the low level of disorder. Quantum mobility and lifetimes are also higher compared to SiMOS ($\mu_q \approx 75 \times 10^3$ cm^2/Vs, $\tau_q \approx 9$ ps) [25]. The low level of disorder made it possible to control multi-quantum dot devices [26] and linear arrays of qubits [4].

The two current challenges of the Si/SiGe platform are the low average valley splitting compared to Si-MOS and the large dot-to-dot variability of this parameter, which can prevent the isolation of the two-level qubit system. Moreover, the charge noise has also proved to limit the coherence time [27] by coupling to the spin degree of freedom through the magnetic field gradient created by the micromagnets [28].

Conversely, Ge/SiGe heterostructures comprise a compressively strained Ge quantum well between two Ge-rich $Si_{(1-x)}Ge_x$ ($x \approx 0.8$) layers. These are grown in similar conditions as the Si/SiGe platform and have seen fast progress in the last years[6]. The smaller effective mass of holes in these heterostructures [29] ($m^* = 0.055$) allows to de-

fine quantum dots using larger gate electrodes (≈ 80 nm), facilitating the fabrication process. At the same time, the sizeable spin-orbit coupling permits the full-electrical and fast drive of the spin state [30]. In recent years, the utilization of Ge substrates further improved the level of disorder, boosting mobility > 10^6 cm^2/Vs and reducing percolation density (< 10^{10} cm^{-2}) [31]. Quantum mobility and single particle lifetime are comparable with Si/SiGe heterostructures ($\mu_q \approx 25 \times 10^3$ cm^2/Vs and $\tau_q \approx 1$ ps [29]). For these reasons, Ge/SiGe heterostructures have seen an extremely fast development, moving from proof of principle demonstrations [32] to single-qubit [30] and multi-qubit operations [33] in just a few years. Arrays with as many as 16 quantum dots have been demonstrated[34], and ten qubit chips are currently being measured in the laboratory.

In Ge/SiGe, the large g-factor anisotropy [35, 36] and dot-to-dot variability pose a challenge in scaling to large arrays while ensuring single qubit addressability. Moreover, the strong spin-orbit coupling represents a double-edged sword, opening the qubits to decoherence from electrostatic fluctuations and charge noise.

2.2. SI/SIGE HETEROSTRUCTURE

In this thesis, we focus on the Si/SiGe platform tailored to host electron spin qubits. Here, we provide a brief introduction to the band structure of bulk Si, which is used to understand the single electron energy levels achieved in Si/SiGe heterostructures. We then move to analyze the multiple disorder and noise sources that currently limit the operation of electron spin qubits in Si/SiGe heterostructures.

2.2.1. BAND STRUCTURE

Solids are collections of tightly bound atoms. For most solids, these atoms arrange themselves in regular patterns on an underlying crystalline lattice. When the atoms are brought together to form the crystal, their orbitals overlap, and the interaction between orbitals spreads the energy levels to form bands of almost continuous energy levels, *i.e.*, the electronic energy bands. The electronic band structure in solids is a direct consequence of the periodicity of their crystalline lattice and the interaction of the atoms forming the lattice. The smallest unit of this periodicity is called the lattice unit cell.

Silicon (Si) and Germanium (Ge) are group IV semiconductors that crystallize in the diamond cubic structure with a lattice constant of $a_{Si} = 5.43070$Å and $a_{Ge} = 5.65735$Å, respectively [38]. This is a special case of zincblende structure, most typical of III-V semiconductors like Gallium Arsenide (GaAs) and Indium Arsenide (InAs). The zincblende structure can be seen as formed by two interpenetrating face-centered cubic (FFC) structures with the two atoms forming the primitive cell in the origin $d_1 = (0,0,0)$ and at one-fourth of the diagonal of the cube $d_2 = a/4(1,1,1)$. Such lattice has three translation vectors:

$$\tau_1 = \frac{a}{2}(0,1,1) \qquad \tau_2 = \frac{a}{2}(1,0,1) \qquad \tau_3 = \frac{a}{2}(1,1,0) \tag{2.1}$$

These are the directions in which the crystal is symmetric under translations, *i.e.*, the so-called crystallographic axes. Figure 2.2(a) shows the primitive cell formed by these vectors. The entire diamond crystal can be built using translations of such a primitive cell. To fully emphasize the cubic symmetry of the lattice, it is also common to use a larger conventional unit cell (displayed in fig. 2.2(b)).

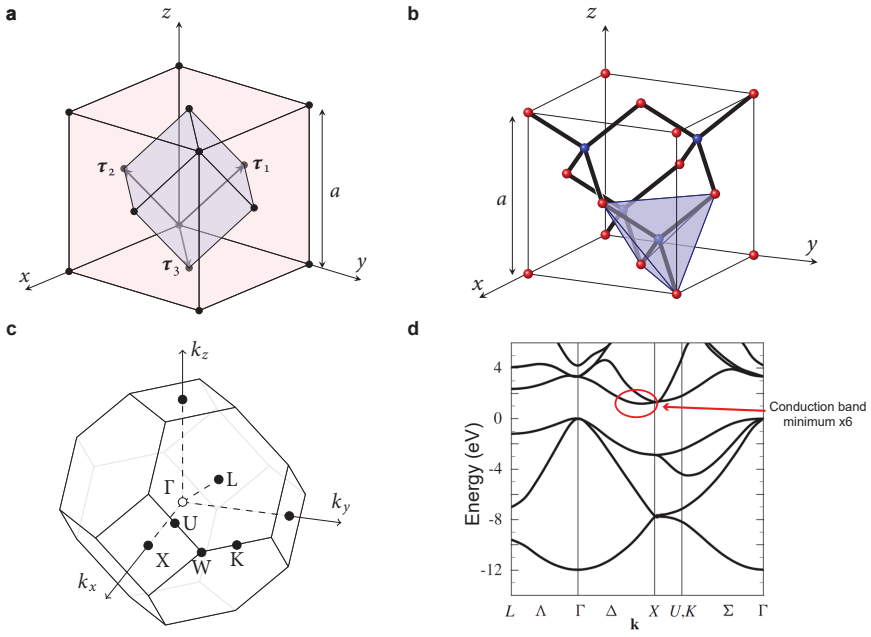


Figure 2.2: **Primitive cell and band structure of Silicon. a** FCC lattice. The primitive vectors τ_1 τ_2 and τ_3 are shown. a is the dimension of the conventional unit cell. The primitive cell is shown in a different colour at the centre. The conventional unit cell emphasizes the full cubic symmetry of the lattice. **b** Conventional unit cell of the zincblende structure. First-neighbor bonds are also shown. Blue and red atoms belong to the two compenetrating FFC cells forming the conventional unit cell. In the case of group IV semiconductors, all the atoms are identical, and the zincblende reduces to the diamond structure. In the zincblende structure, each atom has four first neighbours of the opposite kind, which form a regular tetrahedron centred on the atom. One tetrahedron is shown in blue. **c** Brillouin zone of a crystal with an FCC Bravais lattice. The reciprocal lattice is a body-centred cubic (BCC), and the Brillouin zone is a truncated octahedron centred on $\Gamma = (0,0,0)$. The points of high symmetry are shown. **d** Band structure of crystalline silicon between the symmetry point of the Brillouin zone. The energy zero is set to the Fermi energy. The conduction band minimum instead is located between the Γ and X points. This makes Si an indirect band gap semiconductor with an energy band gap of $E_G = 1.14$ eV. Adapted from [37].

The periodicity in the physical space (x, y, z) translates into a periodicity in momentum space (k_x, k_y, k_z) where another primitive cell can be defined. This is called the Brillouin zone. The Brillouin zone of a diamond lattice assumes the form of a truncated octaedron (BBC) characterized by the three translation vectors:

$$g_1 = \frac{2\pi}{a}(-1,1,1) \qquad g_2 = \frac{2\pi}{a}(1,-1,1) \qquad g_3 = \frac{2\pi}{a}(1,1,-1) \tag{2.2}$$

The BCC Brillouin zone is shown in fig. 2.2(c) together with some high symmetry points. The use of momentum space is particularly useful because the wavefunctions in momentum space are eigenvectors of the Shroedinger equation for an electron in a crystal [37, 39]. Therefore, for each momentum vector, we can calculate an energy. The dispersion relation between momentum vectors and energy is the electronic band structure of the solid.

Figure 2.2(d) shows a portion of the electronic band structure of Si around the Γ symmetry point. The zero of the energy axis is set at the Fermi energy, *i.e.*, the energy of the last electron filling the top of the valence band at the Γ point. The bottom of the conduction band is highlighted with a red circle. This is in between the Γ and X points, making Si a semiconductor with an indirect bandgap semiconductor. Due to the cubic symmetry of Si, the X point is six-fold degenerate, and therefore, the conduction band minimum has the same degeneracy.

2.2.2. STRAINED HETEROSTRUCTURES

The key element of a Si/SiGe heterostructure is a thin Si layer sandwiched between two layers of SiGe. The bandgap in the SiGe alloys is larger than in Si and depends on the Ge concentration. Therefore, the electrons populating the conduction band in the Si layer are confined by two energy walls in a structure called *quantum well*. Moreover, Ge has a 4.2 % larger lattice constant than Si. Therefore, the thin Si layer has to adapt its lattice constant, *i.e. is strained*, to the cladding SiGe. The lattice constant of a relaxed $Si_{1-x}Ge_x$ layer with Ge concentration x ($0 < x < 1$) varies between the lattice constant of Si and Ge. It is described by an empirical relation called Vegard's law [41, 42]:

$$a_{Si_{1-x}Ge_x} = 0.5431 + 0.01992x + 0.002733x^2 \ (nm) \tag{2.3}$$

which is accurate to about 10^{-4} nm.

If a sufficiently thin layer of $Si_{1-x}Ge_x$ is grown on top of a $Si_{1-y}Ge_y$ substrate, the top layer will be compressively strained for $x > y$ and tensely strained for $x < y$ due to the lattice mismatch. In both cases, the strain is in-plane ($\epsilon_x = \epsilon_y = \epsilon_\parallel$), *i.e.*, perpendicular to the growth direction (z). This also results in a perpendicular strain ($\epsilon_\perp$) caused by an opposite distortion of the lattice cell in the z direction due to the fact that the crystalline cell readjusts to minimize the total energy, and resulting in a tetragonal distortion of the unit cell as shown in fig. 2.3(b). The parallel ($\epsilon_\parallel$) and perpendicular ($\epsilon_\perp$) components of the strain tensor can be related by the Poisson ratio (ν) through the relation:

$$\epsilon_\perp = \frac{-2\nu}{1-\nu}\epsilon_\parallel \tag{2.4}$$

which is accurate as long as the strain is fully elastic and uniform in the entire layer.

A strained layer can be grown on a strain-relaxed or bulk $Si_{1-x}Ge_x$ substrate, which is substantially thicker than the epitaxial layer. The first atomic layers grown on such a substrate will be strained and lattice matched to the substrate. In this case, the heterointerface is coherent and pseudomorphic, and the epitaxial layer is forced to have the same in-plane lattice constant of the substrate, consequently reducing its out-of-plane lattice constant following Eq.2.4.

As the thickness of the strained layer increases, there is a critical thickness (t_c) above which it costs too much energy to strain additional heterolayers in coherence with the substrate. As soon as the strained layer thickness exceeds t_c, misfits dislocation at the heterointerface starts to appear and relieve the strain in the epitaxial film (fig. 2.3(c)). The misfit dislocations create subsequent defects called threading dislocations (fig. 2.3(e)), which propagate following a specific 60°through the (110) crystallographic direction. At

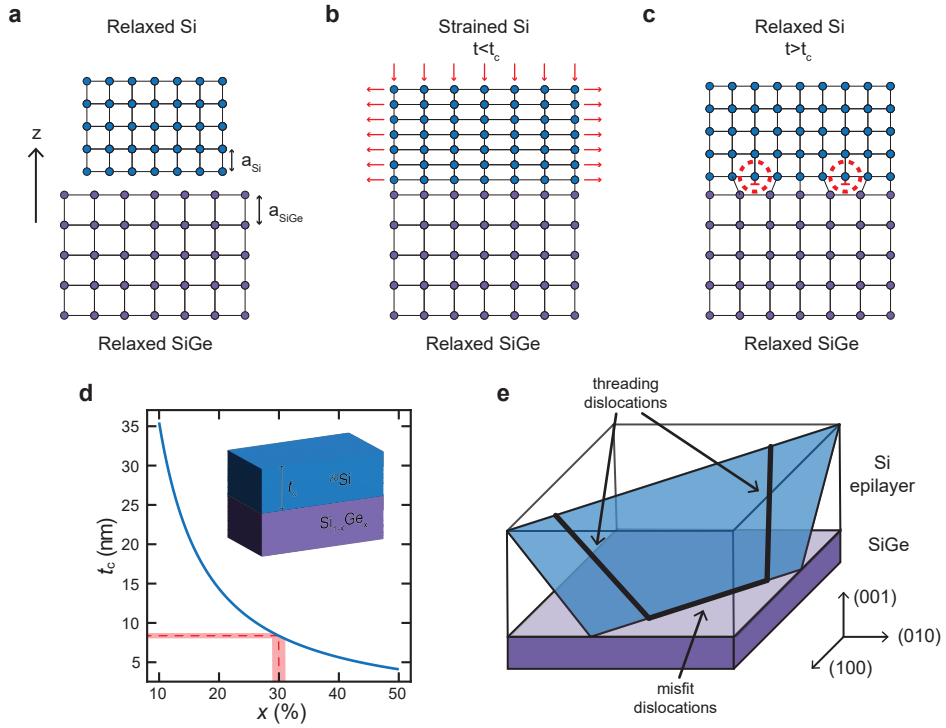


Figure 2.3: **Strain and dislocations in Si/SiGe heterostructure. a** Schematic representation of fully relaxed Si and SiGe layers. The arrow indicates the growth direction *z*. **b** The ^{28}Si epilayer making the quantum well is grown on top of the SiGe strain relaxed buffer. If the thickness of the ^{28}Si quantum well (t) is smaller than the critical thickness (t_c), the epilayer is conformal and pseudomorphic with the virtual substrate. Hence, the quantum well is tensile-strained in the in-plane direction, and there are no strain-induced defects or dangling bonds at the hetero-interface. **c** Growing a Si quantum well beyond the critical thickness triggers relaxation of the epilayer. As a consequence, dangling bonds (in red) and defects start to form at the heterointerface. **d** Critical thickness of a strained silicon epilayer, grown on top of a fully relaxed $Si_{1-x}Ge_x$ substrate, as a function of Ge composition (x) of the underlying relaxed substrate. A Si layer grown on top of a $Si_{70}Ge_{30}$ substrate has a critical thickness of 8.5 nm[40] (red dashed line). Fluctuations in the chemical composition of the substrate will result in a lower local critical thickness, facilitating an early relaxation (red shade). **d** Schematic representation of the crystallographic defects forming after relaxation at the interface between the SiGe and Si layers. As soon as the Si epilayer exceeds the critical thickness and starts to relax, a series of dislocations arises at the SiGe/Si interface. These propagate along the crystallographic directions in-plane called *misfit* dislocations, and out-of-plane called threading dislocations.

this point, the epitaxial layer relaxes, and the defects may interact with the electrical, optical, and thermal properties of the material, typically degrading the performances [40].

An analytic expression for the critical thickness can be obtained by balancing the force of the threading dislocation arm in an uncapped epilayer with the restoring force from the extra interfacial dislocation created during relaxation. In the case of a strained Si layer grown on top of a SiGe relaxed virtual substrate, the People and Bean criterion

based on the Matthews-Blakeslee calculations[43] yield:

$$t_c \approx \frac{b}{4\pi f(1+\nu)}\left(\ln\frac{t_c}{b}+1\right) \tag{2.5}$$

where $b = 0.384$ is the Burgers vector, $\nu = 0.28$ is the Poisson ratio, and f is the lattice mismatch between Si and the relaxed SiGe virtual substrate calculated from eq. (2.3). This critical thickness is plotted in fig. 2.3(d) and predicts a critical thickness of 8.5 nm for a Si layer grown on a $Si_{1-x}Ge_x$ relaxed virtual substrate with 30% Ge concentration. Since the critical thickness is a direct function of the chemical composition, via the lattice mismatch f in eq. (2.5), fluctuations in the chemical composition of the substrate can result in a smaller local critical thickness, favouring an early relaxation of the Si quantum well. Therefore, the choice of the quantum well thickness becomes very critical, as it might be easily overlooked in the design phase of the material stack.

2.3. MATERIAL CHALLENGES AND METRICS

Some of the major improvements in spin qubit performances can be traced down to the advancements of the material science of the host heterostructure [45]. The first Si/SiGe heterostructures used a phosphorous-doped δ-layer to accumulate electrons in the quantum well and depletion gates to confine single electrons. The subsequent adoption of undoped heterostructures, where the δ-layer is removed, and the gate electrodes are used to directly accumulate the electrons, decreased disorder, reduced hysteresis, and gate leakage [46, 47]. Again, the purification of the naturally abundant ^{28}Si isotope boosted the coherence times of more than an order of magnitude by placing the electrons in a nuclear-spin-free magnetic vacuum [48]. Major advances in the materials science of quantum information devices will still be needed to realize large-scale systems. In particular, material issues will be crucial to address in the coming years as the field transitions from few qubits noisy systems to large-scale fault-tolerant quantum processors.

In the following, we identify the critical material challenges that currently limit the progress of electron spin qubits in Si/SiGe heterostructures. We review the theoretical framework leading to the interaction between the single electron spin and the source of decoherence and pinpoint the weaknesses and strengths of such a platform.

2.3.1. DISORDER

We refer to *disorder* as any scattering mechanisms that can interact with the electrons accumulated in the Si/SiGe heterostructure. Scattering centers may also interact with the single electrons and constitute a source of decoherence for the qubit state. Moreover, a low disorder landscape is desirable to ensure uniform control of the single qubits and their interaction. Controlling disorder at different length scales will be, therefore, paramount in scaling to larger quantum devices. Electron mobility (μ) is the standard metric used in classical integrated circuits to quantify disorder. The mobility is related to the average time between two scattering events (τ_t) through the relations:

$$\mu = e\tau_t / m^* \tag{2.6}$$

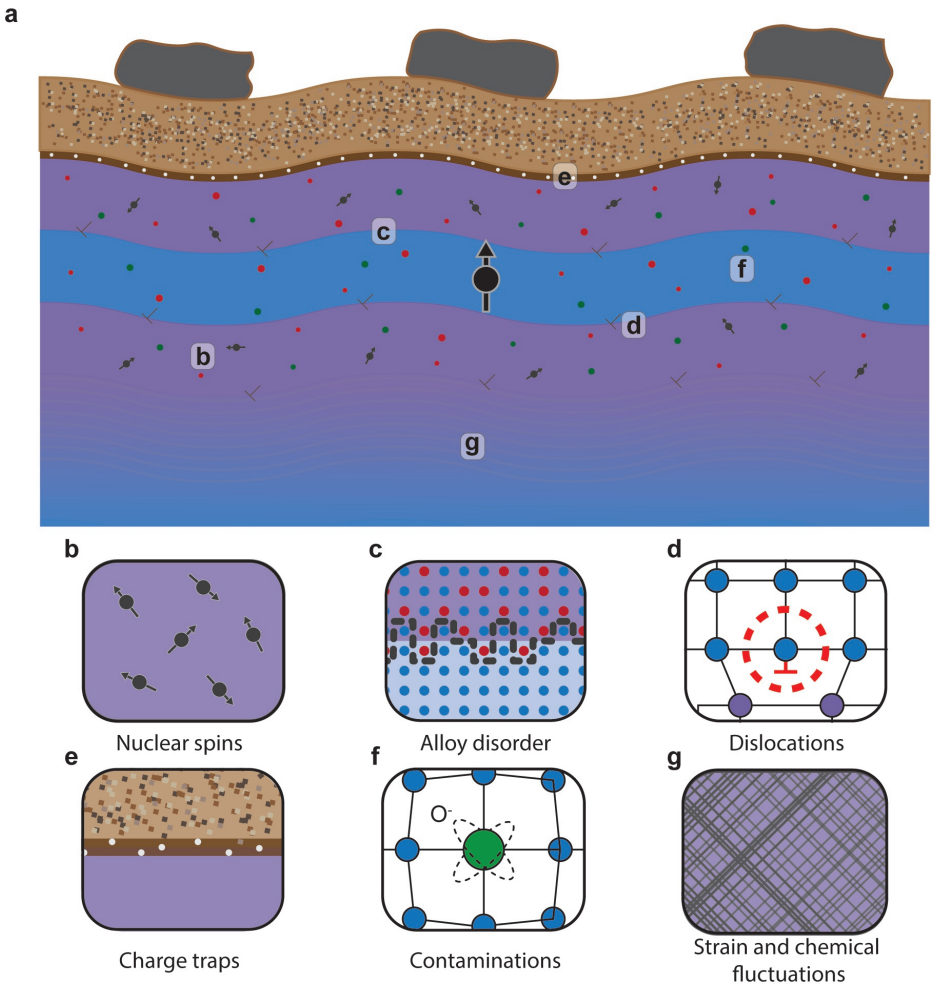


Figure 2.4: **Sources of disorder in Si/SiGe heterostructures. a** Schematic representation of a realistic Si/SiGe heterostructure with the dielectric and metallic gate layers on top. The main layers of the material stack include the SiGe bottom buffer and top spacer (purple), the purified ^{28}Si quantum well (blue), and the AlOx dielectric (brown) used to isolate the metallic gates (grey). The drawings are not in scale, and the amplitude of the topographic undulations arising from the strain-relaxed SiGe buffer (cross-hatch pattern) is magnified for representation purposes. The typical wavelength is of the order of a few microns ($\lambda_{cross-hatch} \approx 5\ \mu$m) with a valley-to-peak amplitude of a few nanometers ($\sigma_{RMS} \approx 2.4$ nm) [44]. This is compared to a typical quantum well thickness of about 5–9 nm and a SiGe barrier on top of about 30-50 nm **b** Nuclear spin fluctuations due to non-zero spin isotopes in non-purified layers lead to increased decoherence coupling directly to the magnetic spin degree of freedom. **c** Since Si and Ge can interchange in the SiGe spacer, the electron wavefunction samples a random Ge concentration that depends on the specific location and causes dot-to-dot variability but also affects valley splitting. **d** Dislocations due to the lattice mismatch between different layers can travel through the virtual substrate and reach the active layers. Moreover, dislocations due to strain relaxation of the Si quantum well directly affect the vicinity of the electron spin qubit. **e** Interface traps and impurities in the amorphous dielectric layers are a major cause of electric noise directly altering the confining potential. **f** Carbon and oxygen contamination in the active layers are strong scattering centers and can greatly increase the disorder landscape. **g** Strain and chemical composition fluctuations in the virtual substrate arise as a morphological modulation at the surface and create in-plane non-uniformities of the band structure.

where e is the electron charge and m^* is the electron effective mass. High mobility indicates a long time between scattering events, a low scattering rate, and, therefore, a low disorder landscape.

Mobility is usually reported at the highest carrier density, where it peaks and assumes the maximum value due to the electrostatic screening of the charges present in the quantum well. However, high electron density is a very different regime compared to the single electron occupation of quantum dots. The percolation density (n_p) is measured in the low-density regime and quantifies the minimum density required to establish a metallic conduction channel [49]. For this reason, it is considered a complementary metric to characterize the disorder landscape in a regime closer to the spin qubit operation [29]. It is extracted by fitting the longitudinal conductivity (σ_{xx}) as a function of density (n) curve with the function [50]:

$$\sigma_{xx} \propto (n - n_p)^{1.31} \tag{2.7}$$

where n_p is the extracted percolation density, and the critical exponent 1.31 is theoretically extracted under the assumption of two-dimensional transport.

Although classical mobility and percolation density are already informative metrics of the disorder landscape, transport properties in the quantum Hall regime give further insights into the scattering phenomena. Classical mobility strongly depends on the scattering process in the same direction as the charge's motions. On the other hand, quantum mobility considers scattering phenomena at all angles. For this reason, it is a more informative and sensible metric of the disorder landscape because it does not exclude a priori scattering sources which could influence qubit performance. The difference between the classical transport (τ_t) and quantum single-particle (τ_q) relaxation times can be understood by comparing their theoretical expressions [13, 51]:

$$\frac{1}{\tau_t} = \int_0^\pi Q(\theta)(1 - \cos\theta)\, d\theta \qquad \text{and} \qquad \frac{1}{\tau_q} = \int_0^\pi Q(\theta)\, d\theta \tag{2.8}$$

where $Q(\theta)$ is proportional to the probability of scattering through an angle θ. The presence of the factor $1 - \cos\theta$ makes the transport scattering time only sensitive to forward scattering events at low angles, such as impurities in the quantum well or the roughness of the interface. Conversely, the quantum lifetime is also sensitive to high-angle scattering events, such as remote impurities and fluctuations in the gate stack [25], which could be very relevant to qubit performance metrics.

2.3.2. VALLEY SPLITTING

The conduction band minimum of bulk silicon features a six-fold degeneracy called "valleys." The strain induced in the quantum well in Si/SiGe heterostructures breaks the cubic bulk symmetry into in-plane ($+k_x$, $-k_x$, $+k_y$, $-k_y$) and out-of-plane ($+k_z$, $-k_z$) components. As a consequence, the four in-plane valleys (Δ_4) rise in energy, and the two out-of-plane valleys (Δ_2) stay isolated at lower energies [53]. The remaining two-fold degeneracy of the Δ_2 valleys is lifted by the external electric field (E), confining the electrons at the Si/SiGe heterointerface and breaking the symmetry in the growth direction (z). The energy separation between the two low-lying valley states is called *valley*

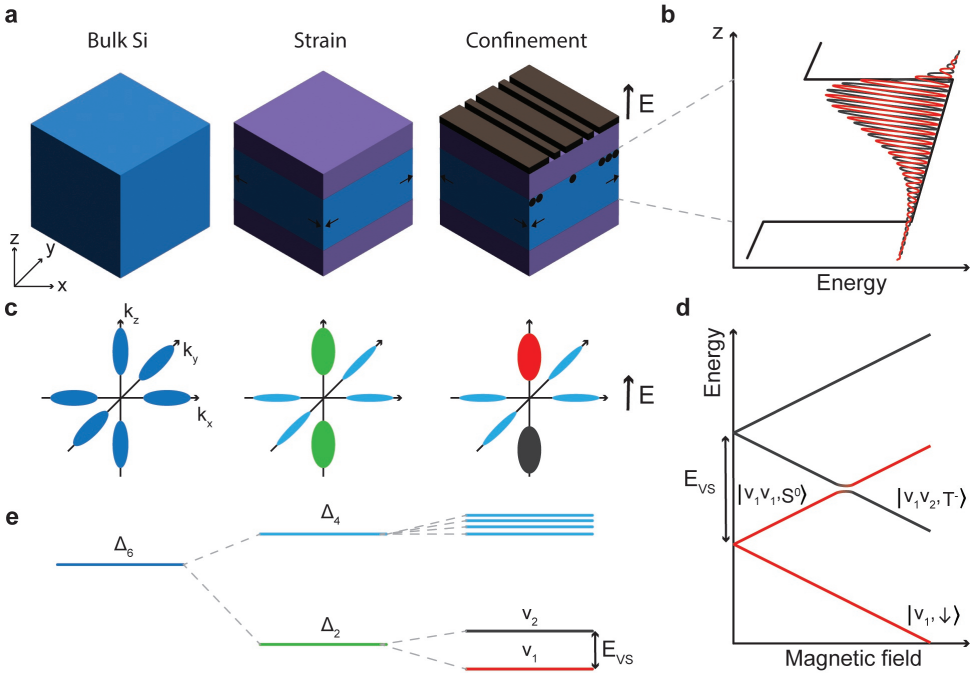


Figure 2.5: **Valley splitting in Si/SiGe. a** The six degenerate valley states of the conduction band in bulk Si split thanks to the combination of strain created by the heterostructure and confinement induced by the electric field (E). The strain is caused by the lattice mismatch between Si and SiGe. The confinement is due to the voltages applied to the top gates confining the electrons in the Si quantum well. **b** Schematic representation of the single electron wavefunction of the first (v_1, red) and second (v_2, black) valley states. The electric field pushes part of the wavefunction inside the SiGe barrier. Inspired by [52]. **c** Constant energy surfaces in momentum (k) space. In bulk Silicon, all directions are symmetric. First, the in-plane strain breaks the symmetry in the z direction, which is further lifted by the electric field in the same direction. **d** Energy representation of the lowest spin and valley states for one and two electrons confined in a quantum dot as a function of the magnetic field. For a sufficiently high magnetic field, the Zeeman splitting equals the valley splitting, and the two-electron state changes from $|v_1\, v_1, S^0\rangle$ to $|v_1\, v_2, T^-\rangle$. **e** Schematic representation of the subsequent splitting of the six degenerate valleys (Δ_6) into single energy states. Inspired by [52].

splitting (E_{VS}). [1] Controlling and maximizing this splitting is critical for Si-based spin qubits, as it is typically the lowest energy excitation next to the two-level spin up and down system defining the qubit and set by the Zeeman splitting.

Multiple theories have been developed to understand the underlying physics, and practical strategies have been put forward to enhance such valley splitting [55]. In the assumption of quantum well with sharp heterointerfaces ($\delta(z - z_i)$), the valley mixing (Δ_{VS}) can be expressed as [56, 57]:

$$\Delta_{VS} = v_0 F(z) e^{2ik_z z_i} \tag{2.9}$$

[1] In Si-MOS, the channel is not strained. However, the strong confinement at the Si/SiOx interface and the effective mass anisotropy increase the energy of the Δ_4 valleys and further split the Δ_2 valleys typically more than in Si/SiGe heterostructures[54].

where v_0 is the interfacial valley coupling, $F(z)$ is the valley-free envelope function, k_z is the reciprocal vector in momentum space and z_i is the interface position. The valley splitting can be calculated as $E_{VS} = 2|\Delta_{VS}| \propto |F(z_i)|^2$. This means that the amplitude of the valley splitting is dependent on the overlap of the electron wavefunction with the interface. At the same time, Δ_{VS} oscillates with a frequency set by k_z ($k_z > 1/(a_{Si}/2) \approx 0.18$ Å^{-1}) These are extremely fast oscillations with a period similar to the interatomic spacing, which makes the valley splitting extremely sensitive to the specific atomic characteristic of the heterointerface between Si and SiGe at the quantum dot location, causing great dot-to-dot variability. Figure 2.5(b) shows a representation of the electronic wavefunction for the first (red) and second (black) valley states.

Valley splitting also impacts the readout of semiconductor spin qubits [58]. The Pauli spin blockade (PSB) spin-to-charge conversion scheme relies on the energy separation (E_{ST}) between the antisymmetric (Singlet) and symmetric (Triplet) two spin states to recognize different single spin configurations. If the valley splitting is too small and comparable with such energy scale ($E_{VS} \approx E_{ST}$), the identification of the singlet and triplet states becomes impossible and therefore the spin readout [4, 58].

Magnetospectroscopy is a powerful technique to ensure that the valley degree of freedom is well separated from the Singlet and Triplet states. It is performed by scanning the $1 \rightarrow 2$ electron transition as a function of the magnetic field. Figure 2.5(d) shows the energy dispersion of the first four electronic states in a single quantum dot as a function of the magnetic field (B) and in the assumption of $E_{ST} \ll E_{VS}$. For low magnetic fields such that the Zeeman splitting (E_Z) is lower than the valley splitting ($E_Z < E_{VS}$), the two electrons will have the same valley state (v_1). As a consequence, the spin state will account for the total antisymmetric part of the wavefunction and, therefore, will be a singlet state ($|S_0\rangle = |\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle$). By increasing the magnetic field, the Zeeman splitting will increase and become greater than the valley splitting ($E_Z > E_{VS}$) for a certain magnetic field. In this case, the second electron will be loaded in the second valley state (v_2), which has the opposite symmetry. Therefore, the valley wavefunction is antisymmetric, and the two-electron spin can be in the symmetric combination, *i.e.*, $|\downarrow\downarrow\rangle = |T^-\rangle$. Note that changing from $|S_0\rangle \rightarrow |T^-\rangle$ costs an additional energy equal to the Singlet-Triplet splitting E_{ST}. For this reason, the kink position will be at an energy equal to $E_{kink} = g\mu_B B = E_{VS} - E_{ST}$, which can be approximated with E_{VS} in the limit of $E_{ST} \ll E_{VS}$, *i.e.*, if the two energy scales are well separated. The possibility of measuring a well-defined kink at a certain magnetic field already guarantees that $E_{ST} \ll E_{VS}$.

2.3.3. STRAIN NOISE

Si-MOS homostructures and GaAs/AlGaAs heterostructures rely on a single-crystal substrate on top of which the active layers are grown lattice-matched, *i.e.*, coherently and pseudomorphically. In Si/SiGe heterostructures, the absence of a single crystal SiGe substrate of desired chemical concentration and sufficient structural quality forces the adoption of an alternative solution, typically *i.e.*, the growth of a SiGe *virtual substrates*. The virtual substrate aims to create a SiGe epitaxial buffer with the desired lattice parameter by tuning accordingly the SiGe chemical composition and intentionally inducing strain-relaxation by growing thick layers above the critical thickness. The growth starts on top of a silicon substrate and uses a series of strained relaxed $Si_{1-x}Ge_x$ layers where

the Ge chemical composition x is varied to reach the desired ratio. With the convention that x refers to the Ge concentration in the $Si_{1-x}Ge_x$ alloy, since the chemical composition is ramped up towards the final value, virtual substrates grown with such a scheme are called *forward grading*.

Each layer of the virtual substrate is grown to be thicker than the respective critical thickness and, therefore, fully relaxed. The strain relaxation is carried out by the misfit dislocation network at the heterointerface propagating from each interface [42]. This process has a series of consequences. First, the presence of misfit dislocations automatically creates 60°threading dislocations traveling through the epitaxial layers. Moreover, the piling up of such misfit dislocations creates islands distributed along the crystallographic directions, where the nucleation of Ge is preferred during the growth [59]. As a result, the relaxed SiGe buffers are characterized by in-plane chemical and strain fluctuations manifesting as an undulated surface morphology known as *crosshatch* pattern [60–62]. The crosshatch is characteristic of substrates with lattice mismatch lower than 2% and low density of misfits dislocation in the relaxed layers down to $10^4 - 10^6$ cm^{-2} [40]. The roughening can affect the electron mobility [63] and, most importantly, results in a strain modulation of the strained Si layer grown on top [61]. This roughening is a major hurdle for CMOS integration because it makes aligning the extreme ultraviolet lithography tools difficult. Even though such morphology can be cured with chemical mechanical polishing (CMP) techniques, the strain modulation field remains an additional degree of variability. Despite these limitations and decades after their invention, strained-relaxed SiGe buffers are still the mainstream way to achieve strained Si quantum wells.

Another source of strain fluctuations arises from the gate and device stack [64]. The amplitude of the strain tensor due to electrode-induced strain is of ≈ 0.5 % with a bandwidth of ≈ 0.02 %. In Si/SiGe, the average strain of the Si quantum well is ≈ 1.3 % with a bandwidth, due to the cross-hatch pattern, of ≈ 0.1 % [44]. Therefore, strain fluctuations driven by the misfit dislocation network drive a larger variability. However, the strain induced by the electrodes has a much shorter wavelength than the strain induced by the cross-hatch pattern ($\lambda_{gates} \approx 0.1\ \mu m \ll \lambda_{Cross-Hatch} \approx 5 \mu m$) and can induce a substantial shift in the quantum well average strain [65]. For this reason, recent proposals use a careful gate design to reduce the induced strain fluctuations [66]. On the other side, the device fabrication process could also be used to enhance performance. Another proposal uses a careful etching of the heterostructure around the quantum dots to induce shear strain in the quantum well and improve valley splitting [67].

In the Si/SiGe heterostructure, the strain of the Si layer is responsible for lifting the degeneracy of the conduction band, and the chemical composition of the SiGe buffer is related to the band gap. Understanding and minimizing such fluctuations will be paramount in scaling quantum technologies on Si/SiGe heterostructures and ensuring the full compatibility of this platform with planar integrated circuit technologies.

2.3.4. CHARGE NOISE

Charge noise is currently identified as the major limitation to the performances of semiconductor spin qubits [4, 27]. We refer to charge noise as random and unwanted electric field fluctuations in the vicinity of the spin qubit. Although electrostatic noise does not

couple directly with the spin degree of freedom, the use of spin-to-charge conversion for readout and the synthetic spin-orbit interaction from the micromagnets necessary to ensure addressability allow charge noise to dephase and decohere the spin state. Charge noise may be caused by fluctuating defects in the heterostructure [68] (dislocations, contaminations, *e.g.*, carbon and oxygen) and in the gate stack [69] (interface traps, strain mismatch), by spurious voltage noise originating from the control electronics, or from the random motion of charges anywhere in the device. The typical charge noise power spectral density in semiconductor devices follows a $1/f$ power law [70]. Such behaviour has been measured in Si/SiGe qubits over 13 decades of frequencies [71]. Moreover, the specific shape of the power spectral density, deviations from the $1/f$ behaviour, and temperature dependence can help distinguish the nature of the noise sources[72]. For example, a "pure" $1/f$ behaviour is usually related to a quasi-continuous ensemble of two-level-fluctuators (TLF). In contrast, a Lorentian $1/f^2$ behaviour is caused by a single TLF strongly coupling to the system.

Charged defects can also lead to unwanted accumulation or depletion of electrons in parasitic quantum dots, complicating the device tuning [73, 74]. Strain fields due to the elastic distortion at low temperatures of the metallic gates could have similar results, motivating the use of polysilicon [74] and palladium gates [75].

Semiconductor spin qubits are defined and operated by electrostatic potentials. While material choices and careful gate stack engineering may improve charge-noise-induced decoherence, the underlying noise sources are unlikely to be removed from semiconductor devices [76] (unlike hyperfine interaction from magnetic noise) This is particularly true in the Si/SiGe platform, where the dielectric has so far been fabricated using low-temperature atomic layer deposition, which is known to have a high density of interface traps. Striking a balance between robustness to electric noise while guaranteeing effective control of the spin state will remain a key trade-off to pursue in designing semiconductor spin qubits across multiple materials and designs.

2.3.5. MAGNETIC NOISE

All Ga and As isotopes carry a $I = 3/2$ nuclear spin that strongly limits coherence time in the GaAs/AlGaAs platform to $T_2^* \approx 10$ ns [1]. On the contrary, Si and Ge have naturally abundant zero-spin isotopes with remaining concentrations of 4.7 % (^{29}Si, $I = 1/2$) and 7.8 % (^{73}Ge, $I = 9/2$). These values can be further lowered through isotopic purification down to the few tens of parts per million, placing the electrons in a nuclear spin-free magnetic vacuum [17, 77]. Contrary to charge noise, magnetic noise from the host semiconductor can be reduced to a very low level through isotopic purification [78].

In addition to isotopic content, the size of the electronic wavefunction defines the amplitude of the hyperfine interaction. In the limit of interaction with many nuclei (continuous limit), the dephasing time (T_2^*) can be expressed as [76]:

$$T_2^* \propto \sqrt{\frac{N}{P_I}} \tag{2.10}$$

where N is the total number of nuclei for which the electron wavefunction is larger than some threshold, and P_I is the probability that a given lattice nucleus has spin.

Therefore, in this many nuclei limit, the wave function overlapping with a larger number of spin-carrying nuclear will have a longer coherence time [76]. In semiconductor spin qubits, the dimension of the electronic wave function is mainly set by the effective mass, which could result in a larger variability of the dephasing times in platforms with larger effective mass, such as Si/SiGe [4], and in more uniform values in platforms with a smaller effective mass, such as Ge/SiGe [33].

BIBLIOGRAPHY

[1] J. R. Petta et al. “Coherent Manipulation of Coupled Electron Spins in Semiconductor Quantum Dots”. en. In: *Science* 309.5744 (Sept. 2005), pp. 2180–2184. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.1116955. URL: https://www.science.org/doi/10.1126/science.1116955 (visited on 11/22/2023).

[2] A. M. J. Zwerver et al. “Qubits made by advanced semiconductor manufacturing”. In: *Nature Electronics* 5.3 (Mar. 2022), pp. 184–190. ISSN: 2520-1131. DOI: 10.1038/s41928-022-00727-9.

[3] M. Veldhorst et al. “An addressable quantum dot qubit with fault-tolerant control-fidelity”. en. In: *Nature Nanotechnology* 9.12 (Dec. 2014), pp. 981–985. ISSN: 1748-3387, 1748-3395. DOI: 10.1038/nnano.2014.216. URL: http://www.nature.com/articles/nnano.2014.216 (visited on 05/27/2020).

[4] Stephan G. J. Philips et al. “Universal control of a six-qubit quantum processor in silicon”. In: *Preprint at http://arxiv.org/abs/2202.09252* (Feb. 2022). URL: http://arxiv.org/abs/2202.09252.

[5] B M Maune et al. “Coherent singlet-triplet oscillations in a silicon-based double quantum dot”. In: *Nature* 481.7381 (2012), pp. 344–347. ISSN: 00280836. DOI: 10.1038/nature10707. URL: http://dx.doi.org/10.1038/nature10707.

[6] Giordano Scappucci et al. “The germanium quantum information route”. In: *Nature Reviews Materials* 6.10 (Oct. 2021), pp. 926–943. ISSN: 2058-8437. DOI: 10.1038/s41578-020-00262-z.

[7] N. W. Hendrickx et al. “Fast two-qubit logic with holes in germanium”. en. In: *Nature* 577.7791 (Jan. 2020), pp. 487–491. ISSN: 1476-4687. DOI: 10.1038/s41586-019-1919-3. URL: https://www.nature.com/articles/s41586-019-1919-3 (visited on 12/19/2023).

[8] Daniel Loss and David P Divincenzo. *Quantum computation with quantum dots*. Tech. rep. 1998.

[9] Michael J. Manfra. “Molecular Beam Epitaxy of Ultra-High-Quality AlGaAs/GaAs Heterostructures: Enabling Physics in Low-Dimensional Electronic Systems”. en. In: *Annual Review of Condensed Matter Physics* 5.1 (Mar. 2014), pp. 347–373. ISSN: 1947-5454, 1947-5462. DOI: 10.1146/annurev-conmatphys-031113-133905. URL: https://www.annualreviews.org/doi/10.1146/annurev-conmatphys-031113-133905 (visited on 11/24/2023).

[10] J. P. Eisenstein et al. “Insulating and Fractional Quantum Hall States in the First Excited Landau Level”. In: *Physical Review Letters* 88.7 (Jan. 2002), p. 076801. DOI: 10.1103/PhysRevLett.88.076801. URL: https://link.aps.org/doi/10.1103/PhysRevLett.88.076801 (visited on 11/24/2023).

[11] Y. Ashlea Alava et al. “High electron mobility and low noise quantum point contacts in an ultra-shallow all-epitaxial metal gate GaAs/Al *x* Ga1- *x* As heterostructure”. en. In: *Applied Physics Letters* 119.6 (Aug. 2021), p. 063105. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0053816. URL: https://pubs.aip.org/apl/article/119/6/063105/41858/High-electron-mobility-and-low-noise-quantum-point (visited on 12/08/2023).

[12] M. J. Manfra et al. “Transport and Percolation in a Low-Density High-Mobility Two-Dimensional Hole System”. In: *Physical Review Letters* 99.23 (Dec. 2007), p. 236402. DOI: 10.1103/PhysRevLett.99.236402. URL: https://link.aps.org/doi/10.1103/PhysRevLett.99.236402 (visited on 11/24/2023).

[13] Qi Qian et al. “Quantum lifetime in ultrahigh quality GaAs quantum wells: Relationship to Δ 5/2 and impact of density fluctuations”. In: *Physical Review B* 96.3 (2017), p. 035309.

[14] K. C. Nowack et al. “Coherent Control of a Single Electron Spin with Electric Fields”. en. In: *Science* 318.5855 (Nov. 2007), pp. 1430–1433. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.1148092. URL: https://www.science.org/doi/10.1126/science.1148092 (visited on 11/24/2023).

[15] Giordano Scappucci. “Semiconductor materials stacks for quantum dot spin qubits”. In: *MRS Bulletin* 46.7 (July 2021). arXiv:2102.10897 [cond-mat], pp. 596–606. ISSN: 0883-7694, 1938-1425. DOI: 10.1557/s43577-021-00147-8. URL: http://arxiv.org/abs/2102.10897 (visited on 12/12/2023).

[16] Floris A. Zwanenburg et al. “Silicon quantum electronics”. In: *Reviews of Modern Physics* 85.3 (July 2013), pp. 961–1019. DOI: 10.1103/RevModPhys.85.961. URL: https://link.aps.org/doi/10.1103/RevModPhys.85.961 (visited on 05/27/2020).

[17] D. Sabbagh et al. “Quantum Transport Properties of Industrial 28Si/28Si O2”. In: *Physical Review Applied* 12.1 (July 2019), p. 014013. ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.12.014013.

[18] N. V. Abrosimov et al. “A new generation of 99.999% enriched 28Si single crystals for the determination of Avogadro’s constant”. en. In: *Metrologia* 54.4 (July 2017), p. 599. ISSN: 0026-1394. DOI: 10.1088/1681-7575/aa7a62. URL: https://dx.doi.org/10.1088/1681-7575/aa7a62 (visited on 11/24/2023).

[19] WIL Lawrie et al. “Quantum dot arrays in silicon and germanium”. In: *Applied Physics Letters* 116.8 (2020), p. 080501.

[20] M. G. Borselli et al. “Pauli spin blockade in undoped Si/SiGe two-electron double quantum dots”. In: *Applied Physics Letters* 99.6 (Aug. 2011), p. 063109. ISSN: 0003-6951. DOI: 10.1063/1.3623479.

[21] C. H. Yang et al. “Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting”. en. In: *Nature Communications* 4.1 (June 2013), p. 2069. ISSN: 2041-1723. DOI: 10.1038/ncomms3069. URL: https://www.nature.com/articles/ncomms3069 (visited on 05/27/2020).

[22] L. Petit et al. “Universal quantum logic in hot silicon qubits”. en. In: *Nature* 580.7803 (Apr. 2020), pp. 355–359. ISSN: 1476-4687. DOI: 10.1038/s41586-020-2170-7. URL: https://www.nature.com/articles/s41586-020-2170-7 (visited on 05/27/2020).

[23] Asser Elsayed et al. *Low charge noise quantum dots with industrial CMOS manufacturing*. arXiv:2212.06464 [cond-mat, physics:quant-ph]. Dec. 2022. DOI: 10.48550/arXiv.2212.06464. URL: http://arxiv.org/abs/2212.06464 (visited on 12/11/2023).

[24] Brian Paquelet Wuetz et al. “Effect of Quantum Hall Edge Strips on Valley Splitting in Silicon Quantum Wells”. In: *Physical Review Letters* 125.18 (Oct. 2020), p. 186801. DOI: 10.1103/PhysRevLett.125.186801. URL: https://link.aps.org/doi/10.1103/PhysRevLett.125.186801 (visited on 12/08/2023).

[25] Davide Degli Esposti et al. “Wafer-scale low-disorder 2DEG in 28Si/SiGe without an epitaxial Si cap”. en. In: *Applied Physics Letters* 120.18 (May 2022), p. 184003. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0088576. URL: https://pubs.aip.org/apl/article/120/18/184003/2833621/Wafer-scale-low-disorder-2DEG-in-28Si-SiGe-without (visited on 07/10/2023).

[26] A. R. Mills et al. “Shuttling a single charge across a one-dimensional array of silicon quantum dots”. en. In: *Nature Communications* 10.1 (Mar. 2019), p. 1063. ISSN: 2041-1723. DOI: 10.1038/s41467-019-08970-z. URL: https://www.nature.com/articles/s41467-019-08970-z (visited on 08/30/2022).

[27] J. Yoneda et al. “Coherent spin qubit transport in silicon”. en. In: *Nature Communications* 12.1 (July 2021), p. 4114. ISSN: 2041-1723. DOI: 10.1038/s41467-021-24371-7. URL: https://www.nature.com/articles/s41467-021-24371-7 (visited on 09/01/2022).

[28] Allen Kha, Robert Joynt, and Dimitrie Culcer. “Do micromagnets expose spin qubits to charge and Johnson noise?” In: *Applied Physics Letters* 107.17 (Oct. 2015), p. 172101. ISSN: 0003-6951. DOI: 10.1063/1.4934693.

[29] Mario Lodari et al. “Low percolation density and charge noise with holes in germanium”. In: *Materials for Quantum Technology* 1.1 (2021), p. 11002. URL: https://iopscience.iop.org/article/10.1088/2633-4356/abcd82.

[30] N. W. Hendrickx et al. “Fast two-qubit logic with holes in germanium”. In: *Nature* 577.7791 (Jan. 2020), pp. 487–491. ISSN: 0028-0836. DOI: 10.1038/s41586-019-1919-3.

[31] Lucas E. A. Stehouwer et al. “Germanium wafers for strained quantum wells with low disorder”. en. In: *Applied Physics Letters* 123.9 (Aug. 2023), p. 092101. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0158262. URL: https://pubs.aip.org/apl/article/123/9/092101/2908280/Germanium-wafers-for-strained-quantum-wells-with (visited on 12/08/2023).

[32] Amir Sammak et al. “Shallow and Undoped Germanium Quantum Wells: A Playground for Spin and Hybrid Quantum Technology”. en. In: *Advanced Functional Materials* 29.14 (2019), p. 1807613. ISSN: 1616-3028. DOI: 10.1002/adfm.201807613. URL: https://onlinelibrary.wiley.com/doi/abs/10.1002/adfm.201807613 (visited on 05/27/2020).

[33] Nico W. Hendrickx et al. “A four-qubit germanium quantum processor”. en. In: *Nature* 591.7851 (Mar. 2021), pp. 580–585. ISSN: 1476-4687. DOI: 10.1038/s41586-021-03332-6. URL: https://www.nature.com/articles/s41586-021-03332-6 (visited on 11/24/2023).

[34] Francesco Borsoi et al. “Shared control of a 16 semiconductor quantum dot crossbar array”. en. In: *Nature Nanotechnology* (Aug. 2023), pp. 1–7. ISSN: 1748-3395. DOI: 10.1038/s41565-023-01491-3. URL: https://www.nature.com/articles/s41565-023-01491-3 (visited on 12/11/2023).

[35] N. W. Hendrickx et al. *Sweet-spot operation of a germanium hole spin qubit with highly anisotropic noise sensitivity*. arXiv:2305.13150 [cond-mat, physics:quant-ph]. May 2023. DOI: 10.48550/arXiv.2305.13150. URL: http://arxiv.org/abs/2305.13150 (visited on 11/24/2023).

[36] Andrew J. Miller et al. “Effective out-of-plane g factor in strained-Ge/SiGe quantum dots”. In: *Physical Review B* 106.12 (Sept. 2022), p. L121402. DOI: 10.1103/PhysRevB.106.L121402. URL: https://link.aps.org/doi/10.1103/PhysRevB.106.L121402 (visited on 11/24/2023).

[37] Giovanni Pizzi. “Band Structure Engineering of Ge-rich SiGe Nanostructures for Photonics Applications”. PhD thesis. Pisa: Scuola Normale Superiore di Pisa, Dec. 2012.

[38] S.M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices*. en. 1st ed. Wiley, Oct. 2006. ISBN: 9780471143239 9780470068328. DOI: 10.1002/0470068329. URL: https://onlinelibrary.wiley.com/doi/book/10.1002/0470068329 (visited on 05/05/2024).

[39] Giuseppe Pastori Parravicini Giuseppe Grosso. *Solid state physics*. Academic Press, 2004.

[40] Yujia Liu et al. “Role of critical thickness in SiGe/Si/SiGe heterostructure design for qubits”. en. In: *Journal of Applied Physics* 132.8 (Aug. 2022), p. 085302. ISSN: 0021-8979, 1089-7550. DOI: 10.1063/5.0101753. URL: https://pubs.aip.org/jap/article/132/8/085302/2837521/Role-of-critical-thickness-in-SiGe-Si-SiGe (visited on 10/08/2023).

[41] J. P. Dismukes, L. Ekstrom, and R. J. Paff. “Lattice Parameter and Density in Germanium-Silicon Alloys [1]”. en. In: *The Journal of Physical Chemistry* 68.10 (Oct. 1964), pp. 3021–3027. ISSN: 0022-3654, 1541-5740. DOI: 10.1021/j100792a049. URL: https://pubs.acs.org/doi/abs/10.1021/j100792a049 (visited on 07/17/2023).

[42] Douglas J Paul. “Si/SiGe heterostructures: from material and physics to devices and circuits”. In: *Semiconductor Science and Technology* 19.10 (Oct. 2004), R75–R108. ISSN: 0268-1242, 1361-6641. DOI: 10.1088/0268-1242/19/10/R02. URL: https://iopscience.iop.org/article/10.1088/0268-1242/19/10/R02 (visited on 10/07/2023).

[43] R. People and J. C. Bean. “Calculation of critical layer thickness versus lattice mismatch for GexSi1-x/Si strained-layer heterostructures”. In: *Applied Physics Letters* 47.3 (Aug. 1985), pp. 322–324. ISSN: 0003-6951. DOI: 10.1063/1.96206. URL: https://aip.scitation.org/doi/10.1063/1.96206 (visited on 08/31/2022).

[44] Davide Degli Esposti et al. *Low disorder and high valley splitting in silicon*. arXiv:2309.02832 [cond-mat]. Sept. 2023. DOI: 10.48550/arXiv.2309.02832. URL: http://arxiv.org/abs/2309.02832 (visited on 12/19/2023).

[45] Chia-Tse Tai and Jiun-Yun Li. “Recent progress in undoped group-IV heterostructures for quantum technologies”. In: *Materials for Quantum Technology* 4.1 (Mar. 2024), p. 012001. ISSN: 2633-4356. DOI: 10.1088/2633-4356/ad2980. URL: https://iopscience.iop.org/article/10.1088/2633-4356/ad2980 (visited on 05/18/2024).

[46] X Mi et al. “Magnetotransport studies of mobility limiting mechanisms in undoped Si/SiGe heterostructures”. In: *Physical Review B - Condensed Matter and Materials Physics* 92.3 (2015), pp. 1–8. ISSN: 1550235X. DOI: 10.1103/PhysRevB.92.035304.

[47] A. Wild et al. “Few electron double quantum dot in an isotopically purified 28Si quantum well”. en. In: *Applied Physics Letters* 100.14 (Apr. 2012), p. 143110. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.3701588. URL: https://pubs.aip.org/apl/article/100/14/143110/151365/Few-electron-double-quantum-dot-in-an-isotopically (visited on 12/08/2023).

[48] Jun Yoneda et al. “A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%”. In: *Nature Nanotechnology* 13.2 (2018), pp. 102–106. ISSN: 17483395. DOI: 10.1038/s41565-017-0014-x. URL: http://dx.doi.org/10.1038/s41565-017-0014-x.

[49] S. Das Sarma et al. “Two-Dimensional Metal-Insulator Transition as a Percolation Transition in a High-Mobility Electron System”. In: *Physical Review Letters* 94.13 (Apr. 2005), p. 136401. DOI: 10.1103/PhysRevLett.94.136401. URL: https://link.aps.org/doi/10.1103/PhysRevLett.94.136401 (visited on 05/05/2024).

[50] L. A. Tracy et al. “Observation of percolation-induced two-dimensional metal-insulator transition in a Si MOSFET”. In: *Physical Review B* 79.23 (June 2009), p. 235307. DOI: 10.1103/PhysRevB.79.235307. URL: https://link.aps.org/doi/10.1103/PhysRevB.79.235307 (visited on 05/27/2020).

[51] PT Coleridge. “Small-angle scattering in two-dimensional electron gases”. In: *Physical Review B* 44.8 (1991), p. 3793.

[52] J. C. Abadillo-Uriel, et al. *(unpublished)*.

[53] Friedrich Schäffler. "High-mobility Si and Ge structures". In: *Semiconductor Science and Technology* 12.12 (Dec. 1997), pp. 1515–1549. ISSN: 0268-1242. DOI: 10.1088/0268-1242/12/12/001.

[54] M. Lodari et al. "Valley Splitting in Silicon from the Interference Pattern of Quantum Oscillations". In: *Physical Review Letters* 128.17 (Apr. 2022), p. 176603. DOI: 10.1103/PhysRevLett.128.176603. URL: https://link.aps.org/doi/10.1103/PhysRevLett.128.176603 (visited on 07/10/2023).

[55] Merritt P. Losert et al. "Practical strategies for enhancing the valley splitting in Si/SiGe quantum wells". In: *Physical Review B* 108.12 (Sept. 2023), p. 125405. DOI: 10.1103/PhysRevB.108.125405. URL: https://link.aps.org/doi/10.1103/PhysRevB.108.125405 (visited on 09/06/2023).

[56] Mark Friesen et al. "Valley splitting theory of Si/SiGe quantum wells". In: *Physical Review B* 75.11 (Mar. 2007), p. 115318. DOI: 10.1103/PhysRevB.75.115318. URL: https://link.aps.org/doi/10.1103/PhysRevB.75.115318 (visited on 05/27/2020).

[57] A L Saraiva et al. "Physical mechanisms of interface-mediated intervalley coupling in Si". In: *Physical Review B - Condensed Matter and Materials Physics* 80.8 (2009), pp. 1–4. ISSN: 10980121. DOI: 10.1103/PhysRevB.80.081305.

[58] M. L. V. Tagliaferri et al. "Impact of valley phase and splitting on readout of silicon spin qubits". In: *Physical Review B* 97.24 (June 2018), p. 245412. ISSN: 2469-9950. DOI: 10.1103/PhysRevB.97.245412.

[59] Sergey Yu. Shiryaev, Flemming Jensen, and Jon Wulff Petersen. "On the nature of cross-hatch patterns on compositionally graded Si1- *x* Ge *x* alloy layers". en. In: *Applied Physics Letters* 64.24 (June 1994), pp. 3305–3307. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.111287. URL: https://pubs.aip.org/apl/article/64/24/3305/63779/On-the-nature-of-cross-hatch-patterns-on (visited on 12/14/2023).

[60] H. Chen et al. "Crosshatching on a SiGe film grown on a Si(001) substrate studied by Raman mapping and atomic force microscopy". In: *Physical Review B* 65.23 (May 2002), p. 233303. DOI: 10.1103/PhysRevB.65.233303. URL: https://link.aps.org/doi/10.1103/PhysRevB.65.233303 (visited on 12/08/2023).

[61] Kentaro Kutsukake et al. "On the origin of strain fluctuation in strained-Si grown on SiGe-on-insulator and SiGe virtual substrates". en. In: *Applied Physics Letters* 85.8 (Aug. 2004), pp. 1335–1337. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.1784036. URL: https://pubs.aip.org/apl/article/85/8/1335/902743/On-the-origin-of-strain-fluctuation-in-strained-Si (visited on 12/08/2023).

[62] K. Sawano et al. "In-plane strain fluctuation in strained-Si/SiGe heterostructures". en. In: *Applied Physics Letters* 83.21 (Nov. 2003), pp. 4339–4341. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.1629142. URL: https://pubs.aip.org/apl/article/83/21/4339/509342/In-plane-strain-fluctuation-in-strained-Si-SiGe (visited on 12/08/2023).

[63] Don Monroe et al. “Comparison of mobility-limiting mechanisms in high-mobility Si1-xGex heterostructures”. In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 11.4 (July 1993), pp. 1731–1737. ISSN: 1071-1023. DOI: 10.1116/1.586471. URL: https://avs.scitation.org/doi/abs/10.1116/1.586471 (visited on 02/08/2022).

[64] Cedric Corley-Wiciak et al. “Nanoscale Mapping of the 3D Strain Tensor in a Germanium Quantum Well Hosting a Functional Spin Qubit Device”. en. In: *ACS Applied Materials & Interfaces* 15.2 (Jan. 2023), pp. 3119–3130. ISSN: 1944-8244, 1944-8252. DOI: 10.1021/acsami.2c17395. URL: https://pubs.acs.org/doi/10.1021/acsami.2c17395 (visited on 12/20/2023).

[65] C Corley-Wiciak et al. “Lattice Deformation at Submicron Scale: X-Ray Nanobeam Measurements of Elastic Strain in Electron Shuttling Devices”. In: *Physical Review Applied* 20.2 (2023), p. 024056.

[66] Collin C. D. Frink. *Reducing strain fluctuations in quantum dot devices by gate-layer stacking*. en. URL: https://arxiv.org/pdf/2312.09235.pdf.

[67] Benjamin D. Woods. *Coupling conduction-band valleys in modulated SiGe heterostructures via shear strain*. en. Dec. 2023. DOI: https://arxiv.org/pdf/2310.18879.pdf. URL: https://arxiv.org/pdf/2310.18879.pdf (visited on 12/14/2023).

[68] Brian Paquelet Wuetz et al. “Reducing charge noise in quantum dots by using thin silicon quantum wells”. en. In: *Nature Communications* 14.1 (Mar. 2023), p. 1385. ISSN: 2041-1723. DOI: 10.1038/s41467-023-36951-w. URL: https://www.nature.com/articles/s41467-023-36951-w (visited on 12/14/2023).

[69] Elliot J Connors et al. “Low-frequency charge noise in Si/SiGe quantum dots”. In: *Physical Review B* 100.16 (2019), p. 165305.

[70] P. Dutta and P. M. Horn. “Low-frequency fluctuations in solids: 1/f-noise”. In: *Reviews of Modern Physics* 53.3 (July 1981), pp. 497–516. ISSN: 0034-6861. DOI: 10.1103/RevModPhys.53.497.

[71] Elliot J Connors, J J Nelson, and John M Nichol. “Charge-noise spectroscopy of Si/SiGe quantum dots via dynamically-decoupled exchange oscillations”. In: *arXiv preprint arXiv:2103.02448* (2021).

[72] Félix Beaudoin and W. A. Coish. “Microscopic models for charge-noise-induced dephasing of solid-state qubits”. In: *Physical Review B* 91.16 (Apr. 2015), p. 165432. ISSN: 1098-0121. DOI: 10.1103/PhysRevB.91.165432.

[73] John J. L. Morton et al. “Embracing the quantum limit in silicon computing”. en. In: *Nature* 479.7373 (Nov. 2011), pp. 345–353. ISSN: 1476-4687. DOI: 10.1038/nature10681. URL: https://www.nature.com/articles/nature10681 (visited on 12/08/2023).

[74] Ted Thorbeck and Neil M. Zimmerman. "Formation of strain-induced quantum dots in gated semiconductor nanostructures". en. In: *AIP Advances* 5.8 (Aug. 2015), p. 087107. ISSN: 2158-3226. DOI: 10.1063/1.4928320. URL: https://pubs.aip.org/adv/article/5/8/087107/661335/Formation-of-strain-induced-quantum-dots-in-gated (visited on 12/08/2023).

[75] Matthias Brauns et al. "Palladium gates for reproducible quantum dots in silicon". en. In: *Scientific Reports* 8.1 (Apr. 2018), p. 5690. ISSN: 2045-2322. DOI: 10.1038/s41598-018-24004-y. URL: https://www.nature.com/articles/s41598-018-24004-y (visited on 12/08/2023).

[76] Guido Burkard et al. "Semiconductor Spin Qubits". In: (Dec. 2021).

[77] Tom Struck et al. "Low-frequency spin qubit energy splitting noise in highly purified 28Si/SiGe". In: *npj Quantum Information* 6 (1 Dec. 2020), p. 40. ISSN: 2056-6387. DOI: 10.1038/s41534-020-0276-2.

[78] Ravi Acharya et al. "Highly ^{28}Si enriched silicon by localised focused ion beam implantation". In: *arXiv preprint arXiv:2308.12471* (2023).

3

Methods

Science is a collaborative effort.

John Bardeen

3.1. EPITAXY OF SI/SIGE HETEROSTRUCTURES

Chemical vapour deposition (CVD) is a widely used growth technique in which thin films are formed on a heated substrate via chemical reactions at the substrate surface with precursor gasses. Compared to other deposition techniques (*e.g.*, MBE, evaporation, sputtering, etc.) CVD stands for the wide range of possible growth rates, the high conformality of the epitaxial layers, and the very low levels of contamination from bioproducts. Moreover, the same technique is used in the advanced semiconductor process to manufacture transistors, chips, and integrated circuits. Irrespective of the specific conditions, all CVD processes share some common elementary steps [1]. First, the reaction is carried out by precursor gasses in a laminar flow carrying the desired chemical specimens. These are then inserted in the reaction chamber, adsorb on the heated substrate surface, and diffuse on the surface. The reaction at the gas/solid interface (fig. 3.1(a)) leads to the continuous nucleation of new atoms on the surface and the progression of the growth front. finally, the unreacted species and the products of the chemical reactions desorb from the surface and are carried away from the reaction zone by the laminar gas flow.

This thesis considers ^{28}Si/SiGe heterostructures grown at the Else Kooi Laboratories (EKL) in Delft via Reduced-Pressure Chemical-Vapour-Deposition (RP-CVD). We use an ASMI Epsilon 2000 CVD reactor. The reactor is equipped with natural dichlorosilane ($SiCl_2H_2$), germane (GeH_4) 2% diluted in H_2, and isotopically enriched silane ($^{28}SiH_4$) 1% diluted in H_2 with 800 ppm of residual non-zero isotopes[2]. These precursor gases allow the growth of SiGe alloys of variable Ge concentration and purified ^{28}Si. The reactor can use single 4" (100 mm) wafers. Figure 3.1(b-c) shows a schematic representation of the quartz chamber where the growth is carried out. The wafer used as a substrate for the subsequent epitaxial layers is placed on a rotating graphite susceptor. The chamber is equipped with integrated heating lamps to control the growth temperature up to 1200 °C. The precursor bottles are connected to a mass flow controller to manage the desired ratio, combine them, and create a uniform laminar flow. The growth happens at reduced pressure (20 mbar) and in H_2 atmosphere. The pressure is controlled by a scroll pump connected to the chamber with a variable butterfly valve.

Figure 3.1(d) shows a schematic representation of a Si/SiGe heterostructure with exemplified the chemical reactions happening at the surface of the growth front. Below is a more in-depth description of the various steps involved in growing a Si/SiGe heterostructure. In particular, we nail down the processes used to grow the Si/SiGe heterostructure used in Chapter 6 (QT724):

Cleaning We use 100 mm (100) silicon wafers with a resistivity of 1-5 Ωcm as substrates for the epitaxial growth. The silicon wafer is located in the reactor and baked at 1100 °C for 90 s. The baking is necessary to clean the carrier wafer,ensure that water and moisture are not present on the surface, and desorb the silicon oxide grown naturally on the wafer surface.

Virtual Substrate The purpose of the "virtual" substrate (VS) is to provide an artificial substrate with a larger lattice parameter than bulk silicon for subsequent growth of a tensile strained thin silicon quantum well. The VS is composed of a series of step layers with increasing Ge concentration (x). Starting from pure Si ($x = 0$), the VS comprises four other layers with target Ge concentrations of $x = 0.07, 0.14, 0.21, 0.30$

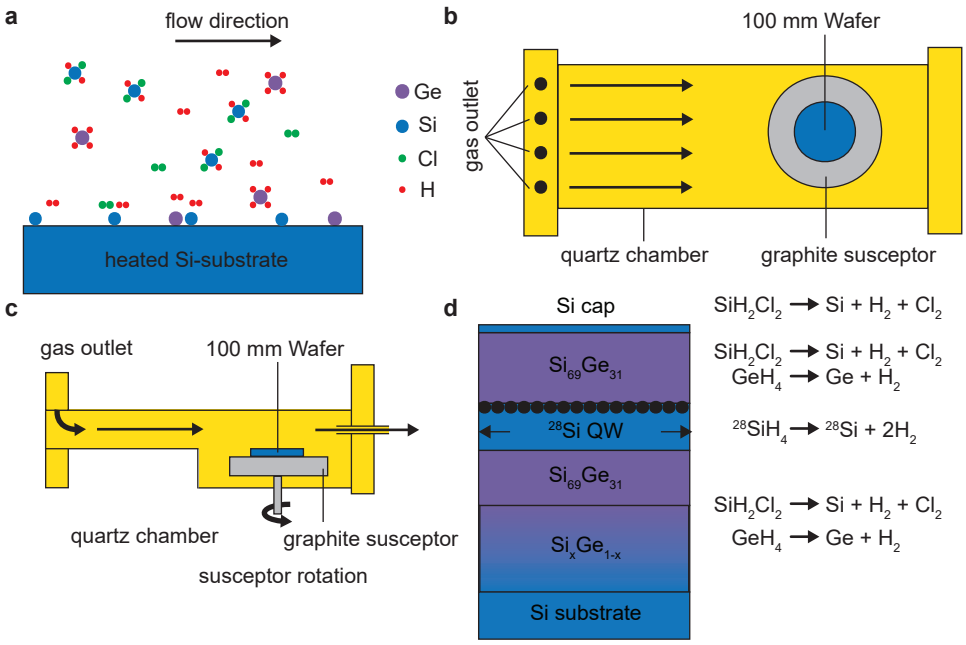


Figure 3.1: **CVD epitaxy. a** Schematic diagram of the chemical process occurring at the surface of a Si-substrate inside the RP-CVD reactor. For the growth of the SiGe layers, the dichlorosilane (SiH_2Cl_2) and Germane (GeH_4) precursors desorb chlorine (Cl_2) and hydrogen (H_2), leaving Silicon and Ge atoms on the growth front. **b** Schematic top view of the susceptor plate and gas flow controller inside the quartz chamber of the ASMI Epsilon 2000 CVD reactor. The growth happens at a constant pressure in hydrogen atmosphere. The gas outlets control the magnitude of the laminar flow carrying the precursor gases. **c** Side view of the same components as in **b**. The susceptor plate holding the carrier wafer rotates during the growth to ensure uniformity across the surface. **d** Schematic of a typical Si/SiGe heterostructure with the chemical reactions occurring to grow the different layers. The various Ge concentrations in the step-graded virtual substrate are achieved by controlling the relative concentration of dichlorosilane and germane in the laminar flow. The black points at the top of the Si quantum well highlight where electron accumulation occurs. All the images are adapted from [3, 4].

approximately 1 μm thick each. The entire virtual substrate is grown at 750 °C. After each layer, the stack is baked at 850 °C to ensure full relaxation and extend the misfits dislocation network in order to obtain a lattice constant corresponding to the targeted Ge composition in each layer.

Relaxed buffer At the end of the VS, the temperature is lowered to 625 °C for the growth of a 300 nm thick $Si_{0.69}Ge_{0.31}$ relaxed buffer, whose purpose is to separate the quantum well from the underlying dislocation network. The final Ge concentration of such a layer is $x = 0.31(1)$.

^{28}Si quantum well The growth of the ^{28}Si quantum well (QW) is carried out at 750 °C using isotopically enriched silane ($^{28}SiH_4$). In the specific condition the growth of the QW lasts for a few minutes, enabling the possibility of fine-tuning the thickness of such a layer and a great in-plane uniformity. The resulting thickness is 6.9(5) nm.

SiGe spacer The growth of the SiGe spacer is carried out in the same low-temperature conditions used for the relaxed buffer. The resulting thickness is 30(1) nm with below nanometer wafer-to-wafer variation.

Si cap At the end of the growth, the Si/SiGe heterostructure is terminated by a 300 s exposure to DCS at 500 °C [5]. This creates a DCS-saturated surface that becomes a thin (≈ 1 nm) silicon-oxide layer upon exposure of the wafer to air, protecting the heterostructure.

High temperature and fast growth conditions are preferred for the SiGe VS to keep the growth time reasonable and avoid oxygen and carbon incorporation. Low temperature can be useful to create growth interruptions and ensure sharp heterointerfaces. Overall, careful tuning of multiple parameters (temperature, pressure, flow, precursors ratio, annealing temperature, and cleaning) is necessary to ensure low dislocations, chemical contamination, and overall high crystalline quality of the heterostructures. The Si/SiGe heterostructures described in this thesis routinely show Oxygen and Carbon contamination below secondary ion mass spectrometry (SIMS) detection limit of $\simeq 5 \times 10^{16}$ cm^{-2} and low density of dislocations in the active layer ($\approx 10^5$ cm^{-2}).

3.2. STRUCTURAL CHARACTERIZATION

The structural and chemical characterization of the material stack lays at the basis of any feedback loop (fig. 1.2). Figure 3.2 compares the chemical and spatial resolution of many techniques normally used for material characterization. Throughout the thesis, we will mainly use information gained from scanning-transmission electron microscopy (STEM), secondary ion mass spectroscopy (SIMS), electron energy loss spectroscopy (EELS), and Raman spectroscopy.

STEM is an imaging technique that uses a high-energy (200-300 keV) electron beam to reach subatomic spatial resolution. To allow the imaging, the sample is cut into a thin slice, a few tents of atoms called lamella. Depending on the detector used, the contrast of STEM images can be sensitive to the atomic weight (Z-Constrast), making it possible to recognize between different alloys, *e.g.*, Si, and SiGe. STEM is the core technique used in developing Si/SiGe heterostructures to control the thickness of the multiple layers (step-graded virtual substrate, quantum well, SiGe spacer) and tune the growth rates. Thanks to the extremely high spatial resolution, we also use it to measure the Ge concentration profile of the quantum well and the sharpness of the SiGe/Si and Si/SiGe interfaces.

SIMS is the technique with the highest sensitivity to different chemical elements and isotopes. It is able to recognize concentrations down to a few parts per million (ppm). Therefore, it is particularly useful to ensure the chemical purity of the heterostructure, the absence of contaminations or bioproducts, and the residual isotope concentration in the purified layers. It is a destructive technique that uses an ion beam to sputter the specimen. For this reason, the spatial resolution is usually not very accurate, and sharp discontinuities in chemical concentrations are smeared out.

EELS can be performed during STEM imaging to understand the chemical composition of the specimen under analysis. It can detect relative chemical concentrations down to a few percent. Since it usually involves fitting peaks and background subtraction, the absolute chemical compositions are usually not completely reliable, Moreover,

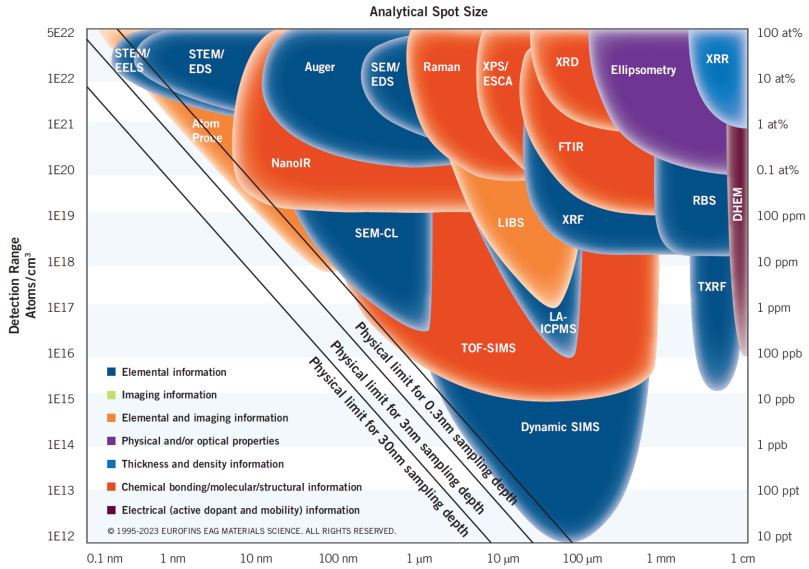


Figure 3.2: **SMART Chart:** The EAG SMART (Spectroscopy and Microscopy Analytical Resolution Tool) Chart compares chemical detection limits and spatial resolution of multiple techniques used for material characterization. Besides chemistry, these techniques can also offer information about strain, molecular phase, and crystalline structure. Adapted from [6] .

it cannot identify light elements such as hydrogen that would have energy peaks at too low energies. However, its high energy resolution permits the identification of different molecular phases of the same element (*e.g.*, Si-crystal vs Si-amorphous) with high spatial precision. This has proved extremely useful in chapter 4 to analyse the topmost SiGe/SiOx/AlOx interfaces and the transition from a crystalline SiGe to the amorphous oxide layers.

Raman spectroscopy uses laser light to excite the vibrational states of a crystal. The spatial resolution is constrained by the wavelength of the laser in use, and it is usually around 1 μm. Vibrational properties give insight into the chemistry and strain. We used Raman spectroscopy to measure the average strain and the amplitude of the strain fluctuations of the Si quantum well in chapter 6.

Although most of these techniques are nowadays mainstream, interpreting the actual results usually requires a considerable degree of understanding of the physical principles behind the measurement. Dielectric layers are more sensitive to damage from electron beam exposure during STEM imaging than the heterostructure to damage. Oxygen and Carbon noise floors in SIMS can vary considerably depending on the particular detector conditions. Relative chemical concentrations in EELS depend on the fitting and various elements under analysis. Absorption of visible light employed in Raman spectroscopy strongly depends on the Ge concentration, requiring specific engineering of the stack to pick up the signal from the Si quantum well.

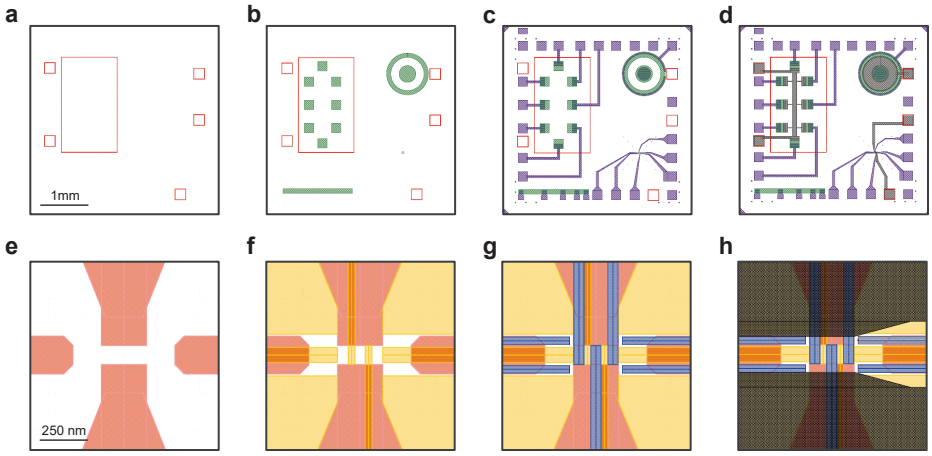


Figure 3.3: **Device fabrication:** Schematic illustrations of the main pre-nanofabrication (**a-d**) and nanofabrication (**e-h**) steps. The pre-nanofabrication process comprises mesa trench dry etching (**a**), red), phosphorus implantation and activation (**b**), green), Ti:Pt ohmic contacts (**c**), blue), Al_2O_3 atomic layer deposition, and Al metallic gate sputter deposition (**d**), grey). At the end of the pre-nanofabrication process, the wafer is diced in 20x20 mm^2 coupons, and the quantum dot nanofabrication starts. The nanofabrication comprises three Ti:Pd evaporations for the screening (**e**), red), plungers (**f**), yellow) and barrier (**g**), blue) gates isolated by Al_2O_3 dielectric. Finally, a last Al_2O_3 separates the Ti:Co micromagnets (**h**), grey) evaporated on top of the gate stack.

3.3. DEVICE FABRICATION

The characterization of the heterostructure and material stack relies greatly on the measurement at low temperatures of test structures and quantum devices. The fabrication of such test structures and quantum devices is divided into two steps. We perform a first set of steps on a 100 mm wafer scale using photolithography, comprising photo markers, P+ implantation, ohmic evaporation, a first dielectric layer, and gate metal for test structures. The validation of the test structures ensures correct ohmic contact with the quantum well, electron accumulation in the quantum well, and quality of the first dielectric layer. Then, using electron beam lithography, we start fabricating nanostructures and quantum dot devices on top of the same wafers. This second part of the process consists of three metal evaporations with insulating dielectrics in between, forming the quantum dot gates, and a final evaporation for the micromagnets.

3.3.1. PRE-NANOFABRICATION

Figure 3.3(a-d) describes the various layers necessary to create the test structures during the *Pre fabrication* process. We use SPR 3012 positive photoresist and MF322 developer (TMAH-based) in all steps. Depending on the specific layer, the resist is stripped away using a combination of oxygen plasma and chemicals such as Acetone, HNO_3, and NMP. The surface is cleaned at the beginning of each layer using 99% HNO_3 and warm 69.5% HNO_3 at 100°C.

MESA and markers: The first layer is showed in fig. 3.3(a) and consist of a reactive dry

etch using an HBr + Cl plasma. This process digs a mesa trench from the surface down to the Si quantum well approximately 100 nm deep. As a result, the electronic transport in the quantum well is disconnected by the mesa trench and can only happen inside of it. During this step, we also pattern the markers used for the alignment of the subsequent layers.

Implantation and activation: We implant with phosphorus (P) ions selected parts of the surface (fig. 3.3(b)) to create ohmic conduction through the SiGe spacer. The ion implantation uses 20kV acceleration voltage and a dose of 10^{15} ions/cm^2. After the implantation, the surface is cleaned with HNO_3, and the implants are activated via a rapid thermal process at 712 °C for 12 s.

Atomic layer deposition: Next, we deposit a 10 nm (100 cycles) thick layer of Al_2O_3 using atomic layer deposition at 300 C.

Ohmic contact: We use a Buffered oxide etch (BOE, HF 7:1) to open windows on the Al_2O_3 and be able to contact the implanted areas. We use a Ti:Pt (5:55 nm) evaporation to create ohmic contact on the surface. During this step, we also pattern the markers of the subsequent e-beam lithography.

Metallic gate: The last step of the prefabrication process uses a sputtering tool to deposit a 200 nm thick Al film, forming the metallic gate of the test structures.

At the end of the prefabrication process, the 100 mm wafer is diced into 20x20 mm^2 coupons. Each coupon comprises four 4x4 mm^2 dies hosting test structures (identical to fig. 3.3(d)) and twelve empty 4x4 mm^2 dies, which can be used for the fabrication of quantum dot devices. The test structures are a hall-bar (HB) shaped heterostructure field effect transistor (H-FET), a Corbino disk, a transfer length method (TLM) device, and a micro HB. Each 100 mm wafer is divided into 12 complete 20x20 mm^2 coupons, *i.e.*, 48 test structures dies, and 144 quantum dot dies.

Several considerations need to be considered in the development of each process. The mesa trench has to be deeper than the quantum well to disconnect the electronic transport. The energy of the P^+ ions has to be low enough to effectively contact the surface and high enough to reach the Si quantum well. The rapid thermal anneal temperature has to be lower than the growth temperature of the Si quantum well (750 °C) to avoid strain relaxation and mitigate Ge atoms redistribution. The use of Ti:Pt film for the ohmic contacts is mainly driven by the high conductivity of Pt films and the high atomic number, making it good to be used as a marker for beam lithography. The use of a sputter tool for the Al gate ensures the continuity of the metallic gate crossing the mesa trench.

3.3.2. NANOFABRICATION

The nanofabrication of quantum dot devices is performed in the van Leeuwenhoek laboratory's (VLL) clean room. The electron-beam (e-beam) lithographic process uses AR-P6200 series resist, penthylacetate for development, and AR600-71 dioxolane-based stripper for lift-off. The quantum dot fabrication process comprises three Ti:Pd metal evaporation with increasing thickness (3:17, 3:27, 3:37 nm), as reported in fig. 3.3(e-g). The

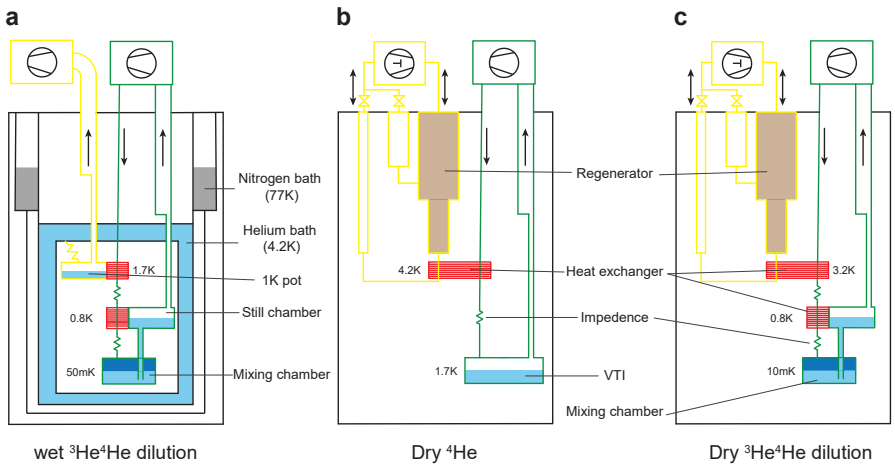


Figure 3.4: **Cryogenic equipment.** Schematic representations of the various kinds of refrigerators used for the electrical measurements at cryogenic temperatures. The schematics show the main components of a wet-$^3H^4H$ dilution refrigerator (**a**), dry-^{4}He refrigerator (**b**), and a dry-$^3He^4$He dilution refrigerator (**c**). The two main circuits constituting each system are highlighted in yellow (pre-cooling circuit) and green (cooling circuit). Adapted from [7].

metallic layers are isolated with 5 nm (50 cycles) of Al_2O_3 dielectric deposited via atomic layer deposition (ALD) at 300 °C. The usual layer order comprises screening gates and ohmic contacts, accumulation gates, and barrier gates. Another ALD layer separates the gate metals from the Ti:Co (5:200 nm) micromagnets. In recent years, the thickness of this last ALD layer has varied between 5 and 30 nm, with the intention of smoothing the top surface before the micromagnet evaporation. The layout of the central zone of a quantum dot spin qubit device is shown in fig. 3.3(h).

3.4. EXPERIMENTAL SETUP FOR CRYOGENIC MEASUREMENTS

Temperature (T) sets one of the most important energy scales for the operation of quantum devices. It converts into energy through the Boltzmann constant (k_B) via the relation: $E_T = k_B T$. On the other side, spin qubits are defined by the Zeeman splitting: $E_Z = g\mu_B B$, where B is the magnetic field, g is the gyromagnetic factor, and μ_B is the Bohr magneton. Common values of operation for spin qubits in silicon use $B = 0.4T$ equivalent to $E_Z(0.4\,T) \approx 57\ \mu$eV. To suppress thermal excitations ($E_T \ll E_Z$), the spin qubit samples are cooled down to a temperature of ≈ 100 mK equivalent to a thermal energy of $E_T(100\,mK) \approx 9\ \mu$eV.

Throughout this thesis, we use multiple refrigerating systems to cool down samples to low temperatures. In particular, we used a wet-^{3}He^{4}He dilution (Leiden MCK50-400) refrigerator, a dry-^{4}He (AttoDry2100) refrigerator, and a dry-^{3}He^{4}He dilution (BluFors LD400) refrigerator. Figure 3.4 shows a schematic representation of the main components necessary for the operation of each one of these systems. Every system uses a combination of a pre-cooling (yellow) and a cooling (green) circuit to achieve the lowest

temperature.

The so-called "wet" systems use cryogenic liquids such as Nitrogen (77 K) and Helium (4.2 K) as main reservoirs to cool multiple thermal shields at progressively colder temperatures. These liquids evaporate over time to keep the system cold and, therefore, need to be refilled every few days. A small portion of the liquid He from the main bath is directed into an isolated chamber called "1K-pot" and connected to an external pump to further lower the temperature. The He evaporation is increased by lowering the pressure in the 1K-pot, and the temperature can be lowered to ≈ 1.7 K. This part constitutes the pre-cooling circuit. It is connected to the main cooling circuit via a heat exchanger. The cooling circuit comprises a mixing chamber, a still chamber, and a series of pumps. The closed circuit uses a mixture of ^{3}He and ^{4}He isotopes as cooling gas. After the pumps at room temperature, the mixture enters the fridge through the condensing line. It is cooled by the heat exchangers with the 1K-pot and still chamber and condenses in liquid form. thanks to the low temperature, the ^{3}He^{4}He mixture undergoes a phase separation in the mixing chamber, dividing into concentrated (top) and diluted (bottom) ^{3}He phases. The cooling process consists of the concentrated phase "evaporating" into the diluted phase. The diluted phase is then led into the still chamber, where it returns in gaseous form and is pumped away to close the loop.

The main limitation of "wet" systems is that they constantly refills cryogenic liquids to maintain low temperatures. The invention of closed-circle pulsed tube refrigerators circumvents this. A two-stage pulse tube usually forms the precooling circuit of the so-called "Dry" systems. It uses a compressor and a piston to push and pull high pressure (≈ 17 bars) ^{4}He through a magnetic porous material with a large specific heat called *regenerator*. The regenerator absorbs the heat, resulting in effective cooling, the base temperature of which depends on the specific material used for the regenerator.

Dry systems are, therefore, cryogen liquid-free and can operate for long periods of time without any maintenance. The pulse tube cryocooler can be used as a pre-cooling stage in ^{4}He fridges where it is used to liquefy the ^{4}He or to replace the 1K-pot in ^{3}He^{4}He dilution units. Note that since the base temperature of the cryocooler is higher than the temperature of a 1K-pot in a wet fridge, the pressure on the condensing line is usually higher in dry dilution refrigerators.

3.4.1. HALLBAR MEASUREMENT

Hall-bar shaped heterostructure field effect transistors (H-FETs) are characterised using the standard four-wire low-frequency lock-in technique. Figure 3.5(a) shows a schematic representation of a Hall-bar shaped heterostructure field effect transistor with the necessary connections for the electrical characterization. The devices are operated in accumulation mode. A fixed DC voltage is applied to the top gate electrode (V_G) to accumulate the electrons in the quantum well. The Source-Drain electrical current (I_{SD}) is measured after applying a low-frequency AC excitation (V_{SD}) to the source ohmic contact. We typically use V_{SD} = 0.1 mV at a frequency of 17.777 Hz. The longitudinal (V_{xx}) and transverse (V_{xy}) voltage drops are measured using additional ohmic contacts and voltage amplifiers with high input impedance ($Z_{in} \approx 10$ GΩ). Since the input impedance of the voltage amplifier is much greater than the other impedances in the circuit, *e.g.*, ohmic contact, and channel resistance, there is no current flowing in the circuit formed

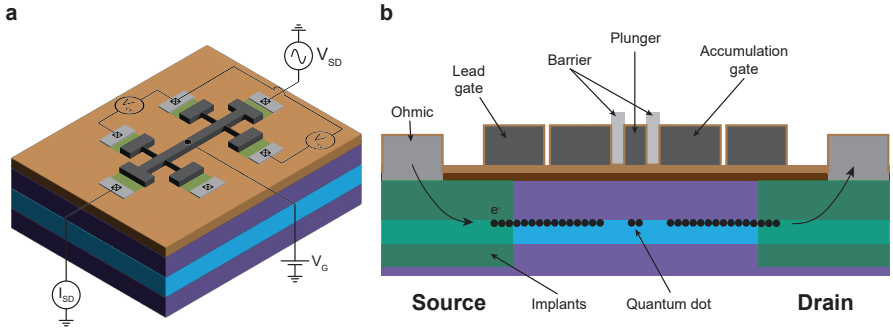


Figure 3.5: **Measurements schemes for Hall-bar and quantum dot characterization. a** Schematic representation of a Hall-bar (HB) shaped heterostructure field effect transistor with superimposed the necessary electrical connection for the electrical characterization. We apply a fixed DC gate voltage (V_g) to the topmost electrode and use a low-frequency AC excitation (V_{SD}). The current (I_{SD}) and the longitudinal (V_{xx}) and transverse (V_{xy}) drop of voltages are recorded by lock-in amplifiers set at the same frequency of V_{SD}. **b** Schematic representation of the gates and electron transport in a quantum dot device featuring *split gates* architecture. A masked BOE cleaning ensures the absence of dielectric underneath the metallic ohmic contacts. The implanted regions are heavily doped and effectively behave as a low-resistance metal. The lead and accumulation gates are closely spaced (50-100 nm separation) to ensure the continuity of the 2DEG underneath. The lead gates allow the close of the conduction path from the ohmic to the quantum dots while keeping an electron's reservoir under the accumulation gates.

by the voltage amplifier. This ensures that V_{xx} and V_{xy} are precisely the drop of voltages of the probes at the device location and that the specific connection and wiring are not contributing to the measurement.

We use twisted pairs of coaxial cables to connect the bottom of the fridges with the sample to the room-temperature instrumentation. At room temperature, the lines are connected to isolate break-out boxes equipped with π-filters to suppress high-frequency noise (> 10 GHz). The current and voltage amplifiers are located in galvanically decoupled IVVI or SPI racks and share the same ground as the break-out boxes. Digital-to-analog converters (DACs) included in the racks are used to apply the DC gate voltage. The source-drain excitation is generated by a lock-in amplifier (SR830) amplified by a voltage amplifier in the IVVI rack. The source-drain current, V_{xx}, and V_{xy} are measured using current/voltage trans-impedance and voltage amplifiers ultimately connected to other lock-in amplifiers.

3.4.2. QUANTUM DOT MEASUREMENTS

Quantum dot measurements are performed in transport in DC. Figure 3.5(b) depicts the cross-section of a quantum dot device embedded in a Si/SiGe heterostructure. A fixed DC source-drain excitation is applied to the source electrode. Then, the electrical current (I_{SD}) flows from the metallic ohmic contact to the implanted region to the 2DEG accumulated under the lead and accumulation gates. I_{SD} is finally collected from the drain electrode connected to ground. The electrical current is converted into a voltage difference by a trans-impedance amplifier with a sufficiently high bandwidth ($\approx$ 10 kHz) to speed up the measurement. The voltage drop is ultimately acquired using a Keithley DMM6500 digital multimeter equipped with a 16-bit digitizer card with a maximum

sample rate of 1Msamples/s We use multiple DACs with a 16-bit resolution to apply and sweep the voltages to the topmost gate electrodes, forming the quantum dots and controlling the 2DEG accumulation. These are directly connected to the twisted lines from the break-out boxes.

BIBLIOGRAPHY

[1] Luzhao Sun et al. “Chemical vapour deposition”. en. In: *Nature Reviews Methods Primers* 1.1 (Jan. 2021), pp. 1–20. ISSN: 2662-8449. DOI: 10.1038/s43586-020-00005-y. URL: https://www.nature.com/articles/s43586-020-00005-y (visited on 12/15/2023).

[2] D. Sabbagh et al. “Quantum Transport Properties of Industrial $^{28}\mathrm{Si}/^{28}{\mathrm{Si}\mathrm{O}}_{2}$”. In: *Physical Review Applied* 12.1 (July 2019), p. 014013. DOI: 10.1103/PhysRevApplied.12.014013. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.12.014013 (visited on 07/10/2023).

[3] Amir Sammak. “Silicon-Based Integration of Groups III, IV, V Chemical Vapor Depositions in High-Quality Photodiodes”. Available at https://doi.org/10.4233/uuid:d484f6ed-05f4-4f59-b148-9d28de4fd2b0. PhD thesis. Delft: Delft University of Technology, 2012.

[4] Brian Paquelet Wuetz. “Silicon/silicon-germanium heterostructures for spin-qubit quantum processors”. Available at https://doi.org/10.4233/uuid:955fab3d-fc33-4ccb-8c58-c6eaf7b56c9c. PhD thesis. Delft: Delft University of Technology, July 2022.

[5] Davide Degli Esposti et al. “Wafer-scale low-disorder 2DEG in 28Si/SiGe without an epitaxial Si cap”. en. In: *Applied Physics Letters* 120.18 (May 2022), p. 184003. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0088576. URL: https://pubs.aip.org/apl/article/120/18/184003/2833621/Wafer-scale-low-disorder-2DEG-in-28Si-SiGe-without (visited on 07/10/2023).

[6] eurofins EAG laboratories. *EAG SMART (Spectroscopy and Microscopy Analytical Resolution Tool) Chart*. URL: https://www.eag.com/techniques/.

[7] H. Zu, W. Dai, and A.T.A.M. De Waele. “Development of dilution refrigerators—A review”. en. In: *Cryogenics* 121 (Jan. 2022), p. 103390. ISSN: 00112275. DOI: 10.1016/j.cryogenics.2021.103390. URL: https://linkinghub.elsevier.com/retrieve/pii/S001122752100148X (visited on 12/29/2023).

4

^{28}Si/SiGe heterostructures without an epitaxial Si cap

We grow ^{28}Si/SiGe heterostructures by reduced-pressure chemical vapor deposition and terminate the stack without an epitaxial Si cap but with an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. As a result, ^{28}Si/SiGe heterostructure field-effect transistors feature a sharp semiconductor/dielectric interface and support a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 mm wafer. At $T = 1.7$ K we measure a high mean mobility of $(1.8 \pm 0.5) \times 10^5$ cm^2/Vs and a low mean percolation density of $(9 \pm 1) \times 10^{10}$ cm^{-2}. From the analysis of Shubnikov–de Haas oscillations at $T = 190$ mK, we obtain a long mean single particle relaxation time of (8.1 ± 0.5) ps, corresponding to a mean quantum mobility and quantum level broadening of $(7.5 \pm 0.6) \times 10^4$ cm^2/Vs and (40 ± 3) μeV, respectively, and a small mean Dingle ratio of (2.3 ± 0.2), indicating reduced scattering from long range impurities and a low-disorder environment for hosting high-performance spin-qubits.

This chapter has been published as: **Davide Degli Esposti**, Brian Paquelet Wuetz, Viviana Fezzi, Mario Lodari, Amir Sammak, Giordano Scappucci, "Wafer-scale low-disorder 2DEG in ^{28}Si/SiGe without an epitaxial Si cap", Applied Physics Letters, **120**, 184003 (2022).

4.1. INTRODUCTION

Strained ^{28}Si/SiGe heterostructures are a compelling platform for scalable qubit tiles based on gate-defined quantum dots.[1, 2] In these ^{28}Si buried quantum wells, electron spins experience a quiet electrical and magnetic environment. The electronically noisy semiconductor/dielectric interface is far away, separated from the quantum well by a SiGe epitaxial barrier, and the nuclear spins have been removed by isotopic enrichment. Continuous advances in the material science of ^{28}Si/SiGe and improved device fabrication have enabled quantum logic with spin qubits crossing the surface code threshold,[3–5] coherent coupling of two electron spins at a distance via virtual microwave photons,[6] and CMOS-based cryogenic control of quantum circuits[7]. In the mainstream approach to quantum dot fabrication, the last step in the heterostructure growth cycle comprises the heteroepitaxial deposition of a thin epitaxial Si cap on the SiGe barrier.[8] This is to avoid the formation of low-quality Ge-based oxides upon exposure of SiGe to air. After the Si cap deposition, a high-κ dielectric is deposited *ex-situ* and at low-temperature ($\approx 300\,^{\circ}$C) to insulate the gate from the buried and undoped quantum well. This low-temperature process preserves the strain in the quantum well but induces large concentrations of impurities at the critical semiconductor/dielectric interface. These impurities can influence the electrostatic confining potential landscape induced by the gates, leading to the formation of unintentional quantum dots, [9] and are a source of charge noise limiting qubit performance.[10, 11] While efforts have focused on achieving uniform and high-purity ^{28}Si quantum wells with sharp interfaces, [12–14] now more attention is needed to optimize the step which terminates the heterostructure deposition cycle and has a critical role in defining the semiconductor/dielectric interface.

In this letter, we explore ^{28}Si/SiGe heterostructures terminated by exposure to dichlorosilane (DCS) gas at a temperature well below the threshold for epitaxial growth of Si. By avoiding the growth of an epitaxial Si cap altogether, we obtain ^{28}Si/SiGe heterostructure field effect transistors (H-FETs) with a sharp semiconductor/dielectric interface. We show that the ^{28}Si quantum well supports a two-dimensional electron gas with less disorder and improved quantum transport properties compared to heterostructures with an epitaxial Si cap.

4.2. ^{28}SI/SIGE HETEROSTRUCTURES

Figure 4.3(a) illustrates the workflow to fabricate ^{28}Si/SiGe H-FETs. We grow ^{28}Si/SiGe heterostructures on 100 mm Si(001) wafers using an Epsilon 2000 (ASMI) reduced-pressure chemical vapor deposition reactor. We use isotopically-enriched $^{28}SiH_4$ for growing the ^{28}Si quantum well (residual ^{29}Si concentration of 0.08%[3, 7, 15]) and DCS (H_2SiCl_2) and GeH_4 for all other layers. The heterostructure comprises a 3 µm step-graded $Si_{1-x}Ge_x$ layer (final $x \simeq 0.3$), a 2.5 µm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer, an 8 nm tensile-strained ^{28}Si quantum well and a 30 nm $Si_{0.7}Ge_{0.3}$ barrier[1] and in the SiGe barrier is $\simeq 4\times10^{17}$ cm^{-3}. To achieve sharp interfaces and minimize Si/Ge interdiffusion at the quantum well-barrier interface[12], the temperature is decreased from 750 °C for growing the quantum well to 625 °C for the barrier. We now introduce a major difference compared to our previous

[1] A typical secondary ions mass spectrometry of our heterostructures is reported in Fig. S13 of Ref. [12]. The oxygen concentration in the ^{28}Si quantum well is $\simeq 4\times10^{17}$ cm^{-3}

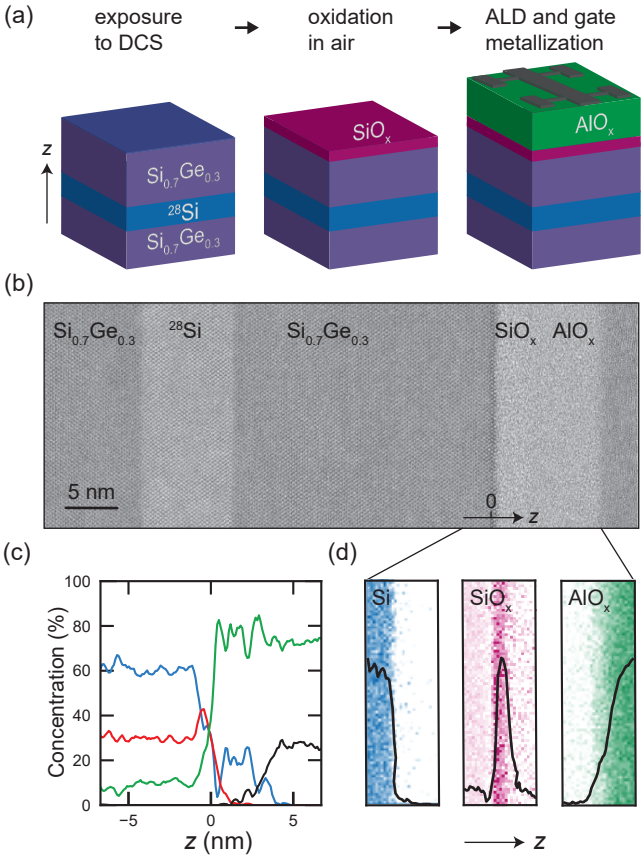


Figure 4.1: (a) Schematics of the ^{28}Si/SiGe heterostructure and formation of the dielectric interface in a Hall-bar heterostructure field effect transistor. z indicates the heterostructure growth direction. The heterostructure is terminated by exposure to dichlorosilane (DCS) gas at a temperature below the threshold for growing an epitaxial Si cap, and the dielectric stack comprises a SiO_x layer formed by exposure of the heterostructure to air at room temperature and an AlO_x layer formed by atomic layer deposition (ALD). (b) BF-STEM image of the active layers of the ^{28}Si/SiGe heterostructure field effect transistor showing, from left to right, the $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer layer, the tensile-strained ^{28}Si quantum well, the $Si_{0.7}Ge_{0.3}$ barrier, followed by the SiO_x/AlO_x dielectric stack. (c) Electron energy loss spectroscopy (EELS) semi-quantitative concentration depth profiles across the semiconductor/dielectric interface for Si (blue), Ge (red), O (green), and Al (black). (d) 15 nm×45 nm wide 2D maps by EELS using low-energy edges to recognize differences between the different bonding states: Si (blue), SiO_x (magenta), and AlO_x (green). We do not detect any Cl or H signal above the background noise in our EELS data.

experiments. In Refs. [3, 7, 12, 16]) we deposited a thin epitaxial Si cap at 675 °C using DCS. Here we reduce the substrate temperature to 500 °C, below the desorption temperature of chlorine from the surface (600–650 °C),[17, 18] under the same conditions of DCS flow and pressure. According to literature[19–25], we expect that exposure to DCS at 500 °C essentially suppresses crystalline growth but creates an amorphous Si-rich layer on $Si_{0.7}Ge_{0.3}$. After terminating the deposition cycle with this step, the heterostructure

is removed from the growth reactor and a native oxide is formed upon exposure to air at room temperature. We identify the native oxide as SiO_x based on the chemical analysis in Fig. 4.3(c),(d). Then, we fabricate Hall-bar shaped H-FETs using the process described in Ref. [12]. In short, the process comprises the implantation of ohmic contacts and rapid thermal annealing at 700 °C, the atomic layer deposition at 300 °C of a 10 nm Al_2O_3 dielectric layer on the SiO_x, and the final deposition of a Hall-bar shaped metallic gate, electrically insulated from the heterostructure by the SiO_x/Al_2O_3 dielectric stack.

Figure 4.3(b) shows a bright-field scanning transmission electron microscopy (BF-STEM) image of the heterostructure and of the dielectric stack under the gate stack at the end of the H-FET fabrication process. The Si quantum well is uniform, without extended defects, and is characterized by sharp top and bottom interfaces to the $Si_{0.7}Ge_{0.3}$ layers, in agreement with our previous reports.[3, 7, 12] The semiconductor/dielectric interface is similarly sharp, highlighted by the perfect atomically sharp semiconductor surface as imaged by BF-STEM. two distinct amorphous layers, which we identify as the SiO_x and AlO_x layers, appear on the dielectric side of the interface. We gain insights into the nature of the semiconductor/dielectric interface and the dielectric stack by performing electron energy loss spectroscopy (EELS)(Supplementary). In Fig. 4.3(c), we show the semi-quantitative concentration profiles using the Si-K (1839-2084 eV), Al-K (1560-1700 eV), O-L (532-660 eV), and Ge-L (1220-1400 eV) high energy edge. The Si (blue) and Ge (red) concentration profiles decrease together whilst the oxygen (green) signal is increasing. We deduce that oxidation of the $Si_{0.7}Ge_{0.3}$ barrier on top of an amorphous Si-rich layer results in a sharp $SiGe/SiO_x$ semiconductor/dielectric interface. This is confirmed by the minor Ge pile-up on the semiconductor side of the interface,[26, 27] which appears as a dark line in BF-STEM [Fig. 4.3(b)] and suggests that the top of the single crystalline $Si_0.7Ge_{0.3}$ barrier has been oxidized and that Ge oxides at the interface are absent[28, 29]. Furthermore, the Al signal (black line) rises after the Si signal from SiO_x has trailed, indicating that the dielectric stack retains the two distinct SiO_x and AlO_x layers.

In Fig. 4.3(d), we show the chemical mapping by EELS of Si (blue), SiO_x (magenta), and AlO_x (green) along and across the semiconductor/dielectric interface, together with the intensity profiles. To recognize differences between the different bonding states, we use the low-energy Si-L edge (96.3-100.8 eV) for the semiconductor phase and a shifted Si-L edge (101.4-107.1 eV) for the oxide phase and Al-L (73.8-79.5 eV) for the oxidized Al phase. The $SiGe/SiO_x$ interface is sharp throughout the image, whereas the SiO_x/AlO_x interface shows some interdiffusion. By fitting the intensity profiles with exponential functions[30], we characterize the size of the interfaces with the leading (towards the surface) and trailing (from the surface) exponential slopes λ_L and λ_T. We find $\lambda_L^{\mathrm{Si}} = (1.0 \pm 0.1)$ nm and $\lambda_T^{\mathrm{SiO_x}} = (0.8 \pm 0.1)$ nm. Conversely, we find $\lambda_L^{\mathrm{SiO_x}} = (1.9 \pm 0.1)$ nm and $\lambda_T^{\mathrm{AlO_x}} = (3.1 \pm 0.2)$ nm. Overall, the transition from epitaxial SiGe to amorphous SiO_x interface is sharper than the transition between SiO_x and AlO_x, pointing to a degree of intermixing at the latter interface.

We characterized the H-FETs by magnetotransport measurements at a temperature of 1.7 K and 190 mK[2] in refrigerators equipped with cryo-multiplexers.[31] With this approach, we measure multiple devices from a wafer in the same cool-down. The devices are operated in accumulation mode, in which electrons populate the undoped ^{28}Si quantum well by applying a positive DC gate voltage (V_G). We measure the longitudinal and transverse components of the resistivity tensor, ρ_{xx} and ρ_{xy}, by using standard four-probe lock-in techniques at fixed AC source-drain bias of 100 µV. We calculate the longitudinal σ_{xx} and transverse σ_{xy} conductivity via tensor inversion. We measure electron density (n) and mobility (μ) with the classical Hall effect at low perpendicular magnetic field B.

4.3. ELECTRICAL CHARACTERIZATION AT 1.7 K

Figure 4.2(a) shows for a typical device the turn-on and pinch-off source-drain current I_{SD} as a function of increasing and decreasing V_G, respectively. Above a threshold voltage (V_G = 350 mV), the current starts flowing in the channel and increases monotonically. If the gate voltage is operated within the operational gate voltage range ΔV_G (red curve), I_{SD} is stable, and the threshold and pinch-off voltages overlap. At higher V_G, I_{SD} saturates due to charge build-up at the semiconductor/dielectric interface, triggering hysteresis and, consequently, a shift in pinch-off voltage. As shown in Fig. 4.2(b), if V_G is swept within the operational gate voltage range, n increases linearly with V_G up to 6×10^{11} cm^{-2}. From the slope $\frac{dn}{dV_G}$ we derive an effective capacitance per unit area $C \simeq 205$ nF/cm^2 using the relationship $C = e\frac{dn}{dV_G}$.[31]. This capacitance characterizes the parallel-plate capacitor where the 2DEG in the ^{28}Si quantum well and the metallic top gate are insulated by a SiGe/SiO_x/AlO_x dielectric stack. Figure 4.2(c) shows the density-dependent mobility measured in the same density range as in Fig. 4.2(b). In the low density regime ($n \leq 3 \times 10^{11}$ cm^{-2}), the mobility rises steeply due to the increasing screening of Coulomb scattering from remote charged impurities located at semiconductor/dielectric interface.[32] At higher density ($n \geq 5 \times 10^{11}$ cm^{-2}), the mobility approaches saturation at a value above 2.5×10^5 cm^2/Vs. This weaker density-dependence is typical of a high-quality 2DEG, where the maximum mobility is limited by short-range scattering from impurities within or near the quantum well.[31, 33, 34]

In Fig. 4.2(d)–(f) we plot the distributions of the maximum electric field (E_z^{max}), the percolation density (n_p), and the mobility at high density for heterostructures terminated with an amorphous Si-rich layer (blue) and, as a benchmark, for heterostructures with an epitaxial Si cap (red). These three metrics are obtained from the analysis of measurements in Fig. 4.2(a)–(c), repeated on multiple H-FETs on dies that are randomly selected from different locations across the 100 mm wafer. E_z^{max}, calculated as $C\Delta V_G/\epsilon_0\epsilon_r$, where $\epsilon_r = 11.68$ is the dielectric constant of Si, indicates the maximum electric field that we can apply to the quantum well in the H-FETs before hysteresis. Large E_z^{max} are desirable for device stability, increased tunability, and large valley splitting.[12, 14, 35, 36] n_p

[2] T = 190 mK is the electron temperature obtained by fitting Coulomb blockade peaks (Supplementary) measured on quantum dot devices[7] fabricated on a similar heterostructure. The electron temperature is higher than the temperature of 70 mK measured by a thermometer located on the mixing chamber of the dilution refrigerator

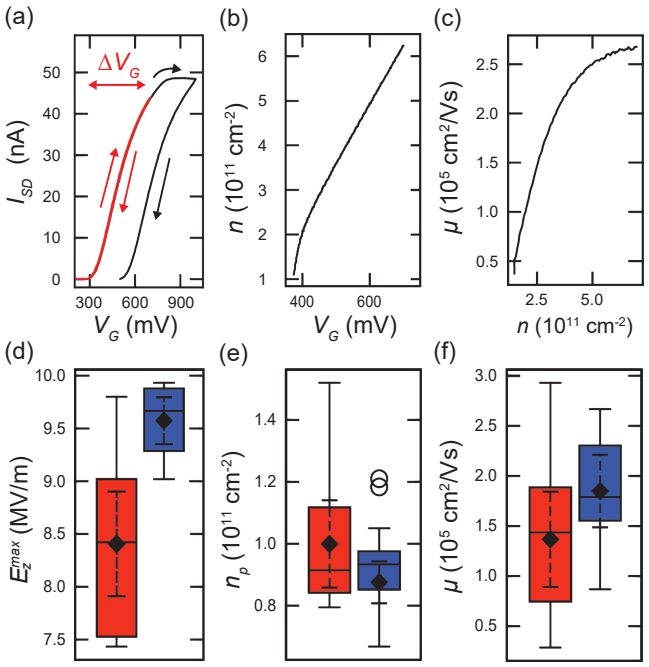


Figure 4.2: (a) Source-drain current I_{SD} measured at $T = 1.7$ K as a function of gate voltage V_G for a typical Hall bar heterostructure field effect transistor (H-FET). The operational gate voltage range ΔV_G indicates the range over which an I_{SD}-V_G curve (red line) can be measured repeatedly without hysteresis and drift. (b) Density n as a function of gate voltage V_G and (c) electron mobility μ as a function of n measured within the operational gate voltage range. (d), (e), (f) Distributions of maximum electric field applicable before hysteresis E_z^{max}, percolation density n_p, and μ measured at $n = 6 \times 10^{11}$ cm^{-2} for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 14 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 16 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.

characterizes disorder in low-density regime, relevant for quantum dot operation, and is obtained by fitting the density-dependent σ_{xx} to percolation theory.[37] Finally, the mobility at high density is a probe for disorder arising from within or nearby the quantum well.[32–34] Overall, H-FETs perform better when the SiGe barrier is terminated with an amorphous Si-rich layer. We measure a 9% increase in mean E_z^{max}, a 7% decrease in mean percolation density, and a 40% increase in mean mobility. Most importantly, we observe a reduction in the spread of E_z^{max}, n_p, and μ of $\simeq$ 300%, $\simeq$ 200%, and $\simeq$ 30% respectively, pointing to an increased uniformity on a 100 mm wafer scale.

We further characterize disorder in the ^{28}Si/SiGe heterostructure at 190 mK by measuring the single-particle relaxation time τ_q[38] in the quantum Hall regime. From τ_q we derive the quantum mobility $\mu_q = e\tau_q/m^*$, where e is the elementary charge and m^* is the effective mass, and the quantum level broadening of the momentum eigenstates $\Gamma = \hbar/2\tau_q$, here $\hbar$ is the reduced Planck constant. μ_q, associated with τ_q, is influenced by all scattering events and is different from the mobility $\mu = e\tau_t/m^*$, where the scattering

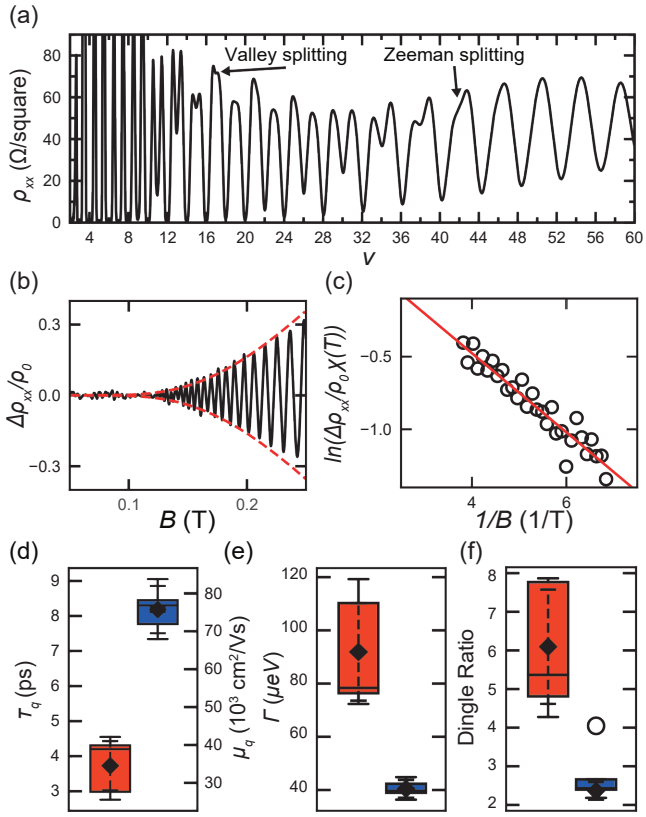


Figure 4.3: (a) Longitudinal resistivity ρ_{xx} measured at $T = 190$ mK as a function of Landau level filling factor ν. These measurements are performed at fixed $n = 4.75 \times 10^{11}$ cm^{-2} while sweeping the perpendicular magnetic field B. Spin and valley degenerate Landau levels correspond to $\nu = 4k$ (k = 1,2,3...), Zeeman split levels to $\nu = (4k\text{-}2)$, whereas valley split levels correspond to odd integer filling factors ν. Arrows indicate the filling factors at which Zeeman spin splitting and valley splitting are resolved. (b) Normalized resistivity oscillation amplitude (black curve) as a function of B after polynomial background subtraction. The arrow indicates the magnetic field at which Shubnikov–de Haas oscillations are resolved. The red dashed line is the theoretical fit of the oscillations envelope from which we extract τ_q. (c) Dingle plot (open circles) from the first twenty most resolved resistivity oscillation maxima and minima and theoretical curve (solid red line) computed using τ_q from the analysis in (b). (d), (e), (f) Distributions of τ_q, μ_q, Γ, and Dingle ratio measured at $n = (5-6) \times 10^{11}$ cm^{-2} for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 5 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 7 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.

time τ_t is unaffected by forward scattering. Therefore, τ_q and μ_q qualify the disorder in the heterostructure more comprehensively than τ_t and μ.

Figure 4.3(a) shows for the H-FET with the highest mobility a measurement of ρ_{xx} plotted for clarity against the Landau level filling factor $\nu = hn/eB$, where h is the Plank constant. This measurement was performed at fixed density $n = 4.75 \times 10^{11}$ cm^{-2} by keeping V_G constant and sweeping B. Onset of Shubnikov–de Haas oscillation, Zeeman splitting, and valley splitting occurs at 0.125, 0.43, and 1.15 T, respectively, corresponding to $\nu = 152$, 42 and 17. The observation of Shubnikov–de Haas oscillations, Zeeman and valley splitting at these high filling factors indicates a very low level of disorder.[39] Figure 4.3(b) shows the normalized oscillation amplitude $\Delta\rho_{xx}/\rho_0 = (\rho_{xx} - \rho_0)/\rho_0$ in the low magnetic field regime after polynomial background subtraction. $\rho_0 \simeq 63\ \Omega$/square is the longitudinal resistivity at zero magnetic field from which we extract a mobility of 2.7×10^5 cm^2/Vs. We estimate $\tau_q = (7.4 \pm 0.1)$ ps from a fit of the Shubnikov-de Haas oscillation envelope to the function $\Delta\rho_{xx} = 4\rho_0\chi(T)\exp(-\pi/\omega_c\tau_q)$, where $\chi(T) = (2\pi^2 k_B T/\hbar\omega_c)/\sinh(2\pi^2 k_B T/\hbar\omega_c)$. Here $T = 190$ mK, k_B is the Boltzmann constant, and ω_c is the cyclotron frequency calculated using a fixed $m^* = 0.19\, m_e$.[39, 40] From τ_q we derive $\mu_q = (6.8 \pm 0.1) \times 10^4$ cm^2/Vs, $\Gamma = (44 \pm 1)$ μeV, and find a Dingle ratio $\tau_t/\tau_q \simeq 3.8$. The Dingle plot of Fig. 4.3(c) highlights the high number of oscillation maxima and minima used in the fitting procedure.

In Fig. 4.3(d)–(f) we plot the distributions for τ_q (and μ_q), Γ, and the Dingle ratio τ_t/τ_q, measured in the high density regime ($n = (5-6) \times 10^{11}$) cm^{-2}). As in Fig. 4.2(d)–(f), we consider heterostructures terminated with an amorphous Si-rich layer (blue, 5 H-FETs measured) and heterostructures with an epitaxial Si cap (red, 7 H-FETs measured). Heterostructures with an amorphous Si-rich layer have a mean τ_q of (8.1 ± 0.5) ps, and consequently a mean μ_q of $(7.5 \pm 0.6) \times 10^4$ cm^2/Vs and Γ of (40 ± 3) μeV, representing a $\simeq 2\times$ improvement compared to heterostructures with an epitaxial Si cap. Consistent with the trend in Fig. 4.2(d)–(f), we find a significant reduction in spread for τ_q (30%), and consequently for μ_q, Γ. Furthermore, in heterostructures with an amorphous Si-rich layer, we find a mean Dingle ratio of (2.3 ± 0.2) in heterostructures with an amorphous Si-rich layer. This mean value is $\simeq 300\%$ smaller and has an 80% reduction in spread compared to heterostructures with an epitaxial Si cap. This low value of the Dingle ratio indicates that short-range scattering from impurities within or near the quantum well is the dominant scattering mechanism[32], in agreement with the analysis of the mobility-density curve. Scattering from remote impurities is reduced thanks to a better semiconductor/dielectric interface. Our mean value for τ_q in ^{28}Si/SiGe is also on par with the best value reported in Ref. [33] from H-FETs in Si/SiGe heterostructures featuring an epitaxial Si cap. However, in our samples, the semiconductor/dielectric interface is much closer to the channel (30 nm compared to 50 nm in Ref. [33]). Therefore, this comparison confirms that our devices have limited scattering from remote impurities due to a high-quality and uniform semiconductor/dielectric interface associated with the termination process at 500 °C.

4.4. DISCUSSION

In summary, we challenged the mainstream approach to deposit an epitaxial Si cap on ^{28}Si/SiGe heterostructures and, instead, we terminated the SiGe barrier with an amorphous Si-rich layer, obtained by exposure to DCS at 500 °C. Compared to previous heterostructures that feature an epitaxial Si cap and that have already produced high-performance spin qubits,[3, 7], we demonstrate an improvement in performance of H-FETs in terms of mean value and spread of mobility, percolation density, maximum electric field before hysteresis, and single particle relaxation time (and hence quantum mobility). We speculate that performance improves because the amorphous Si-rich layer gets completely oxidized compared to the epitaxial Si cap (Supplementary), thereby creating a more uniform SiO_x layer with fewer scattering centers. By having a better semiconductor/dielectric interface and wafer-scale uniformity, we expect this material stack to lead to Si spin qubits with improved yield and performance. In this direction, charge noise measured in quantum dots on these heterostructures will be very informative as these measurements probe the dynamics of charge fluctuations that transport experiments are not very sensitive to. These results motivate new studies, for example, by varying the temperature and/or time of exposure to DCS to understand in detail the nature of the amorphous Si-rich layer on the SiGe barrier, the role of Cl and H upon oxidation in air, and to use this knowledge as a tool for further optimizing the semiconductor/dielectric interface.

4.5. SUPPLEMENTARY

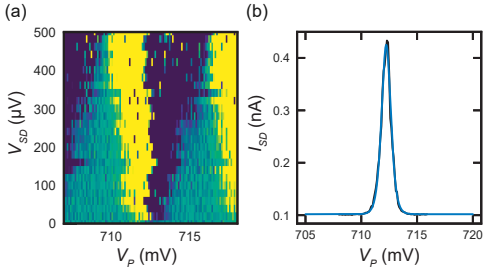


Figure 4.4: Differential conductance (dI/dV) showing representative Coulomb blockade diamonds as a function of the source-drain voltage (V_{SD}) and plunger gate voltage (V_P). The measurements are performed using the sensing dot on single-layer quantum dot devices in transport regime [3]. From the shape of the Coulomb diamond, we derive an effective lever arm via the equation $\alpha = \frac{m_S m_D}{m_S - m_D} = 0.06$ (eV/V), where m_S and m_D are the slopes of the Coulomb diamond from source and drain. (b) Coulomb peak with superimposed fit to the function $I(V_P) = A + B\cosh^{-2}(\frac{\alpha(V_0 - V)}{2k_B T})$ where A, B, V_0, and T_e are fitting parameter [41]. From the fit, we derive an electron temperature of $T_e = 190(10)$ mK. The Coulomb peak is measured using a source-drain voltage of $V_{SD} = 100\ \mu$V.

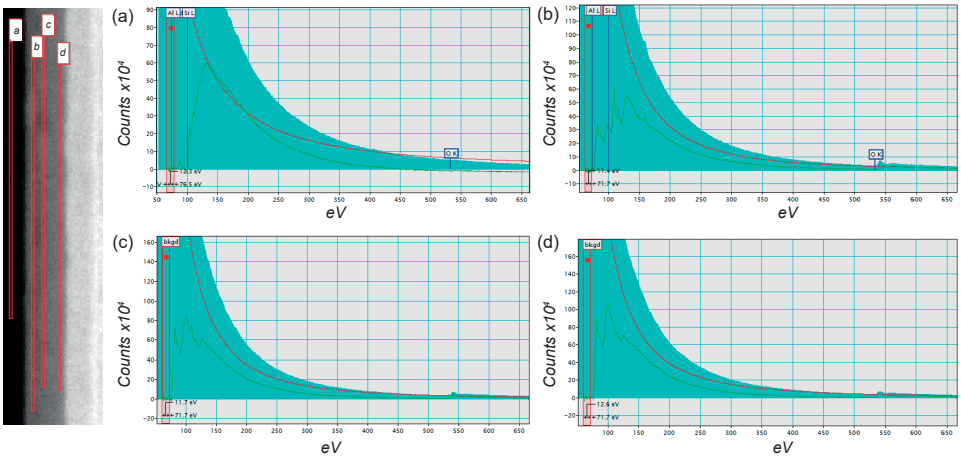


Figure 4.5: Extended data comparing the structural and chemical properties of the semiconductor/dielectric interface for heterostructures terminated by a Si-rich amorphous layer obtained by exposure to DCS at 500 °C (first row) and for heterostructures with an epitaxial Si cap grown at 675 °C (second row). (a), (e) Bright Field-STEM zoom-in images of the dielectric and gate metal stack (b), (f) Electron energy loss spectroscopy (EELS) semi-quantitative concentration depth profiles across the semiconductor/dielectric interface for Si (blue), Ge (red), O (green), and Al (black). (c), (g) 15 nm×45 nm wide 2D maps by EELS using low-energy edges to recognize the different bonding states: Si (blue), SiO_x (magenta) and AlO_x (green). (d), (h) Z Contrast-STEM zoom images of the ^{28}Si QW with superimposed intensity profiles. QW thickness and interface sharpness remain similar in the two heterostructures.

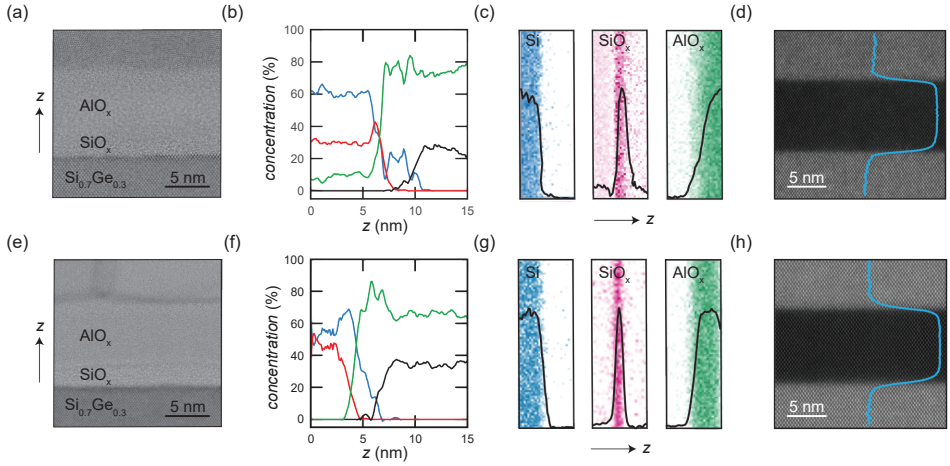


Figure 4.6: EELS raw energy profiles taken in the SiGe spacer (a), in the SiO_x layer (b), and in the AlOx dielectric (c), (d). The raw spectrum (blue), the background profile (red), and the edge profile (green) are shown. The O-L edge (≃540 eV) is visible in the oxide layers (b,c,d) while it is absent in the SiGe spectrum (a). It is impossible to recognize any trace of Cl, which should appear as an energy peak at around 200 eV.

BIBLIOGRAPHY

[1] L. M. K. Vandersypen et al. “Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent”. In: *npj Quantum Information* 3.1 (2017), p. 34. DOI: 10.1038/s41534-017-0038-y.

[2] Ruoyu Li et al. “A crossbar network for silicon quantum dot qubits”. In: *Science Advances* 4.7 (2018), eaar3960.

[3] Xiao Xue et al. “Quantum logic with spin qubits crossing the surface code threshold”. In: *Nature* 601.7893 (2022), pp. 343–347.

[4] Akito Noiri et al. “Fast universal quantum gate above the fault-tolerance threshold in silicon”. In: *Nature* 601.7893 (2022), pp. 338–342.

[5] AR Mills et al. “Two-qubit silicon quantum processor with operation fidelity exceeding 99%”. In: *arXiv preprint arXiv:2111.11937* (2021).

[6] Patrick Harvey-Collard et al. “Circuit quantum electrodynamics with two remote electron spins”. In: *Preprint at http://arxiv.org/abs/2108.01206* (Aug. 2021).

[7] Xiao Xue et al. “CMOS-based cryogenic control of silicon quantum circuits”. In: *Nature* 593.7858 (2021), pp. 205–210.

[8] WIL Lawrie et al. “Quantum dot arrays in silicon and germanium”. In: *Applied Physics Letters* 116.8 (2020), p. 080501.

[9] Ted Thorbeck and Neil M Zimmerman. “Formation of strain-induced quantum dots in gated semiconductor nanostructures”. In: *AIP Advances* 5.8 (2015), p. 087107.

[10] Elliot J Connors et al. “Low-frequency charge noise in Si/SiGe quantum dots”. In: *Physical Review B* 100.16 (2019), p. 165305.

[11] Tom Struck et al. “Low-frequency spin qubit energy splitting noise in highly purified 28Si/SiGe”. In: *npj Quantum Information* 6.1 (May 2020), p. 40. ISSN: 2056.

[12] Brian Paquelet Wuetz et al. “Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots”. In: *arXiv preprint arXiv:2112.09606* (2021).

[13] Edward H. Chen et al. “Detuning Axis Pulsed Spectroscopy of Valley-Orbital States in Si / Si - Ge Quantum Dots”. en. In: *Physical Review Applied* 15.4 (Apr. 2021), p. 044033. ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.15.044033. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.15.044033 (visited on 02/04/2022).

[14] Arne Hollmann et al. “Large, Tunable Valley Splitting and Single-Spin Relaxation Mechanisms in a Si/SiGe Quantum Dot”. In: *Physical Review Applied* 13.3 (Mar. 2020), p. 034068. DOI: 10.1103/PhysRevApplied.13.034068. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.13.034068 (visited on 02/04/2022).

[15] D. Sabbagh et al. “Quantum Transport Properties of Industrial $^{28}Si/^{28}SiO_2$”. In: *Phys. Rev. Applied* 12 (1 July 2019), p. 014013. DOI: 10.1103/PhysRevApplied.12.014013. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.12.014013.

[16] Nodar Samkharadze et al. “Strong spin-photon coupling in silicon”. In: *Science* 359.6380 (2018), pp. 1123–1127.

[17] Q. Gao et al. “Chlorine bonding sites and bonding configurations on Si(100)–(2×1)”. In: *The Journal of Chemical Physics* 98.10 (May 1993), pp. 8308–8323. ISSN: 0021-9606. DOI: 10.1063/1.464536. URL: https://aip.scitation.org/doi/10.1063/1.464536 (visited on 02/15/2022).

[18] Leonid Bolotov et al. “Electronic modification of wet-prepared Si surfaces by a dichlorosilane reaction at elevated temperature”. en. In: *Applied Surface Science* 570 (Dec. 2021), p. 151135. ISSN: 01694332. DOI: 10.1016/j.apsusc.2021.151135. URL: https://linkinghub.elsevier.com/retrieve/pii/S0169433221021917 (visited on 02/15/2022).

[19] J. M. Hartmann et al. “Reduced Pressure–Chemical Vapour Deposition of Si/SiGe heterostructures for nanoelectronics”. en. In: *Materials Science and Engineering: B.* Front-End Junction and Contact Formation in Future Silicon/Germanium Based Devices 154-155 (Dec. 2008), pp. 76–84. ISSN: 0921-5107. DOI: 10.1016/j.mseb.2008.08.009. URL: https://www.sciencedirect.com/science/article/pii/S0921510708003462 (visited on 02/15/2022).

[20] J M Hartmann et al. “Epitaxial growth of Ge thick layers on nominal and 6° off Si(0 0 1); Ge surface passivation by Si”. In: *Semiconductor Science and Technology* 24.5 (May 2009), p. 055002. ISSN: 0268-1242, 1361-6641. DOI: 10.1088/0268-1242/24/5/055002. URL: https://iopscience.iop.org/article/10.1088/0268-1242/24/5/055002 (visited on 02/15/2022).

[21] M. Bauer and S.G. Thomas. “Novel chemical precursors and novel CVD strategies enabling low temperature epitaxy of Si and Si:C alloys”. en. In: *Thin Solid Films* 518.6 (Jan. 2010), S200–S203. ISSN: 00406090. DOI: 10.1016/j.tsf.2009.10.088. URL: https://linkinghub.elsevier.com/retrieve/pii/S0040609009017337 (visited on 02/15/2022).

[22] B. Vincent et al. “Low temperature Si homo-epitaxy by reduced pressure chemical vapor deposition using dichlorosilane, silane and trisilane”. en. In: *Journal of Crystal Growth* 312.19 (Sept. 2010), pp. 2671–2676. ISSN: 00220248. DOI: 10.1016/j.jcrysgro.2010.06.013. URL: https://linkinghub.elsevier.com/retrieve/pii/S0022024810003994 (visited on 02/15/2022).

[23] B. Vincent et al. “Si passivation for Ge pMOSFETs: Impact of Si cap growth conditions”. en. In: *Solid-State Electronics* 60.1 (June 2011), pp. 116–121. ISSN: 00381101. DOI: 10.1016/j.sse.2011.01.049. URL: https://linkinghub.elsevier.com/retrieve/pii/S0038110111000785 (visited on 02/15/2022).

[24] J. M. Hartmann et al. “A benchmarking of silane, disilane and dichlorosilane for the low temperature growth of group IV layers”. en. In: *Thin Solid Films*. ICSI-7 520.8 (Feb. 2012), pp. 3185–3189. ISSN: 0040-6090. DOI: 10.1016/j.tsf.2011.10.164. URL: https://www.sciencedirect.com/science/article/pii/S0040609011019043 (visited on 02/15/2022).

[25] J. Aubin, J. M. Hartmann, and V. Benevent. “Epitaxial growth of Si and SiGe at temperatures lower than 500°C with disilane and germane”. en. In: *Thin Solid Films*. The 9th International Conference on Silicon Epitaxy and Heterostructures 602 (Mar. 2016), pp. 36–42. ISSN: 0040-6090. DOI: 10.1016/j.tsf.2015.07.024. URL: https://www.sciencedirect.com/science/article/pii/S0040609015006902 (visited on 02/15/2022).

[26] WS Liu et al. “The hydridation and nitridation of GeSi oxide annealed in ammonia”. In: *Journal of Applied Physics* 78.4 (1995), pp. 2631–2634.

[27] Ethan Long et al. “Ge redistribution in SiO2/SiGe structures under thermal oxidation: Dynamics and predictions”. In: *Journal of Applied Physics* 111.2 (Jan. 2012), p. 024308. ISSN: 0021-8979. DOI: 10.1063/1.3677987. URL: https://aip.scitation.org/doi/10.1063/1.3677987 (visited on 02/04/2022).

[28] HK Liou et al. “Effects of Ge concentration on SiGe oxidation behavior”. In: *Applied physics letters* 59.10 (1991), pp. 1200–1202.

[29] FK LeGoues et al. “Oxidation studies of SiGe”. In: *Journal of Applied Physics* 65.4 (1989), pp. 1724–1728.

[30] EF Schubert. “Delta-doping of semiconductors: Electronic, optical, and structural properties of materials and devices”. In: *Semiconductors and Semimetals*. Vol. 40. Elsevier, 1994, pp. 1–151.

[31] B. Paquelet Wuetz et al. “Multiplexed quantum transport using commercial off-the-shelf CMOS at sub-kelvin temperatures”. en. In: *npj Quantum Information* 6.1 (May 2020), p. 43. ISSN: 2056-6387. DOI: 10.1038/s41534-020-0274-4. URL: https://www.nature.com/articles/s41534-020-0274-4 (visited on 05/27/2020).

[32] Don Monroe et al. “Comparison of mobility-limiting mechanisms in high-mobility Si1-xGex heterostructures”. In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 11.4 (July 1993), pp. 1731–1737. ISSN: 1071-1023. DOI: 10.1116/1.586471. URL: https://avs.scitation.org/doi/abs/10.1116/1.586471 (visited on 02/08/2022).

[33] X Mi et al. “Magnetotransport studies of mobility limiting mechanisms in undoped Si/SiGe heterostructures”. In: *Physical Review B* 92.3 (2015), p. 035304.

[34] D. Laroche et al. “Scattering mechanisms in shallow undoped Si/SiGe quantum wells”. In: *AIP Advances* 5.10 (Oct. 2015), p. 107106. DOI: 10.1063/1.4933026. URL: https://aip.scitation.org/doi/10.1063/1.4933026 (visited on 02/08/2022).

[35] Mark Friesen et al. “Valley splitting theory of Si/SiGe quantum wells”. In: *Physical Review B* 75.11 (Mar. 2007), p. 115318. DOI: 10.1103/PhysRevB.75.115318. URL: https://link.aps.org/doi/10.1103/PhysRevB.75.115318 (visited on 05/27/2020).

[36] Brian Paquelet Wuetz et al. “Effect of Quantum Hall Edge Strips on Valley Splitting in Silicon Quantum Wells”. In: *Physical Review Letters* 125.18 (Oct. 2020), p. 186801. DOI: 10.1103/PhysRevLett.125.186801. URL: https://link.aps.org/doi/10.1103/PhysRevLett.125.186801 (visited on 02/16/2022).

[37] L. A. Tracy et al. “Observation of percolation-induced two-dimensional metal-insulator transition in a Si MOSFET”. In: *Physical Review B* 79.23 (June 2009), p. 235307. DOI: 10.1103/PhysRevB.79.235307. URL: https://link.aps.org/doi/10.1103/PhysRevB.79.235307 (visited on 05/27/2020).

[38] S. Das Sarma and Frank Stern. “Single-particle relaxation time versus scattering time in an impure electron gas”. In: *Physical Review B* 32.12 (Dec. 1985), pp. 8442–8444. DOI: 10.1103/PhysRevB.32.8442. URL: https://link.aps.org/doi/10.1103/PhysRevB.32.8442 (visited on 06/26/2020).

[39] Qi Qian et al. “Quantum lifetime in ultrahigh quality GaAs quantum wells: Relationship to Δ 5/2 and impact of density fluctuations”. In: *Physical Review B* 96.3 (2017), p. 035309.

[40] PT Coleridge. “Small-angle scattering in two-dimensional electron gases”. In: *Physical Review B* 44.8 (1991), p. 3793.

[41] C. W. J. Beenakker. “Theory of Coulomb-blockade oscillations in the conductance of a quantum dot”. In: *Physical Review B* 44.4 (July 1991), pp. 1646–1656. ISSN: 0163-1829. DOI: 10.1103/PhysRevB.44.1646.

5

REDUCING CHARGE NOISE IN QUANTUM DOTS BY USING A THIN SI QUANTUM WELL

Charge noise in the host semiconductor degrades the performance of spin qubits and poses an obstacle to controlling large quantum processors. However, it is challenging to engineer the heterogeneous material stack of gate-defined quantum dots to improve charge noise systematically. Here, we address the semiconductor-dielectric interface and the buried quantum well of a ^{28}*Si/SiGe heterostructure and show the connection between charge noise, measured locally in quantum dots, and global disorder in the host semiconductor, measured with macroscopic Hall bars. In 5 nm thick* ^{28}*Si quantum wells, we find that improvements in the scattering properties and uniformity of the two-dimensional electron gas over a 100 mm wafer correspond to a significant reduction in charge noise, with a minimum value of* 0.29 ± 0.02 $\mu eV/\sqrt{Hz}$ *at 1 Hz averaged over several quantum dots. We extrapolate the measured charge noise to simulated dephasing times to* CZ*-gate fidelities that improve nearly one order of magnitude. These results indicate a clean and quiet crystalline environment for integrating long-lived and high-fidelity spin qubits into a larger system.*

This chapter has been published as: Brian Paquelet Wuetz, **Davide Degli Esposti**, Anne-Marije J. Zwerver, Sergey V. Amitonov, Marc Botifoll, Jordi Arbiol, Amir Sammak, Lieven M. K. Vandersypen, Maximilian Russ & Giordano Scappucci, "Reducing charge noise in quantum dots by using thin silicon quantum wells." Nature Communication **14**, 1385 (2023).

5.1. INTRODUCTION

Spin-qubits in silicon quantum dots are a promising platform for building a scalable quantum processor because they have a small footprint[1], long coherence times[2, 3], and are compatible with advanced semiconductor manufacturing[4]. Furthermore, rudimentary quantum algorithms have been executed[5] and quantum logic at high-fidelity performed[6–9]. As the qubit count is increasing, with a six-qubit processor demonstrated[10], significant steps have been taken to couple silicon spin qubits at a distance, via microwave photons or spin shuttling[11–16], towards networked spin-qubit tiles[17]. However, electrical fluctuations associated with charge noise in the host semiconductor can decrease qubit readout and control fidelity[18]. Reducing charge noise independently of the device location on a wafer is pivotal to achieving the ubiquitous high-fidelity of quantum operations within and across qubit tiles, necessary to execute more complex quantum algorithms.

Charge noise is commonly associated with two-level fluctuators (TLF)[19] in the semiconductor host. In gated heterostructures with buried quantum wells, TLF may arise from impurities in several locations: within the quantum well, the semiconductor barrier, the semiconductor/dielectric interface, and the dielectrics layers above[20–26]. Furthermore, previous work on strained-Si MOSFETs[27–29], with strained-Si channels deposited on SiGe strain relaxed buffers, has associated charge noise with dislocations arising from strain relaxation, either deep in the SiGe buffer or at the quantum well/buffer interface. Since these impurities and dislocations are randomly distributed over the wafer and are also a main scattering source for electron transport in buried quantum wells[30], a holistic approach to materials engineering should be taken to address disorder in two-dimensional electron gases and charge noise in quantum dots.

In this work, we demonstrate thin quantum wells in ^{28}Si/SiGe heterostructures with low and uniform charge noise, measured over several gate-defined quantum dot devices. By linking charge noise measurements to the scattering properties of the two-dimensional electron gas, we show that a quiet environment for quantum dots is obtained by improving the semiconductor/dielectric interface and the crystalline quality of the quantum well. We feed the measured charge noise into a theoretical model, benchmark the model against recent experimental results [6, 10], and predict that these optimized heterostructures may support long-lived and high-fidelity spin qubits.

5.2. RESULTS

5.2.1. DESCRIPTION OF SI/SIGE HETEROSTRUCTURES

Figure 5.1a illustrates the undoped ^{28}Si/SiGe heterostructures grown by reduced-pressure chemical vapour deposition and the gate-stack above. From bottom to top, the material stack comprises a 100 mm Si substrate, a strain-relaxed SiGe buffer layer, a strained ^{28}Si quantum well, a 30 nm thick SiGe barrier, a Si cap oxidized in air to form a SiO_x layer, an AlO_x layer formed by atomic layer deposition, and metallic gates. The SiGe layers above and below the quantum well have a Ge concentration of $\simeq 0.3$ (Methods).

We consider three ^{28}Si/SiGe heterostructures (A, B, C) to improve, in sequence, the semiconductor/dielectric interface (from A to B) and the crystalline quality of the quantum well (from B to C). Heterostructure A has an $\simeq 9$ nm thick quantum well and is termi-

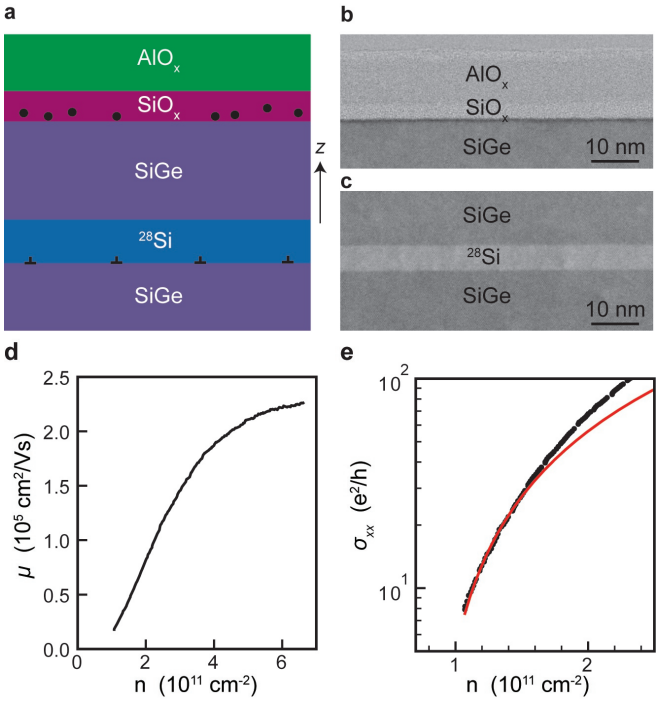


Figure 5.1: **a** Schematics of the ^{28}Si/SiGe heterostructure and dielectric stack above. z indicates the heterostructure growth direction. Circles represent remote impurities at the semiconductor/dielectric interface and perpendicular symbols represent misfit dislocations that might arise at the quantum well/buffer interface due to strain relaxation. **b**, **c** BF-STEM images from heterostructure C highlighting the semiconductor/dielectric interface and the 5 nm thick ^{28}Si quantum well, respectively. **d** Mobility μ and **e** conductivity σ_{xx} measured as a function of density n at a temperature of 1.6 K in a Hall bar H-FET from heterostructure C. The red curve in **e** is a fit to percolation theory.

nated with an epitaxial Si cap grown by dichlorosilane at 675 °C. This kind of heterostructure has already produced high performance spin-qubits[6, 10, 31]. Heterostructure B misses a final epitaxial Si cap but features an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. Compared to A, heterostructure B supports a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 mm wafer, owing to a more uniform SiO_x layer with less scattering centers[32]. Finally, we introduce here heterostructure C, having the same amorphous Si-rich termination as in heterostructure B, but a thinner quantum well of $\simeq 5$ nm (Supplementary Fig. 1). This is much thinner than the Matthews-Blakeslee critical thickness [33, 34], which is $\simeq 10$ nm[35] for the relaxation of tensile Si on $Si_{0.7}Ge_{0.3}$ via the formation of misfit dislocation at the bottom interface of the quantum well.

Figures 5.1b, c show bright-field scanning transmission electron microscopy (BF-STEM) images from heterostructure C after fabrication of a Hall bar-shaped heterostructure field effect transistors (H-FET). We observe a sharp SiGe/SiO_x semiconductor/dielectric interface (Fig. 5.1b), characterized by a minor Ge pile up (dark line) in line with

Ref. [32]. The ≃ 5 nm thick quantum well (Fig. 5.1c) is uniform and has sharp interfaces to the nearby SiGe, and appears of high crystalline quality.

5.2.2. ELECTRICAL CHARACTERIZATION OF H-FETS

We evaluate the scattering properties of the two-dimensional electron gases by wafer-scale electrical transport measured on Hall-bar shaped H-FETs operated in accumulation mode (Methods). For each heterostructure, multiple H-FETs over a wafer are measured in the same cool-down at a temperature of 1.7 K in refrigerators equipped with cryo-multiplexers[36]. Figures 5.1d, e show typical mobility-density and conductivity-density curves for heterostructure C, from which we extract the mobility measured at high density ($n = 6 \times 10^{11}$ cm^{-2}) and the percolation density (n_p)[37]. The mobility rises steeply at low density due to progressive screening of scattering from remote impurities and flattens at higher density ($n > 5 \times 10^{11}$ cm^{-2}), limited by scattering from impurities within or nearby the quantum well, for example uniform background charges, surface roughness, or crystalline defects such as threading or misfit dislocations[30, 38].

5.2.3. CHARGE NOISE MEASUREMENTS IN QUANTUM DOTS

For charge noise measurements, we use devices comprising a double quantum dot and a charge sensor quantum dot nearby, illustrated in Fig. 5.2a. Using the same device design, two-qubit gates with fidelity above 99% were demonstrated[6], silicon quantum circuits were controlled by CMOS-based cryogenic electronics[31], and energy splittings in ^{28}Si/SiGe heterostructures were studied with statistical significance[39].

Here, we electrostatically define a multi-electron quantum dot in the charge sensor by applying gate voltages to the accumulation gates SDRAcc and SDLAcc, the barriers SDLB and SDRB, and the plunger gate P. All other gates (red in Fig. 5.2a) are set to 0 V for measurements of heterostructure B and C, whereas they are positively biased in heterostructure A to facilitate charge accumulation in the sensor (Methods). Figure 5.2b shows typical Coulomb blockade oscillations of the source-drain current I_{SD} for a charge sensor from heterostructure C measured at a dilution refrigerator base temperature of 50 mK. We follow the same tune-up procedure (Methods) consistently for all devices, and we measure charge noise at the flank of each Coulomb peak within the V_P range defined by the first peak observable in transport and the last one before the onset of a background channel (Supplementary Figs. 3,4). For example, in Figure 5.2b, we consider Coulomb peaks within the V_P range from 260 mV to 370 mV. The data collected in this systematic way is taken as a basis for comparison between the three different heterostructures in this study.

For each charge noise measurement at a given V_P we acquire 60 s (heterostructure A) or 600 s (heterostructures B, C) long traces of I_{SD} and split them into 10 (heterostructure A) or 15 windows (heterostructures B, C). We obtain the current noise spectrum S_I by averaging over the 10 (15) windows the discrete Fourier transform of the segments (Methods). We convert S_I to a charge noise spectrum S_ϵ using lever arms from Coulomb diamond measurements and the slope of the Coulomb peaks(inset Fig. 5.2b, Methods, and Supplementary Fig.5). A representative charge noise spectrum S_ϵ measured at V_P = 360.3 mV is shown in Fig. 5.2c. We observe an approximate $1/f$ trend at low frequency, pointing towards an ensemble of TLF with a broad range of activation energies affecting

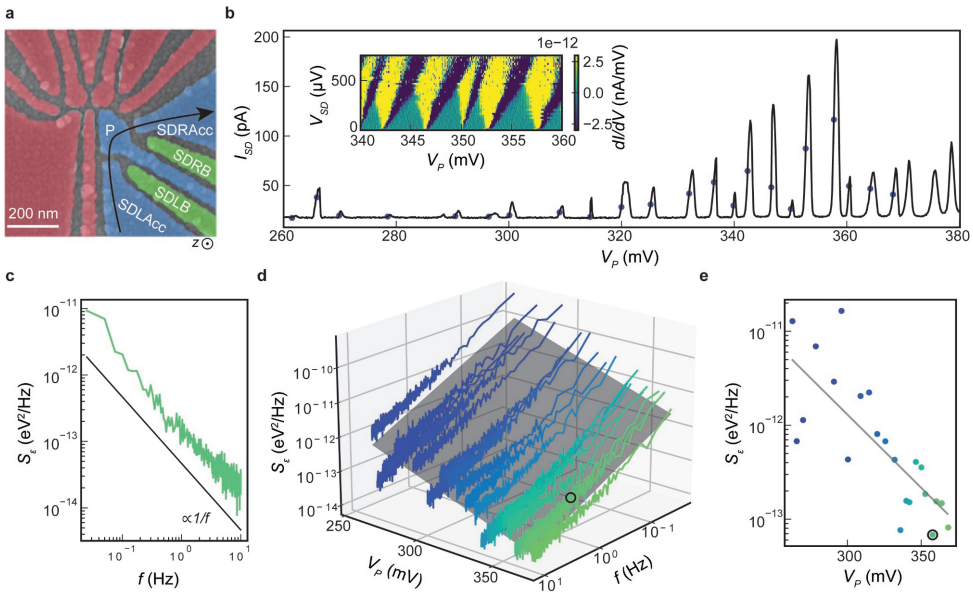


Figure 5.2: **a** False colored SEM-image of a double quantum dot system with a nearby charge sensor. Charge noise is measured in the multi-electron quantum dot defined by accumulation gates SDLAcc and SDRAcc (blue), plunger P (blue), with the current going along the black arrow. In these experiments, the gates defining the double quantum dot (red) are used as screening gates. There is an additional global top gate (not shown) to facilitate charge accumulation when needed. **b** Source-drain current I_{SD} through a charge sensor device fabricated on heterostructure C against the plunger gate voltage V_P. Colored dots mark the position of the flank of the Coulomb peak where charge noise measurements are performed. The inset shows Coulomb diamonds from the same device, plotted as the differential of the current dI/dV as a function of V_P and the source-drain bias V_{SD}. **c** Charge noise spectrum S_ϵ measured at the Coulomb peak at $V_P \simeq 360.3$ mV in **b** and extracted using the corresponding lever arm from Coulomb diamonds. The black trendline is proportional to $1/f$. **d** S_ϵ for the same device in **b**, plotted in 3D as a function of f and V_P. The dark grey plane is a fit through the datasets, i.e., the collection of noise spectra as in **c** measured at different V_P. **e** Line cut through the data in **d** at $f = 1$ Hz, showing the experimental noise S_ϵ (colored dots) and fit (grey line). The black circled data point (also in **d**) marks the minimum charge noise measured for this specific device ($S_{\epsilon,min}$) at $f = 1$ Hz.

charge noise around the charge sensor [40, 41]. Figure 5.2e shows the charge noise $S_\epsilon^{1/2}$ at 1 Hz as a function of V_P. The charge noise decreases, with a linear trend, with increasing V_P, suggesting that, similar to scattering in 2D, screening by an increased electron density shields the electronically active region from noise arising from the heterostructure and the gate stack[42]. From this measurement, we extract, for a given device, the minimum measured charge noise at 1 Hz ($S_{\epsilon,min}^{1/2}$) upon variation of V_P in our experimental range. We use $S_{\epsilon,min}^{1/2}$, as an informative metric to compare charge noise levels from device to device in a given heterostructure. For a given device, all charge noise spectra S_ϵ are plotted in 3D as a function of f and V_P (Fig. 5.2d). To quantify our observations, we fit the data to the plane $\log S_\epsilon = -\alpha \log f + \beta V_P + \gamma$ with coefficient $\alpha = 0.84 \pm 0.01$ indicating the spectrum power law exponent and coefficient $\beta = -15.6 \pm 0.1$ μeV^2/VHz quantifying the change in noise spectrum with increasing plunger gate and, consequently, the susceptibility of charge noise to the increasing electron number in the sensor.

5.2.4. DISTRIBUTION OF TRANSPORT PROPERTIES AND CHARGE NOISE

We have introduced key metrics for 2D electrical transport (μ, n_p) and charge noise (α, β and $S_{\epsilon,min}^{1/2}$) from Hall bar and quantum dot measurements, respectively. In Figs. 5.3a–e we compare the distributions of all these metrics for the three heterostructures A, B, C. Each box-plot is obtained from the analysis of measurements in Figs. 5.1d,e, and Fig. 5.2d repeated on multiple H-FETs or quantum dots, on dies randomly selected from different locations across the 100 mm wafers (Methods). As reported earlier in Ref. [32], the improvement in both mean values and spread for μ and n_p was associated with a reduction of remote impurities when replacing the epitaxial Si cap in heterostructure A with a Si-rich passivation layer in heterostructure B. Moving to heterostructure C, we measure a high mean mobility of $(2.10 \pm 0.08) \times 10^5$ cm^2/Vs and a low mean percolation density of $(7.68 \pm 0.37) \times 10^{10}$ cm^{-2}, representing an improvement by a factor $\simeq 1.4$ and $\simeq 1.3$, respectively (compared to heterostructure A). Most strikingly, the 99% confidence intervals of the mean for μ and n_p are drastically reduced by a factor $\simeq 9.8$ and $\simeq 4.8$, respectively. We speculate that these improvements in heterostructure C are associated with the suppression of misfit dislocations at the quantum well/buffer interface, thereby reducing short-range scattering and increasing uniformity on a wafer scale. This interpretation is supported by the strain characterization discussed above and by previous studies of mobility limiting mechanisms as a function of the quantum well thickness in strained Si/SiGe heterostructures[38].

We now shift our attention to the results of charge noise measurements. First, the power law exponent α (Fig. 5.3c) shows a mean value $\simeq 1$, however the 99% confidence interval and interquartile range increase when moving from heterostructure A to B and C. Next, we observe a decreasing trend for the absolute mean value of coefficient β (Fig. 5.3d), meaning that the noise spectrum is less susceptible to changes in V_P. Finally, we plot in Fig. 5.3e the distributions for $S_{\epsilon,min}^{1/2}$, the minimum charge noise at 1 Hz upon varying V_P. We find in heterostructure C an almost order of magnitude reduction in mean $S_{\epsilon,min}^{1/2}$ to 0.29 ± 0.02 μeV/$\sqrt{\text{Hz}}$. Furthermore, within the distribution of $S_{\epsilon,min}^{1/2}$ for heterostructure C, the minimum value of the measured charge noise as a function of V_P and across quantum dots is 0.15 μeV/$\sqrt{\text{Hz}}$. These charge noise values are on par or compare favorably to the best values reported previously at 1 Hz in gate-defined quantum dots. In multi-electron quantum dots, charge noise of 0.47 μeV/$\sqrt{\text{Hz}}$ was reported for Si/SiGe[43], 0.6 μeV/$\sqrt{\text{Hz}}$ (average value, with a minimum of $\leq$ 0.2 μeV/$\sqrt{\text{Hz}}$) for Ge/SiGe[44], 0.49 ± 0.1 μeV/$\sqrt{\text{Hz}}$ for Si/SiO_2[45], and 1 μeV/$\sqrt{\text{Hz}}$ for InSb[46]. In single-electron quantum dots, charge noise of 0.33 μeV/$\sqrt{\text{Hz}}$ was reported for Si/SiGe[47] and 7.5 μeV/$\sqrt{\text{Hz}}$ for GaAs[48].

We understand the charge noise trends in Figs. 5.3c–e by relating them to the evolution of the disorder landscape moving from heterostructures A to B and C, as inferred by the electrical transport measurements in Figs. 5.3a,b. The narrow distribution of α in heterostructure A points to charge noise from many TLFs possibly located at the low-quality semiconductor/dielectric interface and above. Instead, the larger spread in α in heterostructure B and C implies that deviations from $1/f$ behavior become more frequent, possibly originating from a non-uniform distribution of TLF or from one low-frequency TLF in the surrounding environment of the quantum dot that dominates the power spectrum in the measured interval. The electrical transport measurements sup-

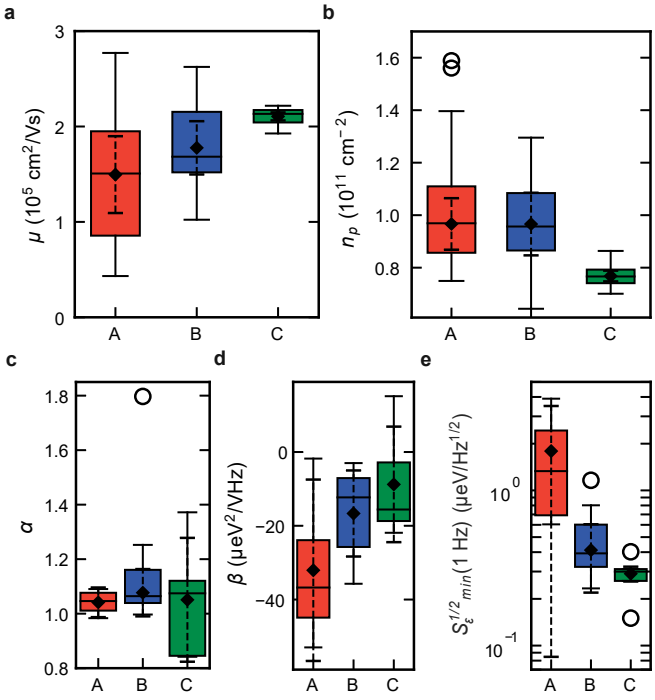


Figure 5.3: **a**, **b** Distributions of mobility μ measured at $n = 6 \times 10^{11}$ cm^{-2} and percolation density n_p for heterostructure A (red, 20 H-FETs measured, of which 16 reported in Ref. [32]), B (blue, 16 H-FETs measured of which 14 reported in Ref. [32]), and C (green, 22 H-FETs measured). **c**- **e** Distributions of noise spectrum power law exponent α, coefficient β indicating the change in noise spectrum with increasing V_P, and minimum charge noise $S^{1/2}_{\epsilon,min}$ within the range of V_P investigated for heterostructure A (red, 4 devices measured), B (blue, 7 devices measured), and C (green, 5 devices measured). Quartile box plots, mode (horizontal line), means (diamonds), 99% confidence intervals of the mean (dashed whiskers), and outliers (circles) are shown.

port this interpretation: scattering from many remote impurities is dominant in heterostructure A, whereas with a better semiconductor/dielectric interface, remote scattering has less impact on the transport metrics of heterostructures B and C.

The decreasing trend in $|\beta|$ is in line with the observation from electrical transport. As the impurity density decreases from heterostructure A to B and C, charge noise is less affected by an increasing V_P, since screening of electrical noise through adding electrons to the charge sensor becomes less effective, possibly due to a smaller TLF-per-volume ratio. While we are not able to measure directly the electron number in the charge sensor, we deem unlikely the hypothesis that charge sensors in heterostructure A are operated with considerably fewer electrons than in heterostructure C. This is because all operation gate voltages in heterostructure A are consistently larger than in heterostructure C (Supplementary Fig. 4), due to the higher disorder.

Finally, the drastic reduction in mean value and spread of $S^{1/2}_{\epsilon,min}$ mirrors the evolution of mean value and spread of n_p and μ. From heterostructure A to B, a reduction in scattering from remote impurities is likely to result in less charge noise from long-range

TLFs. From heterostructure B to C, the larger strain, and consequently the reduction in the possible number of dislocations at the quantum well/buffer interface, further reduces the charge noise picked up by quantum dots. This explanation is based on earlier studies of charge noise in strained Si-MOSFETs[27–29], which showed a correlation between low-frequency noise spectral density and static device parameters. Dislocations at the bottom of the strained channel may act as scattering centers that degrade mobility and as traps for the capture and release of carriers, which causes noise similarly to traps at the dielectric interface.

5.2.5. CALCULATED DEPHASING TIME AND INFIDELITY

To emphasize the improvement of the electrical environment in the semiconductor host, we calculate the dephasing time $T_2^\star$ of charge and spin qubits assuming these qubits experience the same fluctuations as our ^{28}Si/SiGe quantum dots. The dephasing time of a qubit (in the quasistatic limit and far off from a sweet spot) is given by [49]

$$T_2^\star = \frac{h}{\sqrt{2}\pi\sigma} \tag{5.1}$$

with the Planck constant h and the standard deviation

$$\sigma^2 = \left|\frac{\partial \mathscr{E}}{\partial \mu}\right|^2 \times 2\int_{f_{\text{low}}}^{f_{\text{high}}} \frac{S_\epsilon^2}{f^\alpha} \mathrm{d}f. \tag{5.2}$$

Importantly, both the charge noise amplitude $S_\epsilon^2(f)$ and the noise exponent α have a strong impact on the dephasing time while the low and high-frequency cut-off, f_{low} and f_{high}, given by the duration of the experiment have a weaker impact. The prefactor $\left|\frac{\partial \mathscr{E}}{\partial \mu}\right|$ translates shifts in chemical potential of the charge sensor into energy shifts of the qubit and depends on many parameters such as the type of qubit and the device itself. We find $\left|\frac{\partial \mathscr{E}}{\partial \mu}\right| = 1$ for a charge qubit [50] and $\left|\frac{\partial \mathscr{E}}{\partial \mu}\right| \approx 10^{-5}$ for an uncoupled spin- qubit [43] (see Supplementary Information for a derivation of these numbers and the used frequency bandwidths).

Figure 5.4a shows the computed dephasing times of charge qubits (circle) and spin qubits (star) for all three heterostructures. The improvements in our material can be best seen by investigating $T_2^\star$ of the charge qubit since it is directly affected by charge noise. Our theoretical extrapolation shows two orders of magnitude improvement in $T_2^\star$ by switching from heterostructures A to heterostructures B and C [1]. Note, that the integration regimes differ for spin and charge qubits due to the different experimental setups and operation speeds [43, 50]. For potential spin qubits in heterostructure A the calculated $T_2^\star$ shows an average $\overline{T}_2^\star = 8.4 \pm 5.6$ µs. This distribution compares well with the distribution $\overline{T}_2^\star = 6.7 \pm 5.6$ µs of experimental $T_2^\star$ data from state-of-the-art semiconductor spin qubits in materials with similar stacks as in heterostructure A[6, 10]. Note that while such comparisons oversimplify actual semiconductor spin-qubit devices by reducing them to a single number, they fulfill two aims. They allow us to benchmark the

[1] One order is gained from the reduced charge noise amplitude and another order is gained through a more beneficial noise exponent $\alpha > 1$.

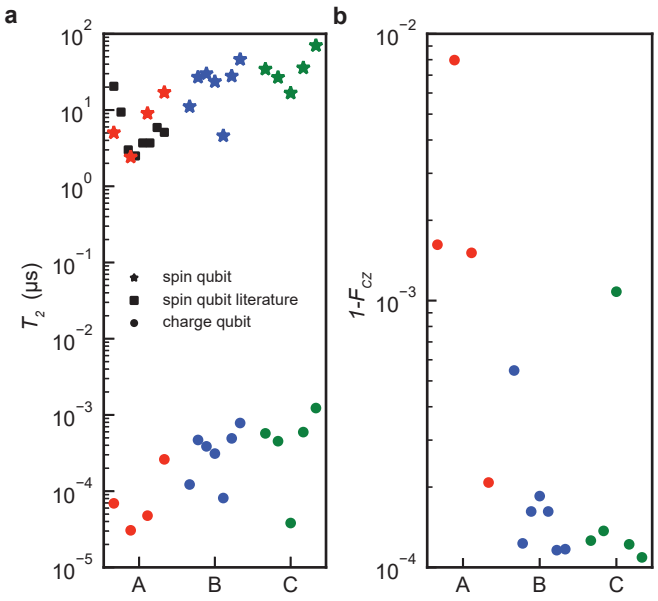


Figure 5.4: **a** Computed dephasing times $T_2^\star$ of a charge qubit (circle) and a spin-qubit (star) using $S_{\epsilon,min}$ from heterostructure A (red), B (blue), C (green). Eq. (5.1) was used to compute $T_2^\star$ as a function of S_ϵ and α from Fig. 5.3 with frequency cutoffs (f_{min}, f_{max}) = (1.6 mHz, 33 GHz) and (f_{min}, f_{max}) = (1.6 mHz, 10 kHz). Literature values (squares) are taken from Refs. [6, 10]. **b** Simulated infidelity of a CZ-gate between two spin qubits following the Ref. [6] using S_ϵ and α from heterostructure A (red), B (blue), C (green) in Fig. 5.3 as input for barrier fluctuations.

computed performance of heterostructure A to past experiments and provide a prognosis on the qubit quality in novel material stacks. Heterostructures B and C, in this case, may support average dephasing times of $\overline{T}_2^\star$ = 24.3 ± 12.5 µs and $\overline{T}_2^\star$ = 36.7 ± 18 µs, respectively. The highest values $T_2^\star$ = 70.1 µs hints towards a long spin qubit dephasing times previously only reported in Ref. [2].

Figure 5.4b shows the simulated infidelity, a metric to measure the closeness to the ideal operation, of a universal CZ-gate between two spin qubits following Ref. [6] and Section 5 in the Supplementary Information. Note, that the device used in Ref. [6] has the same architecture as our test devices. In the CZ-gate simulation, noise dominantly couples in via barrier voltage fluctuations which affect the interaction between the electron spins. Again, we assume the charge noise amplitude and exponents measured in our quantum dot experiments as input for the simulations. The simulations show an averaged average gate infidelity $1 - \overline{F}_{CZ}$ = 0.02 ± 0.01 % which means on average a single error every 5000 runs. We also observe a saturation value close to $1 - F = 10^{-4}$ which arises from single-qubit dephasing $T_2^\star$ = 20 µs used in the simulations estimated from nuclear spin noise due to an 800 ppm concentration of the ^{29}Si silicon isotope which has a non-zero nuclear spin [43].

5.2.6. DISCUSSION

In summary, we have measured electron transport and charge noise in ^{28}Si/SiGe heterostructures where we improve the semiconductor/dielectric interface, by adopting an amorphous Si-rich passivation and the structural quality of the quantum well, by reducing the quantum well thickness significantly below the Matthew-Blakeslee critical thickness for strain relaxation. We relate disorder in 2D to charge noise in quantum dots by following a statistical approach to measurements. A reduction of remote impurities and dislocations nearby the quantum well is connected with the key improvements in the scattering properties of the 2D electron gas, such as mobility and percolation density, and their uniformity across a 100 mm wafer. The trend observed from electron transport in 2D is compatible with the observations from measurements of charge noise in quantum dots. As remote impurities are reduced, charge noise becomes more sensitive to local fluctuators nearby the quantum well and less subject to screening by an increased number of electrons in the dot. Furthermore, with this materials optimization, we achieve a statistical improvement of nearly one order of magnitude in the charge noise supported by quantum dots. Using the charge noise distribution as an input parameter and benchmarking against published spin-qubit data, we predict that our optimized semiconductor host could support long-lived and high-fidelity spin qubits. We envisage that further materials improvements in the structural quality of the quantum well, in addition to the commonly considered semiconductor/dielectric interface, may lead systematically to quantum dots with less noise and to better qubit performance.

5

5.3. METHODS

Si/SiGe heterostructure growth. The ^{28}Si/SiGe heterostructures are grown on a 100-mm n-type Si(001) substrate using an Epsilon 2000 (ASMI) reduced-pressure chemical vapor deposition reactor. The reactor is equipped with a $^{28}SiH_4$ gas cylinder (1% dilution in H_2) for the growth of isotopically enriched ^{28}Si. The $^{28}SiH_4$ gas was obtained by reducing $^{28}SiF_4$ with a residual ^{29}Si concentration of 0.08%[51]. Starting from the Si substrate, the layer sequence of all heterostructures comprises a 3 µm step-graded $Si_{(1-x)}Ge_x$ layer with a final Ge concentration of $x = 0.3$ achieved in four grading steps ($x = 0.07$, 0.14, 0.21, and 0.3), followed by a 2.4 µm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer. The heterostructures differ for the active layers on top of the strain-relaxed buffer. Heterostructure A has a 9 nm tensile strained ^{28}Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial 1 nm epitaxial Si cap. Heterostructure B has an 9 nm tensile strained ^{28}Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial passivated Si cap grown at 500 °C. Heterostructure C has a 5 nm tensile strained ^{28}Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial passivated Si cap grown at 500 °C. A typical secondary ions mass spectrometry of our heterostructures is reported in Fig. S13 of [39], and the Ge concentration in the SiGe layers is confirmed by quantitative electron energy loss spectroscopy (EELS).

Device fabrication. The fabrication process for Hall-bar shaped heterostructure field effect transistors (H-FETs) involves: reactive ion etching of mesa-trench to isolate the two-dimensional electron gas; P-ion implantation and activation by rapid thermal annealing at 700 °C; atomic layer deposition of a 10-nm-thick Al_2O_3 gate oxide; deposition of thick dielectric pads to protect gate oxide during subsequent wire bonding step; sputtering of Al gate; electron beam evaporation of Ti:Pt to create ohmic contacts to the two-dimensional electron gas via doped areas. All patterning is done by optical lithography. Double quantum dot devices are fabricated on wafer coupons from the same H-FET fabrication run and share the process steps listed above. Double-quantum dot devices feature a single-layer gate metallization and further require electron beam lithography, evaporation of Al (27 nm) or Ti:Pd (3:27 nm) thin film metal gate, lift-off, and the global top-gate layer.

Electrical characterization of H-FETs. Hall-bar H-FETs measurements are performed in an attoDRY2100 variable temperature insert refrigerator at a base temperature of 1.7 K[32]. We apply a source-drain bias of 100 µV and measure the source-drain current I_{SD}, the longitudinal voltage V_{xx}, and the transverse Hall voltage V_{xy} as function of the top gate voltage V_g and the external perpendicular magnetic field B. From here we calculate the longitudinal resistivity ρ_{xx} and transverse Hall resistivity ρ_{xy}. The Hall electron density n is

obtained from the linear relationship $\rho_{xy} = B/en$ at low magnetic fields. The carrier mobility μ is extracted from the relationship $\sigma_{xx} = ne\mu$, where e is the electron charge. The percolation density n_p is extracted by fitting the longitudinal conductivity σ_{xx} to the relation $\sigma_{xx} \propto (n - n_p)^{1.31}$. Here σ_{xx} is obtained via tensor inversion of ρ_{xx} at $B = 0$. The box plots in Figs. 5.3a,b for heterostructure A (red) and B (blue) expand previously published data in Figs. 2f,e of Ref. [32] by considering measurements of 4 additional H-FETs for heterostructure A (20 H-FETs in total) and of 2 additional H-FETs for heterostructure B (16 H-FETs in total).

Electrical characterization of quantum dots. Measurements of the multi-electron quantum dots defined in the charge sensor are performed in a Leiden cryogenic dilution refrigerator with a mixing chamber base temperature $T_{\mathrm{MC}} = 50$ mK[39]. The devices are tuned systematically with the following procedure. We sweep all gate voltages (V_{SDRAcc}, V_{SDRB}, V_P, V_{SDLB}, and V_{SDLAcc}) from 0 V towards more positive bias, until a source-drain current I_{SD} of ≈ 1 nA is measured, indicating that a conductive channel has formed in the device. We then reduce the barrier voltages to find the pinch-off voltages for each barrier. Subsequently, we measure I_{SD} as a function of V_{SDLB} and V_{SDRB} and from this 2D map we find a set of gate voltage parameters so that Coulomb blockade peaks are visible. We then fix the barrier voltages and sweep V_P to count how many clearly defined Coulomb peaks are observed before onset of a background current. The quantum dot is tuned to show at least 9 Coulomb peaks, so that noise spectra may be fitted as in Fig. 5.2d with meaningful error bars. If we see less than 9 Coulomb peaks we readjust the accumulation gate voltages V_{SDRAcc}, and V_{SDLAcc}, and repeat the 2D scan of V_{SDLB} against V_{SDRB}. In one case (device 2 of heterostructure A), we tuned device to show past 5 Coulomb peaks and still performed the fit of the charge noise spectra similar to the one shown in Fig. 5.2d. Further details on the extraction of the lever arms and operation gate voltages of the devices are provided in Supplementary Figs 4,5. We estimate an electron temperature of 190 mK by fitting Coulomb blockade peaks (see Supplementary Fig. 2 in Ref. [32]) measured on quantum dot devices.

For heterostructure A, we apply a source drain bias of 100 μV (1 device) or 150 μV (3 devices) across the quantum dot, finite gate voltages across the operation gates of the dot, and finite gate voltages across the screening gates. We measure the current I_{SD} and the current noise spectrum S_I on the left side of the Coulomb peak where $|dI/dV_P|$ is the largest. We use a sampling rate of 1 kHz for 1 minute using a Keithley DMM6500 multimeter. The spectra are then divided into 10 segments of equal length, and we use a Fourier transform to convert from time-domain to frequency-domain for a frequency range of 167 mHz-500 Hz. We set the upper limit of the frequency spectra at 10 Hz, to avoid influences from a broad peak at around 150 Hz coming from the setup (Supplementary Fig. 3). A peak in the power spectral density at 9 Hz is removed from the analysis since it is an artifact of the pre-amplifier. To convert the current noise spectrum to a charge noise spectrum, we use the formula

$$S_\epsilon = \frac{aS_I}{|dI/dV_P|^2} \tag{5.3}$$

where a is the lever arm and $|dI/dV_P|$ is the slope of Coulomb peak around the center of the Coulomb peak.

For heterostructures B and C we apply a source drain bias of 150 μV across the quantum dot, finite gate voltages across the operation gates of the quantum dot, and we apply 0 V to all other gates. We measure the current I_{SD} and the current noise spectrum S_I on the left side of the Coulomb peak where $|dI/dV_P|$ is the largest. We use a sampling rate of 1 kHz for 10 minutes using a Keithley DMM6500 multimeter. The spectra are then divided into 15 segments of equal length, and we use a Fourier transform to convert from time-domain to frequency-domain for a frequency range of 25 mHz-500 Hz. We set the upper limit of the frequency spectra at 10 Hz, to avoid influences from a broad peak at around 150 Hz coming from the setup. We use Eq. 5.3 to convert the current noise spectrum to a charge noise spectrum.

(Scanning) Transmission Electron Microscopy. For structural characterization with (S)TEM, we prepared cross-sections of the quantum well heterostructures by using a Focused Ion Beam (Helios 600 dual beam microscope). HR-TEM micrographs were acquired in a TECNAI F20 microscope operated at 200 kV. Atomically resolved HAADF STEM data was acquired in a probe corrected TITAN microscope operated at 300 kV. EELS mapping was carried out in a TECNAI F20 microscope operated at 200 kV with approximately 2 eV energy resolution and 1 eV energy dispersion. Principal Component Analysis (PCA) was applied to the spectrum images to enhance S/N ratio.

5.4. SUPPLEMENTARY

To avoid possible errors associated with calibration, we measure the thickness of the Si layer in the quantum wells (t_{qw}) for heterostructures B and C by considering the interplanar spacing of the horizontal planes (002) of the quantum well (d_{qw}) and of the underlying the strain-relaxed SiGe buffer layer (d_{buffer}). For the $Si_{1-x}Ge_x$ buffer layer, we consider the stoichiometry x as measured by means of quantitative EELS and calculate the theoretical expected cell parameter a_{cell} using the following approximation of Vegard's law:

$$a_{cell} = a_{Si} + 0.2x + 0.027x^2, \tag{5.4}$$

where a_{Si} = 5.431 Å is the cell parameter of the diamond cubic Si crystal phase. To calculate d_{buff} we use the formula for the interplanar distance of the desired plane (002) of a diamond cubic system:

$$d_{hkl} = \frac{a_{cell}}{\sqrt{h^2+k^2+l^2}} = \frac{a_{cell}}{\sqrt{0^2+0^2+2^2}} = \frac{a_{cell}}{2}. \tag{5.5}$$

5

Since the quantum well is strained, d_{qw} is found by considering the average dilatation δ of the quantum well (002) planes with respect the (002) planes of the buffer. The dilatation δ is obtained experimentally by Geometrical Phase Analysis (GPA). The standard deviation of GPA is high for dilatation close to 0, as happens with the (220) epitaxial planes, for which the method is not the preferred choice. Nevertheless, for the larger dilatation of the (002) planes, the relatively smaller standard deviation makes the measurement significative. As a result, d_{qw} is computed by:

$$d_{qw} = d_{buff}(1+\delta). \tag{5.6}$$

Finally, the thickness of the quantum well is given by:

$$t_{qw} = n_{qw} d_{qw}, \tag{5.7}$$

where we count the number of planes forming the quantum well (n_{qw}) and multiply by d_{qw}. Therefore, the expected uncertainty of the thickness measurement lies in whether the initial and last plane of the well are being considered or not, *i.e.* the standard deviation is given by $\sigma = 2d_{qw}$.

With this in mind, for heterostructure B, where $x = 0.31$, four different measurements counting the (002) planes were performed in different regions of the quantum well, n_{qw} = 33 (3 times) and 34. With an average experimental δ of -1.6±0.2 %, we obtain $d_{qw} = 2.704 \pm 0.007$ Å, resulting in an average thickness $t_{qw} = 9.0 \pm 0.5$ nm.

For heterostructure C, x = 0.31 and two measurements counting the (002) planes were performed, n_{qw} = 19 and 20. With an average experimental δ of -1.7±0.5 %, we obtain $d_{qw} = 2.701 \pm 0.014$ Å, resulting in an average thickness $t_{qw} = 5.3 \pm 0.5$ nm.

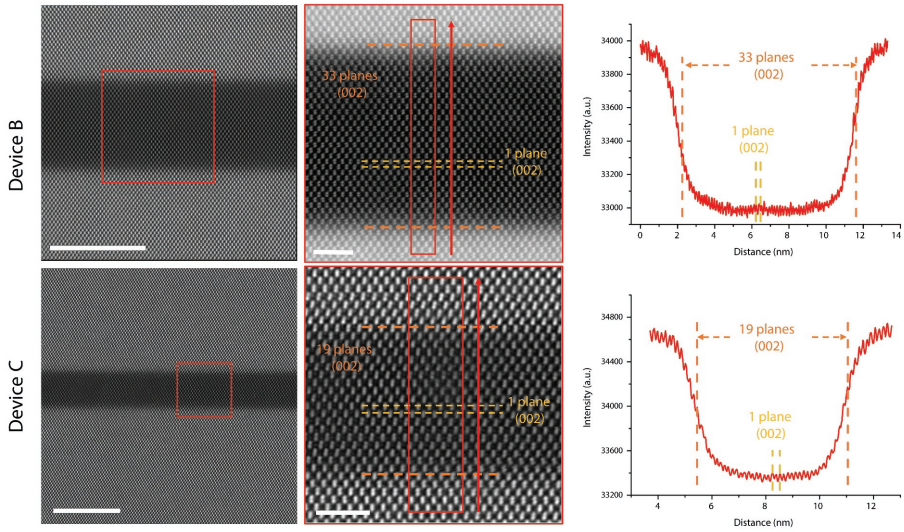


Figure 5.5: Method for computing the thickness of the quantum well based on the counting of the (002) horizontal planes, which reduces the uncertainty and bias associated to properly detecting the margins of the quantum well, for both heterostructures B and C. Scale bars of the images in the left column stand for 10 nm, while the zoom-ins in the middle column are 2 nm

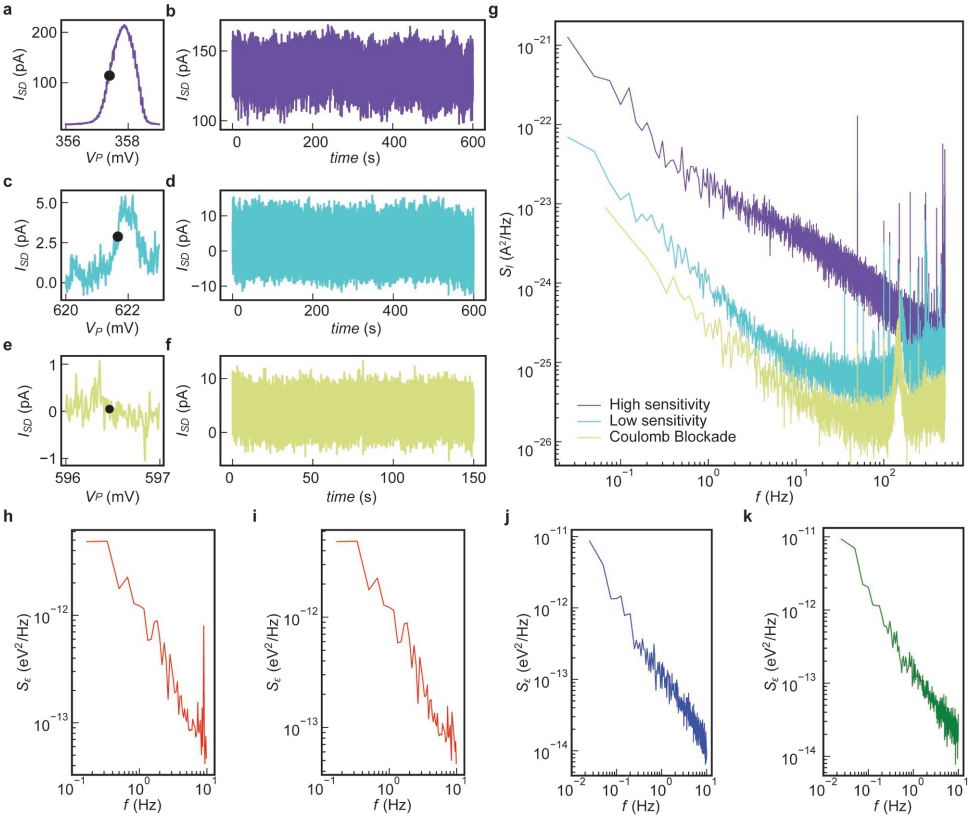


Figure 5.6: Comparison, for illustration purposes, of charge noise measurements spectra under different conditions. **a** Coulomb peak with large derivative dI_{SD}/dV_P and **b** time-resolved I_{SD} measured at the flank of the Coulomb peak (dot in **a**). Measurements are from a device from heterostructure C. **c** Coulomb peak with smaller derivative dI_{SD}/dV_P and **d** time-resolved I_{SD} measured at the flank of the Coulomb peak (dot in **c**). Measurements are from a device from heterostructure B. **c** Coulomb blockade and **d** time-resolved I_{SD} measured on a test device from heterostructure B, indicative of the noise floor of our measurement setup. The time traces in **b**,**d**,**f** show a consistent decrease in the noise bandwidth going from the most sensitive ($\Delta I_{SD} \simeq 50$ pA in **b**) to the less sensitive ($\Delta I_{SD} \simeq 10$ pA in **f**) configuration. **g** Comparison of the current noise spectrum under different sensitivity conditions. Purple (high sensitivity), cyan (low-sensitivity), and lemon (noise floor) curves show $S_I(f)$ obtained from measurements in **b**, **d**, and **f**, respectively. Lemon and cyan curves show a broad interference peak at 150 Hz, as well as a flattening out of the curve at ≈40 Hz. **h** Charge noise measurement of heterostructure A with an interference peak at 9 Hz arising from the measurement module. In **i** we remove the interference peak from the analysis. **j**,**k** Charge noise of a device from heterostructure B and C, respectively, measured with a different measurement module compared to **j** showing no interference peak.

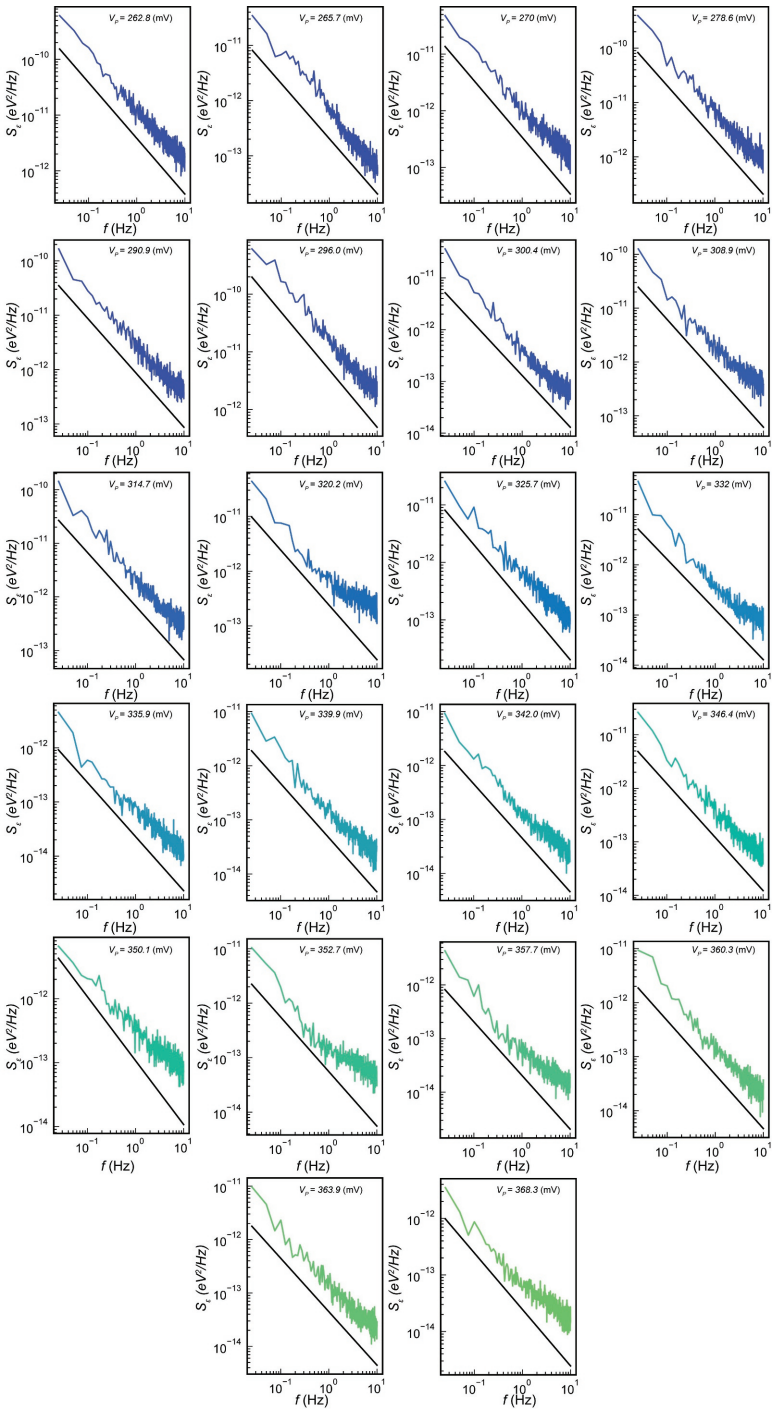


Figure 5.7: Charge noise spectra $S_\epsilon(f)$ at different plunger gate voltage V_P from a quantum dot from heterostructure C. The same data is plotted in Fig. 2d in three dimensions. The black trendline shows a $1/f$ dependence.

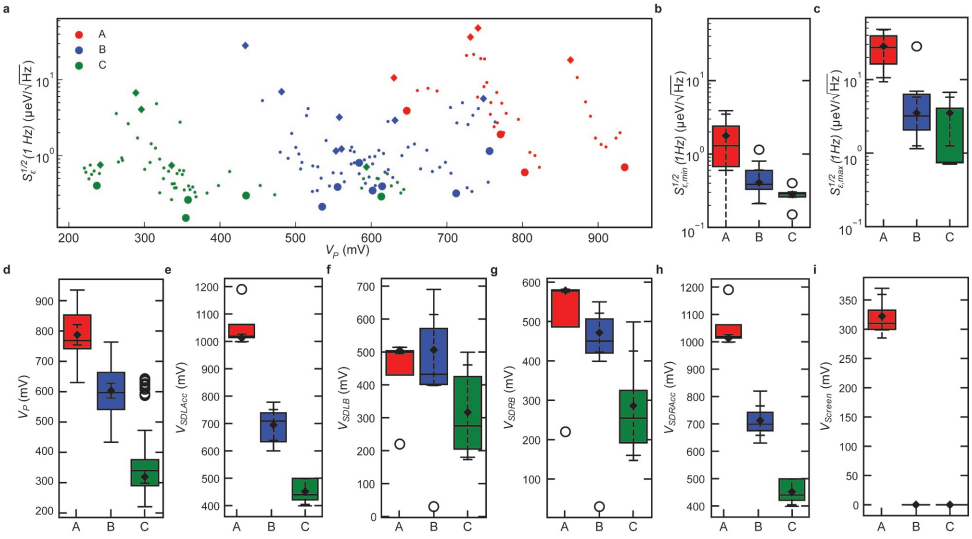


Figure 5.8: **a** Charge noise $S_\epsilon^{1/2}$ at 1 Hz as a function of the plunger gate voltage V_P for all measured devices of heterostructure A (red), B (blue), and C (green). Circles and diamonds highlight, respectively, the minimum ($S_{\epsilon,min}$) and maximum ($S_{\epsilon,max}$ charge noise at 1 Hz for each device upon varying V_P. For a given heterostructure, these $S_{\epsilon,min}$ and $S_{\epsilon,max}$ values build up the distributions plotted, respectively, in b (Fig. 2e main text) and c. The trend of charge noise improvement from A to B and C is observed both for $S_{E,min}$ and $S_{E,max}$. $S_{E,min}$ varies less than $S_{E,max}$ between different devices for a given heterostructure since $S_{E,max}$ is more affected by device-specific effects such as geometry of wave-function, screening, and the exact electron number on the island. Because we do not know the exact electron number, we believe that $S_{E,min}$ is more suited to compare the different heterostructures. **d-i** Distributions of the operation gate voltages of the plunger, SDLAcc, SDLB, SDRB, SDRAcc, and screening gates, respectively (see Fig. 1**f** in the main text) for heterostructure A (red, 4 devices measured), B (blue, 8 devices measured), and C (green, 5 devices measured). With the exception of gate SDLB, all operation voltages of the charge sensor are highest in heterostructure A and lowest in heterostructure C with a difference of up to 600 mV. Note that a global screening gate is only used for the operation of heterostructure A. Quartile box plots, mode (horizontal line), means (diamonds), 99% confidence intervals of the mean (dashed whiskers), and outliers (circles) are shown.

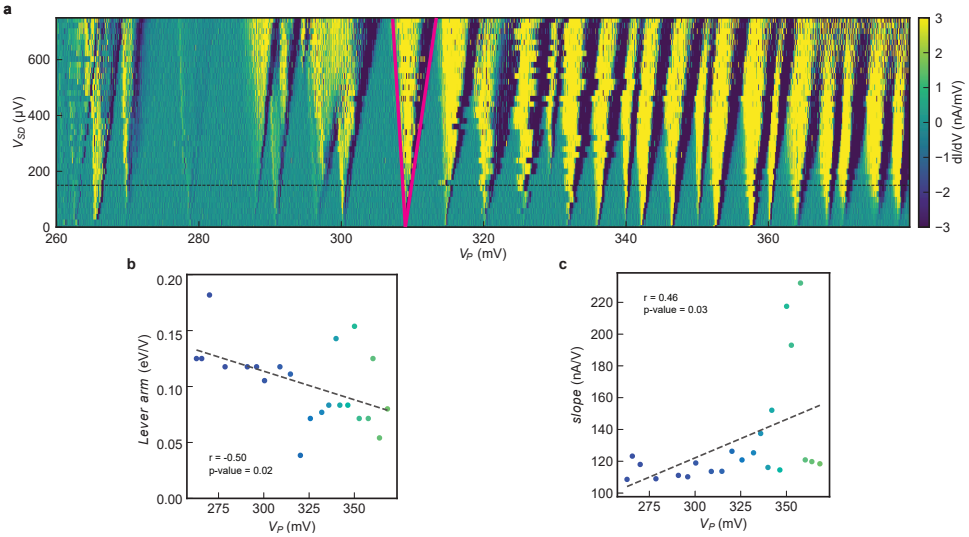


Figure 5.9: **a** Differential conductance (dI/dV) showing representative Coulomb blockade diamonds as a function of the source-drain voltage (V_{SD}) and plunger gate voltage (V_P) for heterostructure C. We derive the two slopes m_S and m_D on both sides of each Coulomb diamond. Using the equation $a = |\frac{m_S m_D}{m_S - m_D}|$, we extract a lever arm of $a = 0.12$ eV/V for the Coulomb peak at $V_P \approx 308$ mV, where we indicate m_S and m_D with magenta lines. The dashed line indicates the source-drain voltage ($V_{SD} = 150$ (μV)) used for the charge noise measurements. **b** Lever arm and **c** slope at the flank of the Coulomb peak for the peaks reported in **a**. We calculate the Pearson correlation coefficient (r), measuring the linear correlation between the two parameters. It varies between -1 and 1, with 0 implying no correlation. We also calculate the p-value of the null hypothesis, i.e., $r = 0$. We remember that the p-value indicates the probability of an uncorrelated system producing datasets that have a Pearson correlation at least as extreme as the one computed from these datasets. We remember that a p-value greater than 0.05 is considered not statistically relevant.

BIBLIOGRAPHY

[1] Lieven M. K. Vandersypen and Mark A. Eriksson. "Quantum computing with semiconductor spins". In: *Physics Today* 72.8 (Aug. 2019), pp. 38–45. ISSN: 0031-9228. DOI: 10.1063/PT.3.4270.

[2] M. Veldhorst et al. "A two-qubit logic gate in silicon". In: *Nature* 526.7573 (Oct. 2015), pp. 410–414. ISSN: 0028-0836. DOI: 10.1038/nature15263.

[3] Peter Stano and Daniel Loss. "Review of performance metrics of spin qubits in gated semiconducting nanostructures". en. In: *Nature Reviews Physics* (Aug. 2022). ISSN: 2522-5820. DOI: 10.1038/s42254-022-00484-w. URL: https://www.nature.com/articles/s42254-022-00484-w (visited on 09/01/2022).

[4] A. M. J. Zwerver et al. "Qubits made by advanced semiconductor manufacturing". In: *Nature Electronics* 5.3 (Mar. 2022), pp. 184–190. ISSN: 2520-1131. DOI: 10.1038/s41928-022-00727-9.

[5] T F Watson et al. "A programmable two-qubit quantum processor in silicon". In: *Nature* 555.7698 (2018), pp. 633–637. ISSN: 14764687. DOI: 10.1038/nature25766. URL: http://dx.doi.org/10.1038/nature25766.

[6] Xiao Xue et al. "Quantum logic with spin qubits crossing the surface code threshold". In: *Nature* 601.7893 (Jan. 2022), pp. 343–347. ISSN: 0028-0836. DOI: 10.1038/s41586-021-04273-w.

[7] Akito Noiri et al. "Fast universal quantum gate above the fault-tolerance threshold in silicon". In: *Nature* 601.7893 (Jan. 2022), pp. 338–342. ISSN: 0028-0836. DOI: 10.1038/s41586-021-04182-y.

[8] Mateusz T. Madzik et al. "Precision tomography of a three-qubit donor quantum processor in silicon". In: *Nature* 601.7893 (Jan. 2022), pp. 348–353. ISSN: 0028-0836. DOI: 10.1038/s41586-021-04292-7.

[9] Adam R. Mills et al. "Two-qubit silicon quantum processor with operation fidelity exceeding 99%". en. In: *Science Advances* 8.14 (Apr. 2022), eabn5130. ISSN: 2375-2548. DOI: 10.1126/sciadv.abn5130. URL: https://www.science.org/doi/10.1126/sciadv.abn5130 (visited on 08/16/2022).

[10] Stephan G. J. Philips et al. "Universal control of a six-qubit quantum processor in silicon". In: *Preprint at http://arxiv.org/abs/2202.09252* (Feb. 2022). URL: http://arxiv.org/abs/2202.09252.

[11] N Samkharadze et al. "Strong spin-photon coupling in silicon". In: *Science* 359.6380 (2018), pp. 1123–1127. ISSN: 10959203. DOI: 10.1126/science.aar4054.

[12] D. M. Zajac et al. "Resonantly driven CNOT gate for electron spins". In: *Science* 359.6374 (2018), pp. 439–442. ISSN: 10959203. DOI: 10.1126/science.aao5965.

[13] F. Borjans et al. “Resonant microwave-mediated interactions between distant electron spins”. en. In: *Nature* 577.7789 (Jan. 2020), pp. 195–198. ISSN: 1476-4687. DOI: 10.1038/s41586-019-1867-y. URL: https://www.nature.com/articles/s41586-019-1867-y (visited on 08/30/2022).

[14] Patrick Harvey-Collard et al. “Coherent Spin-Spin Coupling Mediated by Virtual Microwave Photons”. In: *Physical Review X* 12.2 (2022), p. 021026. DOI: 10.1103/PhysRevX.12.021026.

[15] J. Yoneda et al. “Coherent spin qubit transport in silicon”. en. In: *Nature Communications* 12.1 (July 2021), p. 4114. ISSN: 2041-1723. DOI: 10.1038/s41467-021-24371-7. URL: https://www.nature.com/articles/s41467-021-24371-7 (visited on 09/01/2022).

[16] Akito Noiri et al. “A Shuttling-Based Two-Qubit Logic Gate for Linking Distant Silicon Quantum Processors”. In: *Preprint at http://arXiv:2202.01357* (2022). URL: http://arxiv.org/abs/2202.01357.

[17] L. M. K. Vandersypen et al. “Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent”. In: *npj Quantum Information* 3.1 (2017), p. 34. DOI: 10.1038/s41534-017-0038-y.

[18] Jun Yoneda et al. “A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%”. In: *Nature Nanotechnology* 13.2 (2018), pp. 102–106. ISSN: 17483395. DOI: 10 . 1038 / s41565 - 017 - 0014 - x. URL: http://dx.doi.org/10.1038/s41565-017-0014-x.

[19] E Paladino et al. “1/f noise: Implications for solid-state quantum information”. In: *Reviews of Modern Physics* 86.2 (2014), p. 361.

[20] Elliot J Connors et al. “Low-frequency charge noise in Si/SiGe quantum dots”. In: *Physical Review B* 100.16 (2019), p. 165305.

[21] Elliot J. Connors et al. “Charge-noise spectroscopy of Si/SiGe quantum dots via dynamically-decoupled exchange oscillations”. en. In: *Nature Communications* 13.1 (Dec. 2022), p. 940. ISSN: 2041-1723. DOI: 10.1038/s41467-022-28519-x. URL: https://www.nature.com/articles/s41467-022-28519-x (visited on 08/12/2022).

[22] Dimitrie Culcer, Xuedong Hu, and S. Das Sarma. “Dephasing of Si spin qubits due to charge noise”. In: *Applied Physics Letters* 95.7 (Aug. 2009), p. 073102. ISSN: 0003-6951. DOI: 10.1063/1.3194778.

[23] C. Dekker et al. “Spontaneous resistance switching and low-frequency noise in quantum point contacts”. In: *Physical Review Letters* 66.16 (Apr. 1991), pp. 2148–2151. ISSN: 0031-9007. DOI: 10.1103/PhysRevLett.66.2148.

[24] T. Sakamoto, Y. Nakamura, and K. Nakamura. “Distributions of single-carrier traps in GaAs/Al _x Ga _{1- x} As heterostructures”. In: *Applied Physics Letters* 67.15 (Oct. 1995), pp. 2220–2222. ISSN: 0003-6951. DOI: 10.1063/1.115109.

[25] F Liefrink, J I Dijkhuis, and H van Houten. “Low-frequency noise in quantum point contacts”. In: *Semiconductor Science and Technology* 9.12 (Dec. 1994), pp. 2178–2189. ISSN: 0268-1242. DOI: 10.1088/0268-1242/9/12/003.

[26] Guy Ramon and Xuedong Hu. “Decoherence of spin qubits due to a nearby charge fluctuator in gate-defined double dots”. In: *Physical Review B* 81.4 (Jan. 2010), p. 045304. ISSN: 1098-0121. DOI: 10.1103/PhysRevB.81.045304.

[27] W.-C. Hua et al. “Threading dislocation induced low frequency noise in strained-Si nMOSFETs”. In: *IEEE Electron Device Letters* 26.9 (Sept. 2005), pp. 667–669. ISSN: 0741-3106. DOI: 10.1109/LED.2005.853672.

[28] M.H. Lee et al. “Comprehensive low-frequency and RF noise characteristics in strained-Si NMOSFETs”. In: *IEEE International Electron Devices Meeting 2003*. Dec. 2003, pp. 3.6.1–3.6.4. DOI: 10.1109/IEDM.2003.1269168.

[29] E. Simoen et al. “Processing aspects in the low-frequency noise of nMOSFETs on strained-silicon substrates”. In: *IEEE Transactions on Electron Devices* 53.5 (May 2006), pp. 1039–1047. ISSN: 0018-9383. DOI: 10.1109/TED.2006.871859.

[30] Don Monroe. “Comparison of mobility-limiting mechanisms in high-mobility Si1-xGex heterostructures”. In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 11.4 (1993), p. 1731. ISSN: 0734211X. DOI: 10.1116/1.586471.

[31] Xiao Xue et al. “CMOS-based cryogenic control of silicon quantum circuits”. In: *Nature* 593 (7858 May 2021), pp. 205–210. ISSN: 0028-0836. DOI: 10.1038/s41586-021-03469-4.

[32] Davide Degli Esposti et al. “Wafer-scale low-disorder 2DEG in 28Si/SiGe without an epitaxial Si cap”. en. In: *Applied Physics Letters* 120.18 (May 2022), p. 184003. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0088576. URL: https://pubs.aip.org/apl/article/120/18/184003/2833621/Wafer-scale-low-disorder-2DEG-in-28Si-SiGe-without (visited on 07/10/2023).

[33] J W Matthews and A E Blakeslee. “Defects in epitaxial multilayers: I. Misfit dislocations”. In: *Journal of Crystal growth* 27 (1974), pp. 118–125.

[34] R. People and J. C. Bean. “Calculation of critical layer thickness versus lattice mismatch for GexSi1-x/Si strained-layer heterostructures”. In: *Applied Physics Letters* 47.3 (Aug. 1985), pp. 322–324. ISSN: 0003-6951. DOI: 10.1063/1.96206. URL: https://aip.scitation.org/doi/10.1063/1.96206 (visited on 08/31/2022).

[35] K. Ismail. “Effect of dislocations in strained Si/SiGe on electron mobility”. In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 14.4 (July 1996), p. 2776. ISSN: 0734211X. DOI: 10.1116/1.588831.

[36] B. Paquelet Wuetz et al. “Multiplexed quantum transport using commercial off-the-shelf CMOS at sub-kelvin temperatures”. In: *npj Quantum Information* 6.6 (May 2020), p. 43. ISSN: 2056-6387. DOI: 10.1038/s41534-020-0274-4. URL: https://www.nature.com/articles/s41534-020-0274-4 (visited on 12/21/2021).

[37] L. A. Tracy et al. “Observation of percolation-induced two-dimensional metal-insulator transition in a Si MOSFET”. In: *Physical Review B* 79.23 (June 2009), p. 235307. DOI: 10.1103/PhysRevB.79.235307. URL: https://link.aps.org/doi/10.1103/PhysRevB.79.235307 (visited on 05/27/2020).

[38] K. Ismail et al. “Identification of a Mobility-Limiting Scattering Mechanism in Modulation-Doped Si/SiGe Heterostructures”. In: *Physical Review Letters* 73.25 (Dec. 1994), pp. 3447–3450. ISSN: 0031-9007. DOI: 10.1103/PhysRevLett.73.3447.

[39] B. Paquelet Wuetz et al. “Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots”. In: *Preprint at http://arxiv.org/abs/2112.09606* (2021). URL: http://arxiv.org/abs/2112.09606 (visited on 08/16/2022).

[40] Sh. Kogan. *Electronic Noise and Fluctuations in Solids*. Cambridge University Press, Aug. 1996. ISBN: 9780521460347. DOI: 10.1017/CBO9780511551666.

[41] Seongjin Ahn, S Das Sarma, and J P Kestner. “Microscopic bath effects on noise spectra in semiconductor quantum dot qubits”. In: *Physical Review B* 103.4 (2021), p. L041304. URL: https://link.aps.org/doi/10.1103/PhysRevB.103.L041304.

[42] Brandur Thorgrimsson et al. “Extending the coherence of a quantum dot hybrid qubit”. In: *npj Quantum Information* 3 (1 Dec. 2017), p. 32. ISSN: 2056-6387. DOI: 10.1038/s41534-017-0034-2.

[43] Tom Struck et al. “Low-frequency spin qubit energy splitting noise in highly purified 28Si/SiGe”. In: *npj Quantum Information* 6 (1 Dec. 2020), p. 40. ISSN: 2056-6387. DOI: 10.1038/s41534-020-0276-2.

[44] Mario Lodari et al. “Low percolation density and charge noise with holes in germanium”. In: *Materials for Quantum Technology* 1.1 (2021), p. 11002. URL: https://iopscience.iop.org/article/10.1088/2633-4356/abcd82.

[45] Blake M Freeman, Joshua S Schoenfield, and HongWen Jiang. “Comparison of low frequency charge noise in identically patterned Si/SiO2 and Si/SiGe quantum dots”. In: *Applied Physics Letters* 108.25 (2016), p. 253108. URL: http://aip.scitation.org/doi/10.1063/1.4954700.

[46] Felix Jekat et al. “Exfoliated hexagonal BN as gate dielectric for InSb nanowire quantum dots with improved gate hysteresis and charge noise”. en. In: *Applied Physics Letters* 116.25 (June 2020), p. 253101. ISSN: 0003-6951. DOI: 10.1063/5.0002112. URL: https://aip.scitation.org/doi/abs/10.1063/5.0002112 (visited on 07/07/2020).

[47] X Mi, S Kohler, and Jason R Petta. “Landau-Zener interferometry of valley-orbit states in Si/SiGe double quantum dots”. In: *Physical Review B* 98.16 (2018), p. 161404. URL: https://link.aps.org/doi/10.1103/PhysRevB.98.161404.

[48] J. Basset et al. “Evaluating charge noise acting on semiconductor quantum dots in the circuit quantum electrodynamics architecture”. In: *Applied Physics Letters* 105.6 (Aug. 2014), p. 063105. ISSN: 0003-6951. DOI: 10.1063/1.4892828. URL: https://aip.scitation.org/doi/10.1063/1.4892828 (visited on 06/10/2020).

[49] G. Ithier et al. “Decoherence in a superconducting quantum bit circuit”. In: *Physical Review B* 72 (13 Oct. 2005), p. 134519. ISSN: 1098-0121. DOI: 10.1103/PhysRevB.72.134519.

[50] E R MacQuarrie et al. “Progress toward a Capacitively Mediated CNOT between Two Charge Qubits in Si/SiGe”. In: *npj Quantum Information* 6 (2020), p. 81. ISSN: 2056-6387. DOI: 10.1038/s41534-020-00314-w.

[51] D. Sabbagh et al. “Quantum Transport Properties of Industrial 28Si/28Si O2”. In: *Physical Review Applied* 12.1 (July 2019), p. 014013. ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.12.014013.

6

LOW DISORDER AND HIGH VALLEY SPLITTING IN SILICON

The electrical characterisation of classical and quantum devices is a critical step in the development cycle of heterogeneous material stacks for semiconductor spin qubits. In the case of silicon, properties such as disorder and energy separation of conduction band valleys are commonly investigated individually upon modifications in selected parameters of the material stack. However, this reductionist approach fails to consider the interdependence between different structural and electronic properties at the danger of optimizing one metric at the expense of the others. Here, we achieve a significant improvement in both disorder and valley splitting by taking a co-design approach to the material stack. We demonstrate isotopically-purified, strained quantum wells with high mobility of $3.14(8) \times 10^5$ *cm*^{2}*/Vs and low percolation density of* $6.9(1) \times 10^{10}$ *cm*$^{-2}$*. These low disorder quantum wells support quantum dots with low charge noise of* $0.9(3)$ $\mu eV/Hz^{1/2}$ *and large mean valley splitting energy of* $0.24(7)$ *meV, measured in qubit devices. By striking the delicate balance between disorder, charge noise, and valley splitting, these findings provide a benchmark for silicon as a host semiconductor for quantum dot qubits. We foresee the application of these heterostructures in larger, high-performance quantum processors.*

This chapter has been published as: **Davide Degli Esposti**, Lucas E. A. Stehouwer, Önder Gül, Nodar Samkharadze, Corentin Déprez, Marcel Meyer, Ilja N. Meijer, Larysa Tryputen, Saurabh Karwal, Marc Botifoll, Jordi Arbiol, Sergey V. Amitonov, Lieven M. K. Vandersypen, Amir Sammak, Menno Veldhorst & Giordano Scappucci, "Low disorder and high valley splitting in silicon.", npj Quantum Information, **10**, 32 (2024).

6.1. INTRODUCTION

The development of fault-tolerant quantum computing hardware relies on significant advancements in the quality of quantum materials hosting qubits[1]. For spin qubits in gate-defined silicon quantum dots[2], there are currently three material-science driven requirements being pursued[3]. The first is to minimise potential fluctuations arising from static disorder in the host semiconductor, to ensure precise control of the charging energies and tunnel coupling between quantum dots, and to enable shared control in crossbar arrays[4]. The second requirement is to reduce the presence of two-level fluctuators and other sources of dynamic disorder responsible for charge noise, which currently limits qubit performance[5, 6]. Lastly, it is crucial to maximize the energy separation between the two low-lying conduction valleys[7]. Achieving large valley splitting energy prevents leakage outside the computational two-level Hilbert space and is essential to ensure high fidelity qubit initialization, readout, and control and shuttling[2, 8–12].

Satisfying these multiple requirements simultaneously is challenging because the constraints on material stack design and processing conditions may conflict. In gate-defined silicon quantum dots, single electron spins are confined either at the semiconductor-dielectric interface in metal-oxide-semiconductor (Si-MOS) stacks or in buried strained quantum wells at the hetero-epitaxial Si/SiGe interface. In Si-MOS, the large electric field at the interface between the semiconductor and the dielectric drives a large valley splitting energy in tightly confined quantum dots[13]. However, the proximity of the dielectric interface induces significant static and dynamic disorder, affecting mobility, percolation density, and charge noise[14]. The latter can be improved through careful optimisation of the multi-layer gate stack resorting to industrial fabrication processes[15].

In conventional Si/SiGe heterostructures, a strained Si quantum well is separated from the semiconductor-dielectric interface by an epitaxial SiGe barrier[3]. The buried Si quantum well naturally ensures a quiet environment, away from the impurities at the semiconductor-dielectric interface, leading to lower disorder and charge noise compared to Si-MOS[16–18]. However, strain and compositional fluctuations in the SiGe strain-relaxed buffer (SRB) below the quantum well result in band-structure variations and device non-uniformity[19]. Furthermore, valley splitting is limited and may vary from device to device[20–27] due to the weaker electric field compared to Si-MOS[28, 29] and the additional in-built random alloy composition fluctuations at the strained Si-SiGe hetero-interface[30], posing a challenge for device reliability and qubit operation.

Practical strategies have been recently considered to enhance valley splitting in Si/SiGe quantum wells[31], including the use of unconventional heterostructures that incorporate Ge to the interior[30, 32–34] or the boundary of the quantum well[35–37]. Without a co-design for high electron mobility, enhancing valley splitting, which requires breaking translation symmetry, tends to occur at the expense of a deteriorated disorder landscape, posing challenges for scaling to large qubit systems. Indeed, the few experimental reports[18, 34, 38] of large valley splitting (e.g. > 0.2 meV) in Si/SiGe quantum dots have shown relatively low mobility ($< 6 \times 10^4$ cm^2/Vs) of the parent two-dimensional electron gas, thereby spoiling one major advantage of Si/SiGe over Si-MOS. A large valley splitting up to 0.239 meV has been measured in quantum wells incorporat-

ing an oscillating Ge concentration[34]. However, the additional scattering from random alloy disorder yields an electron mobility of $2-3\times10^4$ cm^2/Vs. This mobility is significantly lower than what is obtained with conventional Si/SiGe heterostructures[39, 40] and is even comparable to the mobility in the best Si-MOS stacks[15]. Instances of large valley splittings (up to 0.286 ± 0.026 meV) within a wide distribution have also been measured in 3 nm ultra-thin quantum wells[41]. Likewise, ultra-thin quantum wells may degrade mobility due to increased scattering from random alloy disorder as the wave function penetrates deeper into the SiGe barrier[42], potentially compounded by interface roughness as well[43]. Conversely, very high mobility of 6.5×10^5 cm^2/Vs was reported in conventional Si/SiGe heterostructures although the quantum dots showed rather low valley splitting in the range of $35-70$ μeV[25].

In this work, we present significant advancements in isotopically purified ^{28}Si/SiGe heterostructures by conducting a study across multiple Hall bars and quantum dots in spin-qubit devices. We demonstrate simultaneous improvement in the channel static disorder, qualified by mobility and percolation density, and in the mean valley splitting while keeping respectable levels of low-frequency charge noise. These advancements are achieved without resorting to unconventional heterostructures. Instead, they result from explicitly accounting for the unavoidable broadening of Si-SiGe interfaces and optimising the quantum well thickness, while considering the design constraints imposed by the chemical composition of the SiGe buffer. Specifically, we ensure that the quantum well thickness is chosen to maintain coherent epitaxy of the strained Si layer with the underlying SiGe buffer while also minimising the impact of disorder originating from barrier penetration effects.

6.2. RESULTS

6.2.1. DESCRIPTION OF ^{28}SI/SIGE HETEROSTRUCTURES

The ^{28}Si/SiGe heterostructures are grown on a 100 mm Si(001) substrate by reduced-pressure chemical vapour deposition (Methods). From bottom to top (Fig. 6.1a), the heterostructure comprises a thick SiGe strained relaxed buffer (SRB) made of a step graded $Si_{1-x}Ge_x$ buffer layer with increasing Ge concentration followed by a SiGe layer with constant Ge concentration, a tensile-strained ^{28}Si quantum well, and a SiGe barrier passivated by an amorphous Si-rich layer[16]. Given the in-plane random distribution of Si and Ge at the interfaces between Si and SiGe layers, the description of a realistic Si quantum well may be reduced to the one-dimensional Ge concentration profile along the growth direction[30, 44]. This is modelled by sigmoidal interfaces[44] (Methods) as in Fig 6.1b and is characterised by three parameters: ρ_b is the asymptotic limit value of the maximum Ge concentration in the SiGe barriers surrounding the quantum well; 4τ is the interface width, which corresponds to the length over which the Ge concentration changes from 12% to 88% of ρ_b; w is the quantum well width defined as the distance between the inflexion points of the two interfaces. Our growth protocol yields a reproducible quantum well profile with $\rho_b = 0.31(1)$[30, 45], $4\tau \approx 1$ nm, and $w \approx 7$ nm (see Supplementary Figs. 1 and 2). The quantum well thickness was chosen on purpose to fall within the range of 5 nm to 9 nm, which correspond to the thicknesses of quantum wells studied in ref. [17] and used here as a benchmark. We expect a quantum well of

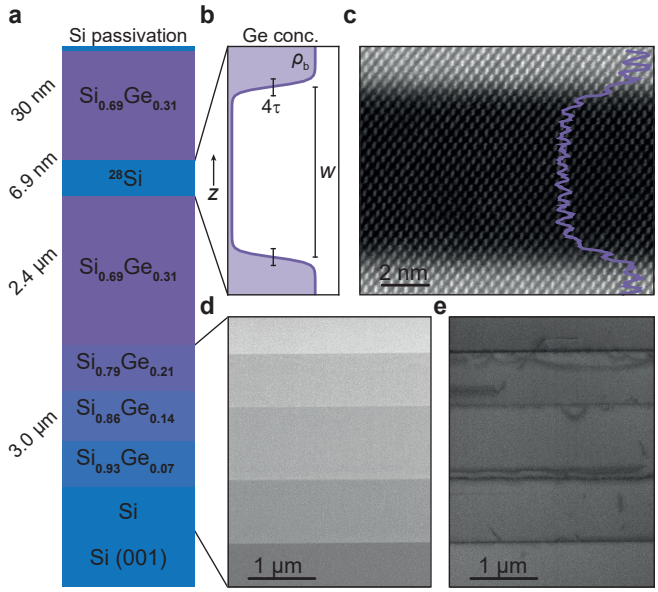


Figure 6.1: **Semiconductor material stack a** Schematic illustration of the ^{28}Si/SiGe heterostructure. z indicates the heterostructure growth direction. **b** Schematic Ge concentration profile defining a realistic Si quantum well, characterised by the final Ge concentration (ρ_b) in the SiGe barriers, the interface sharpness (4τ), and quantum well width (w). **c** Atomic resolution high angle annular dark field (HAADF) (Z-contrast) scanning transmission electron microscopy (STEM) image of the ^{28}Si quantum well with superimposed intensity profile used to count the number of crystallographic planes in the (002) direction forming the quantum well. **d**, **e** STEM images of the step-graded SiGe buffer layer below the quantum well acquired in HAADF (Z-contrast) and bright field mode, respectively.

6

about 7 nm to be thin enough to suppress strain-release defects and also increase the valley splitting compared to the results in ref [5, 30, 45, 46]. At the same time, the quantum well was chosen to be sufficiently thick to mitigate the effect of disorder arising from penetration of the wave function into the SiGe barrier[42] and possibly from the interface roughness[43].

Figure 6.1d shows aberration corrected (AC) atomic resolution high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) images and superimposed intensity profiles to validate the thickness of the ^{28}Si quantum well by counting the (002) horizontal planes as in ref. [17]. We estimate that the quantum well is formed by 26 atomic planes, corresponding to a thickness $w = 6.9 \pm 0.5$ nm (see Supplementary Fig. 1). Further electron microscopy characterisation of all quantum wells considered in this study highlights the robustness of our growth protocol (see Supplementary Fig. 2). Images in Fig. 6.1d,e, acquired in HAADF (Z-contrast) and bright field (BF) STEM modes, respectively, highlight two critical characteristics of the compositionally graded SiGe layers beneath the quantum well. Firstly, the step-wise increase of the Ge content corresponds clearly to the varying shades of contrast in Fig. 6.1d. Secondly, strain-release defects and dislocations in Fig. 6.1e are confined at the multiple and sharp interfaces within the compositionally graded buffer layer, highlighting the overall crys-

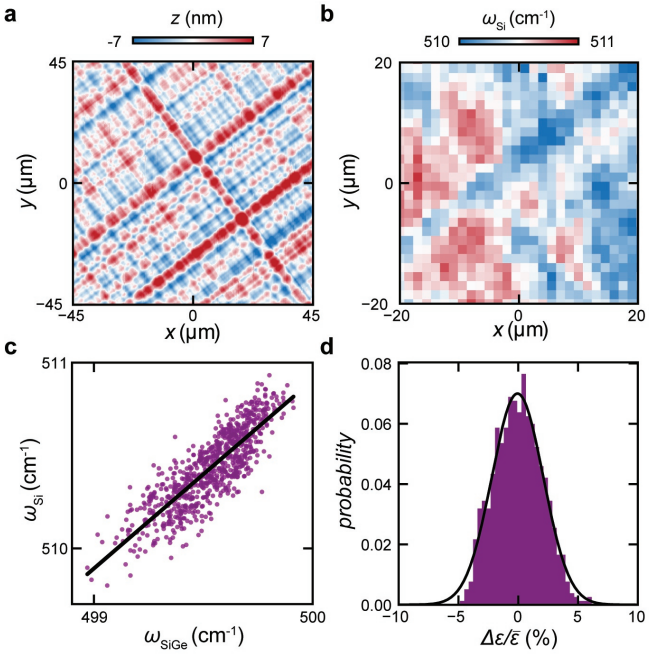


Figure 6.2: **Strain fluctuations measurements a** Atomic force microscopy image of the ^{28}Si/SiGe heterostructure taken with an alignment of about 45 degrees to the 110 crystallographic axis. **b** Raman shift map of the Si-Si vibration ω_{Si} from a strained Si quantum well with a thickness of 6.9(5) nm. The map was taken with an alignment of about 45 degrees to the 110 crystallographic axis. **c** Cross-correlation between ω_{Si} and the Si-Si vibration from the SiGe buffer (ω_{SiGe}) obtained by analysing Raman spectra over the same area mapped in **b** and linear fit (black line). **d** Relative in-plane strain distribution percentage of the Si quantum well $\Delta\epsilon/\bar{\epsilon}$, where $\bar{\epsilon} = 1.31(3)$ % is the mean value of strain in the Si quantum well. The solid line is a fit to a normal distribution.

talline quality of the SiGe SRB below the quantum well.

6.2.2. CHARACTERISATION OF STRAIN DISTRIBUTION

After confirming the quantum well thickness, we examine the coherence of the Si quantum well epitaxy with the underlying SiGe and quantify the in-plane strain (ϵ) of the quantum well, along with the amplitude ($\Delta\epsilon$) of its fluctuations. Following the approach in ref. [47], we employ scanning Raman spectroscopy on a heterostructure where the SiGe top barrier is intentionally omitted. Since this configuration maximises the signal from the thin strained Si quantum well, we are able to efficiently map the shift in Si-Si vibrations originating from both the Si quantum well (ω_{Si}) and from the SiGe buffer layer below (ω_{SiGe}) (see Supplementary Fig. 3). Fig. 6.2a shows an atomic-force microscopy image of a pristine grown ^{28}Si/SiGe heterostructure over an area of 90×90 μm^2. The surface is characterised by a root mean square (RMS) roughness of ≈ 2.4 nm and by the typical cross-hatch pattern arising from the misfit dislocation network within the SiGe SRB. The cross-hatch undulations have a characteristic wavelength of ≈ 5 μm estimated from the Fourier transform spectrum.

The Raman map in Fig. 6.2b tracks ω_{Si} over an area of 40 × 40 μm. This area is sufficiently large to identify fluctuations due to the cross-hatch pattern in Fig. 6.2a, with regions featuring higher and lower Raman shifts around a mean value of $\overline{\omega}_{Si} = 510.4(2)$ cm^{-1}. In Fig. 6.2c, we investigate the relationship between the Raman shifts from the quantum well ω_{Si} and from the SiGe buffer ω_{SiGe}. We find a strong linear correlation with a slope $\Delta\omega_{Si}/\Delta\omega_{SiGe} = 1.01(2)$, suggesting that the distribution of the Raman shift in the Si quantum well is mainly driven by strain fluctuations in the SiGe SRB, rather than compositional fluctuation[47].

We calculate the strain in the quantum well using the equation $\epsilon = (\omega_{Si} - \omega_0)/b_{Si}$, where $\omega_0 = 520.7$ cm^{-1} is the Raman shift for bulk, relaxed Si and $b_{Si} = 784(4)$ cm^{-1} is the Raman phonon strain shift coefficient of strained silicon on similar SiGe SRBs[48]. From $\overline{\omega}_{Si}$, we estimate the mean value of the in-plane strain for the quantum well $\overline{\epsilon} = 1.31(3)$ %. This value is qualitatively comparable to the expected value of ≈ 1.19(4) % from the lattice mismatch between Si and the $Si_{0.69}Ge_{0.31}$ SRB (see Supplementary Note 2). A more quantitative comparison would require a direct measurement of b_{Si} on our heterostructures based upon high-resolution X-ray diffraction analysis across multiple samples with varying strain conditions. Figure 6.2d shows the normalised distribution of strain fluctuations percentage around the mean value $\Delta\epsilon/\overline{\epsilon} = (\epsilon - \overline{\epsilon})/\overline{\epsilon}$. The data follows a normal distribution (black line) characterised by a standard deviation of 3.0(1) %, comparable with similar measurements in strained Ge/SiGe heterostructures[49]. Given the significant correlation between Raman shifts in the quantum well and the SiGe buffer, alongside the measured strain levels exhibiting a narrow bandwidth of fluctuations, we argue that, with our growth conditions, the Si quantum well is uniformly and coherently grown on the underlying SiGe buffer. As a consequence, we expect strain-release defects in the quantum well to be very limited, if present at all.

6.2.3. ELECTRICAL CHARACTERISATION OF HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

We evaluate the influence of the design choice of a 7 nm thick quantum well on the scattering properties of the 2D electron gas (2DEG) through wafer-scale electrical transport measurements. The measurements are performed on Hall-bar-shaped Heterostructure Field-Effect Transistors (H-FETs) operated in accumulation mode (Methods). Multiple H-FETs across the wafer are measured within the same cool-down at a temperature of 1.7 K using refrigerators equipped with cryo-multiplexers[40]. Figure 6.3a,b show the mean mobility-density and conductivity-density curves in the low-density regime relevant for quantum dots. These curves are obtained by averaging the mobility-density curves from ten H-FETs fabricated from the same wafer (solid line), and the different shadings represent the intervals corresponding to one, two, and three standard deviations. The distribution of mobility and conductivity is narrow, with a variance lower than 5% over the entire density range. Furthermore, we observe similar performance from H-FETs fabricated on a nominally identical heterostructure grown subsequently (see Supplementary Fig. 5), indicating the robustness of both our heterostructure growth and H-FET fabrication process. At low densities, the mobility increases steeply due to the increasing screening of scattering from remote impurities at the semiconductor-dielectric interface. This is confirmed by the large power law exponent $\alpha = 2.7$ obtained by fitting the

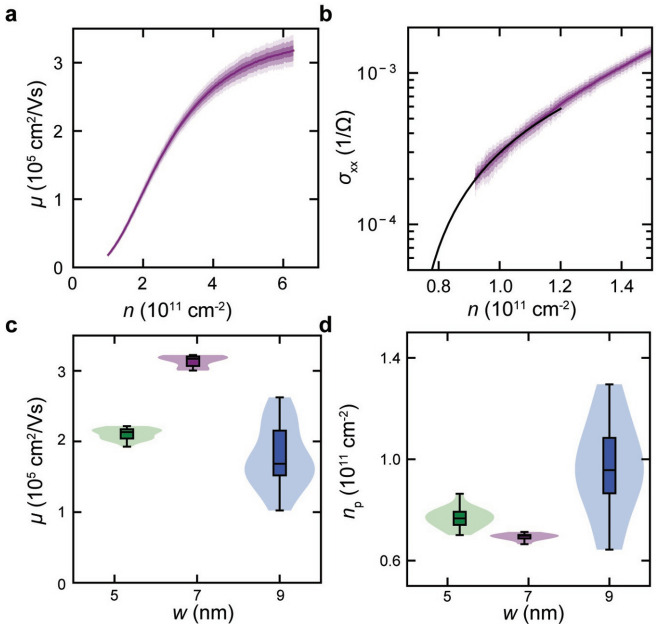


Figure 6.3: **Electrical transport measurements. a** Mean mobility μ as a function of density n at $T = 1.7$ K obtained by averaging measurements from 10 H-FETs fabricated on the heterostructure with a 6.9(5) nm quantum well. The shaded region represents one, two, and three standard deviations of μ at a fixed n. Data from this heterostructure are color-coded in purple in all subsequent figures. **b** Mean conductivity σ_{xx} as a function of n and fit to the percolation theory[50] in the low-density regime (solid line). **c**, **d** Distributions of mobility μ measured at $n = 6 \times 10^{11}$ cm^{-2} and percolation density n_p for heterostructures featuring quantum wells of different thickness w: 9.0(5) nm (blue, 16 H-FETs measured and reported in ref. [17]), 6.9(5) nm (purple, from the analysis of the same dataset in **a**, **b**), and 5.3(5) nm (green, 22 H-FETs measured and reported in ref. [17]). Violin plots, quartile box plots, and mode (horizontal line) are shown.

mean mobility-density curve to the relationship $\mu \propto n^{\alpha}$ in the low-density regime[51]. At high density, the mobility keeps increasing, albeit with a much smaller power law exponent $\alpha = 0.3$. This indicates that scattering from nearby background impurities, likely oxygen within the quantum well[39], and potentially interface roughness[52] become the limiting mechanism for transport in the 2DEG.

From the curves in Fig. 6.3a,b, we obtain the distributions of mobility μ measured at high density ($n = 6 \times 10^{11}$ cm^{-2}) and of the percolation density n_p, extracted by fitting (black line) to percolation theory[50]. In Fig. 6.3c,d, we benchmark these metrics for the 6.9 nm thick quantum well against the distributions obtained previously[17] for a quantum well thickness of 5.3(5) nm and 9.0(5) nm. The 6.9 nm quantum well performs the best, with a mean mobility at high densities of $\mu = 3.14(8) \times 10^5$ cm^2/Vs and a percolation density of $n_p = 6.9(1) \times 10^{10}$ cm^{-2}.

The distributions show two noteworthy features: a 50 % increase in mobility between the 5.3 nm and 6.9 nm quantum well and a three-fold reduction in the variance of the distribution between the 9.0 nm quantum well and the remaining two. We attribute the mobility increase to reduced scattering from alloy disorder, as the wave function delo-

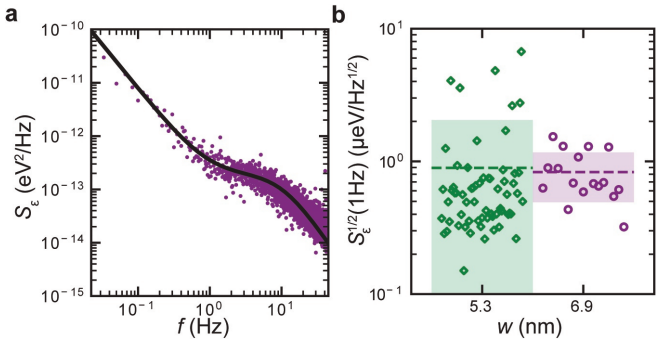


Figure 6.4: **Charge noise measurements. a** Charge noise power spectral density S_ϵ measured on a flank of a Coulomb peak and extracted using the lever arm of the corresponding Coulomb diamond. The black line is a fit to the function, which is the sum of a power law and a Lorentzian. **b** Experimental scatter plots of charge noise at 1 Hz ($S_\epsilon^{1/2}$(1 Hz)) obtained by repeating charge noise spectrum measurements as in **a** for multiple devices and different electron occupancy. Data from the 6.9(5) nm quantum well (purple, 2 devices, 17 spectra) is compared to data from the 5.3(5) nm quantum well (green, 63 spectra, 5 devices, reported in ref. [17]). We compare single-layer devices (diamonds) and multi-layer devices featuring overlapping gate geometry and micromagnets (circles). Dashed lines and shaded area denote the mean value and two standard deviations.

calizes further into the quantum well rather than penetrating into the barrier[42]. We attribute the large spread in transport properties of the widest quantum well to some degree of strain relaxation and associated defects[17]. This explanation is further supported by comparative measurements of Raman shift correlation (see Supplementary Fig. 4) and highlights the sensitivity of the transport properties and their distributions to strain relaxation in the quantum well.

6.2.4. CHARGE NOISE MEASUREMENTS IN QUANTUM DOTS

Moving on to quantum dot characterisation, we focus on the measurement of low-frequency charge noise using complete spin qubit devices cooled at the base temperature of a dilution refrigerator (Methods). The device design is identical to the one in refs. [53, 54] and features overlapping gates for electrostatic confinement and micromagnets for coherent driving. We tune the sensing dot in the single electron regime, measure time traces of the source-drain current I_{SD} on a flank of a Coulomb peak, and repeat for several peaks before the onset of a background current. From the time-dependent I_{SD} we obtain the current noise power spectral density S_I and convert to charge noise power spectral density S_ϵ using the measured lever arm and slope of each Coulomb peak (Methods). We confirm that chemical potential fluctuations are the dominant contributions to the noise traces by measuring the noise in the Coulomb blockade and on top of a Coulomb peak (see Supplementary Fig. 6)[55]. The latter measurement also excludes that the noise traces have any relation to the change of noise floor of the current amplifier[56].

Figure 6.4a shows a representative noise spectrum. We observe an approximate $1/f$ trend at low frequency, suggesting the presence of an ensemble of two-level fluctuators (TLFs) with a wide range of activation energies[57, 58]. Notably, a kink appears at a specific frequency, which is attributed to the additional contribution in the power spectral

density of a single TLF near the sensor[15, 55]. We fit this spectrum to a function which is the sum of a power law and a Lorentzian of the form $\frac{A}{f^{\alpha}} + \frac{B}{f/f_0+1}$, where A, B, α, and f_0 are fitting parameters. We extract $f_0 = 10.38(3)$ Hz, $\alpha = 1.66(2)$, and the power spectral density at 1 Hz $S_\epsilon(1\text{ Hz}) = 0.60(5)$ μeV/Hz$^{1/2}$. We repeat the analysis on a set of 17 noise spectra obtained from measurements of two separate devices (Supplementary Figs. 7 and 8). We do not observe a clear monotonic dependence of the noise spectra on the increasing electron occupancy in the quantum dots, in agreement with the measurement in ref. [17] for devices with a similar semiconductor-dielectric interface and a thinner ($w = 5.3$ nm) quantum well.

In Fig. 6.4b, we evaluate the noise power spectral density at 1 Hz $S_\epsilon^{1/2}(1\text{ Hz})$ to compare the performance of the 6.9(5) nm and the 5.3(5) nm quantum well. In addition to the different thickness of the quantum well, the devices on the 5.3 nm quantum well are defined by a single-layer of gates, whilst the devices on the 6.9 nm quantum well are complete qubit devices featuring a three-layers of overlapping gates, additional dielectric films in between, and micromagnets. The noise power spectral density in the multi-layer devices (purple) and single-layer devices (green) are similar, with $|S_\epsilon| = 0.9(3))$ μeV/Hz$^{1/2}$ and $|S_\epsilon| = 0.9(9)$ μeV/Hz$^{1/2}$, respectively. Because both narrow quantum wells are fully strained, we expect the two heterostructures to contribute similarly to the electrostatic noise. Therefore, our measurements suggest that using multiple metallic gates, dielectric layers, and micromagnets does not degrade the noise performance in our devices. Our observations are consistent with previous measurements in Si/SiGe heterostructures at base temperature when impurities in the dielectric likely freeze out[55, 59]. We attribute this robustness to the distinctive characteristics of Si/SiGe heterostructures, where the active region of the device resides within a buried quantum well, well separated from the gate stack, unlike Si-MOS. We speculate that the metallic layers in the gate stack, positioned between the quantum well and the micromagnets, may shield the effects of additional impurities and traps in the topmost layers.

6.2.5. VALLEY SPLITTING MEASUREMENTS IN QUANTUM DOTS

To complete the quantum dot characterisation, we measure the two-electron singlet-triplet splitting E_{ST} in quantum dot arrays as in the six spin qubit devices described in ref. [5] by mapping the 1e → 2e transition as a function of the parallel magnetic field (B). E_{ST} is a reliable estimate of the valley splitting energy E_V in strongly confined quantum dots[20, 30, 60, 61] and is the relevant energy scale for spin-to-charge conversion readout with Pauli spin-blockade[5, 62].

Figure 6.5a shows a typical magnetospectroscopy map with a superimposed thin line highlighting the 1e → 2e transition at a given magnetic field (Methods). The thick line is a fit of the transition to the theoretical model[30, 61], allowing us to estimate the singlet-triplet splitting $E_{ST} = g\mu_B B_{ST}$. Here, $g = 2$ is the electron gyromagnetic ratio, μ_B is the Bohr magneton, and B_{ST} corresponds to the magnetic field at which the energy of the 1e → 2e transition starts to decrease, signalling the transition from the singlet state S_0 to the triplet state (T_-) as the new ground state of the two-electron system. For this specific quantum dot, we find $B_{ST} = 1.77(2)$ T, corresponding to $E_V = 0.205(2)$ meV.

Figure 6.5b compares the valley splitting of spin qubit devices on the 6.9 nm quantum well (purple, see Supplementary Fig. 9) and on the 9.0 nm quantum well (blue) from

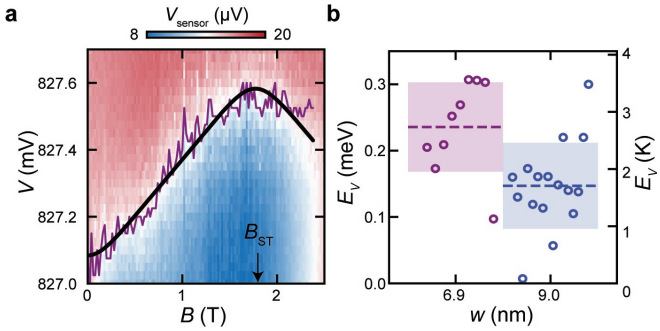


Figure 6.5: **Valley splitting measurements.** **a** Typical magnetospectroscopy map of the (1e) → (2e) charge transition, used to measure singlet-triplet splittings. The thin purple line shows the location of the charge transition at a fixed magnetic field. The thick black line is a fit to the data (Methods), from which we extract the kink position B_{ST}. The valley splitting E_V is given by $E_V = g\mu_B B_{ST}$, where $g = 2$ is the gyromagnetic ratio, and μ_B is the Bohr magneton. **b** Experimental scatter plots of valley splitting obtained by magnetospectroscopy on complete spin qubit devices. Data from heterostructures with a 6.9(5) nm quantum well (purple, 9 quantum dots from 2 devices) is compared to data from a 9.0(5) nm quantum well (blue, 16 quantum dots, 3 devices, from ref. [5]). Dashed lines and shaded area denote the mean value and two standard deviations.

6

ref. [5]. While the dots in all devices measured have the same nominal design and share the same fabrication process (Methods), the heterostructures further differ in the passivation of the SiGe top barrier. The heterostructure with the 6.9 nm well is passivated by an amorphous self-terminating Si-rich layer, while the 9.0 nm well has a conventional epitaxial Si cap[16] (Methods). Passivation by a self-terminating Si-rich layer yields a more uniform and less noisy semiconductor-dielectric interface, which in turn promotes higher electric fields at the Si/SiGe interface[16, 17]. We observe a statistically significant 60% increase in the mean valley splitting in the 6.9 nm quantum well with an amorphous Si-rich termination, featuring a mean value of $\overline{E_V} = 0.24 \pm 0.07$ meV (see Supplementary Note 5). Furthermore, the distribution of valley splitting in devices with the wider quantum well shows instances of low values (e.g., $E_V < 0.1$ meV), as predicted by prevailing theory[31]. In contrast, these instances are absent (although still predicted) in the measured devices with the narrower quantum well.

While we cannot pinpoint a single mechanism responsible for the increase in the mean value of valley splitting, we speculate that multiple factors contribute to this observed improvement. The tighter vertical confinement within the narrower quantum well[41], coupled with the relatively wide quantum well interface width, increases the overlap of the electron wavefunction with Ge atoms in the barrier. This amplifies the effect of random alloy disorder, which is known to increase valley splitting[30, 31]. Similarly, the improved semiconductor-dielectric facilitates tighter lateral and vertical confinement of the dots, which leads to a stronger electric field, contributing to drive the valley splitting[28, 29]. Furthermore, the near-absence (or, at most, very limited density) of strain-release defects in the thin quantum well ensures a smoother potential landscape, promoting improved electrostatic control and confinement of the dot. Additionally, we suggest that a larger amount of experimental data points is required to comprehensively explore the distribution of valley splitting in the 6.9 nm quantum well. Mapping of valley-

splitting by spin-coherent electron shuttling[63], for example, could enable a meaningful comparison with existing theory[31] and help determine whether the absence of low instances of valley splitting results from undersampling the distribution or is influenced by some other underlying factor.

6.2.6. DISCUSSION

In summary, we developed strained ^{28}Si/SiGe heterostructures providing a benchmark for silicon as a host semiconductor for gate-defined quantum dot spin qubits. Our growth protocol yields reproducible heterostructures that feature a 6.9 nm thick ^{28}Si quantum well, surrounded by SiGe with a Ge concentration of 0.31 and an interface width of about 1 nm. These quantum wells are narrow enough to be fully strained and maintain coherence with the underlying substrate, displaying reasonable strain fluctuations. Yet, the quantum wells are sufficiently wide to mitigate the effects of penetration of the wave function into the barrier. Coupled with a high-quality semiconductor-dielectric interface, these ^{28}Si/SiGe heterostructures strike the delicate balance between disorder, charge noise, and valley splitting. We comprehensively probe these properties with statistical significance using classical and quantum devices. Compared to our control heterostructures supporting qubits, we demonstrate a remarkable 50 % increase in mean mobility alongside a 10 % decrease in percolation density while preserving a tight distribution of these transport properties. Our characterization of low-frequency charge noise in quantum dot qubit devices consistently reveals low charge noise levels, featuring a mean value of power spectral density of 0.9(3) μeV/Hz$^{1/2}$ at 1 Hz. These heterostructures support consistently large valley splitting with a mean value of 0.24(7) meV. This is a significant advancement considering that instances of similarly large valley splitting were obtained previously on heterostructures with about one order of magnitude less mobility[18, 34, 38]. We envisage that fine-tuning the distance between the quantum well and the semiconductor-dielectric interface, as well as the Ge concentration in the SiGe alloy, could offer avenues to further increase performance. Our findings highlight the significance of embracing a co-design approach to drive innovation in material stacks for quantum computing. As quantum processors mature in complexity, additional metrics characterising the heterostructures will likely need to be considered to optimise the design parameters and to fully leverage the advantages of the Si/SiGe platform for spin qubits.

6.3. METHODS

Si/SiGe heterostructure growth. The ^{28}Si/SiGe heterostructures are grown on a 100-mm n-type Si(001) substrate using an Epsilon 2000 (ASMI) reduced-pressure chemical vapour deposition reactor. The reactor is equipped with a $^{28}SiH_4$ gas cylinder (1% dilution in H_2) for the growth of isotopically enriched ^{28}Si with 800 ppm of residuals of other isotopes[14]. Starting from the Si substrate, the layer sequence of all heterostructures comprises a step-graded $Si_{(1-x)}Ge_x$ layer with a final Ge concentration of $x = 0.31$ achieved in four grading steps ($x = 0.07$, 0.14, 0.21, and 0.31), followed by a $Si_{0.69}Ge_{0.31}$ strain-relaxed buffer (SRB). The step-graded buffer and the SRB are ≈3 μm and ≈2.4 μm thick, respectively. We grow the SRB at 625 °C, followed by a growth interruption and the quantum well growth at 750 °C[30]. The various heterostructures compared in Fig. 6.3 of the main text differ in the thickness of the Si quantum well, which are 9.0(5) nm, 6.9(5) nm, and 5.3(5) nm. We change the thickness of the quantum well by only acting on the quantum well growth time and leaving all the other conditions unaltered. This yields heterostructures with similar interface widths (see Supplementary Figs. 1 and 2 and analysis in ref. [30]) On top of the Si quantum well, the heterostructure is terminated with a 30 nm thick SiGe spacer, grown using the same conditions as the virtual substrate. The surface of the SiGe spacer is passivated with DCS at 500 °Cbefore exposure to air [16]. We confirm the Ge concentration in the spacer and virtual substrate via secondary ions mass spectrometry (similar to Fig.S13 from ref. [30]) and quantitative electron energy loss spectroscopy.

Raman spectroscopy. The two-dimensional Raman mapping follows a similar approach as in ref. [47]. We perform the measurements on heterostructures where we stop the growth after the quantum well and do not grow the SiGe spacer. This maximises the Raman signal coming from the Si quantum well. The measurements were performed with a LabRam HR Evolution spectrometer from Horiba-J.Y. at the backscattering geometry using an Olympus microscope (objective x100 with a 1 μm lateral resolution). We use a violet laser ($\lambda = 405$ nm) and an 1800 gr/mm grating to achieve the highest spectral resolution. We focus the laser spot to have a spatial dimension of ≈ 1 μm. Given the laser wavelength, we expect to probe the Si quantum well and the SiGe SRB below (which has a uniform composition of Ge). We calibrate the Raman shift using a stress-free single crystal Si substrate with a Raman peak position at $\omega_0 = 520.7$ cm^{-1}. We use this value as a reference for the calculation of the strain of the Si quantum well.

Device fabrication. The fabrication process for H-FETs involves reactive ion etching of mesa-trench and markers; selective P-ion implantation and activation by rapid thermal annealing at 700 °C; atomic layer deposition (ALD) of a 10-nm-thick Al_2O_3 gate oxide; sputtering of Al gate; selective chemical etching of the dielectric with BOE (7:1) followed by electron beam evaporation of Ti:Pt to create ohmic contacts. All patterning is done by optical lithography on a four-inch wafer scale. Single and multi-layer quantum dot devices are fabricated on wafer coupons from the same H-FET fabrication run and share the process steps listed above. Single-layer quantum devices feature all the gates in a single evaporation of Ti:Pd (3:17 nm), followed by the deposition via ALD of a 5 nm thick AlOx layer and consequent evaporation of a global top screening gate of Ti:Pd (3:27 nm). Multi-layer quantum dot devices feature three overlapping gate metallizations with increasing thickness of Ti:Pd (3:17 nm, 3:27 nm, 3:37 nm), each isolated by a 5 nm thick AlOx dielectric. Finally, a last AlOx layer of 5 nm separates the gate stack from the micro-magnets (Ti:Co, 5:200 nm). All patterning in quantum dot devices is done via electron beam lithography.

H-FETs electrical characterisation. Hall-bar heterostructure field effect transistor (H-FET) measurements are performed in an attoDRY2100 dry refrigerator equipped with cryo-multiplexer[40] at a base temperature of 1.7 K[16]. We operate the device in accumulation mode using a gate electrode to apply a positive DC voltage (V_G) to the quantum well. We apply a source-drain bias of 100 μV and use standard four-probe lock-in technique to measure the source-drain current I_{SD}, the longitudinal voltage V_{xx}, and the transverse Hall voltage V_{xy} as a function of V_G and perpendicular magnetic field B. From here, we calculate the longitudinal resistivity ρ_{xx} and transverse Hall resistivity ρ_{xy}. The Hall electron density n is obtained from the linear relationship $\rho_{xy} = B/en$ at low magnetic fields. The electron mobility μ is extracted as $\sigma_{xx} = ne\mu$, where e is the electron charge. The percolation density n_p is extracted by fitting the longitudinal conductivity σ_{xx} to the relation $\sigma_{xx} \propto (n - n_p)^{1.31}$ [50]. We invert the resistivity tensor to calculate the longitudinal (σ_{xx}) and perpendicular (σ_{xy}) conductivity.

Low-frequency charge noise. We perform low-frequency charge noise measurements in a Bluefors LD400 dilution refrigerator with a base temperature of $T_{MC} \approx 20$ mK. We use devices lithographically identical to those described in ref. [53]. We tune the sensing dot of the devices in the Coulomb blockade regime and use it as a single electron transistor (SET). We apply a fixed source-drain excitation to the two reservoirs connected to the SET and record the current I_{SD} as a function of time using a sampling rate of 1 kHz for 600 s. We measure I_{SD} on the flank of each Coulomb peak where $|dI_{SD}/dV_P|$ is the largest, and therefore, the SET is the most

sensitive to fluctuations. We check that chemical potential fluctuations are the dominant contributions to the noise traces by measuring the noise in blockade and on top of a coulomb peak (see Supplementary Fig.6)[55]. The latter also excludes that the noise traces have any relation to the change of noise floor of the current amplifier[56]. We divide the time traces into ten segments of equal length and use the Fourier transform to convert the traces in the frequency domain. We average the ten different spectral densities to obtain the final current noise spectrum in a range centred to 1 Hz between 25 mHz and 40 Hz to avoid a strong interference around 50 Hz coming from the setup. We convert the current noise spectrum (S_I) in a charge noise spectrum (S_ϵ) using the formula [17, 55]:

$$S_\epsilon = \frac{a^2 S_I}{|dI/dV_\mathrm{P}|^2} \tag{6.1}$$

where a is the lever arm and $|dI/dV_\mathrm{P}|$ is the slope of the specific Coulomb peak selected to acquire the time trace. We calculate the lever arm from the slopes of the Coulomb diamonds as $a = |\frac{m_\mathrm{S} m_\mathrm{D}}{m_\mathrm{S} - m_\mathrm{D}}|$, where m_S and m_D are the slopes to source and to drain, and we estimate $|dI/dV_\mathrm{P}|$ from the numerical derivative of the Coulomb peak. We perform this analysis for every Coulomb peak and use the specific values of the lever arm and slope to calculate the charge noise spectrum.

Valley splitting. We perform magnetospectroscopy experiments in quantum dot devices cooled in a dilution refrigerator with a base temperature of $T_\mathrm{MC} \approx 10$ mK. We use devices lithographically similar to those described in ref. [5]. We tune the quantum dots in the single-electron regime to isolate the 1e → 2e transition. We start the magnetospectroscopy measurement from the quantum dot closest to the sensing dot and use the remaining dots as an electron reservoir. We use the impedance of a nearby sensing dot to monitor the charge state of every quantum dot. The impedance of the sensing dot is measured using RF reflectometry. The signal is measured by monitoring the reflected amplitude of the rf readout signal through a nearby charge sensor. We use the amplitude (Device 1) and the Y component (Device 2) of the reflected signal to map the 1e → 2e transition. We fit the 1e → 2e transition as a function of the magnetic field with the relation[30, 61]:

$$V_\mathrm{P} = \frac{1}{\alpha\beta_\mathrm{e}} \ln \frac{e^{\frac{1}{2}kB+\beta_\mathrm{e}E_\mathrm{ST}}(e^{kB}+1)}{e^{kB}+e^{2kB}+e^{kB+\beta_\mathrm{e}E_\mathrm{ST}}+1} \tag{6.2}$$

where α is the lever arm, V_P is the plunger gate voltage, E_ST is the single-triplet energy splitting, $k = g\mu_\mathrm{B}\beta_e$, $\beta_e = 1/k_\mathrm{B}T_\mathrm{e}$, $g = 2$ is the g-factor in silicon, μ_B is the Bohr magneton, B is the magnetic field, k_B is Boltzmann's constant, and T_e is the electron temperature. E_ST is linked to the position of the kink (B_ST) in the magnetospectroscopy traces by the relation $E_\mathrm{ST} = g\mu_\mathrm{B}B_\mathrm{ST}$.

(Scanning) Transmission Electron Microscopy. For structural characterization with (S)TEM, we prepared lamella cross-sections of the quantum well heterostructures using a Focused Ion Beam (Helios 600 dual beam microscope). HR-TEM micrographs were acquired in a TECNAI F20 microscope operated at 200 kV. Atomically resolved HAADF-STEM data was obtained in a probe-corrected TITAN microscope operated at 300 kV. EELS mapping was carried out in a TECNAI F20 microscope operated at 200 kV with approximately 2 eV energy resolution and 1 eV energy dispersion. Principal Component Analysis (PCA) was applied to the spectrum images to enhance the signal-to-noise ratio.

6.4. SUPPLEMENTARY

6.4.1. MEASUREMENT OF THE THICKNESS AND SHARPNESS OF THE QUANTUM WELLS

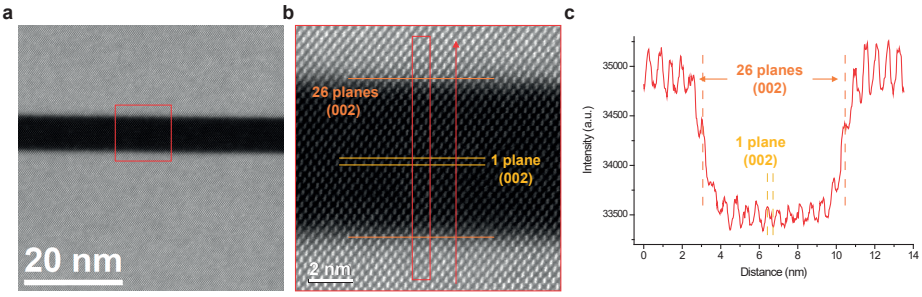


Figure 6.6: Method for computing the thickness of the quantum well based on the counting of the (002) horizontal planes, which reduces the uncertainty and bias associated with properly detecting the margins of the quantum well.

We measure the thickness of the Si layer quantum well (w) by considering the interplanar spacing of the horizontal planes (002) of the quantum well (d_{qw}) and of the underlying strain-relaxed SiGe buffer layer (d_{buffer}). For the $Si_{1-x}Ge_x$ buffer layer, we consider the stoichiometry $x = 0.31(1)$ as measured by means of quantitative EELS and SIMS[30, 45] and calculate the expected cell parameter a_{cell} using the following approximation of Vegard's law[64]:

$$a_{cell} = a_{Si} + 0.20x + 0.027x^2 = 2.75(9)\ \text{Å} \tag{6.3}$$

where $a_{Si} = 5.431$ Å bulk Si lattice constant, and $x = 0.31(1)$. To calculate d_{buff}, we use the formula for the interplanar distance of the (002) plane in a diamond cubic system:

$$d_{hkl} = \frac{a_{cell}}{\sqrt{h^2+k^2+l^2}} = \frac{a_{cell}}{\sqrt{0^2+0^2+2^2}} = \frac{a_{cell}}{2}. \tag{6.4}$$

Since the quantum well is strained, d_{qw} is found by considering the average dilatation δ of the quantum well (002) planes with respect to the (002) planes of the buffer. The dilatation δ is measured by Geometrical Phase Analysis (GPA). The standard deviation of GPA is high for dilatation close to 0, as happens with the (220) epitaxial planes, for which the method is not the preferred choice. Nevertheless, for the larger dilatation of the (002) planes, the relatively smaller standard deviation makes the measurement significant. As a result, d_{qw} is computed by:

$$d_{qw} = d_{buff}(1+\delta). \tag{6.5}$$

Finally, the thickness of the quantum well is given by:

$$w = n_{qw} d_{qw}, \tag{6.6}$$

where n_{qw} is the number of atomic planes in the (002) direction forming the quantum well, and d_{qw} is the distance between two planes. Therefore, the expected uncertainty of the thickness measurement lies in whether the initial and last plane of the well is being considered or not, *i.e.*, the standard deviation is given by $\sigma = 2d_{qw}$.

We perform four different measurements and count the (002) planes in different regions of the quantum well. We find $n_{qw} = 25$ two times, and $n_{qw} = 26$ two times. We measure an average $\delta = -1.700 \pm 0.003$ of %, leading to $d_{qw} = 2.70 \pm 0.01$ Å, and resulting in an average thickness $w = 6.9 \pm 0.5$ nm.

We validate the thickness of the quantum well (w) and quantify the sharpness of the top and bottom interfaces by fitting the intensity profile with a Sigmoid function[44]:

$$I(x) = \frac{1}{1 + e^{\frac{x_{top} - x}{\tau_{top}}}} + \frac{1}{1 + e^{\frac{x - x_{bottom}}{\tau_{bottom}}}} \tag{6.7}$$

where x_{top} and x_{bottom} are the position of the top and bottom interfaces, and τ_{top} and τ_{bottom} are the characteristic length quantifying the top and bottom interfaces of the quantum well, *i.e.*, the SiGe/Si and Si/SiGe interfaces. We characterize the interface sharpness with the 4τ parameter corresponding to the length over which the intensity profile changes from 0.12 to 0.88 of the asymptotic value.

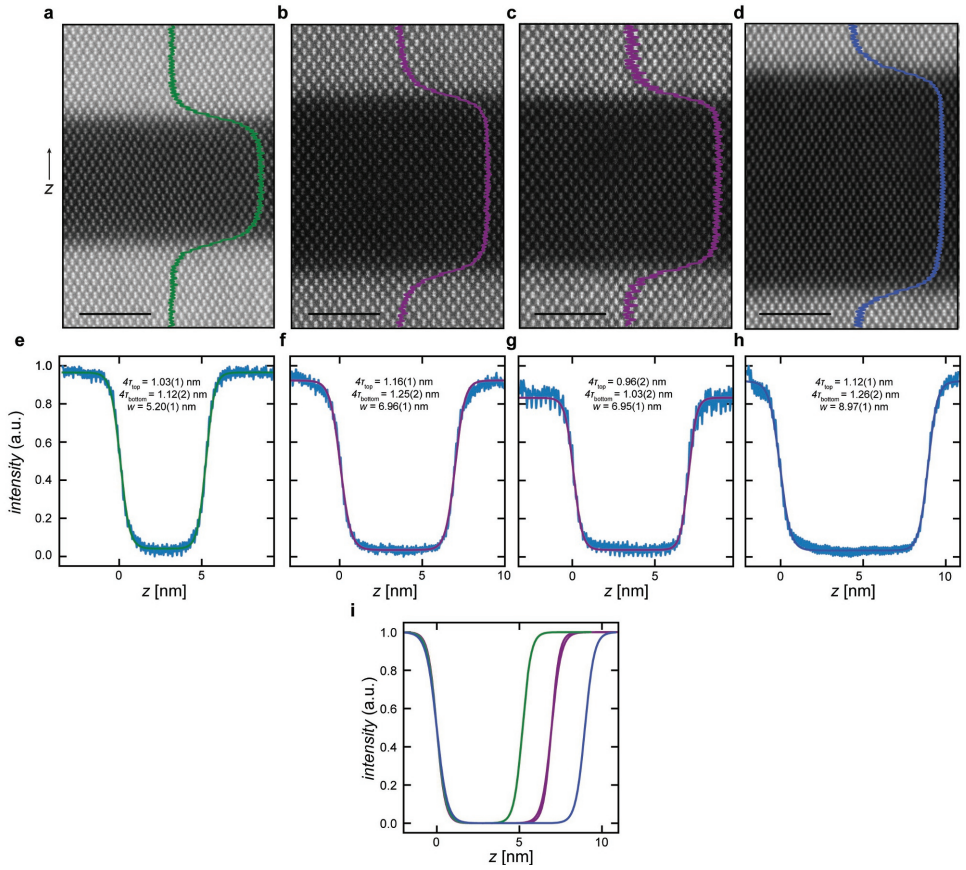


Figure 6.7: **a**-**d** High-resolution STEM with superimposed intensity profiles from multiple wafers featuring different thicknesses of the quantum well. All images are taken on wafers featuring the H-FET gate stack, *i.e.*, where the first steps of the fabrication process have been executed to resemble the condition of the actual quantum dot devices. The black scale in all images corresponds to 3 nm. Images in **b** and **c** come from two nominally identical heterostructures, *i.e.* grown using the same recipe on two wafers. **e**-**h** Corresponding intensity profile from **a**-**d** with superimposed fit to a sigmoid function as reported in Eq. 6.7. From this fit, we extract the parameters characterizing the sharpness of the bottom (τ_{bottom}) and top (τ_{top}) interfaces, and the quantum well thickness ($w = x_{top} - x_{bottom}$). **i** Comparison of the fitted sigmoid intensity profiles for the three heterostructures considered in the main text featuring quantum wells that are nominally 5 nm, 7 nm, and 9 nm wide

6.4.2. STRAIN ANALYSIS WITH RAMAN SPECTROSCOPY

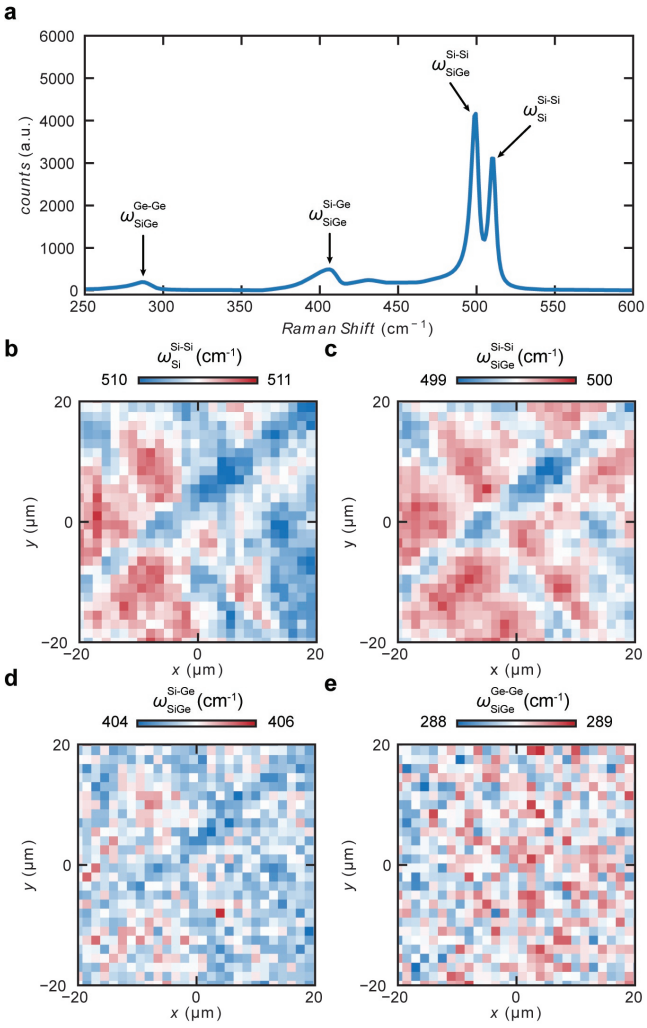


Figure 6.8: **a** Typical Raman spectrum of a Si/SiGe heterostructure without the SiGe topmost barrier acquired using a violet laser. The spectrum shows multiple peaks corresponding to the Si-Si vibration in the Si quantum well ($\omega^{\text{Si-Si}}_{\text{Si}}$), and the Si-Ge, Si-Si, and Ge-Ge vibrations in the SiGe SRB ($\omega^{\text{Si-Ge}}_{\text{SiGe}}$, $\omega^{\text{Si-Si}}_{\text{SiGe}}$, and $\omega^{\text{Ge-Ge}}_{\text{SiGe}}$, respectively). **b-e** 2D Raman mapping on a 40 μm of the various vibrations from the strained Si quantum well and virtual substrate. We find the average Raman shifts of these vibrations to be: $\overline{\omega}^{\text{Si-Si}}_{\text{Si}} = 510.4(2)$ cm^{-1}, $\overline{\omega}^{\text{Si-Si}}_{\text{SiGe}} = 499.5(2))$ cm^{-1}, $\overline{\omega}^{\text{Si-Ge}}_{\text{SiGe}} = 404.8(3)$ cm^{-1}, and $\overline{\omega}^{\text{Ge-Ge}}_{\text{SiGe}} = 288.5(5)$ cm^{-1}.

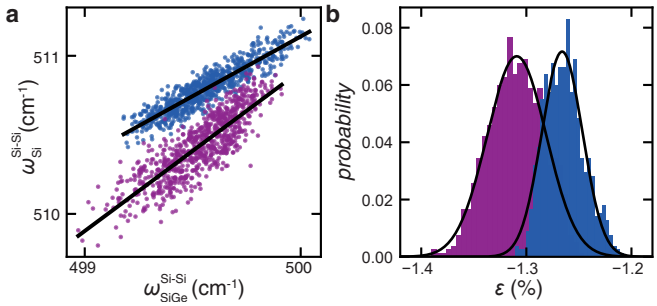


Figure 6.9: **a** Comparative cross-correlation plot of the Si-Si vibration from the strained Si quantum well (ω_{Si}) and from the SiGe relaxed buffer (ω_{SiGe}) for a quantum well with a thickness of 6.9(5) nm (purple) and 9.0(5) nm (blue). The black line is a linear fit to the data with an angular coefficient $a = 1.01(1)$ for the thinner well and $a = 0.75(2)$ for the thicker well. **b** Strain distributions for the two Si quantum wells. We find an average strain of $\bar{\epsilon} = -1.31(3)$ % for the 6.9(5) nm quantum well, and $\bar{\epsilon} = -1.26(2)$ % for the 9.0(5) nm quantum well.

We calculate the strain of the Si quantum wells by converting phonon frequency shifts into strain[65, 66]:

$$\epsilon = \frac{\omega(\epsilon) - \omega_0}{b^{Si}}, \tag{6.8}$$

where $\omega_0 = 520.7$ cm^{-1} is the Raman shift associated with the Si-Si vibration from the unstrained Si substrate used to calibrate the Raman spectrometer, $b^{Si} = 784 \pm 4$ cm^{-1} is the strain-shift coefficient for Si reported in ref. [48], and $\omega(\epsilon)$ is the Raman shift associated with the Si-Si vibration from the strained quantum well.

We calculate the expected strain (ϵ) of the Si quantum well as:

$$\epsilon = (a_{SiGe} - a_{Si})/a_{Si} = 1.19(4)\% \tag{6.9}$$

where a_{SiGe} is calculated from Eq. 6.3 where $x = 0.31(1)$ is the Ge concentration in the SiGe buffer and spacer, and $a_{Si} = 0.5431$ nm is the lattice constant of bulk Si.

6.4.3. SUPPLEMENTARY MOBILITY DENSITY CURVES

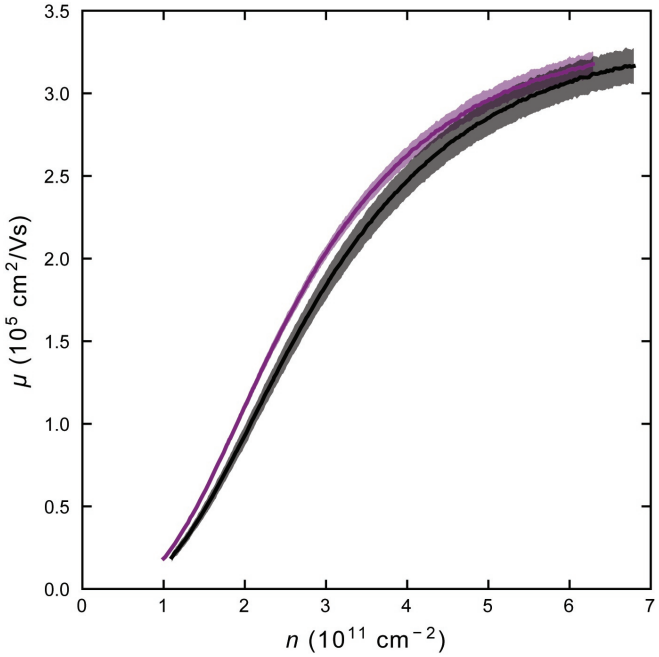


Figure 6.10: Mean mobility μ as a function of density n measured at $T = 1.7$ K for H-FET coming from two different wafers grown using the same recipe at a distance of six months. Purple shows the data from the wafer SQ22-22-3 (10 HFET), and black shows data from SQ21-160-6 (10 HFET). The average mobility at a fixed density (solid line) and one standard deviation (shaded region) are shown.

6.4.4. CHARGE NOISE MEASUREMENTS

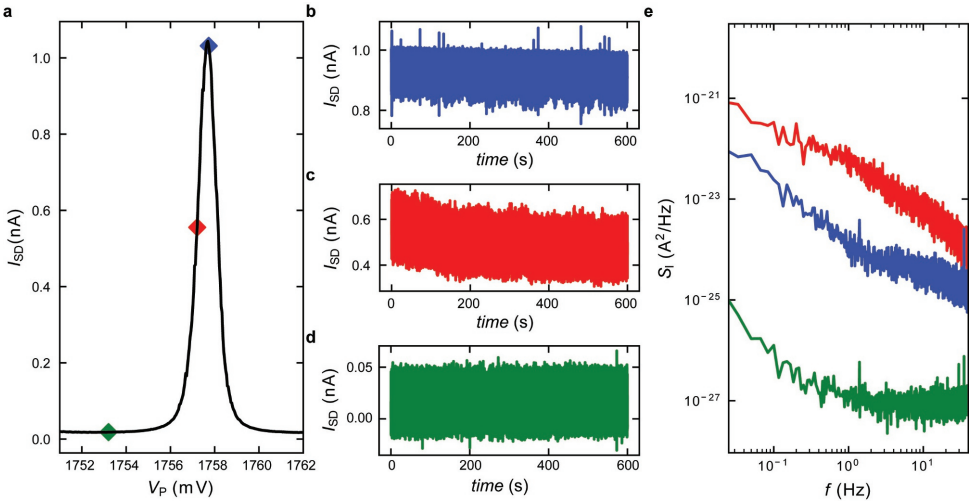


Figure 6.11: **a** Current (I_{SD}) as a function of plunger voltage (V_P) through one of the sensing dots tuned in the single electron regime. The top (blue), flank (red), and blockade (green) are highlighted with diamonds. **b-d** Current time traces in the three different configurations. We acquire ten minutes long time traces at a sampling rate of 1kHz. **e** Current noise power spectral density (S_I). S_I is calculated by dividing the time traces into 10 segments of equal length, using the Fourier transform to convert to the frequency domain, and averaging the ten different Fourier transforms before calculating the power spectral density. As expected, we find that the noise measured at the flank of the Coulomb peak is the greatest [55].

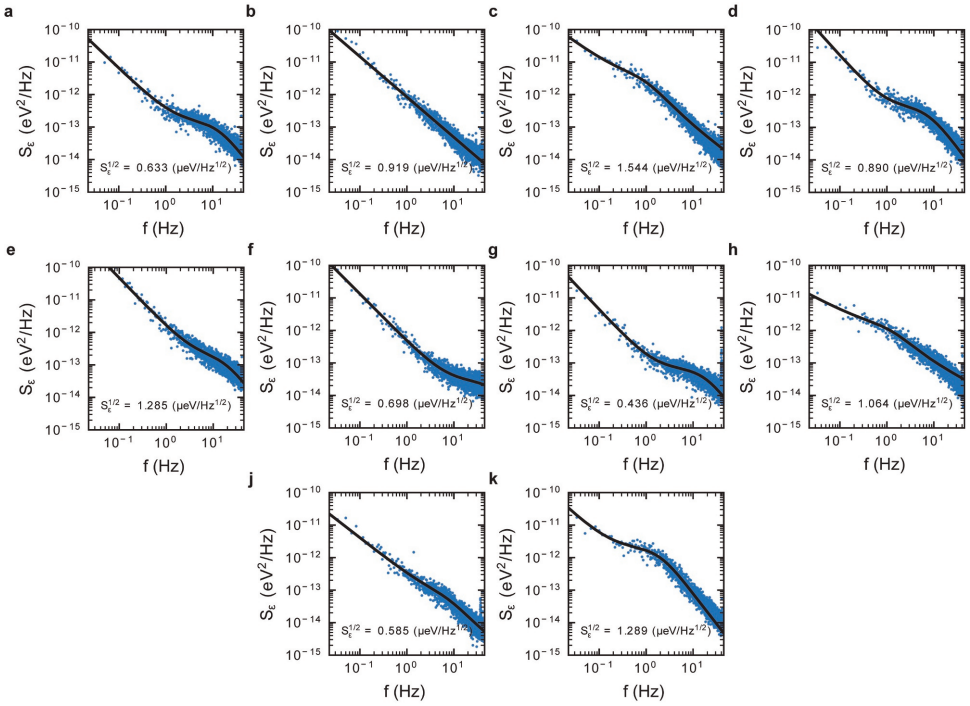


Figure 6.12: Charge noise power spectral density ($S_\epsilon(f)$) measured on a flank of a Coulomb peak and extracted using the lever arm of the corresponding Coulomb diamond for device A. The black line is a fit to the function which is the sum of a power law and a Lorentzian from which we extract the power spectral density at 1 Hz ($S_\epsilon^{1/2}$). The plots are arranged from **a** to **k** for increasing voltage applied to the sensor plunger.

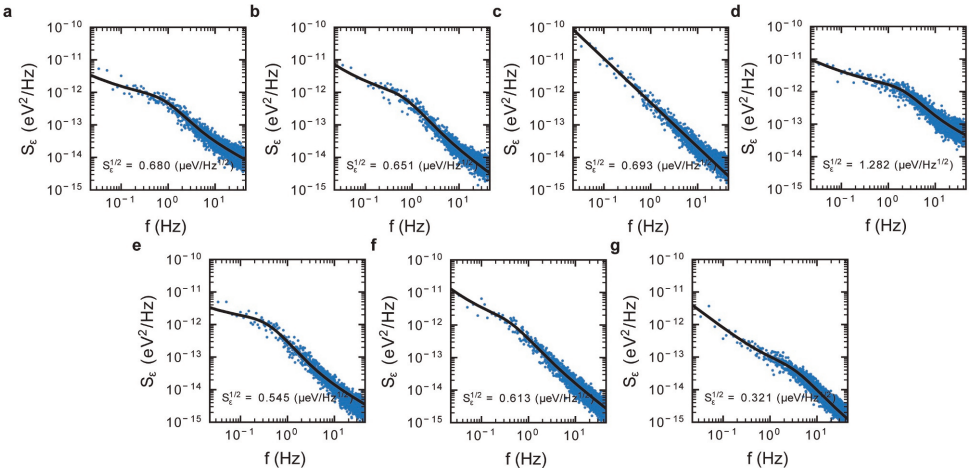


Figure 6.13: Charge noise power spectral density ($S_\epsilon(f)$) measured on a flank of a Coulomb peak and extracted using the lever arm of the corresponding Coulomb diamond for device B. The black line is a fit to the function, which is the sum of a power law and a Lorentzian from which we extract the power spectral density at 1 Hz ($S_\epsilon^{1/2}$). The plots are arranged from **a** to **g** for increasing voltage applied to the plunger.

6.4.5. VALLEY SPLITTING MEASUREMENTS

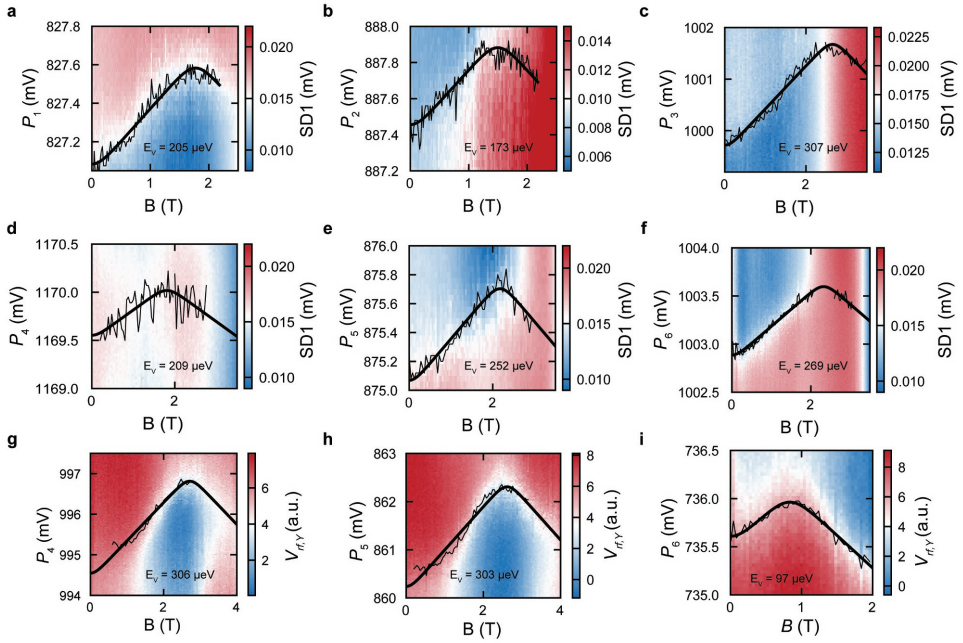


Figure 6.14: Magnetospectroscopy measurements of the 1e → 2e transition for Device 1 (six dots, **a**-**f**) and Device 2 (three dots, **g**-**i**). The thin black line follows the charge transition at a fixed magnetic field. We fit the evolution of the charge transition to the theoretical formula from ref.[30, 61] (thick black line). For $B = B_{ST}$, the Zeeman energy ($E_Z = -e\mu_B B$) equals the single-triplet splitting energy, and the typical kink can be observed.

We perform a Welch test[67] on the valley splitting measurements reported in Fig. 5b of the main text to quantify the statistical significance of our data. The Welch test is used to test the hypothesis that two populations with different variances have equal means. We obtain a t-value of 3.05 corresponding to a p-value of 0.78%, indicating that the probability that the measured data comes from distributions with the same mean is lower than 1 %. This confirms that our improvement in mean valley splitting has statistical significance.

BIBLIOGRAPHY

[1] Nathalie P. De Leon et al. “Materials challenges and opportunities for quantum computing hardware”. en. In: *Science* 372.6539 (Apr. 2021), eabb2823. ISSN: 0036-8075, 1095-9203. DOI: 10.1126/science.abb2823. URL: https://www.science.org/doi/10.1126/science.abb2823 (visited on 07/10/2023).

[2] L. M. K. Vandersypen et al. “Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent”. en. In: *npj Quantum Information* 3.1 (Sept. 2017), pp. 1–10. ISSN: 2056-6387. DOI: 10.1038/s41534-017-0038-y. URL: https://www.nature.com/articles/s41534-017-0038-y (visited on 07/10/2023).

[3] G. Scappucci et al. “Crystalline materials for quantum computing: Semiconductor heterostructures and topological insulators exemplars”. en. In: *MRS Bulletin* 46.7 (July 2021), pp. 596–606. ISSN: 1938-1425. DOI: 10.1557/s43577-021-00147-8. URL: https://doi.org/10.1557/s43577-021-00147-8 (visited on 09/01/2023).

[4] Ruoyu Li et al. “A crossbar network for silicon quantum dot qubits”. en. In: *Science Advances* 4.7 (July 2018), eaar3960. ISSN: 2375-2548. DOI: 10.1126/sciadv.aar3960. URL: https://www.science.org/doi/10.1126/sciadv.aar3960 (visited on 06/15/2023).

[5] Stephan G. J. Philips et al. “Universal control of a six-qubit quantum processor in silicon”. en. In: *Nature* 609.7929 (Sept. 2022), pp. 919–924. ISSN: 1476-4687. DOI: 10.1038/s41586-022-05117-x. URL: https://www.nature.com/articles/s41586-022-05117-x (visited on 07/10/2023).

[6] Jun Yoneda et al. “A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%”. en. In: *Nature Nanotechnology* 13.2 (Feb. 2018), pp. 102–106. ISSN: 1748-3395. DOI: 10.1038/s41565-017-0014-x. URL: https://www.nature.com/articles/s41565-017-0014-x (visited on 07/10/2023).

[7] Floris A. Zwanenburg et al. “Silicon quantum electronics”. In: *Reviews of Modern Physics* 85.3 (July 2013), pp. 961–1019. DOI: 10.1103/RevModPhys.85.961. URL: https://link.aps.org/doi/10.1103/RevModPhys.85.961 (visited on 05/27/2020).

[8] M. L. V. Tagliaferri et al. “Impact of valley phase and splitting on readout of silicon spin qubits”. en. In: *Physical Review B* 97.24 (June 2018), p. 245412. ISSN: 2469-9950, 2469-9969. DOI: 10.1103/PhysRevB.97.245412. URL: https://link.aps.org/doi/10.1103/PhysRevB.97.245412 (visited on 06/22/2023).

[9] Peihao Huang and Xuedong Hu. “Spin relaxation in a Si quantum dot due to spin-valley mixing”. en. In: *Physical Review B* 90.23 (Dec. 2014), p. 235315. ISSN: 1098-0121, 1550-235X. DOI: 10.1103/PhysRevB.90.235315. URL: https://link.aps.org/doi/10.1103/PhysRevB.90.235315 (visited on 06/22/2023).

[10] Inga Seidler et al. “Conveyor-mode single-electron shuttling in Si/SiGe for a scalable quantum computing architecture”. en. In: *npj Quantum Information* 8.1 (Aug. 2022), p. 100. ISSN: 2056-6387. DOI: 10.1038/s41534-022-00615-2. URL: https://www.nature.com/articles/s41534-022-00615-2 (visited on 01/30/2024).

[11] Veit Langrock et al. “Blueprint of a Scalable Spin Qubit Shuttle Device for Coherent Mid-Range Qubit Transfer in Disordered ${\text{Si/SiGe/SiO}}_{2}$”. In: *PRX Quantum* 4.2 (Apr. 2023), p. 020305. DOI: 10.1103/PRXQuantum.4.020305. URL: https://link.aps.org/doi/10.1103/PRXQuantum.4.020305 (visited on 01/30/2024).

[12] A.M.J. Zwerver et al. “Shuttling an Electron Spin through a Silicon Quantum Dot Array”. en. In: *PRX Quantum* 4.3 (July 2023), p. 030303. ISSN: 2691-3399. DOI: 10.1103/PRXQuantum.4.030303. URL: https://link.aps.org/doi/10.1103/PRXQuantum.4.030303 (visited on 07/19/2023).

[13] C. H. Yang et al. “Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting”. en. In: *Nature Communications* 4.1 (June 2013), p. 2069. ISSN: 2041-1723. DOI: 10.1038/ncomms3069. URL: https://www.nature.com/articles/ncomms3069 (visited on 05/27/2020).

[14] D. Sabbagh et al. “Quantum Transport Properties of Industrial $^{28}\mathrm{Si}/^{28}{\mathrm{Si}\mathrm{O}}_{2}$”. In: *Physical Review Applied* 12.1 (July 2019), p. 014013. DOI: 10.1103/PhysRevApplied.12.014013. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.12.014013 (visited on 07/10/2023).

[15] Asser Elsayed et al. *Low charge noise quantum dots with industrial CMOS manufacturing*. arXiv:2212.06464 [cond-mat, physics:quant-ph]. Dec. 2022. DOI: 10.48550/arXiv.2212.06464. URL: http://arxiv.org/abs/2212.06464 (visited on 12/11/2023).

[16] Davide Degli Esposti et al. “Wafer-scale low-disorder 2DEG in 28Si/SiGe without an epitaxial Si cap”. en. In: *Applied Physics Letters* 120.18 (May 2022), p. 184003. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0088576. URL: https://pubs.aip.org/apl/article/120/18/184003/2833621/Wafer-scale-low-disorder-2DEG-in-28Si-SiGe-without (visited on 07/10/2023).

[17] Brian Paquelet Wuetz et al. “Reducing charge noise in quantum dots by using thin silicon quantum wells”. en. In: *Nature Communications* 14.1 (Mar. 2023), p. 1385. ISSN: 2041-1723. DOI: 10.1038/s41467-023-36951-w. URL: https://www.nature.com/articles/s41467-023-36951-w (visited on 12/14/2023).

[18] M. G. Borselli et al. “Measurement of valley splitting in high-symmetry Si/SiGe quantum dots”. en. In: *Applied Physics Letters* 98.12 (Mar. 2011), p. 123118. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.3569717. URL: https://pubs.aip.org/apl/article/98/12/123118/340062/Measurement-of-valley-splitting-in-high-symmetry (visited on 07/10/2023).

[19] P. G. Evans et al. “Nanoscale Distortions of Si Quantum Wells in Si/SiGe Quantum-Electronic Heterostructures”. en. In: *Advanced Materials* 24.38 (Oct. 2012), pp. 5217–5221. ISSN: 09359648. DOI: 10.1002/adma.201201833. URL: https://onlinelibrary.wiley.com/doi/10.1002/adma.201201833 (visited on 07/10/2023).

[20] D. M. Zajac et al. “A reconfigurable gate architecture for Si/SiGe quantum dots”. en. In: *Applied Physics Letters* 106.22 (June 2015), p. 223507. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.4922249. URL: https://pubs.aip.org/apl/article/106/22/223507/27629/A-reconfigurable-gate-architecture-for-Si-SiGe (visited on 07/10/2023).

[21] Zhan Shi et al. “Tunable singlet-triplet splitting in a few-electron Si/SiGe quantum dot”. en. In: *Applied Physics Letters* 99.23 (Dec. 2011), p. 233108. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.3666232. URL: https://pubs.aip.org/apl/article/99/23/233108/282245/Tunable-singlet-triplet-splitting-in-a-few (visited on 07/10/2023).

[22] P. Scarlino et al. “Dressed photon-orbital states in a quantum dot: Intervalley spin resonance”. en. In: *Physical Review B* 95.16 (Apr. 2017), p. 165429. ISSN: 2469-9950, 2469-9969. DOI: 10.1103/PhysRevB.95.165429. URL: http://link.aps.org/doi/10.1103/PhysRevB.95.165429 (visited on 07/10/2023).

[23] Rifat Ferdous et al. “Valley dependent anisotropic spin splitting in silicon quantum dots”. en. In: *npj Quantum Information* 4.1 (June 2018), p. 26. ISSN: 2056-6387. DOI: 10.1038/s41534-018-0075-1. URL: https://www.nature.com/articles/s41534-018-0075-1 (visited on 07/10/2023).

[24] X. Mi et al. “High-Resolution Valley Spectroscopy of Si Quantum Dots”. en. In: *Physical Review Letters* 119.17 (Oct. 2017), p. 176803. ISSN: 0031-9007, 1079-7114. DOI: 10.1103/PhysRevLett.119.176803. URL: https://link.aps.org/doi/10.1103/PhysRevLett.119.176803 (visited on 07/10/2023).

[25] X. Mi et al. “Circuit quantum electrodynamics architecture for gate-defined quantum dots in silicon”. en. In: *Applied Physics Letters* 110.4 (Jan. 2017), p. 043502. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.4974536. URL: https://pubs.aip.org/apl/article/110/4/043502/33909/Circuit-quantum-electrodynamics-architecture-for (visited on 09/01/2023).

[26] X. Mi, S. Kohler, and J. R. Petta. “Landau-Zener interferometry of valley-orbit states in Si/SiGe double quantum dots”. In: *Physical Review B* 98.16 (Oct. 2018), p. 161404. DOI: 10.1103/PhysRevB.98.161404. URL: https://link.aps.org/doi/10.1103/PhysRevB.98.161404 (visited on 08/12/2022).

[27] E. Kawakami et al. “Electrical control of a long-lived spin qubit in a Si/SiGe quantum dot”. en. In: *Nature Nanotechnology* 9.9 (Sept. 2014), pp. 666–670. ISSN: 1748-3387, 1748-3395. DOI: 10.1038/nnano.2014.153. URL: https://www.nature.com/articles/nnano.2014.153 (visited on 07/10/2023).

[28] Mark Friesen et al. “Valley splitting theory of SiGe/Si/SiGe quantum wells”. In: *Phys. Rev. B* 75 (11 Mar. 2007), p. 115318. DOI: 10.1103/PhysRevB.75.115318. URL: https://link.aps.org/doi/10.1103/PhysRevB.75.115318.

[29] M. Lodari et al. “Valley Splitting in Silicon from the Interference Pattern of Quantum Oscillations”. In: *Physical Review Letters* 128.17 (Apr. 2022), p. 176603. DOI: 10.1103/PhysRevLett.128.176603. URL: https://link.aps.org/doi/10.1103/PhysRevLett.128.176603 (visited on 07/10/2023).

[30] Brian Paquelet Wuetz et al. “Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots”. en. In: *Nature Communications* 13.1 (Dec. 2022), p. 7730. ISSN: 2041-1723. DOI: 10.1038/s41467-022-35458-0. URL: https://www.nature.com/articles/s41467-022-35458-0 (visited on 07/10/2023).

[31] Merritt P. Losert et al. “Practical strategies for enhancing the valley splitting in Si/SiGe quantum wells”. In: *Physical Review B* 108.12 (Sept. 2023), p. 125405. DOI: 10.1103/PhysRevB.108.125405. URL: https://link.aps.org/doi/10.1103/PhysRevB.108.125405 (visited on 09/06/2023).

[32] Thomas McJunkin et al. “Valley splittings in Si/SiGe quantum dots with a germanium spike in the silicon well”. In: *Physical Review B* 104.8 (Aug. 2021), p. 085406. DOI: 10.1103/PhysRevB.104.085406. URL: https://link.aps.org/doi/10.1103/PhysRevB.104.085406 (visited on 09/06/2023).

[33] Yi Feng and Robert Joynt. “Enhanced valley splitting in Si layers with oscillatory Ge concentration”. In: *Physical Review B* 106.8 (Aug. 2022), p. 085304. DOI: 10.1103/PhysRevB.106.085304. URL: https://link.aps.org/doi/10.1103/PhysRevB.106.085304 (visited on 09/06/2023).

[34] Thomas McJunkin et al. “SiGe quantum wells with oscillating Ge concentrations for quantum dot qubits”. en. In: *Nature Communications* 13.1 (Dec. 2022), p. 7777. ISSN: 2041-1723. DOI: 10.1038/s41467-022-35510-z. URL: https://www.nature.com/articles/s41467-022-35510-z (visited on 08/29/2023).

[35] Lijun Zhang et al. “Genetic design of enhanced valley splitting towards a spin qubit in silicon”. en. In: *Nature Communications* 4.1 (Sept. 2013), p. 2396. ISSN: 2041-1723. DOI: 10.1038/ncomms3396. URL: https://www.nature.com/articles/ncomms3396 (visited on 09/06/2023).

[36] Samuel F. Neyens et al. “The critical role of substrate disorder in valley splitting in Si quantum wells”. en. In: *Applied Physics Letters* 112.24 (June 2018), p. 243107. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.5033447. URL: https://pubs.aip.org/apl/article/112/24/243107/35358/The-critical-role-of-substrate-disorder-in-valley (visited on 09/06/2023).

[37] Gang Wang et al. “Origin of giant valley splitting in silicon quantum wells induced by superlattice barriers”. In: *Physical Review B* 105.16 (Apr. 2022), p. 165308. DOI: 10.1103/PhysRevB.105.165308. URL: https://link.aps.org/doi/10.1103/PhysRevB.105.165308 (visited on 09/06/2023).

[38] Arne Hollmann et al. “Large, Tunable Valley Splitting and Single-Spin Relaxation Mechanisms in a Si/SiGe Quantum Dot”. In: *Physical Review Applied* 13.3 (Mar. 2020), p. 034068. DOI: 10.1103/PhysRevApplied.13.034068. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.13.034068 (visited on 02/04/2022).

[39] X. Mi et al. “Magnetotransport studies of mobility limiting mechanisms in undoped Si/SiGe heterostructures”. In: *Physical Review B* 92.3 (July 2015), p. 035304. DOI: 10.1103/PhysRevB.92.035304. URL: https://link.aps.org/doi/10.1103/PhysRevB.92.035304 (visited on 08/01/2023).

[40] B. Paquelet Wuetz et al. “Multiplexed quantum transport using commercial off-the-shelf CMOS at sub-kelvin temperatures”. In: *npj Quantum Information* 6.6 (May 2020), p. 43. ISSN: 2056-6387. DOI: 10.1038/s41534-020-0274-4. URL: https://www.nature.com/articles/s41534-020-0274-4 (visited on 12/21/2021).

[41] Edward H. Chen et al. “Detuning Axis Pulsed Spectroscopy of Valley-Orbital States in Si / Si - Ge Quantum Dots”. en. In: *Physical Review Applied* 15.4 (Apr. 2021), p. 044033. ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.15.044033. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.15.044033 (visited on 02/04/2022).

[42] A. Gold. “Barrier penetration effects for electrons in quantum wells: screening, mobility, and shallow impurity states”. en. In: *Zeitschrift for Physik B Condensed Matter* 74.1 (Mar. 1989), pp. 53–65. ISSN: 0722-3277, 1434-6036. DOI: 10.1007/BF01307238. URL: http://link.springer.com/10.1007/BF01307238 (visited on 09/25/2023).

[43] K. Ismail et al. “Identification of a Mobility-Limiting Scattering Mechanism in Modulation-Doped Si/SiGe Heterostructures”. In: *Physical Review Letters* 73.25 (Dec. 1994), pp. 3447–3450. DOI: 10.1103/PhysRevLett.73.3447. URL: https://link.aps.org/doi/10.1103/PhysRevLett.73.3447 (visited on 07/10/2023).

[44] Ondrej Dyck et al. “Accurate Quantification of Si/SiGe Interface Profiles via Atom Probe Tomography”. en. In: *Advanced Materials Interfaces* 4.21 (Nov. 2017), p. 1700622. ISSN: 21967350. DOI: 10.1002/admi.201700622. URL: https://onlinelibrary.wiley.com/doi/10.1002/admi.201700622 (visited on 06/16/2023).

[45] Xiao Xue et al. “Quantum logic with spin qubits crossing the surface code threshold”. en. In: *Nature* 601.7893 (Jan. 2022), pp. 343–347. ISSN: 0028-0836, 1476-4687. DOI: 10.1038/s41586-021-04273-w. URL: https://www.nature.com/articles/s41586-021-04273-w (visited on 07/12/2023).

[46] Akito Noiri et al. “Fast universal quantum gate above the fault-tolerance threshold in silicon”. en. In: *Nature* 601.7893 (Jan. 2022), pp. 338–342. ISSN: 0028-0836, 1476-4687. DOI: 10.1038/s41586-021-04182-y. URL: https://www.nature.com/articles/s41586-021-04182-y (visited on 07/12/2023).

[47] Kentaro Kutsukake et al. “On the origin of strain fluctuation in strained-Si grown on SiGe-on-insulator and SiGe virtual substrates”. en. In: *Applied Physics Letters* 85.8 (Aug. 2004), pp. 1335–1337. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.1784036. URL: https://pubs.aip.org/apl/article/85/8/1335/902743/On-the-origin-of-strain-fluctuation-in-strained-Si (visited on 12/08/2023).

[48] L. H. Wong et al. “Determination of Raman Phonon Strain Shift Coefficient of Strained Silicon and Strained SiGe”. en. In: *Japanese Journal of Applied Physics* 44.11R (Nov. 2005), p. 7922. ISSN: 1347-4065. DOI: 10.1143/JJAP.44.7922. URL: https://iopscience.iop.org/article/10.1143/JJAP.44.7922/meta (visited on 07/10/2023).

[49] Lucas E. A. Stehouwer et al. “Germanium wafers for strained quantum wells with low disorder”. en. In: *Applied Physics Letters* 123.9 (Aug. 2023), p. 092101. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0158262. URL: https://pubs.aip.org/apl/article/123/9/092101/2908280/Germanium-wafers-for-strained-quantum-wells-with (visited on 12/08/2023).

[50] L. A. Tracy et al. “Observation of percolation-induced two-dimensional metal-insulator transition in a Si MOSFET”. en. In: *Physical Review B* 79.23 (June 2009), p. 235307. ISSN: 1098-0121, 1550-235X. DOI: 10.1103/PhysRevB.79.235307. URL: https://link.aps.org/doi/10.1103/PhysRevB.79.235307 (visited on 07/14/2023).

[51] D. Laroche et al. “Scattering mechanisms in shallow undoped Si/SiGe quantum wells”. In: *AIP Advances* 5.10 (Oct. 2015), p. 107106. DOI: 10.1063/1.4933026. URL: https://aip.scitation.org/doi/10.1063/1.4933026 (visited on 02/08/2022).

[52] Yi Huang and Sankar Das Sarma. “Understanding disorder in Silicon quantum computing platforms: Scattering mechanisms in Si/SiGe quantum wells”. In: *Preprint at https://arxiv.org/abs/2312.07717* (Dec. 2023). URL: http://arxiv.org/abs/2312.07717 (visited on 01/30/2024).

[53] F. K. Unseld et al. “A 2D quantum dot array in planar 28Si/SiGe”. en. In: *Applied Physics Letters* 123.8 (Aug. 2023), p. 084002. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0160847. URL: https://pubs.aip.org/apl/article/123/8/084002/2907709/A-2D-quantum-dot-array-in-planar-28Si-SiGe (visited on 09/01/2023).

[54] Marcel Meyer et al. “Electrical Control of Uniformity in Quantum Dot Devices”. en. In: *Nano Letters* 23.7 (Apr. 2023), pp. 2522–2529. ISSN: 1530-6984, 1530-6992. DOI: 10.1021/acs.nanolett.2c04446. URL: https://pubs.acs.org/doi/10.1021/acs.nanolett.2c04446 (visited on 07/10/2023).

[55] Elliot J. Connors et al. “Low-frequency charge noise in Si/SiGe quantum dots”. en. In: *Physical Review B* 100.16 (Oct. 2019), p. 165305. ISSN: 2469-9950, 2469-9969. DOI: 10.1103/PhysRevB.100.165305. URL: https://link.aps.org/doi/10.1103/PhysRevB.100.165305 (visited on 07/10/2023).

[56] Mario Lodari et al. “Low percolation density and charge noise with holes in germanium”. In: *Materials for Quantum Technology* 1.1 (Mar. 2021), p. 011002. ISSN: 2633-4356. DOI: 10.1088/2633-4356/abcd82. URL: https://iopscience.iop.org/article/10.1088/2633-4356/abcd82 (visited on 07/10/2023).

[57] P. Dutta, P. Dimon, and P. M. Horn. “Energy Scales for Noise Processes in Metals”. In: *Physical Review Letters* 43.9 (Aug. 1979), pp. 646–649. DOI: 10.1103/PhysRevLett.43.646. URL: https://link.aps.org/doi/10.1103/PhysRevLett.43.646 (visited on 08/08/2023).

[58] Seongjin Ahn, S. Das Sarma, and J. P. Kestner. “Microscopic bath effects on noise spectra in semiconductor quantum dot qubits”. In: *Physical Review B* 103.4 (Jan. 2021), p. L041304. DOI: 10.1103/PhysRevB.103.L041304. URL: https://link.aps.org/doi/10.1103/PhysRevB.103.L041304 (visited on 06/20/2023).

[59] Brennan Undseth et al. “Hotter is easier: unexpected temperature dependence of spin qubit frequencies”. In: *Preprint at https://arxiv.org/abs/2304.12984* (Apr. 2023). URL: http://arxiv.org/abs/2304.12984 (visited on 09/01/2023).

[60] H. Ekmel Ercan, S. N. Coppersmith, and Mark Friesen. “Strong electron-electron interactions in Si/SiGe quantum dots”. In: *Physical Review B* 104.23 (Dec. 2021), p. 235302. DOI: 10.1103/PhysRevB.104.235302. URL: https://link.aps.org/doi/10.1103/PhysRevB.104.235302 (visited on 08/28/2023).

[61] J. P. Dodson et al. “How Valley-Orbit States in Silicon Quantum Dots Probe Quantum Well Interfaces”. In: *Physical Review Letters* 128.14 (Apr. 2022), p. 146802. DOI: 10.1103/PhysRevLett.128.146802. URL: https://link.aps.org/doi/10.1103/PhysRevLett.128.146802 (visited on 07/10/2023).

[62] M. G. Borselli et al. “Pauli spin blockade in undoped Si/SiGe two-electron double quantum dots”. en. In: *Applied Physics Letters* 99.6 (Aug. 2011), p. 063109. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.3623479. URL: https://pubs.aip.org/apl/article/99/6/063109/341601/Pauli-spin-blockade-in-undoped-Si-SiGe-two (visited on 09/06/2023).

[63] Mats Volmer et al. “Mapping of valley-splitting by conveyor-mode spin-coherent electron shuttling”. In: *arXiv preprint arXiv:2312.17694* (2023).

[64] J. P. Dismukes, L. Ekstrom, and R. J. Paff. “Lattice Parameter and Density in Germanium-Silicon Alloys [1]”. en. In: *The Journal of Physical Chemistry* 68.10 (Oct. 1964), pp. 3021–3027. ISSN: 0022-3654, 1541-5740. DOI: 10.1021/j100792a049. URL: https://pubs.acs.org/doi/abs/10.1021/j100792a049 (visited on 07/17/2023).

[65] F. Pezzoli et al. “Phonon strain shift coefficients in Si1-xGex alloys”. en. In: *Journal of Applied Physics* 103.9 (May 2008), p. 093521. ISSN: 0021-8979, 1089-7550. DOI: 10.1063/1.2913052. URL: https://pubs.aip.org/aip/jap/article/899226 (visited on 07/17/2023).

[66] F. Cerdeira et al. “Stress-Induced Shifts of First-Order Raman Frequencies of Diamond- and Zinc-Blende-Type Semiconductors”. en. In: *Physical Review B* 5.2 (Jan. 1972), pp. 580–593. ISSN: 0556-2805. DOI: 10.1103/PhysRevB.5.580. URL: https://link.aps.org/doi/10.1103/PhysRevB.5.580 (visited on 07/17/2023).

[67] B. L. Welch. “THE GENERALIZATION OF ‘STUDENT’S’ PROBLEM WHEN SEVERAL DIFFERENT POPULATION VARLANCES ARE INVOLVED”. en. In: *Biometrika* 34.1-2 (1947), pp. 28–35. ISSN: 0006-3444, 1464-3510. DOI: 10.1093/biomet/34.1-2.28. URL: https://academic.oup.com/biomet/article-lookup/doi/10.1093/biomet/34.1-2.28 (visited on 07/20/2023).

7

DISCUSSION AND OUTLOOK

Good writing ends strong.

Steven Pincker

Over the last four years, electron spin qubits in Si/SiGe heterostructures have progressed in multiple directions. The efforts of the community have been focusing on scaling the quantum dot devices in two dimensions [1], demonstrating distant photon-mediated two-qubit logic [2], implementing error correction schemes [3], analyzing the effect noise correlation in dense arrays [4, 5], and implementing long distance [6] and high fidelity spin shuttling [7]. Although most of these proof-of-principle demonstrations still used heterostructures and devices fabricated in academic cleanrooms, we have started to see the first spin qubit devices on Si/SiGe heterostructures fabricated in semiconductor foundries. Above all, this proves the ability of the semiconductor foundries to grow high-quality Si/SiGe heterostructures and the full compatibility of this platform with the advanced semiconductor manufactory process. The recent efforts undertaken by Intel [8, 9], IMEC [10] and Infineon [11] are encouraging examples in the transition from academic hero-devices to reliable industrial devices that leverage the knowledge of the semiconductor industry.

Here, we report on the advancements of the Si/SiGe heterostructure grown at TU Delft via RP-CVD, which is the same technique used by the semiconductor industry. The studies focused on improving the disorder and electrostatics chapter 4, the charge-noise chapter 5, and the valley splitting chapter 6. These are three of the most important parameters in qualifying a Si/SiGe heterostructure hosting electron spin qubits. In chapter 4, we exploit the low-temperature passivation of the topmost SiGe spacer and demonstrate lower disorder and an improved uniformity on a wafer scale compared to the more traditional growth of a sacrificial Si cap. The uniformity of the electrostatic potential is fundamental in accumulation mode devices to ease the tuning and reliability of quantum dots. Here, we also demonstrate that such heterostructures can sustain a larger maximum electric field, which is one of the underlying mechanisms also driving the Valley splitting. In chapter 5, we draw our attention to the thickness of the Si quantum well and the dislocation arising at the interface with the SiGe buffer. We prove that even if the epitaxial Si/SiGe interface ensures a very low level of disorder, dislocations at such interface still substantially contribute to the charge noise experienced by the electrons trapped in the Si quantum well. We continue the analysis in chapter 6 where we fine-tune the thickness of the Si quantum well and demonstrate Si/SiGe heterostructure with low disorder and high valley splitting. In contrast with other methods relying on increasing the alloy scattering by introducing Ge inside the quantum well to enhance the valley splitting at the cost of increased disorder, our heterostructures can show respectable values of valley splitting and high mobility at the same time. In chapter 6, we also raise awareness of the strain fluctuation arising from the virtual substrate and the length of the roughness arising from the cross-hatch pattern, which will probably be of interest in larger micrometre-scale devices.

Besides the spin qubit groups at QuTech and TU Delft, the heterostructures described in this thesis have been used by a growing number of research groups, including the groups of Seigo Tarucha (RIKEN - Japan), Dohun Kim (Seoul - South Korea), and Lars Schreiber (Aachen - Germany). This gives us confidence about the reproducibility of the results independently of the specific designs and fabrication conditions. In the following, we highlight a few directions we think necessary to address when scaling to larger arrays in the coming years.

7.1. NOISE AND ADDRESSABILITY

Gate-defined quantum dots use the electric field generated by the gate electrodes to control the spin of a single electron. In principle, the spin degree of freedom does not couple directly with the electric fields. However, in all the spin qubits exploiting electric dipole spin resonance (EDSR) control, there is always a spin-to-charge coupling mechanism that allows for manipulating the spin state via an electric field. This greatly eases the spin control and means that any electric noise, *i.e.*, the charge noise, can couple in and reduce the spin coherence. In Si/SiGe heterostructures, this spin-to-charge coupling is provided by the gradient field of the micromagnet. The gradient depends on the geometrical dimension of the micromagnets and the distance between the electrons in the quantum well and the micromagnet itself. In this sense, Si/SiGe heterostructures stand compared to other platforms, exploiting intrinsic spin-orbit coupling, for example, thanks to the possibility of engineering this gradient by acting on specific parameters such as the depth of the quantum well and the thickness of the dielectric in the gate stack. We can, therefore, choose the balance between effective control and sensitivity to electrostatic noise.

While the careful engineering of this balance will be paramount in the future of electron spin qubits, in this thesis, we report on a few methods that ultimately reduce charge noise in semiconductor quantum dots. In chapter 4, we focus our attention on the topmost interface of the epitaxial heterostructure with the amorphous dielectric layers and combine the results with the reduction in the quantum well thickness in chapter 5 to improve the low-frequency charge noise. We explain the reduction of low frequency-charge noise as a consequence of the reduction of remote impurities at the semiconductor/dielectric interface and misfit dislocations at the quantum well epitaxial interface. Besides these, other parameters of the heterostructure and material stack could also be explored to improve the electric noise environment. As said before, increasing the distance between the electrons and the micromagnet directly affects the magnetic gradient used for the qubit control and, therefore, makes them less sensitive to electric fluctuations. At the same time, it also moves the electrons away from impurities and charges trapped in the dielectric and places them in a quieter environment. Next, carbon and oxygen contamination are also known to be strong scattering sources for electrons in the Si quantum well, limiting mobility, forming spurious and unwanted quantum dots and possibly increasing charge noise. Here, increasing the temperature of the growth of the SiGe spacer might be beneficial, especially now that the interfaces to the quantum well are voluntarily broadened to increase the alloy scattering. Ultimately, the careful engineering of the dielectric and gate stack will be fundamental to ensure a very low density of interface traps and further lower the charge noise level. Industry-fabricated devices already show effort in this direction [9].

As we explored in chapter 5, reducing charge noise also means that the average number of two-level systems (TLS) generating the noise and interacting with the quantum dots enters a regime where the noise power spectral density assumes a well-defined $1/f^2$ behaviour that permits the identification of the contribution of single TLSs. In this regime, the remaining TLSs could probably be tuned with the same electric gates used to operate the qubits in a weak interaction regime and ultimately increase coherence.

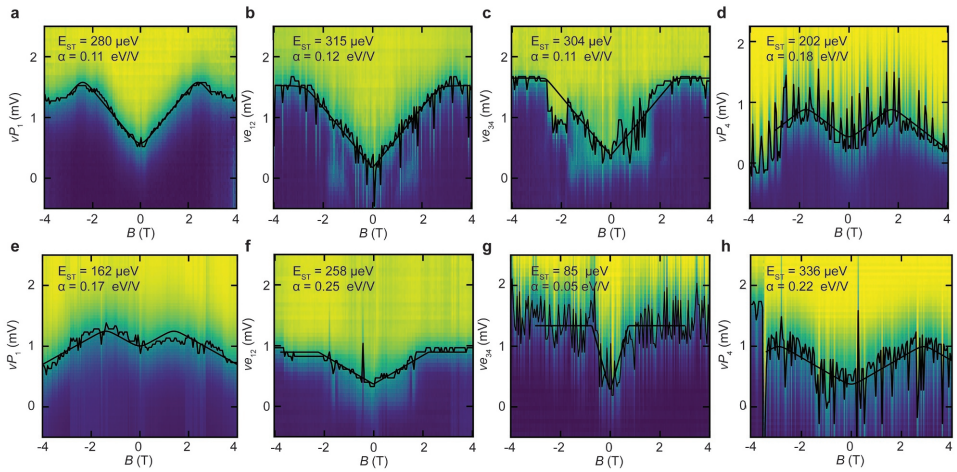


Figure 7.1: **Magnetospectroscopy of two four-dots devices.** From **a** to **d** magneto-spectroscopy measurements of the four dots (P1 to P4) of a linear four-dot device as a function of the external parallel magnetic field (B). **e** to **h** magneto-spectroscopy measurements for the four dots of a lithographically identical device as for **a** to **d**. For the external dots P1 and P4 (**a** and **d**) close to the electron reservoir we scan the $1e \rightarrow 2e$ addition line loading from the sensing dot, while for the inner dots P2 and P3 (**b** and **c**) we scan the inter-dot transition $(1,1) \rightarrow (0,2)$. The Singlet-Triplet splitting (E_{ST}) extracted from the fit of the curves to the theoretical models and gate lever arm (α) extracted from the slope of the trace as a function of the magnetic field are shown. These measurements confirm the high single triplet energy splitting values independently of specific fabrication runs and wafer growth.

7

7.2. VALLEYS AND SINGLE-TRIPLET SPLITTING

Electron spin qubits in Si suffer from the quasi-degeneracy of the conduction band, known as valleys. The energy splitting between these two states can widely range from 20 to 300 μeV even in the same device for dots a few hundred nanometers apart. The current theories of valley splitting predict a distribution of values starting from zero with an average that depends on the characteristics of the heterostructure and confinement experienced by the electrons in the quantum well. Multiple heterostructures [12] have, therefore, been proposed to increase the average of the valley splitting distribution and avoid the occurrence of very low values.

In this thesis, we report many surprisingly high values of valley splitting. Moreover, we did not encounter any occurrence of low values that could prevent the qubit operation, *i.e.*, below 100 μeV. In chapter 6 we report on the characterization of two different devices both showing high values of valley splitting on multiple quantum dots. Figure 7.1 confirm these findings on another device fabricated on a different but nominally identical heterostructure, which gives us confidence in the robustness of our results independently of the specific growth and fabrication conditions.

In this thesis, we use magnetospectroscopy of the 2-electron transition to characterize the Singlet-Triplet splitting of the quantum dots. This is a lower bound, and it converges to the single-electron valley splitting in the case of tightly confined quantum dots in which the exchange interaction is much smaller than the single-electron energy

scales. However, precise measurements of the single electron valley splitting in their heterostructure are missing. This could be done with other spectroscopy techniques using only single electron occupation, such as the pulsed spectroscopy [13] and the detuning axis pulsed spectroscopy [14], which will also give information about the confinement and the orbital energy. Although precise, the measurements of single quantum dots do not allow us to easily acquire enough statistics to fully sample the distribution of the valley splitting. In this case, shuttling [15, 16] has also emerged as a powerful tool for investigating the valley splitting distribution and finding the hotspots with very low values. Comparing such distribution with the theoretical prediction could ultimately shed light on the mechanism driving the valley splitting in these heterostructures.

7.3. FUTURE SI/SIGE HETEROSTRUCTURES

The main advantage of semiconductor spin qubits is that they can leverage the knowledge already developed by the advanced semiconductor industry. In this thesis, we highlight and improve multiple material metrics that ultimately affect single electron and qubit performances. We used metrics already used by the classical electronics community, such as mobility and percolation density, and metrics closer to the quantum information community, such as quantum mobility, charge noise and valley splitting. Still, the Si/SiGe heterostructures presented here are far from perfect, and there is room for improvement on multiple sides.

The full purification of the heterostructure is still desirable to place the qubit in a nuclear spin-free magnetic vacuum. While there is no physical impediment to its realization, it is important to be aware of the technological challenges in its pursuit. First, a new precursor bottle must be added to account for the purified ^{70}Ge and the CVD tool needs to be modified accordingly. Next, the new precursor gas has to match the purified Si to allow for the growth of both specimens simultaneously. In this sense, having a Si bottle with a high concentration (> 10%) is desirable to be able to sustain a reasonable flow while growing Si-rich SiGe substrates. This will also be necessary to grow fully purified quantum wells with a Ge concentration on the inside.

In chapter 6, we discuss the surface roughness arising from the threading dislocation network in the SiGe virtual substrate. This is a challenge to device integration in semiconductor foundries that is usually worked around by using chemical-mechanical polishing to flatten the surface before growing the topmost active layers. However, the strain fluctuation associated with the same dislocation network will remain and pose a critical challenge to address in scaling quantum dot arrays in the NISQ era beyond the micrometre scales.

BIBLIOGRAPHY

[1] F. K. Unseld et al. “A 2D quantum dot array in planar 28Si/SiGe”. en. In: *Applied Physics Letters* 123.8 (Aug. 2023), p. 084002. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/5.0160847. URL: https://pubs.aip.org/apl/article/123/8/084002/2907709/A-2D-quantum-dot-array-in-planar-28Si-SiGe (visited on 09/01/2023).

[2] Jurgen Dijkema et al. *Two-qubit logic between distant spins in silicon*. arXiv:2310.16805 [cond-mat, physics:quant-ph]. Oct. 2023. DOI: 10.48550/arXiv.2310.16805. URL: http://arxiv.org/abs/2310.16805 (visited on 10/29/2024).

[3] Kenta Takeda et al. “Quantum error correction with silicon spin qubits”. en. In: *Nature* 608.7924 (Aug. 2022), pp. 682–686. ISSN: 1476-4687. DOI: 10.1038/s41586-022-04986-6. URL: https://www.nature.com/articles/s41586-022-04986-6 (visited on 10/29/2024).

[4] J.S. Rojas-Arias et al. “Spatial noise correlations beyond nearest neighbors in 28 Si / Si-Ge spin qubits”. en. In: *Physical Review Applied* 20.5 (Nov. 2023), p. 054024. ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.20.054024. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.20.054024 (visited on 10/29/2024).

[5] J. Yoneda et al. “Noise-correlation spectrum for a pair of spin qubits in silicon”. en. In: *Nature Physics* 19.12 (Dec. 2023), pp. 1793–1798. ISSN: 1745-2481. DOI: 10.1038/s41567-023-02238-6. URL: https://www.nature.com/articles/s41567-023-02238-6 (visited on 10/29/2024).

[6] Ran Xue et al. “Si/SiGe QuBus for single electron information-processing devices with memory and micron-scale connectivity function”. en. In: *Nature Communications* 15.1 (Mar. 2024), p. 2296. ISSN: 2041-1723. DOI: 10.1038/s41467-024-46519-x. URL: https://www.nature.com/articles/s41467-024-46519-x (visited on 10/29/2024).

[7] Maxim De Smet et al. *High-fidelity single-spin shuttling in silicon*. arXiv:2406.07267 [cond-mat, physics:quant-ph]. June 2024. DOI: 10.48550/arXiv.2406.07267. URL: http://arxiv.org/abs/2406.07267 (visited on 10/29/2024).

[8] Samuel Neyens et al. “Probing single electrons across 300-mm spin qubit wafers”. en. In: *Nature* 629.8010 (May 2024), pp. 80–85. ISSN: 1476-4687. DOI: 10.1038/s41586-024-07275-6. URL: https://www.nature.com/articles/s41586-024-07275-6 (visited on 10/29/2024).

[9] Hubert C. George et al. *12-spin-qubit arrays fabricated on a 300 mm semiconductor manufacturing line*. arXiv:2410.16583 [cond-mat, physics:quant-ph]. Oct. 2024. DOI: 10.48550/arXiv.2410.16583. URL: http://arxiv.org/abs/2410.16583 (visited on 10/29/2024).

[10] Mohit P. Dalwadi. *Rapidly yawing spheroids in viscous shear flow: Emergent loss of symmetry*. arXiv:2409.01273 [cond-mat, physics:physics]. Sept. 2024. DOI: 10.48550/arXiv.2409.01273. URL: http://arxiv.org/abs/2409.01273 (visited on 10/29/2024).

[11] Till Huckemann et al. *Industrially fabricated single-electron quantum dots in Si/Si-Ge heterostructures*. arXiv:2410.16913 [cond-mat, physics:quant-ph]. Oct. 2024. DOI: 10.48550/arXiv.2410.16913. URL: http://arxiv.org/abs/2410.16913 (visited on 10/29/2024).

[12] Merritt P. Losert et al. "Practical strategies for enhancing the valley splitting in Si/SiGe quantum wells". In: *Physical Review B* 108.12 (Sept. 2023), p. 125405. DOI: 10.1103/PhysRevB.108.125405. URL: https://link.aps.org/doi/10.1103/PhysRevB.108.125405 (visited on 09/06/2023).

[13] J. M. Elzerman et al. "Excited-state spectroscopy on a nearly closed quantum dot via charge detection". en. In: *Applied Physics Letters* 84.23 (June 2004), pp. 4617–4619. ISSN: 0003-6951, 1077-3118. DOI: 10.1063/1.1757023. URL: https://pubs.aip.org/apl/article/84/23/4617/116707/Excited-state-spectroscopy-on-a-nearly-closed (visited on 11/04/2024).

[14] Edward H. Chen et al. "Detuning Axis Pulsed Spectroscopy of Valley-Orbital States in Si / Si - Ge Quantum Dots". en. In: *Physical Review Applied* 15.4 (Apr. 2021), p. 044033. ISSN: 2331-7019. DOI: 10.1103/PhysRevApplied.15.044033. URL: https://link.aps.org/doi/10.1103/PhysRevApplied.15.044033 (visited on 02/04/2022).

[15] Merritt P. Losert et al. *Strategies for enhancing spin-shuttling fidelities in Si/SiGe quantum wells with random-alloy disorder*. arXiv:2405.01832 [cond-mat]. Oct. 2024. DOI: 10.48550/arXiv.2405.01832. URL: http://arxiv.org/abs/2405.01832 (visited on 10/29/2024).

[16] Mats Volmer et al. "Mapping of valley splitting by conveyor-mode spin-coherent electron shuttling". en. In: *npj Quantum Information* 10.1 (June 2024), pp. 1–8. ISSN: 2056-6387. DOI: 10.1038/s41534-024-00852-7. URL: https://www.nature.com/articles/s41534-024-00852-7 (visited on 10/29/2024).

ACKNOWLEDGEMENTS

The work contained in this thesis could not have been possible without the numerous people I had the privilege to meet during the last four years, to whom I will always be grateful.

Giordano, I still remember the first time I arrived in Delft and met you outside of building 22 during one of the COVID-19 lockdowns. I will miss our yearly and more frequent energetic discussion. Thank you for giving me the chance to take responsibility beyond my sight and to make my own decisions. Even if it might have been overwhelming at times, it made me grow more than I could have hoped for. Thank you for giving me the chance to come to Delft. Going back, I would do it exactly the same way.

Lieven Thank you for being my promotor. I admire your ever-lasting calm and positive attitude and your ability to encourage a collaborative environment within the Spin-Qubit groups. I think everyone is very happy to be able to spend more and more time with you recently.

First and foremost, I would like to thank the friends of the breakfast club, **Pablo**, **Uri** and **Hanifa**, with whom I share too many WhatsApp groups and never breakfast.

Pablo, you have been coping with my being hetero-basic more than anyone, and I believe you managed to smooth it a bit. Thank you for being a great companion and listener. Talking with you has always been helpful. Thank you for all the bike rides, the brunches, the board games and the Spanish music.

Uri, we have been officemates from the very beginning and spent much time together travelling after conferences or just for holidays. You have always been a safe space to turn to in F235 and outside. Thank you for all the help that you gave me in setting up the new fridge and the time you spent debugging and discussing electronics, fridges, projects and experiments. I learned a lot from you, especially about the Catalan culture. I will keep eating 12 grapes every New Year.

Hanifa, I broke your couch and your arm, and yet you are still spending time with me. You have undoubtedly been the glue holding our small and large groups of friends. After spending three Christmass together, you have become family to me.

Nina, we started almost at the same time and shared a lot of cleanroom struggles. You have been supporting me and heard many of my complaints during the most difficult times of this PhD. Thank you for all the Sunday gossip and tea with cake. I will never forget you stealing the bottles of wine from the bar in Vegas.

I would like to thank all the members of "**The Scappuccinos**" who joined the group throughout the years, always creating a great environment and keeping the mood up even in the most problematic times. **Brian**, thank you for all the discussion and the training in my first year. You have greatly supported the development of the Si quantum wells. **Mario**, thanks for all the training in the cleanroom and time spent together on the AttoCube. Being with you was a lot of fun. **Vivi** and **Bea**, it was great to have you around in the first year. Thank you. **Luka**, thank you for the bouldering sessions and

tips. I am sure you will be doing great at Intel. **Alberto**, you have always been a source of chaos in the lab. Thank you for all the energy you brought and the ability to solve problems. I learned a lot from you about coding. I am happy to see the impact of the Qarpet project. **Lucas**, we shared a lot of struggles together at the beginning. I am happy to see the Ge wafers taking over and being used in more and more projects. It was fun to explore Friesland together. **Desa**, you can be extremely professional in the lab and be a lot of fun outside. I could not ask for a better trainee. I am sure you will manage F010 and the fabrication at best. **Cornelius**, you arrived at one of my PhD's busiest times and proved very independent. I really liked your ability to pursue your own ideas. I am happy to see that you are going with your PhD. **Karina** you are a very chaotic person yet precise in the cleanroom. I agree with you: "A good fabrication engineer is always a good cook". **Asser**, you taught us a lot of fun facts about Egypt. Your perspective on things is always surprising (inspiring). I am very happy that you took over the Malibu setup. I am sure you will do great with it. **Federico**, you joined the most advanced project and managed to fabricate the next-generation Qarpet in your first year. Good luck with the experiment. **Maia**, you have been around the spin qubit groups a lot. From the trip to Milan to the very recent one. I am sure you can use your knowledge at your best in Basel. **Luca**, I like your willingness to understand what is going on in depth. I am sure the CVD will be in good hands with you. **Vlad**, good luck with the CVD and the material characterization.

I would also like to thank all the SpinQubit people. **Brennan**, my snoring companion. We have been relegated to the same room. You are a great person to have around. **Irene**, since the first moment you joined the office, you brought great energy and a new couch. I am very grateful to have you behind me. **Daniel** joking with you has always been a lot of fun. Thank you for all the chats and walks with Mascott. **Kenji** You have a great ability to stay calm in any circumstance and take things not too seriously. I share your interest in the sources of noise in our Si/SiGe heterostructures and Terraforming Mars. I am happy to see you taking over with the ESR experiment. **Eline** We travelled to every conference together. I have many fun memories with you: the cheesecake, the gelato, the flowery swimsuit. I will never forget to stop every hour when we travel together by car. **Nicolino** You had a rough path in your first year but also learned a lot. Now, I can safely say that you are a complete debugging master. I will call you anytime my 50Hz noise will be a problem. **Tobias** (El-Pimentador), spending time with you in Spain has been fun. I am sure you will do great with the resonator project. **Barnaby**, you are a very strong biker and an incredibly easy-to-understand British English speaker. Keep practising your Italian accent. **Corentin**, thanks for all the tips about cables and suppliers. They have been extremely useful and saved me a lot of time. **Sander**, thank you for always answering all the programming questions, even multiple times the same ones and even the most basic. Thank you to all the SpinQubit people to be always ready to help and have a laugh together, **Florian**, **Liza**, **Xin**, **Maxim**, **Francesco**, **Chien-An**, **Valentin**, **Sasha**, **Marion**, **Stefano**, and **Setareh**.

Vicky, you are a spicy Spanish but fun to be around. Your ability to fall asleep as soon as you enter a car will always amaze me. I agree with you: Noto will always be my favourite place in Sicily.

I would also like to thank the new group of PhDs, the **high-schoolers**, that made the last months very entertaining. **Dario** We spent about six months together in QCLab3.

Thank you for the taralli and for participating and supporting all of my nonsense. I hope, if not instructive, it was at least fun for you. **Edmondo**, you caught up quickly, even if you arrived from a very different background. Thank you for sharing (in part) my sense of humour. **Chris**, you are very motivated and smart. I am sure you will do great in your PhD. **Michele**, you have a very good impression of people and are not afraid to defend your arguments. It is fun to have you around. **Zarije**, you are a very nice person. Keep being nice for the rest of your PhD. **Federico**, thanks for keeping these guys as civilized as possible.

I would also like to thank the old SpinQubit guard who helped me at the beginning and for a large part of my PhD. **Amir**, we used to discuss a lot at the beginning of my PhD. You taught me most of what I know about epitaxial growth. **Sergey**, I still remember when the implantation tool broke during my first year, and you calmly dismissed the news, saying: "No problem. We will find another solution". This optimism became my mantra. Thank you for all the help. Your willingness to help anyone in the cleanroom has inspired me. **Dave** Thank you for all the discussions about the H-termination and the oxidation of the Si cap or passivation layer. I would also like to thank all the members of the spin qubit fabrication team, **Delphine**, **Lara**, **Gertjan**, **Filiberto**, and **Stefan** for always being ready to share their knowledge and good tips of advice.

I would like to thank all the committee members for finding the time to read my thesis and participate in the defence ceremony: **Mark Friesen**, **Kristiaan De Greve**, **Anasua Chatterjee**, **Leonardo Di-Carlo**, and **Gary Steele** to be available as a reserve member. In particular, I would like to thank **Mark** and **Kristiaan** for finding the time to travel to Delft.

I would like to thank also all the people that QuTech and the building 22 gave me a chance to meet: **Julia**, **Nick**, **Tobi**, **Luise**, **Tim**, **Mariagrazia**, **Chris**, **Matteo**, **Gert**, **Eliana**, **Riccardo**, **Francesca**, and **Matteo**.

The life of an experimentalist is full of challenges that go beyond the scientific experiment, and that would be impossible to solve without great technical support. **Olaf** You taught me most of what I know about dilution refrigerators and cryogenic knowledge, from fixing the primary impedance of the Leiden fridge to all the many times we had problems. **Tom**, you helped me (who had never used an LD before) and the Blufors technicians (who had never installed an LD before) in the installation of the Malibu fridge. Thank you very much. Your calm attitude saved us. **Jason** thank you for the enthusiasm and your ability to jump on solutions, **Erik** thank you for all the help with the copper powder filters, **Vinud**, **Jelle**, **Siebe** thank you for all the times fighting with the water cooling lines and for all the help with the more heavy duties. I would also like to thank **Raymond**, **Raymond**, **Roy**, and **Berend** for sharing so much electronics knowledge and always being ready to advise for the best electronics to use. Even when the requirements of the experiment were far from clear. **Yannick**, **Kees** and **Sowimini** I have been bothering a lot in the last year. Thank you for all the discussion and explanation about PCB design and for consistently responding to my not-so-clear requests. I also want to thank **Nico** and **Tim** from the mechanical workshop to be always ready to put together a quick fix. I would also like to thank **Marja** and **Jenny** for all the support with shipments, customs control, orders, travel arrangements and any kind of questions. You helped me solve so many problems and saved me countless times. I would also like to thank **Rick** from the procurement of the TU Delft. I will never forget to include the VAT

in my orders. I want also to thank all the **Eugene**, **Pauline**, **Mark**, **Bas**, **Marinus**, **Marinus**, **Charles**, **Arnold**, **Anja**, and **Eshter**.

Un ringraziamento special va alle coinquilini di Accattostraat che hanno vissuto e sopportato molte delle storia degli ultimi anni. **Alberto** tu sei l'unica persona che conoscevo prima di arrivare a Delft ed anche chi mi ha consigliato di venire qui. Grazie per tutte le discussioni nerd che per fortuna o purtroppo si soon andate ampliando. **Vec** ti sei unita al gruppo del mattino. Grazie per la pazienza nel sopportare le mie conversazioni senza senso. **Ale**, grazie per essere sempre una presenza tranquillizzante della casa e per ridere ogni tanto alle mie battute. **Davide**, grazie della pazienza con le mie battute non sempre felici, **La Belen**, per avermi accolto in Professor Henkentstraat, **Manu**, per condividere la passione per il trash, **La Fede**, per essere la prenseza più drammatica della casa. **Lucy** sei stata praticamente una coinquilina acquisita. Ogni volta che eri in visita è sempra stato un piacere. **Il Cocchi** e **Ricky**.

Anche se la distanza di ha sparpagliato sempre di più negli ultimi anni un ringraziamento alla gente di Pisa che nonostante tutto è rimasta vicina **Emanuele**, **Luigi**, **Cappe**, **Vitto**, **Marco**, **Luca**, **Nicoletta**, **Tommaso**, **Stefano**, **Giovanni**, **Elisa**, **Dario**, e **Francesca**.

Un ringraziamento anche a tutti gli amici in Abruzzo che si sono lamentati sempre di non vedermi abbastanza spesso e che mi hanno sempre ricordato di essere educato ben al di sopra della mia intelligenza per farmi rimanere umile, **Alessandro**, **Edoardo**, **Valerio**, **Francesco**, **Filippo**, **Paolo**, **Giuseppe**, **Alberto**, **Stefano**, **Francesco**, **Filippo**, **Claudia**, e **Claudia**.

Un ringraziamento di cuore alla mia famiglia. A mia madre **Leda** e mia sorella **Sara** per il supporto e la fiducia costante nel corso degli anni e per la pazienza con il mio tornare a casa sempre più di rado. Un ringraziamento speciale alla zia **Sandra**. Sei stata il punto di riferimento scientifico della famiglia. Mi spiace non poterti avere qui oggi. Grazie di tutto il supporto, allo zio **Adriano** e allo zio **Nicola** e a tutti i cugini **Alessia**, **Aurora**, **Marco**, **Giacomo**, **Edoardo**, **Laura** e **Francesca**.

Curriculum Vitæ

Davide Degli Esposti

02-04-1995 Born in Teramo, Italy.

Education

2014–2017 Bachelor of Science in Physics
Univeristà di Pisa, Pisa

2017–2020 Master of Science in Physics
Università di Pisa, Pisa
Thesis: Suspended Titanium Nanowire Field-Effect-Transistor
Supervisor: dr. F. Giazotto

2018–2019 Erasmus student
KU Leuven, Leuven

2021–2025 PhD. Physics
Delft University of Technology, Delft
Thesis: Strained Silicon quantum wells for spin qubits
Promotor: prof. dr. ir. L.M.K. Vandersypen
Co-Promotor: dr. G. Scappucci

LIST OF PUBLICATIONS

10. L.E.A. Stehouwer, C.X. Yu, B. van Straaten, A. Tosato, V. John, **D. Degli Esposti**, A. Elsayed, D. Costa, S D. Oosterhout, N.W. Hendrickx, M. Veldhorst, F. Borsoi, G. Scappucci *Exploiting epitaxial strained germanium for scaling low noise spin qubits at the micron-scale*, arXiv preprint arXiv:2411.11526, (2024).

9. H. Sohn, J. Jung, J. Park, H. Jang, L.E.A. Stehouwer, **D. Degli Esposti**, G. Scappucci, D. Kim, *Application of zero-noise extrapolation-based quantum error mitigation to a silicon spin qubit*, arXiv preprint arXiv:2410.10339, (2024).

8. D. Costa, L.E.A. Stehouwer, Y. Huang, S. Martí-Sánchez, **D. Degli Esposti**, J. Arbiol, G. Scappucci, *Reducing disorder in Ge quantum wells by using thick SiGe barriers*, Applied Physics Letters **125**, 22 (2024).

7. **D. Degli Esposti**, L.E.A. Stehouwer, Ö. Gül, N. Samkharadze, C. Déprez, M. Meyer, I.N. Meijer, L. Tryputen, S. Karwal, M. Botifoll, J. Arbiol, S. V. Amitonov, L.M.K. Vandersypen, A. Sammak, M. Veldhorst, G. Scappucci, *Low disorder and high valley splitting in silicon*, npj Quantum Information **10** (1), 32 (2024).

6. J. Park, H. Jang, H. Sohn, J. Yun, Y. Song, B. Kang, L.E.A. Stehouwer, **D. Degli Esposti**, G. Scappucci, D. Kim *Passive and active suppression of transduced noise in silicon spin qubits*, arXiv preprint arXiv:2403.02666 (2024).

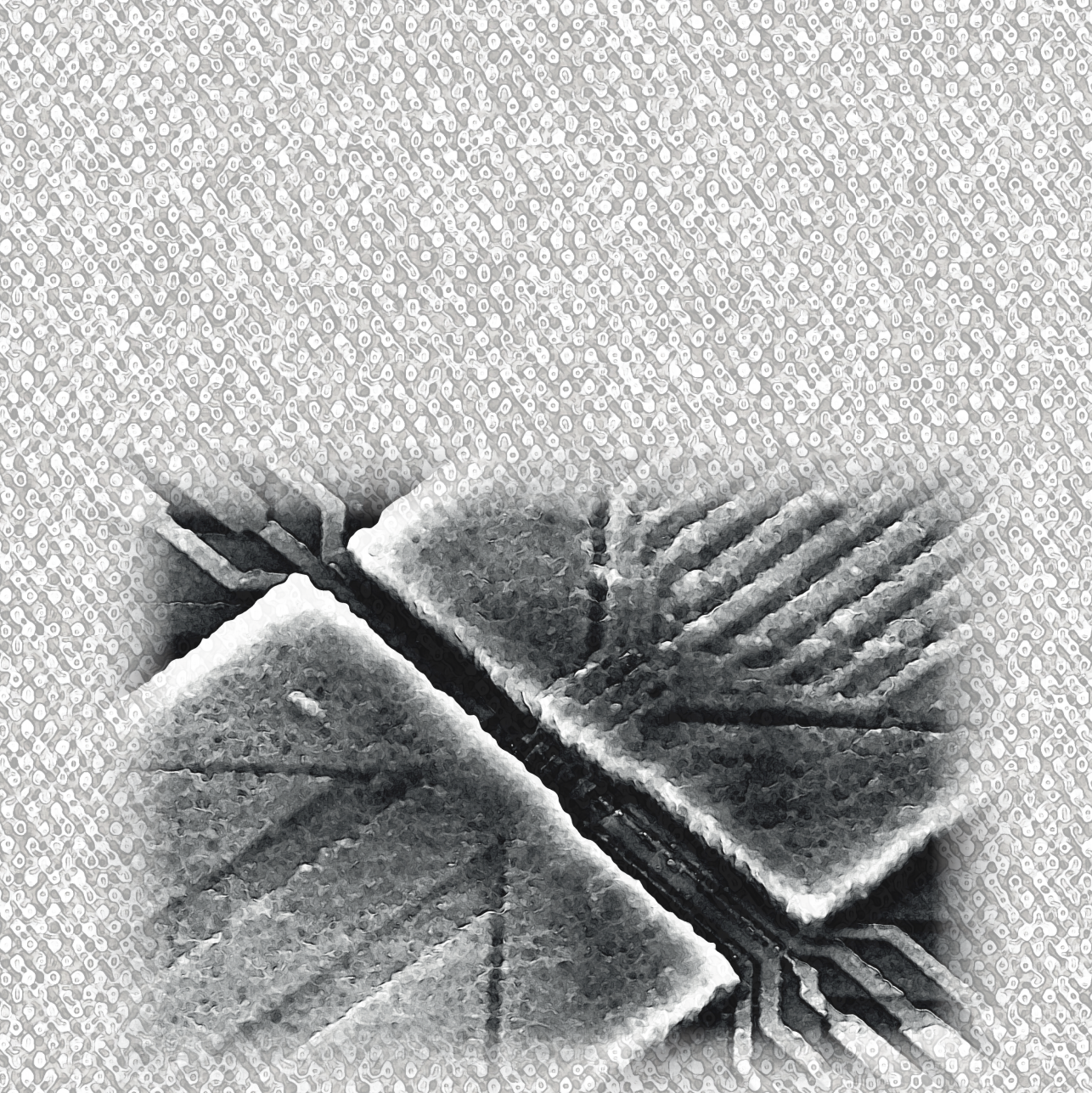
5. L.E.A. Stehouwer, A. Tosato, **D. Degli Esposti**, D. Costa, M. Veldhorst, A. Sammak, G. Scappucci, *Germanium wafers for strained quantum wells with low disorder*, Applied Physics Letters **123**, 9 (2023).

4. B. Undseth, O. Pietx-Casas, E. Raymenants, M. Mehmandoost, M. T Madzik, S. GJ Philips, S. L de Snoo, D. J Michalak, S. V Amitonov, L. Tryputen, B. Paquelet Wuetz, V. Fezzi, **D. Degli Esposti**, A. Sammak, G. Scappucci, L. MK Vandersypen, *Hotter is easier: unexpected temperature dependence of spin qubit frequencies*, PRX **17**, 891 (2023).

3. B. Paquelet Wuetz, **D. Degli Esposti**, A. J Zwerver, S. V Amitonov, M. Botifoll, J. Arbiol, A. Sammak, L. MK Vandersypen, M. Russ, G. Scappucci, *Reducing charge noise in quantum dots by using thin silicon quantum wells*, Nat. Com. **14**, 1385 (2023).

2. **D. Degli Esposti**, B. Paquelet Wuetz, V. Fezzi, M. Lodari, A. Sammak, G. Scappucci, *Wafer-scale low-disorder 2DEG in ^{28}Si/SiGe without an epitaxial Si cap*, Appl. Phys. Lett. **120**, 184003 (2022).

1. M. Rocci, D. De Simoni, C. Puglia, **D. Degli Esposti**, E. Strambini, V. Zannier, L. Sorba, F. Giazotto, *Gate-controlled suspended titanium nanobridge supercurrent transistor*, ACS nano, **14**(10), 12621-12628 (2020).



ISBN 978-94-6384-734-6